

# TLV320DAC3203 具有集成式耳机放大器的超低功率立体声音频编解码器

## 1 特性

- 具有100dB 信噪比 (SNR) 的立体声音频数模转换器 (DAC)
- 4.1mW立体声 48ksps 回放
- PowerTune™
- 大范围的信号处理选项
- Stereo Headphone Outputs
- 低功耗模拟旁路模式
- 可编程锁相环 (PLL)
- 集成型低压降稳压器 (LDO)
- 4mm x 4mm VQFN 和 2.7mm x 2.7mm DSGBA 封装

## 2 应用

- 移动手持机
- 通信
- 便携式计算机

## 3 描述

TLV320DAC3203 (有时是指DAC3203) 是一款灵活、低功耗、低压立体声音频编解码器, 此编解码器带有可编程输出、PowerTune 功能、固定的预定义且可参数化的信号处理块、集成型 PLL、集成 LDO 和灵活的数字接口。包括时钟和引脚复用在内的大范围基于寄存器的功率、输入/输出通道配置、增益、效应控制使得此器件能够精准的针对其目标应用。

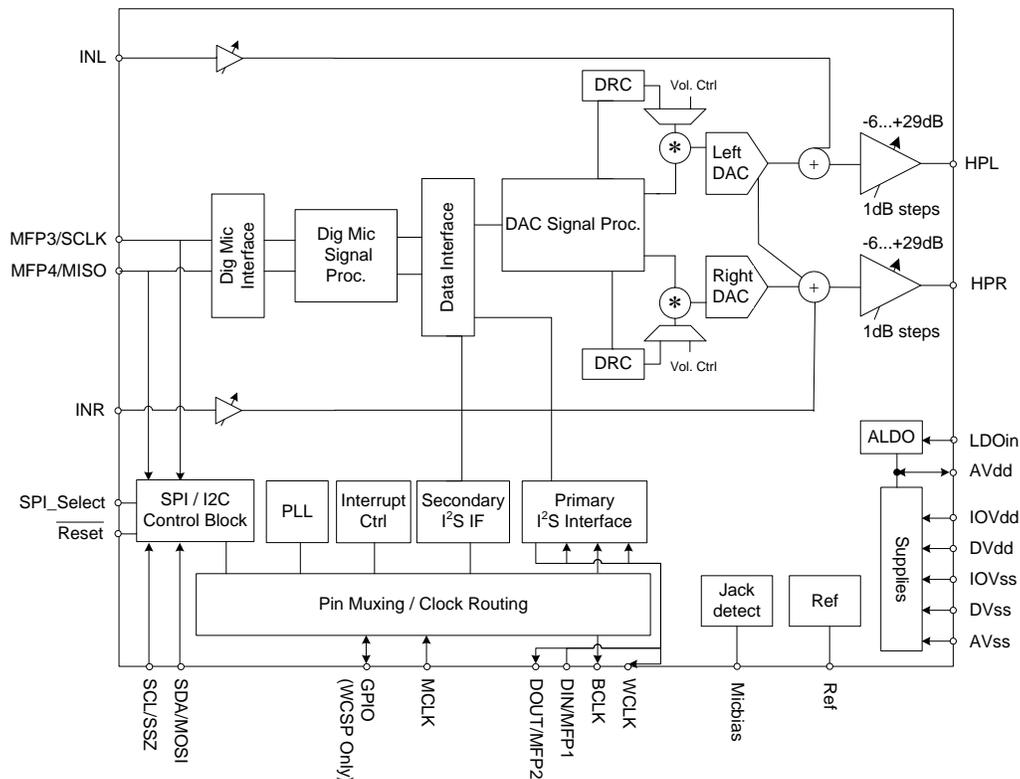
该器件采用 4mm x 4mm VQFN 和 2.7mm x 2.7mm DSGBA 封装。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TLV320DAC3203	VQFN (24)	4.00mm x 4.00mm
	DSBGA (25)	2.70mm x 2.70mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

简化方框图



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目录

1	特性 .....	1	7	Detailed Description .....	16
2	应用 .....	1	7.1	Overview .....	16
3	描述 .....	1	7.2	Functional Block Diagram .....	16
4	修订历史记录 .....	2	7.3	Feature Description .....	17
5	<b>Pin Configuration and Functions</b> .....	3	7.4	Device Functional Modes .....	22
6	<b>Specifications</b> .....	5	7.5	Register Maps .....	23
6.1	Absolute Maximum Ratings .....	5	8	<b>Application and Implementation</b> .....	26
6.2	ESD Ratings .....	5	8.1	Application Information .....	26
6.3	Recommended Operating Conditions .....	5	8.2	Typical Application .....	26
6.4	Thermal Information .....	6	9	<b>Power Supply Recommendations</b> .....	27
6.5	Electrical Characteristics, Bypass Outputs .....	6	10	<b>Layout</b> .....	28
6.6	Electrical Characteristics, Microphone Interface .....	6	10.1	Layout Guidelines .....	28
6.7	Electrical Characteristics, Audio Outputs .....	7	10.2	Layout Example .....	28
6.8	Electrical Characteristics, LDO .....	9	11	器件和文档支持 .....	29
6.9	Electrical Characteristics, Misc. .....	9	11.1	文档支持 .....	29
6.10	Electrical Characteristics, Logic Levels .....	9	11.2	接收文档更新通知 .....	29
6.11	Typical Timing Characteristics — Audio Data Serial Interface Timing (I <sup>2</sup> S) .....	10	11.3	社区资源 .....	29
6.12	Typical DSP Timing Characteristics .....	11	11.4	商标 .....	29
6.13	I <sup>2</sup> C Interface Timing .....	12	11.5	静电放电警告 .....	29
6.14	SPI Interface Timing (See 图 6) .....	13	11.6	术语表 .....	29
6.15	Typical Characteristics .....	14	12	机械、封装和可订购信息 .....	29

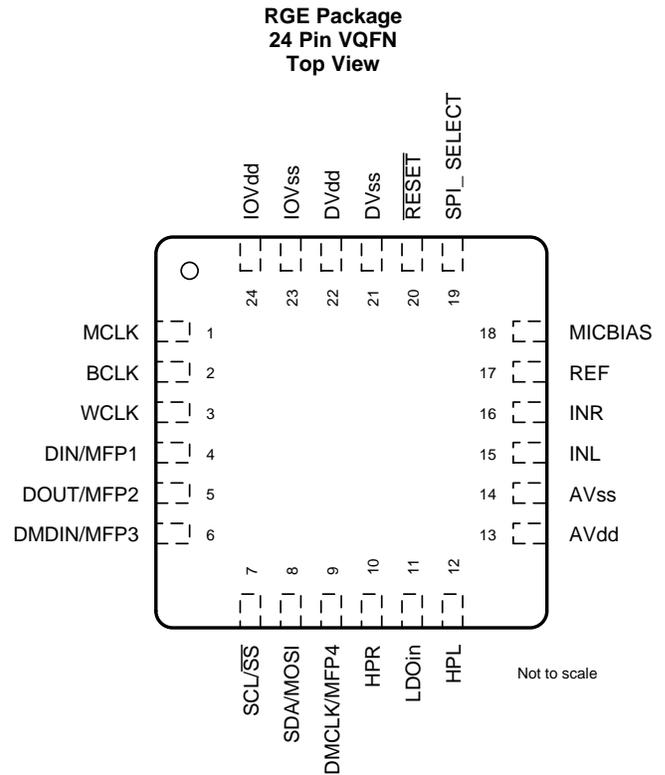
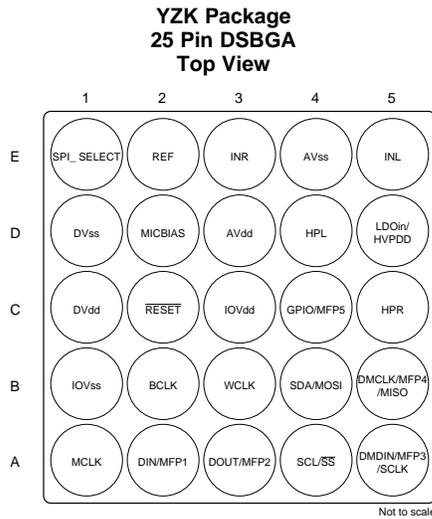
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (March 2017) to Revision B	Page
• Changed Description of pin 7 in the <i>Pin Functions</i> table .....	4
• Changed TYPE and Description of pin 8 in the <i>Pin Functions</i> table .....	4
• Changed pin 14 (ball E4) TYPE From: AVdd To: AVss in the <i>Pin Functions</i> table .....	4
• Changed pin 21 (ball D1) TYPE From: DVdd To: DVss in the <i>Pin Functions</i> table .....	4
• Changed pin 23 (ball B1) TYPE From: IOVdd To: IOVss in the <i>Pin Functions</i> table .....	4
• Changed ball C4 TYPE From: I To: I/O in the <i>Pin Functions</i> table .....	4

Changes from Original (May 2012) to Revision A	Page
• 将特性从“4mm x 4mm QFN 和 2.7mm x 2.7mm WCSP 封装”更改为“4mm x 4mm VQFN 和 2.7mm x 2.7mm DSGBA 封装” .....	1
• 添加了器件信息表、引脚配置和功能部分、ESD 额定值表、热性能信息表、详细说明部分、应用和实施部分、器件和文档支持以及机械、封装和可订购信息部分 .....	1
• Corrected the pin names of the RGE Package image .....	3

## 5 Pin Configuration and Functions



### Pin Functions

PIN		NAME	TYPE	DESCRIPTION
QFN PIN	WCSP BALL			
1	A1	MCLK	I	Master Clock Input
2	B2	BCLK	IO	Audio serial data bus (primary) bit clock
3	B3	WCLK	IO	Audio serial data bus (primary) word clock
4	A2	DIN/MFP1	I	Primary function Audio serial data bus data input Secondary function Digital Microphone Input General Purpose Input
5	A3	DOUT/MFP2	O	Primary Audio serial data bus data output Secondary General Purpose Output Clock Output INT1 Output INT2 Output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output

**Pin Functions (continued)**

PIN		NAME	TYPE	DESCRIPTION
QFN PIN	WCSP BALL			
6	A5	DMDIN/ MFP3/	I	Primary (SPI_Select = 1) SPI serial clock Secondary: (SPI_Select = 0) Digital microphone input Headset detect input Audio serial data bus (secondary) bit clock input Audio serial data bus (secondary) DAC/common word clock input Audio serial data bus (secondary) ADC word clock input Audio serial data bus (secondary) data input General Purpose Input
7	A4	SCL/ SS	I	Multi-function digital input. For (SPI_SELECT=0): Clock Pin for I2C control bus. For (SPI_SELECT = 1): SPI chip selection pin.
8	B4	SDA/ MOSI	I/O	Multi-function digital pin. For (SPI_SELECT=0): Data Pin for I2C control bus. For (SPI_SELECT = 1): SPI data input.
9	B5	DMCLK/ MFP4	O	Primary (SPI_Select = 1) Serial data output Secondary (SPI_Select = 0) Multifunction pin #4 (MFP4) options are only available using I <sup>2</sup> C Digital microphone clock output General purpose output CLKOUT output INT1 output INT2 output Audio serial data bus (primary) ADC word clock output Audio serial data bus (secondary) data output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output
10	C5	HPR	O	Right high-power output driver
11	D5	LDOin	Power	LDO Input supply and Headphone Power supply 1.9V– 3.6V
12	D4	HPL	O	Left high power output driver
13	D3	AVdd	Power	Analog voltage supply 1.5V–1.95V Input when A-LDO disabled, Filtering output when A-LDO enabled
14	E4	AVss	Ground	Analog ground supply
15	E5	INL	I	Left Analog Bypass Input
16	E3	INR	I	Right Analog Bypass Input
17	E2	REF	O	Reference voltage output for filtering
18	D2	MICBIAS	O	Microphone bias voltage output
19	E1	SPI_SELECT	I	Control mode select pin ( 1 = SPI, 0 = I2C )
20	C2	RESET	I	Reset (active low)
21	D1	DVss	Ground	Digital Ground and Chip-substrate
22	C1	DVdd	Power	Digital voltage supply 1.26V–1.95V
23	B1	IOVss	Ground	I/O ground supply
24	C3	IOVdd	Power	I/O voltage supply 1.1V – 3.6V
n/a	C4	GPIO/MFP5	I/O	Primary General Purpose digital IO Secondary CLKOUT Output INT1 Output INT2 Output Audio serial data bus ADC word clock output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output Digital microphone clock output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	MIN	MAX	UNIT
AVdd to AVss	-0.3	2.2	V
DVdd to DVss	-0.3	2.2	V
IOVDD to IOVSS	-0.3	3.9	V
LDOIN to AVss	-0.3	3.9	V
Digital Input voltage	-0.3	IOVDD + 0.3	V
Analog input voltage	-0.3	AVdd + 0.3	V
Operating temperature range	-40	85	°C
Storage temperature range	-55	125	°C
Junction temperature (T <sub>J</sub> Max)		105	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), YZK, per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Human-body model (HBM), RGE, per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2500
		Charged-device model (CDM), YZK, per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000
		Charged-device model (CDM), RGE, per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT	
LDOIN <sup>(1)</sup>	Power Supply Voltage Range	Referenced to AVss <sup>(2)</sup>	1.9		3.6	V	
AVdd			1.5	1.8	1.95		
IOVDD			Referenced to IOVSS <sup>(2)</sup>	1.1			3.6
DVdd			Referenced to DVss <sup>(2)</sup>	1.65	1.8		1.95
DVdd <sup>(3)</sup>				1.26	1.8		1.95
PLL Input Frequency		Clock divider uses fractional divide (D > 0), P=1, D <sub>Vdd</sub> ≥ 1.65V (See table in SLAU434, <i>Maximum TLV320DAC3203 Clock Frequencies</i> )	10		20	MHz	
		Clock divider uses integer divide (D = 0), P=1, D <sub>Vdd</sub> ≥ 1.65V (Refer to table in SLAU434, <i>Maximum TLV320DAC3203 Clock Frequencies</i> )	0.512		20	MHz	
MCLK	Master Clock Frequency	MCLK; Master Clock Frequency; D <sub>Vdd</sub> ≥ 1.65V			50	MHz	
SCL	SCL Clock Frequency				400	kHz	
HPL, HPR	Stereo headphone output load resistance	Single-ended configuration	14.4	16		Ω	
	Headphone output load resistance	Differential configuration	24.4	32		Ω	
C <sub>Lout</sub>	Digital output load capacitance			10		pF	
C <sub>ref</sub>	Reference decoupling capacitor			1		μF	

- (1) Minimum spec applies if LDO is used. Minimum is 1.5V if LDO is not enabled. Using the LDO below 1.9V degrades LDO performance.

- (2) All grounds on board are tied together, so they should not differ in voltage by more than 0.2V max, for any combination of ground signals.

- (3) At DVdd values lower than 1.65V, the PLL does not function. Please see table in SLAU434, *Maximum TLV320DAC3203 Clock Frequencies* for details on maximum clock frequencies.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TLV320DAC3203		UNIT
		YZK (DSBGA)	RGE (VQFN)	
		25 PINS	24 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	57.6	34.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	0.3	26.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	13.7	12.5	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.1	0.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	13.7	12.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics, Bypass Outputs

At 25°C, AV<sub>dd</sub>, DV<sub>dd</sub>, IOVDD = 1.8V, LDO<sub>in</sub> = 1.8V, AV<sub>dd</sub> LDO disabled, f<sub>s</sub> (Audio) = 48kHz, C<sub>ref</sub> = 10μF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG BYPASS TO HEADPHONE AMPLIFIER, DIRECT MODE</b>					
Device Setup	Load = 16Ω (single-ended), 50pF; Input and Output CM = 0.9V; Headphone Output on LDOIN Supply; INL routed to HPL and INR routed to HPR; Channel Gain = 0dB				
Gain Error			±0.4		dB
Noise, A-weighted <sup>(1)</sup>	Idle Channel, INL and INR ac-shortened to ground		3		μV <sub>RMS</sub>
THD	Total Harmonic Distortion	446mVrms, 1-kHz input signal	-82		dB

(1) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

## 6.6 Electrical Characteristics, Microphone Interface

At 25°C, AV<sub>dd</sub>, DV<sub>dd</sub>, IOVDD = 1.8V, LDO<sub>in</sub> = 1.8V, AV<sub>dd</sub> LDO disabled, C<sub>ref</sub> = 10μF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>MICROPHONE BIAS</b>					
Bias voltage	CM = 0.9V, LDOin = 3.3V, no load	Micbias Mode 0, Connect to AV <sub>dd</sub> or LDOin	1.25		V
		Micbias Mode 1, Connect to LDOin	1.7		V
		Micbias Mode 2, Connect to LDOin	2.5		V
		Micbias Mode 3, Connect to AV <sub>dd</sub>	AV <sub>dd</sub>		V
		Micbias Mode 3, Connect to LDOin	LDOin		V
	CM = 0.75V, LDOin = 3.3V	Micbias Mode 0, Connect to AV <sub>dd</sub> or LDOin	1.04		V
		Micbias Mode 1, Connect to AV <sub>dd</sub> or LDOin	1.42		V
		Micbias Mode 2, Connect to LDOin	2.08		V
		Micbias Mode 3, Connect to AV <sub>dd</sub>	AV <sub>dd</sub>		V
		Micbias Mode 3, Connect to LDOin	LDOin		V
Output Noise	CM = 0.9V		10		μV <sub>RMS</sub>
Current Sourcing	Micbias Mode 2, Connect to LDOin		3		mA
Inline Resistance	Micbias Mode 3, Connect to AV <sub>dd</sub>		160		Ω
	Micbias Mode 3, Connect to LDOin		110		

## 6.7 Electrical Characteristics, Audio Outputs

At 25°C, AVdd, DVdd, IOVDD = 1.8V, LDO\_in = 1.8V, AVdd LDO disabled, f<sub>s</sub> (Audio) = 48kHz, C<sub>ref</sub> = 10 μF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Audio DAC – Stereo Single-Ended Headphone Output</b>						
Device Setup		Load = 16Ω (single-ended), 50pF Headphone Output on AVdd Supply, Input & Output CM = 0.9V, DOSR = 128, MCLK = 256* f <sub>s</sub> , Channel Gain = 0dB word length = 16 bits; Processing Block = PRB_P1 Power Tune = PTM_P3				
Full scale output voltage (0dB)				0.5		V <sub>RMS</sub>
SNR	Signal-to-noise ratio, A-weighted <sup>(1)</sup> (2)	All zeros fed to DAC input, modulator in excited state	88	100		dB
DR	Dynamic range, A-weighted <sup>(1)</sup> (2)	–60dB 1kHz input full-scale signal, Word Length = 20 bits, Power Tune = PTM_P4		99		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–80	–70	dB
DAC Gain Error		0dB, 1kHz input full scale signal		±0.1		dB
DAC Mute Attenuation		Mute		127		dB
DAC channel separation		–1dB, 1kHz signal, between left and right HP out		92		dB
DAC PSRR		100mVpp, 1kHz signal applied to AVdd		70		dB
		100mVpp, 217Hz signal applied to AVdd		75		dB
Power Delivered		R <sub>L</sub> =16Ω, Output Stage on AVdd = 1.8V THDN < 1%, Input CM=0.9V, Output CM=0.9V, Channel Gain = 2dB		13		mW
		R <sub>L</sub> = 16Ω Output Stage on LDOIN = 3.3V, THDN < 1% Input CM = 0.9V, Output CM = 1.65V, Channel Gain = 8dB		47		
<b>Audio DAC – Stereo Single-Ended Headphone Output</b>						
Device Setup		Load = 16Ω (single-ended), 50pF, Headphone Output on AVdd Supply, Input and Output CM = 0.75V; AVdd = 1.5V, DOSR = 128, MCLK = 256 x f <sub>s</sub> , Channel Gain = –2dB, word length = 20-bits; Processing Block = PRB_P1, Power Tune = PTM_P4				
Full scale output voltage (0dB)				0.375		V <sub>RMS</sub>
SNR	Signal-to-noise ratio, A-weighted <sup>(1)</sup> (2)	All zeros fed to DAC input, modulator in excited state		99		dB
DR	Dynamic range, A-weighted <sup>(1)</sup> (2)	–60dB 1 kHz input full-scale signal		98		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–84		dB

(1) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

**Electrical Characteristics, Audio Outputs (continued)**

At 25°C, AVdd, DVdd, IOVDD = 1.8V, LDO\_in = 1.8V, AVdd LDO disabled,  $f_s$  (Audio) = 48kHz, Cref = 10  $\mu$ F on REF PIN, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Audio DAC – Mono Differential Headphone Output</b>						
Device Setup		Load = 32 $\Omega$ (differential), 50pF, Headphone Output on LDOIN Supply Input CM = 0.75V, Output CM = 1.5V, AVdd=1.8V, LDOIN = 3.0V, DOSR = 128 MCLK = 256* $f_s$ , Channel (headphone driver) Gain = 5dB for full scale output signal, word length = 16-bits, Processing Block = PRB_P1, Power Tune = PTM_P3				
	Full scale output voltage (0dB)			1778		mV <sub>RMS</sub>
SNR	Signal-to-noise ratio, A-weighted <sup>(1) (2)</sup>	All zeros fed to DAC input, modulator in excited state		101		dB
DR	Dynamic range, A-weighted <sup>(1) (2)</sup>	–60dB 1kHz input full-scale signal		98		dB
THD	Total Harmonic Distortion	–3dB full-scale, 1-kHz input signal		–82		dB
Power Delivered		$R_L = 32\Omega$ , Output Stage on LDOIN = 3.3V, THDN < 1%, Input CM = 0.9V, Output CM = 1.65V, Channel Gain = 8dB		125		mW
		$R_L = 32\Omega$ Output Stage on LDOIN = 3V, THDN < 1% Input CM = 0.9V, Output CM = 1.5V, Channel Gain = 8dB		103		mW

## 6.8 Electrical Characteristics, LDO

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LOW DROPOUT REGULATOR (AV<sub>DD</sub>)</b>					
Output Voltage	LDO <sub>Mode</sub> = 1, LDO <sub>in</sub> > 1.95V, I <sub>O</sub> = 15mA		1.63		V
	LDO <sub>Mode</sub> = 0, LDO <sub>in</sub> > 2.0V, I <sub>O</sub> = 15mA		1.68		
	LDO <sub>Mode</sub> = 2, LDO <sub>in</sub> > 2.05V, I <sub>O</sub> = 15mA		1.73		
Output Voltage Accuracy			±2%		
Load Regulation	Load current range 0 to 50mA		26		mV
Line Regulation	Input Supply Range 1.9V to 3.6V		3		mV
Decoupling Capacitor		1			μF
Bias Current			50		μA

## 6.9 Electrical Characteristics, Misc.

At 25°C, AV<sub>DD</sub>, DV<sub>DD</sub>, IOV<sub>DD</sub> = 1.8V, LDO<sub>in</sub> = 3.3V, AV<sub>DD</sub> LDO disabled, f<sub>s</sub> (Audio) = 48kHz, C<sub>ref</sub> = 10 μF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>REFERENCE</b>					
Reference Voltage Settings	C <sub>MMode</sub> = 0 (0.9V)		0.9		V
	C <sub>MMode</sub> = 1 (0.75V)		0.75		
Reference Noise	C <sub>M</sub> =0.9V, A-weighted, 20Hz to 20kHz bandwidth, C <sub>ref</sub> = 10μF		1		μV <sub>RMS</sub>
Decoupling Capacitor		1	10		μF
Bias Current			120		μA
<b>Shutdown Current</b>					
Device Setup	Coarse AV <sub>DD</sub> supply turned off, LDO <sub>select</sub> held at ground, No external digital input is toggled				
I <sub>DVDD</sub>			1.4		μA
I <sub>AVDD</sub>			1		
I <sub>LDOin</sub>			1		
I <sub>IOVDD</sub>			<0.1		

## 6.10 Electrical Characteristics, Logic Levels<sup>(1)</sup>

At 25°C, AV<sub>DD</sub>, DV<sub>DD</sub>, IOV<sub>DD</sub> = 1.8V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LOGIC FAMILY</b>					
<b>CMOS</b>					
V <sub>IH</sub> Logic Level	I <sub>IH</sub> = 5 μA, IOV <sub>DD</sub> > 1.6V	0.7 × IOV <sub>DD</sub>			V
	I <sub>IH</sub> = 5μA, 1.2V ≤ IOV <sub>DD</sub> < 1.6V	0.9 × IOV <sub>DD</sub>			V
	I <sub>IH</sub> = 5μA, IOV <sub>DD</sub> < 1.2V	IOV <sub>DD</sub>			V
V <sub>IL</sub>	I <sub>IL</sub> = 5 μA, IOV <sub>DD</sub> > 1.6V	-0.3	0.3 × IOV <sub>DD</sub>		V
	I <sub>IL</sub> = 5μA, 1.2V ≤ IOV <sub>DD</sub> < 1.6V		0.1 × IOV <sub>DD</sub>		V
	I <sub>IL</sub> = 5μA, IOV <sub>DD</sub> < 1.2V		0		V
V <sub>OH</sub>	I <sub>OH</sub> = 2 TTL loads	0.8 × IOV <sub>DD</sub>			V
V <sub>OL</sub>	I <sub>OL</sub> = 2 TTL loads		0.1 × IOV <sub>DD</sub>		V
Capacitive Load			10		pF

(1) Applies to all DI, DO, and DIO pins shown in .

### 6.11 Typical Timing Characteristics — Audio Data Serial Interface Timing (I<sup>2</sup>S)

All specifications at 25°C, DV<sub>DD</sub> = 1.8V

		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
<b>I<sup>2</sup>S/LJF/RJF Timing in Master Mode (see 图 1)</b>						
t <sub>d</sub> (WS)	WCLK delay		30	20		ns
t <sub>d</sub> (DO-WS)	WCLK to DOUT delay (For LJF Mode only)		50	25		ns
t <sub>d</sub> (DO-BCLK)	BCLK to DOUT delay		50	25		ns
t <sub>s</sub> (DI)	DIN setup	8		8		ns
t <sub>h</sub> (DI)	DIN hold	8		8		ns
t <sub>r</sub>	Rise time		24	12		ns
t <sub>f</sub>	Fall time		24	15		ns
<b>I<sup>2</sup>S/LJF/RJF Timing in Slave Mode (see 图 2)</b>						
t <sub>H</sub> (BCLK)	BCLK high period	35		35		ns
t <sub>L</sub> (BCLK)	BCLK low period	35		35		ns
t <sub>s</sub> (WS)	WCLK setup	8		8		ns
t <sub>h</sub> (WS)	WCLK hold	8		8		ns
t <sub>d</sub> (DO-WS)	WCLK to DOUT delay (For LJF mode only)		50	25		ns
t <sub>d</sub> (DO-BCLK)	BCLK to DOUT delay		50	25		ns
t <sub>s</sub> (DI)	DIN setup	8		8		ns
t <sub>h</sub> (DI)	DIN hold	8		8		ns
t <sub>r</sub>	Rise time		4	4		ns
t <sub>f</sub>	Fall time		4	4		ns

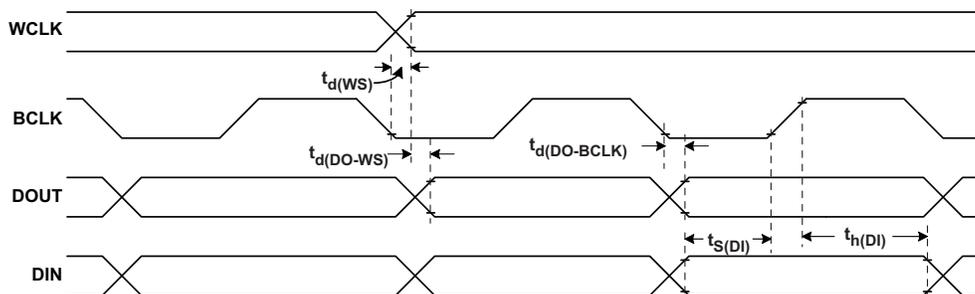


图 1. I<sup>2</sup>S/LJF/RJF Timing in Master Mode

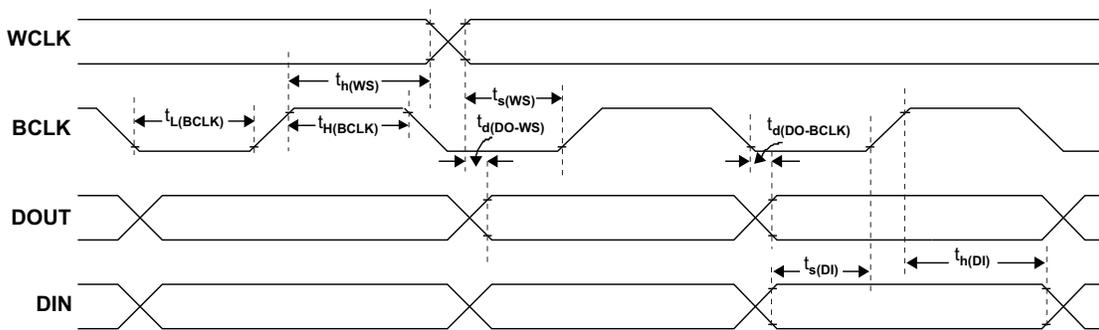


图 2. I<sup>2</sup>S/LJF/RJF Timing in Slave Mode

## 6.12 Typical DSP Timing Characteristics

All specifications at 25°C, DVdd = 1.8V

		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
<b>DSP Timing in Master Mode (see 图 3)</b>						
$t_d$ (WS)	WCLK delay		30		20	ns
$t_d$ (DO-BCLK)	BCLK to DOUT delay		40		20	ns
$t_s$ (DI)	DIN setup	8		8		ns
$t_h$ (DI)	DIN hold	8		8		ns
$t_r$	Rise time		24		12	ns
$t_f$	Fall time		24		12	ns
<b>DSP Timing in Slave Mode (see 图 4)</b>						
$t_H$ (BCLK)	BCLK high period	35		35		ns
$t_L$ (BCLK)	BCLK low period	35		35		ns
$t_s$ (WS)	WCLK setup	8		8		ns
$t_h$ (WS)	WCLK hold	8		8		ns
$t_d$ (DO-BCLK)	BCLK to DOUT delay		40		22	ns
$t_s$ (DI)	DIN setup	8		8		ns
$t_h$ (DI)	DIN hold	8		8		ns
$t_r$	Rise time		4		4	ns
$t_f$	Fall time		4		4	ns

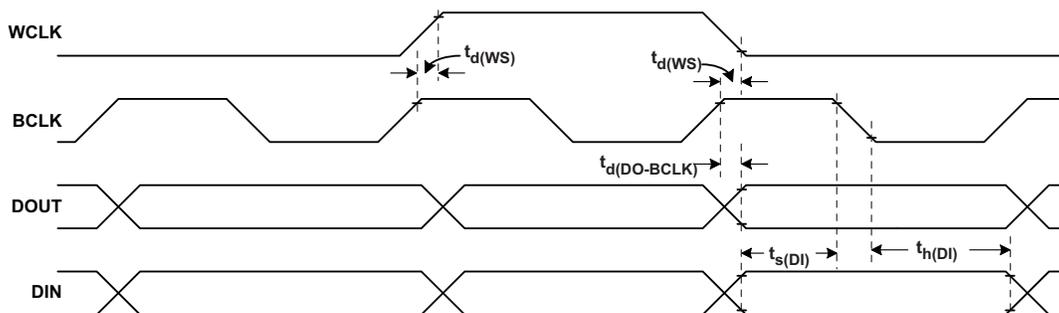


图 3. DSP Timing in Master Mode

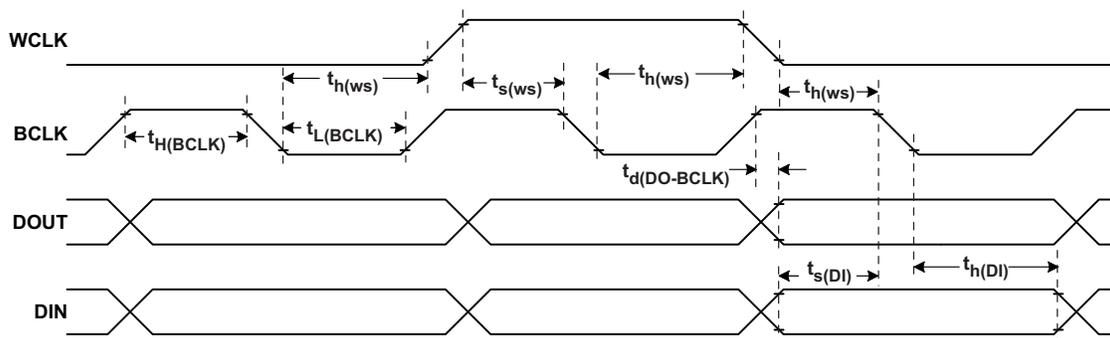


图 4. DSP Timing in Slave Mode

### 6.13 I<sup>2</sup>C Interface Timing

		Standard-Mode			Fast-Mode			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$f_{SCL}$	SCL clock frequency	0		100	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0			0.8			$\mu$ s
$t_{LOW}$	LOW period of the SCL clock	4.7			1.3			$\mu$ s
$t_{HIGH}$	HIGH period of the SCL clock	4.0			0.6			$\mu$ s
$t_{SU;STA}$	Setup time for a repeated START condition	4.7			0.8			$\mu$ s
$t_{HD;DAT}$	Data hold time: For I2C bus devices	0		3.45	0		0.9	$\mu$ s
$t_{SU;DAT}$	Data set-up time	250			100			ns
$t_r$	SDA and SCL Rise Time			1000	$20+0.1C_b$		300	ns
$t_f$	SDA and SCL Fall Time			300	$20+0.1C_b$		300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0			0.8			$\mu$ s
$t_{BUF}$	Bus free time between a STOP and START condition	4.7			1.3			$\mu$ s
$C_b$	Capacitive load for each bus line			400			400	pF

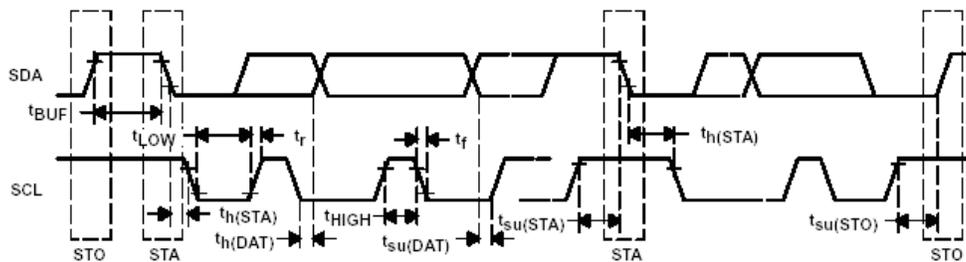


图 5. I<sup>2</sup>C Interface Timing

### 6.14 SPI Interface Timing (See 图 6)

All specifications at 25°C, DVdd = 1.8V

		IOVDD=1.8V			IOVDD=3.3V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{sck}$	SCLK Period	100			50			ns
$t_{sckh}$	SCLK Pulse width High	50			25			ns
$t_{sckl}$	SCLK Pulse width Low	50			25			ns
$t_{lead}$	Enable Lead Time	30			20			ns
$t_{lag}$	Enable Lag Time	30			20			ns
$t_{d,seqxfr}$	Sequential Transfer Delay	40			20			ns
$t_a$	Slave DOUT access time			40			20	ns
$t_{dis}$	Slave DOUT disable time			40			25	ns
$t_{su}$	DIN data setup time	15			10			ns
$t_{h,DIN}$	DIN data hold time	15			10			ns
$t_{v,DOUT}$	DOUT data valid time			45			25	ns
$t_r$	SCLK Rise Time			4			4	ns
$t_f$	SCLK Fall Time			4			4	ns

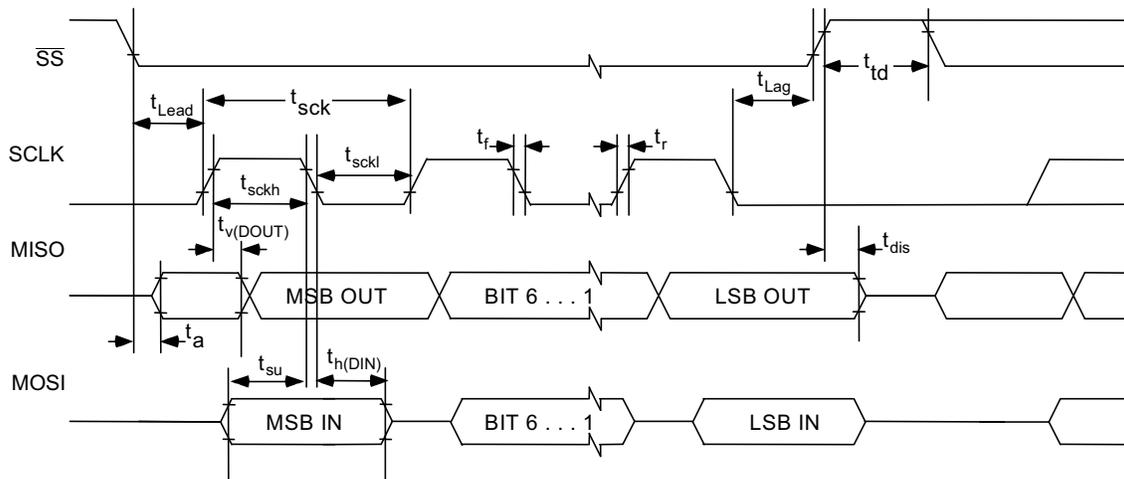


图 6. SPI Interface Timing Diagram

### 6.15 Typical Characteristics

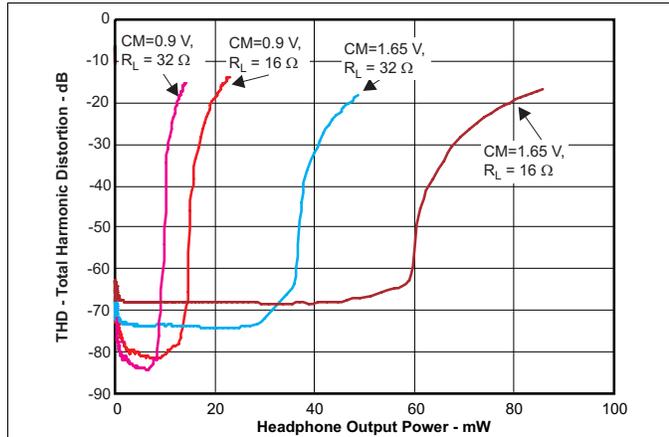


图 7. Total Harmonic Distortion vs Headphone Output Power

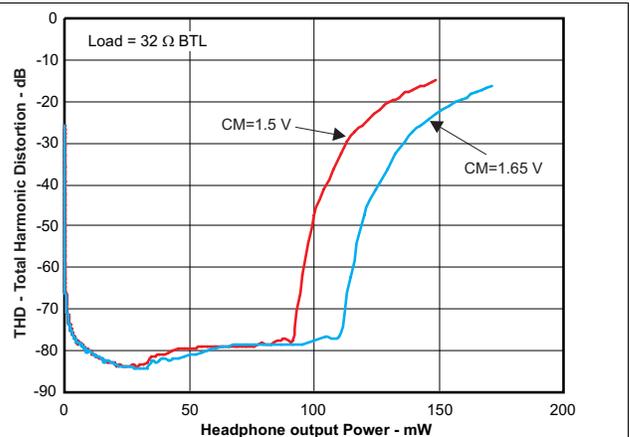


图 8. Total Harmonic Distortion vs Headphone Output Power

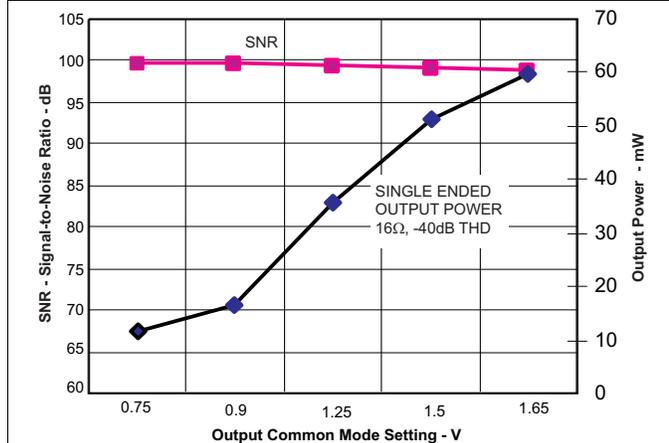


图 9. Headphone SNR and SE Output Power vs Output Common Mode Setting

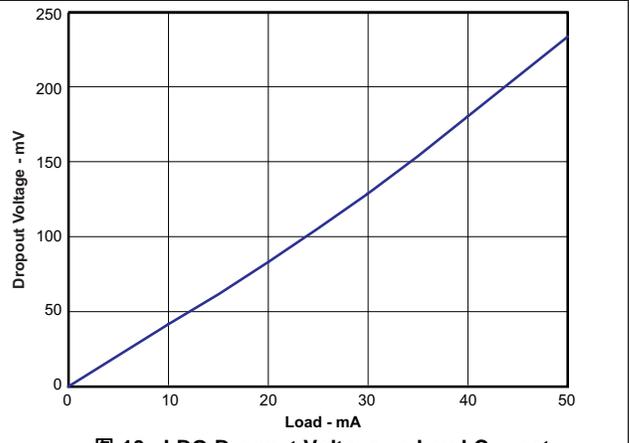


图 10. LDO Dropout Voltage vs Load Current

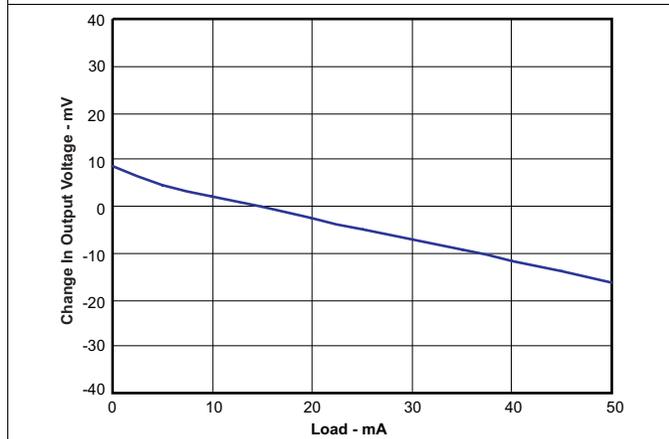


图 11. LDO Load Response

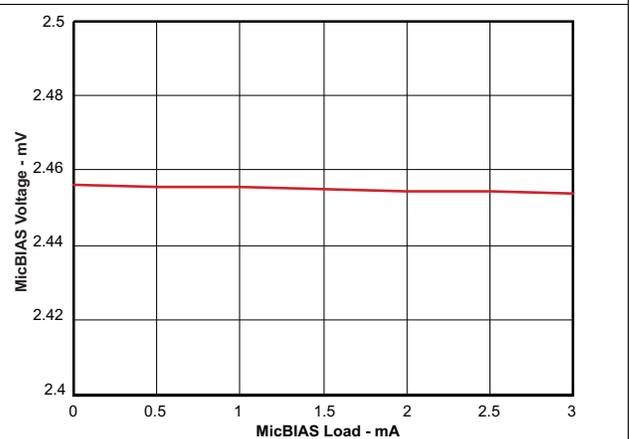
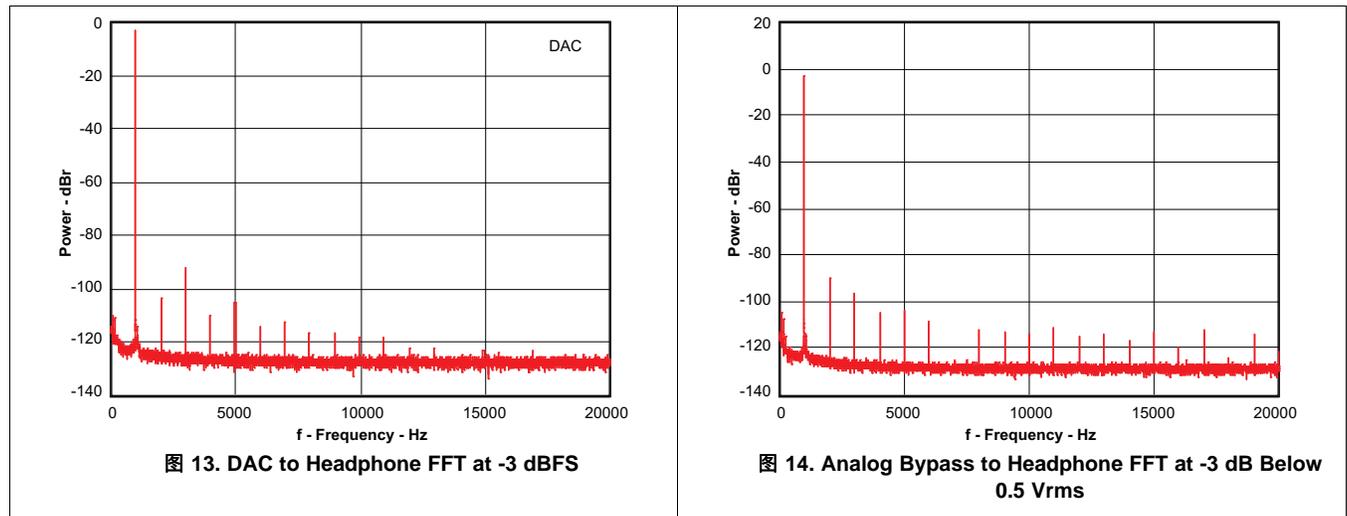


图 12. MICBIAS Mode 2, CM = 0.9 V, LDOIN OP Stage vs MICBIAS Load Current

### 6.15.1 Typical Characteristics, FFT



## 7 Detailed Description

### 7.1 Overview

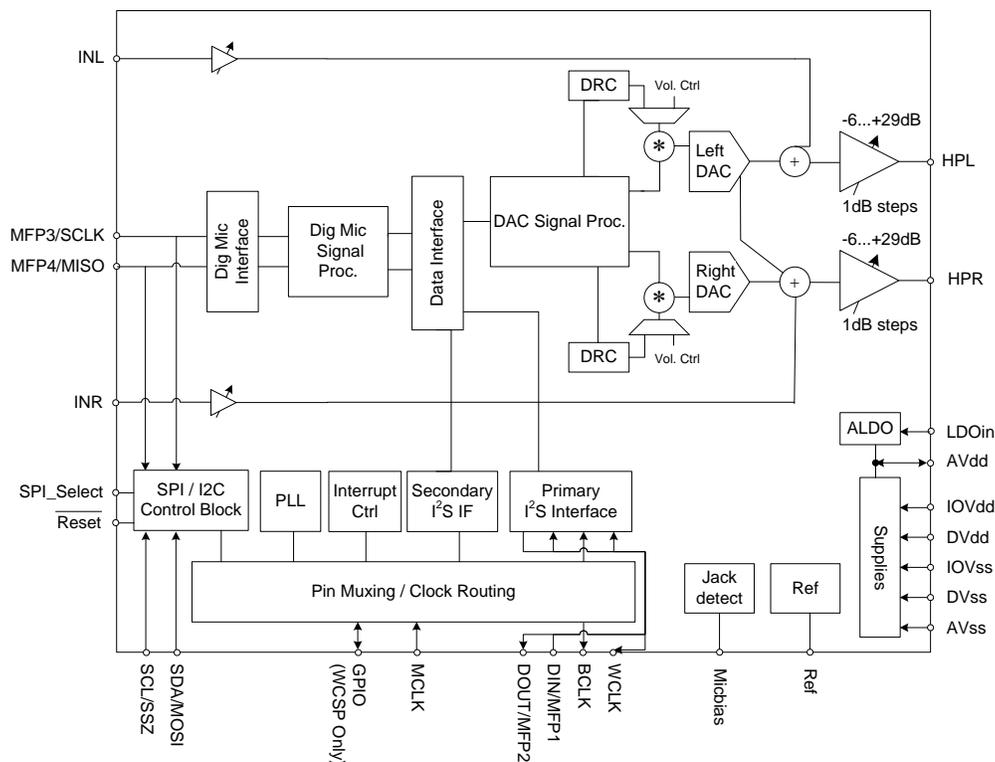
Combined with the advanced PowerTune technology, the device can cover operations from 8kHz mono voice playback to stereo 192kHz DAC playback, making it ideal for portable battery-powered audio and telephony applications.

The playback path offers signal processing blocks for filtering and effects, true differential output signal, flexible mixing of DAC and analog input signals as well as programmable volume controls. The TLV320DAC3203 contains two high-power output drivers which can be configured in multiple ways, including stereo and mono BTL. The integrated PowerTune technology allows the device to be tuned to just the right power-performance trade-off. Mobile applications frequently have multiple use cases requiring very low-power operation while being used in a mobile environment. When used in a docked environment, power consumption typically is less of a concern and lowest possible noise is more important. With PowerTune the TLV320DAC3203 can address both cases.

The voltage supply range for the TLV320DAC3203 for analog is 1.5V–1.95V, and for digital it is 1.26V–1.95V. To ease system-level design, a low-dropout regulator (LDO) is integrated to generate the appropriate analog supply from input voltages ranging from 1.8V to 3.6V. Digital I/O voltages are supported in the range of 1.1V–3.6V.

The required internal clock of the TLV320DAC3203 can be derived from multiple sources, including the MCLK, BCLK, GPIO pins or the output of internal PLL, where the input to the PLL again can be derived from the MCLK, BCLK or GPIO pins. Although using the internal, fractional PLL ensures the availability of a suitable clock signal, it is not recommended for the lowest power settings. The PLL is highly programmable and can accept available input clocks in the range of 512kHz to 50MHz.

### 7.2 Functional Block Diagram



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## 7.3 Feature Description

### 7.3.1 Device Connections

#### 7.3.1.1 Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are  $\overline{\text{Reset}}$  and the  $\overline{\text{SPI\_Select}}$  pin, which are HW control pins. Depending on the state of  $\overline{\text{SPI\_Select}}$ , the two control-bus pins SCL/SS and SDA/MOSI are configured for either I<sup>2</sup>C or SPI protocol.

Other digital IO pins can be configured for various functions via register control. An overview of available functionality is given in [Multifunction Pins](#).

##### 7.3.1.1.1 Multifunction Pins

Table 1 shows the possible allocation of pins for specific functions. The PLL input, for example, can be programmed to be any of 4 pins (MCLK, BCLK, DIN, GPIO).

**Table 1. Multifunction Pin Assignments**

		1	2	3	4	5	6	7	8
	Pin Function	MCLK	BCLK	WCLK	DIN MFP1	DOU MFP2	MFP3/ SCLK	MFP4/ MISO	GPIO MFP5
A	PLL Input	S <sup>(1)</sup>	S <sup>(2)</sup>		E				S <sup>(3)</sup>
B	Codec Clock Input	S <sup>(1)</sup> ,D <sup>(4)</sup>	S <sup>(2)</sup>						S <sup>(3)</sup>
C	I <sup>2</sup> S BCLK input		S,D						
D	I <sup>2</sup> S BCLK output		E <sup>(5)</sup>						
E	I <sup>2</sup> S WCLK input			E, D					
F	I <sup>2</sup> S WCLK output			E					
G	I <sup>2</sup> S ADC word clock input						E		E
H	I <sup>2</sup> S ADC WCLK out							E	E
I	I <sup>2</sup> S DIN				E, D				
J	I <sup>2</sup> S DOU					E, D			
K	General Purpose Output I					E			
K	General Purpose Output II							E	
K	General Purpose Output III								E
L	General Purpose Input I				E				
L	General Purpose Input II						E		
L	General Purpose Input III								E
M	INT1 output					E		E	E
N	INT2 output					E		E	E
Q	Secondary I <sup>2</sup> S BCLK input						E		E
R	Secondary I <sup>2</sup> S WCLK in						E		E
S	Secondary I <sup>2</sup> S DIN						E		E
T	Secondary I <sup>2</sup> S DOU							E	
U	Secondary I <sup>2</sup> S BCLK OUT					E		E	E
V	Secondary I <sup>2</sup> S WCLK OUT					E		E	E
X	Aux Clock Output					E		E	E

(1) S<sup>(1)</sup>: The MCLK pin can drive the PLL and Codec Clock inputs **simultaneously**.

(2) S<sup>(2)</sup>: The BCLK pin can drive the PLL and Codec Clock and audio interface bit clock inputs **simultaneously**.

(3) S<sup>(3)</sup>: The GPIO/MFP5 pin can drive the PLL and Codec Clock inputs simultaneously.

(4) D: Default Function

(5) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin. (If GPIO/MFP5 has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time.)

### 7.3.1.2 Analog Pins

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

### 7.3.2 Analog Audio I/O

The analog I/O path of the TLV320DAC3203 offers a variety of options for signal conditioning and routing:

- 2 headphone amplifier outputs
- Analog gain setting
- Single ended and differential modes

#### 7.3.2.1 Analog Low Power Bypass

The TLV320DAC3203 offers an analog-bypass mode. An analog signal can be routed from the analog input pin to the output amplifier. Neither the digital-input processing blocks nor the DAC resources are required for such operation; this supports low-power operation during analog-bypass mode.

In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs INL to the left headphone amplifier (HPL) and INR to HPR.

#### 7.3.2.2 Headphone Outputs

The stereo headphone drivers on pins HPL and HPR can drive loads with impedances down to 16Ω in single-ended AC-coupled headphone configurations, or loads down to 32Ω in differential mode, where a speaker is connected between HPL and HPR. In single-ended drive configuration these drivers can drive up to 15mW power into each headphone channel while operating from 1.8V analog supplies. While running from the AVdd supply, the output common-mode of the headphone driver is set by the common-mode setting of analog inputs to allow maximum utilization of the analog supply range while simultaneously providing a higher output-voltage swing. In cases when higher output-voltage swing is required, the headphone amplifiers can run directly from the higher supply voltage on LDOIN input (up to 3.6V). To use the higher supply voltage for higher output signal swing, the output common-mode can be adjusted to either 1.25V, 1.5V or 1.65V. When the common-mode voltage is configured at 1.65V and LDOIN supply is 3.3V, the headphones can each deliver up to 40mW power into a 16Ω load.

The headphone drivers are capable of driving a mixed combination of DAC signal and bypass from analog input INL and INR. The analog input signals can be attenuated up to 72dB before routing. The level of the DAC signal can be controlled using the digital volume control of the DAC. To control the output-voltage swing of headphone drivers, the digital volume control provides a range of –6.0dB to +29.0dB <sup>(1)</sup> in steps of 1dB. These level controls are not meant to be used as dynamic volume control, but more to set output levels during initial device configuration. Refer to for recommendations for using headphone volume control for achieving 0dB gain through the DAC channel with various configurations.

### 7.3.3 Digital Microphone Interface

The TLV320DAC3203 includes a stereo decimation filter for digital microphone inputs. The stereo recording path can be powered up one channel at a time, to support the case where only mono record capability is required.

The digital microphone input path of the TLV320DAC3203 features a large set of options for signal conditioning as well as signal routing:

- Stereo decimation filters (PDM input)
- Fine gain adjustment of digital channels with 0.1dB step size
- Digital volume control with a range of -12 to +20dB
- Mute function

In addition to the standard set of stereo decimation filter features the TLV320DAC3203 also offers the following special functions:

- Channel-to-channel phase adjustment
- Adaptive filter mode

(1) If the device must be placed into 'mute' from the –6.0dB setting, set the device at a gain of –5.0dB first, then place the device into mute.

### 7.3.3.1 ADC Processing Blocks — Overview

The TLV320DAC3203 includes a built-in digital decimation filter to process the oversampled data from the PDM input to generate digital data at Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay and sampling rate.

#### 7.3.3.1.1 Processing Blocks

The TLV320DAC3203 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

Table 2 gives an overview of the available processing blocks and their properties.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter

The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first order IIR, BiQuad and FIR filters have fully user-programmable coefficients. The Resource Class Column (RC) gives an approximate indication of power consumption.

**Table 2. Processing Blocks**

Processing Blocks	Channel	Decimation Filter	1st Order IIR Available	Number BiQuads	FIR	Required AOSR Value	Resource Class
PRB_R1 <sup>(1)</sup>	Stereo	A	Yes	0	No	128,64	6
PRB_R2	Stereo	A	Yes	5	No	128,64	8
PRB_R3	Stereo	A	Yes	0	25-Tap	128,64	8
PRB_R4	Right	A	Yes	0	No	128,64	3
PRB_R5	Right	A	Yes	5	No	128,64	4
PRB_R6	Right	A	Yes	0	25-Tap	128,64	4
PRB_R7	Stereo	B	Yes	0	No	64	3
PRB_R8	Stereo	B	Yes	3	No	64	4
PRB_R9	Stereo	B	Yes	0	20-Tap	64	4
PRB_R10	Right	B	Yes	0	No	64	2
PRB_R11	Right	B	Yes	3	No	64	2
PRB_R12	Right	B	Yes	0	20-Tap	64	2
PRB_R13	Stereo	C	Yes	0	No	32	3
PRB_R14	Stereo	C	Yes	5	No	32	4
PRB_R15	Stereo	C	Yes	0	25-Tap	32	4
PRB_R16	Right	C	Yes	0	No	32	2
PRB_R17	Right	C	Yes	5	No	32	2
PRB_R18	Right	C	Yes	0	25-Tap	32	2

(1) Default

For more detailed information see the *TLV320DAC3203 Application Reference Guide*

### 7.3.4 DAC

The TLV320DAC3203 includes a stereo audio DAC supporting data rates from 8kHz to 192kHz. Each channel of the stereo audio DAC consists of a signal-processing engine with fixed processing blocks, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20kHz. To handle multiple input rates and optimize performance, the TLV320DAC3203 allows the system designer to program the oversampling rates over a wide range from 1 to 1024. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TLV320DAC3203 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the sigma-delta modulator. The interpolation filter can be chosen from three different types depending on required frequency response, group delay and sampling rate.

The DAC path of the TLV320DAC3203 features many options for signal conditioning and signal routing:

- Digital volume control with a range of -63.5 to +24dB
- Mute function
- Dynamic range compression (DRC)

In addition to the standard set of DAC features the TLV320DAC3203 also offers the following special features:

- Built in sine wave generation (beep generator)
- Digital auto mute
- Adaptive filter mode

#### 7.3.4.1 DAC Processing Blocks — Overview

The TLV320DAC3203 implements signal processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

**Table 3** gives an overview over all available processing blocks of the DAC channel and their properties.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- 3D – Effect
- Beep Generator

The processing blocks are tuned for typical cases and can achieve high image rejection or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients. The Resource Class Column (RC) gives an approximate indication of power consumption.

**Table 3. Overview – DAC Predefined Processing Blocks**

Processing Block No.	Interpolation Filter	Channel	1st Order IIR Available	Num. of Biquads	DRC	3D	Beep Generator	Resource Class
PRB_P1 <sup>(1)</sup>	A	Stereo	No	3	No	No	No	8
PRB_P2	A	Stereo	Yes	6	Yes	No	No	12
PRB_P3	A	Stereo	Yes	6	No	No	No	10
PRB_P4	A	Left	No	3	No	No	No	4
PRB_P5	A	Left	Yes	6	Yes	No	No	6
PRB_P6	A	Left	Yes	6	No	No	No	6
PRB_P7	B	Stereo	Yes	0	No	No	No	6
PRB_P8	B	Stereo	No	4	Yes	No	No	8

(1) Default

**Table 3. Overview – DAC Predefined Processing Blocks (continued)**

Processing Block No.	Interpolation Filter	Channel	1st Order IIR Available	Num. of Biquads	DRC	3D	Beep Generator	Resource Class
PRB_P9	B	Stereo	No	4	No	No	No	8
PRB_P10	B	Stereo	Yes	6	Yes	No	No	10
PRB_P11	B	Stereo	Yes	6	No	No	No	8
PRB_P12	B	Left	Yes	0	No	No	No	3
PRB_P13	B	Left	No	4	Yes	No	No	4
PRB_P14	B	Left	No	4	No	No	No	4
PRB_P15	B	Left	Yes	6	Yes	No	No	6
PRB_P16	B	Left	Yes	6	No	No	No	4
PRB_P17	C	Stereo	Yes	0	No	No	No	3
PRB_P18	C	Stereo	Yes	4	Yes	No	No	6
PRB_P19	C	Stereo	Yes	4	No	No	No	4
PRB_P20	C	Left	Yes	0	No	No	No	2
PRB_P21	C	Left	Yes	4	Yes	No	No	3
PRB_P22	C	Left	Yes	4	No	No	No	2
PRB_P23	A	Stereo	No	2	No	Yes	No	8
PRB_P24	A	Stereo	Yes	5	Yes	Yes	No	12
PRB_P25	A	Stereo	Yes	5	Yes	Yes	Yes	12

For more detailed information see the *TLV320DAC3203 Application Reference Guide*.

### 7.3.5 Powertune

The TLV320DAC3203 features PowerTune, a mechanism to balance power-versus-performance trade-offs at the time of device configuration. The device can be tuned to minimize power dissipation, to maximize performance, or to an operating point between the two extremes to best fit the application.

For more detailed information see the *TLV320DAC3203 Application Reference Guide*.

### 7.3.6 Digital Audio I/O Interface

Audio data is transferred between the host processor and the TLV320DAC3203 via the digital audio data serial interface, or audio bus. The audio bus on this device is very flexible, including left or right-justified data options, support for I<sup>2</sup>S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The audio bus of the TLV320DAC3203 can be configured for left or right-justified, I<sup>2</sup>S, DSP, or TDM modes of operation, where communication with standard PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring Page 0, Register 27, D(5:4). In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the DAC sampling frequency.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider in Page 0, Register 30. The number of bit-clock pulses in a frame may need adjustment to accommodate various word-lengths as well as to support the case when multiple TLV320DAC3203s may share the same audio bus.

The TLV320DAC3203 also includes a feature to offset the position of start of data transfer with respect to the word-clock. This offset can be controlled in terms of number of bit-clocks and can be programmed in Page 0, Register 28.

The TLV320DAC3203 also has the feature of inverting the polarity of the bit-clock used for transferring the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen. This can be configured via Page 0, Register 29, D(3).

The TLV320DAC3203 includes the programmability to program at what bit clock in a frame does audio data begin. This enables time-division multiplexing (TDM), enabling use of multiple codecs on a single audio bus. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface are put into a hi-Z output condition.

By default when the word-clocks and bit-clocks are generated by the TLV320DAC3203, these clocks are active only when the DAC is powered up within the device. This is done to save power. However, it also supports a feature when both the word clocks and bit-clocks can be active even when the DAC in the device is powered down. This is useful when using the TDM mode with multiple codecs on the same bus, or when word-clock or bit-clocks are used in the system as general-purpose clocks.

### 7.3.7 Clock Generation and PLL

The TLV320DAC3203 supports a wide range of options for generating clocks for the DAC as well as interface and other control blocks. The clocks for the DAC require a source reference clock. This clock can be provided on a variety of device pins such as MCLK, BCLK, or GPIO pins. The CODEC\_CLKIN can then be routed through highly-flexible clock dividers to generate the various clocks required for the DAC sections. In the event that the desired audio clocks cannot be generated from the reference clocks on MCLK, BCLK, or GPIO, the TLV320DAC3203 also provides the option of using the on-chip PLL, which supports a wide range of fractional multiplication values to generate the required clocks. Starting from CODEC\_CLKIN the TLV320DAC3203 provides several programmable clock dividers to help achieve a variety of sampling rates for the DAC.

For more detailed information see the *TLV320DAC3203 Application Reference Guide*.

### 7.3.8 Control Interfaces

The TLV320DAC3203 control interface supports SPI or I<sup>2</sup>C communication protocols, with the protocol selectable using the SPI\_SELECT pin. For SPI, SPI\_SELECT should be tied high; for I<sup>2</sup>C, SPI\_SELECT should be tied low. Changing the state of SPI\_SELECT during device operation is not recommended.

#### 7.3.8.1 I<sup>2</sup>C Control

The TLV320DAC3203 supports the I<sup>2</sup>C control protocol, and will respond to the I<sup>2</sup>C address of 0011000. I<sup>2</sup>C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I<sup>2</sup>C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This circuit prevents two devices from conflicting; if two devices drive the bus simultaneously, there is no driver contention.

#### 7.3.8.2 SPI Control

In the SPI control mode, the TLV320DAC3203 uses the pins SCL/ $\overline{SS}$  as  $\overline{SS}$ , SCLK as SCLK, MISO as MISO, SDA/MOSI as MOSI; a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TLV320DAC3203) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

For more detailed information see the *TLV320DAC3203 Application Reference Guide*.

## 7.4 Device Functional Modes

The following special functions are available to support advanced system requirements:

- Headset detection
- Interrupt generation
- Flexible pin multiplexing

For more detailed information see the *TLV320DAC3203 Application Reference Guide*.

## 7.5 Register Maps

**Table 4. Summary of Register Map**

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	0	0x00	0x00	Page Select Register
0	1	0x00	0x01	Software Reset Register
0	2	0x00	0x02	Reserved Register
0	3	0x00	0x03	Reserved Register
0	4	0x00	0x04	Clock Setting Register 1, Multiplexers
0	5	0x00	0x05	Clock Setting Register 2, PLL P&R Values
0	6	0x00	0x06	Clock Setting Register 3, PLL J Values
0	7	0x00	0x07	Clock Setting Register 4, PLL D Values (MSB)
0	8	0x00	0x08	Clock Setting Register 5, PLL D Values (LSB)
0	9-10	0x00	0x09-0x0A	Reserved Register
0	11	0x00	0x0B	Clock Setting Register 6, NDAC Values
0	12	0x00	0x0C	Clock Setting Register 7, MDAC Values
0	13	0x00	0x0D	DAC OSR Setting Register 1, MSB Value
0	14	0x00	0x0E	DAC OSR Setting Register 2, LSB Value
0	15-17	0x00	0x0F-0x11	Reserved Register
0	18	0x00	0x12	Clock Setting Register 8, NADC Values
0	19	0x00	0x13	Clock Setting Register 9, MADC Values
0	20-24	0x00	0x14-0x18	Reserved Register
0	25	0x00	0x19	Clock Setting Register 10, Multiplexers
0	26	0x00	0x1A	Clock Setting Register 11, CLKOUT M divider value
0	27	0x00	0x1B	Audio Interface Setting Register 1
0	28	0x00	0x1C	Audio Interface Setting Register 2, Data offset setting
0	29	0x00	0x1D	Audio Interface Setting Register 3
0	30	0x00	0x1E	Clock Setting Register 12, BCLK N Divider
0	31	0x00	0x1F	Audio Interface Setting Register 4, Secondary Audio Interface
0	32	0x00	0x20	Audio Interface Setting Register 5
0	33	0x00	0x21	Audio Interface Setting Register 6
0	34	0x00	0x22	Digital Interface Misc. Setting Register
0	35-36	0x00	0x23-0x24	Reserved Register
0	37	0x00	0x25	DAC Flag Register 1
0	38	0x00	0x26	DAC Flag Register 2
0	39-41	0x00	0x27-0x29	Reserved Register
0	42	0x00	0x2A	Sticky Flag Register 1
0	43	0x00	0x2B	Interrupt Flag Register 1
0	44	0x00	0x2C	Sticky Flag Register 2
0	45	0x00	0x2D	Sticky Flag Register 3
0	46	0x00	0x2E	Interrupt Flag Register 2
0	47	0x00	0x2F	Interrupt Flag Register 3
0	48	0x00	0x30	INT1 Interrupt Control Register
0	49	0x00	0x31	INT2 Interrupt Control Register
0	50-51	0x00	0x32-0x33	Reserved Register
0	52	0x00	0x34	GPIO/MFP5 Control Register (YZK Package only)
0	53	0x00	0x35	MFP2 Function Control Register
0	54	0x00	0x36	DIN/MFP1 Function Control Register
0	55	0x00	0x37	MISO/MFP4 Function Control Register

**Register Maps (continued)**
**Table 4. Summary of Register Map (continued)**

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	56	0x00	0x38	SCLK/MFP3 Function Control Register
0	57-59	0x00	0x39-0x3B	Reserved Registers
0	60	0x00	0x3C	DAC Signal Processing Block Control Register
0	61-62	0x00	0x3D-0x3E	Reserved Register
0	63	0x00	0x3F	DAC Channel Setup Register 1
0	64	0x00	0x40	DAC Channel Setup Register 2
0	65	0x00	0x41	Left DAC Channel Digital Volume Control Register
0	66	0x00	0x42	Right DAC Channel Digital Volume Control Register
0	67	0x00	0x43	Headset Detection Configuration Register
0	68	0x00	0x44	DRC Control Register 1
0	69	0x00	0x45	DRC Control Register 2
0	70	0x00	0x46	DRC Control Register 3
0	71	0x00	0x47	Beep Generator Register 1
0	72	0x00	0x48	Beep Generator Register 2
0	73	0x00	0x49	Beep Generator Register 3
0	74	0x00	0x4A	Beep Generator Register 4
0	75	0x00	0x4B	Beep Generator Register 5
0	76	0x00	0x4C	Beep Generator Register 6
0	77	0x00	0x4D	Beep Generator Register 7
0	78	0x00	0x4E	Beep Generator Register 8
0	79	0x00	0x4F	Beep Generator Register 9
0	80-127	0x00	0x50-0x7F	Reserved Register
1	0	0x01	0x00	Page Select Register
1	1	0x01	0x01	Power Configuration Register
1	2	0x01	0x02	LDO Control Register
1	3	0x01	0x03	Playback Configuration Register 1
1	4	0x01	0x04	Playback Configuration Register 2
1	5-8	0x01	0x05-0x08	Reserved Register
1	9	0x01	0x09	Output Driver Power Control Register
1	10	0x01	0x0A	Common Mode Control Register
1	11	0x01	0x0B	Over Current Protection Configuration Register
1	12	0x01	0x0C	HPL Routing Selection Register
1	13	0x01	0x0D	HPR Routing Selection Register
1	14-15	0x01	0x0E-0x0F	Reserved Register
1	16	0x01	0x10	HPL Driver Gain Setting Register
1	17	0x01	0x11	HPR Driver Gain Setting Register
1	18-19	0x01	0x12-0x13	Reserved Register
1	20	0x01	0x14	Headphone Driver Startup Control Register
1	21	0x01	0x15	Reserved Register
1	22	0x01	0x16	INL to HPL Volume Control Register
1	23	0x01	0x17	INR to HPR Volume Control Register
1	24-50	0x01	0x18-0x32	Reserved Register
1	51	0x01	0x33	MICBIAS Configuration Register
1	52-57	0x01	0x34-0x39	Reserved Register
1	58	0x01	0x3A	Analog Input Settings

**Register Maps (continued)**
**Table 4. Summary of Register Map (continued)**

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
1	59-62	0x01	0x3B-0x3E	Reserved Register
1	63	0x01	0x3F	DAC Analog Gain Control Flag Register
1	64-122	0x01	0x40-0x7A	Reserved Register
1	123	0x01	0x7B	Reference Power-up Configuration Register
1	124	0x01	0x7C	Reserved Register
1	125	0x01	0x7D	Offset Calibration Register
1	126-127	0x01	0x7E-0x7F	Reserved Register
8	0-127	0x08	0x00-0x7F	Reserved Register
9-16	0-127	0x09-0x10	0x00-0x7F	Reserved Register
26-34	0-127	0x1A-0x22	0x00-0x7F	Reserved Register
44	0	0x2C	0x00	Page Select Register
44	1	0x2C	0x01	DAC Adaptive Filter Configuration Register
44	2-7	0x2C	0x02-0x07	Reserved
44	8-127	0x2C	0x08-0x7F	DAC Coefficients Buffer-A C(0:29)
45-52	0	0x2D-0x34	0x00	Page Select Register
45-52	1-7	0x2D-0x34	0x01-0x07	Reserved.
45-52	8-127	0x2D-0x34	0x08-0x7F	DAC Coefficients Buffer-A C(30:255)
62-70	0	0x3E-0x46	0x00	Page Select Register
62-70	1-7	0x3E-0x46	0x01-0x07	Reserved.
62-70	8-127	0x3E-0x46	0x08-0x7F	DAC Coefficients Buffer-B C(0:255)
80-114	0-127	0x50-0x72	0x00-0x7F	Reserved Register
152-186	0-127	0x98-0xBA	0x00-0x7F	Reserved Register

## 8 Application and Implementation

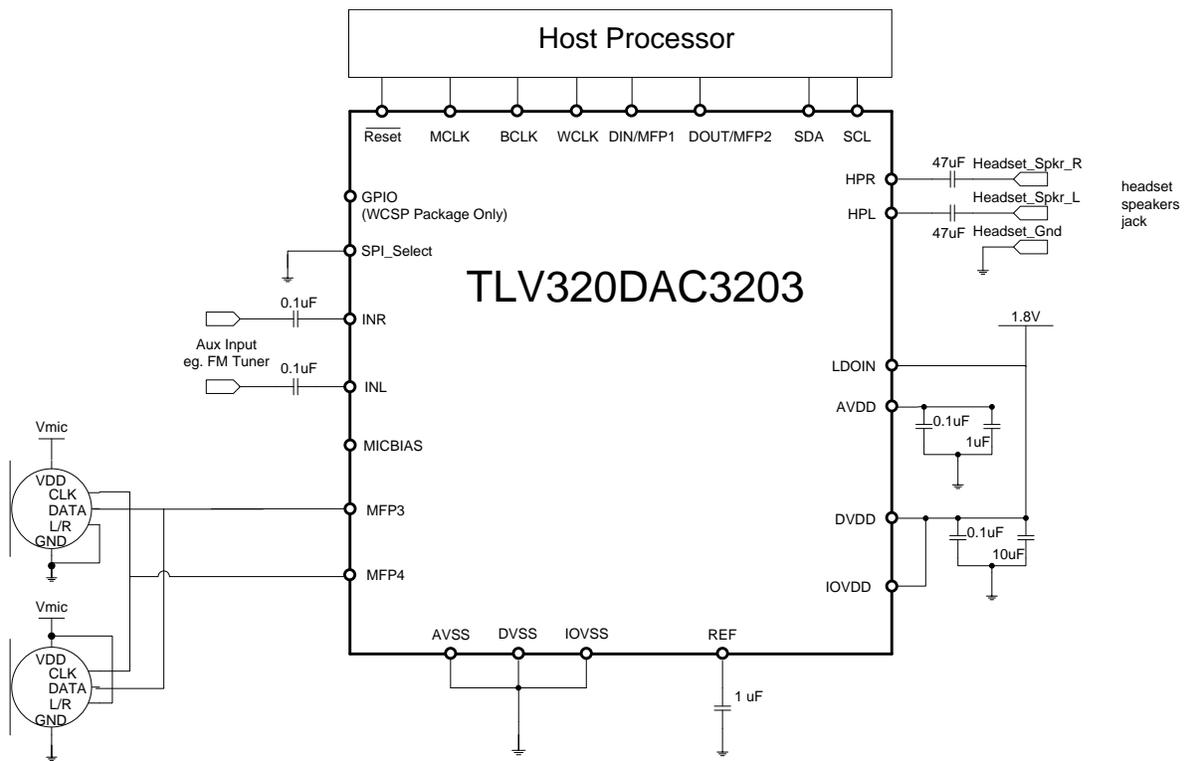
### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TLV320DAC3203 offers a wide range of configuration options. shows the basic functional blocks of the device.

### 8.2 Typical Application



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图 15. Typical Circuit Configuration

#### 8.2.1 Design Requirements

For this design example, us the parameters in 表 5.

表 5. Design Parameters

PARAMETER	EXAMPLE VALUE
Audio input	Digital Audio (I2S), Analog Audio INx
Speaker	Single-Ended 16-Ω Differential 32-Ω
Internal LDO	Enabled
Control interface	I2C

### 8.2.2 Detailed Design Procedure

In this application, the device is able to use both digital and analog inputs, routing this signal into the headphone outputs.

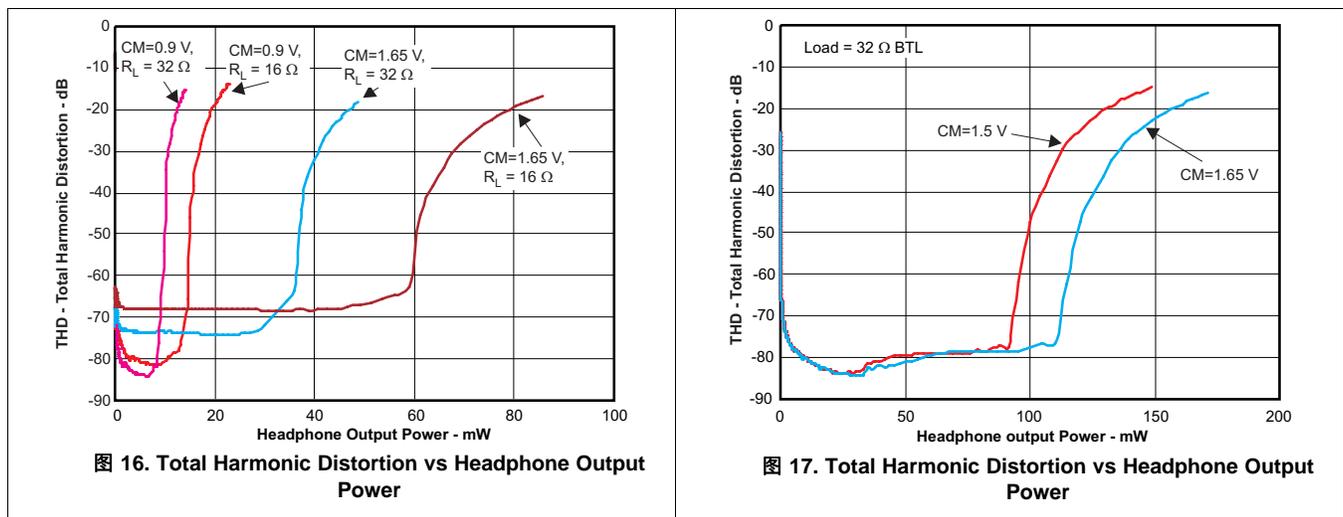
The internal LDO is being used in this application. External 1.8-V supply is used to power LDOIN, DVDD and IOVDD. AVDD is internally supplied by the LDO.

Decoupling capacitors should be used at all the supply lines. TI recommends using 0.1- $\mu$ F and 10- $\mu$ F capacitors for a better system performance.

Decoupling series capacitors must be used at the analog input and headphone output. The headphone output can be connected in single-ended mode with DC offset voltage while the decoupling series capacitor protects the speaker from the DC voltage. In addition the headphone output can be connected in a mono differential mode.

All grounds are tied together; route analog and digital paths are separated to avoid interference.

### 8.2.3 Application Curves



## 9 Power Supply Recommendations

Device power consumption largely depends on PowerTune configuration. For information on device power consumption, see the [TLV320DAC3203 Application Reference Guide](#).

## 10 Layout

### 10.1 Layout Guidelines

If the analog inputs are:

- Used, analog input traces must be routed symmetrically for true differential performance.
- Used, do not run analog input traces parallel to digital lines.
- Used, they must be AC-coupled.
- Not used, they must be grounded through a capacitor.

Use a ground plane with multiple vias for each terminal to create a low-impedance connection to GND for minimum ground noise.

Use supply decoupling capacitors and place them as close as possible to the device.

### 10.2 Layout Example

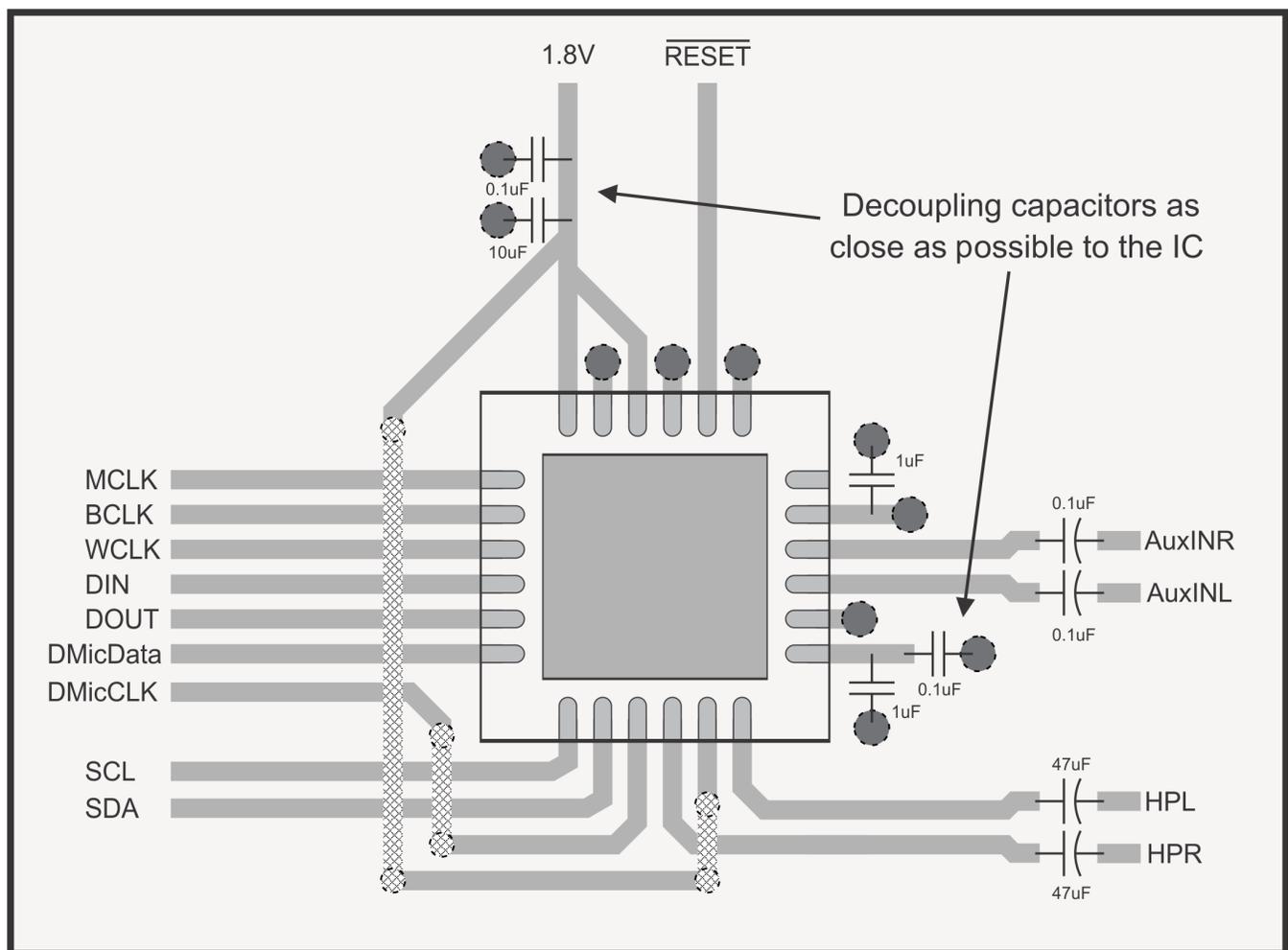


图 18. Layout Example

## 11 器件和文档支持

### 11.1 文档支持

#### 11.1.1 相关文档

请参阅如下相关文档：

- [TLV320DAC3203 应用参考指南](#)

### 11.2 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](#) 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.6 术语表

**SLYZ022** — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV320DAC3203IRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	DAC 3203I	<a href="#">Samples</a>
TLV320DAC3203IRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	DAC 3203I	<a href="#">Samples</a>
TLV320DAC3203IYZKR	ACTIVE	DSBGA	YZK	25	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DAC3203I	<a href="#">Samples</a>
TLV320DAC3203IYZKT	ACTIVE	DSBGA	YZK	25	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DAC3203I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

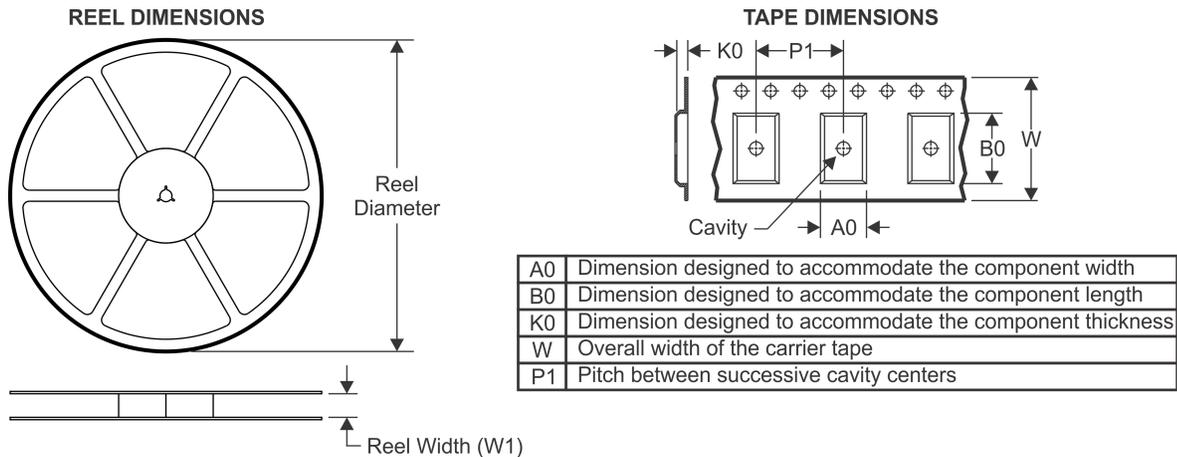
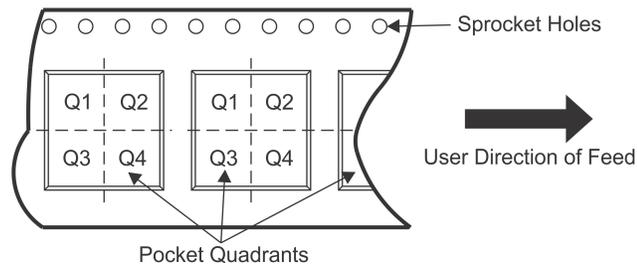
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

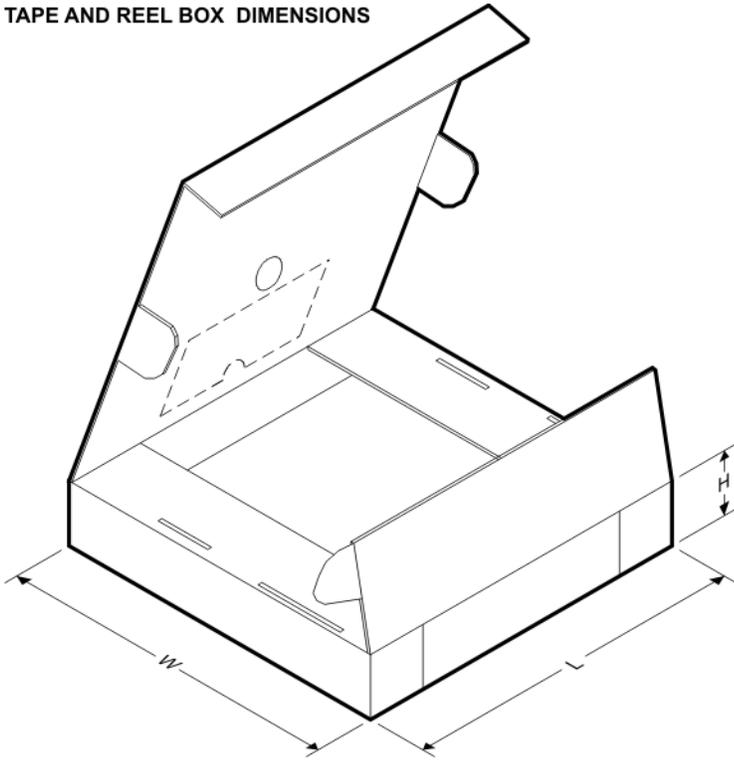
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320DAC3203IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV320DAC3203IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV320DAC3203IYZKR	DSBGA	YZK	25	3000	180.0	8.4	2.75	2.75	0.81	4.0	8.0	Q1
TLV320DAC3203IYZKT	DSBGA	YZK	25	250	180.0	8.4	2.75	2.75	0.81	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

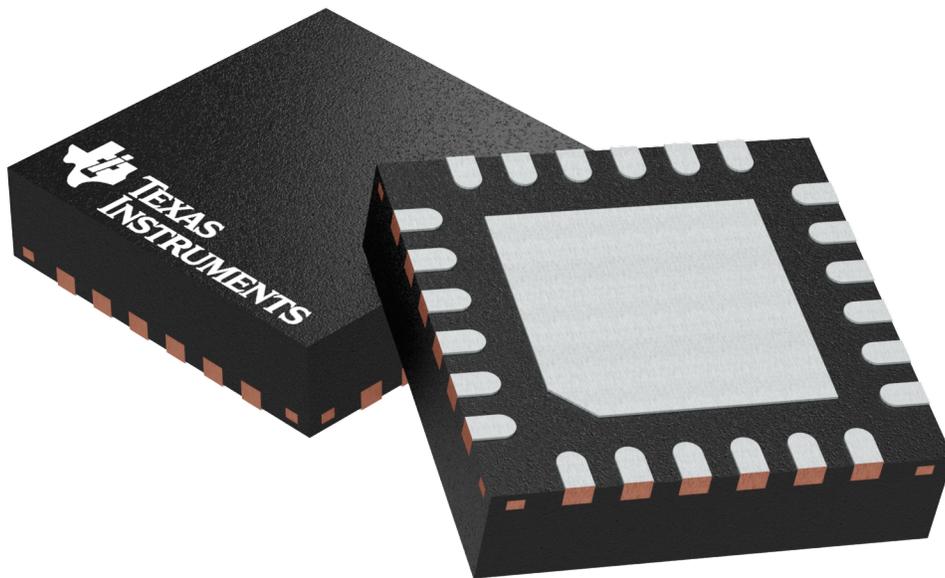
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320DAC3203IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TLV320DAC3203IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
TLV320DAC3203IYZKR	DSBGA	YZK	25	3000	182.0	182.0	20.0
TLV320DAC3203IYZKT	DSBGA	YZK	25	250	182.0	182.0	20.0

**RGE 24**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

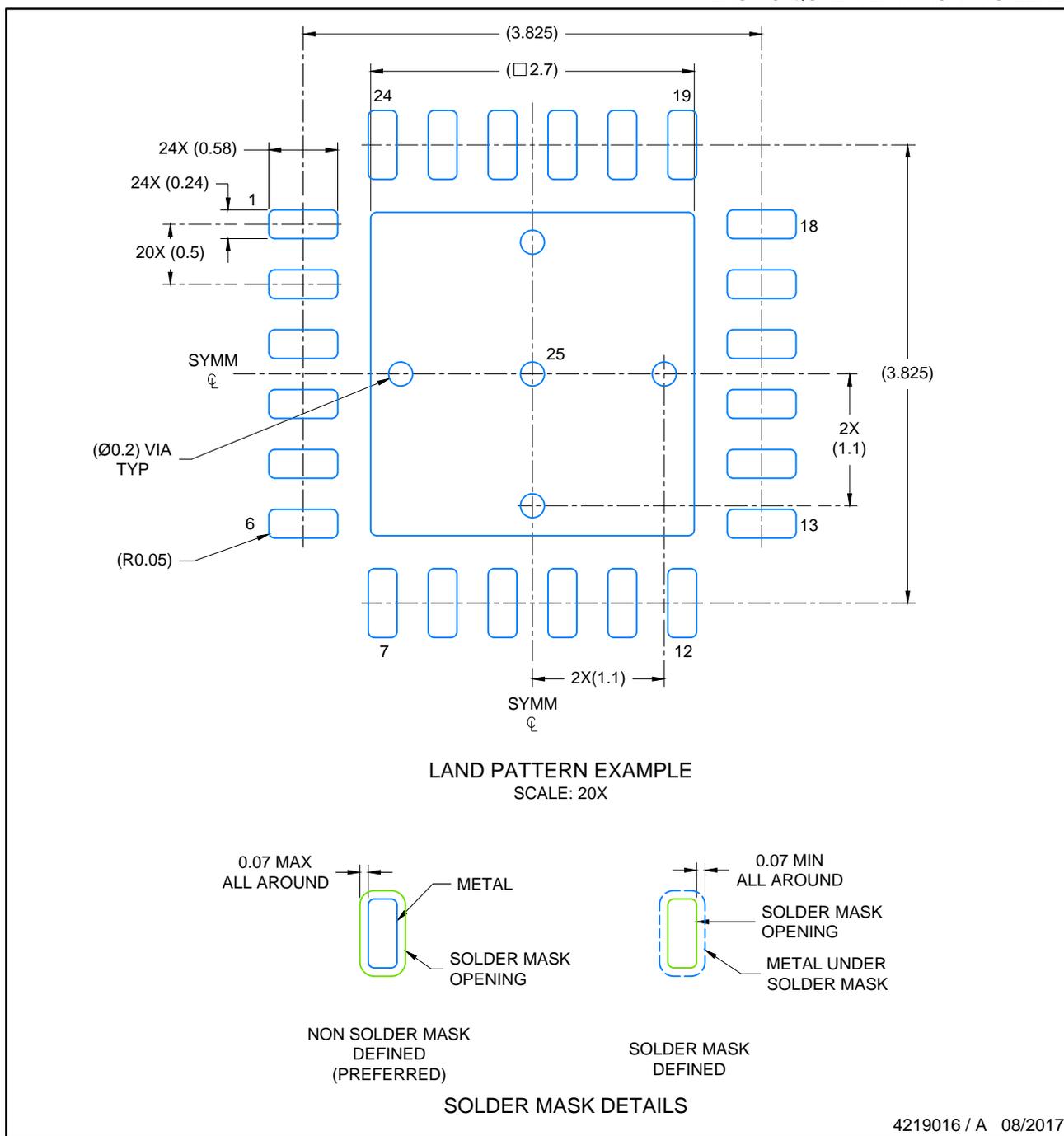
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H

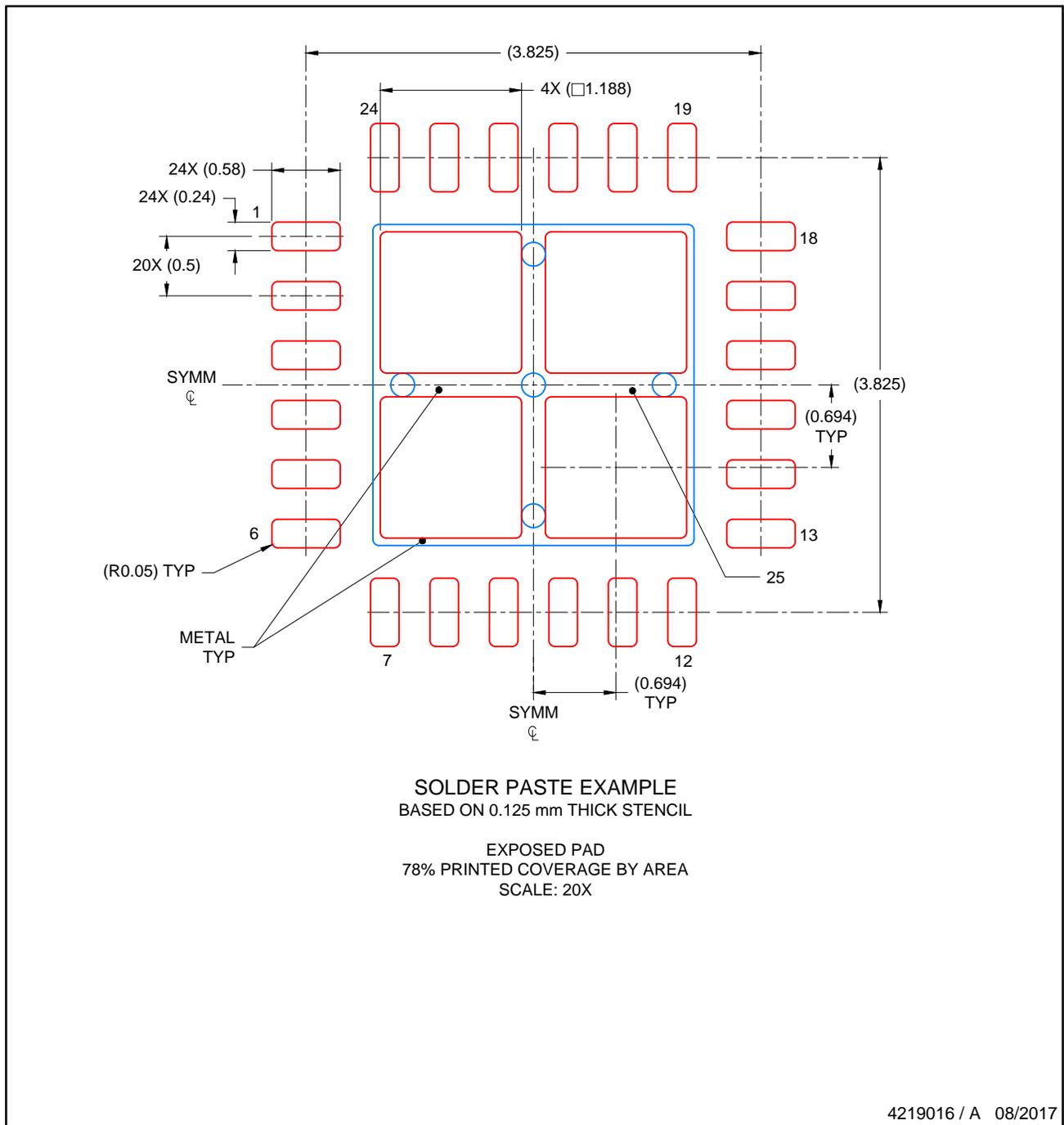




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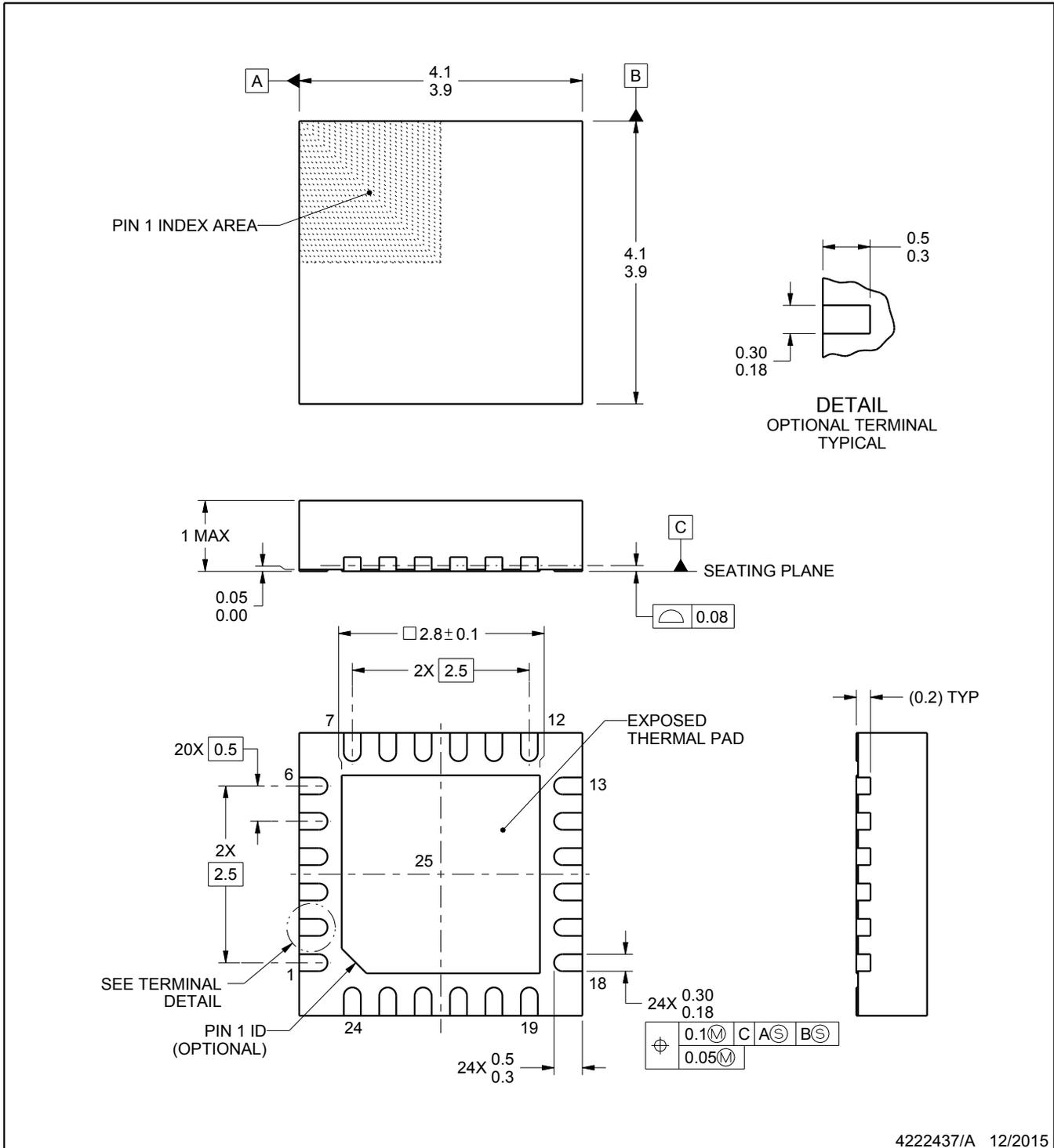
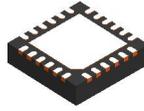
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..



4222437/A 12/2015

NOTES:

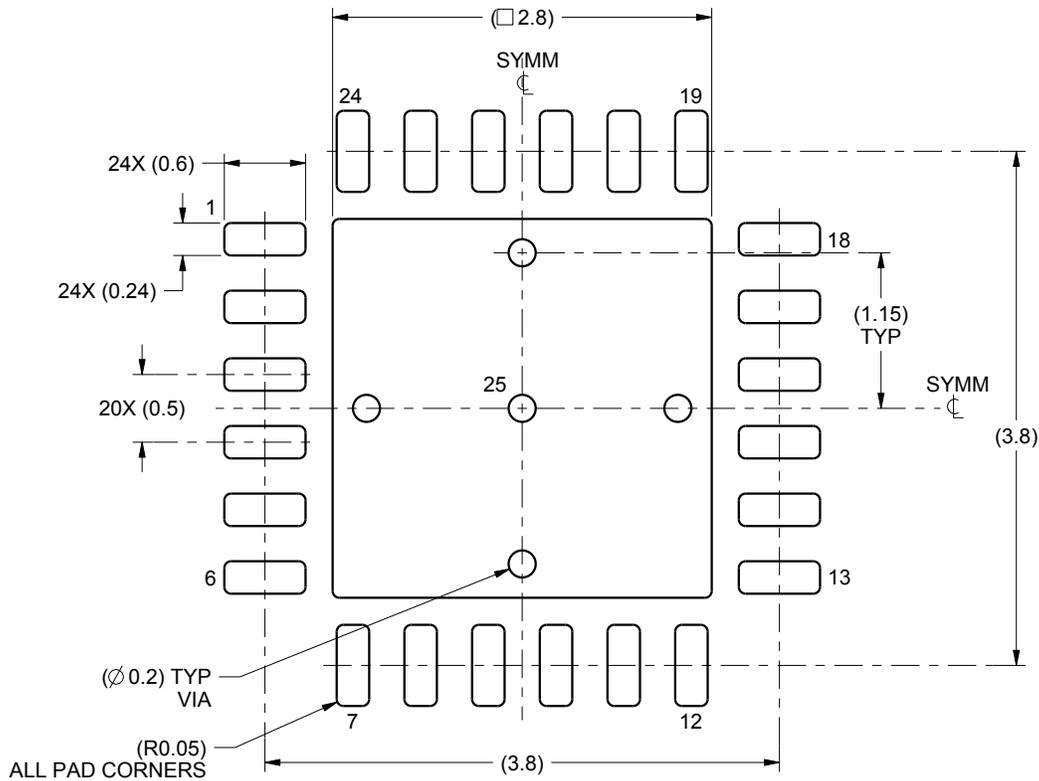
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.

# EXAMPLE BOARD LAYOUT

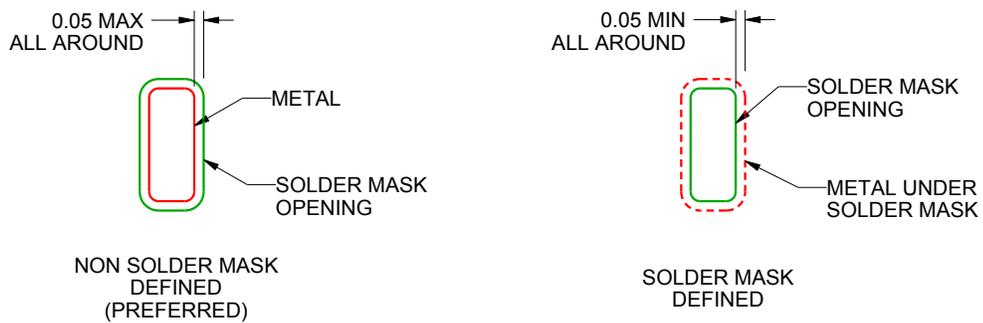
RGE0024F

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:18X



SOLDER MASK DETAILS

4222437/A 12/2015

NOTES: (continued)

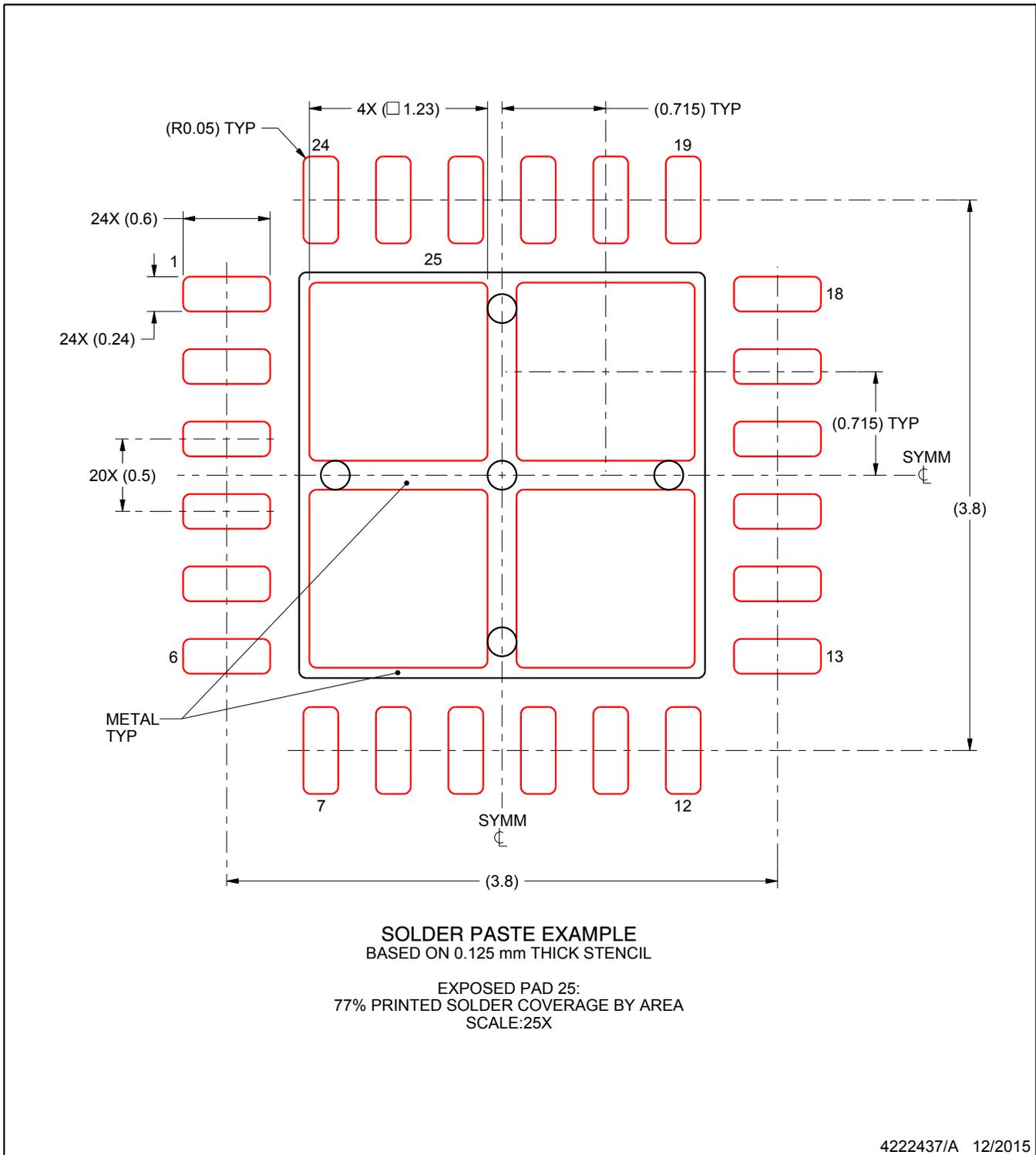
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).
- Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

RGE0024F

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

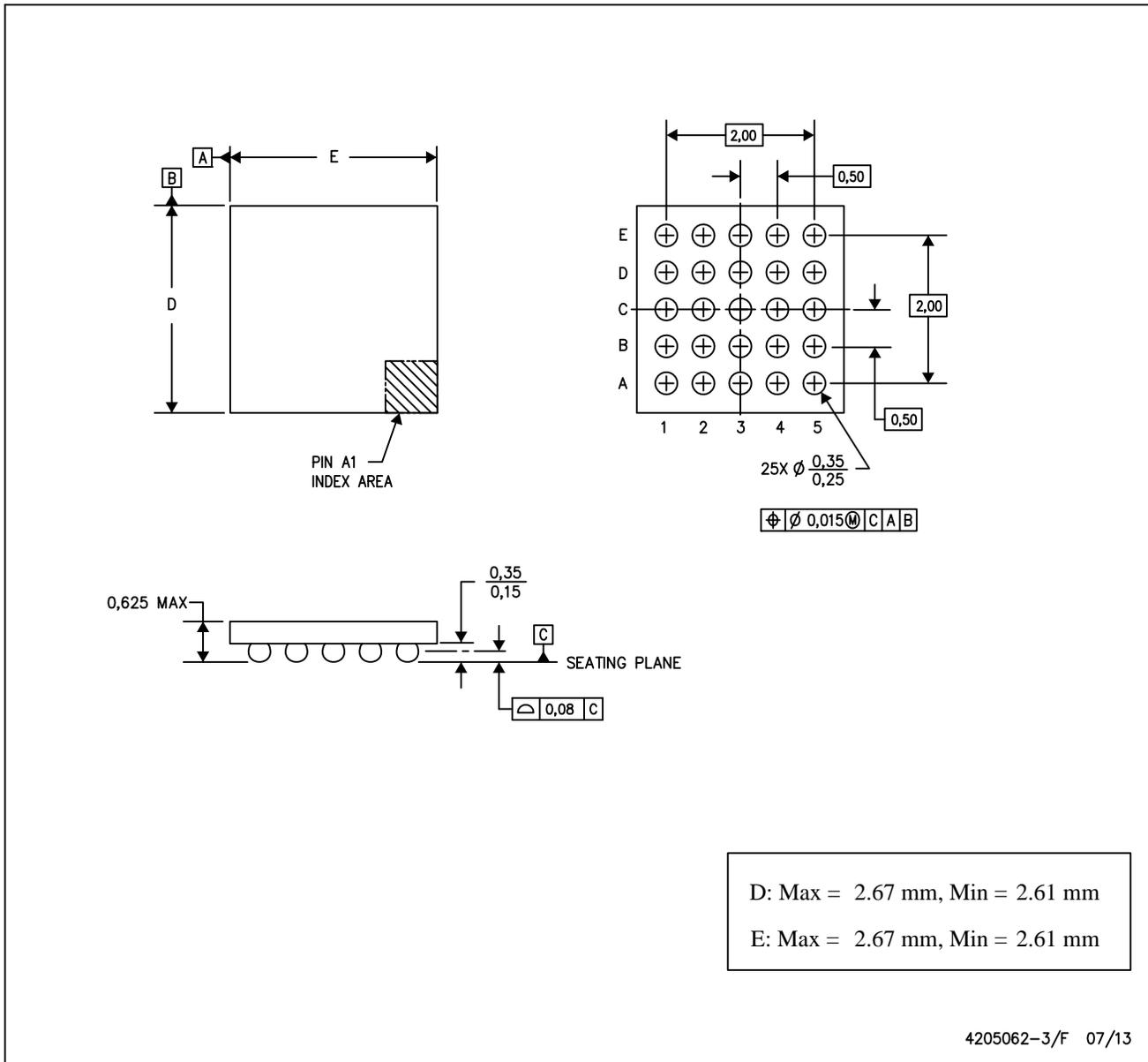


NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YZK (S-XBGA-N25)

DIE-SIZE BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
 B. This drawing is subject to change without notice.  
 C. NanoFree™ package configuration.

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