XIO2213B

XIO2213B

PCI Express™ TO 1394b OHCI WITH 3-PORT PHY

Data Manual

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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XIO2213B
PCI Express™ TO 1394b OHCI WITH 3-PORT PHY

Check for Samples: XIO2213B

1 Introduction

1.1 XIO2213B Features

- **Full ×1 PCI Express™ (PCIe) Throughput**
- **Fully Compliant With PCI Express Base Specification, Revision 1.1**
- **Utilizes 100-MHz Differential PCI Express Common Reference Clock or 125-MHz Single-Ended Reference Clock**
- **Fully Supports Provisions of IEEE Std P1394b-2002**
- **Fully Compliant With Provisions of IEEE Std 1394-1995 for a High-Performance Serial Bus and IEEE Std 1394a-2000**
- **Fully Compliant With 1394 Open Host Controller Interface (OHCI) Specification, Revision 1.1 and Revision 1.2 Draft**
- **Three IEEE Std 1394b Fully Compliant Cable Ports at 100M Bit/s, 200M Bit/s, 400M Bit/s, and 800M Bit/s**
- **Cable Ports Monitor Line Conditions for Active Connection to Remote Node**
- **Cable Power Presence Monitoring**
- **EEPROM Configuration Support to Load Global Unique ID for 1394 Fabric**
- **Support for D1, D2, $D3_{hot}$**
- **Active-State Link Power Management Saves Power When Packet Activity on the PCI Express Link Is Idle, Using Both L0s and L1 States**
- **Eight 3.3-V Multifunction General-Purpose I/O (GPIO) Terminals**

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2 Overview

The Texas Instruments XIO2213B is a single-function PCI Express™ (PCIe) to PCI local bus translation bridge, where the PCI bus interface is internally connected to a 1394b open host controller/link-layer controller with a 3-port 1394b physical layer (PHY). When the XIO2213B is properly configured, this solution provides full PCIe and 1394b functionality and performance.

The TI XIO2213B is a PCIe to PCI translation bridge, where the PCI bus interface is internally connected to a 1394b open host controller/link-layer controller with a 3-port 1394b PHY. The PCIe to PCI translation bridge is fully compatible with the PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0. Also, the bridge supports the standard PCI-to-PCI bridge programming model. The 1394b OHCI controller function is fully compatible with IEEE Std 1394b and the latest 1394 Open Host Controller Interface (OHCI) Specification.

The XIO2213B simultaneously supports up to four posted write transactions, four nonposted transactions, and four completion transactions pending in each direction at any time. Each posted write data queue and completion data queue can store up to 8K bytes of data. The nonposted data queues can store up to 128 bytes of data.

The PCIe interface supports a ×1 link operating at full 250 Mbit/s packet throughput in each direction simultaneously. Also, the bridge supports the advanced error reporting capability including ECRC as defined in the PCI Express Base Specification, Revision 1.1. Supplemental firmware or software is required to fully utilize both of these features.

Robust pipeline architecture is implemented to minimize system latency. If parity errors are detected, packet poisoning is supported for both upstream and downstream operations.

PCIe power management (PM) features include active-state link PM, PME mechanisms, and all conventional PCI D states. If the active-state link PM is enabled, the link automatically saves power when idle using the L0s and L1 states. PM active-state NAK, PM PME, and PME-to-ACK messages are supported. The bridge is compliant with the latest PCI Bus Power Management Specification and provides several low-power modes, which enable the host power system to further reduce power consumption

Eight general-purpose inputs and outputs (GPIOs), configured through accesses to the PCIe configuration space, allow for further system control and customization.

Deep FIFOs are provided to buffer 1394 data and accommodate large host bus latencies. The device provides physical write posting and a highly tuned physical data path for SBP-2 performance. The device is capable of transferring data between the PCIe bus and the 1394 bus at 100M bit/s, 200M bit/s, 400M bit/s, and 800M bit/s. The device provides three 1394 ports that have separate cable bias (TPBIAS).

As required by the 1394 Open Host Controller Interface (OHCI) Specification, internal control registers are memory mapped and nonprefetchable. This configuration header is accessed through configuration cycles specified by PCIe, and it provides plug-and-play (PnP) compatibility.

The PHY provides the digital and analog transceiver functions needed to implement a 3-port node in a cable-based 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. An optional external 2-wire serial EEPROM interface is provided to load the global unique ID for the 1394 fabric.

The XIO2213B requires an external 98.304-MHz crystal oscillator to generate a reference clock. The external clock drives an internal phase-locked loop (PLL), which generates the required reference signal. This reference signal provides the clock signals that control transmission of the outbound encoded information. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL. Data bits to be transmitted through the cable ports are latched internally, combined serially, encoded, and transmitted at 98.304, 196.608, 393.216, 491.52, or 983.04 Mbit/s (referred to as S100, S200, S400, S400B, or S800 speed, respectively) as the outbound information stream.

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To ensure that the XIO2213B conforms to IEEE Std 1394b-2002, the BMODE terminal must be asserted. The BMODE terminal does not select the cable-interface mode of operation. BMODE selects the internal PHY-section/LLC-section interface mode of operation and affects the arbitration modes on the cable. BMODE must be pulled high during normal operation.

Three package terminals are used as inputs to set the default value for three configuration status bits in the self-ID packet. They can be pulled high through a 1-kΩ resistor or hardwired low as a function of the equipment design. The PC0, PC1, and PC2 terminals indicate the default power class status for the node (the need for power from the cable or the ability to supply power to the cable). The contender bit in the PHY register set indicates that the node is a contender either for the isochronous resource manager (IRM) or for the bus manager (BM). On the XIO2213B, this bit can only be set by a write to the PHY register set. If a node is to be a contender for IRM or BM, the node software must set this bit in the PHY register set.

2.1 Related Documents

- PCI Express™ to PCI/PCI-X Bridge Specification, Revision 1.0
- PCI Express™ Base Specification, Revision 1.1
- PCI Express™ Card Electromechanical Specification, Revision 1.1
- PCI Local Bus Specification, Revision 2.3 and Revision 3.0
- PCI-to-PCI Bridge Architecture Specification, Revision 1.1
- PCI Bus Power-Management Interface Specification, Revision 1.1 and Revision 1.2
- 1394 Open Host Controller Interface (OHCI) Specification, Release 1.2
- High-Performance Serial Bus, IEEE Std 1394-1995
- High-Performance Serial Bus, Amendment 1, IEEE Std 1394a-2000
- High-Performance Serial Bus, Amendment 2, IEEE Std 1394b-2002
- Express Card Standard, Release 1.0 and Release 1.1
- *PCI Express™ Jitter and BER* white paper
- PCI Mobile Design Guide, Revision 1.1

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2.2 Documents Conventions

Throughout this data manual, several conventions are used to convey information. These conventions are:

- To identify a binary number or field, a lower-case b follows the numbers. For example, 000b is a 3-bit binary field.
- To identify a hexadecimal number or field, a lower-case h follows the numbers. For example, 8AFh is a 12-bit hexadecimal field.
- All other numbers that appear in this document that do not have either a b or h following the number are assumed to be decimal format.
- If the signal or terminal name has a bar above the name (for example, $\overline{\text{GRST}}$), this indicates the logical NOT function. When asserted, this signal is a logic low, 0, or 0b.
- Differential signal names end with P, N, +, or – designators. The P or + designators signify the positive signal associated with the differential pair. The N or – designators signify the negative signal associated with the differential pair.
- RSVD indicates that the referenced item is reserved.
- In Sections 4 through 6, the configuration space for the bridge is defined. For each register bit, the software access method is identified in an access column. The legend for this access column includes the following entries:
  - R: Read access by software
  - U: Updates by the bridge internal hardware
  - W: Write access by software
  - C: Clear an asserted bit with a write back of 1b by software. Write of zero to the field has no effect.
  - S: The field may be set by a write of one. Write of zero to the field has no effect.
  - NA: Not accessible or not applicable
- The XIO2213B consists of a PCIe to PCI translation bridge, where the secondary PCI bus is internally connected to a 1394b OHCI with a 3-port PHY. When describing functionality that is specific to the PCIe to PCI translation bridge, the term bridge is used to reduce text. The term 1394b OHCI is used to reduce text when describing the 1394b OHCI with 3-port PHY function.
- LLC refers to the 1394 link layer controller.

2.3 Ordering Information

PACKAGE	VOLTAGE	ORDERABLE PART NUMBER
167-terminal (Lead-Free) PBGA – ZAY	3.3-V and 1.5-V power terminals	XIO2213BZAY
		XIO2213BIZAY
168-terminal (Lead-Free) BGA – ZAJ	3.3-V and 1.5-V power terminals	XIO2213BZAJ

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2.4 Terminal Assignments

The XIO2213B is packaged in a 168-ball BGA (ZAJ) and a 167-ball PBGA (ZAY). For the ZAJ package Table 2-1 lists the terminals sorted by ball number. Table 2-2 lists the terminals in alphanumerical order. For the ZAY packageTable 2-3 lists the terminals sorted by ball number. Table 2-4 lists the terminals in alphanumerical order.

Table 2-1. 7 × 7 Terminals Sorted By Ball Number

BALL NO.	TERMINAL NAME
A01	VDDA_33
A02	CNA
A03	TESTM
A04	RXN
A05	RXP
A06	$\overline{\text{PHY_RESET}}$
A07	TXN
A08	TXP
A09	PC1
A10	REF1_PCIE
A11	REF0_PCIE
A12	TPBIAS2
A13	TPA2+
B01	REFCLK+
B03	PD
B04	VDDA_15
B05	VDDA_15
B06	BMODE
B07	VREG_PD
B08	PC2
B09	VDD_33_COMB
B10	VDD_33_COM_IO
B11	VDD_15_COMB
B12	$\overline{\text{PERST}}$
B13	TPA2–
C01	REFCLK–
C02	LINKON_L
C03	LPS_L
C04	VDDA_15
C05	VDDA_15
C06	VSSA_PCIE
C07	VDD_15
C08	VDDA_33
C09	VDD_33_AUX
C10	RSVD
C11	PC0
C12	$\overline{\text{GRST}}$
C13	TPB2+
D01	LREQ_L
D02	LKON/DS2_P
D03	LPS_P
D04	VSSA
D05	VSSA_PCIE
D06	VSSA_PCIE

Table 2-1. 7 × 7 Terminals Sorted By Ball Number (continued)

BALL NO.	TERMINAL NAME
D07	VSSA
D08	DVDD_CORE
D09	DVDD_CORE
D10	VDD_33
D11	RSVD
D12	RSVD
D13	TPB2–
E01	LREQ_P
E02	PINT_L
E03	PINT_P
E04	DVDD_3.3
E05	GND
E06	VSSA_PCIE
E07	VSS
E08	VSS
E09	VSSA
E10	AVDD_3.3
E11	RSVD
E12	TPBIAS1
E13	TPA1+
F01	CTL0
F02	PCLK_P
F03	PCLK_L
F04	GND
F05	GND
F06	GND
F07	GND
F08	GND
F09	GND
F10	AVDD_3.3
F11	RSVD
F12	RSVD
F13	TPA1–
G01	CTL1
G02	LCLK_P
G03	LCLK_L
G04	GND
G05	GND
G06	GND
G07	GND
G08	GND
G09	GND
G10	GND
G11	REFCLK_SEL
G12	SCL

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Table 2-1. 7 × 7 Terminals Sorted By Ball Number (continued)

BALL NO.	TERMINAL NAME
G13	TPB1+
H01	D0
H02	D1
H03	VDD_15
H04	GND
H05	GND
H06	GND
H07	GND
H08	GND
H09	VDD_15
H10	AVDD_3.3
H11	SDA
H12	$\overline{\text{CLKREQ}}$
H13	TPB1–
J01	D3
J02	D2
J03	VDD_15
J05	GND
J06	GND
J07	GND
J08	GND
J09	VDD_15
J10	AVDD_3.3
J11	RSVD
J12	TPBIAS0
J13	TPA0+
K01	D5
K02	D4
K03	VDD_33
K04	GPIO5
K05	DVDD_3.3
K06	DVDD_3.3
K07	GND
K08	VDD_33
K09	DVDD_CORE
K10	RSVD
K11	RSVD
K12	RSVD
K13	TPA0–

Table 2-1. 7 × 7 Terminals Sorted By Ball Number (continued)

BALL NO.	TERMINAL NAME
L01	D6
L02	GPIO2
L03	VDD_33
L04	GPIO3
L05	GPIO7
L06	VDD_15
L07	GND
L08	VDD_33
L09	CYCLEOUT
L10	RSVD
L11	RSVD
L12	RSVD
L13	TPB0+
M01	D7
M02	GPIO0
M03	GPIO4
M04	AVDD_3.3
M05	XO
M06	GPIO6
M07	DS1
M08	$\overline{\text{OHCI_PME}}$
M09	RSVD
M10	SE
M11	RSVD
M12	RSVD
M13	TPB0–
N01	GPIO1
N02	R1
N03	R0
N04	PLLGND
N05	XI
N06	PLLVDD_CORE
N07	PLLVDD_3.3
N08	DS0
N09	CPS
N10	SM
N11	RSVD
N12	RSVD

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Table 2-2. 7 × 7 Terminals Sorted Alphanumerically

BALL NO.	TERMINAL NAME
E10	AVDD_3.3
F10	AVDD_3.3
H10	AVDD_3.3
J10	AVDD_3.3
M04	AVDD_3.3
B06	BMODE
H12	$\overline{\text{CLKREQ}}$
A02	CNA
N09	CPS
F01	CTL0
G01	CTL1
L09	CYCLEOUT
H01	D0
H02	D1
J02	D2
J01	D3
K02	D4
K01	D5
L01	D6
M01	D7
N08	DS0
M07	DS1
E04	DVDD_3.3
K05	DVDD_3.3
K06	DVDD_3.3
D08	DVDD_CORE
D09	DVDD_CORE
K09	DVDD_CORE
E05	GND
F04	GND
F05	GND
F06	GND
F07	GND
F08	GND
F09	GND
G04	GND
G05	GND
G06	GND
G07	GND
G08	GND
G09	GND
G10	GND
H04	GND
H05	GND
H06	GND
H07	GND
H08	GND
J04	GND
J05	GND
J06	GND

Table 2-2. 7 × 7 Terminals Sorted Alphanumerically (continued)

BALL NO.	TERMINAL NAME
J07	GND
J08	GND
K07	GND
L07	GND
M02	GPIO0
N01	GPIO1
L02	GPIO2
L04	GPIO3
M03	GPIO4
K04	GPIO5
M06	GPIO6
L05	GPIO7
C12	$\overline{\text{GRST}}$
G03	LCLK_L
G02	LCLK_P
C02	LINKON_L
D02	LKON/DS2_P
C03	LPS_L
D03	LPS_P
D01	LREQ_L
E01	LREQ_P
M08	$\overline{\text{OHCI_PME}}$
C11	PC0
A09	PC1
B08	PC2
F03	PCLK_L
F02	PCLK_P
B03	PD
B12	$\overline{\text{PERST}}$
E02	PINT_L
E03	PINT_P
N04	PLLGND
N07	PLLVDD_3.3
N06	PLLVDD_CORE
N03	R0
N02	R1
A11	REF0_PCIE
A10	REF1_PCIE
C01	REFCLK–
G11	REFCLK_SEL
B01	REFCLK+
A06	$\overline{\text{PHY_RESET}}$
C10	RSVD
D11	RSVD
D12	RSVD
E11	RSVD
F11	RSVD
F12	RSVD
J11	RSVD
K10	RSVD

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Table 2-2. 7 × 7 Terminals Sorted Alphanumerically (continued)

BALL NO.	TERMINAL NAME
K11	RSVD
K12	RSVD
L10	RSVD
L11	RSVD
L12	RSVD
M09	RSVD
M11	RSVD
M12	RSVD
N11	RSVD
N12	RSVD
N13	RSVD
A04	RXN
A05	RXP
G12	SCL
H11	SDA
M10	SE
N10	SM
A03	TESTM
B07	VREG_PD
K13	TPA0–
J13	TPA0+
F13	TPA1–
E13	TPA1+
B13	TPA2–
A13	TPA2+
M13	TPB0–
L13	TPB0+
H13	TPB1–
G13	TPB1+
D13	TPB2–
C13	TPB2+
J12	TPBIAS0
E12	TPBIAS1
A12	TPBIAS2

Table 2-2. 7 × 7 Terminals Sorted Alphanumerically (continued)

BALL NO.	TERMINAL NAME
A07	TXN
A08	TXP
C07	VDD_15
H03	VDD_15
H09	VDD_15
J03	VDD_15
J09	VDD_15
L06	VDD_15
B11	VDD_15_COMB
C09	VDD_33_AUX
D10	VDD_33
K03	VDD_33
K08	VDD_33
L03	VDD_33
L08	VDD_33
B10	VDD_33_COM_IO
B09	VDD_33_COMB
B04	VDDA_15
B05	VDDA_15
C04	VDDA_15
C05	VDDA_15
A01	VDDA_33
C08	VDDA_33
E07	VSS
E08	VSS
D04	VSSA
D07	VSSA
E09	VSSA
C06	VSSA_PCIE
D05	VSSA_PCIE
D06	VSSA_PCIE
E06	VSSA_PCIE
N05	XI
M05	XO

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Table 2-3. 12 × 12 Terminals Sorted By Ball Number

BALL NO.	TERMINAL NAME
A01	REFCLK+
A02	CNA
A03	RXN
A04	RXP
A05	BMODE
A06	VREG_PD
A07	VSS
A08	TXN
A09	TXP
A10	VDDA_33
A11	PC2
A12	REF1_PCIE
A13	REF0_PCIE
A14	VSS
B01	REFCLK–
B02	TESTM
B03	PD
B04	$\overline{\text{PHY_RESET}}$
B05	VDDA_15
B06	VSSA
B07	VDDA_15
B08	VDD_15
B09	VDDA_15
B10	VDDA_15
B11	VDD_33_COMB
B12	VDD_33_AUX
B13	$\overline{\text{PERST}}$
B14	TPA2+
C01	LPS_L
C02	LPS_P
C03	VDDA_33
C04	VSSA_PCIE
C05	VSSA_PCIE
C06	VSSA_PCIE
C07	VSSA_PCIE
C08	DVDD_3.3
C09	DVDD_CORE
C10	VSSA
C11	VDD_33_COM_IO
C12	VDD_15_COMB
C13	$\overline{\text{GRST}}$
C14	TPA2–
D01	LKON/DS2_P
D02	PINT_L
D03	PINT_P
D12	RSVD
D13	RSVD
D14	TPB2+
E01	LINKON_L
E02	LREQ_P

Table 2-3. 12 × 12 Terminals Sorted By Ball Number (continued)

BALL NO.	TERMINAL NAME
E03	VDD_33
E06	GND
E07	GND
E08	PC1
E09	PC0
E10	AVDD_3.3
E12	RSVD
E13	TPBIAS2
E14	TPB2–
F01	PCLK_P
F02	LREQ_L
F03	DVDD_CORE
F05	VSSA
F06	GND
F07	GND
F08	GND
F09	GND
F10	AVDD_3.3
F12	RSVD
F13	RSVD
F14	TPA1+
G01	PCLK_L
G02	LCLK_L
G03	VDD_15
G05	GND
G06	GND
G07	GND
G08	GND
G09	GND
G10	VDD_33
G12	RSVD
G13	TPBIAS1
G14	TPA1–
H01	CTL0
H02	LCLK_P
H03	VDD_15
H05	GND
H06	GND
H07	GND
H08	GND
H09	GND
H10	VDD_33
H12	SDA
H13	REFCLK_SEL
H14	TPB1+
J01	CTL1
J02	D0
J03	DVDD_3.3
J05	GND
J06	GND

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Table 2-3. 12 × 12 Terminals Sorted By Ball Number (continued)

BALL NO.	TERMINAL NAME
J07	GND
J08	GND
J09	AVDD_3.3
J10	VDD_33
J12	$\overline{\text{CLKREQ}}$
J13	SCL
J14	TPB1–
K01	D2
K02	D1
K03	DVDD_3.3
K05	GND
K06	GND
K07	GND
K08	GND
K09	AVDD_3.3
K10	VDD_15
K12	RSVD
K13	TPBIAS0
K14	TPA0+
L01	D3
L02	D4
L03	D5
L12	RSVD
L13	RSVD
L14	TPA0–
M01	R1
M02	D6
M03	D7
M04	AVDD_3.3
M05	VDD_33
M06	VDD_15
M07	PLLVDD_CORE
M08	RSVD
M09	DVDD_CORE

Table 2-3. 12 × 12 Terminals Sorted By Ball Number (continued)

BALL NO.	TERMINAL NAME
M10	AVDD_3.3
M11	RSVD
M12	RSVD
M13	RSVD
M14	TPB0+
N01	R0
N02	GPIO1
N03	GPIO3
N04	GPIO4
N05	PLLGND
N06	GPIO7
N07	PLLVDD_3.3
N08	CYCLEOUT
N09	DS0
N10	RSVD
N11	RSVD
N12	RSVD
N13	RSVD
N14	TPB0–
P01	GPIO0
P02	GPIO2
P03	RSVD
P04	XI
P05	GPIO5
P06	GPIO6
P07	VDD_15
P08	OHCI_PME
P09	DS1
P10	RSVD
P11	RSVD
P12	CPS
P13	SE
P14	SM

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Table 2-4. 12 × 12 Terminals Sorted Alphanumerically

TERMINAL NAME	BALL NO.
AVDD_3.3	E10
AVDD_3.3	F10
AVDD_3.3	J09
AVDD_3.3	K09
AVDD_3.3	M10
AVDD_3.3	M04
BMODE	A05
$\overline{\text{CLKREQ}}$	J12
CNA	A02
CPS	P12
CTL0	H01
CTL1	J01
CYCLEOUT	N08
D0	J02
D1	K02
D2	K01
D3	L01
D4	L02
D5	L03
D6	M02
D7	M03
DS0	N09
DS1	P09
DVDD_3.3	C08
DVDD_3.3	J03
DVDD_3.3	K03
DVDD_CORE	C09
DVDD_CORE	F03
DVDD_CORE	M09
GND	E06
GND	E07
GND	F06
GND	F07
GND	F08
GND	F09
GND	G05
GND	G06
GND	G07
GND	G08
GND	G09
GND	H05
GND	H06
GND	H07
GND	H08
GND	H09
GND	J05

Table 2-4. 12 × 12 Terminals Sorted Alphanumerically (continued)

TERMINAL NAME	BALL NO.
GND	J06
GND	J07
GND	J08
GND	K05
GND	K06
GND	K07
GND	K08
GPIO0	P01
GPIO1	N02
GPIO2	P02
GPIO3	N03
GPIO3	N04
GPIO5	P05
GPIO6	P06
GPIO7	N06
$\overline{\text{GRST}}$	C13
LCLK_L	G02
LCLK_P	H02
LINKON_L	E01
LKON/DS2_P	D01
LPS_L	C01
LPS_P	C02
LREQ_L	F02
LREQ_P	E02
$\overline{\text{OHCI_PME}}$	P08
PC0	E09
PC1	E08
PC2	A11
PCLK_L	G01
PCLK_P	F01
PD	B03
$\overline{\text{PERST}}$	B13
PINT_L	D02
PINT_P	D03
PLLGND	N05
PLLVDD_3.3	N07
PLLVDD_CORE	M07
R0	N01
R1	M01
REF0_PCIE	A13
REF1_PCIE	A12
REFCLK-	B01
REFCLK_SEL	H13
REFCLK+	A01
$\overline{\text{PHY_RESET}}$	B04
RSVD	G12

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Table 2-4. 12 × 12 Terminals Sorted Alphanumerically (continued)

TERMINAL NAME	BALL NO.
RSVD	F13
RSVD	F12
RSVD	E12
RSVD	D12
RSVD	D13
RSVD	M08
RSVD	N10
RSVD	P10
RSVD	P11
RSVD	N11
RSVD	M11
RSVD	N12
RSVD	N13
RSVD	M12
RSVD	M13
RSVD	L13
RSVD	K12
RSVD	L12
RXN	A03
RXP	A04
SCL	J13
SDA	H12
SE	P13
SM	P14
TESTM	B02
VREG_PD	A06
TPA0–	L14
TPA0+	K14
TPA1–	G14
TPA1+	F14
TPA2–	C14
TPA2+	B14
TPB0–	N14
TPB0+	M14
TPB1–	J14
TPB1+	H14
TPB2–	E14
TPB2+	D14

Table 2-4. 12 × 12 Terminals Sorted Alphanumerically (continued)

TERMINAL NAME	BALL NO.
TPBIAS0	K13
TPBIAS1	G13
TPBIAS2	E13
TXN	A08
TXP	A09
VDD_15	G03
VDD_15	H03
VDD_15	K10
VDD_15	M06
VDD_15	B08
VDD_15_COMB	C12
VDD_33	E03
VDD_33	G10
VDD_33	H10
VDD_33	J10
VDD_33	M05
VDD_33_AUX	B12
VDD_33_COM_IO	C11
VDD_33_COMB	B11
VDDA_15	B10
VDDA_15	B09
VDDA_15	B07
VDDA_15	B05
VDDA_33	C03
VDDA_33	A10
VDD_15	P07
VSS	A14
VSS	A07
VSSA	F05
VSSA	C10
VSSA	B06
VSSA_PCIE	C04
VSSA_PCIE	C05
VSSA_PCIE	C06
VSSA_PCIE	C07
XI	P04
RSVD	P03

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2.5 Terminal Descriptions

The following tables give a description of the terminals. These terminals are grouped in tables by functionality. Each table includes the terminal name, terminal number, I/O type, and terminal description.

The following list describes the different input/output cell types that appear in the terminal description tables:

- HS DIFF IN = High-speed differential input
- HS DIFF OUT = High-speed differential output
- LV CMOS = 3.3-V low-voltage CMOS input or output with 3.3-V clamp rail
- BIAS = Input/output terminals that generate a bias voltage to determine a driver's operating current
- Feedthrough = Terminals that connect directly to macros within the part and not through an input or output cell
- PWR = Power terminal
- GND = Ground terminal

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Table 2-5. Power-Supply Terminals

SIGNAL	BALL NO.		I/O TYPE	EXTERNAL PARTS	DESCRIPTION
	ZAY PACKAGE	ZAJ PACKAGE			
V_{DD_15}	G03 H03 K10 M06 B08 P07	C07 H03 H09 J03 J09 L06	PWR	Bypass capacitors	1.5-V digital core power for the link
V_{DDA_15}	B10 B09 B07 B05	B04 B05 C04 C05	PWR	Filter	1.5-V analog power for the link
V_{DD_33}	E03 M05 J10 H10 G10	D10 K03 K08 L03 L08	PWR	Bypass capacitors	3.3-V digital I/O power for the link
$V_{DD_33_AUX}$	B12	C09			This terminal is connected to VSS through a pulldown resistor, since the XIO2213B does not support auxiliary power.
V_{DDA_33}	C03 A10	A01 C08	PWR	Filter	3.3-V analog power for the link. This supply terminal is separated from the other power terminals internal to the device to provide noise isolation.
DVDD_CORE	C09 F03 M09	D08 D09 K09	PWR	Bypass capacitors	Digital 1.95-V circuit power for the PHY. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 µF and 0.001 µF. An additional 1-µF capacitor is required for voltage regulation. These supply terminals are separated from the other power terminals internal to the device to provide noise isolation.
PLLVDD_CORE	M07	N06	PWR	Bypass capacitors	PLL 1.95-V circuit power for the PHY. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 µF and 0.001 µF. An additional 1-µF capacitor is required for voltage regulation, and the PLLVDD_CORE terminals must be separate from the DVDD_CORE terminals. These supply terminals are separated from the other power terminals internal to the device to provide noise isolation.
DVDD_33	C08 J03 K03	E04 K05 K06	PWR	Bypass capacitors	3.3-V digital I/O power for the PHY
AVDD_33	M04 E10 F10 J09 K09 M10	E10 F10 H10 J10 M04	PWR	Filter	3.3-V analog power for the PHY
PLLVDD_33	N07	N07	PWR	Bypass capacitors	PLL 3.3-V circuit power for the PHY. This supply terminal is separated from the other power terminals internal to the device to provide noise isolation. The PLLVDD_33 and V_{DDA_33} pins should be connected together with a low-dc-impedance connection on the circuit board.
$V_{DD_15_COMB}$	C12	B11	PWR	Bypass capacitors	Internal 1.5-V main power output for external bypass capacitor filtering **Caution**: Do not use this terminal to supply external power to other devices.
$V_{DD_33_COMB}$	B11	B09	PWR	Bypass capacitors	Internal 3.3-V main power output for external bypass capacitor filtering **Caution**: Do not use this terminal to supply external power to other devices.
$V_{DD_33_COMBIO}$	C11	B10	PWR	Bypass capacitors	Internal 3.3-V IO power output for external bypass capacitor filtering **Caution**: Do not use this terminal to supply external power to other devices.

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Table 2-6. Ground Terminals

SIGNAL	BALL NO.		I/O TYPE	DESCRIPTION
	ZAY PACKAGE	ZAJ PACKAGE		
V_{SS}	A07 A14	E07 E08	GND	Digital ground for link
V_{SSA}	B06 C10 F05	D04 D07 E09	GND	Analog ground for link
V_{SSA_PCIE}	C04 C05 C06 C07	C06 D05 D06 E06	GND	Analog ground for PCIe function
PLLGND	N05	N04	GND	PLL circuit ground. This terminal must be tied to the low-impedance circuit-board ground plane.
GND	E06 E07 F06 F07 F08 F09 G05 G06 G07 G08 G09 H05 H06 H07 H08 H09 J05 J06 J07 J08 K05 K06 K07 K08	E05 F04 F05 F06 F07 F08 F09 G04 G05 G06 G07 G08 G09 G10 H04 H05 H06 H07 H08 J04 J05 J06 J07 J08 K07 L07	GND	Ground. These terminals must be tied together to the low-impedance circuit-board ground plane.

Table 2-7. PCIe Terminals

SIGNAL	BALL NO.		I/O TYPE	EXTERNAL PARTS	DESCRIPTION
	ZAY PACKAGE	ZAJ PACKAGE			
$\overline{\text{PERST}}$	B13	B12	I		PCI Express reset. $\overline{\text{PERST}}$ identifies when the system power is stable and generates an internal power-on reset. Note: The $\overline{\text{PERST}}$ input buffer has hysteresis.
REF0_PCIE REF1_PCIE	A13 A12	A11 A10	I/O	External resistor	External reference resistor + and terminals for setting TX driver current. An external resistor is connected between terminals REF0_PCIE and REF1_PCIE.
RXP RXN	A04 A03	A05 A04	DI		High-speed receive pair. RXP and RXN comprise the differential receive pair for the single PCIe lane supported.
TXP TXN	A09 A08	A08 A07	DO	Series capacitors	High-speed transmit pair. TXP and TXN comprise the differential transmit pair for the single PCIe lane supported.

Table 2-8. Clock Terminals

SIGNAL	BALL NO.		I/O TYPE	EXTERNAL PARTS	DESCRIPTION
	ZAY PACKAGE	ZAJ PACKAGE			
REFCLK_SEL	H13	G11	I	Pullup or pulldown resistor	Reference clock select. This terminal selects the reference clock input. 0 = 100-MHz differential common reference clock used 1 = 125-MHz single-ended reference clock used
REFCLK+	A01	B01	DI		Reference clock positive. REFCLK+ and REFCLK– comprise the differential input pair for the 100-MHz system reference clock. For a single-ended, 125-MHz system reference clock, use the REFCLK+ input.
REFCLK–	B01	C01	DI	Capacitor to V_{SS} for single-ended mode	Reference clock negative. REFCLK+ and REFCLK– comprise the differential input pair for the 100-MHz system reference clock. For a single-ended, 125-MHz system reference clock, attach a capacitor from REFCLK– to V_{SS}.
$\overline{\text{CLKREQ}}$	J12	H12	O		Clock request. This terminal is used to support the clock request protocol.
XI	P04	N05	I		Oscillator input. This terminal connects to a 98.304-MHz low-jitter external oscillator. XI is a 1.8-V CMOS input. Oscillator jitter must be 5-ps RMS or better. If only 3.3-V oscillators can be acquired, great care must be taken to not introduce significant jitter by the means used to level shift from 3.3 V to 1.8 V. If a resistor divider is used, a high-current oscillator and low-value resistors must be used to minimize RC time constants.

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Table 2-9. 1394 Terminals

SIGNAL	BALL NO.		I/O TYPE	DESCRIPTION
	ZAY PACKAGE	ZAJ PACKAGE		
CNA	A02	A02	I/O	Cable not active. This terminal is asserted high when there are no ports receiving incoming bias voltage. If it is not used, this terminal should be left unconnected.
CPS	P12	N09	I	Cable power status. This terminal is normally connected to cable power through a 400-kΩ resistor. This circuit drives an internal comparator that detects the presence of cable power. If CPS is not used to detect cable power, this terminal must be connected to V_{SSA}.
DS0	N09	N08	I	Data-strobe-only mode for port 0. IEEE Std 1394a-2000-only port-0-enable programming terminal. On hardware reset, this terminal allows the user to select whether port 0 acts like an IEEE Std 1394b-2002 bilingual port (terminal at logic 0) or as an IEEE Std 1394a-2000-only port (terminal at logic 1). Programming is accomplished by tying the terminal low through a 1-kΩ or smaller resistor (to enable IEEE Std 1394b-2002 bilingual mode) or high through a 10-kΩ or smaller resistor (to enable IEEE Std 1394a-2000-only mode).
DS1	P09	M07	I	Data-strobe-only mode for port 1. IEEE Std 1394a-2000-only port-1-enable programming terminal. On hardware reset, this terminal allows the user to select whether port 1 acts like an IEEE Std 1394b-2002 bilingual port (terminal at logic 0) or as an IEEE Std 1394a-2000-only port (terminal at logic 1). Programming is accomplished by tying the terminal low through a 1-kΩ or smaller resistor (to enable IEEE Std 1394b-2002 bilingual mode) or high through a 10-kΩ or smaller resistor (to enable IEEE Std 1394a-2000-only mode).
PC0 PC1 PC2	E09 E08 A11	C11 A09 B08	I	Power-class programming. On hardware reset, these inputs set the default value of the power class indicated during self-ID. Programming is done by tying the terminals high through a 1-kΩ or smaller resistor or by tying directly to ground through a 1-kΩ or smaller resistor. Bus holders are built into these terminals.
R0 R1	N01 M01	N03 N02	I/O	Current-setting resistor. These terminals are connected to an external resistance to set the internal operating currents and cable driver output currents. A resistance of 6.34 kΩ ± 1% is required to meet the IEEE Std 1394-1995 output voltage limits.
TPA0P TPA0N TPB0P TPB0N	K14 L14 M14 N14	J13 K13 L13 M13	I/O	Port 0 twisted-pair cable A differential. Board trace lengths from each pair of positive and negative differential signal pins must be matched and as short as possible to the external load resistors and to the cable connector. For an unused port, TPA+ and TPA– can be left open.
TPA1P TPA1N TPB1P TPB1N	F14 G14 H14 J14	E13 F13 G13 H13	I/O	Port 1 twisted-pair cable A differential. Board trace lengths from each pair of positive and negative differential signal pins must be matched and as short as possible to the external load resistors and to the cable connector. For an unused port, TPA+ and TPA– can be left open.
TPA2P TPA2N TPB2P TPB2N	B14 C14 D14 E14	A13 B13 C13 D13	I/O	Port 2 twisted-pair cable A differential. Board trace lengths from each pair of positive and negative differential signal pins must be matched and as short as possible to the external load resistors and to the cable connector. For an unused port, TPA+ and TPA– can be left open.
TPBIAS0 TPBIAS1 TPBIAS2	K13 G13 E13	J12 E12 A12	O	Twisted-pair bias. These terminals provide the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers, and for signaling to the remote nodes that there is an active cable connection in IEEE Std 1394a-2000 mode. Each of these terminals, except for an unused port, must be decoupled with a 1-μF capacitor to ground. For the unused port, this terminal can be left unconnected.
PCLK_L	G01	F03	I	PHY-section clock. This terminal must be connected to the PCLK_P output of the PHY section.
PCLK_P	F01	F02	O	PHY-section clock. This terminal must be connected to the PCLK_L input of the LLC section.
LCLK_L	G02	G03	O	LLC-section clock. This terminal must be connected to the LCLK_P input terminal of the PHY section.
LCLK_P	H02	G02	I	LLC-section clock. This terminal must be connected to the LCLK_L output terminal of the LLC section.
LPS_L	C01	C03	O	LLC-section power status. This terminal must be connected to the LPS_P input terminal of the PHY section.
LPS_P	C02	D03	I	Link power status. This terminal must be connected to the LPS_L ouput terminal of the LLC section.
PINT_L	D02	E02	I	PHY-section interrupt. The PHY section uses this signal to transfer status and interrupt information serially to the LLC section. This terminal must be connected to the PINT_P output of the PHY section.

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Table 2-9. 1394 Terminals (continued)

SIGNAL	BALL NO.		I/O TYPE	DESCRIPTION
	ZAY PACKAGE	ZAJ PACKAGE		
PINT_P	D03	E03	O	PHY-section interrupt. PINT_P is a serial input to the LLC section from the PHY section that is used to transfer status, register, interrupt, and other information to the link. Information encoded on PINT_P is synchronous to PCLK_P. This terminal must be connected to the PINT_L input of the LLC section.
LKON/DS2_P	D01	D02	I/O	Link-on notification. If port is to operate in DS mode or is unused then it is necessary to pull the terminal high through a 470-Ω or smaller resistor. This terminal must also be connected to the LINKON_L input terminal of the LLC section via a 1-kΩ series resistor. A bus holder is built into this terminal. If the port is to operate in bilingual mode then the terminal should be tied low via a 1-kΩ resistor and directly connected to the link's LINKON_L pin with no series termination. After hardware reset, this terminal is the link-on output, which notifies the LLC section or other power-up logic to power up and become active. The link-on output is a square-wave signal with a period of approximately 163 ns (eight PCLK cycles) when active. The link-on output is otherwise driven low, except during hardware reset when it is high impedance. The link-on output is activated if the LLC section is inactive (the LPS input inactive or the LCtrl bit cleared) and when any of the following occurs: a) The XIO2213B receives a link-on PHY packet addressed to this node. b) The PEI (port-event interrupt) register bit is 1. c) Any of the configuration-timeout interrupt (CTOI), cable-power-status interrupt (CPSI), or state-time-out interrupt (STOI) register bits are 1, and the resuming-port interrupt enable (RPIE) register bit also is 1. d) The PHY is power cycled and the power class is 0 through 4. Once activated, the link-on output is active until the LLC section becomes active (both the LPS_L input active and the LCtrl bit set). The PHY section also deasserts the link-on output when a bus reset occurs unless the link-on output is otherwise active because one of the interrupt bits is set (that is, the link-on output is active due solely to the reception of a link-on PHY packet). In the case of power cycling, the LKON signal must stop after 167 ms if the previous conditions have not been met. Note: If an interrupt condition exists that otherwise causes the link-on output to be activated if the LLC section were inactive, the link-on output is activated when the LLC section subsequently becomes inactive.
LINKON_L	E01	C02	I/O	Link-on notification. LINKON_L is an input to the LLC section from the PHY section that is used to provide notification that a link-on packet has been received or an event, such as a port connection, has occurred. This I/O only has meaning when LPS is disabled. This includes the D0 (uninitialized), D2, and D3 power states. If LINKON_L becomes active in the D0 (uninitialized), D2, or D3 power state, the XIO2213B device sets bit 15 (PME_STS) in the power-management control and status register in the PCI configuration space at offset 48h. This terminal must be connected to the LKON output terminal of the PHY section.
LREQ_L	F02	D01	O	LLC-section request. The LLC section uses this output to initiate a service request to the PHY section.This terminal must be connected to the LREQ_P input of the PHY section.
LREQ_P	E02	E01	I	LLC-section request. LREQ_P is a serial input from the LLC section to the PHY section used to request packet transmissions, read and write PHY section registers, and to indicate the occurrence of certain link events that are relevant to the PHY section. Information encoded on LREQ_P is synchronous to LCLK_P.This terminal must be connected to the LREQ_L output of the LLC section.
$\overline{\text{PHY_RESET}}$	B04	A06	I	Reset for the 1394 PHY logic
CTL1 CTL0	J01 H01	G01 F01	I/O	Control. CTL[1:0] are bidirectional control bus signals that are used to indicate the phase of operation of the PHY link interface. Upon a reset of the interface, this bus is driven by the PHY. When driven by the PHY, information on CTL[1:0] is synchronous to PCLK. When driven by the link, information on CTL[1:0] is synchronous to LCLK. If not implemented, these terminals should be left unconnected.
D0 D1 D2 D3 D4 D5 D6 D7	J02 K02 K01 L01 L02 L03 M02 M03	H01 H02 J02 J01 K02 K01 L01 M01	I/O	Data. D[7:0] comprise a bidirectional data bus that is used to carry 1394 packet data, packet speed, and grant type information between the PHY and the link. Upon a reset of the interface, this bus is driven by the PHY. When driven by the PHY, information on D[7:0] is synchronous to PCLK. When driven by the link, information on D[7:0] is synchronous to LCLK. If not implemented, these terminals should be left unconnected.

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Table 2-10. Reserved Terminals

SIGNAL	BALL NO.		I/O TYPE	DESCRIPTION
	ZAY PACKAGE	ZAJ PACKAGE		
RSVD	E12 F12 F13 K12 L12 L13 M11 M12 M13 N10 N11 N12 N13 P03 P10 P11	D11 E11 F12 J11 K10 K11 K12 L10 L11 L12 M05 M11 M12 N11 N12 N13	I/O	Reserved, do not connect to external signals.
RSVD	D12 D13 G12 M08	C10 D12 F11 M09	I	Must be connected to V_{SS}.

Table 2-11. Miscellaneous Terminals

SIGNAL	BALL NO.		I/O TYPE	DESCRIPTION
	ZAY PACKAGE	ZAJ PACKAGE		
GPIO0	P01	M02	I/O	General-purpose I/O 0. This terminal functions as a GPIO controlled by bit 0 (GPIO0_DIR) in the GPIO control register (see Section 4.60). Note: This terminal has an internal active pullup resistor.
GPIO1	N02	N01	I/O	General-purpose I/O 1. This terminal functions as a GPIO controlled by bit 1 (GPIO1_DIR) in the GPIO control register (see Section 4.60). Note: This terminal has an internal active pullup resistor.
GPIO2	P02	L02	I/O	General-purpose I/O 2. This terminal functions as a GPIO controlled by bit 2 (GPIO2_DIR) in the GPIO control register (see Section 4.60). Note: This terminal has an internal active pullup resistor.
GPIO3	N03	L04	I/O	General-purpose I/O 3. This terminal functions as a GPIO controlled by bit 3 (GPIO3_DIR) in the GPIO control register (see Section 4.60). Note: This terminal has an internal active pullup resistor.
GPIO4	N04	M03	I/O	General-purpose I/O 4. This terminal functions as a GPIO controlled by bit 4 (GPIO4_DIR) in the GPIO control register (see Section 4.60). Note: This terminal has an internal active pullup resistor.
GPIO5	P05	K04	I/O	General-purpose I/O 5. This terminal functions as a GPIO controlled by bit 5 (GPIO5_DIR) in the GPIO control register (see Section 4.60). Note: This terminal has an internal active pullup resistor.
GPIO6	P06	M06	I/O	General-purpose I/O 6. This terminal functions as a GPIO controlled by bit 6 (GPIO6_DIR) in the GPIO control register (see Section 4.60). Note: This terminal has an internal active pullup resistor.
GPIO7	N06	L05	I/O	General-purpose I/O 7. This terminal functions as a GPIO controlled by bit 7 (GPIO7_DIR) in the GPIO control register (see Section 4.60). Note: This terminal has an internal active pullup resistor.
$\overline{\text{OHCI_PME}}$	P08	M08	O	OHCI power-management event. This is an optional signal that can be used by a device to request a change in the device or system power state. This signal must be enabled by software.
CYCLEOUT	N08	L09	O	Cycle out. This terminal provides an 8-kHz cycle timer synchronization signal. If not implemented, this terminal should be left unconnected.
PD	B03	B03	I	Power down. A high on this terminal turns off all internal circuitry, except the cable-active monitor circuits that control the CNA output. Asserting PD high also activates an internal pulldown to force a reset of the internal control logic. If PD is not used, this terminal must be connected to V_{SS}.
$\overline{\text{GRST}}$	C13	C12	I	Global power reset. This reset brings all of the XIO2213B internal link registers to their default states. This should be a one-time power-on reset. This terminal has hysteresis and an integrated pullup resistor.
SCL	J13	G12	I/O	Serial-bus clock. This signal is used as a serial bus clock when a pullup is detected on SDA or when the SBDETECT bit is set in the serial bus control and status register. Note: This terminal has an internal active pullup resistor.

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Table 2-11. Miscellaneous Terminals (continued)

SIGNAL	BALL NO.		I/O TYPE	DESCRIPTION
	ZAY PACKAGE	ZAJ PACKAGE		
SDA	H12	H11	I/O	Serial-bus data. This signal is used as serial bus data when a pullup is detected on SDA or when the SBDETECT bit is set in the serial bus control and status register. Note: In serial-bus mode, an external pullup resistor is required to prevent the SDA signal from floating.
BMODE	A05	B06	I	Beta mode. This terminal determines the PHY-section/LLC-section interface connection protocol. When logic high (asserted), the PHY-section/LLC-section interface complies with the IEEE Std 1394b-2002 Revision 1.33 beta interface. When logic low (deasserted), the PHY-section/LLC-section interface complies with legacy IEEE Std 1394a-2000. This terminal must be pulled high with a 1-kΩ resistor during normal operation.
TESTM	B02	A03	I	Test control. This input is used in the manufacturing test of the XIO2213B. For normal use, this terminal must be pulled high through a 1-kΩ resistor to V_{DD}.
VREG_PD	A06	B07	I	Voltage regulator power-down input. When asserted logic high, this pin will power-down the internal 3.3- to 1.95V regulator. For single 3.3V supply operation, this pin should be tied to GND. When using the internal regulator, the XIO2213B can support a maximum of 2-Beta and 1-DS connection simultaneously. If 3-Beta ports are required to be simultaneously supported, it is recommended to use an external 1.95V regulator.
SE	P13	M10	I	Test control. This input is used in the manufacturing test of the XIO2213B. For normal use, this terminal must be pulled low either through a 1-kΩ resistor to GND or directly to GND.
SM	P14	N10	I	Test control. This input is used in the manufacturing test of the XIO2213B. For normal use, this terminal must be pulled low either through a 1-kΩ resistor to GND or directly to GND.

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3 Feature/Protocol Descriptions

This chapter provides a high-level overview of all significant device features. Figure 3-1 shows a simplified block diagram of the basic architecture of the PCIe to PCI bridge with 1394b OHCI and 3-port PHY. The top of the diagram is the PCIe interface, and the 1394b OHCI with 3-port PHY is located at the bottom of the diagram.

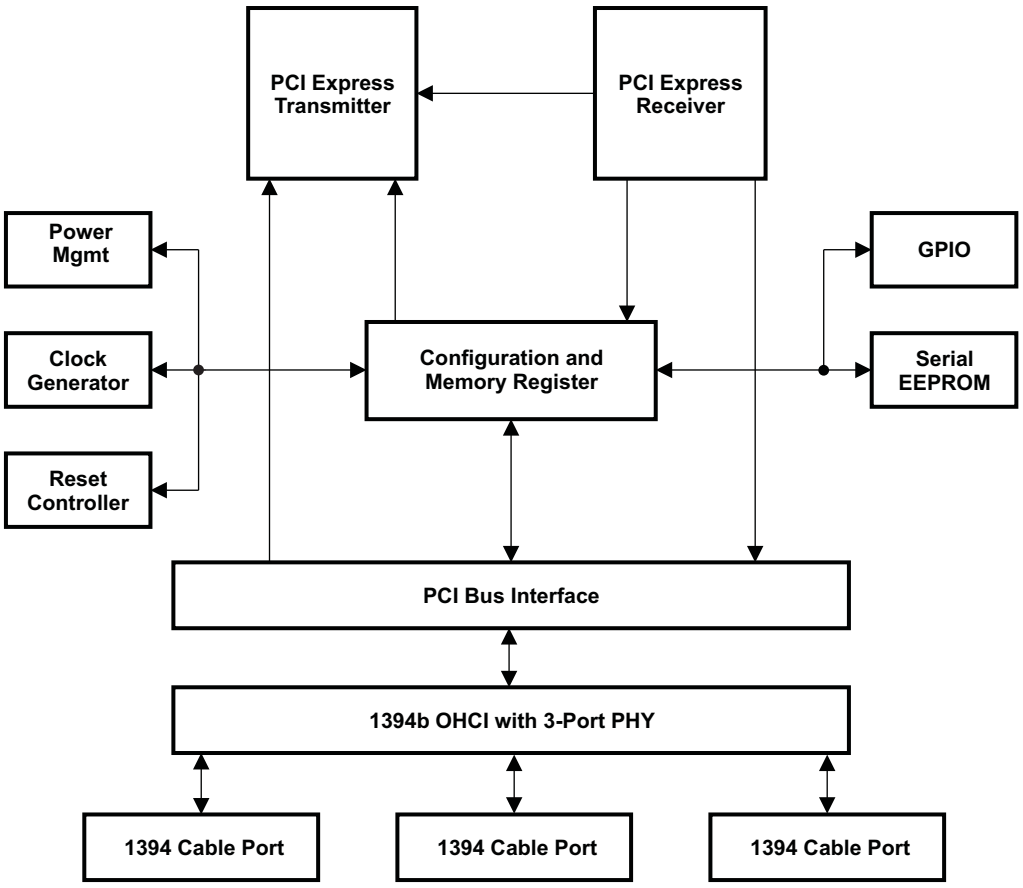


Figure 3-1. XIO2213B Block Diagram

3.1 Power-Up/Power-Down Sequencing

The bridge contains both 1.5-V and 3.3-V power terminals. The following power-up and power-down sequences describe how power is applied to these terminals.

In addition, the bridge has three resets: $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, and an internal power-on reset. These resets are described in Section 3.2. The following power-up and power-down sequences describe how $\overline{\text{PERST}}$ is applied to the bridge.

The application of the PCIe reference clock (REFCLK) is important to the power-up/-down sequence and is included in the following power-up and power-down descriptions.

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3.1.1 Power-Up Sequence

1. Assert $\overline{\text{PERST}}$ to the device.
2. Apply 1.5-V and 3.3-V voltages.
3. Apply a stable PCIe reference clock.
4. To meet PCIe specification requirements, $\overline{\text{PERST}}$ cannot be deasserted until the following two delay requirements are satisfied:
   - Wait a minimum of 100 s after applying a stable PCIe reference clock. The 100-s limit satisfies the requirement for stable device clocks by the deassertion of $\overline{\text{PERST}}$.
   - Wait a minimum of 100 ms after applying power. The 100-ms limit satisfies the requirement for stable power by the deassertion of $\overline{\text{PERST}}$.

See the power-up sequencing diagram in Figure 3-2.

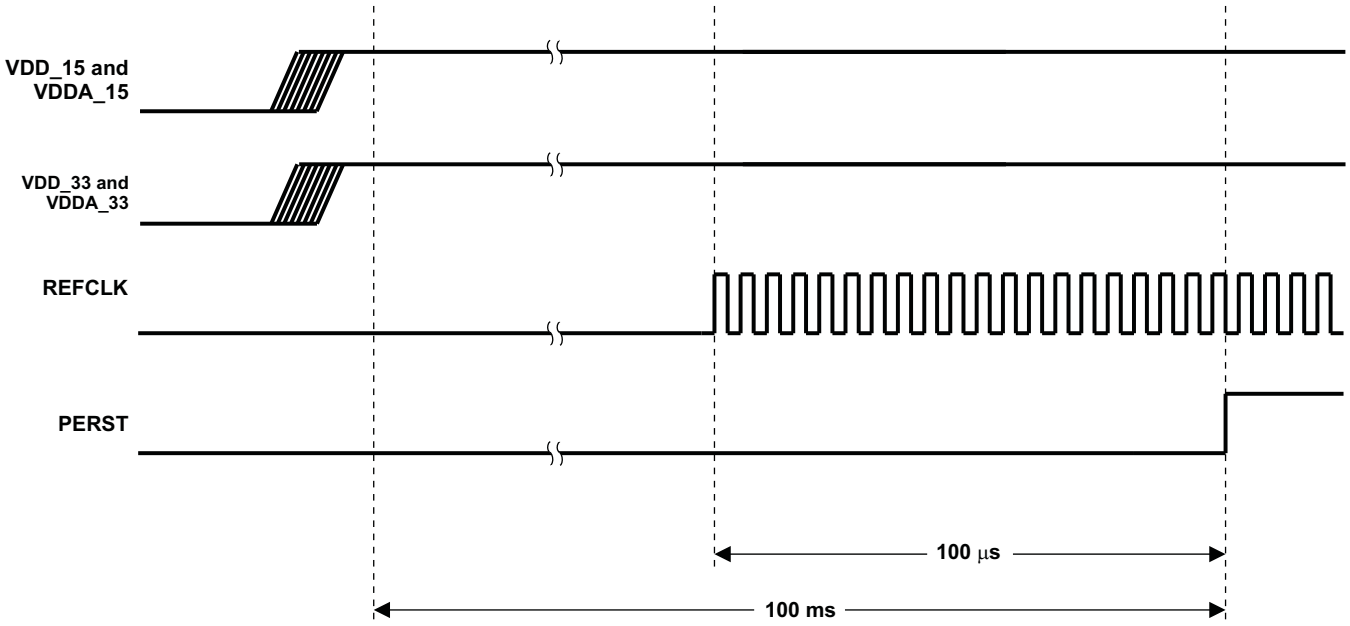


Figure 3-2. Power-Up Sequence

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3.1.2 Power-Down Sequence

1. Assert $\overline{\text{PERST}}$ to the device.
2. Remove the reference clock.
3. Remove 3.3-V and 1.5-V voltages.

See the power-down sequencing diagram in Figure 3-3. If the VDD_33_AUX terminal is to remain powered after a system shutdown, the bridge power-down sequence is the same as shown in Figure 3-3.

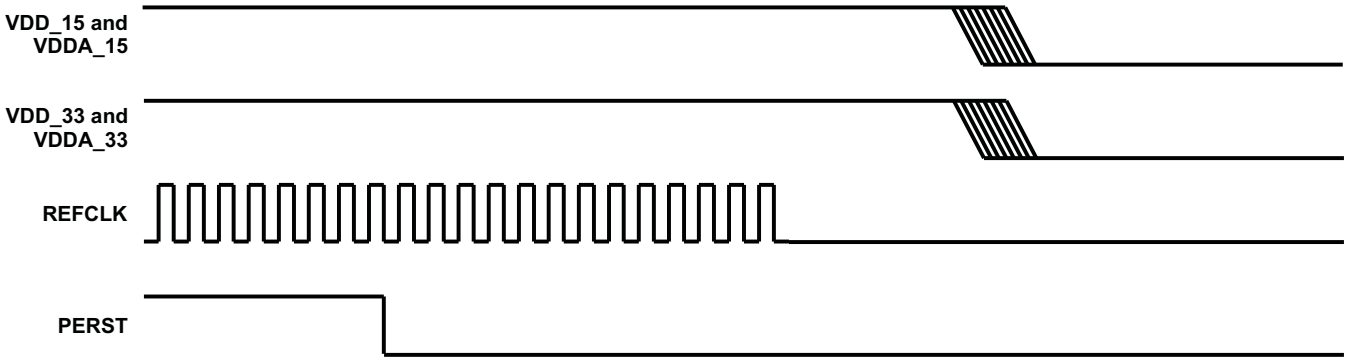


Figure 3-3. Power-Down Sequence

3.2 XIO2213B Reset Features

There are five XIO2213B reset options that include internally-generated power-on reset, resets generated by asserting input terminals, and software-initiated resets that are controlled by sending a PCIe hot reset or setting a configuration register bit. Table 3-1 identifies these reset sources and describes how the XIO2213B responds to each reset.

Table 3-1. XIO2213B Reset Options

RESET OPTION	XIO2213B FEATURE	RESET RESPONSE
XIO2213B internally-generated power-on reset	During a power-on cycle, the XIO2213B asserts an internal reset and monitors the $V_{DD_15_COMB}$ (B11) terminal. When this terminal reaches 90% of the nominal input voltage specification, power is considered stable. After stable power, the XIO2213B monitors the PCIe reference clock (REFCLK) and waits 10 s after active clocks are detected. Then, internal power-on reset is deasserted.	When the internal power-on reset is asserted, all control registers, state machines, sticky register bits, and power management state machines are initialized to their default state. In addition, the XIO2213B asserts the internal PCI bus reset.
PCIe reset input ($\overline{\text{PERST}}$, B12)	This XIO2213B input terminal is used by an upstream PCIe device to generate a PCIe reset and to signal a system power good condition. When $\overline{\text{PERST}}$ is asserted low, the XIO2213B generates an internal PCIe reset as defined in the PCI Express Specification. When $\overline{\text{PERST}}$ transitions from low to high, a system power good condition is assumed by the XIO2213B. Note: The system must assert $\overline{\text{PERST}}$ before power is removed, before REFCLK is removed or before REFCLK becomes unstable.	When $\overline{\text{PERST}}$ is asserted low, all control register bits that are not sticky are reset. Within the configuration register maps, the sticky bits are indicated by the symbol. Also, all state machines that are not associated with sticky functionality are reset. In addition, the XIO2213B asserts the internal PCI bus reset. When the rising edge of $\overline{\text{PERST}}$ occurs, the XIO2213B samples the state of all static control inputs and latches the information internally. If an external serial EEPROM is detected, a download cycle is initiated. Also, the process to configure and initialize the PCIe link is started. The XIO2213B starts link training within 80 ms after $\overline{\text{PERST}}$ is deasserted.
PCIe training control hot reset	The XIO2213B responds to a training control hot reset received on the PCIe interface. After a training control hot reset, the PCIe interface enters the DL_DOWN state.	In the DL_DOWN state, all remaining configuration register bits and state machines are reset. All remaining bits exclude sticky bits and EEPROM loadable bits. All remaining state machines exclude sticky functionality and EEPROM functionality. Within the configuration register maps, the sticky bits are reset by a global reset ($\overline{\text{GRST}}$) or the internally-generated power-on reset and EEPROM loadable bits are rest by a PCIe reset ($\overline{\text{PERST}}$), $\overline{\text{GRST}}$, or internally generated power-on reset. In addition, the XIO2213B asserts the internal PCI bus reset.
PCI bus reset	System software has the ability to assert and deassert the PCI bus reset on the secondary PCI bus interface.	When bit 6 (SRST) in the XIO2213B control register at offset 3Eh (see Section 4.30) is asserted, the XIO2213B asserts the internal PCI bus reset. A 0b in the SRST bit deasserts the PCI bus reset.

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3.3 PCI Express (PCIe) Interface

3.3.1 External Reference Clock

The XIO2213B requires either a differential, 100-MHz common clock reference or a single-ended, 125-MHz clock reference. The selected clock reference must meet all PCI Express Electrical Specification requirements for frequency tolerance, spread-spectrum clocking, and signal electrical characteristics.

If the REFCLK_SEL input is connected to V_{SS}, a differential, 100-MHz common clock reference is expected by the XIO2213B. If the REFCLK_SEL terminal is connected to V_{DD_33}, a single-ended 125-MHz clock reference is expected by the XIO2213B.

When the single-ended, 125-MHz clock reference option is enabled, the single-ended clock signal is connected to the REFCLK+ terminal. The REFCLK terminal is connected to one side of an external capacitor with the other side of the capacitor connected to V_{SS}.

When using a single-ended reference clock, care must be taken to ensure interoperability from a system jitter standpoint. The PCI Express Base Specification does not ensure interoperability when using a differential reference clock commonly used in PC applications along with a single-ended clock in a noncommon clock architecture. System jitter budgets will have to be verified to ensure interoperability (see the *PCI Express Jitter and BER* white paper from PCI-SIG).

3.3.2 Beacon and Wake

Since the 1394b OHCI function in the XIO2213B does not support $\overline{\text{PME}}$ from D3cold, it is not necessary for the PCIe to PCI bridge portion of the design to support beacon generation or $\overline{\text{WAKE}}$ signaling. As a result, the XIO2213B does not implement VAUX power support.

3.3.3 Initial Flow Control Credits

The bridge flow control credits are initialized using the rules defined in the PCI Express Base Specification. Table 3-2 identifies the initial flow control credit advertisement for the bridge.

Table 3-2. Initial Flow Control Credit Advertisements

CREDIT TYPE	INITIAL ADVERTISEMENT
Posted request headers (PH)	8
Posted request data (PD)	128
Nonposted header (NPH)	4
Nonposted data (NPD)	4
Completion header (CPLH)	0 (infinite)
Completion data (CPLD)	0 (infinite)

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3.3.4 PCIe Message Transactions

PCIe messages are both initiated and received by the bridge. Table 3-3 outlines message support within the bridge.

Table 3-3. Messages Supported by Bridge

MESSAGE	SUPPORTED	BRIDGE ACTION
Assert_INTx	Yes	Transmitted upstream
Deassert_INTx	Yes	Transmitted upstream
PM_Active_State_Nak	Yes	Received and processed
PM_PME	Yes	Transmitted upstream
PME_Turn_Off	Yes	Received and processed
PME_TO_Ack	Yes	Transmitted upstream
ERR_COR	Yes	Transmitted upstream
ERR_NONFATAL	Yes	Transmitted upstream
ERR_FATAL	Yes	Transmitted upstream
Set_Slot_Power_Limit	Yes	Received and processed
Unlock	No	Discarded
Hot plug messages	No	Discarded
Advanced switching messages	No	Discarded
Vendor defined type 0	No	Unsupported request
Vendor defined type 1	No	Discarded

All supported message transactions are processed per the PCI Express Base Specification.

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3.4 PCI Interrupt Conversion to PCIe Messages

The bridge converts interrupts from the PCI bus sideband interrupt signals to PCIe interrupt messages. Since the 1394a OHCI only generates $\overline{\text{INTA}}$ interrupts, only PCIe INTA messages are generated by the bridge.

PCIe Assert_INTA messages are generated when the 1394a OHCI signals an $\overline{\text{INTA}}$ interrupt. The requester ID portion of the Assert_INTA message uses the value stored in the primary bus number register (see Section 4.12) as the bus number, 0 as the device number, and 0 as the function number. The tag field for each Assert_INTA message is 00h.

PCIe Deassert_INTA messages are generated when the 1394a OHCI deasserts the $\overline{\text{INTA}}$ interrupt. The requester ID portion of the Deassert_INTA message uses the value stored in the primary bus number register as the bus number, 0 as the device number, and 0 as the function number. The Tag field for each Deassert_INTA message is 00h.

Figure 3-4 and Figure 3-5 show the format for both the assert and deassert INTA messages.

	+0								+1								+2								+3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Byte 0>	R	Fmt		Type					R	TC			Reserved				T D	E P	Attr		R				Length							
		0	1	1	0	1	0	0		0	0	0							0	0					0	0	0	0	0	0	0	0
Byte 4>	Reserved ID																Tag								Code							
																									0	0	1	0	0	0	0	0
Byte 8> Byte 12>	Reserved																															

Figure 3-4. PCIe Assert_INTA Message

	+0								+1								+2								+3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Byte 0>	R	Fmt		Type					R	TC			Reserved				T D	E P	Attr		R				Length							
		0	1	1	0	1	0	0		0	0	0							0	0					0	0	0	0	0	0	0	0
Byte 4>	Reserved ID																Tag								Code							
																									0	0	1	0	0	1	0	0
Byte 8> Byte 12>	Reserved																															

Figure 3-5. PCIe Deassert_INTX Message

3.5 Two-Wire Serial-Bus Interface

The bridge provides a two-wire serial-bus interface to load subsystem identification information and specific register defaults from an external EEPROM. The serial-bus interface signals are SCL and SDA.

3.5.1 Serial-Bus Interface Implementation

To enable the serial-bus interface, a pullup resistor must be implemented on the SDA signal. At the rising edge of $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$, whichever occurs later in time, the SDA terminal is checked for a pullup resistor. If one is detected, bit 3 (SBDETECT) in the serial-bus control and status register (see Section 4.59) is set. Software may disable the serial-bus interface at any time by writing a 0b to the SBDETECT bit. If no external EEPROM is required, the serial-bus interface is permanently disabled by attaching a pulldown resistor to the SDA signal.

The bridge implements a two-terminal serial interface with one clock signal (SCL) and one data signal (SDA). The SCL signal is a unidirectional output from the bridge and the SDA signal is bidirectional. Both are open-drain signals and require pullup resistors. The bridge is a bus master device and drives SCL at approximately 60 kHz during data transfers and places SCL in a high-impedance state (0 frequency) during bus idle states. The serial EEPROM is a bus slave device and must acknowledge a slave address equal to A0h. Figure 3-6 shows an example application implementing the two-wire serial bus.

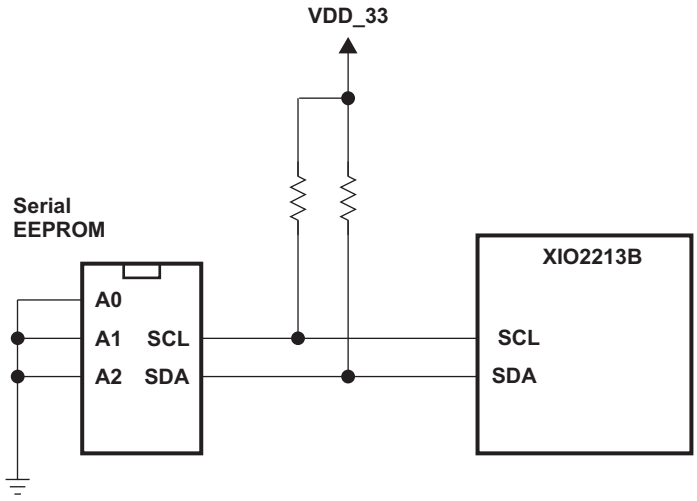


Figure 3-6. Serial EEPROM Application

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3.5.2 Serial-Bus Interface Protocol

All data transfers are initiated by the serial-bus master. The beginning of a data transfer is indicated by a start condition, which is signaled when the SDA line transitions to the low state while SCL is in the high state (see Figure 3-7). The end of a requested data transfer is indicated by a stop condition, which is signaled by a low-to-high transition of SDA while SCL is in the high state (see Figure 3-7). Data on SDA must remain stable during the high state of the SCL signal, as changes on the SDA signal during the high state of SCL are interpreted as control signals, that is, a start or stop condition.

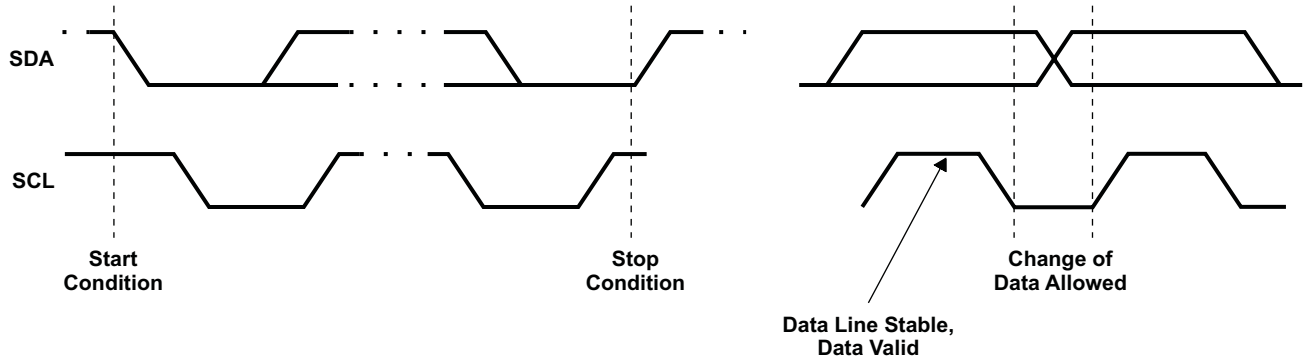


Figure 3-7. Serial-Bus Start/Stop Conditions and Bit Transfers

Data is transferred serially in 8-bit bytes. During a data transfer operation, the exact number of bytes that are transmitted is unlimited. However, each byte must be followed by an acknowledge bit to continue the data transfer operation. An acknowledge (ACK) is indicated by the data byte receiver pulling the SDA signal low, so that it remains low during the high state of the SCL signal. Figure 3-8 shows the acknowledge protocol.

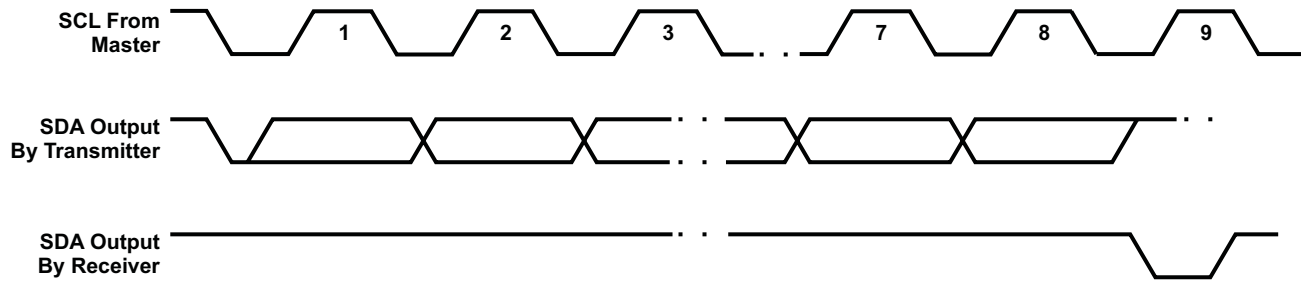


Figure 3-8. Serial-Bus Protocol Acknowledge

The bridge performs three basic serial-bus operations: single-byte reads, single-byte writes, and multibyte reads. The single-byte operations occur under software control. The multibyte read operations are performed by the serial EEPROM initialization circuitry immediately after a PCIe reset (see Section 3.5.3, *Serial-Bus EEPROM Application*, for details on how the bridge automatically loads the subsystem identification and other register defaults from the serial-bus EEPROM.

Figure 3-9 shows a single-byte write. The bridge issues a start condition and sends the 7-bit slave device address, and the R/W command bit is equal to 0b. A 0b in the R/W command bit indicates that the data transfer is a write. The slave device acknowledges if it recognizes the slave address. If no acknowledgment is received by the bridge, bit 1 (SB_ERR) is set in the serial-bus control and status register (PCI offset B3h, see Section 4.59). Next, the EEPROM word address is sent by the bridge, and another slave acknowledgment is expected. Then the bridge delivers the data-byte most significant bit (MSB) first and expects a final acknowledgment before issuing the stop condition.

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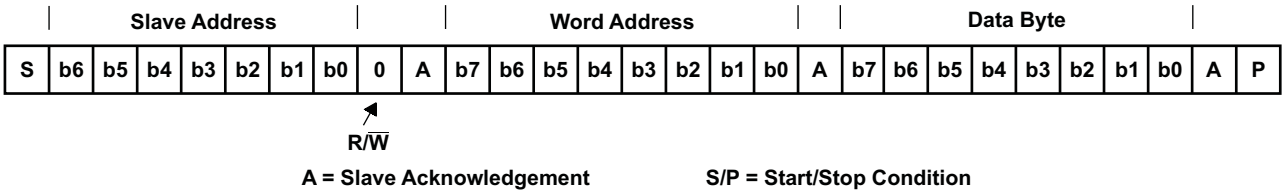


Figure 3-9. Serial-Bus Protocol Byte Write

Figure 3-10 shows a single-byte read. The bridge issues a start condition and sends the 7-bit slave device address, and the R/W command bit is equal to 0b (write). The slave device acknowledges if it recognizes the slave address. Next, the EEPROM word address is sent by the bridge, and another slave acknowledgment is expected. Then, the bridge issues a restart condition followed by the 7-bit slave address, and the R/W command bit is equal to 1b (read). Once again, the slave device responds with an acknowledge. Next, the slave device sends the 8-bit data byte, MSB first. Since this is a 1-byte read, the bridge responds with no acknowledge (logic high) indicating the last data byte. Finally, the bridge issues a stop condition.

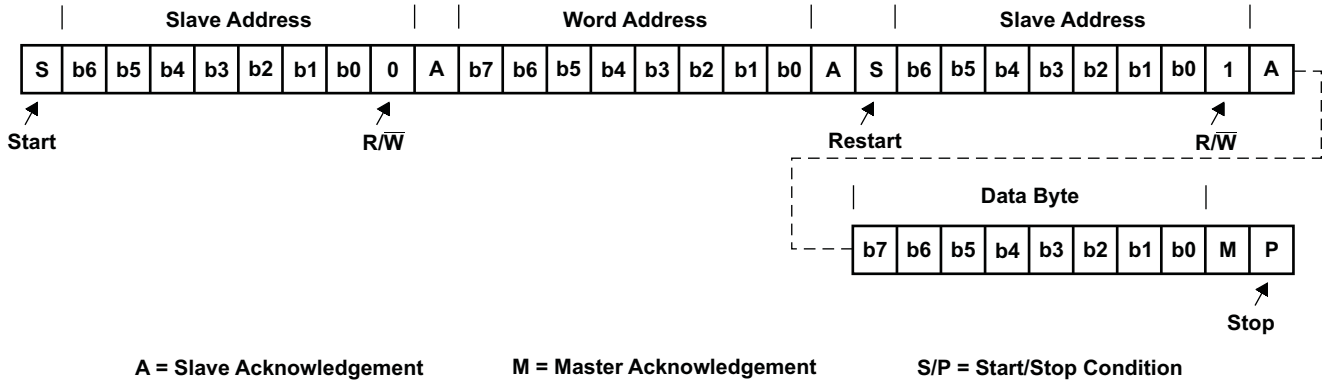


Figure 3-10. Serial-Bus Protocol Byte Read

Figure 3-11 shows the serial interface protocol during a multibyte serial EEPROM download. The serial-bus protocol starts exactly the same as a 1-byte read. The only difference is that multiple data bytes are transferred. The number of transferred data bytes is controlled by the bridge master. After each data byte, the bridge master issues acknowledge (logic low) if more data bytes are requested. The transfer ends after a bridge master no acknowledge (logic high) followed by a stop condition.

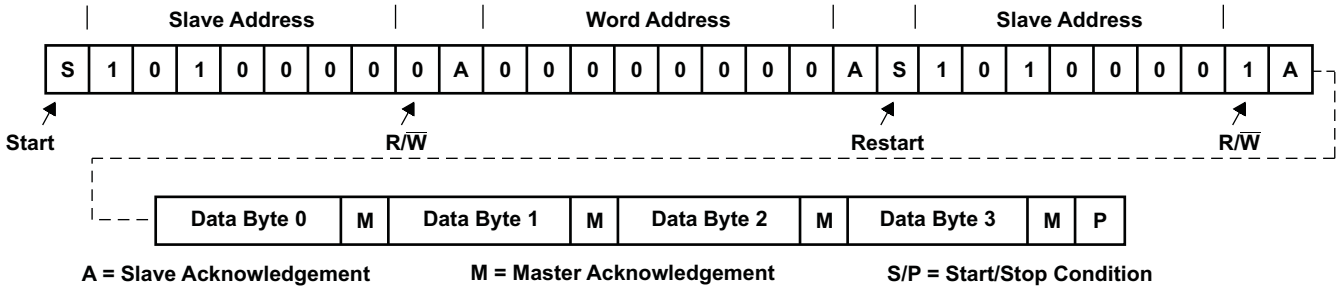


Figure 3-11. Serial-Bus Protocol Multibyte Read

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Bit 7 (PROT_SEL) in the serial-bus control and status register changes the serial-bus protocol. Each of the three previous serial-bus protocol figures show the PROT_SEL bit default (logic low). When this control bit is asserted, the word address and corresponding acknowledge are removed from the serial-bus protocol. This feature allows the system designer a second serial-bus protocol option when selecting external EEPROM devices.

3.5.3 Serial-Bus EEPROM Application

The registers and corresponding bits that are loaded through the EEPROM are provided in Table 3-4.

Table 3-4. EEPROM Register Loading Map

SERIAL EEPROM WORD ADDRESS	BYTE DESCRIPTION	
00h	PCIe to PCI bridge function indicator (00h)	
01h	Number of bytes to download (1Eh)s	
02h	PCI 84h, subsystem vendor ID, byte 0	
03h	PCI 85h, subsystem vendor ID, byte 1	
04h	PCI 86h, subsystem ID, byte 0s	
05h	PCI 87h, subsystem ID, byte 1s	
06h	PCI D4h, general control, byte 0	
07h	PCI D5h, general control, byte 1	
08h	PCI D6h, general control, byte 2	
09h	PCI D7h, general control, byte 3	
0Ah	TI Proprietary register load 00h (PCI D8h)	
0Bh	TI Proprietary register load 00h (PCI D9h)	
0Ch	Reserved — no bits loaded 00h (PCI DAh)	
0Dh	PCI DCh, arbiter control	
0Eh	PCI DDh, arbiter request mask	
0Fh	PCI C0h, TL control and diagnostic register, byte 0	
10h	PCI C0h, TL control and diagnostic register, byte 1	
11h	PCI C0h, TL control and diagnostic register, byte 2	
12h	PCI C0h, TL control and diagnostic register, byte 3	
13h	PCI C4h, DLL control and diagnostic register, byte 0	
14h	PCI C5h, DLL control and diagnostic register, byte 1	
15h	PCI C6h, DLL control and diagnostic register, byte 2	
16h	PCI C7h, DLL control and diagnostic register, byte 3	
17h	PCI C8h, PHY control and diagnostic register, byte 0	
18h	PCI C9h, PHY control and diagnostic register, byte 1	
19h	PCI CAh, PHY control and diagnostic register, byte 2	
1Ah	PCI CBh, PHY control and diagnostic register, byte 3	
1Bh	Reserved — no bits loaded 00h (PCI CEh)	
1Ch	Reserved — no bits loaded 00h (PCI CFh)	
1Dh	TI proprietary register load 00h (PCI E0h)	
1Eh	TI proprietary register load 00h (PCI E2h)	
1Fh	TI proprietary register load 00h (PCI E3h)	
20h	1394 OHCI function indicator (01h)	
21h	Number of bytes (18h)	
22h	PCI 3Fh, maximum latency, bits 7-4	PCI 3Eh, minimum grant, bits 3-0
23h	PCI 2Ch, subsystem vendor ID, byte 0	
24h	PCI 2Dh, subsystem vendor ID, byte 1	
25h	PCI 2Eh, subsystem ID, byte 0	

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Table 3-4. EEPROM Register Loading Map (continued)

SERIAL EEPROM WORD ADDRESS	BYTE DESCRIPTION					
26h	PCI 2Fh, subsystem ID, byte 1					
27h	[7] Link_Enh enab_unfair	[6] HC Control Program Phy Enable	[5:3] RSVD	[2] Link_Enh	[1] Link_Enh enab_accel	[0] RSVD
28h	Mini-ROM address, this byte indicates the MINI ROM offset into the EEPROM 00h = No MINI ROM 01h to FFh = MINI ROM offset					
29h	OHCI 24h, GUIDHi, byte 0					
2Ah	OHCI 25h, GUIDHi, byte 1					
2Bh	OHCI 26h, GUIDHi, byte 2					
2Ch	OHCI 27h, GUIDHi, byte 3					
2Dh	OHCI 28h, GUIDLo, byte 0					
2Eh	OHCI 29h, GUIDLo, byte 1					
2Fh	OHCI 2Ah, GUIDLo, byte 2					
30h	OHCI 2Bh, GUIDLo, byte 3					
31h	Reserved — no bits loaded					
32h	PCI F5h, Link_Enh, byte 1, bits 7, 6, 5, 4					
33h	PCI F0h, PCI miscellaneous, byte 0, bits 7, 4, 2, 1, 0					
34h	PCI F1h, PCI miscellaneous, byte 1, bits 1, 0					
35h	Reserved — no bits loaded					
36h	Reserved — no bits loaded					
37h	Reserved — no bits loaded					
38h	Reserved — no bits loaded					
39h	Reserved multifunction select register					
3Ah	End-of-list indicator (80h)					

This format must be explicitly followed for the bridge to correctly load initialization values from a serial EEPROM. All byte locations must be considered when programming the EEPROM.

The serial EEPROM is addressed by the bridge at slave address 1010 000b. This slave address is internally hardwired and cannot be changed by the system designer. Therefore, all three hardware address bits for the EEPROM are tied to V_{SS} to achieve this address. The serial EEPROM in the sample application circuit (Figure 3-6) assumes the 1010b high-address nibble. The lower three address bits are terminal inputs to the chip, and the sample application shows these terminal inputs tied to V_{SS}.

During an EEPROM download operation, bit 4 (ROMBUSY) in the serial-bus control and status register is asserted. After the download is finished, bit 0 (ROM_ERR) in the serial-bus control and status register may be monitored to verify a successful download.

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3.5.4 Accessing Serial-Bus Devices Through Softwaree

The bridge provides a programming mechanism to control serial-bus devices through system software. The programming is accomplished through a doubleword of PCI configuration space at offset B0h. Table 3-5 lists the registers that program a serial-bus device through software.

Table 3-5. Registers Used To Program Serial-Bus Devices

PCI OFFSET	REGISTER NAME	DESCRIPTION
B0h	Serial-bus data (see Section 4.56)	Contains the data byte to send on write commands or the received data byte on read commands.
B1h	Serial-bus word address (see Section 4.57)	The content of this register is sent as the word address on byte writes or reads. This register is not used in the quick command protocol. Bit 7 (PROT_SEL) in the serial-bus control and status register (offset B3h, see Section 4.59) is set to 1b to enable the slave address to be sent.
B2h	Serial-bus slave address (see Section 4.58)	Write transactions to this register initiate a serial-bus transaction. The slave device address and the R/$\overline{W}$ command selector are programmed through this register.
B3h	Serial-bus control and status (see Section 4.59)	Serial interface enable, busy, and error status are communicated through this register. In addition, the protocol-select bit (PROT_SEL) and serial-bus test bit (SBTEST) are programmed through this register.

To access the serial EEPROM through the software interface, the following steps are performed:

1. The control and status byte is read to verify the EEPROM interface is enabled (SBDETECT asserted) and not busy (REQBUSY and ROMBUSY deasserted).
2. The serial-bus word address is loaded. If the access is a write, the data byte is also loaded.
3. The serial-bus slave address and R/$\overline{W}$ command selector byte is written.
4. REQBUSY is monitored until this bit is deasserted.
5. SB_ERR is checked to verify that the serial-bus operation completed without error. If the operation is a read, the serial-bus data byte is now valid.

3.6 Advanced Error Reporting Registers

In the extended PCIe configuration space, the bridge supports the advanced error reporting capabilities structure. For the PCIe interface, both correctable and uncorrectable error statuses are provided. For the PCI bus interface, secondary uncorrectable error status is provided. All uncorrectable status bits have corresponding mask and severity control bits. For correctable status bits, only mask bits are provided.

Both the primary and secondary interfaces include first error pointer and header log registers. When the first error is detected, the corresponding bit position within the uncorrectable status register is loaded into the first error pointer register. Likewise, the header information associated with the first failing transaction is loaded into the header log. To reset this first error control logic, the corresponding status bit in the uncorrectable status register is cleared by a writeback of 1b.

For systems that require high data reliability, ECRC is fully supported on the PCIe interface. The primary-side advanced error capabilities and control register has both ECRC generation and checking enable control bits. When the checking bit is asserted, all received TLPs are checked for a valid ECRC field. If the generation bit is asserted, all transmitted TLPs contain a valid ECRC field.

3.7 Data Error Forwarding Capability

The bridge supports the transfer of data errors in both directions.

If a downstream PCIe transaction with a data payload is received that targets the internal PCI bus and the EP bit is set indicating poisoned data, the bridge must ensure that this information is transferred to the PCI bus. To do this, the bridge forces a parity error on each PCI bus data phase by inverting the parity bit calculated for each double word of data.

If the bridge is the target of a PCI transaction that is forwarded to the PCIe interface and a data parity error is detected, this information is passed to the PCIe interface. To do this, the bridge sets the EP bit in the upstream PCIe header.

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3.8 General-Purpose I/O (GPIO) Interface

Up to eight GPIO terminals are provided for system customization. These GPIO terminals are 3.3-V tolerant.

The exact number of GPIO terminals varies based on implementing the clock-run, power-override, and serial EEPROM interface features. These features share four of the eight GPIO terminals. When any of the three shared functions are enabled, the associated GPIO terminal is disabled.

All eight GPIO terminals are individually configurable as either inputs or outputs by writing the corresponding bit in the GPIO control register at offset B4h. A GPIO data register at offset B6h exists to either read the logic state of each GPIO input or to set the logic state of each GPIO output. The power-up default state for the GPIO control register is input mode.

3.9 Set Slot Power Limit Functionality

The PCI Express Specification provides a method for devices to limit internal functionality and save power based on the value programmed into the captured slot power limit scale (CSPLS) and capture slot power limit value (CSPLV) fields of the PCIe device capabilities register at offset 94h (see Section 4.50, Device Capabilities Register, for details). The bridge writes these fields when a set slot power limit message is received on the PCIe interface.

After the deassertion of $\overline{\text{PERST}}$, the XIO2213B compares the information within the CSPLS and CSPLV fields of the device capabilities register to the minimum power scale (MIN_POWER_SCALE) and minimum power value (MIN_POWER_VALUE) fields in the general control register at offset D4h (see Section 4.66, General Control Register, for details). If the CSPLS and CSPLV fields are less than the MIN_POWER_SCALE and MIN_POWER_VALUE fields, respectively, the bridge takes the appropriate action that is defined below.

The power usage action is programmable within the bridge. The general control register includes a 3-bit POWER_OVRD field. This field is programmable to the following two options:

- Ignore slot power limit fields.
- Respond with unsupported request to all transactions except type 0/1 configuration transactions, and set slot power limit messages.

3.10 PCIe and PCI Bus Power Management

The bridge supports both software-directed power management and active-state power management through standard PCI configuration space. Software-directed registers are located in the power management capabilities structure located at offset 50h. Active-state power management control registers are located in the PCIe capabilities structure located at offset 90h.

During software-directed power-management state changes, the bridge initiates link state transitions to L1 or L2/L3 after a configuration write transaction places the device in a low-power state. The power-management state machine is also responsible for gating internal clocks based on the power state. Table 3-6 identifies the relationship between the D-states and bridge clock operation.

Table 3-6. Clocking In Low Power States

CLOCK SOURCE	D0/L0	D1/L1	D2/L1	D3/L2/L3
PCIe reference clock input (REFCLK)	On	On	On	On/Off
Internal PCI bus clock to bridge function	On	Off	Off	Off
Internal PCI bus clock to 1394b OHCI function	On	On	On	On/Off

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The link power management (LPM) state machine manages active-state power by monitoring the PCIe transaction activity. If no transactions are pending and the transmitter has been idle for at least the minimum time required by the PCI Express Specification, the LPM state machine transitions the link to either the L0s or L1 state. By reading the bridges L0s and L1 exit latency in the link capabilities register, the system software may make an informed decision relating to system performance versus power savings. The ASLPMC field in the link control register provides an L0s-only option, L1-only option, or both L0s and L1 options.

Finally, the bridge generates the PM_Active_State_Nak Message if a PM_Active_State_Request_L1 DLLP is received on the PCIe interface and the link cannot be transitioned to L1.

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3.11 1394b OHCI Controller Functionality

3.11.1 1394b OHCI Power Management

The 1394b OHCI controller complies with the PCI Bus Power Management Interface Specification. The controller supports the D0 (uninitialized), D0 (active), D1, D2, and D3 power states as defined by the power-management definition in the 1394 Open Host Controller Interface Specification, Appendix A4.

Table 3-7 identifies the supported power-management registers within the 1394 OHCI configuration register map.

Table 3-7. 1394b OHCI Configuration Register Map

REGISTER NAME				OFFSET
Power management capabilities		Next item pointer	Capability ID	44h
PM data	Power management control/status register bridge support extensions	Power management control/status (CSR)		48h

3.11.2 1394b OHCI and V_{AUX}

The 1394b OHCI function within the XIO2213B is powered by V_{DD_MAIN} only. Therefore, during the $D3_{cold}$ power-management state, V_{AUX} is not supplied to the 1394b OHCI function.

This implies that the 1394b OHCI function does not implement sticky bits must be initialized after a $D3_{cold}$ power-management state. An external serial EEPROM interface is available to initialize critical configuration register bits. The EEPROM download is triggered by the deassertion of the $\overline{\text{PERST}}$ input. Otherwise, the BIOS must initialize the 1394b OHCI function.

3.11.3 1394b OHCI and Reset Options

The 1394b OHCI function is completely reset by the internal power-on reset feature, $\overline{\text{GRST}}$ input, or $\overline{\text{PERST}}$ input. This includes all EEPROM loadable bits, power-management functions, and all remaining configuration register bits and logic.

A PCIe training control hot reset or the PCI bus configuration register reset bit (SRST) excludes the EEPROM loadable bits, power-management functions, and 1394 PHY. All remaining configuration registers and logic are reset.

If the OHCI controller is in the power-management D2 or D3 state, or if the OHCI configuration register reset bit (SoftReset) is set, the OHCI controller DMA logic and link logic is reset.

Finally, if the OHCI configuration register PHY reset bit (ISBR) is set, the 1394 PHY logic is reset.

3.11.4 1394b OHCI PCI Bus Master

As a bus master, the 1394 OHCI function supports the memory commands specified in Table 3-8. The commands include memory read, memory read line, memory read multiple, memory write, and memory write and invalidate.

The read command usage for read transactions of greater than two data phases are determined by the selection in bits 9:8 (MR_ENHANCE field) of the PCI miscellaneous configuration register at offset F0h (see Section 7.21). For read transactions of one or two data phases, a memory read command is used.

The write command usage is determined by the MWI_ENB bit 4 of the command configuration register at offset 04h (see Section 4.3). If bit 4 is asserted and a memory write starts on a cache boundary with a length greater than one cache line, memory write and invalidate commands are used. Otherwise, memory write commands are used.

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Table 3-8. 1394 OHCI Memory Command Options

PCI	COMMAND C/BE3C/BE0	OHCI MASTER FUNCTION
Memory read	0110	DMA read from memory
Memory write	0111	DMA write to memory
Memory read multiple	1100	DMA read from memory
Memory read line	1110	DMA read from memory
Memory write and invalidate	1111	DMA write to memory

3.11.5 1394b OHCI Subsystem Identification

The subsystem identification register at offset 2Ch is used for system and option card identification purposes. This register can be initialized from the serial EEPROM or programmed via the subsystem access register at offset F8h in the 1394a OHCI PCI configuration space (see Section 7.23).

Write access to the subsystem access register updates the subsystem identification registers identically to OHCI-Lynx™ integrated circuits. The contents of the subsystem access register are aliased to the subsystem vendor ID and subsystem ID registers at PCI offsets 2Ch and 2Eh, respectively. The subsystem ID value written to this register may also be read back from this register.

3.11.6 1394b OHCI PME Support

Since the 1394b OHCI controller is not connected to VAUX, PME generation is disabled for D3cold power-management states.

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4 Classic PCI Configuration Space

The programming model of the XIO2213B PCIe to PCI bridge is compliant to the classic PCI-to-PCI bridge programming model. The PCI configuration map uses the type 1 PCI bridge header.

Sticky bits are reset by a global reset ($\overline{\text{GRST}}$) or the internally-generated power-on reset. EEPROM loadable bits are reset by a PCIe reset ($\overline{\text{PERST}}$), $\overline{\text{GRST}}$, or the internally-generated power-on reset. The remaining register bits are reset by a PCIe hot reset, $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 4-1. Classic PCI Configuration Register Map

REGISTER NAME				OFFSET
Device ID		Vendor ID		000h
Status		Command		004h
Class code			Revision ID	008h
BIST	Header type	Primary latency timer	Cache line size	00Ch
Device contol base address				010h
Scratchpad RAM base address				014h
Secondary latency timer	Subordinate bus number	Secondary bus number	Primary bus number	018h
Secondary status		I/O limit	I/O base	01Ch
Memory limit		Memory base		020h
Prefetchable memory limit		Prefetchable memory base		024h
Prefetchable base upper 32 bits				028h
Prefetchable limit upper 32 bits				02Ch
I/O limit upper 16 bits		I/O base upper 16 bits		030h
Reserved			Capabilities pointer	034h
Reserved				038h
Bridge control		Interrupt pin	Interrupt line	03Ch
Reserved				040h-04Ch
Power management capabilities		Next item pointer	PM apability ID	050h
Power management data	Power management bridge support extention	Power management control/status		054h
Reserved				058h-05Ch
MSI message control		Next item pointer	MSI capability ID	060h
MSI message lower address				064h
MSI message upper address				068h
Reserved		MSI message data		06Ch
Reserved				070h-07Ch
Reserved		Next item pointer	SSID/SSVID capability ID	080h
Subsystem ID(1)		Subsystem vendor ID(1)		084h
Reserved				088h-08Ch
PCI Express capabilities register		Next item pointer	PCI Express capability ID	090h
Device capabilities				094h
Device status		Device control		098h
Link capabilities				09Ch
Link status		Link control		0A0h
Reserved				0A4h-0ACh
Serial-bus control and status(1)	Serial-bus slave address(1)	Serial-bus word address(1)	Serial-bus data(1)	0B0h
GPIO data(1)		GPIO control(1)		0B4h

(1) One or more bits in this register are reset by $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

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Table 4-1. Classic PCI Configuration Register Map (continued)

REGISTER NAME				OFFSET
Reserved				0B8h-0BCh
Control and diagnostic register 0(1)				0C0h
Control and diagnostic register 1(1)				0C4h
Control and diagnostic register 2(1)				0C8h
Reserved				0CCh
Subsystem access(1)				0D0h
General control(1)				0D4h
Reserved	TI proprietary(1)	TI proprietary(1)	TI proprietary(1)	0D8h
Reserved	Arbiter time-out status	Arbiter request mask(1)	Arbiter control(1)	0DCh
TI proprietary(1)		Reserved	TI proprietary(1)	0E0h
Reserved		TI proprietary		0E4h
Reserved				0E8h-0FCh

4.1 Vendor ID Register

This 16-bit read-only register contains the value 104Ch, which is the vendor ID assigned to TI.,

PCI register offset: 00h
Register type: Read-only
Default value: 104Ch

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0

4.2 Device ID Register

This 16-bit read-only register contains the value 823Eh, which is the device ID assigned by TI for the bridge.,

PCI register offset: 02h
Register type: Read only
Default value: 823Eh

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	1	0	0	0	1	1	0	0	0	1

4.3 Command Register

The command register controls how the bridge behaves on the PCIe interface. See Table 4-2 for a complete description of the register contents.

PCI register offset: 04h
Register type: Read only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-2. Command Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:11	RSVD	R	Reserved. Returns 00000b when read.
10	INT_DISABLE	R	$\overline{\text{INTx}}$ disable. This bit enables device specific interrupts. Since the bridge does not generate any internal interrupts, this bit is read-only 0b.
9	FBB_ENB	R	Fast back-to-back enable. The bridge does not generate fast back-to-back transactions; therefore, this bit returns 0b when read.
8	SERR_ENB	RW	$\overline{\text{SERR}}$ enable. When this bit is set, the bridge can signal fatal and nonfatal errors on the PCIe interface on behalf of SERR assertions detected on the PCI bus. 0 = Disable the reporting of nonfatal errors and fatal errors (default) 1 = Enable the reporting of nonfatal errors and fatal errors
7	STEP_ENB	R	Address/data stepping control. The bridge does not support address/data stepping, and this bit is hardwired to 0b.
6	PERR_ENB	RW	Controls the setting of bit 8 (DATAPAR) in the status register (offset 06h, see Section 4.4) in response to a received poisoned TLP from PCIe. A received poisoned TLP is forwarded with bad parity to conventional PCI, regardless of the setting of this bit. 0 = Disables the setting of the master data parity error bit (default) 1 = Enables the setting of the master data parity error bit
5	VGA_ENB	R	VGA palette snoop enable. The bridge does not support VGA palette snooping; therefore, this bit returns 0b when read.
4	MWI_ENB	RW	Memory write and invalidate enable. When this bit is set, the bridge translates PCIe memory write requests into memory write and invalidate transactions on the PCI interface. 0 = Disable the promotion to memory write and invalidate (default) 1 = Enable the promotion to memory write and invalidate
3	SPECIAL	R	Special cycle enable. The bridge does not respond to special cycle transactions; therefore, this bit returns 0b when read.
2	MASTER_ENB	RW	Bus master enable. When this bit is set, the bridge is enabled to initiate transactions on the PCIe interface. 0 = PCIe interface cannot initiate transactions. The bridge must disable the response to memory and I/O transactions on the PCI interface (default). 1 = PCIe interface can initiate transactions. The bridge can forward memory and I/O transactions from PCI secondary interface to the PCIe interface.
1	MEMORY_ENB	RW	Memory space enable. Setting this bit enables the bridge to respond to memory transactions on the PCIe interface. 0 = PCIe receiver cannot process downstream memory transactions and must respond with an unsupported request (default) 1 = PCIe receiver can process downstream memory transactions. The bridge can forward memory transactions to the PCI interface.
0	IO_ENB	RW	I/O space enable. Setting this bit enables the bridge to respond to I/O transactions on the PCIe interface. 0 = PCIe receiver cannot process downstream I/O transactions and must respond with an unsupported request (default) 1 = PCIe receiver can process downstream I/O transactions. The bridge can forward I/O transactions to the PCI interface.

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4.4 Status Register

The status register provides information about the PCIe interface to the system. See Table 4-3 for a complete description of the register contents.

PCI register offset: 06h

Register type: Read only, Read/Clear

Default value: 0010h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Table 4-3. Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PAR_ERR	RCU	Detected parity error. This bit is set when the PCIe interface receives a poisoned TLP. This bit is set regardless of the state of bit 6 (PERR_ENB) in the command register (offset 04h, see Section 4.3). 0 = No parity error detected 1 = Parity error detected
14	SYS_ERR	RCU	Signaled system error. This bit is set when the bridge sends an ERR_FATAL or ERR_NONFATAL message and bit 8 (SERR_ENB) in the command register (offset 04h, see Section 4.3) is set. 0 = No error signaled 1 = ERR_FATAL or ERR_NONFATAL signaled
13	MABORT	RCU	Received master abort. This bit is set when the PCIe interface of the bridge receives a completion-with-unsupported-request status. 0 = Unsupported request not received on the PCIe interface 1 = Unsupported request received on the PCIe interface
12	TABORT_REC	RCUT	Received target abort. This bit is set when the PCIe interface of the bridge receives a completion-with-completer-abort status. 0 = Completer abort not received on the PCIe interface 1 = Completer abort received on the PCIe interface
11	TABORT_SIG	RCUT	Signaled target abort. This bit is set when the PCIe interface completes a request with completer abort status. 0 = Completer abort not signaled on the PCIe interface 1 = Completer abort signaled on the PCIe interface
10:9	PCI_SPEED	R	DEVSEL timing. These bits are read-only 00b, because they do not apply to PCIe.
8	DATAPAR	RCU	Master data parity error. This bit is set if bit 6 (PERR_ENB) in the command register (offset 04h, see Section 4.3) is set and the bridge receives a completion with data marked as poisoned on the PCIe interface or poisons a write request received on the PCIe interface. 0 = No uncorrectable data error detected on the primary interface 1 = Uncorrectable data error detected on the primary interface
7	FBB_CAP	R	Fast back-to-back capable. This bit does not have a meaningful context for a PCIe device and is hardwired to 0b.
6	RSVD	R	Reserved. Returns 0b when read.
5	66MHZ	R	66-MHz capable. This bit does not have a meaningful context for a PCIe device and is hardwired to 0b.
4	CAPLIST	R	Capabilities list. This bit returns 1b when read, indicating that the bridge supports additional PCI capabilities.
3	INT_STATUS	R	Interrupt status. This bit reflects the interrupt status of the function. This bit is read-only 0b since the bridge does not generate any interrupts internally.
2:0	RSVD	R	Reserved. Returns 000b when read.

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4.5 Class Code and Revision ID Register

This read-only register categorizes the base class, subclass, and programming interface of the bridge. The base class is 06h, identifying the device as a bridge. The subclass is 04h, identifying the function as a PCI to PCI bridge, and the programming interface is 00h. Furthermore, the TI device revision is indicated in the lower byte (00h). See Table 4-4 for a complete description of the register contents.

PCI register offset: 08h

Register type: Read only

Default value: 0604 0001h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4-4. Class Code and Revision ID Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	BASECLASS	R	Base class. This field returns 06h when read, which classifies the function as a bridge device.
23:16	SUBCLASS	R	Subclass. This field returns 04h when read, which classifies the function as a PCI to PCI bridge.
15:8	PGMIF	R	Programming interface. This field returns 00h when read.
7:0	CHIPREV	R	Silicon revision. This field returns the silicon revision of the function.

4.6 Cache Line Size Register

If the EN_CACHE_LINE_CHECK bit in the TL control and diagnostic register is 0, Cheetah- Express shall use side-band signals from the 1394b OHCI core to determine how much data to fetch when handling delayed read transactions. In this case, the cache line size register will have no effect on the design and will essentially be a read/write scratchpad register. If the EN_CACHE_LINE_CHECK bit is 1, the cache line size register is used by the bridge to determine how much data to prefetch when handling delayed read transactions. In this case, the value in this register must be programmed to a power of 2, and any value greater than 32 DWORDs will be treated as 32 DWORDs.

PCI register offset: 0Ch

Register type: Read/Write

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.7 Primary Latency Timer Register

This read-only register has no meaningful context for a PCIe device and returns 00h when read.

PCI register offset: 0Dh

Register type: Read only

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

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4.8 Header Type Register

This read-only register indicates that this function has a type 1 PCI header. Bit 7 of this register is 0b, indicating that the bridge is a single-function device.

PCI register offset: 0Eh
Register type: Read only
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

4.9 BIST Register

Since the bridge does not support a built-in self test (BIST), this read-only register returns the value of 00h when read.

PCI register offset: 0Fh
Register type: Read only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.10 Device Control Base Address Register

This read/write register programs the memory base address that accesses the device control registers. See Table 4-5 for a complete description of the register contents.

PCI register offset: 10h
Register type: Read only, Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-5. Device Control Base Address Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:12	ADDRESS	R or RW	Memory address. The memory address field for XIO2213B uses 20 read/write bits indicating that 4096 bytes of memory space are required. While less than this is actually used, typical systems will allocate this space on a 4K boundary. If the BAR0_EN bit (bit 5 at C8h) is 0, these bits are read only and return zeros when read. If the BAR0_EN bit is 1, these bits are read/write.
11:4	RSVD	R	Reserved. These bits are read only and return 00h when read.
3	PRE_FETCH	R	Prefetchable. This bit is read-only 0b indicating that this memory window is not prefetchable.
2:1	MEM_TYPE	R	Memory type. This field is read-only 00b indicating that this window can be located anywhere in the 32-bit address space.
0	MEM_IND	R	Memory space indicator. This field returns 0b indicating that memory space is used.

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4.11 Scratchpad RAM Base Address

This register is used to program the memory address used to access the embedded scratchpad RAM.

PCI register offset: 14h

Register type: Read only, Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-6. Device Control Base Address Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:12	ADDRESS	R or RW	Memory address. The memory address field for XIO2213B uses 20 read/write bits indicating that 4096 bytes of memory space are required. If the BAR1_EN bit (bit 6 at C8h) is 0, these bits are read only and return zeros when read. If the BAR1_EN bit is 1, these bits are read/write.
11:4	RSVD	R	Reserved. These bits are read only and return 00h when read.
3	PRE_FETCH	R	Prefetchable. This bit is read-only 0b indicating that this memory window is not prefetchable.
2:1	MEM_TYPE	R	Memory type. This field is read-only 00b indicating that this window can be located anywhere in the 32-bit address space.
0	MEM_IND	R	Memory space indicator. This field returns 0b indicating that memory space is used.

4.12 Primary Bus Number Register

This read/write register specifies the bus number of the PCI bus segment that the PCIe interface is connected to.

PCI register offset: 18h

Register type: Read/Write

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.13 Secondary Bus Number Register

This read/write register specifies the bus number of the PCI bus segment that the PCI interface is connected to. The bridge uses this register to determine how to respond to a type 1 configuration transaction.

PCI register offset: 19h

Register type: Read/Write

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

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4.14 Subordinate Bus Number Register

This read/write register specifies the bus number of the highest-number PCI bus segment that is downstream of the bridge. Since the PCI bus is internal and only connects to the 1394a OHCI, this register must always be equal to the secondary bus number register (offset 19h, see Section 4.13). The bridge uses this register to determine how to respond to a type 1 configuration transaction.

PCI register offset: 1Ah
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.15 Secondary Latency Timer Register

This read/write register specifies the secondary bus latency timer for the bridge, in units of PCI clock cycles.

PCI register offset: 1Bh
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.16 I/O Base Register

This read/write register specifies the lower limit of the I/O addresses that the bridge forwards downstream. See Table 4-7 for a complete description of the register contents.

PCI register offset: 1Ch
Register type: Read only, Read/Write
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

Table 4-7. I/O Base Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
		7:4	IOBASE
3:0	IOTYPE	R	I/O type. This field is read-only 1h indicating that the bridge supports 32-bit I/O addressing.

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4.17 I/O Limit Register

This read/write register specifies the upper limit of the I/O addresses that the bridge forwards downstream. See Table 4-8 for a complete description of the register contents.

PCI register offset: 1Dh

Register type: Read only, Read/Write

Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

Table 4-8. I/O Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	IOLIMIT	RW	I/O limit. Defines the top address of the I/O address range that determines when to forward I/O transactions from one interface to the other. These bits correspond to address bits [15:12] in the I/O address. The lower 12 bits are assumed to be FFFh. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O limit upper 16 bits register (offset 32h, see Section 4.26).
3:0	IOTYPE	R	I/O type. This field is read-only 1h indicating that the bridge supports 32-bit I/O addressing.

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4.18 Secondary Status Register

The secondary status register provides information about the PCI bus interface. See Table 4-9 for a complete description of the register contents.

PCI register offset: 1Eh

Register type: Read only, Read/Clear

Default value: 02X0h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	1	0	x	0	0	0	0	0	0	0

Table 4-9. Secondary Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PAR_ERR	RCU	Detected parity error. This bit reports the detection of an uncorrectable address, attribute, or data error by the bridge on its internal PCI bus secondary interface. This bit must be set when any of the following three conditions are true: The bridge detects an uncorrectable address or attribute error as a potential target. The bridge detects an uncorrectable data error when it is the target of a write transaction. The bridge detects an uncorrectable data error when it is the master of a read transaction (immediate read data). The bit is set irrespective of the state of bit 0 (PERR_EN) in the bridge control register at offset 3Eh (see Section 4.30). 0 = Uncorrectable address, attribute, or data error not detected on secondary interface 1 = Uncorrectable address, attribute, or data error detected on secondary interface
14	SYS_ERR	RCU	Received system error. This bit is set when the bridge detects an $\overline{\text{SERR}}$ assertion. 0 = No error asserted on the PCI interface 1 = SERR asserted on the PCI interface
13	MABORT	RCU	Received master abort. This bit is set when the PCI interface of the bridge reports the detection of a master abort termination by the bridge when it is the master of a transaction on its secondary interface. 0 = Master abort not received on the PCI interface 1 = Master abort received on the PCI interface
12	TABORT_REC	RCU	Received target abort. This bit is set when the PCI interface of the bridge receives a target abort. 0 = Target abort not received on the PCI interface 1 = Target abort received on the PCI interface
11	TABORT_SIG	RCU	Signaled target abort. This bit reports the signaling of a target abort termination by the bridge when it responds as the target of a transaction on its secondary interface. 0 = Target abort not signaled on the PCI interface 1 = Target abort signaled on the PCI interface
10:9	PCI_SPEED	R	DEVSEL timing. These bits are 01b indicating that this is a medium-speed decoding device.
8	DATAPAR	RCU	Master data parity error. This bit is set if the bridge is the bus master of the transaction on the PCI bus, bit 0 (PERR_EN) in the bridge control register (offset 3Eh see Section 4.30) is set, and the bridge either asserts $\overline{\text{PERR}}$ on a read transaction or detects $\overline{\text{PERR}}$ asserted on a write transaction. 0 = No data parity error detected on the PCI interface 1 = Data parity error detected on the PCI interface
7	FBB_CAP	R	Fast back-to-back capable. This bit returns a 1b when read indicating that the secondary PCI interface of bridge supports fast back-to-back transactions.
6	RSVD	R	Reserved. Returns 0b when read.
5	66MHZ	R	66-MHz capable. The bridge operates at a PCI bus CLK frequency of 66 MHz; therefore, this bit always returns a 1b.
4:0	RSVD	R	Reserved. Returns 00000b when read.

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4.19 Memory Base Register

This read/write register specifies the lower limit of the memory addresses that the bridge forwards downstream. See Table 4-10 for a complete description of the register contents.

PCI register offset: 20h

Register type: Read only, Read/Write

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-10. Memory Base Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MEMBASE	RW	Memory base. Defines the lowest address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h.
3:0	RSVD	R	Reserved. Returns 0h when read.

4.20 Memory Limit Register

This read/write register specifies the upper limit of the memory addresses that the bridge forwards downstream. See Table 4-11 for a complete description of the register contents.

PCI register offset: 22h

Register type: Read only, Read/Write

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-11. Memory Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MEMLIMIT	RW	Memory limit. Defines the highest address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh.
3:0	RSVD	R	Reserved. Returns 0h when read.

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4.21 Prefetchable Memory Base Register

This read/write register specifies the lower limit of the prefetchable memory addresses that the bridge forwards downstream. See Table 4-12 for a complete description of the register contents.

PCI register offset: 24h
Register type: Read only, Read/Write
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4-12. Prefetchable Memory Base Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	PREBASE	RW	Prefetchable memory base. Defines the lowest address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h. The prefetchable base upper 32 bits register (offset 28h, see Section 4.23) specifies the bit [63:32] of the 64-bit prefetchable memory address.
3:0	64BIT	R	64-bit memory indicator. These read-only bits indicate that 64-bit addressing is supported for this memory window.

4.22 Prefetchable Memory Limit Register

This read/write register specifies the upper limit of the prefetchable memory addresses that the bridge forwards downstream. See Table 4-13 for a complete description of the register contents.

PCI register offset: 26h
Register type: Read only, Read/Write
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4-13. Prefetchable Memory Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	PRELIMIT	RW	Prefetchable memory limit. Defines the highest address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. The prefetchable limit upper 32 bits register (offset 2Ch, see Section 4.24) specifies the bit [63:32] of the 64-bit prefetchable memory address.
3:0	64BIT	R	64-bit memory indicator. These read-only bits indicate that 64-bit addressing is supported for this memory window.

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4.23 Prefetchable Base Upper 32 Bits Register

This read/write register specifies the upper 32 bits of the prefetchable memory base register. See Table 4-14 for a complete description of the register contents.

PCI register offset: 28h

Register type: Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-14. Prefetchable Base Upper 32 Bits Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:0	PREBASE	RW	Prefetchable memory base upper 32 bits. Defines the upper 32 bits of the lowest address of the prefetchable memory address range that determines when to forward memory transactions downstream.

4.24 Prefetchable Limit Upper 32 Bits Register

This read/write register specifies the upper 32 bits of the prefetchable memory limit register. See Table 4-15 for a complete description of the register contents.

PCI register offset: 2Ch

Register type: Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-15. Prefetchable Limit Upper 32 Bits Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:0	PRELIMIT	RW	Prefetchable memory limit upper 32 bits. Defines the upper 32 bits of the highest address of the prefetchable memory address range that determines when to forward memory transactions downstream.

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4.25 I/O Base Upper 16 Bits Register

This read/write register specifies the upper 16 bits of the I/O base register. See Table 4-16 for a complete description of the register contents.

PCI register offset: 30h
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-16. I/O Base Upper 16 Bits Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:0	IOBASE	RW	I/O base upper 16 bits. Defines the upper 16 bits of the lowest address of the I/O address range that determines when to forward I/O transactions downstream. These bits correspond to address bits [31:20] in the I/O address. The lower 20 bits are assumed to be 00000h.

4.26 I/O Limit Upper 16 Bits Register

This read/write register specifies the upper 16 bits of the I/O limit register. See Table 4-17 for a complete description of the register contents.

PCI register offset: 32h
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-17. I/O Limit Upper 16 Bits Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:0	IOLIMIT	RW	I/O limit upper 16 bits. Defines the upper 16 bits of the top address of the I/O address range that determines when to forward I/O transactions downstream. These bits correspond to address bits [31:20] in the I/O address. The lower 20 bits are assumed to be FFFFFh.

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4.27 Capabilities Pointer Register

This read-only register provides a pointer into the PCI configuration header where the PCI power management block resides. Since the PCI power-management registers begin at 50h, this register is hardwired to 50h.

PCI register offset: 34h

Register type: Read only

Default value: 50h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	1	0	0	0	0

4.28 Interrupt Line Register

This read/write register is programmed by the system and indicates to the software which interrupt line the bridge has assigned to it. The default value of this register is FFh, indicating that an interrupt line has not yet been assigned to the function. Since the bridge does not generate interrupts internally, this register is a scratchpad register.

PCI register offset: 3Ch

Register type: Read/Write

Default value: FFh

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	1	1	1	1	1	1	1

4.29 Interrupt Pin Register

The interrupt pin register is read-only 00h indicating that the bridge does not generate internal interrupts. While the bridge does not generate internal interrupts, it does forward interrupts from the secondary interface to the primary interface.

PCI register offset: 3Dh

Register type: Read only

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

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4.30 Bridge Control Register

The bridge control register provides extensions to the command register that are specific to a bridge. See Table 4-18 for a complete description of the register contents.

PCI register offset: 3Eh

Register type: Read only, Read/Write, Read/Clear

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-18. Bridge Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:12	RSVD	R	Reserved. Returns 0h when read.
11	DTSERR	RW	Discard timer $\overline{\text{SERR}}$ enable. Applies only in conventional PCI mode. This bit enables the bridge to generate either an ERR_NONFATAL (by default) or ERR_FATAL transaction on the primary interface when the secondary discard timer expires and a delayed transaction is discarded from a queue in the bridge. The severity is selectable only if advanced error reporting is supported. 0 = Do not generate ERR_NONFATAL or ERR_FATAL on the primary interface as a result of the expiration of the secondary discard timer. Note that an error message can still be sent if advanced error reporting is supported and bit 10 (DISCARD_TIMER_MASK) in the secondary uncorrectable error mask register (offset 130h, see Section 5.11) is clear (default). 1 = Generate ERR_NONFATAL or ERR_FATAL on the primary interface if the secondary discard timer expires and a delayed transaction is discarded from a queue in the bridges.
10	DTSTATUS	RCU	Discard timer status. This bit indicates if a discard timer expires and a delayed transaction is discarded. 0 = No discard timer error 1 = Discard timer error
9	SEC_DT		RW selects the number of PCI clocks that the bridge waits for the 1394a OHCI master on the secondary interface to repeat a delayed transaction request. The counter starts once the delayed completion (the completion of the delayed transaction on the primary interface) has reached the head of the downstream queue of the bridge (i.e., all ordering requirements have been satisfied and the bridge is ready to complete the delayed transaction with the initiating master on the secondary bus). If the master does not repeat the transaction before the counter expires, the bridge deletes the delayed transaction from its queue and sets the discard timer status bit. 0 = Secondary discard timer counts 2^{15} PCI clock cycles (default). 1 = Secondary discard timer counts 2^{10} PCI clock cycles.
8	PRI_DEC	R	Primary discard timer. This bit has no meaning in PCIe and is hardwired to 0b.
7	FBB_EN	RW	Fast back-to-back enable. This bit allows software to enable fast back-to-back transactions on the secondary PCI interface. 0 = Fast back-to-back transactions are disabled (default). 1 = Secondary interface fast back-to-back transactions are enabled.
6	SRST	RW	Secondary bus reset. This bit is set when software wishes to reset all devices downstream of the bridge. Setting this bit causes the $\overline{\text{PRST}}$ signal on the secondary interface to be asserted. 0 = Secondary interface is not in reset state (default). 1 = Secondary interface is in the reset state.

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Table 4-18. Bridge Control Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
5	MAM	RW	Master abort mode. This bit controls the behavior of the bridge when it receives a master abort or an unsupported request. 0 = Do not report master aborts. Returns FFFF FFFFh on reads and discard data on writes (default). 1 = Respond with an unsupported request on PCIe when a master abort is received on PCI. Respond with target abort on PCI when an unsupported request completion on PCIe is received. This bit also enables error signaling on master abort conditions on posted writes.
4	VGA16	RW	VGA 16-bit decode. This bit enables the bridge to provide full 16-bit decoding for VGA I/O addresses. This bit only has meaning if the VGA enable bit is set. 0 = Ignore address bits [15:10] when decoding VGA I/O addresses (default) 1 = Decode address bits [15:10] when decoding VGA I/O addresses
3	VGA	RW	VGA enable. This bit modifies the response by the bridge to VGA compatible addresses. If this bit is set, the bridge decodes and forwards the following accesses on the primary interface to the secondary interface (and, conversely, block the forwarding of these addresses from the secondary to primary interface): Memory accesses in the range 000A 0000h to 000B FFFFh I/O addresses in the first 64 KB of the I/O address space (address bits [31:16] are 0000h) and where address bits [9:0] are in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – address bits [15:10] may possess any value and are not used in the decoding) If this bit is set, forwarding of VGA addresses is independent of the value of bit 2 (ISA), the I/O address and memory address ranges defined by the I/O base and limit registers, the memory base and limit registers, and the prefetchable memory base and limit registers of the bridge. The forwarding of VGA addresses is qualified by bits 0 (IO_ENB) and 1 (MEMORY_ENB) in the command register (offset 04h, see Section 4.3). 0 = Do not forward VGA-compatible memory and I/O addresses from the primary to secondary interface (addresses previously defined) unless they are enabled for forwarding by the defined I/O and memory address ranges (default). 1 = Forward VGA-compatible memory and I/O addresses (addresses previously defined) from the primary interface to the secondary interface (if the I/O enable and memory enable bits are set) independent of the I/O and memory address ranges and independent of the ISA enable bit.
2	ISA	RW	ISA enable. This bit modifies the response by the bridge to ISA I/O addresses. This applies only to I/O addresses that are enabled by the I/O base and I/O limit registers and are in the first 64 KB of PCI I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, the bridge blocks any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block. 0 = Forward downstream all I/O addresses in the address range defined by the I/O base and I/O limit registers (default) 1 = Forward upstream ISA I/O addresses in the address range defined by the I/O base and I/O limit registers that are in the first 64 KB of PCI I/O address space (top 768 bytes of each 1-KB block)
1	SERR_EN	RW	SERR enable. This bit controls forwarding of system error events from the secondary interface to the primary interface. The bridge forwards system error events when: This bit is set. Bit 8 (SERR_ENB) in the command register (offset 04h, see Section 4.3) is set. $\overline{\text{SERR}}$ is asserted on the secondary interface. 0 = Disable the forwarding of system error events (default) 1 = Enable the forwarding of system error events

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Table 4-18. Bridge Control Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
0	PERR_EN	RW	Parity error response enable. Controls the bridge's response to data, uncorrectable address, and attribute errors on the secondary interface. Also, the bridge always forwards data with poisoning, from conventional PCI to PCIe on an uncorrectable conventional PCI data error, regardless of the setting of this bit. 0 = Ignore uncorrectable address, attribute, and data errors on the secondary interface (default) 1 = Enable uncorrectable address, attribute, and data error detection and reporting on the secondary interface

4.31 PM Capability ID Register

This read-only register identifies the linked list item as the register for PCI power management. The register returns 01h when read.

PCI register offset: 50h
Register type: Read only
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

4.32 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 80h pointing to the subsystem ID capabilities registers.

PCI register offset: 51h
Register type: Read only
Default value: 60h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	1	0	0	0	0	0

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4.33 Power Management Capabilities Register

This read-only register indicates the capabilities of the bridge related to PCI power management. See Table 4-19 for a complete description of the register contents.

PCI register offset: 52h

Register type: Read only

Default value: 0603h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1

Table 4-19. Power Management Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:11	PME_SUPPORT	R	$\overline{\text{PME}}$ support. This 5-bit field indicates the power states from which the bridge may assert PME. Because the bridge never generates a PME except on a behalf of a secondary device, this field is read only and returns 00000b.
10	D2_SUPPORT	R	This bit returns a 1b when read, indicating that the function supports the D2 device power state.
9	D1_SUPPORT	R	This bit returns a 1b when read, indicating that the function supports the D1 device power state.
8:6	AUX_CURRENT	R	3.3 V_{AUX} auxiliary current requirements. This field returns 000b since the bridge does not generate $\overline{\text{PME}}$ from $D3_{cold}$.
5	DSI	R	Device specific initialization. This bit returns 0b when read, indicating that the bridge does not require special initialization beyond the standard PCI configuration header before a generic class driver is able to use it.
4	RSVD	R	Reserved. Returns 0b when read.
3	PME_CLK	R	$\overline{\text{PME}}$ clock. This bit returns 0b indicating that the PCI clock is not needed to generate $\overline{\text{PME}}$.
2:0	PM_VERSION	R	Power-management version. If bit 26 (PCI_PM_VERSION_CTRL) in the general control register (offset D4h, see Section 4.66) is 0b, this field returns 010b indicating revision 1.1 compatibility. If PCI_PM_VERSION_CTRL is 1b, this field returns 011b indicating revision 1.2 compatibility.

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4.34 Power Management Control/Status Register

This register determines and changes the current power state of the bridge. No internal reset is generated when transitioning from the $D3_{hot}$ state to the D0 state. See Table 4-20 for a complete description of the register contents.

PCI register offset: 54h
Register type: Read only, Read/Write
Default value: 0008h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Table 4-20. Power Management Control/Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PME_STAT	R	$\overline{PME}$ status. This bit is read only and returns 0b when read.
14:13	DATA_SCALE	R	Data scale. This 2-bit field returns 00b when read since the bridge does not use the data register.
12:9	DATA_SEL	R	Data select. This 4-bit field returns 0h when read since the bridge does not use the data register.
8	PME_EN	RW	$\overline{PME}$ enable. This bit has no function and acts as scratchpad space. The default value for this bit is 0b.
7:4	RSVD	R	Reserved. Returns 0h when read.
3	NO_SOFT_RESET	R	No soft reset. If bit 26 (PCI_PM_VERSION_CTRL) in the general control register (offset D4h, see Section 4.66) is 0b, this bit returns 0b for compatibility with version 1.1 of the PCI Power Management Specification. If PCI_PM_VERSION_CTRL is 1b, this bit returns 1b indicating that no internal reset is generated and the device retains its configuration context when transitioning from the $D3_{hot}$ state to the D0 state.
2	RSVD	R	Reserved. Returns 0b when read.
1:0	PWR_STATE	RW	Power state. This 2-bit field determines the current power state of the function and sets the function into a new power state. This field is encoded as follows: 00 = D0 (default) 01 = D1 10 = D2 11 = $D3_{hot}$

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4.35 Power Management Bridge Support Extension Register

This read-only register indicates to host software what the state of the secondary bus will be when the bridge is placed in D3. See Table 4-21 for a complete description of the register contents.

PCI register offset: 56h

Register type: Read only

Default value: 40h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	0	0	0	0	0

Table 4-21. PM Bridge Support Extension Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	BPCC	R	Bus power/clock control enable. This bit indicates to the host software if the bus secondary clocks are stopped when the bridge is placed in D3. The state of the BPCC bit is controlled by bit 11 (BPCC_E) in the general control register (offset D4h, see Section 4.66). 0 = Secondary bus clocks are not stopped in D3. 1 = Secondary bus clocks are stopped in D3.
6	BSTATE	R	B2/B3 support. This bit is read-only 1b indicating that the bus state in D3 is B2.
5:0	RSVD	R	Reserved. Returns 00 0000b when read.

4.36 Power Management Data Register

The read-only register is not applicable to the bridge and returns 00h when read.

PCI register offset: 57h

Register type: Read only

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.37 MSI Capability ID Register

This read-only register identifies the linked list item as the register for message signaled interrupts capabilities. The register returns 05h when read.

PCI register offset: 60h

Register type: Read only

Default value: 05h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	0	1

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4.38 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 80h pointing to the subsystem ID capabilities registers.

PCI register offset: 61h
Register type: Read only
Default value: 80h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	0	0

4.39 MSI Message Control Register

This register controls the sending of MSI messages. See Table 4-22 for a complete description of the register contents.

PCI register offset: 62h
Register type: Read only, Read/Write
Default value: 0088h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0

Table 4-22. MSI Message Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Returns 00h when read.
7	64CAP	R	64-bit message capability. This bit is read-only 1b indicating that the bridge supports 64-bit MSI message addressing.
6:4	MM_EN	RW	Multiple message enable. This bit indicates the number of distinct messages that the bridge is allowed to generate. 000 = 1 message (default) 001 = 2 messages 010 = 4 messages 011 = 8 messages 100 = 16 messages 101 = Reserved 110 = Reserved 111 = Reserved
3:1	MM_CAP	R	Multiple message capabilities. This field indicates the number of distinct messages that the bridge is capable of generating. This field is read-only 100b, indicating that the bridge can signal 1 interrupt for each IRQ supported on the serial IRQ stream up to a maximum of 16 unique interrupts.
0	MSI_EN	RW	MSI enable. This bit enables MSI interrupt signaling. MSI signaling must be enabled by software for the bridge to signal that a serial IRQ has been detected. 0 = MSI signaling is prohibited (default). 1 = MSI signaling is enabled.

NOTE

Enabling MSI messaging in the XIO2213B has no effect.

4.40 MSI Message Lower Address Register

This register contains the lower 32 bits of the address that a MSI message writes to when a serial IRQ is detected. See Table 4-23 for a complete description of the register contents.

PCI register offset: 64h

Register type: Read only, Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-23. MSI Message Lower Address Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:2	ADDRESS	RW	System specified message address
1:0	RSVD	R	Reserved. Returns 00b when read.

NOTE

Enabling MSI messaging in the XIO2213B has no effect.

4.41 MSI Message Upper Address Register

This register contains the upper 32 bits of the address that a MSI message writes to when a serial IRQ is detected. If this register contains 0000 0000h, 32-bit addressing is used; otherwise, 64-bit addressing is used.

PCI register offset: 68h

Register type: Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTE

Enabling MSI messaging in the XIO2213B has no effect.

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4.42 MSI Message Data Register

This register contains the data that software programmed the bridge to send when it send a MSI message. See Table 4-24 for a complete description of the register contents.

PCI register offset: 6Ch
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-24. MSI Message Data Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MSG	RW	System specific message. This field contains the portion of the message that the bridge forwards unmodified.
3:0	MSG_NUM	RW	Message number. This portion of the message field may be modified to contain the message number is multiple messages are enable. The number of bits that are modifiable depends on the number of messages enabled in the message control register. 1 message = No message data bits can be modified (default). 2 messages = Bit 0 can be modified. 4 messages = Bits 1:0 can be modified. 8 messages = Bits 2:0 can be modified. 16 messages = Bits 3:0 can be modified.

NOTE

Enabling MSI messaging in the XIO2213B has no effect.

4.43 SSID/SSVID Capability ID Register

This read-only register identifies the linked list item as the register for subsystem ID and subsystem vendor ID capabilities. The register returns 0Dh when read.

PCI register offset: 80h
Register type: Read only
Default value: 0Dh

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	1	1	0	1

4.44 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 90h pointing to the PCI Express capabilities registers.

PCI register offset: 81h
Register type: Read only
Default value: 90h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	1	0	0	0	0

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4.45 Subsystem Vendor ID Register

This register, used for system and option card identification purposes, may be required for certain operating systems. This read-only register is initialized through the EEPROM and can be written through the subsystem alias register. This register shall only be reset by a fundamental reset ($\overline{\text{FRST}}$).

PCI register offset: 84h

Register type: Read only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.46 Subsystem ID Register

This register, used for system and option card identification purposes, may be required for certain operating systems. This read-only register is initialized through the EEPROM and can be written through the subsystem alias register. This register shall only be reset by $\overline{\text{FRST}}$.

PCI register offset: 86h

Register type: Read only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.47 PCI Express Capability ID Register

This read-only register identifies the linked list item as the register for PCIe capabilities. The register returns 10h when read.

PCI register offset: 90h

Register type: Read only

Default value: 10h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0

4.48 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 00h indicating no additional capabilities are supported.

PCI register offset: 91h

Register type: Read only

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

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4.49 PCI Express Capabilities Register

This read-only register indicates the capabilities of the bridge related to PCIe. See Table 4-25 for a complete description of the register contents.

PCI register offset: 92h
Register type: Read only
Default value: 0071h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1

Table 4-25. PCI Express Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:9	RSVD	R	Reserved. Returns 000 0000b when read.
8	SLOT	R	Slot implemented. This bit is not valid for the bridge and is read-only 0b.
7:4	DEV_TYPE	R	Device/port type. This read-only field returns 0111b indicating that the device is a PCIe to PCI bridge.
3:0	VERSION	R	Capability version. This field returns 1h indicating revision 1 of the PCIe capability.

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4.50 Device Capabilities Register

This register indicates the device-specific capabilities of the bridge. See Table 4-26 for a complete description of the register contents.

PCI register offset: 94h

Register type: Read only

Default value: 0000 8002

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Table 4-26. Device Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:28	RSVD	R	Reserved. Returns 0h when read.
27:26	CSPLS	RU	Captured slot power limit scale. The value in this field is programmed by the host by issuing a Set_Slot_Power_Limit message. When a Set_Slot_Power_Limit message is received, bits 9:8 are written to this field. The value in this field specifies the scale used for the slot power limit. 00 = 1.0x 01 = 0.1x 10 = 0.01x 11 = 0.001x1
25:18	CSPLV	RU	Captured slot power limit value. The value in this field is programmed by the host by issuing a Set_Slot_Power_Limit message. When a Set_Slot_Power_Limit message is received, bits 7:0 are written to this field. The value in this field in combination with the slot power limit scale value (bits 27:26) specifies the upper limit of power supplied to the slot. The power limit is calculated by multiplying the value in this field by the value in the slot power limit scale field.
17:16	RSVD	R	Reserved. Return 000b when read.
15	RBER	R	Role-based error reporting. This bit is hardwired to 1 indicating that the XIO2213B supports role-based error reporting.
14	PIP	R	Power indicator present. This bit is hardwired to 0b indicating that a power indicator is not implemented.
13	AIP	R	Attention indicator present. This bit is hardwired to 0b indicating that an attention indicator is not implemented.
12	ABP	R	Attention button present. This bit is hardwired to 0b indicating that an attention button is not implemented.
11:9	EP_L1_LAT	RU	Endpoint L1 acceptable latency. This field indicates the maximum acceptable latency for a transition from L1 to L0 state. This field can be programmed by writing to the L1_LATENCY field (bits 15:13) in the general control register (offset D4h, see Section 4.66). The default value for this field is 000b, which indicates a range less than 1s. This field cannot be programmed to be less than the latency for the PHY to exit the L1 state.
8:6	EP_L0S_LAT	RU	Endpoint L0s acceptable latency. This field indicates the maximum acceptable latency for a transition from L0s to L0 state. This field can be programmed by writing to the L0s_LATENCY field (bits 18:16) in the general control register (offset D4h, see Section 4.66). The default value for this field is 000b, which indicates a range less than 1s. This field cannot be programmed to be less than the latency for the PHY to exit the L0s state.
5	ETFS	R	Extended tag field supported. This field indicates the size of the tag field not supported.
4:3	PFS	R	Phantom functions supported. This field is read-only 00b indicating that function numbers are not used for phantom functions.
2:0	MPSS	R	Maximum payload size supported. This field indicates the maximum payload size that the device can support for TLPs. This field is encoded as 010b indicating the maximum payload size for a TLP is 512 bytes.

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4.51 Device Control Register

The device control register controls PCIe device-specific meters. See Table 4-27 for a complete description of the register contents.

PCI register offset: 98h
Register type: Read only, Read/Write
Default value: 2800h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0

Table 4-27. Device Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	CFG_RTRY_ENB	RW	Configuration retry status enable. When this read/write bit is set to 1b, the bridge returns a completion with completion retry status on PCIe if a configuration transaction forwarded to the secondary interface did not complete within the implementation specific time-out period. When this bit is set to 0b, the bridge does not generate completions with completion retry status on behalf of configuration transactions. The default value of this bit is 0b.
14:12	MRRS	RW	Maximum read request size. This field is programmed by host software to set the maximum size of a read request that the bridge can generate. The bridge uses this field in conjunction with the cache line size register (offset 0Ch, see Section 7.6) to determine how much data to fetch on a read request. This field is encoded as: 000 = 128B 001 = 256B 010 = 512B (default) 011 = 1024B 100 = 2048B 101 = 4096B 110 = Reserved 111 = Reserved
11	ENS	RW	Enable no snoop. Controls the setting of the no snoop flag within the TLP header for upstream memory transactions mapped to any traffic class mapped to a virtual channel (VC) other than VC0 through the upstream decode windows. 0 = No snoop field is 0b. 1 = No snoop field is 1b (default).
10*	APPE	RW	Auxiliary power PM enable. This bit has no effect in the bridge. 0 = AUX power is disabled (default). 1 = AUX power is enabled.
9	PFE	R	Phantom function enable. Since the bridge does not support phantom functions, this bit is read-only 0b.
8	ETFE	R	Extended tag field enable. Since the bridge does not support extended tags, this bit is read-only 0b.
7:5	MPS	RW	Maximum payload size. This field is programmed by host software to set the maximum size of posted writes or read completions that the bridge can initiate. This field is encoded as: 000 = 128B (default) 001 = 256B 010 = 512B 011 = 1024B 100 = 2048B 101 = 4096B 110 = Reserved 111 = Reserved
4	ERO	R	Enable relaxed ordering. Since the bridge does not support relaxed ordering, this bit is read-only 0b.
3	URRE	RW	Unsupported request reporting enable. If this bit is set, the bridge sends an ERR_NONFATAL message to the root complex when an unsupported request is received. 0 = Do not report unsupported requests to the root complex (default) 1 = Report unsupported requests to the root complex

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Table 4-27. Device Control Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
2	FERE	RW	Fatal error reporting enable. If this bit is set, the bridge is enabled to send ERR_FATAL messages to the root complex when a system error event occurs. 0 = Do not report fatal errors to the root complex (default) 1 = Report fatal errors to the root complex
1	NFERE	RW	Nonfatal error reporting enable. If this bit is set, the bridge is enabled to send ERR_NONFATAL messages to the root complex when a system error event occurs. 0 = Do not report nonfatal errors to the root complex (default) 1 = Report nonfatal errors to the root complex
0	CERE	RW	Correctable error reporting enable. If this bit is set, the bridge is enabled to send ERR_COR messages to the root complex when a system error event occurs. 0 = Do not report correctable errors to the root complex (default) 1 = Report correctable errors to the root complex

4.52 Device Status Register

The device status register provides PCIe device specific information to the system. See Table 4-28 for a complete description of the register contents.

PCI register offset: 9Ah

Register type: Read only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-28. Device Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:6	RSVD	R	Reserved. Returns 00 0000 0000b when read.
5	PEND	RU	Transaction pending. This bit is set when the bridge has issued a nonposted transaction that has not been completed.
4	APD	RU	AUX power detected. This bit indicates that AUX power is present. 0 = No AUX power detected 1 = AUX power detected
3	URD	RCU	Unsupported request detected. This bit is set by the bridge when an unsupported request is received.
2	FED	RCU	Fatal error detected. This bit is set by the bridge when a fatal error is detected.
1	NFED	RCU	Nonfatal error detected. This bit is set by the bridge when a nonfatal error is detected.
0	CED	RCU	Correctable error detected. This bit is set by the bridge when a correctable error is detected.

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4.53 Link Capabilities Register

The link capabilities register indicates the link-specific capabilities of the bridge. See Table 4-29 for a complete description of the register contents.

PCI register offset: 9Ch
Register type: Read only
Default value: 0006 XC11h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	x	x	x	1	1	0	0	0	0	0	1	0	0	0	1

Table 4-29. Link Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	PORT_NUM	R	Port number. This field indicates port number for the PCIe link. This field is read-only 00h indicating that the link is associated with port 0.
23:19	RSVD	R	Reserved. Return 00 0000b when read.
18	CLK_PM	R	Clock power management. This bit is hardwired to 1 to indicate that XIO2213B supports clock power management through $\overline{\text{CLKREQ}}$ protocol.
17:15	L1_LATENCY	R	L1 exit latency. This field indicates the time that it takes to transition from the L1 state to the L0 state. Bit 6 (CCC) in the link control register (offset A0h, see Section 4.54) equals 1b for a common clock and equals 0b for an asynchronous clock. For a common reference clock, the value of this field is determined by bits 20:18 (L1_EXIT_LAT_ASYNC) of the control and diagnostic register 1 (offset C4h, see Section 4.63). For an asynchronous reference clock, the value of this field is determined by bits 17:15 (L1_EXIT_LAT_COMMON) of the control and diagnostic register 1 (offset C4h, see Section 4.63).
14:12	L0S_LATENCY	R	L0s exit latency. This field indicates the time that it takes to transition from the L0s state to the L0 state. Bit 6 (CCC) in the link control register (offset A0h, see Section 4.54) equals 1b for a common clock and equals 0b for an asynchronous clock. For a common reference clock, the value of 011b indicates that the L1 exit latency falls between 256 ns to less than 512 ns. For an asynchronous reference clock, the value of 100b indicates that the L1 exit latency falls between 512 ns to less than 1 s.
11:10	ASLPMS	R	Active-state link PM support. This field indicates the level of active-state power management that the bridge supports. The value 11b indicates support for both L0s and L1 through active-state power management.
9:4	MLW	R	Maximum link width. This field is encoded 00 0001b to indicate that the bridge only supports a 1× PCIe link.
3:0	MLS	R	Maximum link speed. This field is encoded 1h to indicate that the bridge supports a maximum link speed of 2.5 Gb/s.

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4.54 Link Control Register

The link control register controls link-specific behavior. See Table 4-30 for a complete description of the register contents.

PCI register offset: A0h

Register type: Read only, Read/Write

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-30. Link Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:9	RSVD	RW	Reserved. Returns 00h when read.
8	CPM_EN	RW	Clock power management enable. This bit is used to enable XIO2213B to use $\overline{\text{CLKREQ}}$ for clock power management 0 = Clock power management is disabled and XIO2213B shall hold the $\overline{\text{CLKREQ}}$ signal low. 1 = Clock power management is enabled and XIO2213B is permitted to use the $\overline{\text{CLKREQ}}$ signal to allow the REFCLK input to be stopped.
7	ES	RW	Extended synch. This bit forces the bridge to extend the transmission of FTS ordered sets and an extra TS2 when exiting from L1 prior to entering to L0. 0 = Normal synch (default) 1 = Extended synch
6	CCC	RW	Common clock configuration. When this bit is set, it indicates that the bridge and the device at the opposite end of the link are operating with a common clock source. A value of 0b indicates that the bridge and the device at the opposite end of the link are operating with se te reference clock sources. The bridge uses this common clock configuration information to report the correct L0s and L1 exit latencies. 0 = Reference clock is asynchronous (default). 1 = Reference clock is common.
5	RL	R	Retrain link. This bit has no function and is read-only 0b.
4	LD	R	Link disable. This bit has no function and is read-only 0b.
3	RCB	RW	Read completion boundary. This bit is an indication of the RCB of the root complex. The state of this bit has no effect on the bridge, since the RCB of the bridge is fixed at 128 bytes. 0 = 64 bytes (default) 1 = 128 bytes
2	RSVD	R	Reserved. Returns 0b when read.
1:0	ASLPMC	RW	Active-state link PM control. This field enables and disables the active-state PM. 00 = Active-state PM disabled (default) 01 = L0s entry enabled 10 = L1 entry enabled 11 = L0s and L1 entry enabled

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4.55 Link Status Register

The link status register indicates the current state of the PCIe link. See Table 4-31 for a complete description of the register contents.

PCI register offset: A2h
Register type: Read only
Default value: X011h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	x	0	0	0	0	0	0	0	1	0	0	0	1

Table 4-31. Link Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:13	RSVD	R	Reserved. Returns 000b when read.
12	SCC	R	Slot clock configuration. This bit indicates that the bridge uses the same physical reference clock that the platform provides on the connector. If the bridge uses an independent clock irrespective of the presence of a reference on the connector, this bit must be cleared. 0 = Independent 125-MHz reference clock is used. 1 = Common 100-MHz reference clock is used.
11	LT	R	Link training. This bit has no function and is read-only 0b.
10	TE	R	Retrain link. This bit has no function and is read-only 0b.
9:4	NLW	R	Negotiated link width. This field is read-only 00 0001b indicating the lane width is 1×.
3:0	LS	R	Link speed. This field is read-only 1h indicating the link speed is 2.5 Gb/s.

4.56 Serial-Bus Data Register

The serial-bus data register reads and writes data on the serial-bus interface. Write data is loaded into this register prior to writing the serial-bus slave address register (offset B2h, see Section 4.58) that initiates the bus cycle. When reading data from the serial bus, this register contains the data read after bit 5 (REQBUSY) of the serial-bus control and status register (offset B3h, see Section 4.59) is cleared. This register shall only be reset by $\overline{\text{FRST}}$.

PCI register offset: B0h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.57 Serial-Bus Word Address Register

The value written to the serial-bus word address register represents the word address of the byte being read from or written to the serial-bus device. The word address is loaded into this register prior to writing the serial-bus slave address register (offset B2h, see Section 4.58) that initiates the bus cycle. This register shall only be reset by $\overline{\text{FRST}}$.

PCI register offset: B1h
Register type: Read/Write
Default value: 00h

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BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.58 Serial-Bus Slave Address Register

The serial-bus slave address register indicates the slave address of the device being targeted by the serial-bus cycle. This register also indicates if the cycle is a read or a write cycle. Writing to this register initiates the cycle on the serial interface. See Table 4-32 for a complete description of the register contents.

PCI register offset: B2h

Register type: Read/Write

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4-32. Serial-Bus Slave Address Register Descriptions

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1 (1)	SLAVE_ADDR	RW	Serial-bus slave address. This 7-bit field is the slave address for a serial-bus read or write transaction. The default value for this field is 000 0000b.
0 (1)	RW_CMD	RW	Read/write command. This bit determines if the serial-bus cycle is a read or a write cycle. 0 = A single byte write is requested (default). 1 = A single byte read is requested.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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4.59 Serial-Bus Control and Status Register

The serial-bus control and status register controls the behavior of the serial-bus interface. This register also provides status information about the state of the serial bus. See Table 4-33 for a complete description of the register contents.

PCI register offset: B3h

Register type: Read only, Read/Write, Read/Clear

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4-33. Serial-Bus Control and Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7(1)	PROT_SEL	RW	Protocol select. This bit selects the serial-bus address mode used. 0 = Slave address and word address are sent on the serial bus (default 1 = Only the slave address is sent on the serial bus.
6	RSVD	R	Reserved. Returns 0b when read.
5(1)	REQBUSY	RU	Requested serial-bus access busy. This bit is set when a software-initiated serial-bus cycle is in progress. 0 = No serial-bus cycle 1 = Serial-bus cycle in progress
4(1)	ROMBUSY	RU	Serial EEPROM access busy. This bit is set when the serial EEPROM circuitry in the bridge is downloading register defaults from a serial EEPROM. 0 = No EEPROM activity 1 = EEPROM download in progress
3(1)	SBDETECT	RWU	Serial EEPROM access busy. This bit is set when the serial EEPROM circuitry in the bridge is downloading register defaults from a serial EEPROM. Note: A serial EEPROM is only detected once following $\overline{\text{PERST}}$. 0 = No EEPROM present, EEPROM load process does not happen. GPIO4//SCL and GPIO5//SDA terminals are configured as GPIO signals. 1 = EEPROM present, EEPROM load process takes place. GPIO4//SCL and GPIO5//SDA terminals are configured as serial-bus signals.
2(1)	SBTEST	RW	Serial-bus test. This bit is used for internal test purposes. This bit controls the clock source for the serial interface clock. 0 = Serial-bus clock at normal operating frequency ~60 kHz (default) 1 = Serial-bus clock frequency increased for test purposes ~4 MHz
1(1)	SB_ERR	RCU	Serial-bus error. This bit is set when an error occurs during a software-initiated serial-bus cycle. 0 = No error 1 = Serial-bus error
0(1)	ROM_ERR	RCU	Serial EEPROM load error. This bit is set when an error occurs while downloading registers from serial EEPROM. 0 = No error 1 = EEPROM load error

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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4.60 GPIO Control Register

This register controls the direction of the eight GPIO terminals. This register has no effect on the behavior of GPIO terminals that are enabled to perform secondary functions. The secondary functions share GPIO4 (SCL) and GPIO5 (SDA). See Table 4-34 for a complete description of the register contents.

PCI register offset: B4h

Register type: Read only, Read/Write

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-34. GPIO Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Return 00h when read.
7(1)	GPIO7_DIR	RW	GPIO 7 data direction. This bit selects whether GPIO7 is in input or output mode. 0 = Input (default) 1 = Output
6(1)	GPIO6_DIR	RW	GPIO 6 data direction. This bit selects whether GPIO6 is in input or output mode. 0 = Input (default) 1 = Output
5(1)	GPIO5_DIR	RW	GPIO 5 data direction. This bit selects whether GPIO5 is in input or output mode. 0 = Input (default) 1 = Output
4(1)	GPIO4_DIR	RW	GPIO 4 data direction. This bit selects whether GPIO4 is in input or output mode. 0 = Input (default) 1 = Output
3(1)	GPIO3_DIR	RW	GPIO 3 data direction. This bit selects whether GPIO3 is in input or output mode. 0 = Input (default) 1 = Output
2(1)	GPIO2_DIR	RW	GPIO 2 data direction. This bit selects whether GPIO2 is in input or output mode. 0 = Input (default) 1 = Output
1(1)	GPIO1_DIR	RW	GPIO 1 data direction. This bit selects whether GPIO1 is in input or output mode. 0 = Input (default) 1 = Output
0(1)	GPIO0_DIR	RW	GPIO 0 data direction. This bit selects whether GPIO0 is in input or output mode. 0 = Input (default) 1 = Output

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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4.61 GPIO Data Register

This register reads the state of the input-mode GPIO terminals and changes the state of the output-mode GPIO terminals. Writing to a bit that is in input mode or is enabled for a secondary function is ignored. The secondary functions share GPIO4 (SCL) and GPIO5 (SDA). The default value at power up depends on the state of the GPIO terminals as they default to general-purpose inputs. See Table 4-35 for a complete description of the register contents.

PCI register offset: B6h

Register type: Read only, Read/Write

Default value: 00XXh

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Table 4-35. GPIO Data Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved
7(1)	GPIO7_DATA	RW	GPIO 7 data. This bit reads the state of GPIO7 when in input mode or changes the state of GPIO7 when in output mode.
6(1)	GPIO6_DATA	RW	GPIO 6 data. This bit reads the state of GPIO6 when in input mode or changes the state of GPIO6 when in output mode.
5(1)	GPIO5_DATA	RW	GPIO 5 data. This bit reads the state of GPIO5 when in input mode or changes the state of GPIO5 when in output mode.
4(1)	GPIO4_DATA	RW	GPIO 4 data. This bit reads the state of GPIO4 when in input mode or changes the state of GPIO4 when in output mode.
3(1)	GPIO3_DATA	RW	GPIO 3 data. This bit reads the state of GPIO3 when in input mode or changes the state of GPIO3 when in output mode.
2(1)	GPIO2_DATA	RW	GPIO 2 data. This bit reads the state of GPIO2 when in input mode or changes the state of GPIO2 when in output mode.
1(1)	GPIO1_DATA	RW	GPIO 1 data. This bit reads the state of GPIO1 when in input mode or changes the state of GPIO1 when in output mode.
0(1)	GPIO0_DATA	RW	GPIO 0 data. This bit reads the state of GPIO0 when in input mode or changes the state of GPIO0 when in output mode.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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4.62 Control and Diagnostic Register 0

The contents of this register are used for monitoring status and controlling behavior of the bridge. See Table 4-36 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset: C0h

Register type: Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-36. Control and Diagnostic Register 0 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24(1)	PRI_BUS_NUM	R	This field contains the captured primary bus number.
23:19(1)	PRI_DEVICE_NUM	R	This field contains the captured primary device number.
18	ALT_ERROR_REP	RW	Alternate error reporting. This bit controls the method that the XIO2213B uses for error reporting. 0 = Advisory nonratal error reporting supported (default) 1 = Advisory nonfatal error reporting not supported
17(2)	DIS_BRIDGE_PME	RW	Disable bridge $\overline{\text{PME}}$ input 0 = $\overline{\text{PME}}$ input signal to the bridge is enabled and connected to the $\overline{\text{PME}}$ signal from the 1394 OHCI function (default). 1 = $\overline{\text{PME}}$ input signal to the bridge is disabled.
16(2)	DIS_OHCI_PME	RW	Disable $\overline{\text{OHCI_PME}}$ 0 = $\overline{\text{OHCI_PME}}$ pin is enabled and connected to the $\overline{\text{PME}}$ signal from the 1394 OHCI function (default). 1 = $\overline{\text{OHCI_PME}}$ pin is disabled.
15:14(1)	FIFO_SIZE	RW	FIFO size. This field contains the maximum size (in DW) of the FIFO.
13:12	RSVD	R	Reserved. Returns 00b when read.
11	ALLOW_CFG_ANY_FN	RW	Allow configuration access to any function. When this bit is set, the bridge shall respond to configuration accesses to any function number.
10	RETURN_PW_CREDITS	RW	Return PW packet credits. When this bit is set, the bridge shall return all the PW packet credits.
9	RSVD	R	Reserved. Returns 0b when read.
8	RETURN_CPL_CREDITS	RW	Return completion credits. When this bit is set, the bridge shall return all completion credits immediately.
7	EN_CACHE_LINE_CHECK	RW	Enable cache line check 0 = Bridge shall use side-band signals to determine the transaction size (default). 1 = Bridge shall use the cache line size register to determine the transaction size.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.
(2) These bits are reset only by a global reset ($\overline{\text{GRST}}$) or the internally generated power-on reset.

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Table 4-36. Control and Diagnostic Register 0 Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
6(1)	PREFETCH_4X	RW	Prefetch 4× enable 0 = Bridge prefetches up to two cache lines, as defined in the cache line size register (offset 0Ch, see Section 7.6) for upstream memory read multiple (MRM) transactions (default). 1 = Bridge prefetches up to four cache lines, as defined in the cache line size register (offset 0Ch, see Section 7.6) for upstream memory read multiple (MRM) transactions.
			Note: When this bit is set and the FORCE_MRM bit in the general control register is set, both upstream memory read multiple transactions and upstream memory transactions prefetch up to four cache lines. Note: When the READ_PREFETCH_DIS bit in the general control register is set, this bit has no effect and only one DWORD will be fetched on a burst read. This bit only affects the XIO2213B design when the EN_CACHE_LINE_CHECK bit is set.
5:4(1)	UP_REQ_BUF_VALUE	RW	PCI upstream req-res buffer threshold value. The value in this field controls the buffer space that must be available for the device to accept a PCI bus transaction. If the cache line size is not valid, the device will use eight DW for calculating the threshold value. 00 = 1 cache line + 4 DW (default) 01 = 1 cache line + 8 DW 10 = 1 cache line + 12 DW 11 = 2 cache lines + 4 DW
3(1)	UP_REQ_BUF_CTRL	RW	PCI upstream req-res buffer threshold control. This bit enables the PCI upstream req-res buffer threshold control mode of the bridge. 0 = PCI upstream req-res buffer threshold control mode disabled (default) 1 = PCI upstream req-res buffer threshold control mode enabled
2(1)	CFG_ACCESS_MEM_REG	RW	Configuration access to memory-mapped registers. When this bit is set, the bridge allows configuration access to memory-mapped configuration registers.
1(1)	RSVD	RW	Reserved. Bit 1 defaults to 0b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 0b.
0	RSVD	R	Reserved. Returns 0b when read.

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4.63 Control and Diagnostic Register 1

The contents of this register are used for monitoring status and controlling behavior of the bridge. See Table 4-37 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset: C4h

Register type: Read/Write

Default value: 0012 0108h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0

Table 4-37. Control and Diagnostic Register 1 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
32:21	RSVD	R	Reserved. Returns 000h when read.
20:18(1)	L1_EXIT_LAT_ASYNC	RW	L1 exit latency for asynchronous clock. When bit 6 (CCC) of the link control register (offset A0h, see Section 4.54) is set, the value in this field is mirrored in bits 17:15 (L1_LATENCY) field in the link capabilities register (offset 9Ch, see Section 4.53). This field defaults to 100b.
17:15(1)	L1_EXIT_LAT_COMMON	RW	L1 exit latency for common clock. When bit 6 (CCC) of the link control register (offset A0h, see Section 4.54) is clear, the value in this field is mirrored in bits 17:15 (L1_LATENCY) field in the link capabilities register (offset 9Ch, see Section 4.53). This field defaults to 100b.
14:11(1)	RSVD	RW	Reserved. Bits 14:11 default to 0000b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 0000b.
10(1)	SBUS_RESET_MASK	RW	Secondary bus reset bit mask. When this bit is set, the bridge masks the reset caused by bit 6 (SRST) of the bridge control register (offset 3Eh, see Section 4.30). This bit defaults to 0b.
9:6(1)	L1ASPM_TIMER	RW	L1ASPM entry timer. This field specifies the value (in 512-ns ticks) of the L1ASPM entry timer. This field defaults to 0100b.
5:2(1)	L0s_TIMER	RW	L0s entry timer. This field specifies the value (in 62.5-MHz clock ticks) of the L0s entry timer. This field defaults to 0010b.
1:0(1)	RSVD	RW	Reserved. Bits 1:0 default to 00b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 00b.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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4.64 PHY Control and Diagnostic Register 2

The contents of this register are used for monitoring status and controlling behavior of the PHY macro for diagnostic purposes. See Table 4-38 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset: C8h

Register type: Read/Write

Default value: 3214 2000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	1	1	0	0	1	0	0	0	0	1	0	1	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-38. Control and Diagnostic Register 2 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24(1)	N_FTS_ ASYNC_ CLK	RW	N_FTS for asynchronous clock. When bit 6 (CCC) of the link control register (offset A0h, see Section 4.54) is clear, the value in this field is the number of FTS that are sent on a transition from L0s to L0. This field shall default to 32h.
23:16(1)	N_FTS_COMMON_ CLK	RW	N_FTS for common clock. When bit 6 (CCC) of the link control register (offset A0h, see Section 4.54) is set, the value in this field is the number of FTS that are sent on a transition from L0s to L0. This field defaults to 14h.
15:13	PHY_REV	R	PHY revision number
12:8(1)	LINK_NUM	RW	Link number
7	EN_L2_PWR_ SAVE	RW	Enable L2 power savings 0 = Power savings not enabled when in L2 1 = Power savings enabled when in L2
6	BAR1_EN	RW	BAR 1 enable 0 = BAR at offset 14h is disabled (default). 1 = BAR at offset 14h is enabled.
5	BAR0_EN	RW	BAR 0 enable 0 = BAR at offset 10h is disabled (default). 1 = BAR at offset 10h is enabled.
4	REQ_RECOVERY	RW	REQ_RECOVERY to LTSSM
3	REQ_RECONFIG	RW	REQ_RECONFIGURE to LTSSM
2	REQ_HOT_RESET	RW	REQ_HOT_RESET to LTSSM
1	REQ_DIS_ SCRAMBLER	RW	REQ_DISABLE_SCRAMBLER to LTSSM
0	REQ_LOOPBACK	RW	REQ_LOOPBACK to LTSSM

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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4.65 Subsystem Access Register

The contents of this read/write register are aliased to the subsystem vendor ID and subsystem ID registers at PCI offsets 84h and 86h. See Table 4-39 for a complete description of the register contents.

PCI register offset: D0h

Register type: Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-39. Subsystem Access Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:16(1)	SubsystemID	RW	Subsystem ID. The value written to this field is aliased to the subsystem ID register at PCI offset 86h (see Section 4.46).
15:0(1)	SubsystemVendorID	RW	Subsystem vendor ID. The value written to this field is aliased to the subsystem vendor ID register at PCI offset 84h (see Section 4.45).

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

4.66 General Control Register

This read/write register controls various functions of the bridge. See Table 4-40 for a complete description of the register contents.

PCI register offset: D4h

Register type: Read only, Read/Write

Default value: 8600 025Fh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	1	0	0	1	0	1	1	1	1	1

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Table 4-40. General Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:30(1)	CFG_RETRY_ CNTR	RW	Configuration retry counter. Configures the amount of time that a configuration request must be retried on the secondary PCI bus before it may be completed with configuration retry status on the PCIe side. 00 = 25 s 01 = 1 ms 10 = 25 ms (default) 11 = 50 ms
29:28(1)	ASPM_CTRL_ DEF_OVRD	RW	Active-state power-management control default override. These bits are used to determine the power up default for bits 1:0 of the link control register in the PCIe capability structure. 00 = Power-on default indicates that the active-state power management is disabled (00b) 01 = (default). 10 = Power-on default indicates that the active-state power management is enabled for 11 = L0s (01b). Power-on default indicates that the active-state power management is enabled for L1s (10b). Power-on default indicates that the active-state power management is enabled for L0s and L1s (11b).
27(2)	LOW_POWER _ EN	RW	Low-power enable. When this bit is set, the half-ampitude, no preemphasis mode for the PCIe TX drivers is enabled. The default for this bit is 0b.
26(1)	PCI_PM_ VERSION_ CTRL	RW	PCI power management version control. This bit controls the value reported in bits 2:0 (PM_VERSION) in the power management capabilities register (offset 52h, see Section 4.33). It also controls the value of bit 3 (NO_SOFT_RESET) in the power management control/status register (offset 54h, see Section 4.34). 0 = Version fields reports 010b and NO_SOFT_RESET reports 0b for Power Management 1.1 compliance. 1 = Version fields reports 011b and NO_SOFT_RESET reports 1b for Power Management 1.2 compliance (default).
25(1)	STRICT_ PRIORITY_EN	RW	Strict priority enable. When this bit is 0, the default LOW_PRIORITY_COUNT will be 001. When this bit is 1, the default LOW_PRIORITY_COUNT will be 000. This default value for this bit is 1. When this bit is set and the LOW_PRIORITY_COUNT is 000, meaning that strict priority VC arbitration is used and the extended virtual channel always receives priority over VC0 at the PCIe port. 0 = Default LOW_PRIORITY_COUNT is 001b. 1 = Default LOW_PRIORITY_COUNT is 000b (default).
24(1)	FORCE_MRM	RW	Force memory read multiple 0 = Memory read multiple transactions are disabled (default). 1 = All upstream memory read transactions initiated on the PCI bus are treated as though they are memory read multiple transactions in which prefetching is supported for the transaction. This bit shall only affect the XIO2213B design when the EN_CACHE_LINE_CHECK bit in the TL control and diagnostic register is set.
23(1)	CPM_EN_ DEF_OVRD	RW	Clock power-management enable default override. This bit is used to determine the power up default for bit 8 of the link control register in the PCIe capability structure. 0 = Power-on default indicates that clock power management is disabled (00b) (default). 1 = Power-on default indicates that clock power management is enabled for L0s and L1 (11b).
22:20(1)	POWER_ OVRD	RW	Power override. This bit field determines how the bridge responds when the slot power limit is less than the amount of power required by the bridge and the devices behind the bridge. This field shall be hardwired to 000b since XIO2213B does not support slot power limit functionality. 000 = Ignore slot power limit (default) 001 = Assert the PWR_OVRD terminal 010 = Disable secondary clocks selected by the clock mask register 011 = Disable secondary clocks selected by the clock mask register and assert the PWR_OVRD terminal 100 = Respond with unsupported request to all transactions except for configuration transactions (type 0 or type 1) and set slot power limit messages 101, 110, 111 = Reserved

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.
(2) These bits are reset only by a global reset ($\overline{\text{GRST}}$) or the internally generated power-on reset.

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Table 4-40. General Control Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
19(1)	READ_ PREFETCH_ DIS	RW	Read prefetch disable. This bit controls the prefetch functionality on PCI memory read transactions. 0 = Prefetch to the next cache line boundary on a burst read (default) 1 = Fetch only a single DWORD on a burst read Note: When this bit is set, the PREFETCH_4X bit in the TL control and diagnostic register shall have no effect on the design. This bit shall only affect the XIO2213B when the EN_CACHE_LINE_CHECK bit in the TL control and diagnostic register is set.
18:16(1)	L0s_LATENCY	RW	L0s maximum exit latency. This field programs the maximum acceptable latency when exiting the L0s state. This sets bits 8:6 (EP_L0S_LAT) in the device capabilities register (offset 94h, see Section 4.50). 000 = Less than 64 ns (default) 001 = 64 ns up to less than 128 ns 010 = 128 ns up to less than 256 ns 011 = 256 ns up to less than 512 ns 100 = 512 ns up to less than 1 s 101 = 1 s up to less than 2 s 110 = 2 s to 4 s 111 = More than 4 s
15:13(3)	L1_LATENCY	RW	L1 maximum exit latency. This field programs the maximum acceptable latency when exiting the L1 state. This sets bits 11:9 (EP_L1_LAT) in the device capabilities register (offset 94h, see Section 4.50). 000 = Less than 1 s (default) 001 = 1 s up to less than 2 s 010 = 2 s up to less than 4 s 011 = 4 s up to less than 8 s 100 = 8 s up to less than 16 s 101 = 6 s up to less than 32 s 110 = 32 s to 64 s 111 = More than 64 s
12(3)	VC_CAP_EN	R	VC capability structure enable. This bit enables the VC capability structure by changing the next offset field of the advanced error reporting capability register at offset 102h. This bit is a read only 0b indicating that the VC capability structure is permanently disabled. 0 = VC capability structure disabled (offset field = 000h) 1 = VC capability structure enabled (offset field = 150h)
11(3)	BPCC_E	RW	Bus power clock control enable. This bit controls whether the secondary bus PCI clocks are stopped when the XIO2213B is placed in the D3 state. It is assumed that if the secondary bus clocks are required to be active that a reference clock continues to be provided on the PCIe interface. 0 = Secondary bus clocks are not stopped in D3 (default). 1 = Secondary bus clocks are stopped on D3.
10(4)	BEACON_ ENABLE	RW	Beacon enable. This bit controls the mechanism for waking up the physical PCIe link when in L2. 0 = $\overline{\text{WAKE}}$ mechanism is used exclusively. Beacon is not used (default). 1 = Beacon and $\overline{\text{WAKE}}$ mechanisms are used.
9:8(3)	MIN_POWER_ SCALE	RW	Minimum power scale. This value is programmed to indicate the scale of bits 7:0 (MIN_POWER_VALUE). 00 = 1.0x 01 = 0.1x 10 = 0.01x (default) 11 = 0.001x
7:0(3)	MIN_POWER_ VALUE	RW	Minimum power value. This value is programmed to indicate the minimum power requirements. This value is multiplied by the minimum power scale field (bits 9:8) to determine the minimum power requirements for the bridge. The default is 5Fh, indicating that XIO2213B requires 0.95 W of power. This field can be reprogrammed through an EEPROM or the system BIOS.

(3) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.
(4) These bits are reset only by a global reset ($\overline{\text{GRST}}$) or the internally generated power-on reset.

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4.67 TI Proprietary Register

This read/write TI proprietary register is located at offset D8h and controls TI proprietary functions. This register must not be changed from the specified default state. This register shall only be reset by $\overline{\text{FRST}}$.

PCI register offset: D8h
Register type: Read only, Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.68 TI Proprietary Register

This read/write TI proprietary register is located at offset D9h and controls TI proprietary functions. This register must not be changed from the specified default state. This register shall only be reset by $\overline{\text{FRST}}$.

PCI register offset: D9h
Register type: Read only, Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.69 TI Proprietary Register

This read-only TI proprietary register is located at offset DAh and controls TI proprietary functions. This register must not be changed from the specified default state. This register shall only be reset by $\overline{\text{FRST}}$.

PCI register offset: DAh
Register type: Read only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

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4.70 Arbiter Control Register

The arbiter control register controls the device's internal arbiter. The arbitration scheme used is a two-tier rotational arbitration. The device is the only secondary bus master that defaults to the higher-priority arbitration tier. See Table 4-41 for a complete description of the register contents.

PCI register offset: DCh

Register type: Read/Write

Default value: 40h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	0	0	0	0	0

Table 4-41. Arbiter Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7(1)	PARK	RW	Bus parking mode. This bit determines where the internal arbiter parks the secondary bus. When this bit is set, the arbiter parks the secondary bus on the bridge. When this bit is cleared, the arbiter parks the bus on the last device mastering the secondary bus. 0 = Park the secondary bus on the last secondary bus master (default) 1 = Park the secondary bus on the bridge
6(1)	BRIDGE_TIER_SEL	RW	Bridge tier select. This bit determines in which tier the bridge is placed in the arbitration scheme. 0 = Lowest-priority tier 1 = Highest-priority tier (default)
5:1(1)	RSVD	RW	Reserved. These bits are reserved and must not be changed from their default value of 00000b.
0(1)	TIER_SEL0	RW	GNT0 tier select. This bit determines in which tier GNT0 is placed in the arbitration scheme. 0 = Lowest-priority tier (default) 1 = Highest-priority tier

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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4.71 Arbiter Request Mask Register

The arbiter request mask register enables and disables support for requests from specific masters on the secondary bus. The arbiter request mask register also controls if a request input is automatically masked on an arbiter time-out. See Table 4-42 for a complete description of the register contents.

PCI register offset: DDh
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4-42. Arbiter Request Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7(1)	ARB_TIMEOUT	RW	Arbiter time-out. This bit enables the arbiter time-out feature. The arbiter time-out is defined as the number of PCI clocks after the PCI bus has gone idle for a device to assert $\overline{\text{FRAME}}$ before the arbiter assumes the device will not respond. 0 = Arbiter time disabled (default) 1 = Arbiter time-out set to 16 PCI clocks
6(1)	AUTO_MASK	RW	Automatic request mask. This bit enables automatic request masking when an arbiter time-out occurs. 0 = Automatic request masking disabled (default) 1 = Automatic request masking enabled
5:1(1)	RSVD	RW	Reserved. These bits are reserved and must not be changed from their default value of 00000b.
0(1)	REQ0_MASK	RW	Request 0 (REQ0) mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 0. 0 = Use 1394a OHCI request (default) 1 = Ignore 1394a OHCI request

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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4.72 Arbiter Time-Out Status Register

The arbiter time-out status register contains the status of each request (request 50) time-out. The time-out status bit for the respective request is set if the device did not assert FRAME after the arbiter time-out value. See Table 4-43 for a complete description of the register contents.

PCI register offset: DEh

Register type: Read/Clear

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4-43. Arbiter Time-Out Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:6	RSVD	R	Reserved. Returns 00b when read.
5	REQ5_TO	RCU	Request 5 time-out status 0 = No time-out 1 = Time-out has occurred.
4	REQ4_TO	RCU	Request 4 time-out status 0 = No time-out 1 = Time-out has occurred.
3	REQ3_TO	RCU	Request 3 time-out status 0 = No time-out 1 = Time-out has occurred.
2	REQ2_TO	RCU	Request 2 time-out status 0 = No time-out 1 = Time-out has occurred.
1	REQ1_TO	RCU	Request 1time-out status 0 = No time-out 1 = Time-out has occurred.
0	REQ0_TO	RCU	Request 0 time-out status 0 = No time-out 1 = Time-out has occurred.

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4.73 TI Proprietary Register

This read/write TI proprietary register is located at offset E0h and controls TI proprietary functions. This register must not be changed from the specified default state. This register shall only be reset by $\overline{\text{FRST}}$.

PCI register offset: E0h
Register type: Read only, Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.74 TI Proprietary Register

This read/write TI proprietary register is located at offset E2h and controls TI proprietary functions. This register must not be changed from the specified default state. This register shall only be reset by $\overline{\text{FRST}}$.

PCI register offset: E2h
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.75 TI Proprietary Register

This read/clear TI proprietary register is located at offset E4h and controls TI proprietary functions. This register must not be changed from the specified default state.

PCI register offset: E4h
Register type: Read/Clear
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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5 PCIe Extended Configuration Space

The programming model of the PCIe extended configuration space is compliant to the PCI Express Base Specification and the PCI Express to PCI/PCI-X Bridge Specification programming models. The PCIe extended configuration map uses the PCIe advanced error reporting capability and PCIe virtual channel (VC) capability headers.

Sticky bits are reset by a global reset ($\overline{\text{GRST}}$) or the internally-generated power-on reset. EEPROM loadable bits are reset by a PCIe reset ($\overline{\text{PERST}}$), $\overline{\text{GRST}}$, or the internally-generated power-on reset. The remaining register bits are reset by a PCIe hot reset, $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 5-1. PCIe Extended Configuration Register Map

REGISTER NAME		OFFSET
Next capability offset/capability version	Advanced error reporting capabilities ID	100h
Uncorrectable error status register(1)		104h
Uncorrectable error mask(1)		108h
Uncorrectable error severity(1)		10Ch
Correctable error status(1)		110h
Correctable error mask(1)		114h
Advanced error capabilities and control(1)		118h
Header log(1)		11Ch
Header log(1)		120h
Header log(1)		124h
Header log(1)		128h
Secondary uncorrectable error status(1)		12Ch
Secondary uncorrectable error mask(1)		130h
Secondary uncorrectable error severity(1)		134h
Secondary error capabilities and control(1)		138h
Secondary header log(1)		13Ch
Secondary header log(1)		140h
Secondary header log(1)		144h
Secondary header log(1)		148h
Reserved		14Ch FFCh

(1) This register shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

5.1 Advanced Error Reporting Capability ID Register

This read-only register identifies the linked list item as the register for PCIe advanced error reporting capabilities. The register returns 0001h when read.

PCIe extended register offset: 100h

Register type: Read only

Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

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5.2 Next Capability Offset/Capability Version Register

This read-only register identifies the next location in the PCIe extended capabilities link list. The upper 12 bits in this register shall be 000h, indicating that the advanced error reporting capability is the last capability in the linked list. The least significant four bits identify the revision of the current capability block as 1h.

PCIe extended register offset: 102h

Register type: Read only

Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

5.3 Uncorrectable Error Status Register

The uncorrectable error status register reports the status of individual errors as they occur on the primary PCIe interface. Software may only clear these bits by writing a 1b to the desired location. See Table 5-2 for a complete description of the register contents.

PCIe extended register offset: 104h

Register type: Read only, Read/Clear

Default value: 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-2. Uncorrectable Error Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	R	Reserved. Returns 000 0000 0000b when read.
20(1)	UR_ERROR	RCU	Unsupported request error. This bit is asserted when an unsupported request is received.
19(1)	ECRC_ERROR	RCU	Extended CRC error. This bit is asserted when an extended CRC error is detected.
18(1)	MAL_TLP	RCU	Malformed TLP. This bit is asserted when a malformed TLP is detected.
17(1)	RX_OVERFLOW	RCU	Receiver overflow. This bit is asserted when the flow control logic detects that the transmitting device has illegally exceeded the number of credits that were issued.
16(1)	UNXP_CPL	RCU	Unexpected completion. This bit is asserted when a completion packet is received that does not correspond to an issued request.
15(1)	CPL_ABORT	RCU	Completed abort. This bit is asserted when the bridge signals a completed abort.
14(1)	CPL_TIMEOUT	RCU	Completion time-out. This bit is asserted when no completion has been received for an issued request before the time-out period.
13(1)	FC_ERROR	RCU	Flow control error. This bit is asserted when a flow control protocol error is detected either during initialization or during normal operation.
12(1)	PSN_TLP	RCU	Poisoned TLP. This bit is asserted when a poisoned TLP is received.
11:5	RSVD	R	Reserved. Returns 000 0000b when read.
4(1)	DLL_ERROR	RCU	Data link protocol error. This bit is asserted if a data link layer protocol error is detected.
3:0	RSVD	R	Reserved. Returns 0h when read.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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5.4 Uncorrectable Error Mask Register

The uncorrectable error mask register controls the reporting of individual errors as they occur. When a mask bit is set to 1b, the corresponding error status bit is not set, PCIe error messages are blocked, the header log is not loaded, and the first error pointer is not updated. See Table 5-3 for a complete description of the register contents.

PCIe extended register offset: 108h

Register type: Read only, Read/Write

Default value: 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-3. Uncorrectable Error Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	R	Reserved. Returns 000 0000 0000b when read.
20(1)	UR_ERROR_MASK	RW	Unsupported request error mask 0 = Error condition is unmasked (default).. 1 = Error condition is masked.
19(1)	ECRC_ERROR_MASK	RW	Extended CRC error mask 0 = Error condition is unmasked (default). 1 = Error condition is masked.
18(1)	MAL_TLP_MASK	RW	Malformed TLP mask 0 = Error condition is unmasked (default). 1 = Error condition is masked.
17(1)	RX_OVERFLOW_MASK	RW	Receiver overflow mask 0 = Error condition is unmasked (default). 1 = Error condition is masked.
16(1)	UNXP_CPL_MASK	RW	Unexpected completion mask 0 = Error condition is unmasked (default). 1 = Error condition is masked.
15(1)	CPL_ABORT_MASK	RW	Completer abort mask 0 = Error condition is unmasked (default). 1 = Error condition is masked.
14(1)	CPL_TIMEOUT_MASK	RW	Completion time-out mask 0 = Error condition is unmasked (default). 1 = Error condition is masked.
13(1)	FC_ERROR_MASK	RW	Flow control error mask 0 = Error condition is unmasked (default). 1 = Error condition is masked.
12(1)	PSN_TLP_MASK	RW	Poisoned TLP mask 0 = Error condition is unmasked (default). 1 = Error condition is masked.
11:5	RSVD	R	Reserved. Returns 000 0000b when read.
4(1)	DLL_ERROR_MASK	RW	Data link protocol error mask 0 = Error condition is unmasked (default). 1 = Error condition is masked.
3:0	RSVD	R	Reserved. Returns 0h when read.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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5.5 Uncorrectable Error Severity Register

The uncorrectable error severity register controls the reporting of individual errors as ERR_FATAL or ERR_NONFATAL. When a bit is set, the corresponding error condition is identified as fatal. When a bit is cleared, the corresponding error condition is identified as nonfatal. See Table 5-4 for a complete description of the register contents.

PCIe extended register offset: 10Ch
Register type: Read only, Read/Write
Default value: 0006 2011h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	1

Table 5-4. Uncorrectable Error Severity Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	R	Reserved. Returns 000 0000 0000b when read.
20(1)	UR_ERROR_SEVRO	RW	Unsupported request error severity 0 = Error condition is signaled using ERR_NONFATAL. 1 = Error condition is signaled using ERR_FATAL.
19(1)	ECRC_ERROR_SEVRR	RW	Extended CRC error severity 0 = Error condition is signaled using ERR_NONFATAL. 1 = Error condition is signaled using ERR_FATAL.
18(1)	MAL_TLP_SEVR	RW	Malformed TLP severity 0 = Error condition is signaled using ERR_NONFATAL. 1 = Error condition is signaled using ERR_FATAL.
17(1)	RX_OVERFLOW_SEVR	RW	Receiver overflow severity 0 = Error condition is signaled using ERR_NONFATAL. 1 = Error condition is signaled using ERR_FATAL.
16(1)	UNXP_CPL_SEVRP	RW	Unexpected completion severity 0 = Error condition is signaled using ERR_NONFATAL. 1 = Error condition is signaled using ERR_FATAL.
15(1)	CPL_ABORT_SEVR	RW	Completed abort severity 0 = Error condition is signaled using ERR_NONFATAL. 1 = Error condition is signaled using ERR_FATAL.
14(1)	CPL_TIMEOUT_SEVR	RW	Completion time-out severity 0 = Error condition is signaled using ERR_NONFATAL. 1 = Error condition is signaled using ERR_FATAL.
13(1)	FC_ERROR_SEVR	RW	Flow control error severity 0 = Error condition is signaled using ERR_NONFATAL. 1 = Error condition is signaled using ERR_FATAL.
12(1)	PSN_TLP_SEVR	RW	Poisoned TLP severity 0 = Error condition is signaled using ERR_NONFATAL. 1 = Error condition is signaled using ERR_FATAL.
11:6	RSVD	R	Reserved. Returns 000 000b when read.
5	RSVD	R	Reserved. Returns 1h when read.
4(1)	DLL_ERROR_SEVR	RW	Data link protocol error severity 0 = Error condition is signaled using ERR_NONFATAL. 1 = Error condition is signaled using ERR_FATAL.
3:1	RSVD	R	Reserved. Returns 000b when read.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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Table 5-4. Uncorrectable Error Severity Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
0	RSVD	R	Reserved. Returns 1h when read.

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5.6 Correctable Error Status Register

The correctable error status register reports the status of individual errors as they occur. Software may only clear these bits by writing a 1b to the desired location. See Table 5-5 for a complete description of the register contents.t

PCIe extended register offset: 110h

Register type: Read only, Read/Clear

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-5. Correctable Error Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000b when read.
13	ANFES	RCU	Advisory nonfatal error status. This bit is asserted when an advisory nonfatal error has been reported.
12 (1)	REPLAY_TMOUT	RCU	Replay timer time-out. This bit is asserted when the replay timer expires for a pending request or completion that has not been acknowledged.
11:9	RSVD	R	Reserved. Returns 000b when read.
8(1)	REPLAY_ROLL	RCU	REPLAY_NUM rollover. This bit is asserted when the replay counter rolls over after a pending request or completion has not been acknowledged.
7(1)	BAD_DLLP	RCU	Bad DLLP error. This bit is asserted when an 8b/10b error was detected by the PHY during the reception of a DLLP.
6(1)	BAD_TLP	RCU	Bad TLP error. This bit is asserted when an 8b/10b error was detected by the PHY during the reception of a TLP.
5:1	RSVD	R	Reserved. Returns 00000b when read.
0(1)	RX_ERROR	RCU	Receiver error. This bit is asserted when an 8b/10b error is detected by the PHY at any time.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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5.7 Correctable Error Mask Register

The correctable error mask register controls the reporting of individual errors as they occur. When a mask bit is set to 1b, the corresponding error status bit is not set, PCIe error messages are blocked, the header log is not loaded, and the first error pointer is not updated. See Table 5-6 for a complete description of the register contents.

PCIe extended register offset: 114h

Register type: Read only, Read/Write

Default value: 0000 2000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-6. Correctable Error Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000b when read.
13	ANFEM	RW	Advisory nonfatal error mask 0 = Error condition is unmasked. 1 = Error condition is masked (default).
12(1)	REPLAY_TMOUT_MASK	RW	Replay timer time-out mask 0 = Error condition is unmasked (default). 1 = Error condition is masked.
11:9	RSVD	R	Reserved. Returns 000b when read.
8(1)	REPLAY_ROLL_MASK	RW	REPLAY_NUM rollover mask 0 = Error condition is unmasked (default). 1 = Error condition is masked.
7(1)	BAD_DLLP_MASK	RW	Bad DLLP error mask 0 = Error condition is unmasked (default). 1 = Error condition is masked.
6(1)	BAD_TLP_MASK	RW	Bad TLP error mask 0 = Error condition is unmasked (default). 1 = Error condition is masked.
5:1	RSVD	R	Reserved. Returns 00000b when read.
0(1)	RX_ERROR_MASK	RW	Receiver error mask 0 = Error condition is unmasked (default). 1 = Error condition is masked.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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5.8 Advanced Error Capabilities and Control Register

The advanced error capabilities and control register allows the system to monitor and control the advanced error reporting capabilities. See Table 5-7 for a complete description of the register contents.

PCIe extended register offset: 118h

Register type: Read only, Read/Write

Default value: 0000 00A0h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Table 5-7. Advanced Error Capabilities and Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:9	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000 0000b when read.
8(1)	ECRC_CHK_EN	RW	Extended CRC check enable 0 = Extended CRC checking is disabled. 1 = Extended CRC checking is enabled.
7	ECRC_CHK_CAPABLE	R	Extended CRC check capable. This read-only bit returns a value of 1b indicating that the bridge is capable of checking extended CRC information.
6(1)	ECRC_GEN_EN	RW	Extended CRC generation enable 0 = Extended CRC generation is disabled. 1 = Extended CRC generation is enabled.
5	ECRC_GEN_CAPABLE	R	Extended CRC generation capable. This read-only bit returns a value of 1b indicating that the bridge is capable of generating extended CRC information.
4:0(1)	FIRST_ERR	RU	First error pointer. This 5-bit value reflects the bit position within the uncorrectable error status register (offset 104h, see Section 5.3) corresponding to the class of the first error condition that was detected.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

5.9 Header Log Register

The header log register stores the TLP header for the packet that lead to the most recently detected error condition. Offset 11Ch contains the first DWORD. Offset 128h contains the last DWORD (in the case of a 4DW TLP header). Each DWORD is stored with the least significant byte representing the earliest transmitted. This register shall only be reset by a fundamental reset ($\overline{\text{FRST}}$).

PCIe extended register offset: 11Ch, 120h, 124h, and 128h

Register type: Read only

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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5.10 Secondary Uncorrectable Error Status Register

The secondary uncorrectable error status register reports the status of individual PCI bus errors as they occur. Software may only clear these bits by writing a 1b to the desired location. See Table 5-8 for a complete description of the register contents.

PCIe extended register offset: 12Ch

Register type: Read only, Read/Clear

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-8. Secondary Uncorrectable Error Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:13	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000b when read.
12(1)	SERR_DETECT	RCU	SERR assertion detected. This bit is asserted when the bridge detects the assertion of SERR on the secondary bus.
11(1)	PERR_DETECT	RCU	PERR assertion detected. This bit is asserted when the bridge detects the assertion of PERR on the secondary bus.
10(1)	DISCARD_TIMER	RCU	Delayed transaction discard timer expired. This bit is asserted when the discard timer expires for a pending delayed transaction that was initiated on the secondary bus.
9(1)	UNCOR_ADDR	RCU	Uncorrectable address error. This bit is asserted when the bridge detects a parity error during the address phase of an upstream transaction.
8	RSVD	R	Reserved. Returns 0b when read.
7(1)	UNCOR_DATA	RCU	Uncorrectable data error. This bit is asserted when the bridge detects a parity error during a data phase of an upstream write transaction, or when the bridge detects the assertion of PERR when forwarding read completion data to a PCI device.
6:4	RSVD	R	Reserved. Returns 000b when read.
3(1)	MASTER_ABORT	RCU	Received master abort. This bit is asserted when the bridge receives a master abort on the PCI interface.
2(1)	TARGET_ABORT	RCU	Received target abort. This bit is asserted when the bridge receives a target abort on the PCI interface.
1:0	RSVD	R	Reserved. Returns 00b when read.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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5.11 Secondary Uncorrectable Error Mask Register

The secondary uncorrectable error mask register controls the reporting of individual errors as they occur. When a mask bit is set to 1b, the corresponding error status bit is not set, PCIe error messages are blocked, the header log is not loaded, and the first error pointer is not updated. See Table 5-9 for a complete description of the register contents.

PCIe extended register offset: 130h

Register type: Read only, Read/Write

Default value: 0000 17A8h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	1	1	1	1	0	1	0	1	0	0	0

Table 5-9. Secondary Uncorrectable Error Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	R	Reserved. Returns 00 0000 0000 0000 0000b when read.
13(1)	BRIDGE_ERROR_MASK	RW	Internal bridge error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
12(1)	SERR_DETECT_MASK	RW	$\overline{\text{SERR}}$ assertion detected 0 = Error condition is unmasked. 1 = Error condition is masked (default).
11(1)	PERR_DETECT_MASK	RW	$\overline{\text{PERR}}$ assertion detectedi 0 = Error condition is unmasked. 1 = Error condition is masked (default).
10(1)	DISCARD_TIMER_MASK	RW	Delayed transaction discard timer expired 0 = Error condition is unmasked. 1 = Error condition is masked (default).
9(1)	UNCOR_ADDR_MASK	RW	Uncorrectable address error 0 = Error condition is unmasked. 1 = Error condition is masked (default).
8(1)	ATTR_ERROR_MASK	RW	Uncorrectable attribute error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
7(1)	UNCOR_DATA_MASK	RW	Uncorrectable data error 0 = Error condition is unmasked. 1 = Error condition is masked (default).
6(1)	SC_MSG_DATA_MASK	RW	Uncorrectable split completion message data error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
5(1)	SC_ERROR_MASK	RW	Unexpected split completion error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
4	RSVD	R	Reserved. Returns 0b when read.
3(1)	MASTER_ABORT_MASK	RW	Received master abort 0 = Error condition is unmasked. 1 = Error condition is masked (default).
2(1)	TARGET_ABORT_MASK	RW	Received target abort 0 = Error condition is unmasked. 1 = Error condition is masked (default).
1(1)	SC_MSTR_ABORT_MASK	RW	Master abort on split completion. This mask bit is associated with a PCI-X error and has no effect on the bridge.
0	RSVD	R	Reserved. Returns 0b when read.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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5.12 Secondary Uncorrectable Error Severity

The uncorrectable error severity register controls the reporting of individual errors as ERR_FATAL or ERR_NONFATAL. When a bit is set, the corresponding error condition is identified as fatal. When a bit is cleared, the corresponding error condition is identified as nonfatal. See Table 5-10 for a complete description of the register contents.

PCIe extended register offset: 134h

Register type: Read only, Read/Write

Default value: 0000 1340h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0

Table 5-10. Secondary Uncorrectable Error Severity Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	R	Reserved. Returns 00 0000 0000 0000 0000b when read.
13(1)	BRIDGE_ERROR_SEVR	RW	Internal bridge error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
12(1)	SERR_DETECT_SEVR	RW	$\overline{\text{SERR}}$ assertion detected 0 = Error condition is signaled using ERR_NONFATAL. 1 = Error condition is signaled using ERR_FATAL (default).
11(1)	PERR_DETECT_SEVR	RW	$\overline{\text{PERR}}$ assertion detected 0 = Error condition is signaled using ERR_NONFATAL (default). 1 = Error condition is signaled using ERR_FATAL.
10(1)	DISCARD_TIMER_SEVR	RW	Delayed transaction discard timer expired 0 = Error condition is signaled using ERR_NONFATAL (default). 1 = Error condition is signaled using ERR_FATAL.
9(1)	UNCOR_ADDR_SEVR	RW	Uncorrectable address error 0 = Error condition is signaled using ERR_NONFATAL. 1 = Error condition is signaled using ERR_FATAL (default).
8(1)	ATTR_ERROR_SEVR	RW	Uncorrectable attribute error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
7(1)	UNCOR_DATA_SEVR	RW	Uncorrectable data error 0 = Error condition is signaled using ERR_NONFATAL (default). 1 = Error condition is signaled using ERR_FATAL.
6(1)	SC_MSG_DATA_SEVR	RW	Uncorrectable split completion message data error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
5(1)	SC_ERROR_SEVR	RW	Unexpected split completion error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
4	RSVD	R	Reserved. Returns 0b when read.
3(1)	MASTER_ABORT_SEVR	RW	Received master abort 0 = Error condition is signaled using ERR_NONFATAL (default). 1 = Error condition is signaled using ERR_FATAL.
2(1)	TARGET_ABORT_SEVR	RW	Received target abort 0 = Error condition is signaled using ERR_NONFATAL (default). 1 = Error condition is signaled using ERR_FATAL.
1(1)	SC_MSTR_ABORT_SEVR	RW	Master abort on split completion. This severity bit is associated with a PCI-X error and has no effect on the bridge.
0	RSVD	R	Reserved. Returns 0b when read.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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5.13 Secondary Error Capabilities and Control Register

The secondary error capabilities and control register allows the system to monitor and control the secondary advanced error reporting capabilities. See Table 5-11 for a complete description of the register contents.

PCIe extended register offset: 138h
Register type: Read only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-11. Secondary Error Capabilities and Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:5	RSVD	R	Reserved. Return 000 0000 0000 0000 0000 0000 0000b when read.
4:0(1)	SEC_FIRST_ERR	RU	First error pointer. This 5-bit value reflects the bit position within the secondary uncorrectable error status register (offset12Ch, see Section 5.10) corresponding to the class of the first error condition that was detected.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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5.14 Secondary Header Log Register

The secondary header log register stores the transaction address and command for the PCI bus cycle that led to the most recently detected error condition. Offset 13Ch accesses register bits 31:0. Offset 140h accesses register bits 63:32. Offset 144h accesses register bits 95:64. Offset 148h accesses register bits 127:96. See Table 5-12 for a complete description of the register contents.

PCIe extended register offset: 13Ch, 140h, 144h, and 148h

Register type: Read only

Default value: 0000 0000h

BIT NUMBER	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-12. Secondary Header Log Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
127:64(1)	ADDRESS	RU	Transaction address. The 64-bit value transferred on AD[31:0] during the first and second address phases. The first address phase is logged to 95:64 and the second address phase is logged to 127:96. In the case of a 32-bit address, bits 127:96 are set to 0.
63:44	RSVD	R	Reserved. Returns 0 0000h when read.
43:40(1)	UPPER_CMD	RU	Transaction command upper. Contains the status of the C/BE terminals during the second address phase of the PCI transaction that generated the error if using a dual-address cycle.
39:36(1)	LOWER_CMD	RU	Transaction command lower. Contains the status of the C/BE terminals during the first address phase of the PCI transaction that generated the error.
35:0	TRANS_ATTRIBUTE	R	Transaction attribute. Because the bridge does not support the PCI-X attribute transaction phase, these bits have no function, and return 0 0000 0000h when read.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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6 Memory-Mapped TI Proprietary Register Space

The programming model of the memory-mapped TI proprietary register space is unique to this device. These custom registers are specifically designed to provide enhanced features associated with upstream isochronous applications.

Sticky bits are reset by a fundamental reset ($\overline{\text{FRST}}$).

Table 6-1. Device Control Memory Window Register Map

REGISTER NAME				OFFSET
Reserved		Revision ID	Device control map ID	00h
Reserved				04h-3Ch
GPIO data(1)		GPIO control(1)		40h
Serial-bus control and status(1)	Serial-bus slave address(1)	Serial-bus word address(1)	Serial-bus data(1)	44h

(1) This register shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

6.1 Device Control Map ID Register

The device control map ID register identifies the TI proprietary layout for this device control map. The value 04h identifies this as a PCIe-to-PCI bridge without isochronous capabilities.

Device control memory window register offset: 00h

Register type: Read only

Default value: 04h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	0	0

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6.2 Revision ID Register

Device control memory window register offset: 01h

Register type: Read only

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

6.3 GPIO Control Register

This register controls the direction of the eight GPIO terminals. This register has no effect on the behavior of GPIO terminals that are enabled to perform secondary functions. The secondary functions share GPIO4 (SCL) and GPIO5 (SDA). This register is an alias of the GPIO control register in the classic PCI configuration space (offset B4h, see Section 4.60). See Table 6-2 for a complete description of the register contents.

Device control memory window register offset: 40h

Register type: Read only, Read/Write

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-2. GPIO Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Returns 00h when read.
7(1)	GPIO7_DIR	RW	GPIO 7 data direction. This bit selects whether GPIO7 is in input or output mode. 0 = Input (default) 1 = Output
6(1)	GPIO6_DIR	RW	GPIO 6 data direction. This bit selects whether GPIO6 is in input or output mode. 0 = Input (default) 1 = Output
5(1)	GPIO5_DIR	RW	GPIO 5 data direction. This bit selects whether GPIO5 is in input or output mode. 0 = Input (default) 1 = Output
4(1)	GPIO4_DIR	RW	GPIO 4 data direction. This bit selects whether GPIO4 is in input or output mode. 0 = Input (default) 1 = Output
3(1)	GPIO3_DIR	RW	GPIO 3 data direction. This bit selects whether GPIO3 is in input or output mode. 0 = Input (default) 1 = Output
2(1)	GPIO2_DIR	RW	GPIO 2 data direction. This bit selects whether GPIO2 is in input or output mode. 0 = Input (default) 1 = Output
1(1)	GPIO1_DIR	RW	GPIO 1 data direction. This bit selects whether GPIO1 is in input or output mode. 0 = Input (default) 1 = Output
0(1)	GPIO0_DIR	RW	GPIO 0 data direction. This bit selects whether GPIO0 is in input or output mode. 0 = Input (default) 1 = Output

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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6.4 GPIO Data Register

This register reads the state of the input-mode GPIO terminals and changes the state of the output-mode GPIO terminals. Writing to a bit that is in input mode or is enabled for a secondary function is ignored. The secondary functions share GPIO4 (SCL) and GPIO5 (SDA). The default value at power up depends on the state of the GPIO terminals as they default to general-purpose inputs. This register is an alias of the GPIO data register in the classic PCI configuration space (offset B6h, see Section 4.61). See Table 6-3 for a complete description of the register contents.

Device control memory window register offset: 42h

Register type: Read only, Read/Write

Default value: 00XXh

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Table 6-3. GPIO Data Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved
7(1)	GPIO7_Data	RW	GPIO 7 data. This bit reads the state of GPIO7 when in input mode or changes the state of GPIO7 when in output mode.
6(1)	GPIO6_Data	RW	GPIO 6 data. This bit reads the state of GPIO6 when in input mode or changes the state of GPIO6 when in output mode.
5(1)	GPIO5_Data	RW	GPIO 5 data. This bit reads the state of GPIO5 when in input mode or changes the state of GPIO5 when in output mode.
4(1)	GPIO4_Data	RW	GPIO 4 data. This bit reads the state of GPIO4 when in input mode or changes the state of GPIO4 when in output mode.
3(1)	GPIO3_Data	RW	GPIO 3 data. This bit reads the state of GPIO3 when in input mode or changes the state of GPIO3 when in output mode.
2(1)	GPIO2_Data	RW	GPIO 2 data. This bit reads the state of GPIO2 when in input mode or changes the state of GPIO2 when in output mode.
1(1)	GPIO1_Data	RW	GPIO 1 data. This bit reads the state of GPIO1 when in input mode or changes the state of GPIO1 when in output mode.
0(1)	GPIO0_Data	RW	GPIO 0 data. This bit reads the state of GPIO0 when in input mode or changes the state of GPIO0 when in output mode.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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6.5 Serial-Bus Data Register

The serial-bus data register is used to read and write data on the serial-bus interface. When writing data to the serial bus, this register must be written before writing to the serial-bus address register to initiate the cycle. When reading data from the serial bus, this register will contain the data read after the REQBUSY (bit 5 serial-bus control register) bit is cleared. This register is an alias for the serial-bus data register in the PCI header. This register shall only be reset by $\overline{\text{FRST}}$.

Device control memory window register offset: 44h

Register type: Read/Write

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

6.6 Serial-Bus Word Address Register

The value written to the serial-bus index register represents the byte address of the byte being read or written from the serial-bus device. The serial-bus index register must be written before the before initiating a serial bus cycle by writing to the serial-bus slave address register. This register is an alias for the serial-bus index register in the PCI header. This register shall only be reset by $\overline{\text{FRST}}$.

Device control memory window register offset: 45h

Register type: Read/Write

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

6.7 Serial-Bus Slave Address Register

The serial-bus slave address register is used to indicate the address of the device being targeted by the serial-bus cycle. This register also indicates if the cycle will be a read or a write cycle. Writing to this register initiates the cycle on the serial interface. This register is an alias for the serial-bus slave address register in the PCI header.

Device control memory window register offset: 46h

Register type: Read/Write

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 6-4. Serial-Bus Slave Address Register Descriptions

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1 (1)	SLAVE_ADDR	RW	Serial-bus slave address. This 7-bit field is the slave address for a serial-bus read or write transaction. The default value for this field is 000 0000b.
0 (1)	RW_CMD	RW	Read/write command. This bit determines if the serial-bus cycle is a read or a write cycle. 0 = A single-byte write is requested (default) . 1 = A single-byte read is requested.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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6.8 Serial-Bus Control and Status Register

The serial-bus control and status register is used to control the behavior of the serial-bus interface. This register also provides status information about the state of the serial bus. This register is an alias for the serial-bus control and status register in the PCI header.

Device control memory window register offset: 47h

Register type: Read only, Read/Write, Read/Clear

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 6-5. Serial-Bus Control and Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7(1)	PROT_SEL	RW	Protocol select. This bit selects the serial-bus address mode used. 0 = Slave address and word address are sent on the serial bus (default). 1 = Only the slave address is sent on the serial bus.
6	RSVD	R	Reserved. Returns 0b when read.
5	REQBUSY	RU	Requested serial-bus access busy. This bit is set when a software-initiated serial-bus cycle is in progress. 0 = No serial-bus cycle 1 = Serial-bus cycle in progresss
4(1)	ROMBUSY	RU	Serial EEPROM access busy. This bit is set when the serial EEPROM circuitry in the bridge is downloading register defaults from a serial EEPROM. 0 = No EEPROM activity 1 = EEPROM download in progress
3(1)	SBDETECT	RWU	Serial EEPROM detected. This bit enables the serial-bus interface. The value of this bit controls whether the GPIO4/SCL and GPIO5/SDA terminals are configured as GPIO signals or as serial-bus signals. This bit is automatically set to 1b when a serial EEPROM is detected. Note: A serial EEPROM is only detected once following $\overline{\text{PERST}}$. 0 = No EEPROM present, EEPROM load process does not happen. GPIO4//SCL and GPIO5//SDA terminals are configured as GPIO signals. 1 = EEPROM present, EEPROM load process takes place. GPIO4/SCL and GPIO5/SDA terminals are configured as serial-bus signals.
2(1)	SBTEST	RW	Serial-bus test. This bit is used for internal test purposes. This bit controls the clock source for the serial interface clock. 0 = Serial-bus clock at normal operating frequency ~60 kHz (default) 1 = Serial-bus clock frequency increased for test purposes ~4 MHz
1(1)	SB_ERR	RCU	Serial-bus error. This bit is set when an error occurs during a software-initiated serial-bus cycle. 0 = No error 1 = Serial-bus error
0(1)	ROM_ERR	RCU	Serial EEPROM load error. This bit is set when an error occurs while downloading registers from a serial EEPROM. 0 = No error 1 = EEPROM load error

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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7 1394 OHCI PCI Configuration Space

The 1394 OHCI core is integrated as a PCI device behind the PCIe to PCI bridge. The configuration header for the 1394b OHCI portion of the design is compliant with the PCI specification as a standard header. Table 7-1 shows the configuration header that includes both the predefined portion of the configuration space and the user-definable registers.

Since the 1394 OHCI configuration space is accessed over the bridge secondary PCI bus, PCIe type 1 configuration read and write transactions are required when accessing these registers. The 1394 OHCI configuration register map is accessed as device number 0 and function number 0. Of course, the bus number is determined by the value that is loaded into the secondary bus number field at offset 19h within the PCIe configuration register map.

Sticky bits are reset by a fundamental reset ($\overline{\text{FRST}}$). The remaining register bits are reset by a PCIe hot reset, $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 7-1. 1394 OHCI Configuration Register Map

REGISTER NAME				OFFSET
Device ID		Vendor ID		00h
Status		Command		04h
Class code		Revision ID		08h
BIST	Header type	Latency timer	Cache line size	0Ch
OHCI base address				10h
TI extension base address				14h
CIS base address				18h
Reserved				1Ch-27h
CIS pointer				28h
Subsystem ID(1)		Subsystem vendor ID(1)		2Ch
Reserved				30h
Reserved			Power management capabilities pointer	34h
Reserved				38h
Maximum latency(1)	Minimum grant(1)	Interrupt pin	Interrupt line	3Ch
OHCI control				40h
Power management capabilities		Next item pointer	Capability ID	44h
Power management data (reserved)	PMCSR_BSE	Power management control and status(1)		48h
Reserved				4Ch-E7h
Multifunction select				E8h
PCI PHY control(1)				ECh
PCI miscellaneous configuration(1)				F0h
Link enhancement control(1)				F4h
Subsystem access(1)				F8h
TI proprietary				FCh

(1) This register shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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7.1 Vendor ID Register

The vendor ID register contains a value allocated by the PCI SIG and identifies the manufacturer of the OHCI controller. The vendor ID assigned to TI is 104Ch.

PCI register offset: 00h
Register type: Read only
Default value: 104Ch

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0

7.2 Device ID Register

The device ID register contains a value assigned to the 1394 OHCI function by TI. The device identification for the 1394 OHCI function is 823Fh.

PCI register offset: 02h
Register type: Read only
Default value: 823Fh

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1

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7.3 Command Register

The command register provides control over the 1394b OHCI function interface to the PCI bus. All bit functions adhere to the definitions in the PCI Local Bus Specification, as shown in the following bit descriptions. See Table 7-2 for a complete description of the register contents.

PCI register offset: 04h

Register type: Read/Write, Read only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7-2. Command Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15-11	RSVD	R	Reserved. Return 0 0000b when read.
10	INT_DISABLE	R	Interrupt disable. When bit 10 is set to 1b, the OHCI controller is disabled from asserting an interrupt. When cleared, the OHCI controller is able to send interrupts normally. This default value for this bit is 0b.
9	FBB_ENB	R	Fast back-to-back enable. The 1394b OHCI controller does not generate fast back-to-back transactions; therefore, bit 9 returns 0b when read.
8	SERR_ENB	RW	PCI_SERR enable. When bit 8 is set to 1b, the 1394b OHCI controller PCI_SERR driver is enabled. PCI_SERR can be asserted after detecting an address parity error on the PCI bus. The default value for this bit is 0b.
7	STEP_ENB	R	Address/data stepping control. The 1394b OHCI controller does not support address/data stepping; therefore, bit 7 is hardwired to 0b.
6	PERR_ENB	RW	Parity error enable. When bit 6 is set to 1b, the 1394b OHCI controller is enabled to drive PCI_PERR response to parity errors through the PCI_PERR signal. The default value for this bit is 0b.
5	VGA_ENB	R	VGA palette snoop enable. The 1394b OHCI controller does not feature VGA palette snooping; therefore, bit 5 returns 0b when read.
4	MWI_ENB	RW	Memory write and invalidate enable. When bit 4 is set to 1b, the OHCI controller is enabled to generate MWI PCI bus commands. If this bit is cleared, the 1394b OHCI controller generates memory write commands instead. The default value for this bit is 0b.
3	SPECIAL	R	Special cycle enable. The 1394b OHCI controller function does not respond to special cycle transactions; therefore, bit 3 returns 0b when read.
2	MASTER_ENB	RW	Bus master enable. When bit 2 is set to 1b, the 1394b OHCI controller is enabled to initiate cycles on the PCI bus. The default value for this bit is 0b.
1	MEMORY_ENB	RW	Memory response enable. Setting bit 1 to 1b enables the 1394b OHCI controller to respond to memory cycles on the PCI bus. This bit must be set to access OHCI registers. The default value for this bit is 0b.
0	IO_ENB	R	I/O space enable. The 1394b OHCI controller does not implement any I/O-mapped functionality; therefore, bit 0 returns 0b when read.

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7.4 Status Register

The status register provides status over the 1394b OHCI controller interface to the PCI bus. All bit functions adhere to the definitions in the PCI Local Bus Specification, as shown in the following bit descriptions. See Table 7-3 for a complete description of the register contents.

PCI register offset: 06h

Register type: Read/Clear/Update, Read only

Default value: 0230h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0

Table 7-3. Status Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15	PAR_ERR	RCU	Detected parity error. Bit 15 is set to 1b when either an address parity or data parity error is detected.
14	SYS_ERR	RCU	Signaled system error. Bit 14 is set to 1b when PCI_SERR is enabled and the 1394b OHCI controller has signaled a system error to the host.
13	MABORT	RCU	Received master abort. Bit 13 is set to 1b when a cycle initiated by the 1394b OHCI controller on the PCI bus has been terminated by a master abort.
12	TABORT_REC	RCU	Received target abort. Bit 12 is set to 1b when a cycle initiated by the 1394b OHCI controller on the PCI bus was terminated by a target abort.
11	TABORT_SIG	RCU	Signaled target abort. Bit 11 is set to 1b by the 1394b OHCI controller when it terminates a transaction on the PCI bus with a target abort.
10-9	PCI_SPEEDO	R	DEVSEL timing. Bits 10 and 9 encode the timing of PCI_DEVSEL and are hardwired to 01b, indicating that the 1394b OHCI controller asserts this signal at a medium speed on nonconfiguration cycle accesses.
8	DATAPAR	RCU	Data parity error detected. Bit 8 is set to 1b when the following conditions have been met: a. PCI_PERR was asserted by any PCI device including the OHCI controller. b. 1394b OHCI controller was the bus master during the data parity error. c. Bit 6 (PERR_EN) in the command register at offset 04h in the PCI configuration space (see Section 7.3, Command Register) is set to 1b.
7	FBB_CAP	R	Fast back-to-back capable. The 1394b OHCI controller cannot accept fast back-to-back transactions; therefore, bit 7 is hardwired to 0b.
6	UDF	R	User-definable features (UDFs) supported. The 1394b OHCI controller does not support the UDF; therefore, bit 6 is hardwired to 0b.
5	66MHZ	R	66-MHz capable. The 1394b OHCI controller operates at a maximum PCI_CLK frequency of 66 MHz; therefore, bit 5 is hardwired to 1b.
4	CAPLIST	R	Capabilities list. Bit 4 returns 1b when read, indicating that capabilities additional to standard PCI are implemented. The linked list of PCI power-management capabilities is implemented in this function.
3	INT_STATUS	RU	Interrupt status. This bit reflects the interrupt status of the function. Only when bit 10 (INT_DISABLE) in the command register (PCI offset 04h, see Section 4.3) is a 0 and this bit is a 1, is the functions INTx signal asserted. Setting the INT_DISABLE bit to a 1 has no effect on the state of this bit. This bit has been defined as part of the PCI Local Bus Specification (Revision 2.3).
2-0	RSVD	R	Reserved. Bits 3-0 return 0h when read.

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7.5 Class Code and Revision ID Registers

The class code and revision ID registers categorize the 1394b OHCI controller as a serial bus controller (0Ch), controlling an IEEE Std 1394 bus (00h), with an OHCI programming model (10h). Furthermore, the TI chip revision is indicated in the least significant byte. See Table 7-4 for a complete description of the register contents.

PCI register offset: 08h

Register type: Read only

Default value: 0C00 1001h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1

Table 7-4. Class Code and Revision ID Registers Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31-24	BASECLASS	R	Base class. This field returns 0Ch when read, which broadly classifies the function as a serial bus controller.
23-16	SUBCLASS	R	Subclass. This field returns 00h when read, which specifically classifies the function as controlling an IEEE Std 1394 serial bus.
15-8	PGMIF	R	Programming interface. This field returns 10h when read, which indicates that the programming model is compliant with the 1394 Open Host Controller Interface Specification.
7-0	CHIPREV	R	Silicon revision. This field returns 00h when read, which indicates the silicon revision of the 1394b OHCI controller.

7.6 Cache Line Size and Latency Timer Registers

The latency timer and class cache line size registers are programmed by the host BIOS to indicate system cache-line size and the latency timer are associated with the 1394b OHCI controller. See Table 7-5 for a complete description of the register contents.

PCI register offset: 0Ch

Register type: Read/Write

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7-5. Latency Timer and Class Cache Line Size Registers Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15-8	LATENCY_TIMER	RW	PCI latency timer. The value in this register specifies the latency timer for the 1394b OHCI controller, in units of PCI clock cycles. When the 1394b OHCI function is a PCI bus initiator and asserts PCI_FRAME, the latency timer begins counting from zero. If the latency timer expires before the 1394b OHCI functions transaction has terminated, the 1394b OHCI function terminates the transaction when its PCI_GNT is deasserted.
7-0	CACHELINE_SZ	RW	Cache-line size. This value is used by the OHCI controller during memory write and invalidate, memory-read line, and memory-read multiple transactions. The default value for this field is 00h.

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7.7 Header Type and BIST Registers

The header type and built-in self-test (BIST) registers indicate the OHCI controller PCI header type and no built-in self-test. See Table 7-6 for a complete description of the register contents.

PCI register offset: 0Eh
Register type: Read only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7-6. Header Type and BIST Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15-8	BIST	R	Built-in self-test. The OHCI controller does not include a BIST; therefore, this field returns 00h when read.
7-0	HEADER_TYPE	R	PCI header type. The OHCI controller includes the standard PCI header, which is communicated by returning 00h when this field is read. Since the 1394b OHCI core is implemented as a single-function PCI device, bit 7 of this register must be 0b.

7.8 OHCI Base Address Register

The OHCI base address register is programmed with a base address referencing the memory-mapped OHCI control. When the BIOS writes all 1s to this register, the value read back is FFFF F800h, indicating that at least 2K bytes of memory address space are required for the OHCI registers. See Table 7-7 for a complete description of the register contents.

PCI register offset: 10h
Register type: Read/Write, Read only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7-7. OHCI Base Address Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-11	OHCIREG_PTR	RW	OHCI register pointer. This field specifies the upper 21 bits of the 32-bit OHCI base address register. The default value for this field is all 0s.
10-4	OHCI_SZ	R	OHCI register size. This field returns 000 0000b when read, indicating that the OHCI registers require a 2K-byte region of memory.
3	OHCI_PF	R	OHCI register prefetch. Bit 3 returns 0b when read, indicating that the OHCI registers are nonprefetchable.
2-1	OHCI_MEMTYPE	R	OHCI memory type. This field returns 00b when read, indicating that the OHCI base address register is 32 bits wide and mapping can be done anywhere in the 32-bit memory space.
0	OHCI_MEM	R	OHCI memory indicator. Bit 0 returns 0b when read, indicating that the OHCI registers are mapped into system memory space.

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7.9 TI Extension Base Address Register

The TI extension base address register is programmed with a base address referencing the memory-mapped TI extension registers. When the BIOS writes all 1s to this register, the value read back is FFFF C000h, indicating that at least 16K bytes of memory address space are required for the TI registers. See Table 7-8 for a complete description of the register contents.

PCI register offset: 14h

Register type: Read/Write, Read only

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7-8. TI Base Address Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-14	TIREG_PTR	RW	TI register pointer. This field specifies the upper 18 bits of the 32-bit TI base address register. The default value for this field is all 0s.
13-4	TI_SZ	R	TI register size. This field returns 00 0000 0000b when read, indicating that the TI registers require a 16K-byte region of memory.
3	TI_PF	R	TI register prefetch. Bit 3 returns 0b when read, indicating that the TI registers are nonprefetchable.
2-1	TI_MEMTYPE	R	TI memory type. This field returns 00b when read, indicating that the TI base address register is 32 bits wide and mapping can be done anywhere in the 32-bit memory space.
0	TI_MEM	R	TI memory indicator. Bit 0 returns 0b when read, indicating that the TI registers are mapped into system memory space.

7.10 CIS Base Address Register

The $\overline{\text{CARDBUS}}$ input to the 1394 OHCI core is tied high such that this register returns 0000 0000h when read.

PCI register offset: 18h

Register type: Read only

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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7.11 CIS Pointer Register

The $\overline{\text{CARDBUS}}$ input to the 1394 OHCI core is tied high such that this register returns 0000 0000h when read.

PCI register offset: 28h
Register type: Read only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.12 Subsystem Vendor ID and Subsystem ID Registers

The subsystem vendor ID and subsystem ID registers are used for system and option card identification purposes. These registers can be initialized from the serial EEPROM or programmed via the subsystem access register at offset F8h in the PCI configuration space (see Section 7.23). See Table 7-9 for a complete description of the register contents.

PCI register offset: 2Ch
Register type: Read/Update
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7-9. Subsystem Vendor ID and Subsystem ID Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-16(1)	OHCI_SSID	RU	Subsystem device ID. This field indicates the subsystem device ID.
15-0(1)	OHCI_SSVID	RU	Subsystem vendor ID. This field indicates the subsystem vendor ID.

(1) These bits are reset by $\overline{\text{PERST}}$ or $\overline{\text{FRST}}$.

7.13 Power Management Capabilities Pointer Register

The power management capabilities pointer register provides a pointer into the PCI configuration header where the power-management register block resides. The OHCI controller configuration header double words at offsets 44h and 48h provide the power-management registers. This register is read only and returns 44h when read.

PCI register offset: 34h

Register type: Read only

Default value: 44h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	0	0	1	0	0

7.14 Interrupt Line and Interrupt Pin Registers

The interrupt line and interrupt pin registers communicate interrupt line routing information. See Table 7-10 for a complete description of the register contents.

PCI register offset: 3Ch

Register type: Read/Write

Default value: 01FFh

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Table 7-10. Interrupt Line and Interrupt Pin Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15-8	INTR_PIN	R	Interrupt pin. This field returns 01h when read, indicating that the 1394 OHCI core signals interrupts on the INTA terminal.
7-0	INTR_LINE	RW	Interrupt line. This field is programmed by the system and indicates to software which interrupt line the OHCI controller INTA is connected to. The default value for this field is all FFh, indicating that an interrupt line has not yet been assigned to the function.

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7.15 Minimum Grant and Minimum Latency Registers

The minimum grant and minimum latency registers communicate to the system the desired setting of bits 15–8 in the latency timer and class cache line size register at offset 0Ch in the PCI configuration space (see Section 7.6). If a serial EEPROM is detected, the contents of these registers are loaded through the serial EEPROM interface. If no serial EEPROM is detected, these registers return a default value that corresponds to the MAX_LAT = 4, MIN_GNT = 2. See Table 7-11 for a complete description of the register contents.

PCI register offset: 3Eh
Register type: Read/Update
Default value: 0402h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

Table 7-11. Minimum Grant and Minimum Latency Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15-8(1)	MAX_LAT	RU	Maximum latency. The contents of this field may be used by the host BIOS to assign an arbitration priority level to the OHCI controller. The default for this register indicates that the OHCI controller may access the PCI bus as often as every 0.25 s; thus, an extremely high priority level is requested. Bits 11-8 of this field may also be loaded through the serial EEPROM.
7-0(1)	MIN_GNT	RU	Minimum grant. The contents of this field may be used by the host BIOS to assign a latency timer register value to the OHCI controller. The default for this register indicates that the OHCI controller may sustain burst transfers for nearly 64 s and, thus, request a large value be programmed in bits 15-8 of the OHCI controller latency timer and class cache line size register at offset 0Ch in the PCI configuration space (see Section 7.6). Bits 3-0 of this field may also be loaded through the serial EEPROM.

(1) These bits are reset by $\overline{\text{PERST}}$ or $\overline{\text{FRST}}$.

7.16 OHCI Control Register

The PCI OHCI control register is defined by the 1394 Open Host Controller Interface Specification and provides a bit for big endian PCI support. See Table 7-12 for a complete description of the register contents.

PCI register offset: 40h
Register type: Read/Write, Read only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7-12. OHCI Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-1	RSVD	R	Reserved. Bits 31-1 return 000 0000 0000 0000 0000 0000 0000 0000b when read.
0	GLOBAL_SWAP	RW	When bit 0 is set to 1b, all quadlets read from and written to the PCI interface are byte swapped (big endian). The default value for this bit is 0b, which is little endian mode.

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7.17 Capability ID and Next Item Pointer Registers

The capability ID and next item pointer registers identify the linked-list capability item and provide a pointer to the next capability item. See Table 7-13 for a complete description of the register contents.

PCI register offset: 44h

Register type: Read only

Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 7-13. Capability ID and Next Item Pointer Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15-8	NEXT_ITEM	R	Next item pointer. The OHCI controller supports only one additional capability that is communicated to the system through the extended capabilities list; therefore, this field returns 00h when read.
7-0	CAPABILITY_ID	R	Capability identification. This field returns 01h when read, which is the unique ID assigned by the PCI SIG for PCI power-management capability.

7.18 Power Management Capabilities Register

The power management capabilities register indicates the capabilities of the OHCI core related to PCI power management. See Table 7-14 for a complete description of the register contents.

PCI register offset: 46h

Register type: Read only

Default value: 7E03h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1

Table 7-14. Power Management Capabilities Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15-11	PME_SUPPORT	R	$\overline{\text{PME}}$ support. This 5-bit field indicates the power states from which the OHCI core may assert $\overline{\text{PME}}$. This field returns a value of 01111b, indicating that $\overline{\text{PME}}$ is asserted from the D3hot, D2, D1, and D0 power states.
10	D2_SUPPORT	R	D2 support. Bit 10 is hardwired to 1b, indicating that the OHCI controller supports the D2 power state.
9	D1_SUPPORT	R	D1 support. Bit 9 is hardwired to 1b, indicating that the OHCI controller supports the D1 power state.
8-6	AUX_CURRENT	R	Auxiliary current. This 3-bit field reports the 3.3-V_{AUX} auxiliary current requirements. This field returns 000b, because the 1394a core is not powered by V_{AUX}.
5	DSI	R	Device-specific initialization. This bit returns 0b when read, indicating that the OHCI controller does not require special initialization beyond the standard PCI configuration header before a generic class driver is able to use it.
4	RSVD	R	Reserved. Bit 4 returns 0b when read.
3	PME_CLK	R	$\overline{\text{PME}}$ clock. This bit returns 0b when read, indicating that no host bus clock is required for the OHCI controller to generate $\overline{\text{PME}}$.
2-0	PM_VERSION	R	Power-management version. If bit 7 (PCI_PM_VERSION_CTRL) in the PCI miscellaneous configuration register at offset F0h (see Section 7.21) is 0b, this field returns 010b indicating Revision 1.1 compatibility. If PCI_PM_VERSION_CTRL in the PCI miscellaneous configuration register is 1b, this field returns 011b indicating Revision 1.2 compatibility.

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7.19 Power Management Control and Status Register

The power management control and status register implements the control and status of the PCI power-management function. This register is not affected by the internally-generated reset caused by the transition from the D3hot to D0 state. See Table 7-15 for a complete description of the register contents.

PCI register offset: 48h
Register type: Read/Write, Read only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7-15. Power Management Control and Status Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15	PME_STS	R	PME status. This bit returns 0b, because PME is not supported.
14-13	DATA_SCALE	R	This field returns 00b, because the data register is not implemented.
12-9	DATA_SELECT	R	This field returns 0h, because the data register is not implemented.
8	PME_ENB	R	This bit returns 0b, because PME is not supported.
7-2	RSVD	R	Reserved. Bits 7-2 return 00 0000b when read.
1-0(1)	PWR_STATE	RW	Power state. This 2-bit field sets the 1394b OHCI controller power state and is encoded as: 00 = Current power state is D0 (default). 01 = Current power state is D1. 10 = Current power state is D2. 11 = Current power state is D3.

(1) These bits are reset on the rising edge of $\overline{\text{PRST}}$.

7.20 Power Management Extension Registers

The power management extension registers provide extended power-management features not applicable to the OHCI controller; thus, they are read only and returns 0000h when read. See Table 7-16 for a complete description of the register contents.

PCI register offset: 4Ah
Register type: Read only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7-16. Power Management Extension Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15-0	RSVD	R	Reserved. Bits 15-0 return 0000h when read.

7.21 PCI Miscellaneous Configuration Register

The PCI miscellaneous configuration register provides miscellaneous PCI-related configuration. See Table 7-17 for a complete description of the register contents.

PCI register offset: F0h
Register type: Read/Write, Read only
Default value: 0000 0A90h

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BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7(1)	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	1	0	1	0	1	0	0	1	0	0	0	0

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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Table 7-17. PCI Miscellaneous Configuration Register

BIT	FIELD NAME	TYPE	DESCRIPTION
31-16	RSVD	R	Reserved. Bits 31-16 return 0000h when read.
15	PME_D3COLD	R	PME support from D3cold. The 1394a OHCI core does not support PME generation from D3cold. Therefore, this bit is tied to 0b.
14-12	RSVD	R	Reserved. Bits 14-12 return 000b when read.
11	PCI2_3_EN	R	PCI 2.3 enable. The 1394 OHCI core always conforms to the PCI 2.3 specification; therefore, this bit is tied to 1b.
10	10 IGNORE_ MSTRINT_ ENA_FOR_PME	RW	IGNORE_MSTRINT_ENA_FOR_PME bit for $\overline{\text{PME}}$ generation. When set, this bit causes bit 26 of the OHCI vendor ID register (OHCI offset 40h, see Section 8.15) to read 1b. Otherwise, bit 26 reads 0b. 0 = $\overline{\text{PME}}$ behavior generated from unmasked interrupt bits and IntMask.masterIntEnable bit (default) 1 = $\overline{\text{PME}}$ generation does not depend on the value of IntMask.masterIntEnable.
9-8(1)	MR_ENHANCE	RW	This field selects the read command behavior of the PCI master for read transactions of greater than two data phases. For read transactions of one or two data phases, a memory read command is used. 00 = Memory read line 01 = Memory read 10 = Memory read multiple (default) 11 = Reserved, behavior reverts to default
7(1)	PCI_PM_ VERSION_CTRL	RW	PCI power-management version control. This bit controls the value reported in the Version field of the power management capabilities register of the 1394 OHCI function. 0 = Version fields report 010b for Power Management 1.1 compliance. 1 = Version fields report 011b for Power Management 1.2 compliance (default).
6-5	RSVD	R	Reserved. Bits 6-5 return 00b when read.
4(1)	DIS_TGT_ABT	RW	Disable target abort. Bit 4 controls the no-target-abort mode, in which the OHCI controller returns indeterminate data instead of signaling target abort. The OHCI LLC is divided into the PCLK and SCLK domains. If software tries to access registers in the link that are not active because the SCLK is disabled, a target abort is issued by the link. On some systems, this can cause a problem resulting in a fatal system error. Enabling this bit allows the link to respond to these types of requests by returning FFh. 0 = Responds with OHCI-Lynx compatible target abort. 1 = Responds with indeterminate data equal to FFh. It is recommended that this bit be set to 1b (default).
3(1)	SB_EN	RW	Serial bus enable. In the bridge, the serial bus interface is controlled using the bridge configuration registers. Therefore, this bit has no effect in the 1394b OHCI function. The default value for this bit is 0b.
2(1)	DISABLE_ SCLKGATE	RW	Disable SCLK test feature. This bit controls locking or unlocking the SCLK to the 1394a OHCI core PCI bus clock input. This is a test feature only and must be cleared to 0b (all applications). 0 = Hardware decides auto-gating of the PHY clock (default). 1 = Disables auto-gating of the PHY clock
1(1)	DISABLE_ PCIGATE	RW	Disable PCLK test feature. This bit controls locking or unlocking the PCI clock to the 1394a OHCI core PCI bus clock input. This is a test feature only and must be cleared to 0b (all applications). 0 = Hardware decides auto-gating of the PCI clock (default). 1 = Disables auto-gating of the PCI clock
0(1)	KEEP_PCLK	RW	Keep PCI clock running. This bit controls the PCI clock operation during the CLKRUN protocol. Since the CLKRUN protocol is not supported in the XIO2200, this bit has no effect. The default value for this bit is 0b.

(1) These bits are reset by $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

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7.22 Link Enhancement Control Register

The link enhancement control register implements TI proprietary bits that are initialized by software or by a serial EEPROM, if present. After these bits are set to 1b, their functionality is enabled only if bit 22 (aPhyEnhanceEnable) in the host controller control register at OHCI offset 50h/54h (see Section 3.3.2, Host Controller Control Register) is set to 1. See Table 7-18 for a complete description of the register contents.

PCI register offset: F4h

Register type: Read/Write, Read only

Default value: 0000 4000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 7-18. Link Enhancement Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-16	RSVD	R	Reserved. Bits 31-16 return 0000h when read.
15(1)	dis_at_pipeline	RW	Disable AT pipelining. When bit 15 is set to 1b, out-of-order AT pipelining is disabled. The default value for this bit is 0b.
14(1)	ENAB_DRAFT	RW	Enable OHCI 1.2 draft features. When this bit is set, it enables some features beyond the OHCI 1.1 specification. Specifically, this enables HCControl.LPS to be cleared by writing a 1 to the HCControlClear.LPS bit and enables the link to set bit 9 in the xfer status field of AR and IR context control registers. This bit can be initialized from an attached EEPROM.
13-12(1)	atx_thresh	RW	This field sets the initial AT threshold value, which is used until the AT FIFO is underrun. When the OHCI controller retries the packet, it uses a 4K-byte threshold, resulting in a store-and-forward operation. 00 = Threshold ~4K bytes resulting in a store-and-forward operation (default) 01 = Threshold ~1.7K bytes 10 = Threshold ~1K bytes 11 = Threshold ~512 bytes These bits fine tune the asynchronous transmit threshold. For most applications, the 1.7K-byte threshold is optimal. Changing this value may increase or decrease the 1394 latency depending on the average PCI bus latency. Setting the AT threshold to 1.7K, 1K, or 512 bytes results in data being transmitted at these thresholds or when an entire packet has been checked into the FIFO. If the packet to be transmitted is larger than the AT threshold, the remaining data must be received before the AT FIFO is emptied; otherwise, an underrun condition occurs, resulting in a packet error at the receiving node. As a result, the link then commences store-and-forward operation. Wait until it has the complete packet in the FIFO before retransmitting it on the second attempt to ensure delivery. An AT threshold of 4K results in store-and-forward operation, which means that asynchronous data is not transmitted until an end-of-packet token is received. Restated, setting the AT threshold to 4K results in only complete packets being transmitted. Note that the OHCI controller will always use store-and-forward when the asynchronous transmit retries register at OHCI offset 08h (see Section 8.3, Asynchronous Transmit Retries Register) is cleared.
11	RSVD	R	Reserved. Bit 11 returns 0b when read.
10(1)	enab_mpeg_ts	RW	Enable MPEG CIP timestamp enhancement. When bit 9 is set to 1b, the enhancement is enabled for MPEG CIP transmit streams (FMT = 20h). The default value for this bit is 0b.
9	RSVD	R	Reserved. Bit 9 returns 0b when read.
8(1)	enab_dv_ts	RW	Enable DV CIP timestamp enhancement. When bit 8 is set to 1b, the enhancement is enabled for DV CIP transmit streams (FMT = 00h). The default value for this bit is 0b.
7(1)	enab_unfair	RW	Enable asynchronous priority requests (OHCI-Lynx compatible). Setting bit 7 to 1b enables the link to respond to requests with priority arbitration. It is recommended that this bit be set to 1b. The default value for this bit is 0b.
6-3	RSVD	R	Reserved. Bits 6-3 return 0h when read.
2(1)	RSVD	RW	Reserved. Bit 2 defaults to 0b and must remain 0b for normal operation of the OHCI core.
1(1)	enab_accel	RW	Enable acceleration enhancements (OHCI-Lynx compatible). When bit 1 is set to 1b, the PHY is notified that the link supports the IEEE Std 1394a-2000 acceleration enhancements, that is, ack-accelerated, fly-by concatenation, etc. It is recommended that this bit be set to 1b. The default value for this bit is 0b.
0(1)	RSVD	R	Reserved. Bit 0 returns 0b when read.

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7.23 Subsystem Access Register

Write access to the subsystem access register identically updates the subsystem ID registers to OHCI-Lynx. The system ID value written to this register may also be read back from this register. See Table 7-19 for a complete description of the register contents.

PCI register offset: F8h

Register type: Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7-19. Subsystem Access Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-16(1)	SUBDEV_ID	RW	Subsystem device ID alias. This field indicates the subsystem device ID.
15-0(1)	SUBVEN_ID	RW	Subsystem vendor ID alias. This field indicates the subsystem vendor ID.

(1) These bits shall only be reset by a fundamental reset ($\overline{\text{FRST}}$). $\overline{\text{FRST}}$ is asserted (low) whenever $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is asserted.

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8 1394 OHCI Memory-Mapped Register Space

The OHCI registers defined by the 1394 Open Host Controller Interface Specification are memory mapped into a 2K-byte region of memory pointed to by the OHCI base address register at offset 10h in PCI configuration space (see Section 7.8). These registers are the primary interface for controlling the IEEE Std 1394 link function.

This section provides the register interface and bit descriptions. Several set/clear register pairs in this programming model are implemented to solve various issues with typical read-modify-write control registers. There are two addresses for a set/clear register — RegisterSet and RegisterClear (see Table 8-1 for register listing). A 1 bit written to RegisterSet causes the corresponding bit in the set/clear register to be set to 1b; a 0 bit leaves the corresponding bit unaffected. A 1 bit written to RegisterClear causes the corresponding bit in the set/clear register to be cleared; a 0 bit leaves the corresponding bit in the set/clear register unaffected.

Typically, a read from either RegisterSet or RegisterClear returns the contents of the set or clear register, respectively. However, sometimes reading the RegisterClear provides a masked version of the set or clear register. The interrupt event register is an example of this behavior.

Table 8-1. OHCI Register Map

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
	OHCI version	Version	00h
	GUID ROM	GUID_ROM	04h
	Asynchronous transmit retries	ATRetries	08h
	CSR data	CSRData	0Ch
	CSR compare	CSRCompareData	10h
	CSR control	CSRControl	14h
	Configuration ROM header	ConfigROMhdr	18h
	Bus identification	BusID	1Ch
	Bus options(1)	BusOptions	20h
	GUID high(1)	GUIDHi	24h
	GUID low(1)	GUIDLo	28h
	Reserved(1)		2Ch-30h
	Configuration ROM mapping	ConfigROMmap	34h
	Posted write address low	PostedWriteAddressLo	38h
	Posted write address high	PostedWriteAddressHi	3Ch
	Vendor ID	VendorID	40h
	Reserved		44h-4Ch
	Host controller control (1)	HCControlSet	50h
		HCControlClr	54h
	Reserved		58h-5Ch
Self-ID	Reserved		60h
	Self-ID buffer pointer	SelfIDBuffer	64h
	Self-ID count	SelfIDCount	68h
	Reserved		6Ch
	Isochronous receive channel mask high	IRChannelMaskHiSet	70h
		IRChannelMaskHiClear	74h
	Isochronous receive channel mask low	IRChannelMaskLoSet	78h
		IRChannelMaskLoClear	7Ch

(1) One or more bits in this register are reset by $\overline{\text{PERST}}$ or $\overline{\text{FRST}}$.

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Table 8-1. OHCI Register Map (continued)

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
	Interrupt event	IntEventSet	80h
		IntEventClear	84h
	Interrupt mask	IntMaskSet	88h
		IntMaskClear	8Ch
	Isochronous transmit interrupt event	IsoXmitIntEventSet	90h
		IsoXmitIntEventClear	94h
	Isochronous transmit interrupt mask	IsoXmitIntMaskSet	98h
		IsoXmitIntMaskClear	9Ch
	Isochronous receive interrupt event	IsoRecvIntEventSet	A0h
		IsoRecvIntEventClear	A4h
	Isochronous receive interrupt mask	IsoRecvIntMaskSet	A8h
		IsoRecvIntMaskClear	ACh
	Initial bandwidth available	InitialBandwidthAvailable	B0h
	Initial channels available high	InitialChannelsAvailableHi	B4h
	Initial channels available low	InitialChannelsAvailableLo	B8h
	Reserved		BCh-D8h
	Fairness control	FairnessControl	DCh
	Link control (1)	LinkControlSet	E0h
		LinkControlClear	E4h
	Node identification	NodeID	E8h
	PHY control	PhyControl	ECh
	Isochronous cycle timer	Isocyctimer	F0h
	Reserved		F4h-FCh
	Asynchronous request filter high	AsyncRequestFilterHiSet	100h
		AsyncRequestFilterHiClear	104h
	Asynchronous request filter low	AsyncRequestFilterLoSet	108h
		AsyncRequestFilterLoClear	10Ch
	Physical request filter high	PhysicalRequestFilterHiSet	110h
		PhysicalRequestFilterHiClear	114h
	Physical request filter low	PhysicalRequestFilterLoSet	118h
		PhysicalRequestFilterLoClear	11Ch
	Physical upper bound	PhysicalUpperBound	120h
	Reserved		124h-17Ch
Asynchronous Request Transmit (ATRQ)	Asynchronous context control	ContextControlSet	180h
		ContextControlClear	184h
	Reserved		188h
	Asynchronous context command pointer	CommandPtr	18Ch
	Reserved		190h-19Ch
Asynchronous Response Transmit (ATRS)	Asynchronous context control	ContextControlSet	1A0h
		ContextControlClear	1A4h
	Reserved		1A8h
	Asynchronous context command pointer	CommandPtr	1ACh
	Reserved		1B0h-1BCh

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Table 8-1. OHCI Register Map (continued)

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
Asynchronous Request Receive (ARRQ)	Asynchronous context control	ContextControlSet	1C0h
		ContextControlClear	1C4h
	Reserved		1C8h
	Asynchronous context command pointer	CommandPtr	1CCh
	Reserved		1D0h-1DCh
Asynchronous Response Receive (ARRS)	Asynchronous context control	ContextControlSet	1E0h
		ContextControlClear	1E4h
	Reserved		1E8h
	Asynchronous context command pointer	CommandPtr	1ECh
	Reserved		1F0h-1FCh
Isochronous Transmit Context n n = 0, 1, 2, 3, ..., 7	Isochronous transmit context control	ContextControlSet	200h + 16*n
		ContextControlClear	204h + 16*n
	Reserved		208h + 16*n
	Isochronous transmit context command pointer	CommandPtr	20Ch + 16*n
	Reserved		210h-3FCh
Isochronous Receive Context n n = 0, 1, 2, 3	Isochronous receive context control	ContextControlSet	400h + 32*n
		ContextControlClear	404h + 32*n
	Reserved		408h + 32*n
	Isochronous receive context command pointer	CommandPtr	40Ch + 32*n
	Isochronous receive context match	ContextMatch	410h + 32*n

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8.1 OHCI Version Register

The OHCI version register indicates the OHCI version support and whether or not the serial EEPROM is present. See Table 8-2 for a complete description of the register contents.

OHCI register offset: 00h

Register type: Read only

Default value: 0X01 0010h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	X	0	0	0	0	0	0	0	1

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Table 8-2. OHCI Version Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-25	RSVD	R	Reserved. Bits 31-25 return 000 0000b when read.
24(1)	GUID_ROM	RU	The controller sets bit 24 to 1b if the serial EEPROM is detected. If the serial EEPROM is present, the Bus_Info_Block is automatically loaded on system (hardware) reset. The default value for this bit is 0b.
23-16	version	R	Major version of the OHCI. The controller is compliant with the 1394 Open Host Controller Interface Specification, Release 1.2; thus, this field reads 01h.
15-8	RSVD	R	Reserved. Bits 15-8 return 00h when read.
7-0	revision	R	Minor version of the OHCI. The controller is compliant with the 1394 Open Host Controller Interface Specification, Release 1.2; thus, this field reads 10h.

(1) One or more bits in this register are reset by $\overline{\text{PERST}}$ or $\overline{\text{FRST}}$.

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8.2 GUID ROM Register

The GUID ROM register accesses the serial EEPROM, and is only applicable if bit 24 (GUID_ROM) in the OHCI version register at OHCI offset 00h (see Section 8.1) is set to 1b. See Table 8-3 for a complete description of the register contents.

OHCI register offset: 04h

Register type: Read/Set/Update, Read/Update, Read only

Default value: 00XX 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8-3. GUID ROM Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	addrReset	RSU	Software sets bit 31 to 1b to reset the GUID ROM address to 0. When the controller completes the reset, it clears this bit. The controller does not automatically fill bits 23-16 (rdData field) with the 0 byte.
30-26	RSVD	R	Reserved. Bits 30-26 return 00 0000b when read.
25	rdStart	RSU	A read of the currently addressed byte is started when bit 25 is set to 1b. This bit is automatically cleared when the controller completes the read of the currently addressed GUID ROM byte.
24	RSVD	R	Reserved. Bit 24 returns 0b when read.
23-16	rdData	RU	This field contains the data read from the GUID ROM.
15-8	RSVD	R	Reserved. Bits 15-8 return 00h when read.
7-0	miniROM	R	The miniROM field defaults to 00h indicating that no miniROM is implemented. If an EEPROM is implemented, all eight bits of this miniROM field are downloaded from EEPROM word offset 28h. For this device, the miniROM field must be greater than 39h to indicate a valid miniROM offset into the EEPROM.

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8.3 Asynchronous Transmit Retries Register

The asynchronous transmit retries register indicates the number of times the controller attempts a retry for asynchronous DMA request transmit and for asynchronous physical and DMA response transmit. See Table 8-4 for a complete description of the register contents.

OHCI register offset: 08h

Register type: Read/Write, Read only

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8-4. Asynchronous Transmit Retries Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-29	secondLimit	R	The second limit field returns 000b when read, because outbound dual-phase retry is not implemented.
28-16	cycleLimit	R	The cycle limit field returns 0 0000 0000 0000b when read, because outbound dual-phase retry is not implemented.
15-12	RSVD	R	Reserved. Bits 15-12 return 0h when read.
11-8	maxPhysRespRetries	RW	This field tells the physical response unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node. The default value for this field is 0h.
7-4	maxATRespRetries	RW	This field tells the asynchronous transmit response unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node. The default value for this field is 0h.
3-0	maxATReqRetries	RW	This field tells the asynchronous transmit DMA request unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node. The default value for this field is 0h.

8.4 CSR Data Register

The CSR data register accesses the bus-management CSR registers from the host through compare-swap operations. This register contains the data to be stored in a CSR if the compare is successful.

OHCI register offset: 0Ch

Register type: Read only

Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

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8.5 CSR Compare Register

The CSR compare register accesses the bus-management CSR registers from the host through compare-swap operations. This register contains the data to be compared with the existing value of the CSR resource.

OHCI register offset: 10h
Register type: Read only
Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

8.6 CSR Control Register

The CSR control register accesses the bus-management CSR registers from the host through compare-swap operations. This register controls the compare-swap operation and selects the CSR resource. See Table 8-5 for a complete description of the register contents.

OHCI register offset: 14h
Register type: Read/Write, Read/Update, Read only
Default value: 8000 000Xh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X

Table 8-5. CSR Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	csrDpme	RU	Bit 31 is set to 1b by the controller when a compare-swap operation is complete. It is cleared whenever this register is written.
32-2	RSVD	R	Reserved. Bits 30-2 return 0 0000 0000 0000 0000 0000 0000 0000b when read.
1-0	csrSel	RW	This field selects the CSR resource as follows: 00 = BUS_MANAGER_ID 01 = BANDWIDTH_AVAILABLE 10 = CHANNELS_AVAILABLE_HI 11 = CHANNELS_AVAILABLE_LO

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8.7 Configuration ROM Header Register

The configuration ROM header register externally maps to the first quadlet of the 1394 configuration ROM, offset FFFF F000 0400h. See Table 8-6 for a complete description of the register contents.

OHCI register offset: 18h

Register type: Read/Write

Default value: 0000 XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8-6. Configuration ROM Header Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-24	info_length	RW	Information length. IEEE Std 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 3.3.2) is set to 1b. The default value for this field is 0h.
23-16	crc_length	RW	CRC length. IEEE Std 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 3.3.2) is set to 1b. The default value for this field is 0h.
15-0	rom_crc_value	RW	ROM CRC value. IEEE Std 1394 bus-management field. Must be valid at any time bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 3.3.2) is set to 1b.

8.8 Bus Identification Register

The bus identification register externally maps to the first quadlet in the Bus_Info_Block and contains the constant 3133 3934h, which is the ASCII value of 1394.

OHCI register offset: 1Ch

Register type: Read only

Default value: 3133 3934h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	1	1	0	0	0	1	0	0	1	1	0	0	1	1

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	0

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8.9 Bus Options Register

The bus options register externally maps to the second quadlet of the Bus_Info_Block. See Table 8-7 for a complete description of the register contents.

OHCI register offset: 20h

Register type: Read/Write, Read only

Default value: 0000 B0X3h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	0	1	1	0	0	0	0	X	X	0	0	0	0	1	1

Table 8-7. Bus Options Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	irmc	RW	Isochronous resource-manager capable. IEEE Std 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 3.3.2) is set to 1b. The default value for this bit is 0b.
30	cmc	RW	Cycle master capable. IEEE Std 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 3.3.2) is set to 1b. The default value for this bit is 0b.
29	isc	RW	Isochronous support capable. IEEE Std 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 3.3.2) is set to 1b. The default value for this bit is 0b.
28	bmc	RW	Bus manager capable. IEEE Std 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 3.3.2) is set to 1b. The default value for this bit is 0b.
27	pmc	RW	Power-management capable. IEEE Std 1394 bus-management field. When bit 27 is set to 1b, this indicates that the node is power-management capable. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 3.3.2) is set to 1b. The default value for this bit is 0b.
26-24	RSVD	R	Reserved. Bits 26-24 return 000b when read.
23-16	cyc_clk_acc	RW	Cycle master clock accuracy (in parts per million). IEEE Std 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 3.3.2) is set to 1b. The default value for this field is 00h.
15-12(1)	max_rec	RW	Maximum request. IEEE Std 1394 bus-management field. Hardware initializes this field to indicate the maximum number of bytes in a block request packet that is supported by the implementation. This value, max_rec_bytes, must be 512 or greater, and is calculated by 2^(max_rec + 1). Software may change this field; however, this field must be valid at any time bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 3.3.2) is set to 1b. A received block write request packet with a length greater than max_rec_bytes may generate an ack_type_error. This field is not affected by a software reset, and defaults to value indicating 4096 bytes on a system (hardware) reset. The default value for this field is Bh.
11-8	RSVD	R	Reserved. Bits 11-8 return 0h when read.
7-6	g	RW	Generation counter. This field is incremented if any portion of the configuration ROM has been incremented since the prior bus reset.
5-3	RSVD	R	Reserved. Bits 5-3 return 000b when read.
2-0	Lnk_spd	R	Link speed. This field returns 011b, indicating that the link speeds of 100M bit/s, 200M bit/s, 400M bit/s, and 800M bit/s are supported.

(1) These bits are reset by $\overline{\text{PERST}}$ or $\overline{\text{FRST}}$.

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8.10 GUID High Register

The GUID high register represents the upper quadlet in a 64-bit global unique ID (GUID), which maps to the third quadlet in the Bus_Info_Block. This register contains node_vendor_ID and chip_ID_hi fields. This register initializes to 0000 0000h on a system (hardware) reset, which is an illegal GUID value. If a serial EEPROM is detected, the contents of this register are loaded through the serial EEPROM interface. At that point, the contents of this register cannot be changed. If no serial EEPROM is detected, the contents of this register are loaded by the BIOS. At that point, the contents of this register cannot be changed. This register is reset by a PCIe reset ($\overline{\text{PERST}}$), $\overline{\text{GRST}}$, or the internally-generated power-on reset.

OHCI register offset: 24h

Register type: Read only

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3(1)	2(1)	1(1)	0(1)
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) These bits are reset only by a global reset ($\overline{\text{GRST}}$) or the internally generated power-on reset.

8.11 GUID Low Register

The GUID low register represents the lower quadlet in a 64-bit global unique ID (GUID), which maps to chip_ID_lo in the Bus_Info_Block. This register initializes to 0000 0000h on a system (hardware) reset and behaves identical to the GUID high register at OHCI offset 24h (see Section 8.10). This register is reset by $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

OHCI register offset: 28h

Register type: Read only

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3(1)	2(1)	1(1)	0(1)
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) These bits are reset only by a global reset ($\overline{\text{GRST}}$) or the internally generated power-on reset.

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8.12 Configuration ROM Mapping Register

The configuration ROM mapping register contains the start address within system memory that maps to the start address of 1394 configuration ROM for this node. See Table 8-8 for a complete description of the register contents.

OHCI register offset:: 34h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8-8. Configuration ROM Mapping Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-10	configROMaddr	RW	Configuration ROM address. If a quadlet read request to 1394 offset FFFF F000 0400h through offset FFFF F000 07FFh is received, the low-order ten bits of the offset are added to this register to determine the host memory address of the read request. The default value for this field is all 0s.
9-0	RSVD	R	Reserved. Bits 9-0 return 00 0000 0000b when read.

8.13 Posted Write Address Low Register

The posted write address low register communicates error information if a write request is posted and an error occurs while the posted data packet is being written. See Table 8-9 for a complete description of the register contents.

OHCI register offset: 38h
Register type: Read/Update
Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8-9. Posted Write Address Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-0	offsetLo	RU	Offset low. The lower 32 bits of the 1394 destination offset of the write request that failed.

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8.14 Posted Write Address High Register

The posted write address high register communicates error information if a write request is posted and an error occurs while writing the posted data packet. See Table 8-10 for a complete description of the register contents.

OHCI register offset: 3Ch
Register type: Read/Update
Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8-10. Posted Write Address High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-16	sourceID	RU	Source identification. This field is the 10-bit bus number (bits 31-22) and 6-bit node number (bits 21-16) of the node that issued the write request that failed.
15-0	offsetHi	RU	Offset high. The upper 16 bits of the 1394 destination offset of the write request that failed.

8.15 Vendor ID Register

The vendor ID register holds the company ID of an organization that specifies any vendor-unique registers. The controller implements TI unique behavior with regards to OHCI. Thus, this register is read only and returns 0x08 0028h when read.

OHCI register offset: 40h
Register type: Read only
Default value: 0x08 0028h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	x	x	1	0	0	0	0	1	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0

8.16 Host Controller Control Register

The host controller control set/clear register pair provides flags for controlling the controller. See Table 8-11 for a complete description of the register contents.

OHCI register offset: 50h set register
54h clear register
Register type: Read/Set/Clear/Update, Read/Set/Clear, Read/Clear, Read only
Default value: 0080 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

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BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 8-11. Host Controller Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	BIBimageValid	RSU	When bit 31 is set to 1b, the physical response unit is enabled to respond to block read requests to host configuration ROM and to the mechanism for atomically updating configuration ROM. Software creates a valid image of the bus_info_block in host configuration ROM before setting this bit. When this bit is cleared, the controller returns ack_type_error on block read requests to host configuration ROM. Also, when this bit is cleared and a 1394 bus reset occurs, the configuration ROM mapping register at OHCI offset 34h (see Section 8.12), configuration ROM header register at OHCI offset 18h (see Section 8.7), and bus options register at OHCI offset 20h (see Section 8.9) are not updated. Software can set this bit only when bit 17 (linkEnable) is 0b. Once bit 31 is set to 1b, it can be cleared by a system (hardware) reset, a software reset, or if a fetch error occurs when the controller loads bus_info_block registers from host memory.
30	noByteSwapData	RSC	Bit 30 controls whether physical accesses to locations outside the controller itself, as well as any other DMA data accesses are byte swapped.
29	ack_Tardy_enable	RSC	Bit 29 controls the acknowledgement of ack_tardy. When bit 29 is set to 1b, ack_tardy may be returned as an acknowledgment to accesses from the 1394 bus to the controller, including accesses to the bus_info_block. The controller returns ack_tardy to all other asynchronous packets addressed to the node. When the controller sends ack_tardy, bit 27 (ack_tardy) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) is set to 1b to indicate the attempted asynchronous access. Software ensures that bit 27 (ack_tardy) in the interrupt event register is 0b. Software also unmasks wake-up interrupt events such as bit 19 (phy) and bit 27 (ack_tardy) in the interrupt event register before placing the controller into the D1 power mode. Software must not set this bit if the node is the 1394 bus manager.
28-24	RSVD	R	Reserved. Bits 28-24 return 00000b when read.
23 (1)	programPhyEnable	RC	Bit 23 informs upper-level software that lower-level software has consistently configured the IEEE Std 1394a-2000 enhancements in the link and PHYs. When this bit is 1b, generic software such as the OHCI driver is responsible for configuring IEEE Std 1394a-2000 enhancements in the PHY and bit 22 (aPhyEnhanceEnable). When this bit is 0b, the generic software may not modify the IEEE Std 1394a-2000 enhancements in the PHY and cannot interpret the setting of bit 22 (aPhyEnhanceEnable). This bit is initialized from serial EEPROM.
22	aPhyEnhanceEnable	RSC	When bits 23 (programPhyEnable) and 17 (linkEnable) are 11b, the OHCI driver can set bit 22 to 1b to use all IEEE Std 1394a-2000 enhancements. When bit 23 (programPhyEnable) is cleared to 0b, the software does not change PHY enhancements or this bit.
21-20	RSVD	R	Reserved. Bits 21 and 20 return 00b when read.
19	LPS	RSC	Bit 19 controls the link power status. Software must set this bit to 1b to permit the link-PHY communication. A 0b prevents link-PHY communication. The OHCI link is divided into two clock domains (PCLK and PHY_SCLK). If software tries to access any register in the PHY_SCLK domain while the PHY_SCLK is disabled, a target abort is issued by the link. This problem can be avoided by setting bit 4 (DIS_TGT_ABT) to 1b in the PCI miscellaneous configuration register at offset F0h in the PCI configuration space (see Section 7.21). This allows the link to respond to these types of request by returning all Fs (hex). OHCI registers at offsets DCh-F0h and 100h-11Ch are in the PHY_SCLK domain. After setting LPS, software must wait approximately 10 ms before attempting to access any of the OHCI registers. This gives the PHY_SCLK time to stabilize.
18	postedWriteEnable	RSC	Bit 18 enables (1) or disables (0) posted writes. Software changes this bit only when bit 17 (linkEnable) is 0b.
17	linkEnable	RSC	Bit 17 is cleared to 0b by either a system (hardware) or software reset. Software must set this bit to 1b when the system is ready to begin operation and then force a bus reset. This bit is necessary to keep other nodes from sending transactions before the local system is ready. When this bit is cleared, the controller is logically and immediately disconnected from the 1394 bus, no packets are received or processed, nor are packets transmitted.
16	SoftReset	RSCU	When bit 16 is set to 1b, all states are reset, all FIFOs are flushed, and all OHCI registers are set to their system (hardware) reset values, unless otherwise specified. PCI registers are not affected by this bit. This bit remains set to 1b while the software reset is in progress and reverts back to 0b when the reset has completed.
15-0	RSVD	R	Reserved. Bits 15-0 return 0000h when read.

(1) This bit is reset by $\overline{\text{PERST}}$ or $\overline{\text{FRST}}$.

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8.17 Self-ID Buffer Pointer Register

The self-ID buffer pointer register points to the 2K-byte-aligned base address of the buffer in host memory where the self-ID packets are stored during bus initialization. Bits 31-11 are read/write accessible. Bits 10-0 are reserved and return 000 0000 0000b when read.

OHCI register offset: 64h
Register type: Read/Write, Read only
Default value: XXXX XX00h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0

8.18 Self-ID Count Register

The self-ID count register keeps a count of the number of times the bus self-ID process has occurred, flags self-ID packet errors, and keeps a count of the self-ID data in the self-ID buffer. See Table 8-12 for a complete description of the register contents.

OHCI register offset: 68h
Register type: Read/Update, Read only
Default value: X0XX 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8-12. Self-ID Count Register Description

BIT	FIELD NAME	TYPE	Description
31	selfIDError	RU	Self-ID error. When bit 31 is set to 1b, an error was detected during the most recent self-ID packet reception. The contents of the self-ID buffer are undefined. This bit is cleared after a self-ID reception in which no errors are detected. Note that an error can be a hardware error or a host bus write error.
30-24	RSVD	R	Reserved. Bits 30-24 return 000 0000b when read.
23-16	selfIDGeneration	RU	Self-ID generation. The value in this field increments each time a bus reset is detected. This field rolls over to 0 after reaching 255.
15-11	RSVD	R	Reserved. Bits 15-11 return 00000b when read.
10-2	selfIDSize	RU	Self-ID size. This field indicates the number of quadlets that have been written into the self-ID buffer for the current bits 23-16 (selfIDGeneration field). This includes the header quadlet and the self-ID data. This field is cleared to 0 0000 0000b when the self-ID reception begins.
1-0	RSVD	R	Reserved. Bits 1 and 0 return 00b when read.

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8.19 Isochronous Receive Channel Mask High Register

The isochronous receive channel mask high set/clear register enables packet receives from the upper 32 isochronous data channels. A read from either the set or clear register returns the content of the isochronous receive channel mask high register. See Table 8-13 for a complete description of the register contents.

OHCI register offset: 70h set register
74h clear register

Register type: Read/Set/Clear

Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8-13. Isochronous Receive Channel Mask High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	isoChannel63	RSC	When bit 31 is set to 1b, the controller is enabled to receive from isochronous channel number 63.
30	isoChannel62	RSC	When bit 30 is set to 1b, the controller is enabled to receive from isochronous channel number 62.
29	isoChannel61	RSC	When bit 29 is set to 1b, the controller is enabled to receive from isochronous channel number 61.
28	isoChannel60	RSC	When bit 28 is set to 1b, the controller is enabled to receive from isochronous channel number 60.
27	isoChannel59	RSC	When bit 27 is set to 1b, the controller is enabled to receive from isochronous channel number 59.
26	isoChannel58	RSC	When bit 26 is set to 1b, the controller is enabled to receive from isochronous channel number 58.
25	isoChannel57	RSC	When bit 25 is set to 1b, the controller is enabled to receive from isochronous channel number 57.
24	isoChannel56	RSC	When bit 24 is set to 1b, the controller is enabled to receive from isochronous channel number 56.
23	isoChannel55	RSC	When bit 23 is set to 1b, the controller is enabled to receive from isochronous channel number 55.
22	isoChannel54	RSC	When bit 22 is set to 1b, the controller is enabled to receive from isochronous channel number 54.
21	isoChannel53	RSC	When bit 21 is set to 1b, the controller is enabled to receive from isochronous channel number 53.
20	isoChannel52	RSC	When bit 20 is set to 1b, the controller is enabled to receive from isochronous channel number 52.
19	isoChannel51	RSC	When bit 19 is set to 1b, the controller is enabled to receive from isochronous channel number 51.
18	isoChannel50	RSC	When bit 18 is set to 1b, the controller is enabled to receive from isochronous channel number 50.
17	isoChannel49	RSC	When bit 17 is set to 1b, the controller is enabled to receive from isochronous channel number 49.
16	isoChannel48	RSC	When bit 16 is set to 1b, the controller is enabled to receive from isochronous channel number 48.
15	isoChannel47	RSC	When bit 15 is set to 1b, the controller is enabled to receive from isochronous channel number 47.
14	isoChannel46	RSC	When bit 14 is set to 1b, the controller is enabled to receive from isochronous channel number 46.
13	isoChannel45	RSC	When bit 13 is set to 1b, the controller is enabled to receive from isochronous channel number 45.
12	isoChannel44	RSC	When bit 12 is set to 1b, the controller is enabled to receive from isochronous channel number 44.
11	isoChannel43	RSC	When bit 11 is set to 1b, the controller is enabled to receive from isochronous channel number 43.
10	isoChannel42	RSC	When bit 10 is set to 1b, the controller is enabled to receive from isochronous channel number 42.
9	isoChannel41	RSC	When bit 9 is set to 1b, the controller is enabled to receive from isochronous channel number 41.
8	isoChannel40	RSC	When bit 8 is set to 1b, the controller is enabled to receive from isochronous channel number 40.
7	isoChannel39	RSC	When bit 7 is set to 1b, the controller is enabled to receive from isochronous channel number 39.
6	isoChannel38	RSC	When bit 6 is set to 1b, the controller is enabled to receive from isochronous channel number 38.
5	isoChannel37	RSC	When bit 5 is set to 1b, the controller is enabled to receive from isochronous channel number 37.
4	isoChannel36	RSC	When bit 4 is set to 1b, the controller is enabled to receive from isochronous channel number 36.
3	isoChannel35	RSC	When bit 3 is set to 1b, the controller is enabled to receive from isochronous channel number 35.
2	isoChannel34	RSC	When bit 2 is set to 1b, the controller is enabled to receive from isochronous channel number 34.
1	isoChannel33	RSC	When bit 1 is set to 1b, the controller is enabled to receive from isochronous channel number 33.

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Table 8-13. Isochronous Receive Channel Mask High Register Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
0	isoChannel32	RSC	When bit 0 is set to 1b, the controller is enabled to receive from isochronous channel number 32.

8.20 Isochronous Receive Channel Mask Low Register

The isochronous receive channel mask low set/clear register enables packet receives from the lower 32 isochronous data channels. See Table 8-14 for a complete description of the register contents.

OHCI register offset: 78h set register
7Ch clear register

Register type: Read/Set/Clear

Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8-14. Isochronous Receive Channel Mask Low Register Description

BIT	FIELD NAME	TYPE	Description
31	isoChannel31	RSC	When bit 31 is set to 1b, the controller is enabled to receive from isochronous channel number 31.
30	isoChannel30	RSC	When bit 30 is set to 1b, the controller is enabled to receive from isochronous channel number 30.
29-2	isoChanneln	RSC	Bits 29-2 (isoChanneln, where n = 29, 28, 27, ..., 2) follow the same pattern as bits 31 and 30.
1	isoChannel1	RSC	When bit 1 is set to 1b, the controller is enabled to receive from isochronous channel number 1.
0	isoChannel0	RSC	When bit 0 is set to 1b, the controller is enabled to receive from isochronous channel number 0.

8.21 Interrupt Event Register

The interrupt event set/clear register reflects the state of the various interrupt sources. The interrupt bits are set to 1b by an asserting edge of the corresponding interrupt signal or by writing a 1b in the corresponding bit in the set register. The only mechanism to clear a bit in this register is to write a 1b to the corresponding bit in the clear register.

This register is fully compliant with the 1394 Open Host Controller Interface Specification, and the controller adds a vendor-specific interrupt function to bit 30. When the interrupt event register is read, the return value is the bit-wise AND function of the interrupt event and interrupt mask registers. See Table 8-15 for a complete description of the register contents.

OHCI register offset: 80h set register
84h clear register [returns the content of the interrupt event register bit-wise ANDed with the interrupt mask register when read]

Register type: Read/Set/Clear/Update, Read/Set/Clear, Read/Update, Read only

Default value: XXXX 0XXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	X	0	0	0	X	X	X	X	X	X	X	X	0	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X

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Table 8-15. Interrupt Event Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	RSVD	R	Reserved. Bit 31returns 0b when read.
30	vendorSpecific	RSC	This vendor-specific interrupt event is reported when either of the general-purpose interrupts are asserted. The general-purpose interrupts are enabled by setting the corresponding bits INT_3EN and INT_2EN (bits 31 and 23, respectively) to 1 in the GPIO control register at offset FCh in the PCI configuration space.
29	SoftInterrupt	RSC	Bit 29 is used by software to generate an interrupt for its own use.
28	RSVD	R	Reserved. Bit 28 returns 0b when read.
27	ack_tardy	RSCU	Bit 27 is set to 1b when bit 29 (AckTardyEnable) in the host controller control register at OHCI offset 50h/54h (see Section 3.3.2) is set to 1b and any of the following conditions occur: a. Data is present in a receive FIFO that is to be delivered to the host. b. The physical response unit is busy processing requests or sending responses. c. The controller sent an ack_tardy acknowledgment.
26	phyRegRcvd	RSCU	The controller has received a PHY register data byte that can be read from bits 23-16 in the PHY control register at OHCI offset ECh (see Section 8.33).
25	cycleTooLong	RSCU	If bit 21 (cycleMaster) in the link control register at OHCI offset E0h/E4h (see Section 8.30) is set to 1b, this indicates that over 125 s has elapsed between the start of sending a cycle start packet and the end of a subaction gap. Bit 21 (cycleMaster) in the link control register is cleared by this event.
24	unrecoverableError	RSCU	This event occurs when the controller encounters any error that forces it to stop operations on any or all of its subunits, for example, when a DMA context sets its dead bit to 1b. While bit 24 is set to 1b, all normal interrupts for the context(s) that caused this interrupt are blocked from being set to 1b.
23	cycleInconsistent	RSCU	A cycle start was received that had values for the cycleSeconds and cycleCount fields that are different from the values in bits 31-25 (cycleSeconds field) and bits 24-12 (cycleCount field) in the isochronous cycle timer register at OHCI offset F0h (see Section 8.34).
22	cycleLost	RSCU	A lost cycle is indicated when no cycle_start packet is sent or received between two successive cycleSynch events. A lost cycle can be predicted when a cycle_start packet does not immediately follow the first subaction gap after the cycleSynch event or if an arbitration reset gap is detected after a cycleSynch event without an intervening cycle start. Bit 22 may be set to 1b either when a lost cycle occurs or when logic predicts that one will occur.
21	cycle64Seconds	RSCU	Indicates that the seventh bit of the cycle second counter has changed
20	cycleSynch	RSCU	Indicates that a new isochronous cycle has started. Bit 20 is set to 1b when the low-order bit of the cycle count toggles.
19	phy	RSCU	Indicates that the PHY requests an interrupt through a status transfer
18	regAccessFail	RSCU	Indicates that a register access has failed due to a missing SCLK clock signal from the PHY. When a register access fails, bit 18 is set to 1b before the next register access.
17	busReset	RSCU	Indicates that the PHY has entered bus reset mode
16	selfIDcomplete	RSCU	A self-ID packet stream has been received. It is generated at the end of the bus initialization process. Bit 16 is turned off simultaneously when bit 17 (busReset) is turned on.
15	selfIDcomplete2	RSCU	Secondary indication of the end of a self-ID packet stream. Bit 15 is set to 1b by the controller when it sets bit 16 (selfIDcomplete), and retains the state, independent of bit 17 (busReset).
14-10	RSVD	R	Reserved. Bits 14-10 return 00000b when read.
9	lockRespErr	RSCU	Indicates that the controller sent a lock response for a lock request to a serial bus register, but did not receive an ack_complete
8	postedWriteErr	RSCU	Indicates that a host bus error occurred while the controller was trying to write a 1394 write request, which had already been given an ack_complete, into system memory
7	isochRx	RU	Isochronous receive DMA interrupt. Indicates that one or more isochronous receive contexts have generated an interrupt. This is not a latched event; it is the logical OR of all bits in the isochronous receive interrupt event register at OHCI offset A0h/A4h (see Section 8.25) and isochronous receive interrupt mask register at OHCI offset A8h/ACh (see Section 8.26). The isochronous receive interrupt event register indicates which contexts have been interrupted.
6	isochTx	RU	Isochronous transmit DMA interrupt. Indicates that one or more isochronous transmit contexts have generated an interrupt. This is not a latched event; it is the logical OR of all bits in the isochronous transmit interrupt event register at OHCI offset 90h/94h (see Section 8.23) and isochronous transmit interrupt mask register at OHCI offset 98h/9Ch (see Section 8.24). The isochronous transmit interrupt event register indicates which contexts have been interrupted.

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Table 8-15. Interrupt Event Register Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
5	RSPkt	RSCU	Indicates that a packet was sent to an asynchronous receive response context buffer and the descriptor xferStatus and resCount fields have been updated
4	RQPkt	RSCU	Indicates that a packet was sent to an asynchronous receive request context buffer and the descriptor xferStatus and resCount fields have been updated
3	ARRS	RSCU	Asynchronous receive response DMA interrupt. Bit 3 is conditionally set to 1b upon completion of an ARRS DMA context command descriptor.
2	ARRQ	RSCU	Asynchronous receive request DMA interrupt. Bit 2 is conditionally set to 1b upon completion of an ARRQ DMA context command descriptor.
1	respTxComplete	RSCU	Asynchronous response transmit DMA interrupt. Bit 1 is conditionally set to 1b upon completion of an ATRS DMA command.
0	reqTxCompleter	RSCU	Asynchronous request transmit DMA interrupt. Bit 0 is conditionally set to 1b upon completion of an ATRQ DMA command.

8.22 Interrupt Mask Register

The interrupt mask set/clear register enables the various interrupt sources. Reads from either the set register or the clear register always return the contents of the interrupt mask register. In all cases except masterIntEnable (bit 31) and vendorSpecific (bit 30), the enables for each interrupt event align with the interrupt event register bits detailed in Table 8-15.

This register is fully compliant with the 1394 Open Host Controller Interface Specification, and the controller adds an interrupt function to bit 30. See Table 8-16 for a complete description of bits 31 and 30.

OHCI register offset: 88h set register
8Ch clear register

Register type: Read/Set/Clear/Update, Read/Set/Clear, Read/Update, Read only

Default value: XXXX 0XXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	0	0	0	X	X	X	X	X	X	X	X	0	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X

Table 8-16. Interrupt Mask Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	masterIntEnable	RSCU	Master interrupt enable. If bit 31 is set to 1b, external interrupts are generated in accordance with the interrupt mask register. If this bit is cleared, external interrupts are not generated, regardless of the interrupt mask register settings.
30	VendorSpecific	RSC	When this bit and bit 30 (vendorSpecific) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this vendor-specific interrupt mask enables interrupt generation.
29	SoftInterrupt	RSC	When this bit and bit 29 (SoftInterrupt) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this soft-interrupt mask enables interrupt generation.
28	RSVD	R	Reserved. Bit 28 returns 0b when read.
27	ack_tardy	RSC	When this bit and bit 27 (ack_tardy) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this acknowledge-tardy interrupt mask enables interrupt generation.
26	phyRegRcvd	RSC	When this bit and bit 26 (phyRegRcvd) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this PHY register interrupt mask enables interrupt generation.
25	cycleTooLong	RSC	When this bit and bit 25 (cycleTooLong) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this cycle-too-long interrupt mask enables interrupt generation.

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Table 8-16. Interrupt Mask Register Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
24	unrecoverableError	RSC	When this bit and bit 24 (unrecoverableError) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this unrecoverable-error interrupt mask enables interrupt generation.
23	cycleInconsistent	RSC	When this bit and bit 23 (cycleInconsistent) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this inconsistent-cycle interrupt mask enables interrupt generation.
22	cycleLost	RSC	When this bit and bit 22 (cycleLost) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this lost-cycle interrupt mask enables interrupt generation.
21	cycle64Seconds	RSC	When this bit and bit 21 (cycle64Seconds) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this 64-s cycle interrupt mask enables interrupt generation.
20	cycleSynch	RSC	When this bit and bit 20 (cycleSynch) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this isochronous-cycle interrupt mask enables interrupt generation.
19	phy	RSC	When this bit and bit 19 (phy) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this PHY-status-transfer interrupt mask enables interrupt generation.
18	regAccessFail	RSC	When this bit and bit 18 (regAccessFail) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this register-access-failed interrupt mask enables interrupt generation.
17	busReset	RSC	When this bit and bit 17 (busReset) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this bus-reset interrupt mask enables interrupt generation.
16	selfIDcomplete	RSC	When this bit and bit 16 (selfIDcomplete) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this self-ID-complete interrupt mask enables interrupt generation.
15	selfIDcomplete2	RSC	When this bit and bit 15 (selfIDcomplete2) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this second self-ID-complete interrupt mask enables interrupt generation.
14-10	RSVD	R	Reserved. Bits 14-10 return 00000b when read.
9	lockRespErr	RSC	When this bit and bit 9 (lockRespErr) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this lock-response-error interrupt mask enables interrupt generation.
8	postedWriteErr	RSC	When this bit and bit 8 (postedWriteErr) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this posted-write-error interrupt mask enables interrupt generation.
7	isochRx	RSC	When this bit and bit 7 (isochRx) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this isochronous-receive-DMA interrupt mask enables interrupt generation.
6	isochTx	RSC	When this bit and bit 6 (isochTx) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this isochronous-transmit-DMA interrupt mask enables interrupt generation.
5	RSPkt	RSC	When this bit and bit 5 (RSPkt) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this receive-response-packet interrupt mask enables interrupt generation.
4	RQPkt	RSC	When this bit and bit 4 (RQPkt) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this receive-request-packet interrupt mask enables interrupt generation.
3	ARRS	RSC	When this bit and bit 3 (ARRS) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this asynchronous-receive-response-DMA interrupt mask enables interrupt generation.
2	ARRQ	RSC	When this bit and bit 2 (ARRQ) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this asynchronous-receive-request-DMA interrupt mask enables interrupt generation.
1	respTxComplete	RSC	When this bit and bit 1 (respTxComplete) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this response-transmit-complete interrupt mask enables interrupt generation.
0	reqTxComplete	RSC	When this bit and bit 0 (reqTxComplete) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this request-transmit-complete interrupt mask enables interrupt generation.

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8.23 Isochronous Transmit Interrupt Event Register

The isochronous transmit interrupt event set/clear register reflects the interrupt state of the isochronous transmit contexts. An interrupt is generated on behalf of an isochronous transmit context if an OUTPUT_LAST* command completes and its interrupt bits are set to 1. Upon determining that the isochTx (bit 6) interrupt has occurred in the interrupt event register at OHCI offset 80h/84h (see Section 8.21), software can check this register to determine which context caused the interrupt. The interrupt bits are set to 1 by an asserting edge of the corresponding interrupt signal, or by writing a 1b in the corresponding bit in the set register. The only mechanism to clear a bit in this register is to write a 1b to the corresponding bit in the clear register. See Table 8-17 for a complete description of the register contents.

OHCI register offset:
- 90h set register
- 94h clear register (returns the contents of the isochronous transmit interrupt event register bit-wise ANDed with the isochronous transmit interrupt mask register when read)

Register type: Read/Set/Clear, Read only

Default value: 0000 00XXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

Table 8-17. Isochronous Transmit Interrupt Event Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-8	RSVD	R	Reserved. Bits 31-8 return 0000h when read.
7	isoXmit7	RSC	Isochronous transmit context 7 caused the interrupt event register bit 6 (isochTx) interrupt.
6	isoXmit6	RSC	Isochronous transmit context 6 caused the interrupt event register bit 6 (isochTx) interrupt.
5	isoXmit5	RSC	Isochronous transmit context 5 caused the interrupt event register bit 6 (isochTx) interrupt.
4	isoXmit4	RSC	Isochronous transmit context 4 caused the interrupt event register bit 6 (isochTx) interrupt.
3	isoXmit3	RSC	Isochronous transmit context 3 caused the interrupt event register bit 6 (isochTx) interrupt.
2	isoXmit2	RSC	Isochronous transmit context 2 caused the interrupt event register bit 6 (isochTx) interrupt.
1	isoXmit1	RSC	Isochronous transmit context 1 caused the interrupt event register bit 6 (isochTx) interrupt.
0	isoXmit0	RSC	Isochronous transmit context 0 caused the interrupt event register bit 6 (isochTx) interrupt.

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8.24 Isochronous Transmit Interrupt Mask Register

The isochronous transmit interrupt mask set/clear register enables the isochTx interrupt source on a per-channel basis. Reads from either the set register or the clear register always return the contents of the isochronous transmit interrupt mask register. In all cases, the enables for each interrupt event align with the isochronous transmit interrupt event register bits detailed in Table 8-17.

OHCI register offset: 98h set register
9Ch clear register

Register type: Read/Set/Clear, Read only

Default value: 0000 00XX

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

8.25 Isochronous Receive Interrupt Event Register

The isochronous receive interrupt event set/clear register reflects the interrupt state of the isochronous receive contexts. An interrupt is generated on behalf of an isochronous receive context if an INPUT_* command completes and its interrupt bits are set to 1. Upon determining that the isochRx (bit 7) interrupt in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) has occurred, software can check this register to determine which context(s) caused the interrupt. The interrupt bits are set to 1 by an asserting edge of the corresponding interrupt signal or by writing a 1b in the corresponding bit in the set register. The only mechanism to clear a bit in this register is to write a 1b to the corresponding bit in the clear register. See Table 8-18 for a complete description of the register contents.

OHCI register offset: A0h set register
A4h clear register (returns the contents of isochronous receive interrupt event register bit-wise ANDed with the isochronous receive mask register when read)

Register type: Read/Set/Clear, Read only

Default value: 0000 000Xh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X

Table 8-18. Isochronous Receive Interrupt Event Register Description

BIT	FIELD NAME	TYPE	Description
31-4	RSVD	R	Reserved. Bits 31-4 return 000 0000h when read.
3	isoRecv3	RSC	Isochronous receive channel 3 caused the interrupt event register bit 7 (isochRx) interrupt.
2	isoRecv2	RSC	Isochronous receive channel 2 caused the interrupt event register bit 7 (isochRx) interrupt.
1	isoRecv1	RSC	Isochronous receive channel 1 caused the interrupt event register bit 7 (isochRx) interrupt.
0	isoRecv0	RSC	Isochronous receive channel 0 caused the interrupt event register bit 7 (isochRx) interrupt.

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8.26 Isochronous Receive Interrupt Mask Register

The isochronous receive interrupt mask set/clear register enables the isochRx interrupt source on a per-channel basis. Reads from either the set register or the clear register always return the contents of the isochronous receive interrupt mask register. In all cases, the enables for each interrupt event align with the isochronous receive interrupt event register bits detailed in Table 8-18.

OHCI register offset: A8h set register
ACh clear register

Register type: Read/Set/Clear, Read only

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

8.27 Initial Bandwidth Available Register

The initial bandwidth available register value is loaded into the corresponding bus-management CSR register on a system (hardware) or software reset. See Table 8-19 for a complete description of the register contents.

OHCI register offset: B0h

Register type: Read only, Read/Write

Default value: 0000 1333h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1

Table 8-19. Initial Bandwidth Available Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-13	RSVD	R	Reserved. Bits 31-13 return 000 0000 0000 0000 0000b when read.
12-0	InitBWAvailable	RW	This field is reset to 1333h on a system (hardware) or software reset, and is not affected by a 1394 bus reset. The value of this field is loaded into the BANDWIDTH_AVAILABLE CSR register upon a $\overline{\text{GRST}}$, $\overline{\text{PERST}}$, $\overline{\text{PRST}}$, or 1394 bus reset.

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8.28 Initial Channels Available High Register

The initial channels available high register value is loaded into the corresponding bus-management CSR register on a system (hardware) or software reset. See Table 8-20 for a complete description of the register contents.

OHCI register offset: B4h
Register type: Read/Write
Default value: FFFF FFFFh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 8-20. Initial Channels Available High Register Description

BIT	FIELD NAME	TYPE	Description
31-0	InitChanAvailHi	RW	This field is reset to FFFF_FFFFh on a system (hardware) or software reset, and is not affected by a 1394 bus reset. The value of this field is loaded into the CHANNELS_AVAILABLE_HI CSR register upon a GRST, PERST, PRST, or 1394 bus reset.

8.29 Initial Channels Available Low Register

The initial channels available low register value is loaded into the corresponding bus-management CSR register on a system (hardware) or software reset. See Table 8-21 for complete description of the register contents.

OHCI register offset: B8h
Register type: Read/Write
Default value: FFFF FFFFh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 8-21. Initial Channels Available Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-0	InitChanAvailLo	RW	This field is reset to FFFF_FFFFh on a system (hardware) or software reset, and is not affected by a 1394 bus reset. The value of this field is loaded into the CHANNELS_AVAILABL_LO CSR register upon a GRST, PRST, PRST, or 1394 bus reset.

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8.30 Fairness Control Register

The fairness control register provides a mechanism by which software can direct the host controller to transmit multiple asynchronous requests during a fairness interval. See Table 8-22 for a complete description of the register contents.

OHCI register offset: DCh

Register type: Read only, Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8-22. Fairness Control Registre Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-8	RSVD	R	Reserved. Bits 31-8 return 00 0000h when read.
7-0	pri_req	RW	Priority requests. This field specifies the maximum number of priority arbitration requests for asynchronous request packets that the link is permitted to make of the PHY during a fairness interval. The default value for this field is 00h.

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8.31 Link Control Register

The link control set/clear register provides the control flags that enable and configure the link core protocol portions of the controller. It contains controls for the receiver and cycle timer. See Table 8-23 for a complete description of the register contents.

OHCI register offset: E0h set register
E4h clear register

Register type: Read/Set/Clear/Update, Read/Set/Clear, Read only

Default value: 00X0 0X00h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	X	X	X	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	X	X	0	0	0	0	0	0	0	0	0

Table 8-23. Link Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-23	RSVD	R	Reserved. Bits 31-23 return 0 0000 0000b when read.
22	cycleSource	RSC	When bit 22 is set to 1b, the cycle timer uses an external source (CYCLEIN) to determine when to roll over the cycle timer. When this bit is cleared, the cycle timer rolls over when the timer reaches 3072 cycles of the 24.576-MHz clock (125 s).
21	cycleMaster	RSCU	When bit 21 is set to 1b and the controller is root, it generates a cycle start packet every time the cycle timer rolls over, based on the setting of bit 22 (cycleSource). When the controller is not root, regardless of the setting of bit 21, the controller accepts received cycle start packets to maintain synchronization with the node that is sending them. Bit 21 is automatically cleared when bit 25 (cycleTooLong) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) is set to 1b. Bit 21 cannot be set to 1b until bit 25 (cycleTooLong) is cleared.
20	CycleTimerEnable	RSC	When bit 20 is set to 1b, the cycle timer offset counts cycles of the 24.576-MHz clock and rolls over at the appropriate time, based on the settings of the previous bits. When this bit is cleared, the cycle timer offset does not count.
19-11	RSVD	R	Reserved. Bits 19-11 return 0 0000 0000b when read.
10	RcvPhyPkt	RSC	When bit 10 is set to 1b, the receiver accepts incoming PHY packets into the AR request context if the AR request context is enabled. This bit does not control receipt of self-ID packets.
9	RcvSelfID	RSC	When bit 9 is set to 1b, the receiver accepts incoming self-ID packets. Before setting this bit to 1b, software must ensure that the self-ID buffer pointer register contains a valid address.
8-7	RSVD	R	Reserved. Bits 8 and 7 return 00b when read.
6 (1)	tag1SyncFilterLock	RS	When bit 6 is set to 1b, bit 6 (tag1SyncFilter) in the isochronous receive context match register (see Section 8.46) is set to 1b for all isochronous receive contexts. When bit 6 is cleared, bit 6 (tag1SyncFilter) in the isochronous receive context match register has read/write access.
5-0	RSVD	R	Reserved. Bits 5-0 return 00 0000b when read.

(1) This bit is reset by $\overline{\text{PERST}}$ or $\overline{\text{FRST}}$.

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8.32 Node Identification Register

The node identification register contains the address of the node on which the OHCI-Lynx chip resides, and indicates the valid node number status. The 16-bit combination of the busNumber field (bits 15-6) and the NodeNumber field (bits 5-0) is referred to as the node ID. See Table 8-24 for a complete description of the register contents.

OHCI register offset: E8h

Register type: Read/Write/Update, Read/Update, Read only

Default value: 0000 FFXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	1	1	1	1	1	1	1	1	1	X	X	X	X	X	X

Table 8-24. Node Identification Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	IDValid	RU	Identification valid. Bit 31 indicates whether or not the controller has a valid node number. It is cleared when a 1394 bus reset is detected and set to 1b when the controller receives a new node number from its PHY.
30	root	RU	Root. Bit 30 is set to 1b during the bus reset process if the attached PHY is root.
29-28	RSVD	R	Reserved. Bits 29 and 28 return 00b when read.
27	CPS	RU	Cable power status. Bit 27 is set to 1b if the PHY is reporting that cable power status is OK.
26-16	RSVD	R	Reserved. Bits 26-16 return 000 0000 0000b when read.
15-6	busNumber	RWU	Bus number. This field identifies the specific 1394 bus the controller belongs to when multiple 1394-compatible buses are connected via a bridge. The default value for this field is all 1s.
5-0	NodeNumber	RU	Node number. This field is the physical node number established by the PHY during self identification. It is automatically set to the value received from the PHY after the self-identification phase. If the PHY sets the NodeNumber to 63, software must not set bit 15 (run) in the asynchronous context control register (see Section 8.40) for either of the AT DMA contexts.

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8.33 PHY Control Register

The PHY control register reads from or writes to a PHY register. See Table 8-25 for a complete description of the register contents.

OHCI register offset: ECh
Register type: Read/Write/Update, Read/Write, Read/Update, Read only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8-25. PHY Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	rdDone	RU	Read done. Bit 31 is cleared to 0b by the controller when either bit 15 (rdReg) or bit 14 (wrReg) is set to 1b. This bit is set to 1b when a register transfer is received from the PHY.
30-28	RSVD	R	Reserved. Bits 30-28 return 000b when read.
27-24	rdAddr	RU	Read address. This field is the address of the register most recently received from the PHY.
23-16	rdData	RU	Read data,\. This field is the contents of a PHY register that has been read.
15	rdReg	RWU	Read register. Bit 15 is set to 1b by software to initiate a read request to a PHY register, and is cleared by hardware when the request has been sent. Bits 14 (wrReg) and 15 (rdReg) must not both be set to 1b simultaneously.
14	wrReg	RWU	Write register. Bit 14 is set to 1b by software to initiate a write request to a PHY register, and is cleared by hardware when the request has been sent. Bits 14 (wrReg) and 15 (rdReg) must not both be set to 1b simultaneously.
13-12	RSVD	R	Reserved. Bits 13 and 12 return 00b when read.
11.8	regAddr	RW	Register address. This field is the address of the PHY register to be written or read. The default value for this field is 0h.
7.0	wrData	RW	Write data. This field is the data to be written to a PHY register and is ignored for reads. The default value for this field is 00h.

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8.34 Isochronous Cycle Timer Register

The isochronous cycle timer register indicates the current cycle number and offset. When the controller is cycle master, this register is transmitted with the cycle start message. When the controller is not cycle master, this register is loaded with the data field in an incoming cycle start. In the event that the cycle start message is not received, the fields can continue incrementing on their own (if programmed) to maintain a local time reference. See Table 8-26 for a complete description of the register contents.

OHCI register offset: F0h

Register type: Read/Write/Update

Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8-26. Isochronous Cycle Timer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-25	cycleSeconds	RWU	Cycle seconds. This field counts seconds [rollovers from bits 24-12 (cycleCount field)] modulo 128.
24-12	cycleCount	RWU	Cycle count. This field counts cycles [rollovers from bits 11-0 (cycleOffset field)] modulo 8000.
11-0	cycleOffset	RWU	Cycle offset. This field counts 24.576-MHz clocks modulo 3072, that is, 125 s. If an external 8-kHz clock configuration is being used, this field must be cleared to 000h at each tick of the external clock.

8.35 Asynchronous Request Filter High Register

The asynchronous request filter high set/clear register enables asynchronous receive requests on a per-node basis, and handles the upper node IDs. When a packet is destined for either the physical request context or the ARRQ context, the source node ID is examined. If the bit corresponding to the node ID is not set to 1b in this register, the packet is not acknowledged and the request is not queued. The node ID comparison is done if the source node is on the same bus as the controller. Nonlocal bus-sourced packets are not acknowledged unless bit 31 in this register is set to 1b. See Table 8-27 for a complete description of the register contents.

OHCI register offset: 100h set register
104 h clear register

Register type: Read/Set/Clear

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 8-27. Asynchronous Request Filter High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	asynReqAllBuses	RSC	If bit 31 is set to 1b, all asynchronous requests received by the controller from nonlocal bus nodes are accepted.
30	asynReqResource62	RSC	If bit 30 is set to 1b for local bus node number 62, asynchronous requests received by the controller from that node are accepted.
29	asynReqResource61	RSC	If bit 29 is set to 1b for local bus node number 61, asynchronous requests received by the controller from that node are accepted.
28	asynReqResource60	RSC	If bit 28 is set to 1b for local bus node number 60, asynchronous requests received by the controller from that node are accepted.
27	asynReqResource59	RSC	If bit 27 is set to 1b for local bus node number 59, asynchronous requests received by the controller from that node are accepted.
26	asynReqResource58	RSC	If bit 26 is set to 1b for local bus node number 58, asynchronous requests received by the controller from that node are accepted.
25	asynReqResource57	RSC	If bit 25 is set to 1b for local bus node number 57, asynchronous requests received by the controller from that node are accepted.
24	asynReqResource56	RSC	If bit 24 is set to 1b for local bus node number 56, asynchronous requests received by the controller from that node are accepted.
23	asynReqResource55	RSC	If bit 23 is set to 1b for local bus node number 55, asynchronous requests received by the controller from that node are accepted.
22	asynReqResource54	RSC	If bit 22 is set to 1b for local bus node number 54, asynchronous requests received by the controller from that node are accepted.
21	asynReqResource53	RSC	If bit 21 is set to 1b for local bus node number 53, asynchronous requests received by the controller from that node are accepted.
20	asynReqResource52	RSC	If bit 20 is set to 1b for local bus node number 52, asynchronous requests received by the controller from that node are accepted.
19	asynReqResource51	RSC	If bit 19 is set to 1b for local bus node number 51, asynchronous requests received by the controller from that node are accepted.
18	asynReqResource50	RSC	If bit 18 is set to 1b for local bus node number 50, asynchronous requests received by the controller from that node are accepted.
17	asynReqResource49	RSC	If bit 17 is set to 1b for local bus node number 49, asynchronous requests received by the controller from that node are accepted.
16	asynReqResource48	RSC	If bit 16 is set to 1b for local bus node number 48, asynchronous requests received by the controller from that node are accepted.
15	asynReqResource47	RSC	If bit 15 is set to 1b for local bus node number 47, asynchronous requests received by the controller from that node are accepted.
14	asynReqResource46	RSC	If bit 14 is set to 1b for local bus node number 46, asynchronous requests received by the controller from that node are accepted.
13	asynReqResource45	RSC	If bit 13 is set to 1b for local bus node number 45, asynchronous requests received by the controller from that node are accepted.
12	asynReqResource44	RSC	If bit 12 is set to 1b for local bus node number 44, asynchronous requests received by the controller from that node are accepted.
11	asynReqResource43	RSC	If bit 11 is set to 1b for local bus node number 43, asynchronous requests received by the controller from that node are accepted.
10	asynReqResource42	RSC	If bit 10 is set to 1b for local bus node number 42, asynchronous requests received by the controller from that node are accepted.
9	asynReqResource41	RSC	If bit 9 is set to 1b for local bus node number 41, asynchronous requests received by the controller from that node are accepted.
8	asynReqResource40	RSC	If bit 8 is set to 1b for local bus node number 40, asynchronous requests received by the controller from that node are accepted.
7	asynReqResource39	RSC	If bit 7 is set to 1b for local bus node number 39, asynchronous requests received by the controller from that node are accepted.
6	asynReqResource38	RSC	If bit 6 is set to 1b for local bus node number 38, asynchronous requests received by the controller from that node are accepted.
5	asynReqResource37	RSC	If bit 5 is set to 1b for local bus node number 37, asynchronous requests received by the controller from that node are accepted.
4	asynReqResource36	RSC	If bit 4 is set to 1b for local bus node number 36, asynchronous requests received by the controller from that node are accepted.

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Table 8-27. Asynchronous Request Filter High Register Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
3	asynReqResource35	RSC	If bit 3 is set to 1b for local bus node number 35, asynchronous requests received by the controller from that node are accepted.
2	asynReqResource34	RSC	If bit 2 is set to 1b for local bus node number 34, asynchronous requests received by the controller from that node are accepted.
1	asynReqResource33	RSC	If bit 1 is set to 1b for local bus node number 33, asynchronous requests received by the controller from that node are accepted.
0	asynReqResource32	RSC	If bit 0 is set to 1b for local bus node number 32, asynchronous requests received by the controller from that node are accepted.

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8.36 Asynchronous Request Filter Low Register

The asynchronous request filter low set/clear register enables asynchronous receive requests on a per-node basis, and handles the lower node IDs. Other than filtering different node IDs, this register behaves identically to the asynchronous request filter high register. See Table 8-28 for a complete description of the register contents.

OHCI register offset: 108h set register
10Ch clear register

Register type: Read/Set/Clear

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8-28. Asynchronous Request Filter Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	asynReqResource31	RSC	If bit 31 is set to 1b for local bus node number 31, asynchronous requests received by the controller from that node are accepted.
30	asynReqResource30	RSC	If bit 30 is set to 1b for local bus node number 30, asynchronous requests received by the controller from that node are accepted.
29-2	asynReqResourcen	RSC	Bits 29 through 2 (asynReqResourcen, where n = 29, 28, 27, ..., 2) follow the same pattern as bits 31 and 30.
1	asynReqResource1	RSC	If bit 1 is set to 1b for local bus node number 1, asynchronous requests received by the controller from that node are accepted.
0	asynReqResource0	RSC	If bit 0 is set to 1b for local bus node number 0, asynchronous requests received by the controller from that node are accepted.

8.37 Physical Request Filter High Register

The physical request filter high set/clear register enables physical receive requests on a per-node basis, and handles the upper node IDs. When a packet is destined for the physical request context and the node ID has been compared against the ARRQ registers, the comparison is done again with this register. If the bit corresponding to the node ID is not set to 1b in this register, the request is handled by the ARRQ context instead of the physical request context. The node ID comparison is done if the source node is on the same bus as the controller. Nonlocal bus-sourced packets are not acknowledged unless bit 31 in this register is set to 1b. See Table 8-29 for a complete description of the register contents.

OHCI register offset: 110h set register
114h clear register

Register type: Read/Set/Clear

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 8-29. Physical Request Filter High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	physReqAllBusses	RSC	If bit 31 is set to 1b, all asynchronous requests received by the controller from nonlocal bus nodes are accepted. Bit 31 is not cleared by a PRST.
30	physReqResource 62	RSC	If bit 30 is set to 1b for local bus node number 62, physical requests received by the controller from that node are handled through the physical request context.
29	physReqResource 61	RSC	If bit 29 is set to 1b for local bus node number 61, physical requests received by the controller from that node are handled through the physical request context.
28	physReqResource 60	RSC	If bit 28 is set to 1b for local bus node number 60, physical requests received by the controller from that node are handled through the physical request context.
27	physReqResource 59	RSC	If bit 27 is set to 1b for local bus node number 59, physical requests received by the controller from that node are handled through the physical request context.
26	physReqResource 58	RSC	If bit 26 is set to 1b for local bus node number 58, physical requests received by the controller from that node are handled through the physical request context.
25	physReqResource 57	RSC	If bit 25 is set to 1b for local bus node number 57, physical requests received by the controller from that node are handled through the physical request context.
24	physReqResource 56	RSC	If bit 24 is set to 1b for local bus node number 56, physical requests received by the controller from that node are handled through the physical request context.
23	physReqResource 55	RSC	If bit 23 is set to 1b for local bus node number 55, physical requests received by the controller from that node are handled through the physical request context.
22	physReqResource 54	RSC	If bit 22 is set to 1b for local bus node number 54, physical requests received by the controller from that node are handled through the physical request context.
21	physReqResource 53	RSC	If bit 21 is set to 1b for local bus node number 53, physical requests received by the controller from that node are handled through the physical request context.
20	physReqResource 52	RSC	If bit 20 is set to 1b for local bus node number 52, physical requests received by the controller from that node are handled through the physical request context.
19	physReqResource 51	RSC	If bit 19 is set to 1b for local bus node number 51, physical requests received by the controller from that node are handled through the physical request context.
18	physReqResource 50	RSC	If bit 18 is set to 1b for local bus node number 50, physical requests received by the controller from that node are handled through the physical request context.
17	physReqResource 49	RSC	If bit 17 is set to 1b for local bus node number 49, physical requests received by the controller from that node are handled through the physical request context.
16	physReqResource 48	RSC	If bit 16 is set to 1b for local bus node number 48, physical requests received by the controller from that node are handled through the physical request context.
15	physReqResource 47	RSC	If bit 15 is set to 1b for local bus node number 47, physical requests received by the controller from that node are handled through the physical request context.
14	physReqResource 46	RSC	If bit 14 is set to 1b for local bus node number 46, physical requests received by the controller from that node are handled through the physical request context.
13	physReqResource 45	RSC	If bit 13 is set to 1b for local bus node number 45, physical requests received by the controller from that node are handled through the physical request context.
12	physReqResource 44	RSC	If bit 12 is set to 1b for local bus node number 44, physical requests received by the controller from that node are handled through the physical request context.
11	physReqResource 43	RSC	If bit 11 is set to 1b for local bus node number 43, physical requests received by the controller from that node are handled through the physical request context.
10	physReqResource 42	RSC	If bit 10 is set to 1b for local bus node number 42, physical requests received by the controller from that node are handled through the physical request context.
9	physReqResource 41	RSC	If bit 9 is set to 1b for local bus node number 41, physical requests received by the controller from that node are handled through the physical request context.
8	physReqResource 40	RSC	If bit 8 is set to 1b for local bus node number 40, physical requests received by the controller from that node are handled through the physical request context.
7	physReqResource 39	RSC	If bit 7 is set to 1b for local bus node number 39, physical requests received by the controller from that node are handled through the physical request context.
6	physReqResource 38	RSC	If bit 6 is set to 1b for local bus node number 38, physical requests received by the controller from that node are handled through the physical request context.
5	physReqResource 37	RSC	If bit 5 is set to 1b for local bus node number 37, physical requests received by the controller from that node are handled through the physical request context.
4	physReqResource 36	RSC	If bit 4 is set to 1b for local bus node number 36, physical requests received by the controller from that node are handled through the physical request context.

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Table 8-29. Physical Request Filter High Register Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
3	physReqResource 35	RSC	If bit 3 is set to 1b for local bus node number 35, physical requests received by the controller from that node are handled through the physical request context.
2	physReqResource 34	RSC	If bit 2 is set to 1b for local bus node number 34, physical requests received by the controller from that node are handled through the physical request context.
1	physReqResource 33	RSC	If bit 1 is set to 1b for local bus node number 33, physical requests received by the controller from that node are handled through the physical request context.
0	physReqResource 32	RSC	If bit 0 is set to 1b for local bus node number 32, physical requests received by the controller from that node are handled through the physical request context.

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8.38 Physical Request Filter Low Register

The physical request filter low set/clear register enables physical receive requests on a per-node basis, and handles the lower node IDs. When a packet is destined for the physical request context and the node ID has been compared against the asynchronous request filter registers, the node ID comparison is done again with this register. If the bit corresponding to the node ID is not set to 1b in this register, the request is handled by the asynchronous request context instead of the physical request context. See Table 8-30 for a complete description of the register contents.

OHCI register offset: 118h set register
11Ch clear register

Register type: Read/Set/Clear

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8-30. Physical Request Filter Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	physReqResource31	RSC	If bit 31 is set to 1b for local bus node number 31, physical requests received by the controller from that node are handled through the physical request context.
30	physReqResource30	RSC	If bit 30 is set to 1b for local bus node number 30, physical requests received by the controller from that node are handled through the physical request context.
29-2	physReqResourcen	RSC	Bits 29 through 2 (physReqResourcen, where n = 29, 28, 27, ..., 2) follow the same pattern as bits 31 and 30.
1	physReqResource1	RSC	If bit 1 is set to 1b for local bus node number 1, physical requests received by the controller from that node are handled through the physical request context.
0	physReqResource0	RSC	If bit 0 is set to 1b for local bus node number 0, physical requests received by the controller from that node are handled through the physical request context.

8.39 Physical Upper Bound Register (Optional Register)

The physical upper bound register is an optional register and is not implemented. This register returns 0000 0000h when read.

OHCI register offset: 120h

Register type: Read only

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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8.40 Asynchronous Context Control Register

The asynchronous context control set/clear register controls the state and indicates status of the DMA context. See Table 8-31 for a complete description of the register contents.

OHCI register offset:
- 180h set register (ATRQ)
- 184h clear register (ATRQ)
- 1A0h set register [ATRS]
- 1A4h clear register [ATRS]
- 1C0h set register (ARRQ)
- 1C4h clear register (ARRQ)
- 1E0h set register (ARRS)
- 1E4h clear register (ARRS)

Register type: Read/Set/Clear/Update, Read/Set/Update, Read/Update, Read only

Default value: 0000 X0XXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

Table 8-31. Asynchronous Context Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-16	RSVD	R	Reserved. Bits 31-16 return 0000h when read.
15	run	RSCU	Run. Bit 15 is set to 1b by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The controller changes this bit only on a system (hardware) or software reset.
14-13	RSVD	R	Reserved. Bits 14 and 13 return 00b when read.
12	wake	RSU	Wake. Software sets bit 12 to 1b to cause the controller to continue or resume descriptor processing. The controller clears this bit on every descriptor fetch.
11	dead	RU	Dead. The controller sets bit 11 to 1b when it encounters a fatal error, and clears the bit when software clears bit 15 (run). Asynchronous contexts supporting out-of-order pipelining provide unique ContextControl.dead functionality. See Section 7.7 in the 1394 Open Host Controller Interface Specification, Release 1.1 for more information.
10	active	RU	Active. The controller sets bit 10 to 1b when it is processing descriptors.
9	betaFrame	RU	Beta frame. Set to 1 when the PHY indicates that the received packet is sent in beta format. A response to a request sent using beta format also uses beta format.
8	RSVD	R	Reserved. Bit 8 returns 0b when read.
7-5	spd	RU	Speed. This field indicates the speed at which a packet was received or transmitted and only contains meaningful information for receive contexts. This field is encoded as: 000 = 100M bit/s 001 = 200M bit/s 010 = 400M bit/s 011 = 800M bit/s0 All other values are reserved.
4-0	eventcode	RU	Event code. This field holds the acknowledge sent by the link core for this packet or an internally-generated error code if the packet was not transferred successfully.

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8.41 Asynchronous Context Command Pointer Register

The asynchronous context command pointer register contains a pointer to the address of the first descriptor block that the controller accesses when software enables the context by setting bit 15 (run) in the asynchronous context control register (see Section 8.40) to 1b. See Table 8-32 for a complete description of the register contents.

OHCI register offset: 18Ch (ATRQ)
1ACh (ATRS)
1CCh (ARRQ)
1ECh (ARRS)

Register type: Read/Write/Update

Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8-32. Asynchronous Context Command Pointer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-4	descriptorAddress	RWU	Contains the upper 28 bits of the address of a 16-byte aligned descriptor block.
3-0	Z	RWU	Indicates the number of contiguous descriptors at the address pointed to by the descriptor address. If Z is 0h, it indicates that the descriptorAddress field (bits 31-4) is not valid.

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8.42 Isochronous Transmit Context Control Register

The isochronous transmit context control set/clear register controls options, state, and status for the isochronous transmit DMA contexts. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3, ..., 7). See Table 8-33 for a complete description of the register contents.

OHCI register offset: 200h + (16 * n) set register
204h + (16 * n) clear register

Register type: Read/Set/Clear/Update, Read/Set/Clear, Read/Set/Update, Read/Update, Read only

Default value: XXXX X0XXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

Table 8-33. Isochronous Transmit Context Control Register Description (1)

BIT	FIELD NAME	TYPE	DESCRIPTION
31	cycleMatchEnable	RSCU	When bit 31 is set to 1b, processing occurs such that the packet described by the context first descriptor block is transmitted in the cycle whose number is specified in the cycleMatch field (bits 30-16). The cycleMatch field (bits 30-16) must match the low-order two bits of cycleSeconds and the 13-bit cycleCount field in the cycle start packet that is sent or received immediately before isochronous transmission begins. Since the isochronous transmit DMA controller may work ahead, the processing of the first descriptor block may begin slightly in advance of the actual cycle in which the first packet is transmitted. The effects of this bit, however, are impacted by the values of other bits in this register and are explained in the 1394 Open Host Controller Interface Specification. Once the context has become active, hardware clears this bit.
30-16	cycleMatch	RSC	This field contains a 15-bit value, corresponding to the low-order two bits of the isochronous cycle timer register at OHCI offset F0h (see Section 8.34) cycleSeconds field (bits 31-25) and the cycleCount field (bits 24-12). If bit 31 (cycleMatchEnable) is set to 1b, this isochronous transmit DMA context becomes enabled for transmits when the low-order two bits of the isochronous cycle timer register at OHCI offset F0h cycleSeconds field (bits 31-25) and the cycleCount field (bits 24-12) value equal this field (cycleMatch) value.
15	run	RSC	Bit 15 is set to 1b by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The controller changes this bit only on a system (hardware) or software reset.
14-13	RSVD	R	Reserved. Bits 14 and 13 return 00b when read.
12	wake	RSU	Software sets bit 12 to 1b to cause the controller to continue or resume descriptor processing. The controller clears this bit on every descriptor fetch.
11	dead	RU	The controller sets bit 11 to 1b when it encounters a fatal error, and clears the bit when software clears bit 15 (run) to 0b.
10	active	RU	The controller sets bit 10 to 1b when it is processing descriptors.
9-5	RSVD	R	Reserved. Bits 9-5 return 00000b when read.
4-0	eent code	RU	Following an OUTPUT_LAST* command, the error code is indicated in this field. Possible values are ack_complete, evt_descriptor_read, evt_data_read, and evt_unknown.

(1) On an overflow for each running context, the isochronous transmit DMA supports up to seven cycle skips when the following are true:
- Bit 11 (dead) in either the isochronous transmit or receive context control register is set to 1b.
- Bits 4-0 (eventcode field) in either the isochronous transmit or receive context control register are set to evt_timeout.
- Bit 24 (unrecoverableError) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) is set to 1b.

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8.43 Isochronous Transmit Context Command Pointer Register

The isochronous transmit context command pointer register contains a pointer to the address of the first descriptor block that the controller accesses when software enables an isochronous transmit context by setting bit 15 (run) in the isochronous transmit context control register (see Section 8.42) to 1b. The isochronous transmit DMA context command pointer can be read when a context is active. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3, ..., 7).

OHCI register offset: 20Ch + (16 * n)

Register type: Read only

Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

8.44 Isochronous Receive Context Control Register

The isochronous receive context control set/clear register controls options, state, and status for the isochronous receive DMA contexts. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3). See Table 8-34 for a complete description of the register contents.

OHCI register offset: 400h + (32 * n) set register
404h + (32 * n) clear register

Register type: Read/Set/Clear/Update, Read/Set/Clear, Read/Set/Update, Read/Update, Read only

Default value: XX00 X0XXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

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Table 8-34. Isochronous Receive Context Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	bufferFill	RSC	Buffer fill. When bit 31 is set to 1b, received packets are placed back to back to completely fill each receive buffer. When this bit is cleared, each received packet is placed in a single buffer. If bit 28 (multiChanMode) is set to 1b, this bit must also be set to 1b. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1b.
30	isochHeader	RSC	Isochronous header. When bit 30 is set to 1b, received isochronous packets include the complete 4-byte isochronous packet header seen by the link layer. The end of the packet is marked with a xferStatus in the first doublet, and a 16-bit timestamp indicating the time of the most recently received (or sent) cycleStart packet. When this bit is cleared, the packet header is stripped from received isochronous packets. The packet header, if received, immediately precedes the packet payload. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1b.
29	cycleMatchEnable	RSCU	Cycle match enable. When bit 29 is set to 1b and the 13-bit cycleMatch field (bits 24-12) in the isochronous receive context match register (See Section 8.46) matches the 13-bit cycleCount field in the cycleStart packet, the context begins running. The effects of this bit, however, are impacted by the values of other bits in this register. Once the context has become active, hardware clears this bit. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1b.
28	multiChanMode	RSC	Multichannel mode. When bit 28 is set to 1b, the corresponding isochronous receive DMA context receives packets for all isochronous channels enabled in the isochronous receive channel mask high register at OHCI offset 70h/74h (see Section 8.19) and isochronous receive channel mask low register at OHCI offset 78h/7Ch (see Section 8.20). The isochronous channel number specified in the isochronous receive context match register (see Section 8.46) is ignored. When this bit is cleared, the isochronous receive DMA context receives packets for the single channel specified in the isochronous receive context match register (see Section 8.46). Only one isochronous receive DMA context may use the isochronous receive channel mask registers (see Section 8.19, and Section 8.20). If more than one isochronous receive context control register has this bit set, the results are undefined. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1b.
27	dualBufferMode	RSC	Dual-buffer mode. When bit 27 is set to 1b, receive packets are separated into first and second payload and streamed independently to the firstBuffer series and secondBuffer series as described in Section 10.2.3 in the 1394 Open Host Controller Interface Specification. Also, when bit 27 is set to 1b, both bits 28 (multiChanMode) and 31 (bufferFill) are cleared to 00b. The value of this bit does not change when either bit 10 (active) or bit 15 (run) is set to 1b.
26-16	RSVD	R	Reserved. Bits 26-16 return 000 0000 0000b when read.
15	run	RSCU	Run. Bit 15 is set to 1b by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The controller changes this bit only on a system (hardware) or software reset.
14-13	RSVD	R	Reserved. Bits 14 and 13 return 00b when read.
12	wake	RSU	Wake. Software sets bit 12 to 1b to cause the controller to continue or resume descriptor processing. The controller clears this bit on every descriptor fetch.
11	dead	RU	Dead. The controller sets bit 11 to 1b when it encounters a fatal error, and clears the bit when software clears bit 15 (run).
10	active	RU	Active. The controller sets bit 10 to 1b when it is processing descriptors.
9	betaFrame	RU	Beta frame. Set to 1 when the PHY indicates that the received packet is sent in beta format. A response to a request sent using beta format also uses beta format.
9-8	RSVD	R	Reserved. Bit 8 returns 0b when read.
7-8	spd	RU	Speed. This field indicates the speed at which the packet was received. 000 = 100M bit/s 001 = 200M bit/s 010 = 400M bit/s 011 = 800M bit/s0 All other values are reserved.
4-0	event code	RU	For bufferFill mode, possible values are ack_complete, evt_descriptor_read, evt_data_write, and evt_unknown. Packets with data errors (either dataLength mismatches or dataCRC errors) and packets for which a FIFO overrun occurred are backed out. For packet-per-buffer mode, possible values are ack_complete, ack_data_error, evt_long_packet, evt_overrun, evt_descriptor_read, evt_data_write, and evt_unknown.

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8.45 Isochronous Receive Context Command Pointer Register

The isochronous receive context command pointer register contains a pointer to the address of the first descriptor block that the controller accesses when software enables an isochronous receive context by setting bit 15 (run) in the isochronous receive context control register (see Section 8.44) to 1b. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3).

OHCI register offset: 40Ch + (32 * n)

Register type: Read only

Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

8.46 Isochronous Receive Context Match Register

The isochronous receive context match register starts an isochronous receive context running on a specified cycle number, filters incoming isochronous packets based on tag values, and waits for packets with a specified sync value. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3). See Table 8-35 for a complete description of the register contents.

OHCI register offset: 410h + (32 * n)

Register type: Read/Write, Read only

Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	0	0	0	X	X	X	X	X	X	X	X	X

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8-35. Isochronous Receive Context Match Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	tag3	RW	If bit 31 is set to 1b, this context matches on isochronous receive packets with a tag field of 11b.
30	tag2	RW	If bit 30 is set to 1b, this context matches on isochronous receive packets with a tag field of 10b.
29	tag1	RW	If bit 29 is set to 1b, this context matches on isochronous receive packets with a tag field of 01b.
28	tag0	RW	If bit 28 is set to 1b, this context matches on isochronous receive packets with a tag field of 00b.
27	RSVD	R	Reserved. Bit 27 returns 0b when read.
26-12	cycleMatch	RW	This field contains a 15-bit value corresponding to the two low-order bits of cycleSeconds and the 13-bit cycleCount field in the cycleStart packet. If cycleMatchEnable (bit 29) in the isochronous receive context control register (see Section 8.44) is set to 1b, this context is enabled for receives when the two low-order bits of the isochronous cycle timer register at OHCI offset F0h (see Section 8.34) cycleSeconds field (bits 31-25) and cycleCount field (bits 24-12) value equal this field (cycleMatch) value.
11-8	sync	RW	This 4-bit field is compared to the sync field of each isochronous packet for this channel when the command descriptor w field is set to 11b.
7	RSVD	R	Reserved. Bit 7 returns 0b when read.
6	tag1SyncFilter	RW	If bit 6 and bit 29 (tag1) are set to 11b, packets with tag 01b are accepted into the context if the two most significant bits of the packet sync field are 00b. Packets with tag values other than 01b are filtered according to bit 28 (tag0), bit 30 (tag2), and bit 31 (tag3) without any additional restrictions. If this bit is cleared, this context matches on isochronous receive packets as specified in bits 28-31 (tag0-tag3) with no additional restrictions.

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Table 8-35. Isochronous Receive Context Match Register Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
5-0	channelNumber	RW	This 6-bit field indicates the isochronous channel number for which this isochronous receive DMA context accepts packets.

9 1394 OHCI Memory-Mapped TI Extension Register Space

The TI extension base address register provides a method of accessing memory-mapped TI extension registers. See Section 7.9, TI Extension Base Address Register, for register bit field details. See Table 9-1 for the TI extension register listing.

Table 9-1. TI Extension Register Map

REGISTER NAME	OFFSET
Reserved	00h-A7Fh
Isochronous receive digital video enhancement set	A80h
Isochronous receive digital video enhancement clear	A84h
Link enhancement control set	A88h
Link enhancement control clear	A8Ch
Isochronous transmit context 0 timestamp offset	A90h
Isochronous transmit context 1 timestamp offset	A94h
Isochronous transmit context 2 timestamp offset	A98h
Isochronous transmit context 3 timestamp offset	A9Ch
Isochronous transmit context 4 timestamp offset	AA0h
Isochronous transmit context 5 timestamp offset	AA4h
Isochronous transmit context 6 timestamp offset	AA8h
Isochronous transmit context 7 timestamp offset	AACh
Reserved	AB0h-FFFh

9.1 Digital Video (DV) and MPEG2 Timestamp Enhancements

The DV timestamp enhancements are enabled by bit 8 (enab_dv_ts) in the link enhancement control register located at PCI offset F4h, and are aliased in TI extension register space at offset A88h (set) and A8Ch (clear).

The DV and MPEG transmit enhancements are enabled separately by bits in the link enhancement control register located in PCI configuration space at PCI offset F4h. The link enhancement control register is also aliased as a set/clear register in TI extension space at offset A88h (set) and A8Ch (clear).

Bit 8 (enab_dv_ts) of the link enhancement control register enables DV timestamp support. When enabled, the link calculates a timestamp based on the cycle timer and the timestamp offset register and substitutes it in the SYT field of the CIP once per DV frame.

Bit 10 (enab_mpeg_ts) of the link enhancement control register enables MPEG timestamp support. Two MPEG timestamp modes are supported. The default mode calculates an initial delta that is added to the calculated timestamp in addition to a user-defined offset. The initial offset is calculated as the difference in the intended transmit cycle count and the cycle count field of the timestamp in the first TSP of the MPEG2 stream. The use of the initial delta can be controlled by bit 31 (DisableInitialOffset) in the timestamp offset register (see Section 9.5).

The MPEG2 timestamp enhancements are enabled by bit 10 (enab_mpeg_ts) in the link enhancement control register located at PCI offset F4h, and aliased in TI extension register space at offset A88h (set) and A8Ch (clear).

When bit 10 (enab_mpeg_ts) is set to 1b, the hardware applies the timestamp enhancements to isochronous transmit packets that have the tag field equal to 01b in the isochronous packet header and a FMT field equal to 10h.

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9.2 Isochronous Receive Digital Video Enhancements

The DV frame sync and branch enhancement provides a mechanism in buffer-fill mode to synchronize 1394 DV data that is received in the correct order to DV frame-sized data buffers described by several INPUT_MORE descriptors (see 1394 Open Host Controller Interface Specification, Release 1.1). This is accomplished by waiting for the start-of-frame packet in a DV stream before transferring the received isochronous stream into the memory buffer described by the INPUT_MORE descriptors. This can improve the DV capture application performance by reducing the amount of processing overhead required to strip the CIP header and copy the received packets into frame-sized buffers.

The start of a DV frame is represented in the 1394 packet as a 16-bit pattern of 1FX7h (first byte 1Fh and second byte X7h) received as the first two bytes of the third quadlet in a DV isochronous packet.

9.3 Isochronous Receive Digital Video Enhancement Registers

The isochronous receive digital video enhancement registers enable the DV enhancements in the controller. The bits in these registers may only be modified when both the active (bit 10) and run (bit 15) bits of the corresponding context control register are 00b. See Table 9-2 for a complete description of the register contents.

TI extension register offset: A80h set register
A84h clear register

Register type: Read/Set/Clear, Read only

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 9-2. Isochronous Receive Digital Video Enhancement Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-14	RSVD	R	Reserved. Bits 31-14 return 00 0000 0000 0000 0000b when read.
13	DV_Branch3	RSC	When bit 13 is set to 1b, the isochronous receive context 3 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b, and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is only interpreted when bit 12 (CIP_Strip3) is set to 1b and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 460h/464h (see Section 8.44) is cleared to 0b.
12	CIP_Strip3	RSC	When bit 12 is set to 1b, the isochronous receive context 3 strips the first two quadlets of payload. This bit is only interpreted when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 460h/464h (see Section 8.44) is cleared to 0b.
11-10	RSVD	R	Reserved. Bits 11 and 10 return 00b when read.
9	DV_Branch2	RSC	When bit 9 is set to 1b, the isochronous receive context 2 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b, and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is only interpreted when bit 8 (CIP_Strip2) is set to 1b and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 440h/444h (see Section 8.44) is cleared to 0b.
8	CIP_Strip2	RSC	When bit 8 is set to 1b, the isochronous receive context 2 strips the first two quadlets of payload. This bit is only interpreted when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 440h/444h (see Section 8.44) is cleared to 0b.
7-6	RSVD	R	Reserved. Bits 7 and 6 return 00b when read.
5	DV_Branch1	TSC	When bit 5 is set to 1b, the isochronous receive context 1 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b, and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is only interpreted when bit 4 (CIP_Strip1) is set to 1b and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 420h/424h (see Section 8.44) is cleared to 0b.

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Table 9-2. Isochronous Receive Digital Video Enhancement Registers Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
4	CIP_Strip1	RSC	When bit 4 is set to 1b, the isochronous receive context 1 strips the first two quadlets of payload. This bit is only interpreted when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 420h/424h (see Section 8.44) is cleared to 0b.
3-2	RSVD	R	Reserved. Bits 3 and 2 return 00b when read.
1	DV_Branch0	RSC	When bit 1 is set to 1b, the isochronous receive context 0 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b and jumps to the descriptor pointed to by frameBranch a DV frame start tag is received out of place. This bit is only interpreted when bit 0 (CIP_Strip0) is set to 1b and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 400h/404h (see Section 8.44) is cleared to 0b.
0	CIP_Strip0	RSC	When bit 0 is set to 1b, the isochronous receive context 0 strips the first two quadlets of payload. This bit is only interpreted when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 400h/404h (see Section 8.44) is cleared to 0b.

9.4 Link Enhancement Control Registers

These registers are a memory-mapped set/clear registers that are an alias of the link enhancement control register at PCI offset F4h. These bits may be initialized by software. Some of the bits may also be initialized by a serial EEPROM, if one is present, as noted in the following bit descriptions. If the bits are to be initialized by software, the bits must be initialized prior to setting bit 19 (LPS) in the host controller control register at OHCI offset 50h/54h (see Section 3.3.2). See Table 9-3 for a complete description of the register contents.

TI extension register offset: A88h set register
A8Ch clear register

Register type: Read/Set/Clear, Read only

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Table 9-3. Link Enhancement Control Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31-16	RSVD	R	Reserved. Bits 31-16 return 0000h when read.
15(1)	dis_at_pipleline	RW	Disable AT pipelining. When bit 15 is set to 1b, out-of-order AT pipelining is disabled. The default value for this bit is 0b.
14(1)	RSVD	RW	Reserved. Bit 14 defaults to 0b and must remain 0b for normal operation of the OHCI core.

(1) This bit is reset by $\overline{\text{PERST}}$ or $\overline{\text{FRST}}$.

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Table 9-3. Link Enhancement Control Registers Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
13-12 (2)	atx_thresh	RW	This field sets the initial AT threshold value, which is used until the AT FIFO is underrun. When the OHCI controller retries the packet, it uses a 2K-byte threshold, resulting in a store-and-forward operation. 00 = Threshold ~2K bytes resulting in a store-and-forward operation 01 = Threshold ~1.7K bytes (default) 10 = Threshold ~1K bytes 11 = Threshold ~512 bytes These bits fine tune the asynchronous transmit threshold. For most applications the 1.7K-byte threshold is optimal. Changing this value may increase or decrease the 1394 latency depending on the average PCI bus latency. Setting the AT threshold to 1.7K, 1K, or 512 bytes results in data being transmitted at these thresholds or when an entire packet has been checked into the FIFO. If the packet to be transmitted is larger than the AT threshold, the remaining data must be received before the AT FIFO is emptied; otherwise, an underrun condition occurs, resulting in a packet error at the receiving node. As a result, the link then commences store-and-forward operation. Wait until it has the complete packet in the FIFO before retransmitting it on the second attempt to ensure delivery. An AT threshold of 2K results in store-and-forward operation, which means that asynchronous data will not be transmitted until an end-of-packet token is received. Restated, setting the AT threshold to 2K results in only complete packets being transmitted. Note that the OHCI controller will always use store-and-forward when the asynchronous transmit retries register at OHCI offset 08h (see Section 8.3, Asynchronous Transmit Retries Register) is cleared.
11	RSVD	R	Reserved. Bit 11 returns 0b when read.
10(1)	enab_mpeg_ts	RW	Enable MPEG timestamp enhancement. When this bit is set, Cheetah-Express shall apply time stamp enhancements to isochronous transmit packets that have the tag field equal to 2b01 in the isochronous packet header and a FMT field equal to 6h10.
9	RSVD	R	Reserved. Bit 9 returns 0b when read.
8(1)	enab_dv_ts	RW	Enable DV CIP timestamp enhancement. When bit 8 is set to 1b, the enhancement is enabled for DV CIP transmit streams (FMT = 00h). The default value for this bit is 0b.
7(1)	enab_unfair	RW	Enable asynchronous priority requests (OHCI-Lynx compatible). Setting bit 7 to 1b enables the link to respond to requests with priority arbitration. It is recommended that this bit be set to 1b. The default value for this bit is 0b.
6-3	RSVD	R	Reserved. Bits 6-3 return 0h when read.
2(1)	enab_insert_idle	RW	Enable insert idle (OHCI-Lynx compatible). When the PHY has control of the Ct[0:1] internal control lines and D[0:8] internal data lines and the link requests control, the PHY drives 11b on the Ct[0:1] lines. The link can then start driving these lines immediately. Setting this bit to 1 inserts an idle state, so the link waits one clock cycle before it starts driving the lines (turnaround time). It is recommended that this bit be set to 1. For use with TI phys this bit should be set to 0. If a serial EEPROM is implemented this bit is initialized with the value of EEPROM word 0x05 bit 2.
1(1)	enab_accel	RW	Enable acceleration enhancements (OHCI-Lynx compatible). When bit 1 is set to 1b, the PHY is notified that the link supports the IEEE Std 1394a-2000 acceleration enhancements, that is, ack-accelerated, fly-by concatenation, etc. It is recommended that this bit be set to 1b. The default value for this bit is 0b.
0	RSVD	R	Reserved. Bit 0 returns 0b when read.

(2) This bit is reset by $\overline{\text{PERST}}$ or $\overline{\text{FRST}}$.

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9.5 Timestamp Offset Registers

The value of these registers is added as an offset to the cycle timer value when using the MPEG, DV, and CIP enhancements. A timestamp offset register is implemented per isochronous transmit context. The n value following the offset indicates the context number (n = 0, 1, 2, 3, ..., 7). These registers are programmed by software as appropriate. See Table 9-4 for a complete description of the register contents.

TI extension register offset: A90h + (4*n)

Register type: Read/Write, Read only

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 9-4. Timestamp Offset Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	DisableInitialOffset	RW	Bit 31 disables the use of the initial timestamp offset when the MPEG2 enhancements are enabled. A value of 0b indicates the use of the initial offset, a value of 1b indicates that the initial offset must not be applied to the calculated timestamp. This bit has no meaning for the DV timestamp enhancements. The default value for this bit is 0b.
3-=25	RSVD	R	Reserved. Bits 30-25 return 000 0000b when read.
24-12	CycleCount	RW	This field adds an offset to the cycle count field in the timestamp when the DV or MPEG2 enhancements are enabled. The cycle count field is incremented modulo 8000; therefore, values in this field must be limited between 0 and 7999. The default value for this field is all 0s.
11-0	CycleOffset	RW	This field adds an offset to the cycle offset field in the timestamp when the DV or MPEG2 enhancements are enabled. The cycle offset field is incremented modulo 3072; therefore, values in this field must be limited between 0 and 3071. The default value for this field is all 0s.

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10 Physical Layer (PHY) Section

The cable interface can follow either the IEEE Std 1394a-2000 protocol or the IEEE Std 1394b-2002 protocol on all ports. The mode of operation is determined by the interface capabilities of the ports being connected. When either of the ports is connected to an IEEE Std 1394a-2000-compliant device, the cable interface on that port operates in the IEEE Std 1394a-2000 data-strobe mode at a compatible S100, S200, or S400 speed. When a bilingual port is connected to an IEEE Std 1394b-2002-compliant node, the cable interface on that port operates per the IEEE Std 1394b-2002 standard at S400B or S800 speed. The XIO2213B automatically determines the correct cable interface connection method for the bilingual ports.

To operate a port as an IEEE Std 1394b-2002 bilingual port, the data-strobe-only terminal for the port (DS0, DS1, or DS2_P) must be pulled to ground through a 1-kΩ resistor. The port must be operated in the IEEE Std 1394b-2002 bilingual mode whenever an IEEE Std 1394b-2002 bilingual or an IEEE Std 1394b-2002 beta-only connector is connected to the port. To operate the port as an IEEE Std 1394a-2000-only port, the data-strobe-only terminal (DS0, DS1, or DS2_P) must be pulled to 3.3-V V_{CC} through a 1-kΩ resistor. The only time the port must be forced to the data-strobe-only mode is if the port is connected to an IEEE Std 1394a-2000 connector [either 6 pin (recommended) or 4 pin]. This mode is provided to ensure that IEEE Std 1394b-2002 signaling is never sent across an IEEE Std 1394a-2000 cable.

During packet reception, the serial data bits are split into 2-, 4-, or 8-bit parallel streams by the PHY section and sent to the link-layer controller (LLC) section. The received data is also transmitted (repeated) on the other connected and active cable ports.

Both the twisted pair A (TPA) and the twisted pair B (TPB) cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration when connected to an IEEE Std 1394a-2000-compliant device. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during IEEE Std 1394a-2000-mode arbitration and sets the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted pair bias (TPBIAS) voltage.

When connected to an IEEE Std 1394a-2000-compliant node, the XIO2213B PHY section provides a 1.86-V nominal bias voltage at the TPBIAS terminal for port termination. The PHY section contains three independent TPBIAS circuits (one for each port). This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1 µF.

The line drivers in the XIO2213B PHY section are designed to work with external 112-Ω termination resistor networks in order to match the 110-Ω cable impedance. One termination network is required at each end of a twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The midpoint of the pair of resistors that is connected to the TPA terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the TPB terminals is coupled to ground through a parallel RC network, with recommended values of 5 k and 270 pF. The values of the external line-termination resistors are selected to meet the standard specifications when connected in parallel with the internal receiver circuits. A precision external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents.

When the power supply of the XIO2213B is off while the twisted-pair cables are connected, the XIO2213B transmitter and receiver circuitry present to the cable a high-impedance signal that does not load the device at the other end of the cable.

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When the XIO2213B PHY section is used without one or more of the ports brought out to a connector, the twisted-pair terminals of the unused ports must be terminated for reliable operation. For each unused port, the port must be forced to the IEEE Std 1394a-2000-only mode (data-strobe-only mode) by pulling DSn to VCC through a 1KΩ resistor, after which the TPB+ and TPB– terminals can be tied together and then pulled to ground; or TPB+ and TPB– can be connected to the suggested normal termination network. TPA+ and TPA– of an unused port can be left unconnected. The TPBIAS terminal can be connected through a 1-µF capacitor to ground or left unconnected.

The TESTM, SE, and SM terminals are used to set up various manufacturing test conditions. For normal operation, TESTM must be connected to VDD through a 1-kΩ resistor. The SE and SM terminals must be tied to ground through a 1-kΩ resistor.

The LPS_P (link power status) terminal of the PHY section works with the LKON terminal to manage the power usage in the node. The LPS_L signal from the LLC section is used in conjunction with the LCtrl bit (see Table 10-1 and Table 10-2) to indicate the active/power status of the LLC section. The LPS_P signal also resets, disables, and initializes the PHY-section/LLC-section interface (the state of the PHY-section/LLC-section interface is controlled solely by the LPS_P input, regardless of the state of the LCtrl bit). The LPS_P terminal of the PHY section must be connected to the LPS_L terminal of the LLC section during normal operation.

The LPS_P input is considered inactive if it remains low for more than the $\overline{\text{PHY_RESET}}$ time (see the LPS terminal definition) and is considered active otherwise. When the PHY section detects that the LPS_P input is inactive, the PHY-section/LLC-section interface is placed into a low-power reset state in which the CTL and D outputs are held in the logic 0 state and the LREQ input is ignored; however, the PCLK output remains active. If the LPS input remains low for more than the LPS_DISABLE time (see the LPS terminal definition), the PHY-section/LLC-section interface is put into a low-power disabled state in which the PCLK_P output is also held inactive. The XIO2213B continues the necessary PHY repeater functions required for normal network operation, regardless of the state of the PHY-section/LLC-section interface. When the interface is in the reset or disabled state and the LPS input is again observed active, the PHY section initializes the interface and returns to normal operation. The PHY-section/LLC-section interface is also held in the disabled state during hardware reset. When the LPS_P terminal is returned to an active state after being sensed as having entered the LPS_DISABLE time, the XIO2213B issues a bus reset. This broadcasts the node self-ID packet, which contains the updated L bit state (the PHY section and LLC section now being accessible).

The PHY section uses the LKON terminal to notify the LLC section to power up and become active. When activated, the output LKON signal is a square wave. The PHY section activates the LKON output when the LLC section is inactive and a wake-up event occurs. The LLC section is considered inactive when either the LPS_P input is inactive, as previously described, or the LCtrl bit is cleared to 0. A wake-up event occurs when a link-on PHY packet addressed to this node is received, or conditionally when a PHY interrupt occurs. The PHY section deasserts the LKON output when the LLC section becomes active (both LPS_P sensed as active and the LCtrl bit set to 1). The PHY section also deasserts the LKON output when a bus reset occurs, unless a PHY interrupt condition exists, which would otherwise cause LKON to be active. If the XIO2213B is power cycled and the power class is 0 through 4, the PHY section asserts LKON for approximately 167 ms or until both the LPS_P is active and the LCtrl bit is 1.

10.1 PHY Section Register Configuration

There are 16 accessible PHY section registers in the XIO2213B. The configuration of the registers at addresses 0h through 7h (the base registers) is fixed, while the configuration of the registers at addresses 8h through Fh (the paged registers) is dependent on which of eight pages, numbered 0h through 7h, is currently selected. The selected page is set in base register 7h. Note that while this register set is compatible with IEEE Std 1394a-2000 register sets, some fields have been redefined and this register set contains additional fields.

Table 10-1 shows the configuration of the base registers, and Table 10-2 gives the corresponding field descriptions. The base register field definitions are unaffected by the selected page number.

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A reserved register or register field (marked as Reserved or RSVD in the following register configuration tables) is read as 0, but is subject to future usage. All registers in address pages 2 through 6 are reserved.

Table 10-1. Base Register Description

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	Physical_ID						R	CPS
0001	RHB	IBR	Gap_Count					
0010	Extended (111b)			Num_Ports (00011b)				
0011	PHY_Speed (111b)			RSVD	Delay (0000b)			
0100	LCtrl	C	Jitter (000b)			Pwr_Class		
0101	WDIE	ISBR	CTOI	CPSI	STOI	PEI	EAA	EMC
0110	Max_Legacy_SPD			BLINK	Bridge		RSVD	
0111	Page_Select			RSVD	Port_Select			

Table 10-2. Base Register Field Description

FIELD	SIZE	TYPE	DESCRIPTION
Physical_ID	6	Rd	Physical identification. This field contains the physical address ID of this node determined during self-ID. The Physical_ID is invalid after a bus reset until the self-ID has completed as indicated by an unsolicited register 0 status transfer from the PHY to the LLC.
R	1	Rd	Root. This bit indicates that this node is the root node. The R bit is reset to 0 by bus reset, and is set to 1 during tree-ID if this node becomes root.
CPS	1	Rd	Cable-power-status. This bit indicates the state of the CPS input terminal. The CPS terminal is normally tied to serial bus cable power through a 400-kΩ resistor. A 0 in this bit indicates that the cable power voltage has dropped below its threshold for ensured reliable operation.
RHB	1	Rd/Wr	Root-holdoff bit. This bit instructs the PHY to attempt to become root after the next bus reset. The RHB bit is reset to 0 by a hardware reset and is unaffected by a bus reset. If two nodes on a single bus have their root holdoff bit set, the result is not defined. To prevent two nodes from having their root-holdoff bit set, this bit must only be written using a PHY configuration packet.
IBR	1	Rd/Wr	Initiate bus reset. This bit instructs the PHY to initiate a long (166 μs) bus reset at the next opportunity. Any receive or transmit operation in progress when this bit is set completes before the bus reset is initiated. The IBR bit is reset to 0 after a hardware reset or a bus reset. Care must be exercised when writing to this bit to not change the other bits in this register. It is recommended thatwhenever possible a bus reset be initiated using the ISBR bit and not the IBR bit.
Gap_Count	6	Rd/Wr	Arbitration gap count. This value sets the subaction (fair) gap, arb-reset gap, and arb-delay times. The gap count can be set either by a write to the register, or by reception or transmission of a PHY_CONFIG packet. The gap count is reset to 3Fh by hardware reset or after two consecutive bus resets without an intervening write to the gap count register (either by a write to the PHY register or by a PHY_CONFIG packet). It is strongly recommended that this field only be changed using PHY configuration packets.
Extended	3	Rd	Extended register definition. For the XIO2213B, this field is 111b, indicating that the extended register set is implemented.
Num_Ports	4	Rd	Number of ports. This field indicates the number of ports implemented in the PHY. For the XIO2213B, this field is 3.
PHY_Speed	3	Rd	PHY speed capability. This field is no longer used. For the XIO2213B PHY, this field is 111b. Speeds for 1394b PHYs must be checked on a port-by-port basis.
Delay	4	Rd	PHY repeater data delay. This field indicates the worst-case repeater data delay of the PHY, expressed as 144 + (delay 20) ns. For the XIO2213B, this field is 02h. This value is the repeater delay for the S400B case, which is slower than the S800B or 1394a cases. Since the IEEE Std 1394b-2002 PHY register set only has a single field for the delay parameter, the slowest value is used. If a network uses only S800B or 1394a connections, a delay value of 00h may be used. The worst-case PHY repeater delay is 197 ns for S400B and 127 ns for S800B cable speeds (trained, raw bit speed).

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Table 10-2. Base Register Field Description (continued)

FIELD	SIZE	TYPE	DESCRIPTION
LCtrl	1	Rd/Wr	Link-active status control. This bit controls the indicated active status of the LLC section reported in the self-ID packet. The logical AND of this bit and the LPS active status is replicated in the L field (bit 9) of the self-ID packet. The LLC bit in the node self-ID packet is set active only if both the LPS input is active and the LCtrl bit is set. The LCtrl bit provides a software controllable means to indicate the LLC self-ID active status in lieu of using the LPS input terminal. The LCtrl bit is set to 1 by hardware reset and is unaffected by bus reset. Note: The state of the PHY-section/LLC-section interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit. If the PHY-section/LLC-section interface is operational as determined by the LPS input being active, received packets and status information continue to be presented on the interface, and any requests indicated on the LREQ input are processed, even if the LCtrl bit is cleared to 0.
C	1	Rd/Wr	Contender status. This bit indicates that this node is a contender for the bus or isochronous resource manager. This bit is replicated in the c field (bit 20) of the self-ID packet. This bit is set to 0 on hardware reset. After hardware reset, this bit can only be set via a software register write. This bit is unaffected by a bus reset.
Jitter	3	Rd	PHY-section repeater jitter. This field indicates the worst-case difference between the fastest and slowest repeater data delay, expressed as (jitter + 1) 20 ns. For the XIO2213B, this field is 0.
Pwr_Class	3	Rd/Wr	Node power class. This field indicates this node power consumption and source characteristics and is replicated in the pwr field (bits 21-23) of the self-ID packet. This field is reset to the state specified by the PC0-PC2 input terminals on a hardware reset, and is unaffected by a bus reset.
WDIE	1	Rd/Wr	Watchdog interrupt enable. This bit, if set to 1, enables the port interrupt event (PIE) bit to be set when resume operations begin on any port, or when any of the CTOI, CPSI, or STOI interrupt bits are set and the PHY-section/LLC-section interface is nonoperational. This bit is reset to 0 by hardware reset and is unaffected by bus reset.
ISBR	1	Rd/Wr	Initiate short arbitrated bus reset. This bit, if set to 1, instructs the XIO2213B to initiate a short (1.3-ms) arbitrated bus reset at the next opportunity. This bit is reset to 0 by a bus reset. It is recommended that short bus reset is the only reset type initiated by software. IEC 61883-6 requires that a node initiate short bus resets to minimize any disturbance to an audio stream. Note: Legacy IEEE Std 1394-1995-compliant PHYs are not capable of performing short bus resets. Therefore, initiation of a short bus reset in a network that contains such a legacy device results in a long bus reset being performed.
CTOI	1	Rd/Wr	Configuration time-out interrupt. This bit is set to 1 when the arbitration controller times out during tree-ID start, and might indicate that the bus is configured in a loop. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit. If the CTOI and WDIE bits are both set and the LLC is or becomes inactive, the PHY section activates the LKON output to notify the LLC section to service the interrupt. Note: If the network is configured in a loop, only those nodes that are part of the loop generate a configuration time-out interrupt. Instead, all other nodes time out waiting for the tree-ID and/or self-ID process to complete and then generate a state time-out interrupt and bus reset. This bit is only set when the bus topology includes IEEE Std 1394a-2000 nodes; otherwise, IEEE Std 1394b-2002 loop healing prevents loops from being formed in the topology.
CPSI	1	Rd/Wr	Cable-power-status interrupt. This bit is set to 1 whenever the CPS input transitions from high to low, indicating that cable power might be too low for reliable operation. This bit is reset to 1 by hardware reset. It can be cleared by writing a 1 to this register bit. If the CPSI and WDIE bits are both set and the LLC section is or becomes inactive, the PHY section activates the LKON output to notify the LLC section to service the interrupt.
STOI	1	Rd/Wr	State time-out interrupt. This bit indicates that a state time-out has occurred (which also causes a bus reset to occur). This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit. If the STOI and WDIE bits are both set and the LLC is, or becomes, inactive, the PHY section activates the LKON output to notify the LLC section to service the interrupt.
PEI	1	Rd/Wr	Port event interrupt. This bit is set to 1 on any change in the connected, bias, disabled, or fault bits for any port for which the port interrupt enable (PIE) bit is set. Additionally, if the resuming port interrupt enable (WDIE) bit is set, the PEI bit is set to 1 at the start of resume operations on any port. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit.
EAA	1	Rd/Wr	Enable accelerated arbitration. This bit enables the XIO2213B to perform the various arbitration acceleration enhancements defined in IEEE Std 1394a-2000 (ack-accelerated arbitration, asynchronous fly-by concatenation, and isochronous fly-by concatenation). This bit is reset to 0 by hardware reset and is unaffected by bus reset. This bit has no effect when the device is operating in IEEE Std 1394b-2002 mode.
EMC	1	Rd/Wr	Enable multispeed concatenated packets. This bit enables the XIO2213B to transmit concatenated packets of differing speeds in accordance with the protocols defined in IEEE Std 1394a-2000. This bit is reset to 0 by hardware reset and is unaffected by bus reset. This bit has no effect when the device is operating in IEEE Std 1394b-2002 mode.

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Table 10-2. Base Register Field Description (continued)

FIELD	SIZE	TYPE	DESCRIPTION
Max_Legacy_SPD	3	Rd	Maximum legacy path speed. This field holds the maximum speed capability of any legacy node (IEEE Std 1394a-2000 or 1394-1995 compliant) as indicated in the self-ID packets received during bus initialization. Encoding is the same as for the PHY_SPEED field (but limited to S400 maximum).
BLINK	1	Rd	Beta-mode link. This bit indicates that a beta-mode-capable LLC section is attached to the PHY section. This bit is set by the BMODE input terminal on the XIO2213B and should be set to 1.
Bridge	2	Rd/Wr	Bridge. This field controls the value of the bridge (brdg) field in the self-ID packet. The power reset value is 0. Details for when to set these bits are specified in the IEEE Std 1394.1 bridging specification.
Page_Select	3	Rd/Wr	Page select. This field selects the register page to use when accessing register addresses 8-15. This field is reset to 0 by a hardware reset and is unaffected by bus reset.
Port_Select	4	Rd/Wr	Port select. This field selects the port when accessing per-port status or control (for example, when one of the port status/control registers is accessed in page 0). Ports are numbered starting at 0. This field is reset to 0 by hardware reset and is unaffected by bus reset.

The port status page provides access to configuration and status information for each of the ports. The port is selected by writing 0 to the Page_Select field and the desired port number to the Port_Select field in base register 7. Table 10-3 shows the configuration of the port-status page registers, and Table 10-4 gives the corresponding field descriptions. If the selected port is not implemented, all registers in the port status page are read as 0.

Table 10-3. Page 0 (Port Status) Register Description

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Astat		Bstat		Ch	Con	RxOK	Dis
1001	Negotiated_speed			PIE	Fault	Standby_fault	Disscrm	B_Only
1010	DC_connected	Max_port_speed (011b)			LPP	Cable_speed		
1011	Connection_unreliable	Reserved			Beta_mode	Reserved		
1100	Port_error							
1101	Reserved					Loop_disable	In_standby	Hard_disable
1110	Reserved							
1111	Reserved							

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Table 10-4. Page 0 (Port Status) Register Field Description

FIELD	SIZE	TYPE	DESCRIPTION
Astat	2	Rd	TPA line state. This field indicates the instantaneous TPA line state of the selected port, encoded as: Code Arbitration Value 11 Z 10 1 01 0 00 Invalid
Bstat	2	Rd	TPB line state. This field indicates the TPB line state of the selected port. This field has the same encoding as the Astat field.
Ch	1	Rd	Child/parent status. A 1 indicates that the selected port is a child port. A 0 indicates that the selected port is the parent port. A disconnected, disabled, or suspended port is reported as a child port. The Ch bit is invalid after a bus reset until tree-ID has completed.
Con	1	Rd	Debounced port connection status. This bit indicates that the selected port is connected. The connection must be stable for the debounce time of approximately 341 ms for the Con bit to be set to 1. The Con bit is reset to 0 by hardware reset and is unaffected by bus reset. Note: The Con bit indicates that the port is physically connected to a peer PHY, but this does not necessarily mean that the port is active. For IEEE Std 1394b-2002-coupled connections, the Con bit is set when a port detects connection tones from the peer PHY and operating-speed negotiation is completed.
RxOK	1	Rd	Receive OK. In IEEE Std 1394a-2000 mode, this bit indicates the reception of a debounced TPBias signal. In beta mode, this bit indicates the reception of a continuous electrically valid signal. Note: RxOK is set to false during the time that only connection tones are detected in beta mode.
Dis	1	RdWr	Port disabled control. If this bit is 1, the selected port is disabled. The Dis bit is reset to 0 by hardware reset (all ports are enabled for normal operation following hardware reset). The Dis bit is not affected by bus reset. When this bit is set, the port cannot become active; however, the port still tones, but does not establish an active connection.
Negotiated_speed	1	Rd	Negotiated speed. Indicates the maximum speed negotiated between this port and its immediately connected port. The encoding is as for Max_port_speed. It is set on connection when in beta mode, or to a value established during self-ID when in IEEE Std 1394a-2000 mode.
PIE	1	RdWr	Port event interrupt enable. When this bit is 1, a port event on the selected port sets the port event interrupt (PEI) bit and notifies the link. This bit is reset to 0 by a hardware reset and is unaffected by bus reset.
Fault	1	Rd/Wr	Fault. This bit indicates that a resume-fault or suspend-fault has occurred on the selected port, and that the port is in the suspended state. A resume-fault occurs when a resuming port fails to detect incoming cable bias from its attached peer. A suspend-fault occurs when a suspending port continues to detect incoming cable bias from its attached peer. Writing 1 to this bit clears the Fault bit to 0. This bit is reset to 0 by hardware reset and is unaffected by bus reset.
Standby_fault	1	Rd/Wr	Standby fault. This bit is set to 1 if an error is detected during a standby operation and cleared on exit from the standby state. A write of 1 to this bit or receipt of the appropriate remote command packet clears it to 0. When this bit is cleared, standby errors are cleared.
Disscrm	1	Rd/Wr	Disable scrambler. If this bit is set to 1, the data sent during packet transmission is not scrambled.
B_Only	1	Rd	Beta-mode operation only. For the XIO2213B, this bit is set to 0 for all ports.
DC_connected	1	Rd	If this bit is set to 1, the port has detected a dc connection to the peer port by means of an IEEE Std 1394a-2000-style connect-detect circuit.

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Table 10-4. Page 0 (Port Status) Register Field Description (continued)

FIELD	SIZE	TYPE	DESCRIPTION
Max_port_speed	3	Rd/Wr	Maximum port speed. The maximum speed at which a port is allowed to operate in beta mode. The encoding is: 000 = S100 001 = S200 010 = S400 011 = S800 100 = S1600 101 = S3200 110 = Reserved 111 = Reserved An attempt to write to the register with a value greater than the hardware capability of the port results in the value for the maximum speed of which the port is capable being stored in the register. The port uses this register only when a new connection is established in the beta mode. The power reset value is the maximum speed capable of the port. Software can modify this value to force a port to train at a lower than maximum, but no lower than minimum speed.
LPP	1	Rd	Local plug present. This flag is set permanently to 1.
Cable_speed	3	Rd	Cable speed. This variable is set to the value for the maximum speed that the port is capable of. The encoding is the same as for Max_port_speed.
Connection_unreliable	1	Rd/Wr	Connection unreliable. If this bit is set to 1, a beta-mode speed negotiation has failed or synchronization has failed. A write of 1 to this field resets the value to 0.
Beta_mode	1	Rd	Operating in beta mode. If this bit is 1, the port is operating in beta mode; it is equal to 0 otherwise (that is, when operating in IEEE Std 1394a-2000 mode, or when disconnected). If Con is 1, RxOK is 1, and Beta_mode is 0, the port is active and operating in the IEEE Std 1394a-2000 mode.
Port_error	8	Rd/Wr	Port error. Incremented whenever the port receives an invalid codeword, unless the value is already 255. Cleared when read (including being read by means of a remote access packet). Intended for use by a single bus-wide diagnostic program.
Loop_disable	1	Rd	Loop disable. This bit is set to 1 if the port has been placed in the loop-disable state as part of the loop-free build process (the PHYs at either end of the connection are active, but if the connection itself were activated, a loop would exist). Cleared on bus reset and on disconnection.
In_standby	1	Rd	In standby. This bit is set to 1 if the port is in standby power-management state.
Hard_disable	1	Rd/Wr	Hard disable. No effect unless the port is disabled. If this bit is set to 1, the port does not maintain connectivity status on an ac connection when disabled. The values of the Con and RxOK bits are forced to 0. This flag can be used to force renegotiation of the speed of a connection. It can also be used to place the device into a lower-power state because when hard disabled, a port no longer tones to maintain IEEE Std 1394b-2002 ac-connectivity status.

The vendor ID page identifies the vendor/manufacturer and compliance level. The page is selected by writing 1 to the Page_Select field in base register 7. Table 10-5 shows the configuration of the vendor ID page, and Table 10-6 shows the corresponding field descriptions.

Table 10-5. Page 1 (Vendor ID) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Compliance							
1001	Reserved							
1010	Vendor_ID[0]							
1011	Vendor_ID[1]							
1100	Vendor_ID[2]							
1101	Product_ID[0]							
1110	Product_ID[1]							
1111	Product_ID[2]							

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Table 10-6. Page 1 (Vendor ID) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Compliance	8	Rd	Compliance level. For the XIO2213B, this field is 02h, indicating compliance with the IEEE Std 1394b-2002 specification.
Vendor_ID	24	Rd	Manufacturers organizationally unique identifier (OUI). For the XIO2213B, this field is 08 0028h (TI) (the MSB is at register address 1010b).
Product_ID	24	Rd	Product identifier. For the XIO2213B, this field is 83_13_07h.

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The vendor dependent page provides access to the special control features of the XIO2213B, as well as configuration and status information used in manufacturing test and debug. This page is selected by writing 7 to the Page_Select field in base register 7. Table 10-7 shows the configuration of the vendor dependent page, and Table 10-8 shows the corresponding field descriptions.

Table 10-7. Page 7 (Vendor Dependent) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Reserved							
1001	Reserved for test							
1010	Reserved for test							
1011	Reserved for test							
1100	Reserved for test							
1101	Reserved for test							
1110	SWR	Reserved for test						
1111	Reserved for test							

Table 10-8. Page 7 (Vendor Dependent) Register Field Descriptions

FIELD	SIZE	TYPE	Description
SWR	1	Rd/Wr	Software hard reset. Writing a 1 to this bit forces a hard reset of the PHY section (same effect as momentarily asserting the $\overline{\text{RESET}}$ terminal low). This bit is always read as a 0.

10.2 PHY Section Application Information

10.2.1 Power Class Programming

The PC0–PC2 terminals are programmed to set the default value of the power class indicated in the pwr field (bits 21–23) of the transmitted self-ID packet. Descriptions of the various power classes are given in Table 10-9. The default power-class value is loaded following a hardware reset, but is overridden by any value subsequently loaded into the Pwr_Class field in register 4.

Table 10-9. Power Class Register Description

PC[0:2]	DESCRIPTION
000	Node does not need power and does not repeat power.
001	Node is self powered and provides a minimum of 15 W to the bus.
010	Node is self powered and provides a minimum of 30 W to the bus.
011	Node is self powered and provides a minimum of 5 W to the bus.
100	Node may be powered from the bus and is using up to 3 W; no additional power is needed to enable the link. The node may also provide power to the bus. The amount of bus power that it provides can be found in the configuration ROM.
101	Reserved for future standardization
110	Node is powered from the bus and uses up to 3 W. An additional 3 W is needed to enable the link.
111	Node is powered from the bus and uses up to 3 W. An additional 7 W is needed to enable the link.

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10.2.2 Power-Up Reset

To ensure proper operation of the XIO2213B PHY section, the $\overline{\text{RESET}}$ terminal must be asserted low for a minimum of 2 ms from the time that DVDD, AVDD, and PLLVDD power reaches the minimum required supply voltage and the input clock is valid. If a fundamental-mode crystal is used rather than an oscillator, the start-up time parameter may be set to zero. When using a passive capacitor on the $\overline{\text{RESET}}$ terminal to generate a power-on-reset signal, the minimum reset time is ensured if the value of the capacitor satisfies the following equation (the value must be no smaller than approximately 0.1 µF):

C_{min} = (0.0077 T) + 0.085 + (external_oscillator_start-up_time 0.05)

Where:

C_{min} = Minimum capacitance on $\overline{\text{RESET}}$ terminal (F)

T = V_{DD} ramp time, 10% to 90% (ms)

external_oscillator_start-up_time = Time from power applied to external oscillator until oscillator outputs a valid clock (ms)

10.2.3 Crystal Oscillator Selection

The XIO2213B is designed to use an external 98.304-MHz crystal oscillator connected to the XI terminal to provide the reference clock. This clock, in turn, drives a PLL circuit that generates the various clocks required for transmission and resynchronization of data at the S100 through S800 media data rates.

A variation of less than ±100 ppm from nominal for the media data rates is required by IEEE Std 1394. Adjacent PHYs may, therefore, have a difference of up to 200 ppm from each other in their internal clocks, and PHYs must be able to compensate for this difference over the maximum packet length. Larger clock variations can cause resynchronization overflows or underflows, resulting in corrupted packet data.

For the XIO2213B, the PCLK output can be used to measure the frequency accuracy and stability of the internal oscillator and PLL from which it is derived. The frequency of the PCLK output must be within ±100 ppm of the nominal frequency of 98.304 MHz.

The following are some typical specifications for an oscillator used with the XIO2213B, in order to achieve the required frequency accuracy and stability:

- RMS jitter of 5 ps or less
- RMS phase-noise jitter of 1 ps or less over the range 12 kHz to 20 MHz or higher
- Frequency tolerance at 25°C: Total frequency variation for the complete circuit is ±100 ppm. A device with ±30-ppm or ±50-ppm frequency tolerance is recommended for adequate margin.
- Frequency stability (over temperature and age): A device with ±30-ppm or ±50-ppm frequency stability is recommended for adequate margin.

  The total frequency variation must be kept below ±100 ppm from nominal, with some allowance for error introduced by board and device variations. Trade-offs between frequency tolerance and stability may be made, as long as the total frequency variation is less than ±100 ppm. For example, the frequency tolerance of the crystal may be specified at 50 ppm and the temperature tolerance may be specified at 30 ppm to give a total of 80-ppm possible variation due to the oscillator alone. Aging also contributes to the frequency variation. It is strongly recommended that part of the verification process for the design is to measure the frequency of the PCLK output of the PHY section. This should be done using a frequency counter with an accuracy of six digits or better.

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10.2.4 Bus Reset

It is recommended that whenever the user has a choice, the user should initiate a bus reset by writing to the initiate short bus reset (ISBR) bit (bit 1, PHY register 0101b). Care must be taken not to change the value of any of the other writeable bits in this register when the ISBR bit is written to.

In the XIO2213B, the initiate bus reset (IBR) bit can be set to 1 in order to initiate a bus reset and initialization sequence; however, it is recommended to use the ISBR bit instead. The IBR bit is located in PHY register 1 along with the root holdoff bit (RHB) and gap count. As required by the IEEE Std 1394b-2002 Supplement, this configuration maintains compatibility with older TI PHY designs that were based on either the suggested register set defined in Annex J of IEEE Std 1394-1995 or the IEEE Std 1394a-2000 Supplement. Therefore, whenever the IBR bit is written, the RHB and gap count are also necessarily written.

It is recommended that the RHB and gap count only be updated by PHY configuration packets. The XIO2213B is IEEE Std 1394a-2000 and IEEE Std 1394b-2002 compliant and, therefore, both the reception and transmission of PHY configuration packets cause the RHB and gap count to be loaded, unlike older IEEE Std 1394-1995-compliant PHYs that decode only received PHY configuration packets.

The gap count is set to the maximum value of 63 after two consecutive bus resets without an intervening write to the gap count, either by a write to PHY register 1 or by a PHY configuration packet. This mechanism allows a PHY configuration packet to be transmitted and then a bus reset initiated to verify that all nodes on the bus have updated their RHBs and gap counts, without having the gap count set back to 63 by the bus reset. The subsequent connection of a new node to the bus, which initiates a bus reset, then causes the gap count of each node to be set to 63. Note, however, that if a subsequent bus reset is instead initiated by a write to register 1 to set the IBR bit, all other nodes on the bus have their gap counts set to 63, while this nodes gap count remains set to the value just loaded by the write to PHY register 1.

Therefore, in order to maintain consistent gap counts throughout the bus, the following rules apply to the use of the IBR bit, RHB, and gap count in PHY register 1:

- Following the transmission of a PHY configuration packet, a bus reset must be initiated in order to verify that all nodes have correctly updated their RHBs and gap counts, and to ensure that a subsequent new connection to the bus causes the gap count to be set to 63 on all nodes in the bus. If this bus reset is initiated by setting the IBR bit to 1, the RHB and gap count register must also be loaded with the correct values consistent with the just-transmitted PHY configuration packet. In the XIO2213B, the RHB and gap count have been updated to their correct values on the transmission of the PHY configuration packet, so these values can first be read from register 1 and then rewritten.
- Other than to initiate the bus reset that must follow the transmission of a PHY configuration packet, when the IBR bit is set to 1 in order to initiate a bus reset, the gap count must also be set to 63 to be consistent with other nodes on the bus, and the RHB must be maintained with its current value.
- The PHY register 1 must not be written to except to set the IBR bit. The RHB and gap count must not be written without also setting the IBR bit to 1.
- To avoid these problems, all bus resets initiated by software must be initiated by writing the ISBR bit (bit 1 PHY register 0101b). Care must be taken to not change the value of any of the other writeable bits in this register when the ISBR bit is written to. Also, the only means to change the gap count of any node must be by means of the PHY configuration packet, which changes all nodes to the same gap count.

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11 Electrical Characteristics

11.1 Absolute Maximum Ratings(1)

over operating temperature range (unless otherwise noted)

			VALUE	UNIT
V_{SUP_33}	Supply voltage range	DVDD_33, V_{DDA_33}, V_{DDA_33}, V_{DDPLL_33}, $V_{DD_33_COMB}$, $V_{DD_33_COMBIO}$	0.3 to 3.6	V
V_{SUP_15}	Supply voltage range	V_{DD_15}, V_{DDA_15}, V_{PP}, $V_{DDPL\ L}$, $V_{DD_15_COMB}$	0.5 to 1.65	V
V_{CORE_195}	Supply voltage range	PLLVDD_CORE, DVDD_CORE	0.5 to 2.05	V
V_I	Input voltage range	PCIe (RX)	0.5 to V_{SUP_33} + 0.5	V
		PCIe REFCLK (single ended)	0.5 to V_{SUP_15} + 0.5	
		PCIe REFCLK (differential)	0.5 to V_{SUP_33} + 0.5	
		Miscellaneous 3.3-V I/O	0.5 to V_{SUP_33} + 0.5	
		PHY interface	0.5 to V_{SUP_33} + 0.5	
V_O	Output voltage range	PCIe (TX)	0.5 to V_{SUP_15} + 0.5	V
		Miscellaneous 3.3-V I/O	0.5 to V_{SUP_33} + 0.5	
		PHY interface	0.5 to V_{SUP_33} + 0.5	
	Input clamp current (V_I < 0 or V_I > VDD)(2)		20	mA
	Output clamp current (V_O < 0 or V_O > VDD)(3)		20	mA
T_{stg}	Storage temperature range		-65 to 150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Applies for external input and bidirectional buffers. V_I < 0 or V_I > V_{DD} or V_I > V_{CCP}
(3) Applies for external input and bidirectional buffers. V_O < 0 or V_O > V_{DD} or V_O > V_{CCP}

11.2 Recommended Operating Conditions

		OPERATION	MIN	NOM	MAX	UNIT
V_{SUP_15}	Supply voltage	1.5 V	1.35	1.5	1.65	V
V_{SUP_33}	Supply voltage (I/O)	3.3 V	3	3.3	3.6	V
V_{CORE_195}	Supply voltage	1.95 V	1.85	1.95	2.05	V
T_A	Operating ambient temperature		0	25	70	°C
		Industrial	-40		85	
T_J	Junction temperature		0	25	105	°C
θ_{JA}	Junction-to-free-air thermal resistance	Low K JEDEC test board, 1s, no air flow - ZAY		85		°C/W
		Low K JEDEC test board, 1s, no air flow - ZAJ		88		°C/W
		High K JEDEC test board, 2s2p no air flow - ZAY		65		°C/W
		High K JEDEC test board, 2s2p no air flow - ZAJ		42.1		°C/W
		High K JEDEC test board, 2s2p 200 LFM - ZAY		52		°C/W
		High K JEDEC test board, 2s2p 200 LFM - ZAJ		33		°C/W
θ_{JC}	Junction-to-case thermal resistance	Cu cold plate measurement process - ZAY		13		°C/W
		Cu cold plate measurement process - ZAJ		13		°C/W

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Recommended Operating Conditions *(continued)*

		OPERATION	MIN	NOM	MAX	UNIT
θ_{JB}	Junction-to-board thermal resistance	EIA/JESD 51-8 ZAY		35		°C/W
		EIA/JESD 51-8 ZAJ		27		°C/W
Ψ_{JT}	Junction-to-top of package	EIA/JESD 51-2 ZAY		0.1		°C/W
		EIA/JESD 51-2 ZAJ		0.13		°C/W
Ψ_{JB}	Junction-to-board	EIS/JESD 51-6 ZAY		29.7		°C/W
		EIS/JESD 51-6 ZAJ		22.1		°C/W

11.3 PCIe Differential Transmitter Output Ranges

TXP and TXN

PARAMETER		MIN	NOM	MAX	UNIT	COMMENTS
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps 300 ppm. UI does not account for SSC dictated variations. (1)
$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	0.8		1.2	V	$V_{TX-DIFFp-p} = 2*\|V_{TXP} - V_{TXN}\|$ (2)
$V_{TX-DE-RATIO}$	Deemphasized differential output voltage (ratio)	3.0	3.5	4.0	dB	This is the ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. (2)
TTX-EYE	Minimum TX eye width	0.75			UI	The maximum transmitter jitter can be derived as $T_{TXMAX-JITTER} = 1 – T_{TX-EYE} = 0.3$ UI. (2) (3)
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between jitter median and maximum deviation from the median			0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to recovered TX UI. A recovered TX UI is calculated over 3500 consecutive UIs of sample data. Jitter is measured using all edges of the 250 consecutive UIs in the center of the 3500 UIs used for calculating the TX UI. (2) (3)
$T_{TX-RISE}$ $T_{TX-FALL}$	P/N TX output rise/fall time	0.125			UI	(2) (4)
$V_{TX-CM-ACp}$	RMS ac peak common-mode output voltage			20	mV	$V_{TX-CM-ACp}$ = RMS(|V_{TX}P + V_{TXN}|/2 $V_{TX-CM-DC}$) $V_{TX-CM-DC}$ = DC(avg) of |V_{TXP} + V_{TXN}|/2 (2)
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of dc common-mode voltage during L0 and electrical idle	0		100	mV	|$V_{TX-CM-DC}$ $V_{TX-CM-Idle-DC}$| 100 mV $V_{TX-CM-DC}$ = $DC_{(avg)}$ of |V_{TXP} + V_{TXN}|/2 [during L0] $V_{TX-CM-Idle-DC}$ = $DC_{(avg)}$ of |V_{TXP} + V_{TXN}|/2 (during electrical idle) (2)
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of dc common-mode voltage between P and N	0		25	mV	|$V_{TXP-CM-DC}$ $V_{TXN-CM-DC}$| 25 mV when $V_{TXP-CM-DC}$ = $DC_{(avg)}$ of |V_{TXP}| $V_{TXN-CM-DC}$ = $DC_{(avg)}$ of |V_{TXN}| (2)
$V_{TX-IDLE-DIFFp}$	Electrical idle differential peak output voltage	0		20	mV	$V_{TX-IDLE-DIFFp}$ = |$V_{TXP-Idle}$ $V_{TXN-Idle}$| 20 mV (2)
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during receiver detection			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present
$V_{TX-DC-CM}$	TX dc common-mode voltage	0		3.6	V	The allowed dc common-mode voltage under any condition
$I_{TX-SHORT}$	TX short-circuit current limit			90	mA	The total current the transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in electrical idle	50			UI	Minimum time a transmitter must be in electrical Idle. Utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set.

(1) No test load is necessarily associated with this value.
(2) Specified at the measurement point into a timing and voltage compliance test load and measured over any 250 consecutive TX UIs.
(3) A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
(4) Measured between 20% and 80% at transmitter package terminals into a test load for both V_{TXP} and V_{TXN}.

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PCIe Differential Transmitter Output Ranges *(continued)*

TXP and TXN

PARAMETER		MIN	NOM	MAX	UNIT	COMMENTS
$T_{TX-IDLE-SET-to-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set			20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from L0.
$T_{TX-IDLE-to-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an electrical idle condition			20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle.
$RL_{TX-DIFF}$	Differential return loss	10			dB	Measured over 50 MHz to 1.25 GHz(5)
RL_{TX-CM}	Common-mode return loss	6			dB	Measured over 50 MHz to 1.25 GHz(5)
$Z_{TX-DIFF-DC}$	DC differential TX impedance	80	100	120	Ω	TX dc differential mode low impedance
Z_{TX-DC}	Transmitter dc impedance	40			Ω	Required TXP as well as TXN dc impedance during all states
C_{TX}	AC coupling capacitor	75		200	nF	All transmitters are ac coupled and are required on the PWB.

(5) The transmitter input impedance results in a differential return loss greater than or equal to 12 dB and a common-mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 to ground for both the P and N lines. Note that the series capacitors C_{TX} is optional for the return loss measurement.

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11.4 PCIe Differential Receiver Input Ranges

RXP and RXN

PARAMETER		MIN	NOM	MAX	UNIT	COMMENTS
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps 300 ppm. UI does not account for SSC dictated variations(1)
$V_{RX-DIFFp-p}$	Differential input peak-to-peak voltage	0.175		1.200	V	$V_{RX-DIFFp-p} = 2*\|V_{RXP} V_{RXN}, \|$(2)
T_{RX-EYE}	Minimum receiver eye width	0.4			UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver is derived as $T_{RX-MAX-JITTER} = 1 T_{RX-EYE} = 0.6$ UI(2) (3)
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between jitter median and maximum deviation from median			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to recovered TX UI. A recovered TX UI is calculated over 3500 consecutive UIs of sample data. Jitter is measured using all edges of the 250 consecutive UIs in the center of the 3500 UIs used for calculating the TX UI.(2) (3)
$V_{RX-CM-ACp}$	AC peak common-mode input voltage			150	mV	$V_{RX-CM-ACp} = RMS(\|V_{RXP} + V_{RXN}\|/2 V_{RX-CM-DC})$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\|V_{RXP} + V_{RXN}\|/2$(2)
$RL_{RX-DIFF}$	Differential return loss	10			dB	Measured over 50 MHz to 1.25 GHz with the P and N lines biased at +300 mV and 300 mV, respectively(4)
RL_{RX-CM}	Common-mode return loss	6			dB	Measured over 50 MHz to 1.25 GHz with the P and N lines biased at +300 mV and 300 mV, respectively(4)
$Z_{RX-DIFF-DC}$	DC differential input impedance	80	100	120	Ω	RX dc differential mode impedance(4)
Z_{RX-DC}	DC input impedance	40	50	60	Ω	Required RXP as well as RXN dc impedance (50 }20% tolerance)(2) (5)
$Z_{RX-HIGH-IMP-D}$	Powered down dc input impedance	200			k	Required RXP as well as RXN dc impedance when the receiver terminations do not have power(6)
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\|V_{RXP} V_{RXN}\|$ measured at the receiver package terminals
$T_{RX-IDLE-DET-DIFF-ENTER-TIME}$	Unexpected electrical idle enter detect threshold integration time			10	ms	An unexpected electrical idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTER-TIME}$ to signal an unexpected idle condition.

(1) No test load is necessarily associated with this value.
(2) Specified at the measurement point and measured over any 250 consecutive UIs. A test load must be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI is used as a reference for the eye diagram.
(3) A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total UI jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UIs must be used as the reference for the eye diagram.
(4) The receiver input impedance results in a differential return loss greater than or equal to 15 dB with the P line biased to 300 mV and the N line biased to 300 mV and a common-mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 to ground for both the P and N line (i.e., as measured by a vector network analyzer with 50- probes). The series capacitors CTX is optional for the return loss measurement.
(5) Impedance during all link training status state machine (LTSSM) states. When transitioning from a PCIe reset to the detect state (the initial state of the LTSSM) there is a 5-ms transition time before receiver termination values must be met on the unconfigured lane of a port.
(6) The RX dc common-mode impedance that exists when no power is present or PCIe reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

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11.5 PCIe Differential Reference Clock Input Ranges(1)

REFCLK+ and REFCLK–

PARAMETER		MIN	NOM	MAX	UNIT	COMMENTS
$f_{IN-DIFF}$	Differential input frequency		100		MHz	The input frequency is 100 MHz + 300 ppm and 2800 ppm including SSC-dictated variations.
f_{IN-SE}	Single-ended input frequency		125		MHz	The input frequency is 125 MHz + 300 ppm and 300 ppm.
$V_{RX-DIFFp-p}$	Differential input peak-to-peak voltage	0.175		1.200	V	$V_{RX-DIFFp-p} = 2*\|V_{REFCLK+} V_{REFCLK-}\|R$
V_{IH-SE}	REFCLK+ only	0.7 V_{DD_33}		V_{DD_33}	V	Single-ended, reference clock mode high-level input voltage
V_{IL-SE}	REFCLK+ only	0		0.3 V_{DD_33}	V	Single-ended, reference clock mode low-level input voltage
$V_{RX-CM-ACp}$	AC peak common-mode input voltage			140	mV	$V_{RX-CM-ACp}$ = RMS(|$V_{REFCLK+}$ + $V_{REFCLK-}$|/2 $V_{RX-CM-DC}$) $V_{RX-CM-DC}$ = $DC_{(avg)}$ of |$V_{REFCLK+}$ + $V_{REFCLK-}$|/2
Duty cycle		40%		60%		Differential and single-ended waveform input duty cycle
$Z_{RX-DIFF-DC}$	DC differential input impedance		20		k	REFCLK– dc differential mode impedance
Z_{RX-DC}	DC input impedance		20		k	REFCLK+ dc single-ended mode impedance

(1) The XIO2213B is compliant with the defined system jitter models for a PCIe reference clock and associated TX/RX link. These system jitter models are described in the *PCI Express Jitter Modeling*, Revision 1.0 RD document. Any usage of the XIO2213B in a system configuration that does not conform to the defined system jitter models requires the system designer to validate the system jitter budgets.

11.6 Electrical Characteristics Over Recommended Operating Conditions (3.3-V I/O)

$\overline{PERST}$, $\overline{WAKE}$, REFCLK_SEL, $\overline{GRST}$, GPIO[7:0], CNA, PC[2:0], and all RSVD terminals

PARAMETER		OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage(1)	V_{DD_33}		0.7 V_{DD_33}	V_{DD_33}	V
V_{IL}	Low-level input voltage (1)	V_{DD_33}		0	0.3 V_{DD_33}	V
V_I	Input voltage			0	V_{DD_33}	V
V_O	Output voltage(2)			0	V_{DD_33}	V
t_T	Input transition time (t_{rise} and t_{fall})			0	25	ns
V_{hys}	Input hysteresis(3)				0.3 V_{DD_33}	V
V_{OH}	High-level output voltage	V_{DD_33}	I_{OH} = 4 mA	0.8 V_{DD_33}		V
V_{OL}	Low-level output voltage	V_{DD_33}	I_{OL} = 4 mA		0.22 V_{DD_33}	V
I_{OZ}	High-impedance, output current(2)	V_{DD_33}	V_I = 0 to V_{DD_33}		20	µA
I_{OZP}	High-impedance, output current with internal pullup or pulldown resistor(4)	V_{DD_33}	V_I = 0 to V_{DD_33}		100	µA
I_I	Input current(5)	V_{DD_33}	V_I = 0 to V_{DD_33}		1	µA

(1) Applies to external inputs and bidirectional buffers
(2) Applies to external outputs and bidirectional buffers
(3) Applies to $\overline{PERST}$ and $\overline{GRST}$
(4) Applies to $\overline{GRST}$ (pullup resistor) and most GPIOs (pullup resistor)
(5) Applies to external input buffers

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11.7 Electrical Characteristics Over Recommended Operating Conditions (PHY Port Driver)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OD}	1394a differential output voltage	56 Figure 11-1	172		265	mV
	1394b differential output voltage			700		
I_{DIFF}	Driver difference current (TPA+, TPA–, TPB+, TPB–)	Drivers enabled, speed signaling off	1.05 (1)		1.05 (1)	mA
I_{SP200}	Common-mode speed signaling current (TPB+, TPB–)	S200 speed signaling enabled	4.84 (2)		2.53 (2)	mA
I_{SP400}	Common-mode speed signaling current (TPB+, TPB–)	S400 speed signaling enabled	12.4 (2)		8.1 (2)	mA
V_{OFF}	Off-state differential voltage	Drivers disabled			20	mV
V_{CM}	1394b common-mode voltage			1.5		V

(1) Limits defined as algebraic sum of TPA+ and TPA– driver currents. Limits also apply to algebraic sum of TPB+ and TPB– driver currents.
(2) Limits defined as absolute limit of each of TPB+ and TPB– driver currents.

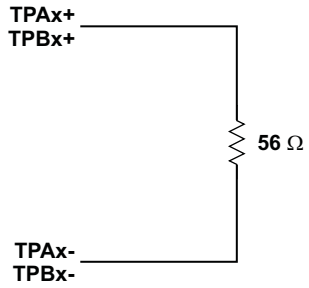


Figure 11-1. Test Load Diagram

11.8 Switching Characteristics for PHY Port Driver

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
	Jitter, transmit	Between TPA and TPB		0.15	ns
	Skew, transmit	Between TPA and TPB		0.1	ns
t_r	TP differential rise time, transmit	10% to 90%, at 1394 connector	0.5	1.2	ns
t_f	TP differential fall time, transmit	90% to 10%, at 1394 connector	0.5	1.2	ns
t_{su}	Setup time, CTL0, CTL1, D1-D7, LREQ until PCLK - 1394a-2000	50% to 50%	2.5		ns
t_h	Hold time, CTL0, CTL1, D1-D7, LREQ after PCLK - 1394a-2000	50% to 50%	0		ns
t_{su}	Setup time, CTL0, CTL1, D1-D7, LREQ until PCLK - 1394b	50% to 50%	2.5		ns
t_h	Hold time, CTL0, CTL1, D1-D7, LREQ after PCLK - 1394b	50% to 50%	1		ns
t_d	Delay time, PCLK until CTL0, CTL1, D1-D7, PINT	50% to 50%	0.5	7	ns

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11.9 Electrical Characteristics Over Recommended Operating Conditions PHY Port Receiver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{ID}	Differential impedance	Drivers disabled	4	7		k
					4	pF
Z_{IC}	Common-mode impedance	Drivers disabled	20			k
					24	pF
V_{TH-R}	Receiver input threshold voltage	Drivers disabled	30		30	mV
V_{TH-CB}	Cable bias detect threshold. TPBx cable inputs	Drivers disabled	0.6		1	V
V_{TH+}	Positive arbitration comparator threshold voltage	Drivers disabled	89		168	mV
V_{TH}	Negative arbitration comparator threshold voltage	Drivers disabled	168		89	mV
$V_{TH-SP200}$	Speed signal threshold	TPBIAS-TPA common mode voltage, drivers disabled	49		131	mV
$V_{TH-SP400}$	Speed signal threshold	TPBIAS-TPA common mode voltage, drivers disabled	314		396	mV

11.10 Jitter/Skew Characteristics for 1394a PHY Port Receiver

PARAMETER		MIN	TYP	MAX	UNIT
1394a Receive input jitter	TPA, TPB cable inputs, S100 operation			1.08	ns
	TPA, TPB cable inputs, S200 operation			0.5	
	TPA, TPB cable inputs, S400 operation			0.315	
1394a Receive input skew	Between TPA and TPB cable inputs, S100 operation			0.8	ns
	Between TPA and TPB cable inputs, S200 operation			0.55	
	Between TPA and TPB cable inputs, S400 operation			0.5	

11.11 Operating, Timing, and Switching Characteristics of XI

PARAMETER		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	0.63 V_{DDA_15}			V
V_{IL}	Low-level input voltage			0.33 V_{DDA_15}	V
	Input clock frequency		98.304		MHz
	Input clock frequency tolerance			<100	ppm
	Input slew rate	0.2		4	V/ns
	Input clock duty cycle	40%		60%	

11.12 Electrical Characteristics Over Recommended Operating Conditions (1394a Miscellaneous I/O)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{TH}	Power status threshold CPS input(1)	400-kΩ resistor(1)	4.7	7.5	V
V_O	TPBIAS output voltage	At rated I_O current	1.665	2.015	V
I_O	TPBIAS output current		5.6	1.3	mA

(1) Measure at cable power side of resistor

12 Glossary

ACRONYM	DEFINITION
BIST	Built-in self test
ECRC	End-to-end cyclic redundancy code
EEPROM	Electrically erasable programmable read-only memory

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GP	General purpose
GPIO	General-purpose input/output
ID	Identification
IF	Interface
IO	Input/output
I2S	Inter IC sound
LPM	Link power management
LSB	Least significant bit
MSB	Most significant bit
MSI	Message signaled interrupts
PCI	Peripheral component interface
PME	PCI power-management event
QoS	Quality of service
RX	Receive
SCL	Serial-bus clock
SDA	Serial-bus data
TC	Traffic class
TLP	Transaction layer packet or protocol
TX	Transmit
VC	Virtual channel
WRR	Weighted round-robin

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XIO2213BIZAY	ACTIVE	NFBGA	ZAY	167	160	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	XIO2213BIZAY	Samples
XIO2213BZAJ	ACTIVE	NFBGA	ZAJ	168	260	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 70	XIO2213B	Samples
XIO2213BZAY	ACTIVE	NFBGA	ZAY	167	160	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 70	XIO2213BZAY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

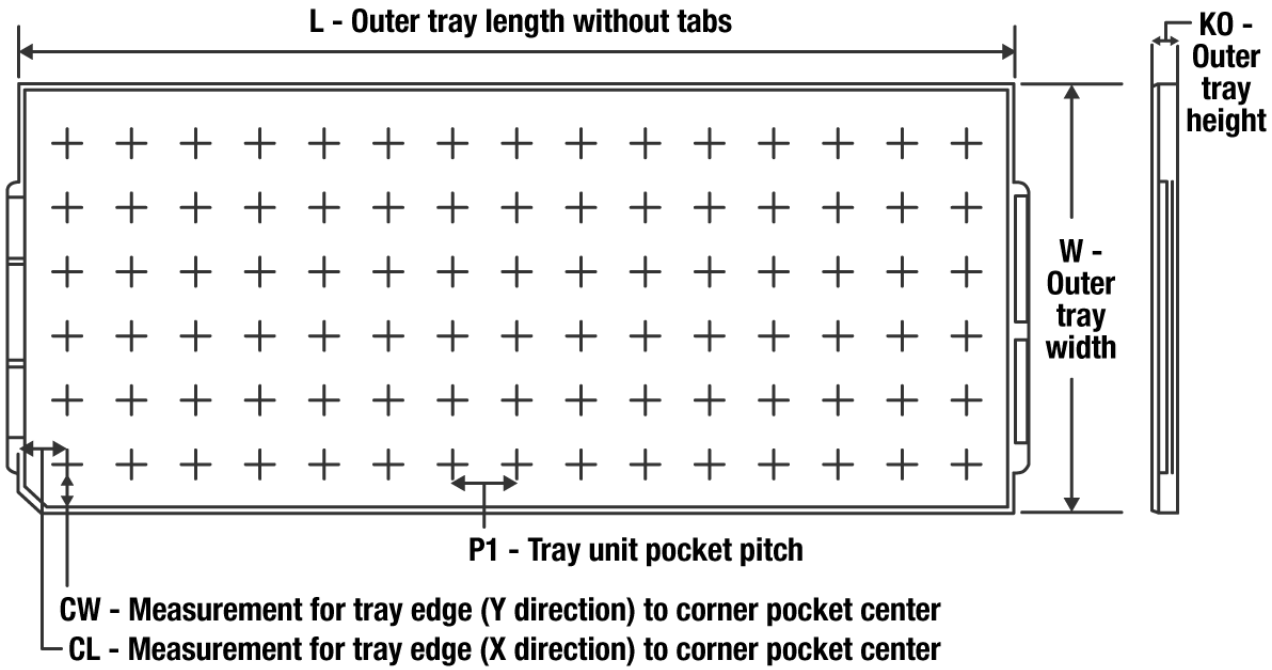
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TRAY

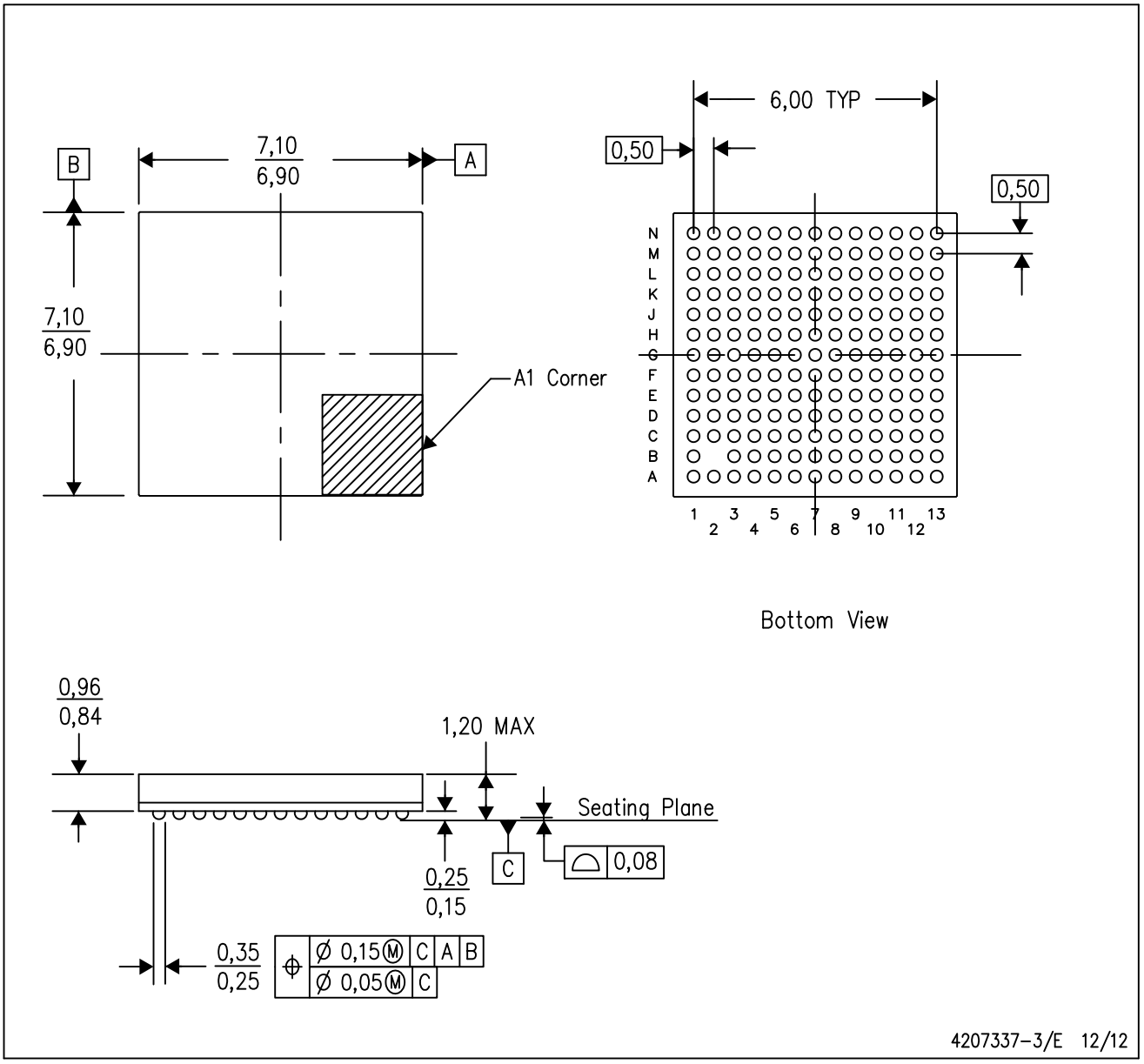


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

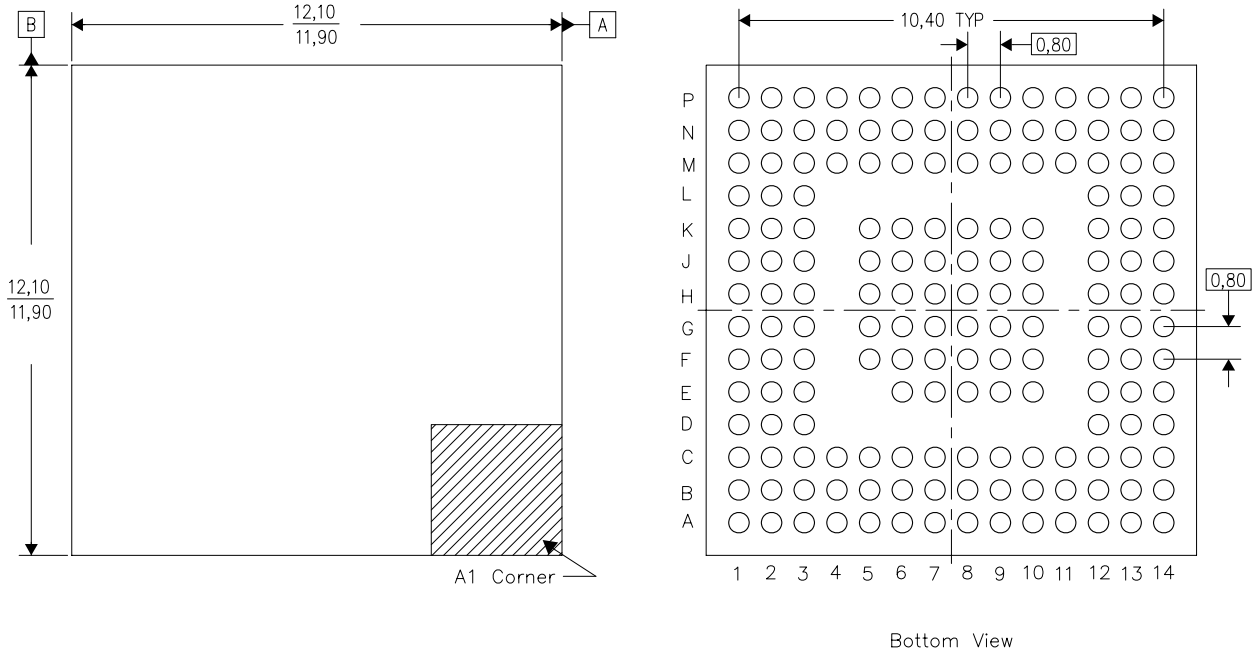
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
XIO2213BIZAY	ZAY	NFBGA	167	160	8 x 20	150	315	135.9	7620	15.4	11.2	19.65
XIO2213BZAJ	ZAJ	NFBGA	168	260	10 x 26	150	315	135.9	7620	11.8	10	10.35
XIO2213BZAY	ZAY	NFBGA	167	160	8 x 20	150	315	135.9	7620	15.4	11.2	19.65

ZAJ (S–PBGA–N168) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

ZAY (S–PBGA–N167) PLASTIC BALL GRID ARRAY



4208324–2/C 09/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
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C. This is a Pb–free solder ball design.

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