TPS56320x 采用 SOT-23 封装的 4.5V 至 17V 输入、3A 同步降压稳压器

1 特性

- TPS563201 和 TPS563208 3A 转换器集成了 95mΩ 和 57mΩ 场效应晶体管 (FET)
- D-CAP2™模式控制，用于快速瞬态响应
- 输入电压范围：4.5V 至 17V
- 输出电压范围：0.76V 至 7V
- 脉冲跳跃模式 (TPS563201) 或持续电流模式 (TPS563208)
- 580kHz 开关频率
- 低关断电流（小于 10μA）
- 2% 反馈电压精度 (25°C)
- 从预偏置输出电压中启动
- 逐周期过流限制
- 断续模式过流保护
- 非锁存欠压保护 (UVP) 和热关断 (TSD) 保护
- 固定软启动时间：1.0ms

2 应用

- 数字电视电源
- 高清 蓝光™光盘播放器
- 网络家庭终端设备
- 数字机顶盒(STB)
- 安全监控

3 说明

TPS563201 和 TPS563208 是采用小外形尺寸晶体管 (SOT)-23 封装的简单易用型 3A 同步降压转换器。

两款器件均经过优化，最大限度地减少了运行所需的外部组件并且可以实现低待机电流。

这些开关模式电源 (SMPS) 器件采用 D-CAP2 模式控制，能够提供快速瞬态响应，并且在无需外部补偿组件的情况下支持诸如高分子聚合物等低等效串联电阻 (ESR) 输出电容以及超低 ESR 陶瓷电容器。

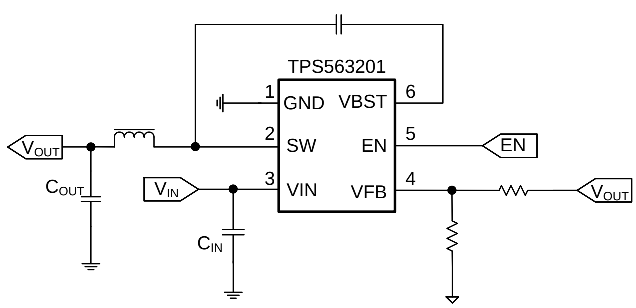
TPS563201 可在脉冲跳跃模式下运行，从而能在轻载运行期间保持高效率。TPS563201 和 TPS563208 采用 6 引脚 1.6mm × 2.9mm SOT (DDC) 封装，额定结温范围为 –40°C 至 125°C。

器件信息(1)

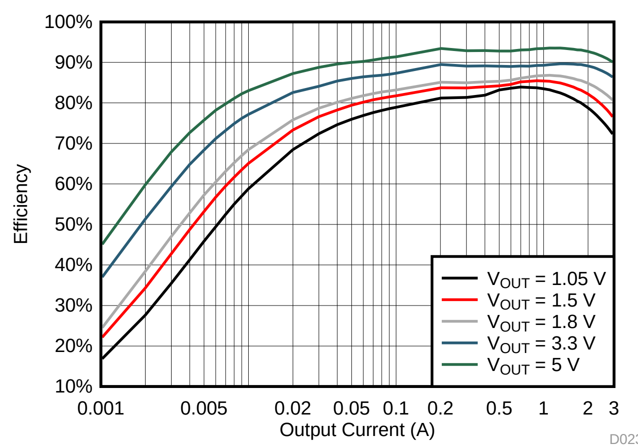
器件型号	封装	封装尺寸（标称值）
TPS563201 TPS563208	DDC (6)	1.60mm x 2.90mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



TPS563201 效率



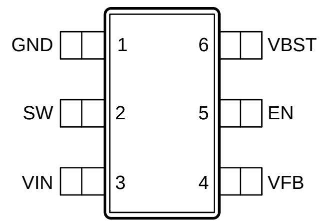
English Data Sheet: SLVSD90

目录

4 修订历史记录

日期	修订版本	注释
2015 年 12 月	*	首次发布。

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	3	I	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 µF capacitor between VBST and SW pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN, EN	–0.3	19	V
	VBST	–0.3	25	V
	VBST (10 ns transient)	–0.3	27	V
	VBST (vs SW)	–0.3	6.5	V
	VFB	–0.3	6.5	V
	SW	–2	19	V
	SW (10 ns transient)	–3.5	21	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage range		4.5		17	V
V_I	Input voltage range	VBST	–0.1		23	V
		VBST (10 ns transient)	–0.1		26	
		VBST (vs SW)	–0.1		6.0	
		EN	–0.1		17	
		VFB	–0.1		5.5	
		SW	–1.8		17	
		SW (10 ns transient)	–3.5		20	
T_J	Operating junction temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS56320x	UNIT
		DDC (SOT)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{VIN}	Operating – non-switching supply current	V_{IN} current, EN = 5 V, V_{FB} = 0.8 V	TPS563201		380	520	µA
			TPS563208		590	750	µA
I_{VINSDN}	Shutdown supply current	V_{IN} current, EN = 0 V			1	10	µA
LOGIC THRESHOLD							
V_{ENH}	EN high-level input voltage	EN		1.6			V
V_{ENL}	EN low-level input voltage	EN				0.8	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V		225	400	900	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE							
V_{FBTH}	V_{FB} threshold voltage	V_O = 1.05 V, I_O = 10 mA, Eco-mode™ operation			774		mV
	V_{FB} threshold voltage	V_O = 1.05 V, continuous mode operation		749	768	787	mV
I_{VFB}	V_{FB} input current	V_{FB} = 0.8 V			0	±0.1	µA
MOSFET							
$R_{DS(on)h}$	High-side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V			95		mΩ
$R_{DS(on)l}$	Low-side switch resistance	T_A = 25°C			57		mΩ
CURRENT LIMIT							
I_{ocl}	Current limit	DC current, V_{OUT} = 1.05 V, L_1 = 1.5 µH		3.3	4.2	5.1	A
THERMAL SHUTDOWN							
T_{SDN}	Thermal shutdown threshold(1)	Shutdown temperature			172		°C
		Hysteresis			37		°C
ON-TIME TIMER CONTROL							
$t_{OFF(MIN)}$	Minimum off time	V_{FB} = 0.5 V			220	310	ns
SOFT START							
Tss	Soft-start time	Internal soft-start time			1.0		ms
FREQUENCY							
F_{sw}	Switching frequency	V_{IN} = 12 V, V_O = 1.05 V, FCCM mode			580		kHz
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION							
V_{UVP}	Output UVP threshold	Hiccup detect (H > L)			65%		
T_{HICCUP_WAIT}	Hiccup on time				1.8		ms
T_{HICCUP_RE}	Hiccup time before restart				15		ms
UVLO							
UVLO	UVLO threshold	Wake up VIN voltage			4.0	4.3	V
		Shutdown VIN voltage		3.3	3.6		V
		Hysteresis VIN voltage			0.4		V

(1) Not production tested.

6.6 Typical Characteristics

V_{IN} = 12 V (unless otherwise noted)

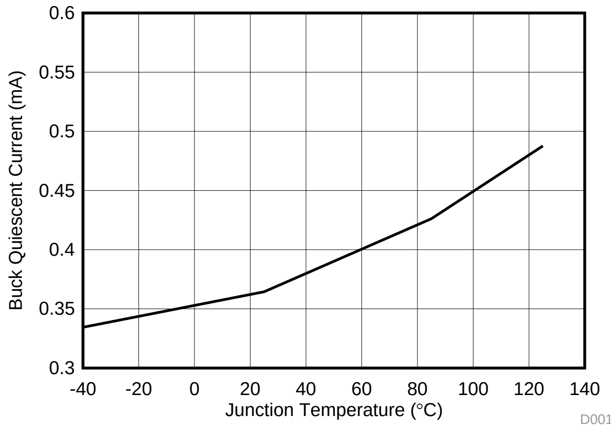


Figure 1. TPS563201 Supply Current vs Junction Temperature

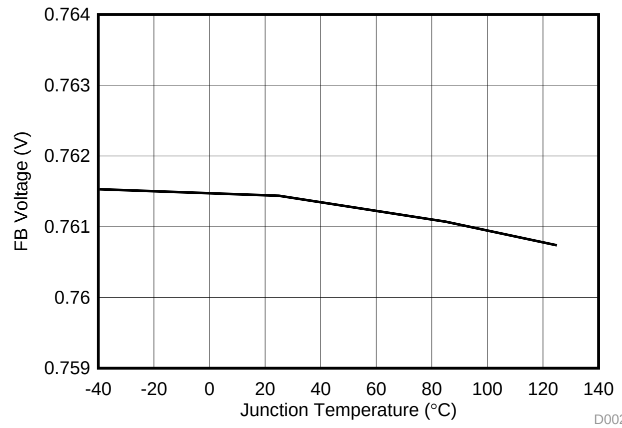


Figure 2. VFB Voltage vs Junction Temperature

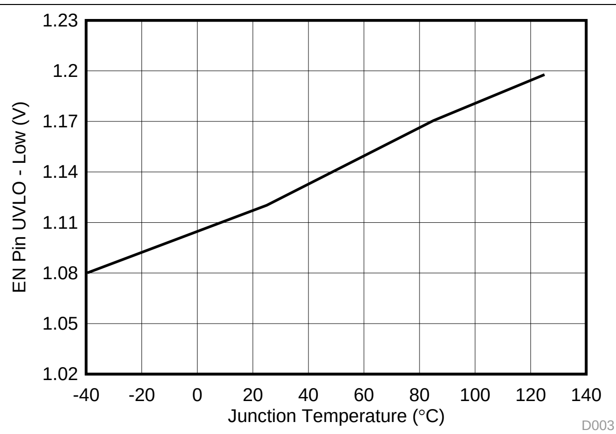


Figure 3. EN Pin UVLO Low Voltage vs Junction Temperature

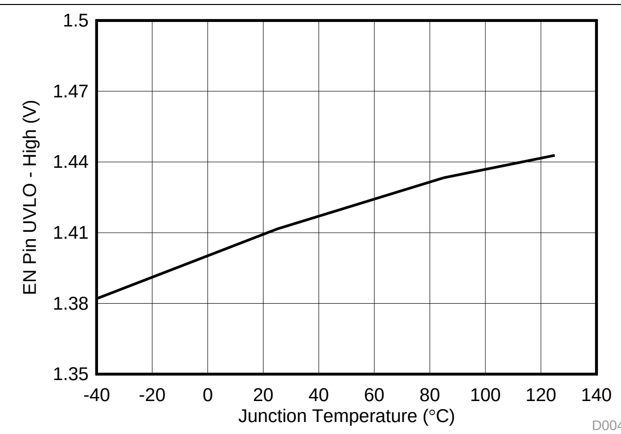


Figure 4. EN Pin UVLO High Voltage vs Junction Temperature

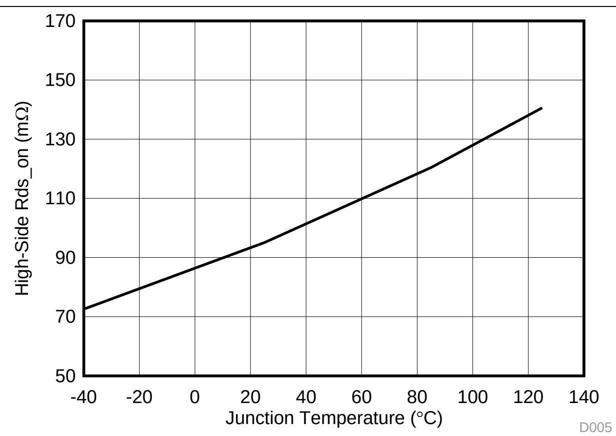


Figure 5. High-Side $R_{ds\text{-}On}$ vs Junction Temperature

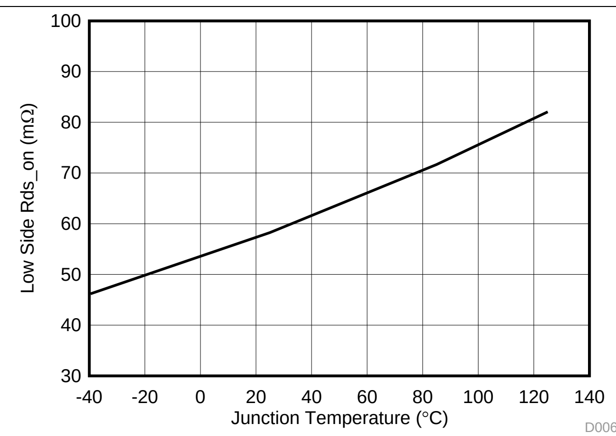
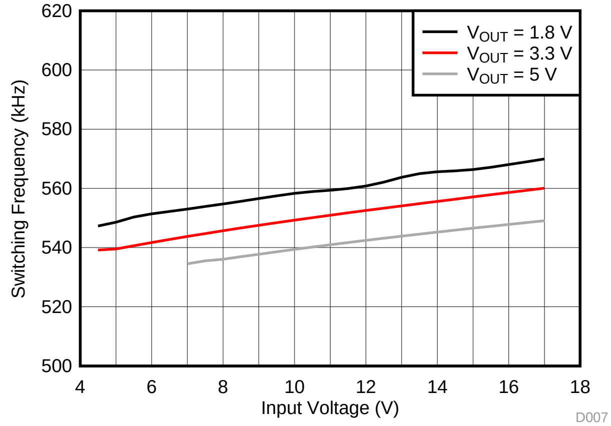


Figure 6. Low-Side $R_{ds\text{-}On}$ vs Junction Temperature

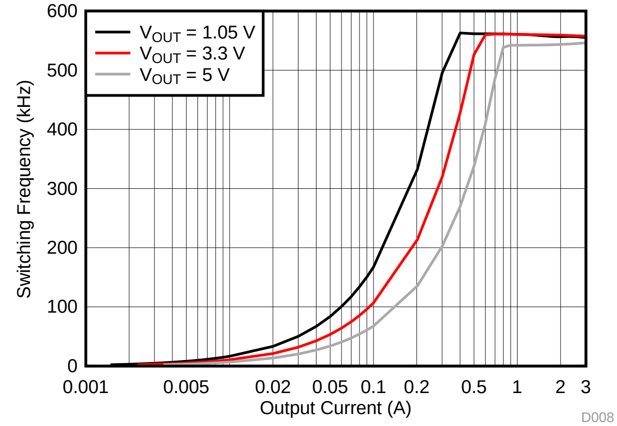
Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)



I_{OUT} = 10 mA

Figure 7. TPS563208 Switching Frequency vs Input Voltage



V_{IN} = 12 V

Figure 8. TPS563201 Switching Frequency vs Output Current

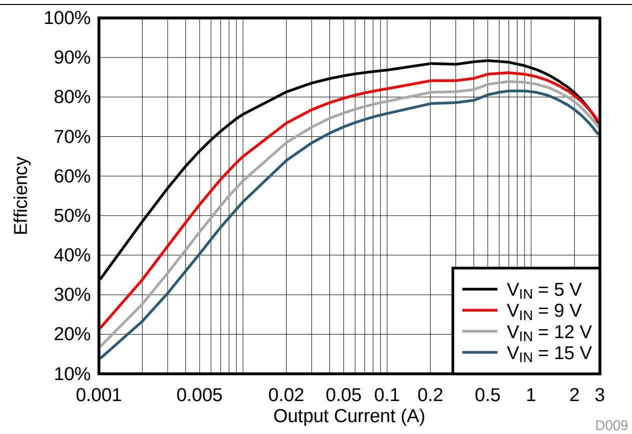


Figure 9. TPS563201 V_{OUT} = 1.05 V Efficiency, L = 2.2 µH

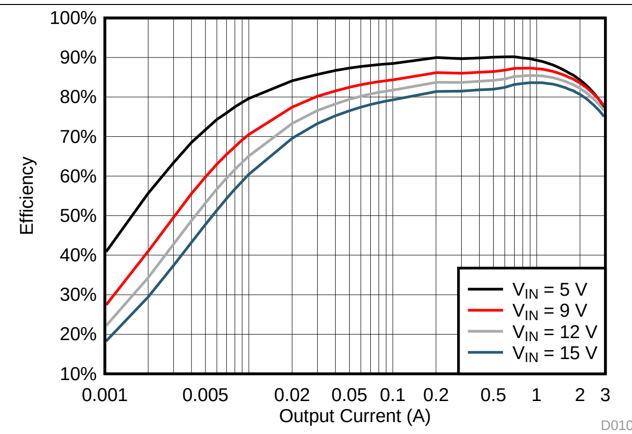


Figure 10. TPS563201 V_{OUT} = 1.5 V Efficiency, L = 2.2 µH

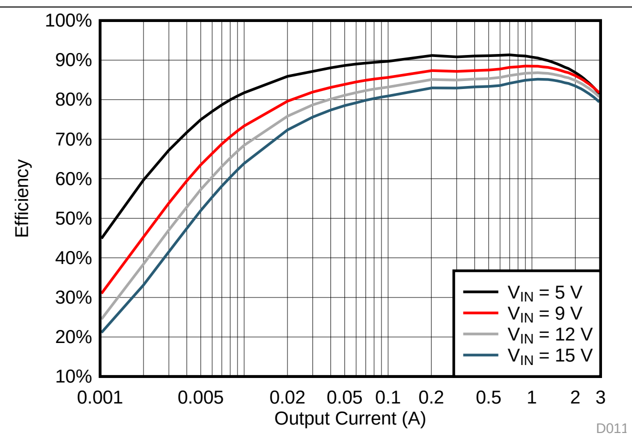


Figure 11. TPS563201 V_{OUT} = 1.8 V Efficiency, L = 2.2 µH

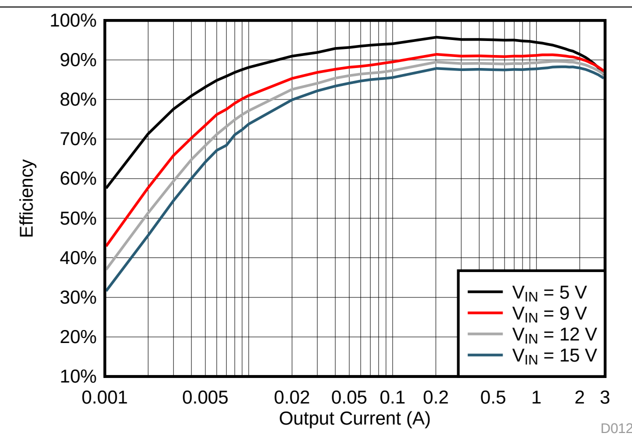


Figure 12. TPS563201 V_{OUT} = 3.3 V Efficiency, L = 2.2 µH

Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

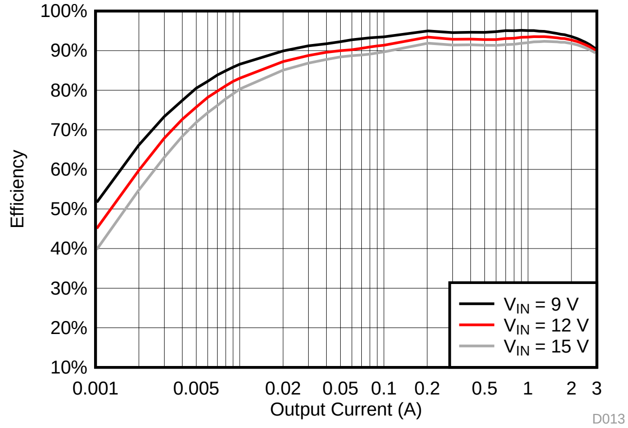


Figure 13. TPS563201 V_{OUT} = 5 V Efficiency, L = 3.3 µH

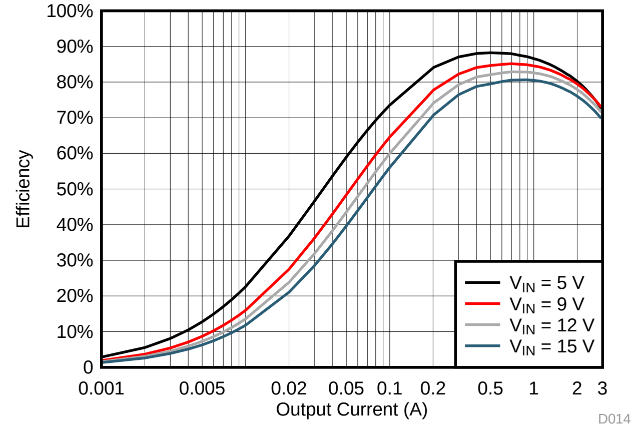


Figure 14. TPS563208 V_{OUT} = 1.05 V Efficiency, L = 2.2 µH

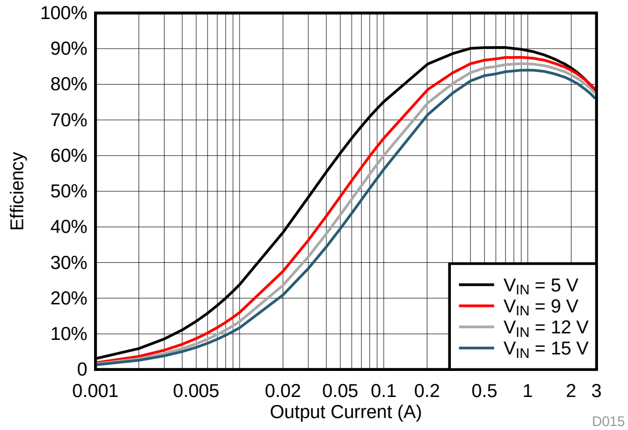


Figure 15. TPS563208 V_{OUT} = 1.5 V Efficiency, L = 2.2 µH

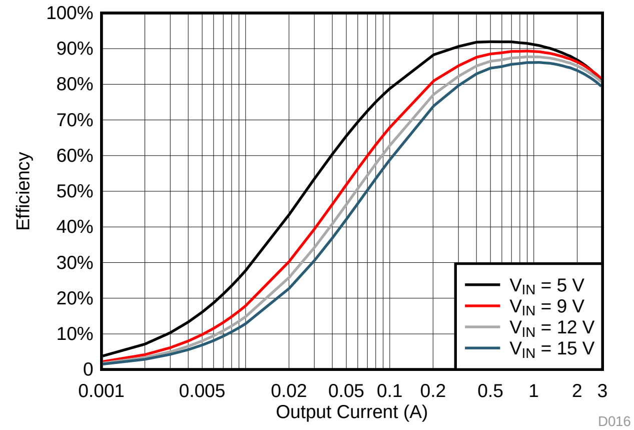


Figure 16. TPS563208 V_{OUT} = 1.8 V Efficiency, L = 2.2 µH

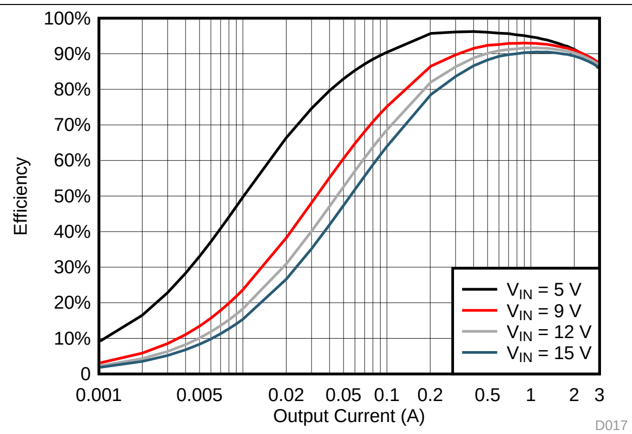


Figure 17. TPS563208 V_{OUT} = 3.3 V Efficiency, L = 2.2 µH

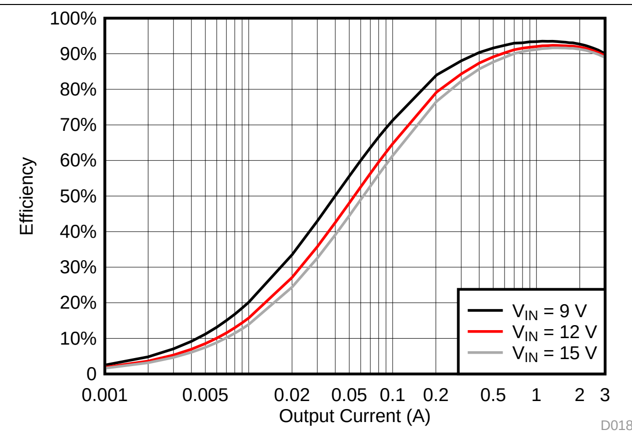


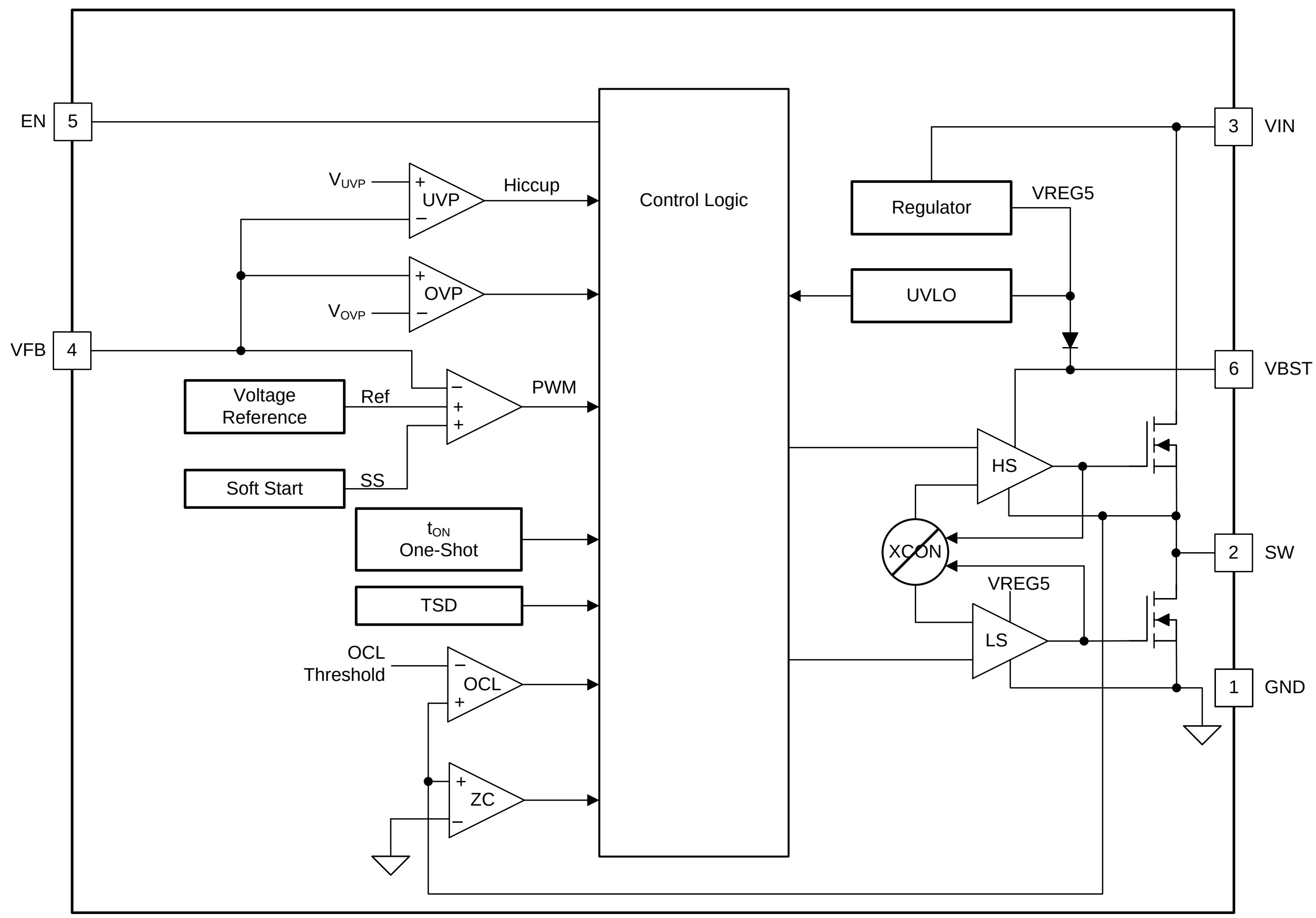
Figure 18. TPS563208 V_{OUT} = 5 V Efficiency, L = 3.3 µH

7 Detailed Description

7.1 Overview

The TPS563201 and TPS563208 are 3-A synchronous step-down converters. The proprietary D-CAP2 mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2 mode control can reduce the output capacitance required to meet a specific level of performance.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS563201 and TPS563208 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 mode control. The D-CAP2 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot duration is set proportional to the converter input voltage, VIN, and inversely proportional to the output voltage, V_O, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 mode control.

Feature Description (continued)

7.3.2 Pulse Skip Control (TPS563201)

The TPS563201 is designed with advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

7.3.3 Soft Start and Pre-Biased Soft Start

The TPS563201 and TPS563208 have an internal 1-ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.4 Current Protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{out}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time (typically 24 µs) and re-start after the hiccup time (typically 15 ms).

When the over current condition is removed, the output voltage returns to the regulated value.

7.3.5 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.6 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 172°C), the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS563201 and TPS563208 can operate in their normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS563201 and TPS563208 operate at a quasi-fixed frequency of 580 kHz.

7.4.2 Eco-mode Operation

When the TPS563201 and TPS563208 are in the normal CCM operating mode and the switch current falls to 0 A, the TPS563201 and TPS563208 begin operating in pulse skipping Eco-mode. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below the Eco-mode threshold voltage. As the output current decreases, the perceived time between switching pulses increases.

7.4.3 Standby Operation

When the TPS563201 and TPS563208 are operating in either normal CCM or Eco-mode, they may be placed in standby by asserting the EN pin low.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The devices are typical step-down DC-DC converters. It typically uses to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 3 A. The following design procedure can be used to select component values for the TPS563201 and TPS563208. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic in Figure 19 was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

Figure 19 shows the TPS563201 and TPS563208 4.5-V to 17-V input, 1.05-V output converter schematics.

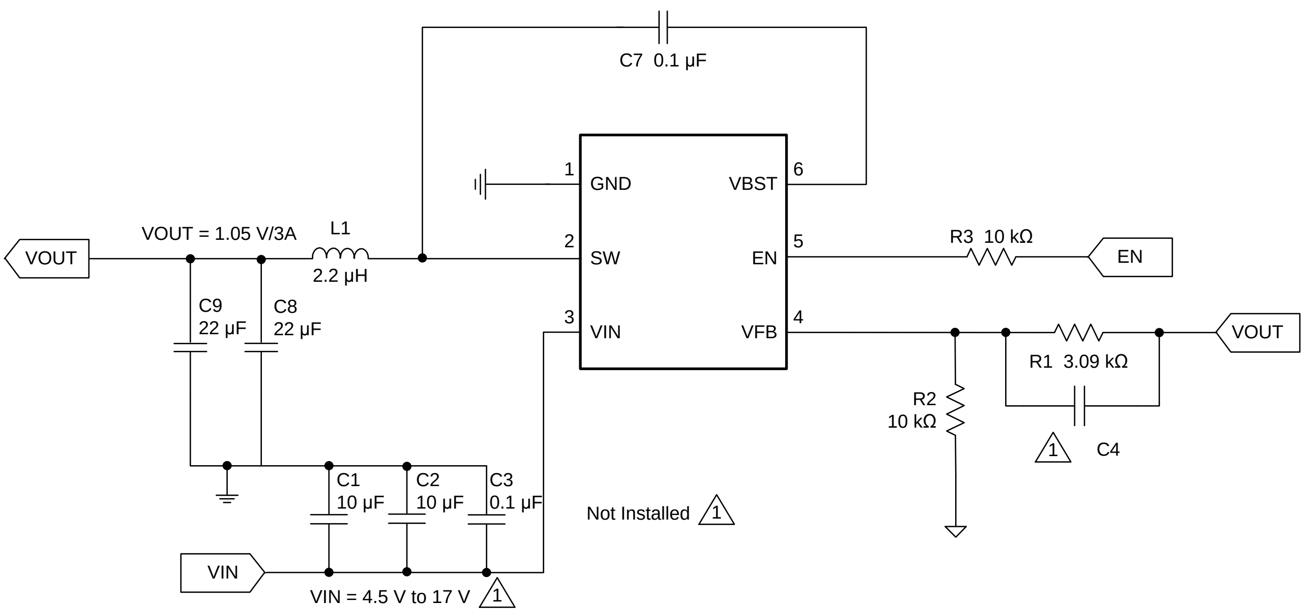


Figure 19. TPS563201 and TPS563208 1.05-V/3-A Reference Design

Typical Application (continued)

8.2.1 Design Requirements

Table 1 shows the design parameters for this application.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 17 V
Output voltage	1.05 V
Transient response, 1.5-A load step	ΔVout = ±5%
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating frequency	580 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using Equation 2 to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.768 \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

8.2.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 2.

Table 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)			C8 + C9 (µF)
			MIN	TYP	MAX	
1	3.09	10.0	1.5	2.2	4.7	20 to 68
1.05	3.74	10.0	1.5	2.2	4.7	20 to 68
1.2	5.76	10.0	1.5	2.2	4.7	20 to 68
1.5	9.53	10.0	1.5	2.2	4.7	20 to 68
1.8	13.7	10.0	1.5	2.2	4.7	20 to 68
2.5	22.6	10.0	2.2	2.2	4.7	20 to 68
3.3	33.2	10.0	2.2	2.2	4.7	20 to 68
5	54.9	10.0	3.3	3.3	4.7	20 to 68
6.5	75	10.0	3.3	3.3	4.7	20 to 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5, and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$Il_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$Il_{PEAK} = I_O + \frac{Il_{P-P}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^{\,2} + \frac{1}{12} Il_{P-P}^{\,2}} \quad (6)$$

For this design example, the calculated peak current is 3.5 A and the calculated RMS current is 3.01 A. The inductor used is a WE 74431122 with a peak current rating of 13 A and an RMS current rating of 9 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS563201 and TPS563208 are intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 µF to 68 µF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286 A and each output capacitor is rated for 4 A.

8.2.2.3 Input Capacitor Selection

The TPS563201 and TPS563208 require an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

8.2.3 Application Curves

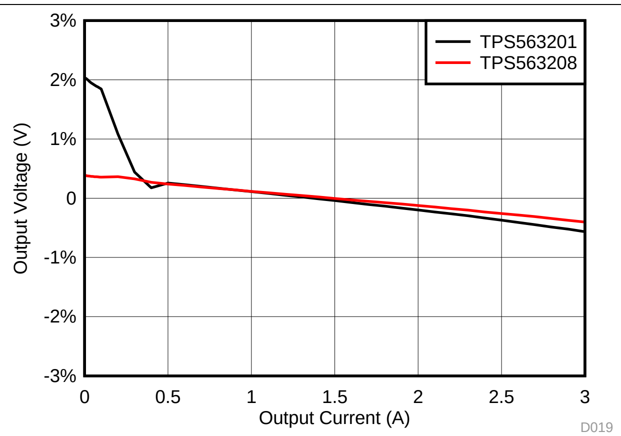


Figure 20. TPS563201 and TPS563208 Load Regulation, V_{IN} = 5 V

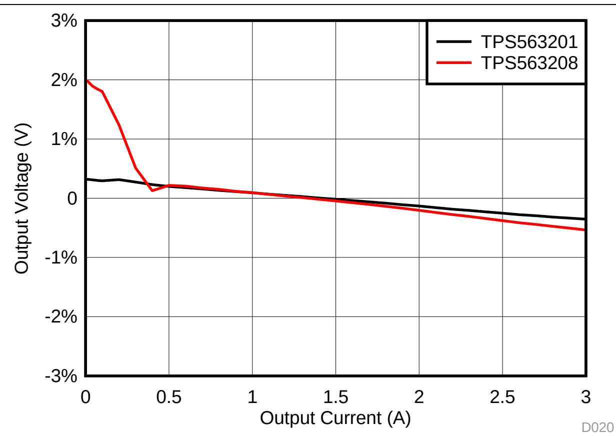
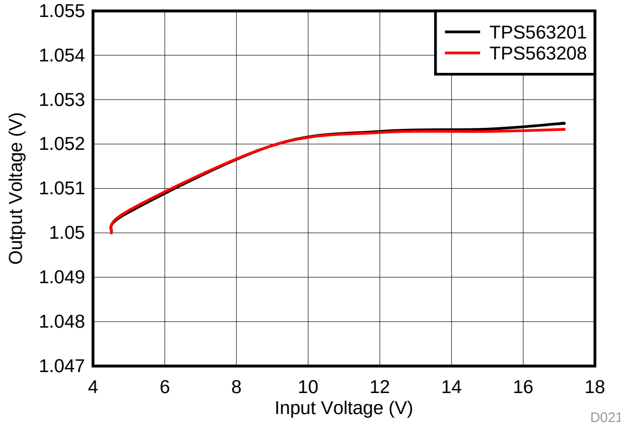


Figure 21. TPS563201 and TPS563208 Load Regulation, V_{IN} = 12 V



I_{OUT} of TPS563201: 1 A

I_{OUT} of TPS563208: 10 mA

Figure 22. TPS563201 and TPS563208 Line Regulation

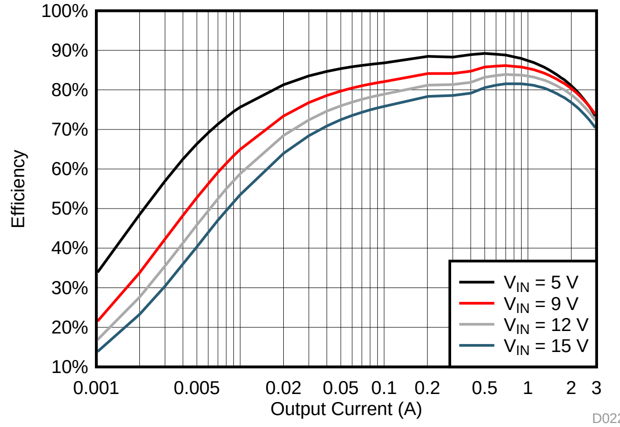


Figure 23. TPS563201 Efficiency

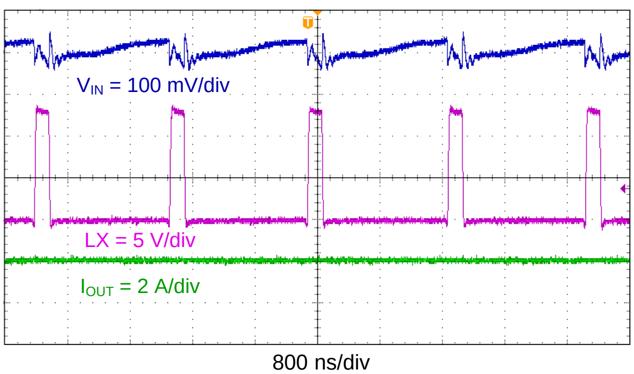


Figure 24. TPS563201 Input Voltage Ripple

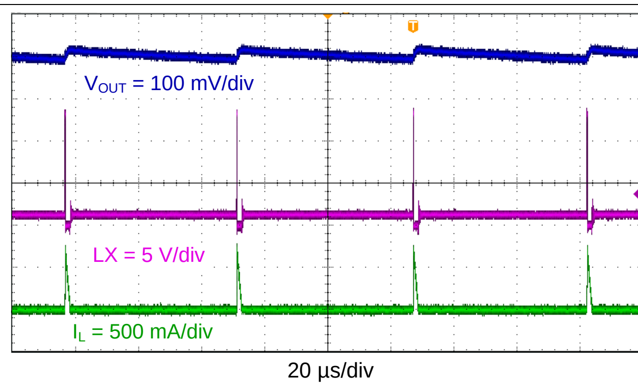


Figure 25. TPS563201 Output Voltage Ripple, 10 mA

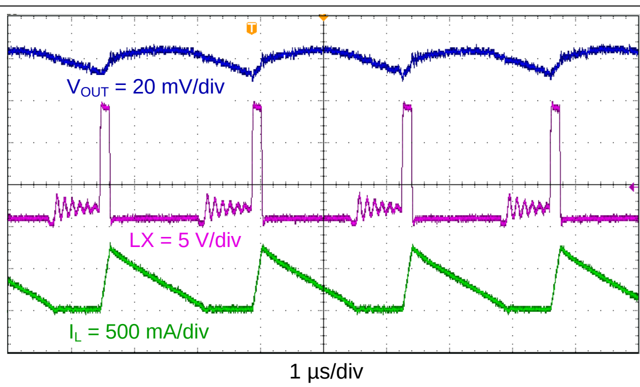


Figure 26. TPS563201 Output Voltage Ripple, I_{out} = 0.25 A

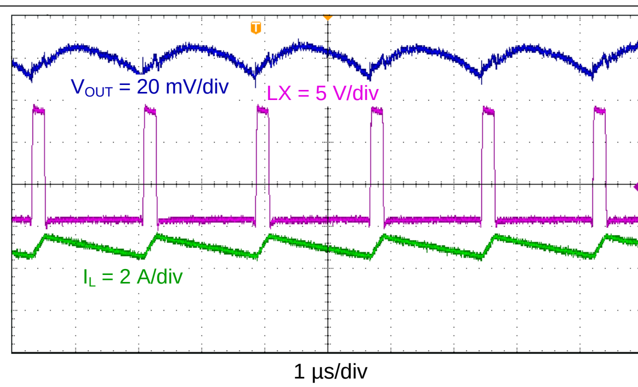


Figure 27. TPS563201 Output Voltage Ripple, I_{out} = 2 A

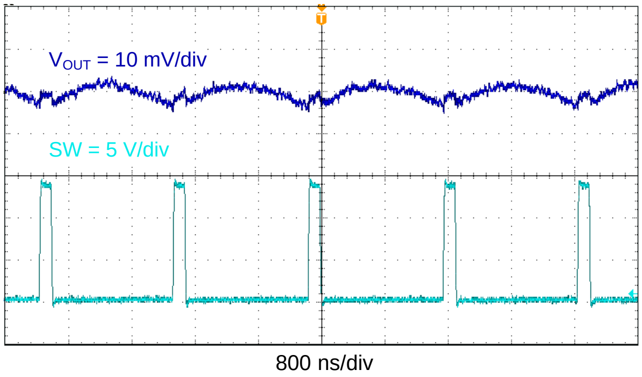


Figure 28. TPS563208 Output Voltage Ripple, I_{OUT} = 0 A

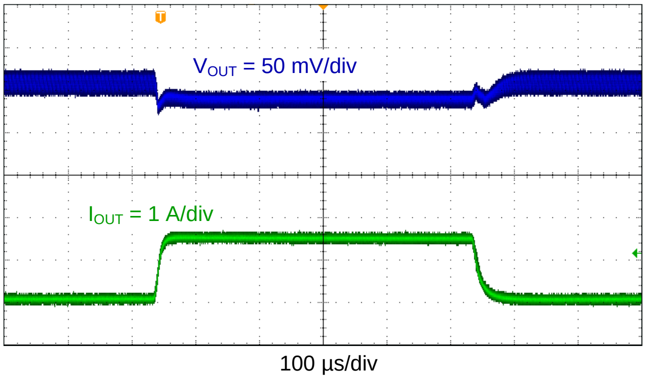


Figure 29. TPS563201 Transient Response, 0.1 to 1.5 A

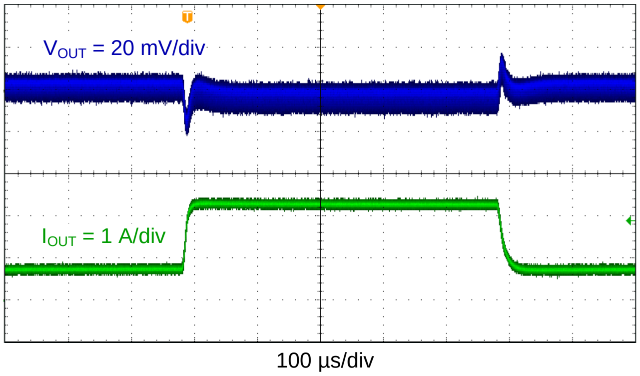


Figure 30. TPS563201 Transient Response, 0.75 to 2.25 A

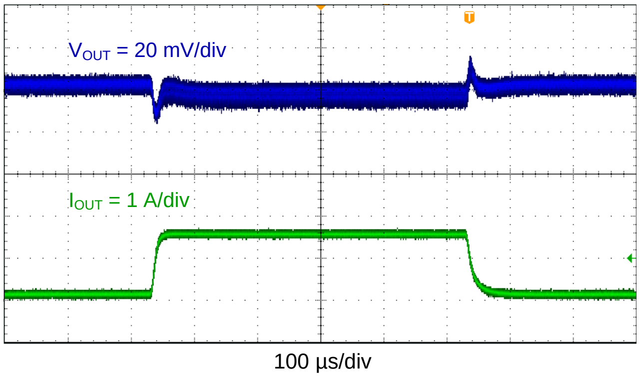


Figure 31. TPS563208 Transient Response 0.1 to 2 A

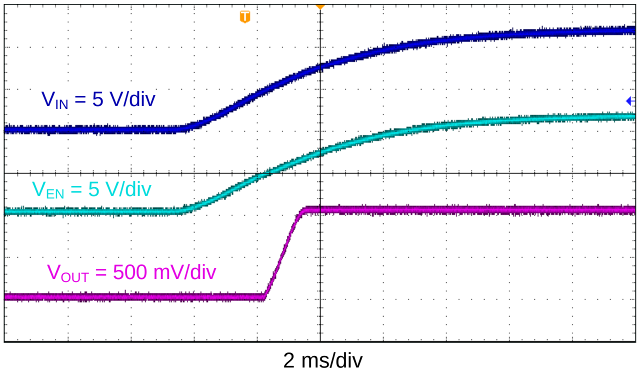


Figure 32. TPS563201 Start Up Relative to V_I

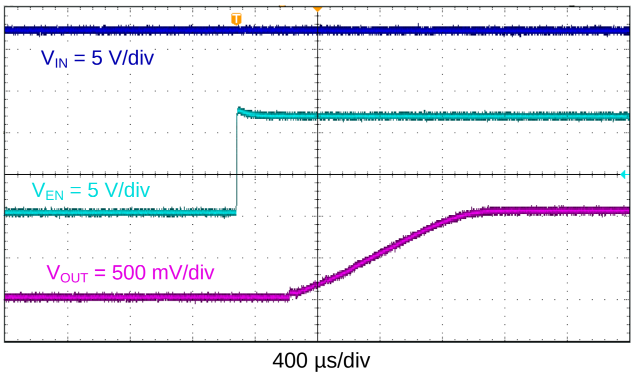


Figure 33. TPS563201 Start-Up Relative to EN

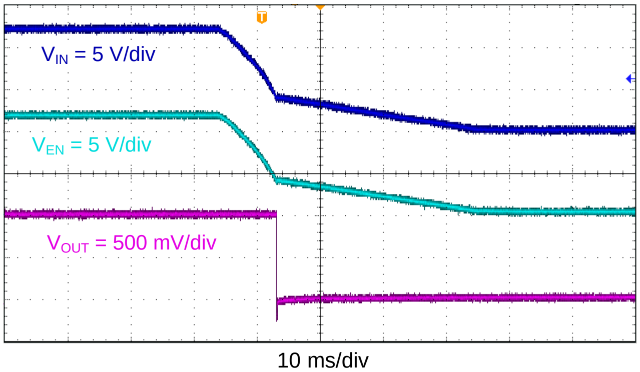


Figure 34. TPS563201 Shutdown Relative to V_I

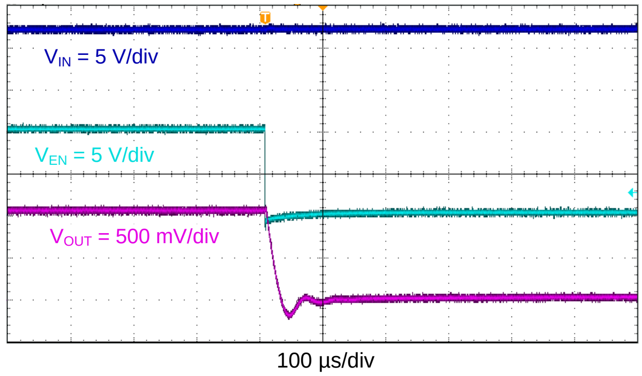


Figure 35. TPS563201 Shutdown Relative to EN

9 Power Supply Recommendations

TPS563201 and TPS563208 are designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is V_O / 0.75.

10 Layout

10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

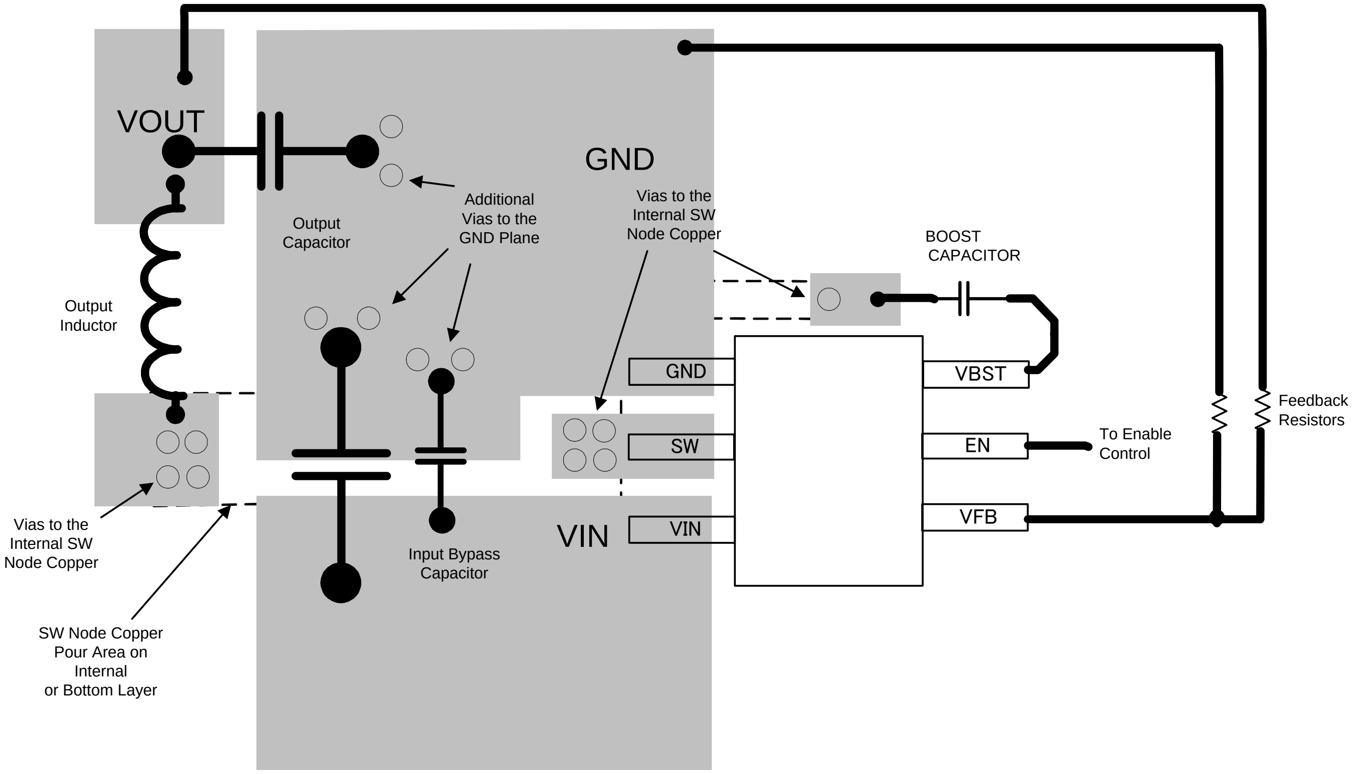


Figure 36. TPS563201 and TPS563208 Layout

11 器件和文档支持

11.1 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持和社区资源、工具和软件，以及样片或购买的快速访问。

表 **3.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS563201	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS563208	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

D-CAP2, Eco-mode, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
蓝光 is a trademark of Blu-ray Disc Association.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
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接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
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无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS563201DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	3201	Samples
TPS563201DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	3201	Samples
TPS563208DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	3208	Samples
TPS563208DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	3208	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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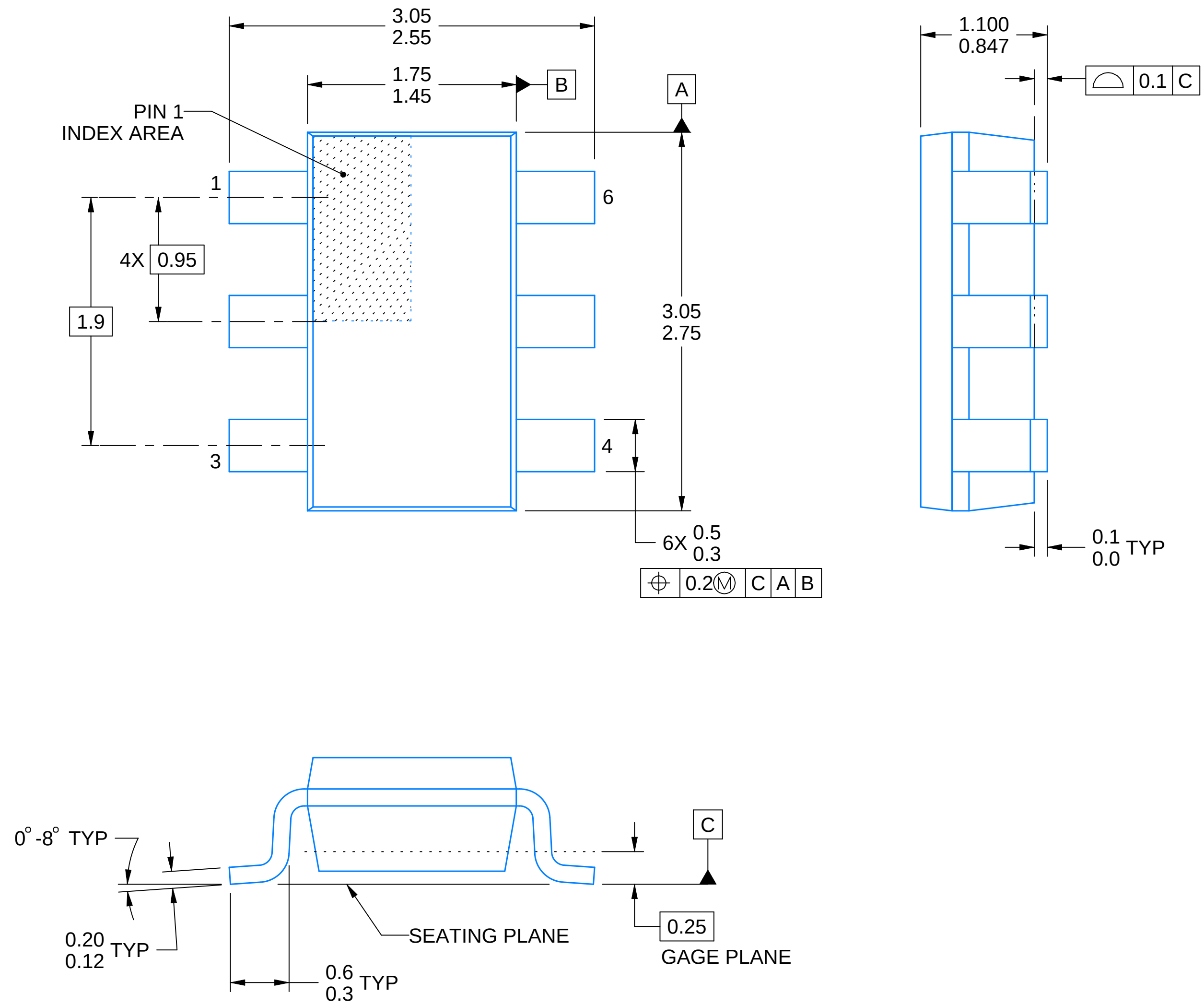
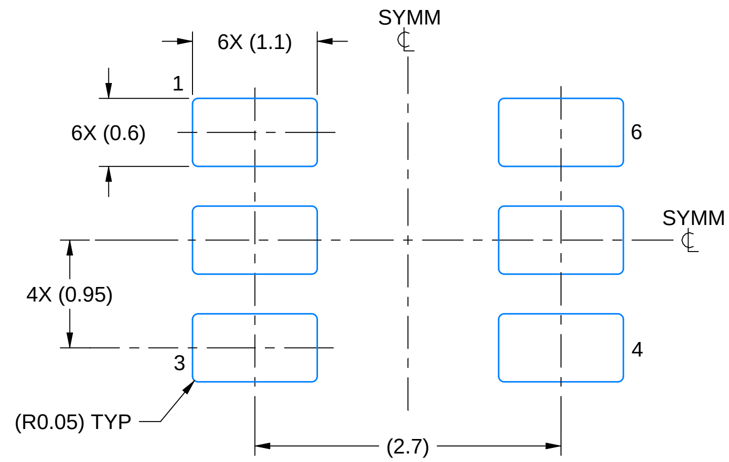


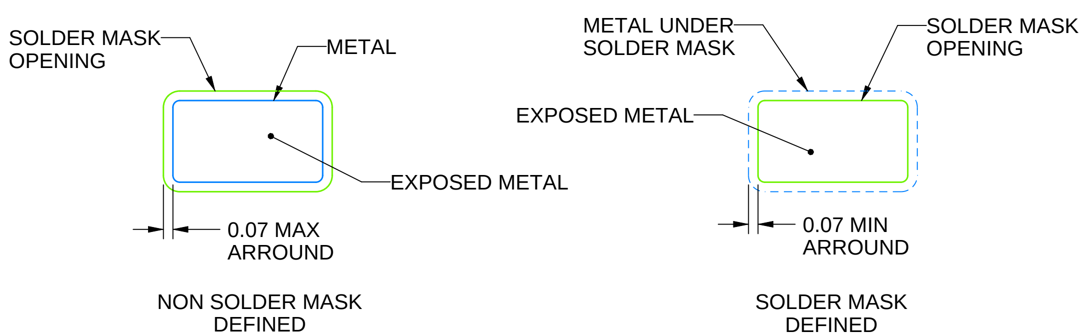
4214841/B 11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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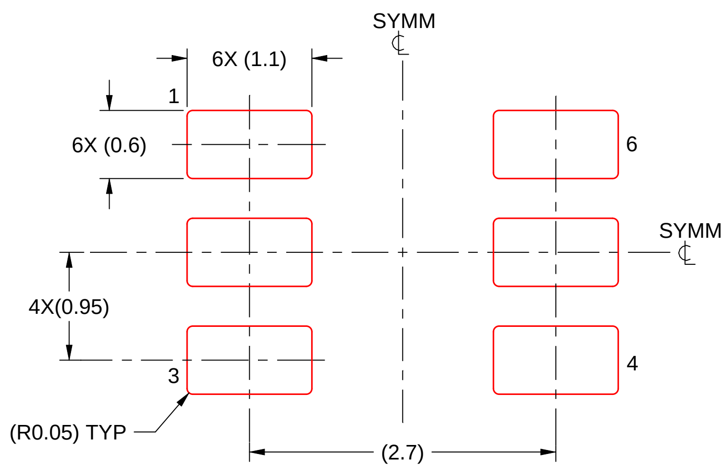
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/B 11/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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