- **High Slew Rate . . . 10.5 V/μs Typ**
- **High-Gain Bandwidth . . . 5.1 MHz Typ**
- **Supply Voltage Range 2.5 V to 5.5 V**
- **Rail-to-Rail Output**
- **360 μV Input Offset Voltage**
- **Low Distortion Driving 600-Ω**
  0.005% THD+N
- **1 mA Supply Current (Per Channel)**
- **17 nV/√Hz Input Noise Voltage**
- **2 pA Input Bias Current**
- **Characterized From T_A = −55°C to 125°C**
- **Available in MSOP and SOT-23 Packages**
- **Micropower Shutdown Mode . . . I_{DD} < 1 μA**
- **Available in Q-Temp Automotive**
  High Reliability Automotive Applications
  Configuration Control / Print Support
  Qualification to Automotive Standards

description

The TLV277x CMOS operational amplifier family combines high slew rate and bandwidth, rail-to-rail output swing, high output drive, and excellent dc precision. The device provides 10.5 V/μs of slew rate and 5.1 MHz of bandwidth while only consuming 1 mA of supply current per channel. This ac performance is much higher than current competitive CMOS amplifiers. The rail-to-rail output swing and high output drive make these devices a good choice for driving the analog input or reference of analog-to-digital converters. These devices also have low distortion while driving a 600-Ω load for use in telecom systems.

These amplifiers have a 360-μV input offset voltage, a 17 nV/√Hz input noise voltage, and a 2-pA input bias current for measurement, medical, and industrial applications. The TLV277x family is also specified across an extended temperature range (−40°C to 125°C), making it useful for automotive systems, and the military temperature range (−55°C to 125°C), for military systems.

These devices operate from a 2.5-V to 5.5-V single supply voltage and are characterized at 2.7 V and 5 V. The single-supply operation and low power consumption make these devices a good solution for portable applications. The following table lists the packages available.

FAMILY PACKAGE TABLE

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES								SHUTDOWN	UNIVERSAL EVM BOARD
		PDIP	CDIP	SOIC	SOT-23	TSSOP	MSOP	LCCC	CPAK		
TLV2770	1	8	—	8	—	—	8	—	—	Yes	Refer to the EVM Selection Guide (Lit# SLOU060)
TLV2771	1	—	—	8	5	—	—	—	—	—	
TLV2772	2	8	8	8	—	8	8	20	10	—	
TLV2773	2	14	—	14	—	—	10	—	—	Yes	
TLV2774	4	14	—	14	—	14	—	—	—	—	
TLV2775	4	16	—	16	—	16	—	—	—	Yes	

A SELECTION OF SINGLE-SUPPLY OPERATIONAL AMPLIFIER PRODUCTS†

DEVICE	V_{DD} (V)	BW (MHz)	SLEW RATE (V/μs)	I_{DD} (per channel) (μA)	RAIL-TO-RAIL
TLV277X	2.5 − 6.0	5.1	10.5	1000	O
TLV247X	2.7 − 6.0	2.8	1.5	600	I/O
TLV245X	2.7 − 6.0	0.22	0.11	23	I/O
TLV246X	2.7 − 6.0	6.4	1.6	550	I/O

† All specifications measured at 5 V.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

TLV2770 and TLV2771 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C (mV)	PACKAGED DEVICES			
		SMALL OUTLINE (D)	SOT-23 (DBV)	MSOP (DGK)	PLASTIC DIP (P)
0°C to 70°C	2.5	TLV2770CD TLV2771CD	— TLV2771CDBV	TLV2770CDGK† —	TLV2770CP —
−40°C to 125°C	2.5	TLV2770ID TLV2771ID	— TLV2771IDBV	TLV2770IDGK† —	TLV2770IP —
	1.6	TLV2770AID TLV2771AID	— —	— —	TLV2770AIP —

† This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

TLV2772 and TLV2773 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C (mV)	PACKAGED DEVICES				
		SMALL OUTLINE (D)	MSOP (DGK)	MSOP (DGS)	PLASTIC DIP (N)	PLASTIC DIP (P)
0°C to 70°C	2.5	TLV2772CD TLV2773CD	TLV2772CDGK —	— TLV2773CDGS	— TLV2773CN	TLV2772CP —
−40°C to 125°C	2.5	TLV2772ID TLV2773ID	TLV2772IDGK —	— TLV2773IDGS	— TLV2773IN	TLV2772IP —
	1.6	TLV2772AID TLV2773AID	— —	— —	— TLV2773AIN	TLV2772AIP —

TLV2774 and TLV2775 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C (mV)	PACKAGED DEVICES			
		SMALL OUTLINE (D)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP (PW)
0°C to 70°C	2.7	TLV2774CD TLV2775CD	— TLV2775CN	TLV2774CP —	TLV2774CPW TLV2775CPW
−40°C to 125°C	2.7	TLV2774ID TLV2775ID	— TLV2775IN	TLV2774IP —	TLV2774IPW TLV2775IPW
	2.1	TLV2774AID TLV2775AID	— TLV2775AIN	TLV2774AIP —	TLV2774AIPW TLV2775AIPW

TLV2772M/Q AND TLV2772AM/Q AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C (mV)	PACKAGED DEVICES				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	CERAMIC FLATPACK (U)	TSSOP (PW)
−40°C to 125°C	2.5	TLV2772QD‡	—	—	—	TLV2772QPW‡
	1.6	TLV2772AQD‡	—	—	—	TLV2772AQPW‡
−55°C to 125°C	2.5	TLV2772MD	TLV2772MFK	TLV2772MJG	TLV2772MU	—
	1.6	TLV2772AMD	TLV2772AMFK	TLV2772AMJG	TLV2772AMU	—

‡ Available in tape and reel

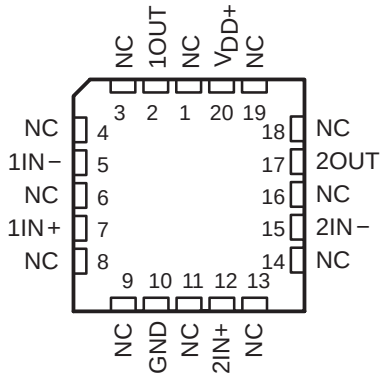
PACKAGE SYMBOLS

PACKAGE TYPE	PINS	PART NUMBER	SYMBOL†
SOT23	5 Pin	TLV2771CDBV	VAMC
		TLV2771IDBV	VAMI
MSOP	8 Pin	TLV2770CDGK	xxTIABO
		TLV2770IDGK	xxTIABP
		TLV2772CDGK	xxTIAAF
		TLV2772IDGK	xxTIAAG
	10 Pin	TLV2773CDGS	xxTIABQ
		TLV2773IDGS	xxTIABR

† xx represents the device date code.

TLV277x PACKAGE PINOUT

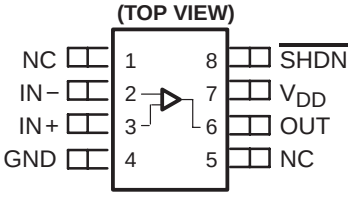
TLV2772M AND TLV2772AM
FK PACKAGE
(TOP VIEW)



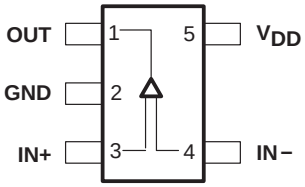
NC − No internal connection

TLV277x PACKAGE PINOUTS(1)

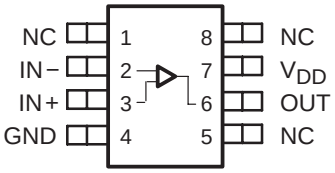
TLV2770
D, DGK† OR P PACKAGE
(TOP VIEW)



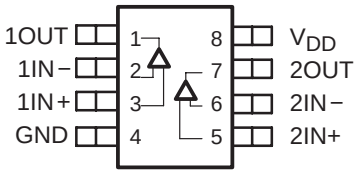
TLV2771
DBV PACKAGE
(TOP VIEW)



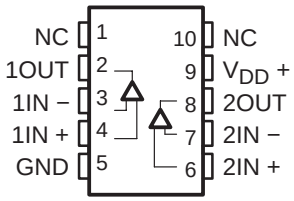
TLV2771
D PACKAGE
(TOP VIEW)



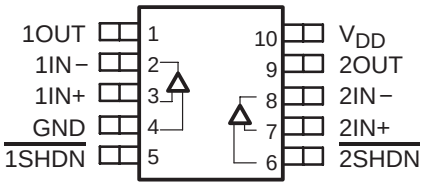
TLV2772
D, DGK, JG, P, OR PW PACKAGE
(TOP VIEW)



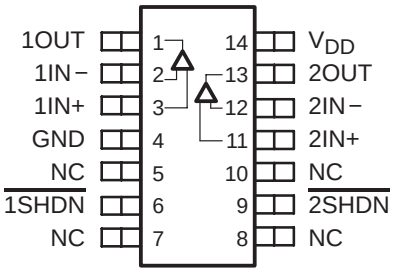
TLV2772M AND TLV2772AM
U PACKAGE
(TOP VIEW)



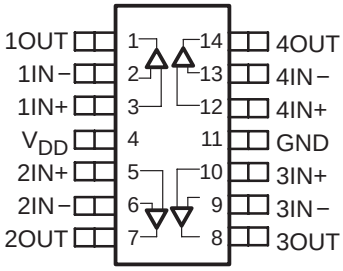
TLV2773
DGS PACKAGE
(TOP VIEW)



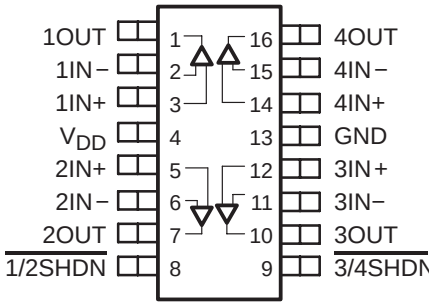
TLV2773
D OR N PACKAGE
(TOP VIEW)



TLV2774
D, N, OR PW PACKAGE
(TOP VIEW)

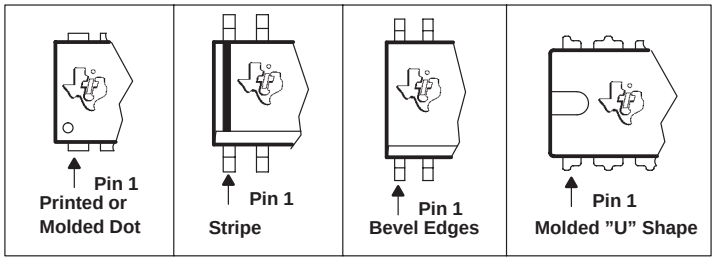


TLV2775
D, N, OR PW PACKAGE
(TOP VIEW)



† This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.
(1) SOT−23 may or may not be indicated

TYPICAL PIN 1 INDICATORS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 7 V
Differential input voltage, V_{ID} (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) . . . . . −0.3 V to V_{DD}
Input current, I_I (any input) . . . . . ±4 mA
Output current, I_O . . . . . ±50 mA
Total current into V_{DD+} . . . . . ±50 mA
Total current out of GND . . . . . ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) . . . . . unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . −40°C to 125°C
Q suffix . . . . . −40°C to 125°C
M suffix . . . . . −55°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to GND.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below GND − 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DBV	437 mW	3.5 mW/°C	280 mW	227 mW	87 mW
DGK	424 mW	3.4 mW/°C	271 mW	220 mW	85 mW
DGS	424 mW	3.4 mW/°C	271 mW	220 mW	85 mW
FK	1375 mW	11.0 mW/°C	672 mW	546 mW	210 mW
JG	1050 mW	8.4 mW/°C	880 mW	714 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW	700 mW	5.6 mW/°C	448 mW	364 mW	140 mW
U	675 mW	5.4 mW/°C	432 mW	350 mW	135 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	2.5	6	2.5	6	2.5	6	2.5	6	V
Input voltage range, V_I	GND	$V_{DD+}-1.3$	GND	$V_{DD+}-1.3$	GND	$V_{DD+}-1.3$	GND	$V_{DD+}-1.3$	V
Common-mode input voltage, V_{IC}	GND	$V_{DD+}-1.3$	GND	$V_{DD+}-1.3$	GND	$V_{DD+}-1.3$	GND	$V_{DD+}-1.3$	V
Operating free-air temperature, T_A	0	70	−40	125	−40	125	−55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLV277xC			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLV2770/1/2	V_{IC} = 0, R_S = 50 Ω, No load	V_O = 0, V_{DD} = ±1.35 V,	25°C		0.48	2.5	mV
					Full range		0.53	2.7	
		TLV2773/4/5			25°C		0.8	2.7	
					Full range		0.86	2.9	
α_{VIO}	Temperature coefficient of input offset voltage		V_{IC} = 0, R_S = 50 Ω	V_O = 0, V_{DD} = ±1.35 V	25°C to 125°C		2		µV/°C
I_{IO}	Input offset current				25°C		1	60	pA
					Full range		2	100	
I_{IB}	Input bias current				25°C		2	60	pA
					Full range		6	100	
V_{OH}	High-level output voltage		I_{OH} = −0.675 mA		25°C		2.6		V
					Full range		2.5		
			I_{OH} = −2.2 mA		25°C		2.4		
					Full range		2.1		
V_{OL}	Low-level output voltage		V_{IC} = 1.35 V,	I_{OL} = 0.675 mA	25°C		0.1		V
					Full range		0.2		
			V_{IC} = 1.35 V,	I_{OL} = 2.2 mA	25°C		0.21		
					Full range		0.6		
A_{VD}	Large-signal differential voltage amplification		V_{IC} = 1.35 V, V_O = 0.6 V to 2.1 V	R_L = 10 kΩ,	25°C	20	380		V/mV
					Full range	13			
$r_{i(d)}$	Differential input resistance				25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance		f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance		f = 100 kHz,	A_V = 10	25°C		25		Ω
CMRR	Common-mode rejection ratio		V_{IC} = 0 to 1.5 V, R_S = 50 Ω	V_O = V_{DD}/2,	25°C	60	84		dB
					Full range	60	82		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})		V_{DD} = 2.7 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	70	89		dB
					Full range	70	84		
I_{DD}	Supply current (per channel)		V_O = V_{DD}/2,	No load	25°C		1	2	mA
					Full range			2	
$I_{DD(SHDN)}$	Supply current in shutdown (per channel)				25°C		0.8	1.5	µA
					Full range		1.3	2	
$V_{(ON)}$	Turnon voltage level	TLV2770	A_V = 5		25°C		1.47		V
		TLV2773					1.43		
		TLV2775					1.40		
$V_{(OFF)}$	Turnoff voltage level	TLV2770	A_V = 5		25°C		1.27		V
		TLV2773					1.21		
		TLV2775					1.20		

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV277xC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	9		V/μs
				Full range	4.7	6		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		21		nV/√Hz
		f = 10 kHz		25°C		17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33		μV
		f = 0.1 Hz to 10 Hz				0.86		
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.0085%		
			A_V = 10			0.025%		
			A_V = 100			0.12%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 600 Ω,	25°C		4.8		MHz
t_s	Settling time	A_V = −1, Step = 1 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.186		μs
			0.01%	25°C		0.3		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω,	C_L = 100 pF	25°C		46°		
	Gain margin			25°C		12		dB

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLV277xC			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLV2770/1/2	V_{IC} = 0, R_S = 50 Ω, No load	V_O = 0, V_{DD} = ±2.5 V,	25°C		0.5	2.5	mV
					Full range		0.6	2.7	
		TLV2773/4/5			25°C		0.7	2.5	
					Full range		0.78	2.7	
α_{VIO}	Temperature coefficient of input offset voltage		V_{IC} = 0, R_S = 50 Ω	V_O = 0, V_{DD} = ±2.5 V	25°C to 125°C		2		µV/°C
I_{IO}	Input offset current				25°C		1	60	pA
					Full range		2	100	
I_{IB}	Input bias current				25°C		2	60	pA
					Full range		6	100	
V_{OH}	High-level output voltage		I_{OH} = −1.3 mA		25°C		4.9		V
					Full range		4.8		
			I_{OH} = −4.2 mA		25°C		4.7		
					Full range		4.4		
V_{OL}	Low-level output voltage		V_{IC} = 2.5 V,	I_{OL} = 1.3 mA	25°C		0.1		V
					Full range		0.2		
			V_{IC} = 2.5 V,	I_{OL} = 4.2 mA	25°C		0.21		
					Full range		0.6		
A_{VD}	Large-signal differential voltage amplification		V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ,	25°C	20	450		V/mV
					Full range	13			
$r_{i(d)}$	Differential input resistance				25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance		f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance		f = 100 kHz,	A_V = 10	25°C		20		Ω
CMRR	Common-mode rejection ratio		V_{IC} = 0 to 3.7 V, R_S = 50 Ω	V_O = V_{DD}/2,	25°C	70	96		dB
					Full range	70	93		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})		V_{DD} = 2.7 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	70	89		dB
					Full range	70	84		
I_{DD}	Supply current (per channel)		V_O = V_{DD}/2,	No load	25°C		1	2	mA
					Full range			2	
$I_{DD(SHDN)}$	Supply current in shutdown (per channel)				25°C		0.8	1.5	µA
					Full range		1.3	2	
$V_{(ON)}$	Turnon voltage level	TLV2770	A_V = 5		25°C		2.59		V
		TLV2773					2.47		
		TLV2775					2.48		
$V_{(OFF)}$	Turnoff voltage level	TLV2770	A_V = 5		25°C		2.41		V
		TLV2773					2.32		
		TLV2775					2.29		

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLV277xC			UNIT
						MIN	TYP	MAX	
SR	Slew rate at unity gain		$V_{O(PP)}$ = 2 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	10.5		V/μs
					Full range	4.7	6		
V_n	Equivalent input noise voltage		f = 1 kHz		25°C		17		nV/√Hz
			f = 10 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 0.1 Hz to 1 Hz		25°C		0.33		μV
			f = 0.1 Hz to 10 Hz				0.86		
I_n	Equivalent input noise current		f = 100 Hz		25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise		R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.005%		
				A_V = 10			0.016%		
				A_V = 100			0.095%		
	Gain-bandwidth product		f = 10 kHz, C_L = 100 pF	R_L = 600 Ω,	25°C		5.1		MHz
t_s	Settling time		A_V = −1, Step = 2 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.335		μs
				0.01%	25°C		0.6		
ϕ_m	Phase margin at unity gain		R_L = 600 Ω,	C_L = 100 pF	25°C		46°		
	Gain margin				25°C		12		dB
$t_{(ON)}$	Amplifier turnon time	TLV2770	A_V = 5, R_L = Open, Measured to 50% point		25°C		1.2		μs
		TLV2773					2.4		
		TLV2775					1.9		
$t_{(OFF)}$	Amplifier turnoff time	TLV2770	A_V = 5 R_L = Open, Measured to 50% point		25°C		335		ns
		TLV2773					444		
		TLV2775					345		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLV277xI			TLV277xAI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLV2770/1/2	V_{IC} = 0, V_O = 0, R_S = 50 Ω, V_{DD} = ±1.35 V, No load	25°C		0.48	2.5		0.48	1.6	mV
				Full range		0.53	2.7		0.53	1.9	
		TLV2773/4/5		25°C		0.8	2.7		0.8	2.1	
				Full range		0.86	2.9		0.86	2.2	
α_{VIO}	Temperature coefficient of input offset voltage		V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C to 125°C		2			2		µV/°C
I_{IO}	Input offset current			25°C		1	60		1	60	pA
				Full range		2	125		2	125	
I_{IB}	Input bias current			25°C		2	60		2	60	pA
				Full range		6	350		6	350	
V_{OH}	High-level output voltage		I_{OH} = −0.675 mA	25°C		2.6			2.6		V
				Full range		2.5			2.5		
			I_{OH} = −2.2 mA	25°C		2.4			2.4		
				Full range		2.1			2.1		
V_{OL}	Low-level output voltage		V_{IC} = 1.35 V, I_{OL} = 0.675 mA	25°C		0.1			0.1		V
				Full range		0.2			0.2		
			V_{IC} = 1.35 V, I_{OL} = 2.2 mA	25°C		0.21			0.21		
				Full range		0.6			0.6		
A_{VD}	Large-signal differential voltage amplification		V_{IC} = 1.35 V, R_L = 10 kΩ, V_O = 0.6 V to 2.1 V	25°C	20	380		20	380		V/mV
				Full range	13			13			
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance		f = 10 kHz,	25°C		8			8		pF
z_o	Closed-loop output impedance		f = 100 kHz, A_V = 10	25°C		25			25		Ω
CMRR	Common-mode rejection ratio		V_{IC} = 0 to 1.5 V, V_O = V_{DD}/2, R_S = 50 Ω	25°C	60	84		60	84		dB
				Full range	60	82		60	82		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})		V_{DD} = 2.7 V to 5 V, V_{IC} = V_{DD}/2, No load	25°C	70	89		70	89		dB
				Full range	70	84		70	84		
I_{DD}	Supply current (per channel)		V_O = V_{DD}/2, No load	25°C		1	2		1	2	mA
				Full range			2			2	
$I_{DD(SHDN)}$	Supply current in shutdown (per channel)			25°C		0.8	1.5		0.8	1.5	µA
				Full range		1.3	2		1.3	2	

† Full range is − 40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS	T_A†	TLV277xI			TLV277xAI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(ON)}$	Turnon voltage level	TLV2770	A_V = 5	25°C		1.47			1.47		V
		TLV2773				1.43			1.43		
		TLV2775				1.40			1.4		
$V_{(OFF)}$	Turnoff voltage level	TLV2770	A_V = 5	25°C		1.27			1.27		V
		TLV2773				1.21			1.21		
		TLV2775				1.20			1.2		

† Full range is − 40°C to 125°C.

operating characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV277xI			TLV277xAI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	9		5	9		V/μs
				Full range	4.7	6		4.7	6		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		21			21		nV/√Hz
		f = 10 kHz		25°C		17			17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33			0.33		μV
		f = 0.1 Hz to 10 Hz		25°C		0.86			0.86		μV
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.0085%			0.0085%		
			A_V = 10			0.025%			0.025%		
			A_V = 100			0.12%			0.12%		
	Gain-bandwidth product	f = 10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		4.8			4.8		MHz
t_s	Settling time	A_V = −1, Step = 0.85 V to 1.85 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.186			0.186		μs
			0.01%	25°C		3.92			3.92		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		46°			46°		
	Gain margin			25°C		12			12		dB

† Full range is −40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLV277xI			TLV277xAI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLV2770/1/2	V_{IC} = 0, No load, V_O = 0, R_S = 50 Ω, V_{DD} = ±2.5 V	25°C		0.5	2.5		0.5	1.6	mV
				Full range		0.6	2.7		0.6	1.9	
		TLV2773/4/5		25°C		0.7	2.5		0.7	2.1	
				Full range		0.78	2.7		0.78	2.2	
α_{VIO}	Temperature coefficient of input offset voltage		V_{IC} = 0, V_O = 0, R_S = 50 Ω, V_{DD} = ±2.5 V	25°C to 125°C		2			2		µV/°C
I_{IO}	Input offset current			25°C		1	60		1	60	pA
				Full range		2	125		2	125	
I_{IB}	Input bias current			25°C		2	60		2	60	pA
				Full range		6	350		6	350	
V_{OH}	High-level output voltage		I_{OH} = −1.3 mA	25°C		4.9			4.9		V
				Full range		4.8			4.8		
			I_{OH} = −4.2 mA	25°C		4.7			4.7		
				Full range		4.4			4.4		
V_{OL}	Low-level output voltage		V_{IC} = 2.5 V, I_{OL} = 1.3 mA	25°C		0.1			0.1		V
				Full range		0.2			0.2		
			V_{IC} = 2.5 V, I_{OL} = 4.2 mA	25°C		0.21			0.21		
				Full range		0.6			0.6		
A_{VD}	Large-signal differential voltage amplification		V_{IC} = 2.5 V, R_L = 10 kΩ, V_O = 1 V to 4 V	25°C	20	450		20	450		V/mV
				Full range	13			13			
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance		f = 10 kHz	25°C		8			8		pF
z_o	Closed-loop output impedance		f = 100 kHz, A_V = 10	25°C		20			20		Ω
CMRR	Common-mode rejection ratio		V_{IC} = 0 to 3.7 V, V_O = V_{DD}/2, R_S = 50 Ω	25°C	60	96		70	96		dB
				Full range	60	93		70	93		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})		V_{DD} = 2.7 V to 5 V, V_{IC} = V_{DD}/2, No load	25°C	70	89		70	89		dB
				Full range	70	84		70	84		
I_{DD}	Supply current (per channel)		V_O = V_{DD}/2, No load	25°C		1	2		1	2	mA
				Full range			2			2	
$I_{DD(SHDN)}$	Supply current shutdown (per channel)			25°C		0.8	1.5		0.8	1.5	µA
				Full range		1.3	2		1.3	2	

† Full range is − 40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS	T_A†	TLV277xI			TLV277xAI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(ON)}$	Turnon voltage level	TLV2770	A_V = 5	25°C		2.59			2.59		V
		TLV2773				2.47			2.47		
		TLV2775				2.48			2.48		
$V_{(OFF)}$	Turnoff voltage level	TLV2770	A_V = 5	25°C		2.41			2.41		V
		TLV2773				2.32			2.32		
		TLV2775				2.29			2.29		

† Full range is − 40°C to 125°C.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLV277xI			TLV277xAI			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain		$V_{O(PP)}$ = 1.5 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	10.5		5	10.5		V/μs
					Full range	4.7	6		4.7	6		
V_n	Equivalent input noise voltage		f = 1 kHz		25°C		17			17		nV/√Hz
			f = 10 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 0.1 Hz to 1 Hz		25°C		0.33			0.33		μV
			f = 0.1 Hz to 10 Hz		25°C		0.86			0.86		μV
I_n	Equivalent input noise current		f = 100 Hz		25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise		R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.005%			0.005%		
				A_V = 10			0.016%			0.016%		
				A_V = 100			0.095%			0.095%		
	Gain-bandwidth product		f = 10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		5.1			5.1		MHz
t_s	Settling time		A_V = −1, Step = 1.5 V to 3.5 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.134			0.134		μs
				0.01%	25°C		1.97			1.97		
ϕ_m	Phase margin at unity gain		R_L = 600 Ω, C_L = 100 pF		25°C		46°			46°		
	Gain margin				25°C		12			12		dB
$t_{(ON)}$	Amplifier turnon time	TLV2770	A_V = 5, R_L = Open, Measured to 50% point		25°C		1.2			1.2		μs
		TLV2773					2.4			2.4		
		TLV2775					1.9			1.9		
$t_{(OFF)}$	Amplifier turnoff time	TLV2770	A_V = 5, R_L = Open, Measured to 50% point		25°C		335			335		ns
		TLV2773					444			444		
		TLV2775					345			345		

† Full range is −40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772Q TLV2772M			TLV2772AQ TLV2772AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = ±1.35 V, V_{IC} = 0, R_S = 50 Ω	V_O = 0,	25°C		0.44	2.5		0.44	1.6	mV
				Full range		0.47	2.7		0.47	1.9	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
I_{IO}	Input offset current			25°C		1	60		1	60	pA
				Full range		2	125		2	125	
I_{IB}	Input bias current			25°C		2	60		2	60	pA
				Full range		6	350		6	350	
V_{ICR}	Common-mode input voltage range	CMRR > 60 dB,	R_S = 50 Ω	25°C	0 to 1.4	−0.3 to 1.7		0 to 1.4	−0.3 to 1.7		V
				Full range	0 to 1.4	−0.3 to 1.7		0 to 1.4	−0.3 to 1.7		
V_{OH}	High-level output voltage	I_{OH} = −0.675 mA		25°C		2.6			2.6		V
				Full range	2.45			2.45			
		I_{OH} = −2.2 mA		25°C		2.4			2.4		
				Full range	2.1			2.1			
V_{OL}	Low-level output voltage	V_{IC} = 1.35 V,	I_{OL} = 0.675 mA	25°C		0.1			0.1		V
				Full range			0.2			0.2	
		V_{IC} = 1.35 V,	I_{OL} = 2.2 mA	25°C		0.21			0.21		
				Full range			0.6			0.6	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.35 V, V_O = 0.6 V to 2.1 V	R_L = 10 kΩ,‡	25°C	20	380		20	380		V/mV
				Full range	13			13			
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		25			25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} (min), R_S = 50 Ω	V_O = 1.5 V,	25°C	60	84		60	84		dB
				Full range	60	82		60	82		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	70	89		70	89		dB
				Full range	70	84		70	84		
I_{DD}	Supply current (per channel)	V_O = 1.5 V,	No load	25°C		1	2		1	2	mA
				Full range			2			2	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 1.35 V

operating characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772Q TLV2772M			TLV2772AQ TLV2772AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	9		5	9		V/μs
				Full range	4.7	6		4.7	6		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		21			21		nV/√Hz
		f = 10 kHz		25°C		17			17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33			0.33		μV
		f = 0.1 Hz to 10 Hz		25°C		0.86			0.86		μV
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.0085%			0.0085%		
			A_V = 10			0.025%			0.025%		
			A_V = 100			0.12%			0.12%		
	Gain-bandwidth product	f = 10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		4.8			4.8		MHz
t_s	Settling time	A_V = −1, Step = 0.85 V to 1.85 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.186			0.186		μs
			0.01%	25°C		3.92			3.92		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		46°			46°		
	Gain margin			25°C		12			12		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772Q TLV2772M			TLV2772AQ TLV2772AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = ±2.5 V, V_{IC} = 0,	V_O = 0, R_S = 50 Ω	25°C		0.36	2.5		0.36	1.6	mV
				Full range		0.4	2.7		0.4	1.9	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
I_{IO}	Input offset current			25°C		1	60		1	60	pA
				Full range		2	125		2	125	
I_{IB}	Input bias current			25°C		2	60		2	60	pA
				Full range		6	350		6	350	
V_{ICR}	Common-mode input voltage range	CMRR > 60 dB,	R_S = 50 Ω	25°C	0 to 3.7	−0.3 to 3.8		0 to 3.7	−0.3 to 3.8		V
				Full range	0 to 3.7	−0.3 to 3.8		0 to 3.7	−0.3 to 3.8		
V_{OH}	High-level output voltage	I_{OH} = −1.3 mA		25°C		4.9			4.9		V
				Full range	4.8			4.8			
		I_{OH} = −4.2 mA		25°C		4.7			4.7		
				Full range	4.4			4.4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 1.3 mA	25°C		0.1			0.1		V
				Full range			0.2			0.2	
		V_{IC} = 2.5 V,	I_{OL} = 4.2 mA	25°C		0.21			0.21		
				Full range			0.6			0.6	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ,‡	25°C	20	450		20	450		V/mV
				Full range	13			13			
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		20			20		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} (min), R_S = 50 Ω	V_O = 3.7 V,	25°C	60	96		60	96		dB
				Full range	60	93		60	93		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	70	89		70	89		dB
				Full range	70	84		70	84		
I_{DD}	Supply current (per channel)	V_O = 1.5 V,	No load	25°C		1	2		1	2	mA
				Full range			2			2	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772Q TLV2772M			TLV2772AQ TLV2772AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 1.5 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	10.5		5	10.5		V/μs
				Full range	4.7	6		4.7	6		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		17			17		nV/√Hz
		f = 10 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33			0.33		μV
		f = 0.1 Hz to 10 Hz		25°C		0.86			0.86		μV
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.005%			0.005%		
			A_V = 10			0.016%			0.016%		
			A_V = 100			0.095%			0.095%		
	Gain-bandwidth product	f = 10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		5.1			5.1		MHz
t_s	Settling time	A_V = −1, Step = 1.5 V to 3.5 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.134			0.134		μs
			0.01%	25°C		1.97			1.97		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		46°			46°		
	Gain margin			25°C		12			12		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

TYPICAL CHARACTERISTICS

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I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	14 15
V_O	Output voltage	vs Differential input voltage	16
A_{VD}	Large-signal differential voltage amplification and phase margin	vs Frequency	17,18
A_{VD}	Differential voltage amplification	vs Load resistance vs Free-air temperature	19 20,21
z_o	Output impedance	vs Frequency	22,23
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	24 25
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	26,27
I_{DD}	Supply current (per channel)	vs Supply voltage	28
SR	Slew rate	vs Load capacitance vs Free-air temperature	29 30
V_O	Voltage-follower small-signal pulse response		31,32
V_O	Voltage-follower large-signal pulse response		33,34
V_O	Inverting small-signal pulse response		35,36
V_O	Inverting large-signal pulse response		37,38
V_n	Equivalent input noise voltage	vs Frequency	39,40
	Noise voltage (referred to input)	Over a 10-second period	41
THD + N	Total harmonic distortion plus noise	vs Frequency	42,43
	Gain-bandwidth product	vs Supply voltage	44
B_1	Unity-gain bandwidth	vs Load capacitance	45
ϕ_m	Phase margin	vs Load capacitance	46
	Gain margin	vs Load capacitance	47
	Amplifier with shutdown pulse turnon/off characteristics		48 − 50
	Supply current with shutdown pulse turnon/off characteristics		51 − 53
	Shutdown supply current	vs Free-air temperature	54
	Shutdown forward/reverse isolation	vs Frequency	55, 56

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2772
INPUT OFFSET VOLTAGE

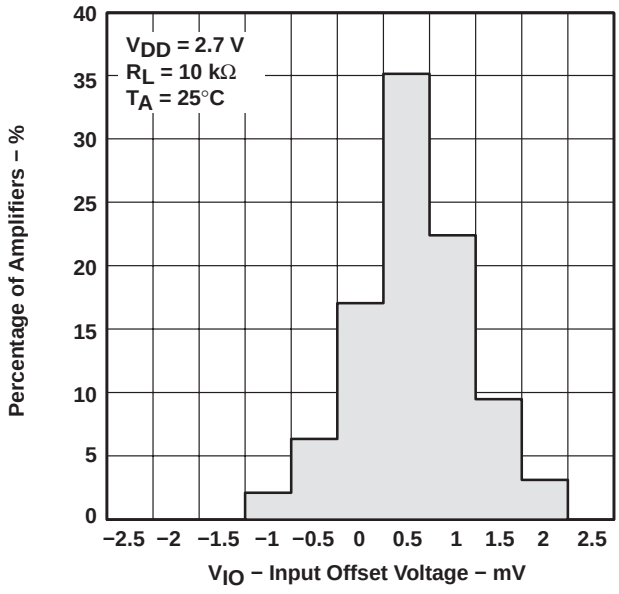


Figure 1

DISTRIBUTION OF TLV2772
INPUT OFFSET VOLTAGE

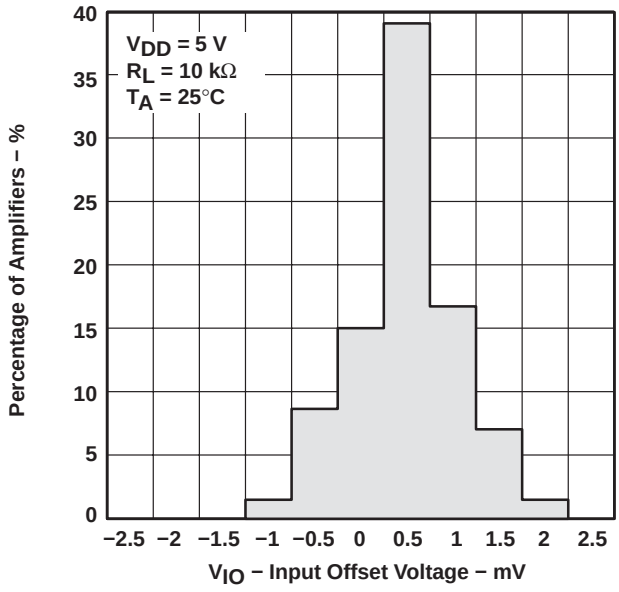


Figure 2

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

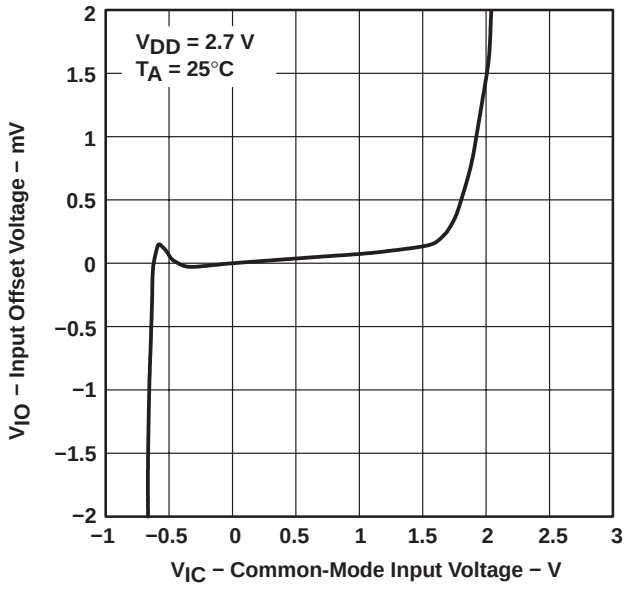


Figure 3

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

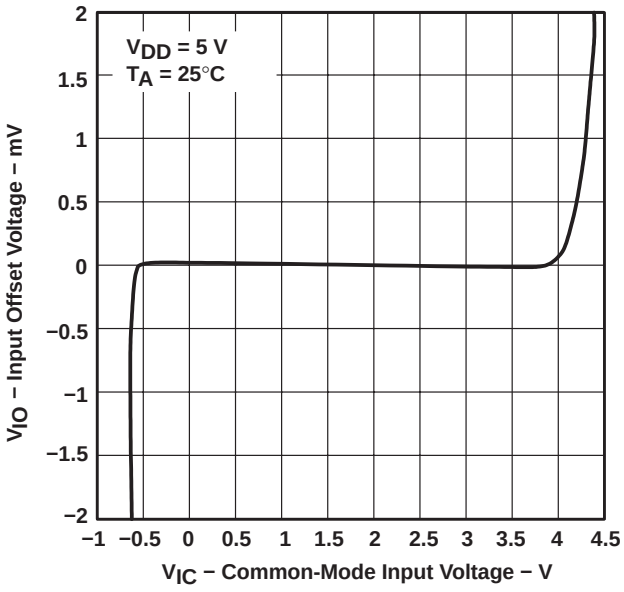


Figure 4

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2772
INPUT OFFSET VOLTAGE

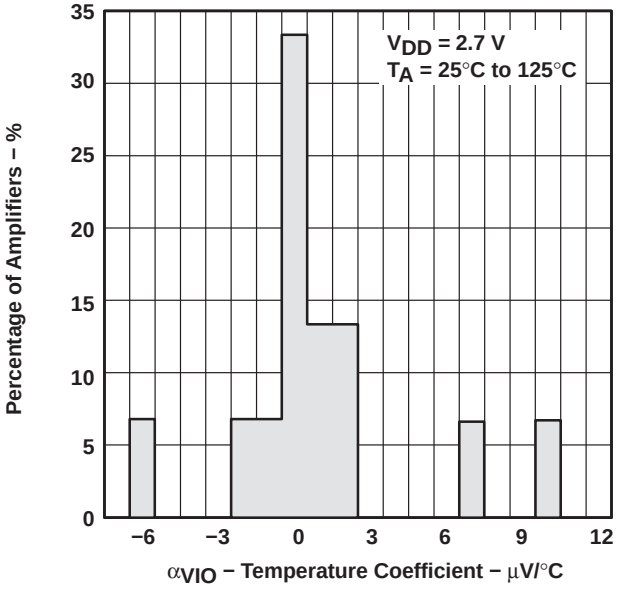


Figure 5

DISTRIBUTION OF TLV2772
INPUT OFFSET VOLTAGE

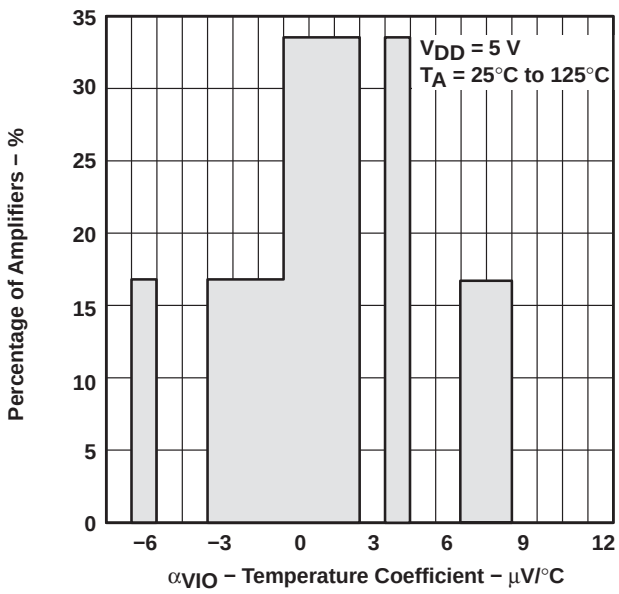


Figure 6

INPUT BIAS AND OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

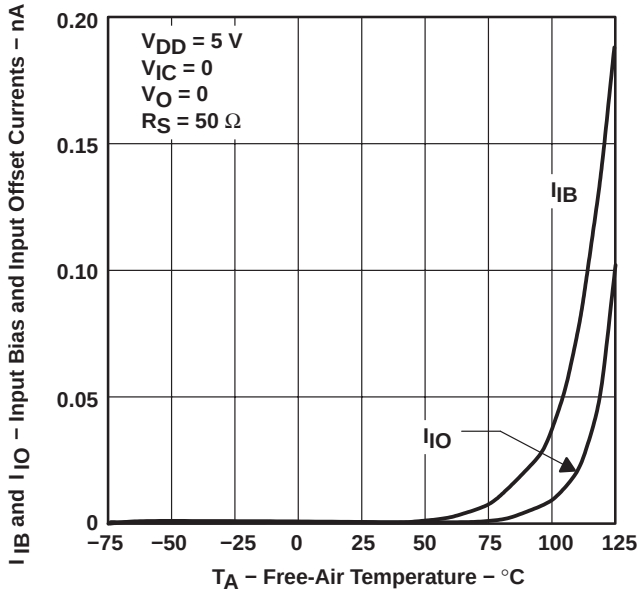


Figure 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

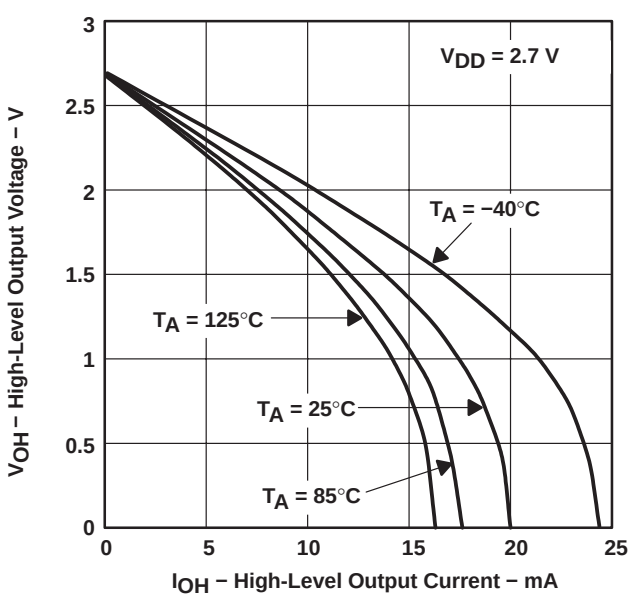


Figure 8

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

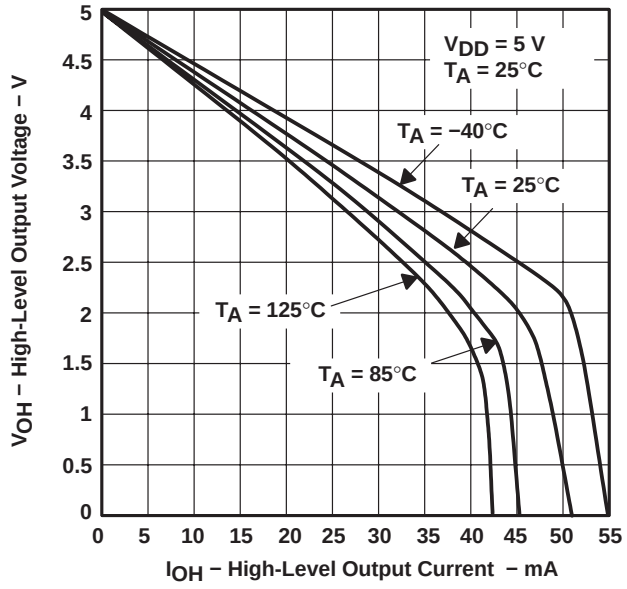


Figure 9

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

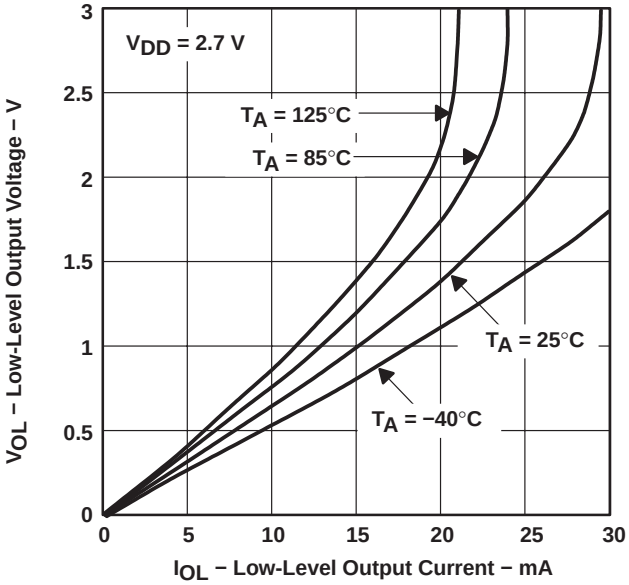


Figure 10

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

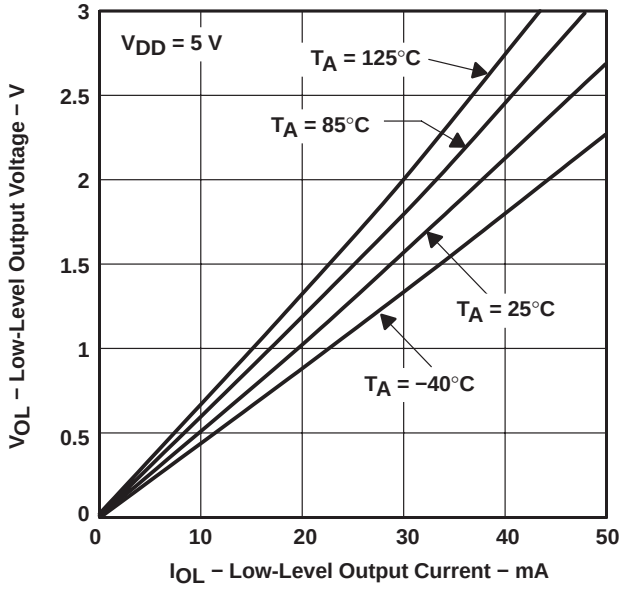


Figure 11

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

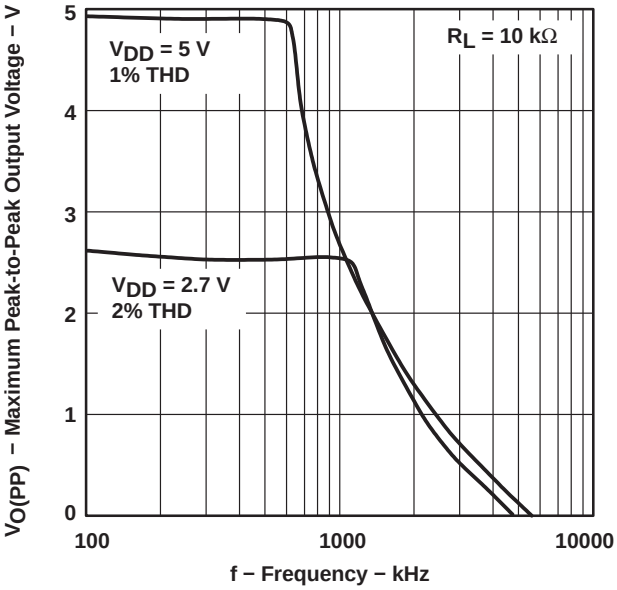


Figure 12

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

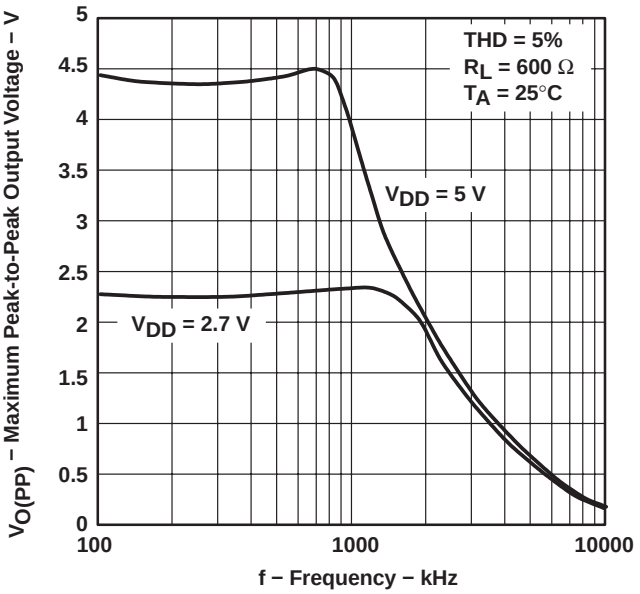


Figure 13

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

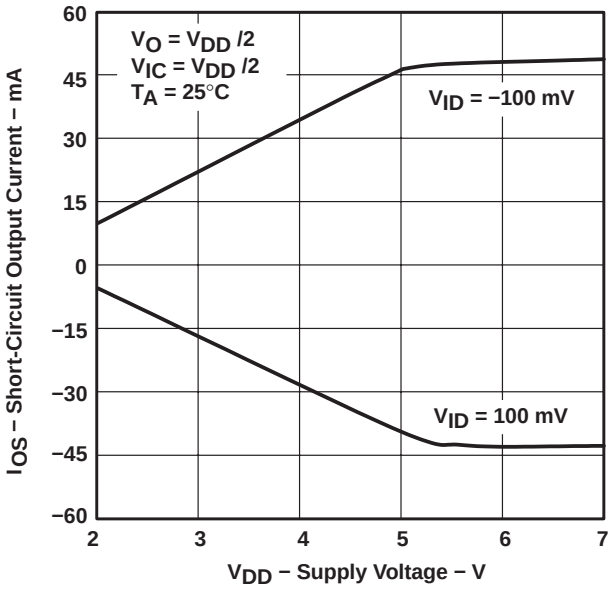


Figure 14

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

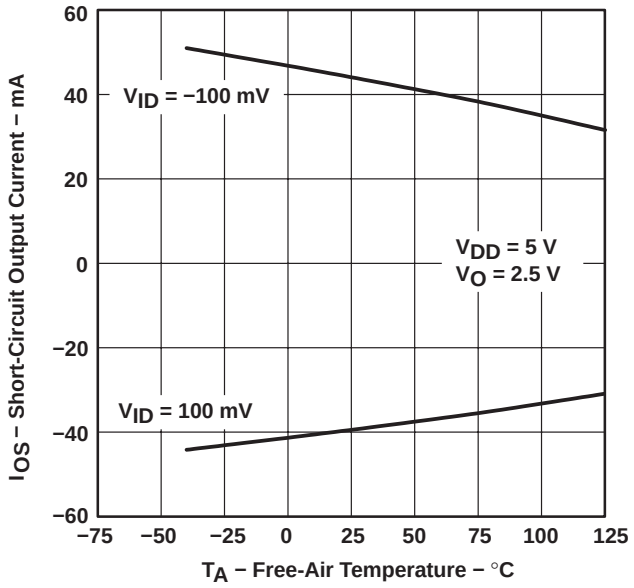


Figure 15

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

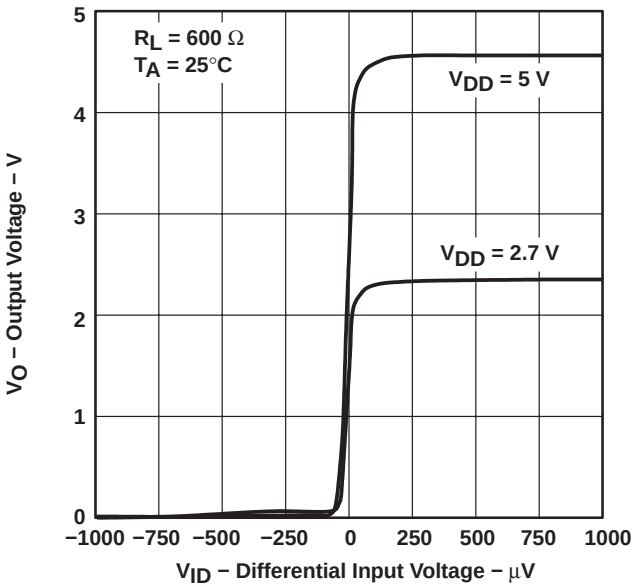


Figure 16

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

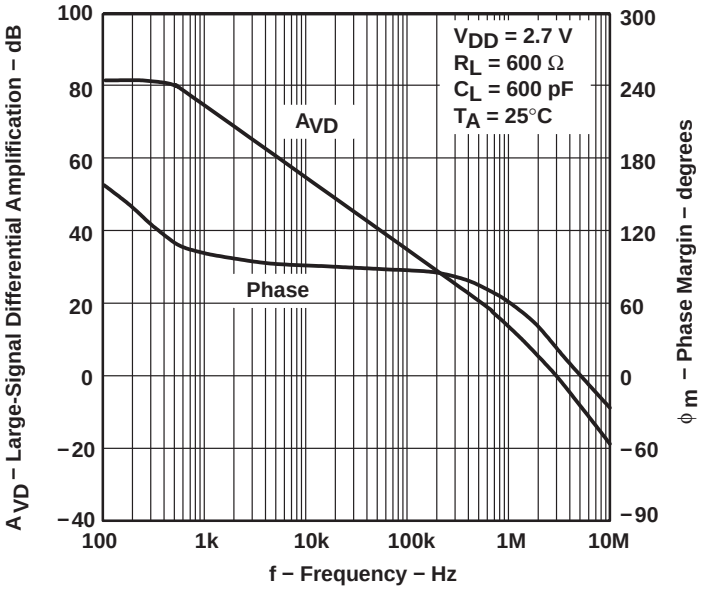


Figure 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

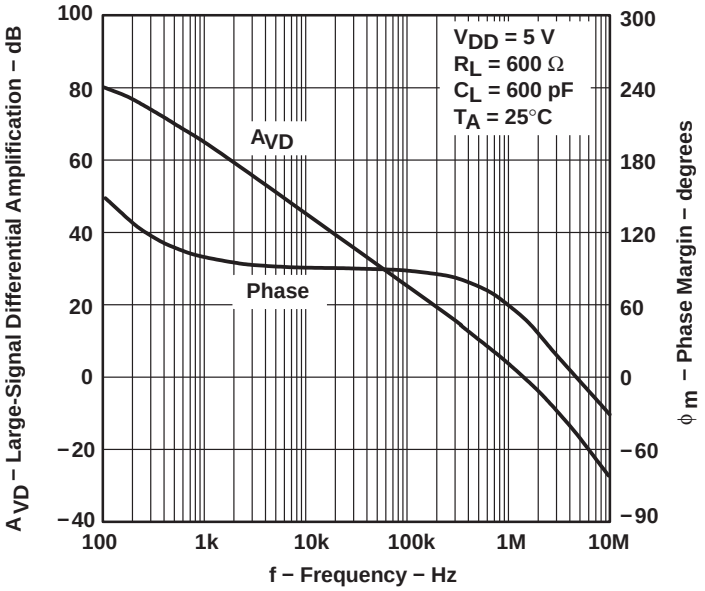


Figure 18

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

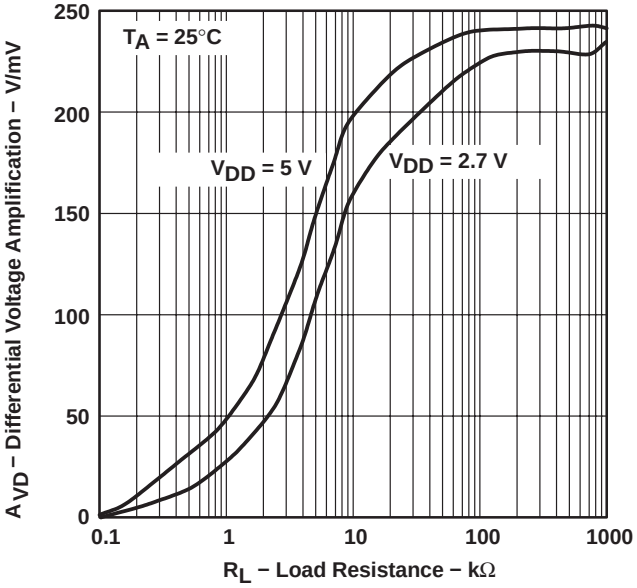


Figure 19

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

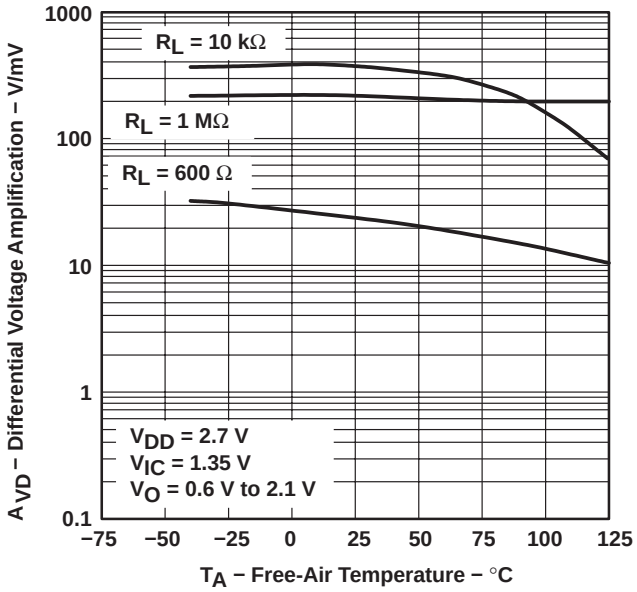


Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

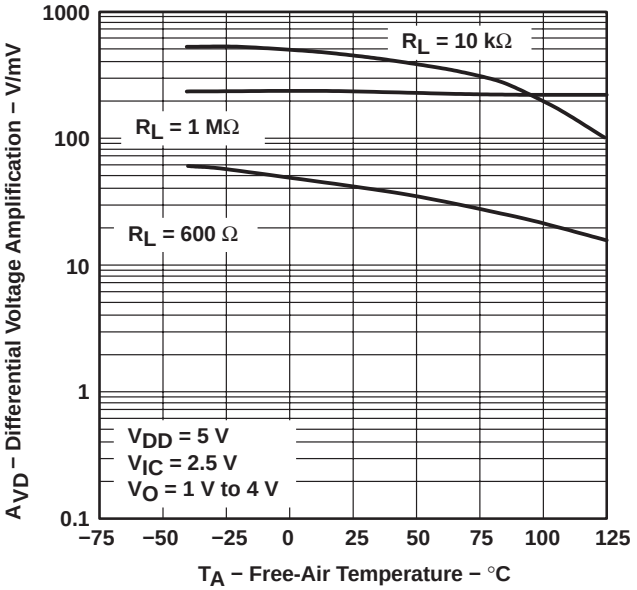


Figure 21

OUTPUT IMPEDANCE vs FREQUENCY

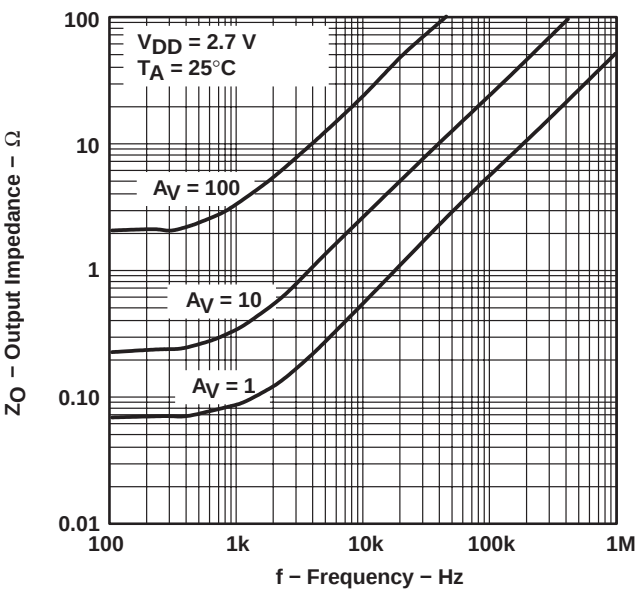


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE vs FREQUENCY

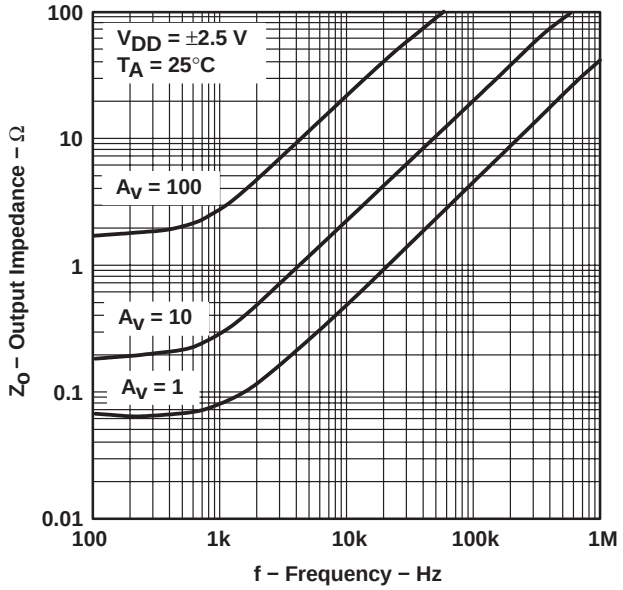


Figure 23

COMMON-MODE REJECTION RATIO vs FREQUENCY

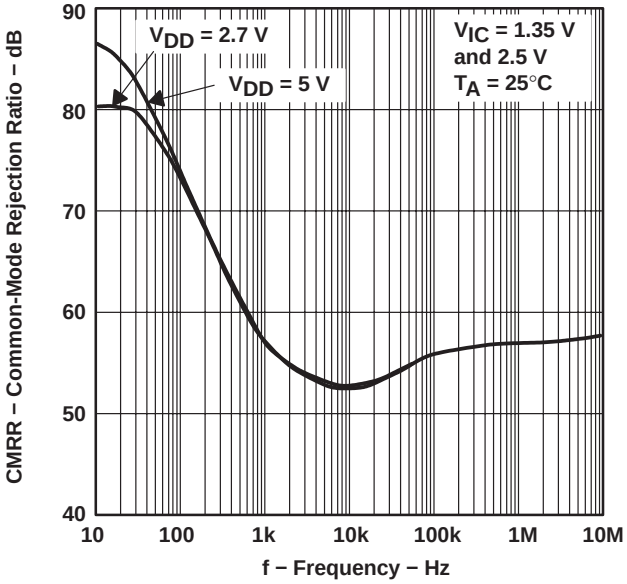


Figure 24

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

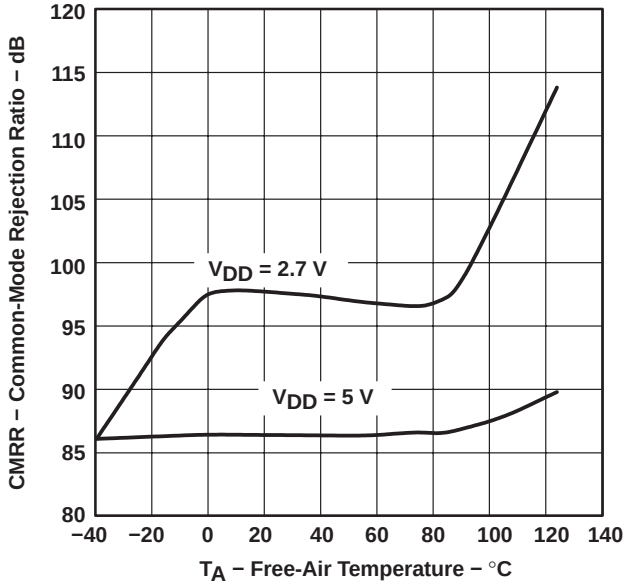


Figure 25

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

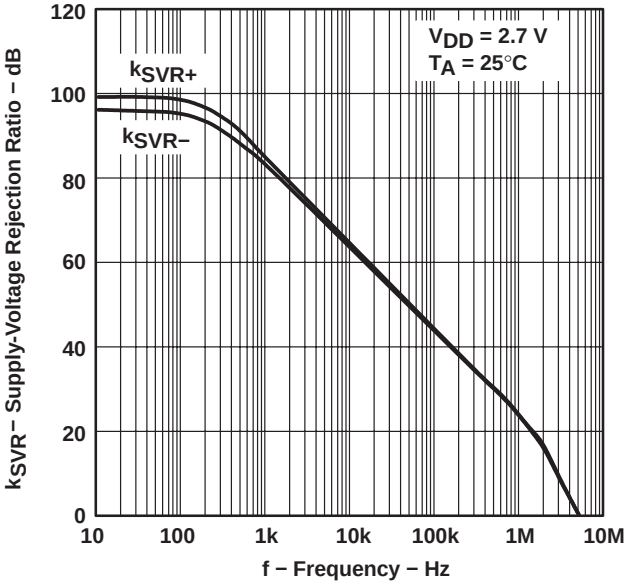


Figure 26

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

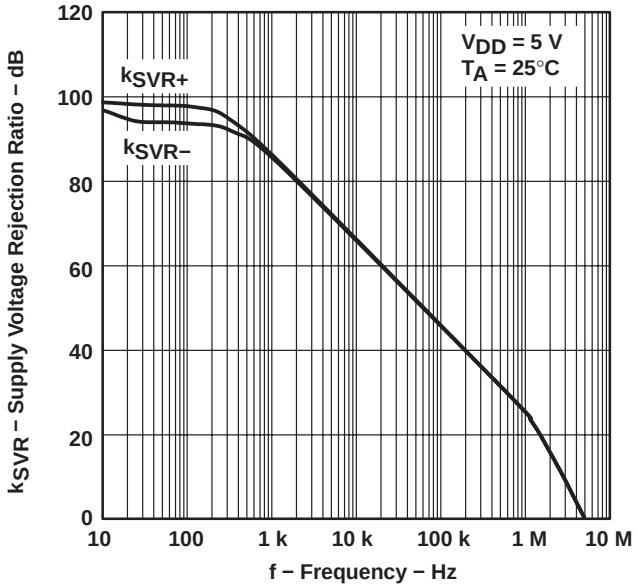


Figure 27

SUPPLY CURRENT (PER CHANNEL)
vs
SUPPLY VOLTAGE

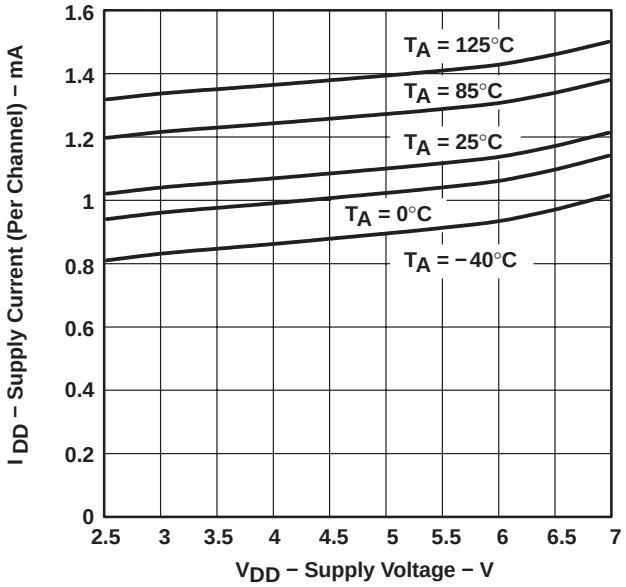


Figure 28

SLEW RATE
vs
LOAD CAPACITANCE

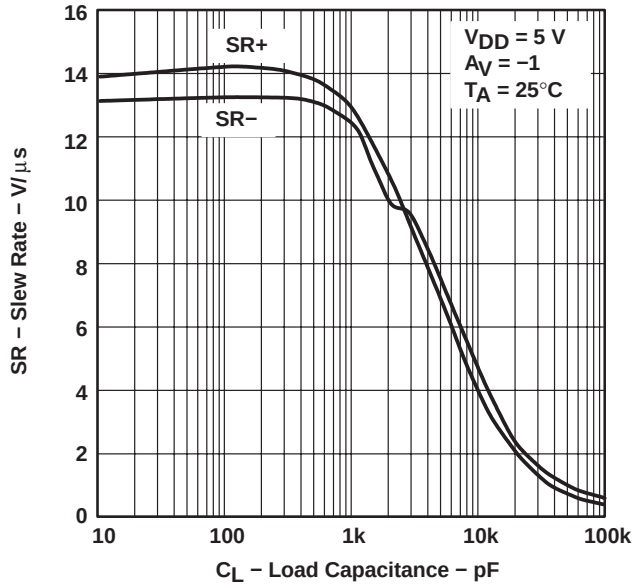


Figure 29

SLEW RATE
vs
FREE-AIR TEMPERATURE

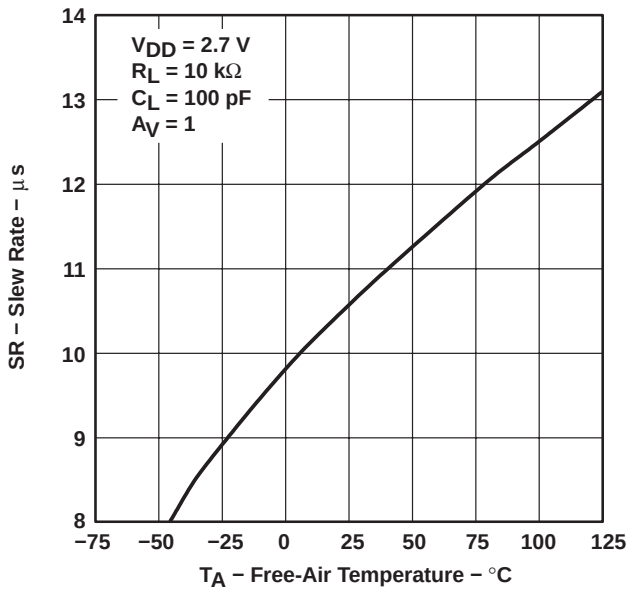


Figure 30

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

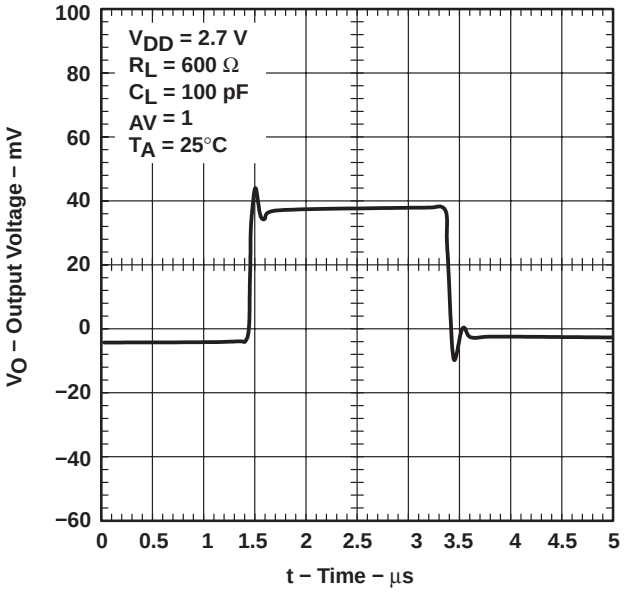


Figure 31

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

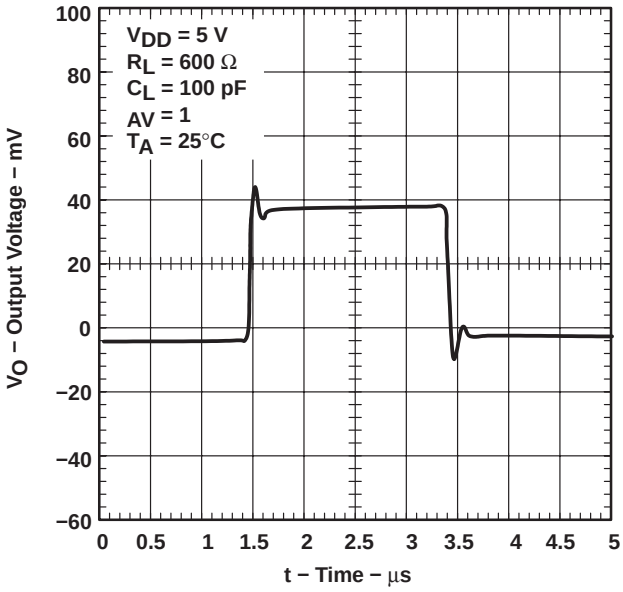


Figure 32

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

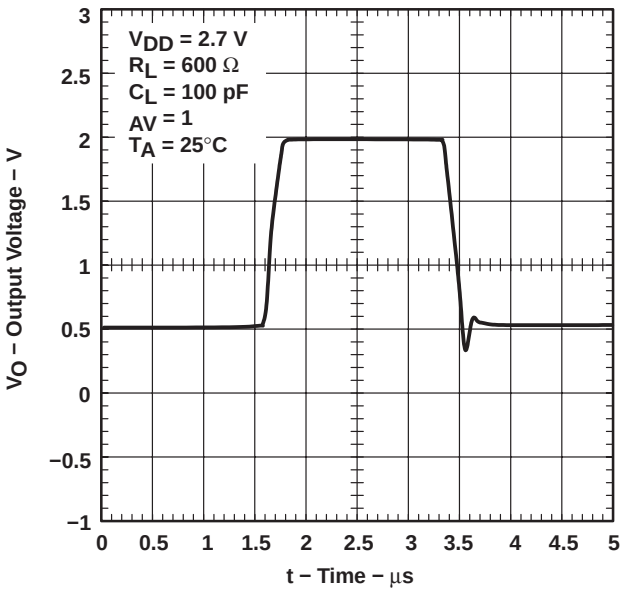


Figure 33

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

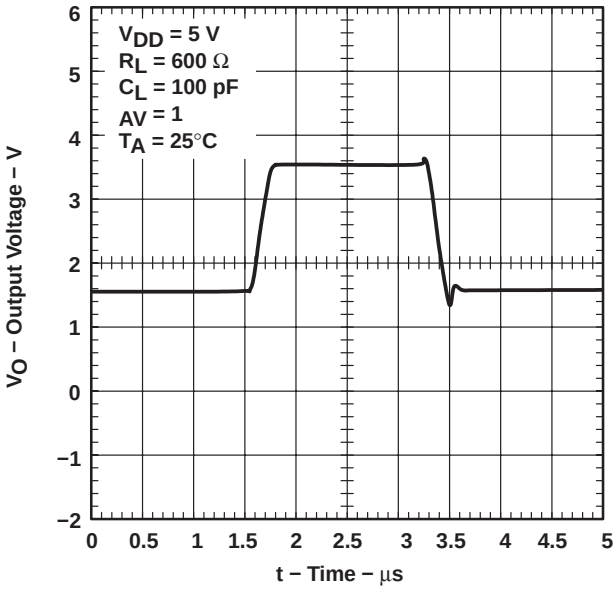


Figure 34

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE

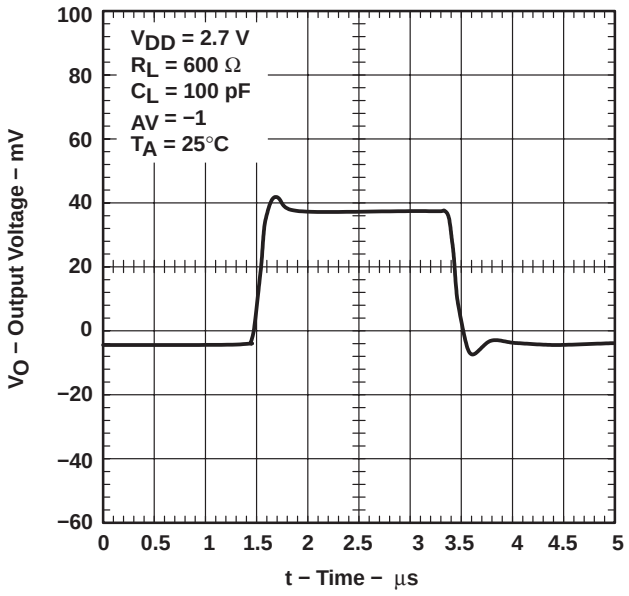


Figure 35

INVERTING SMALL-SIGNAL PULSE RESPONSE

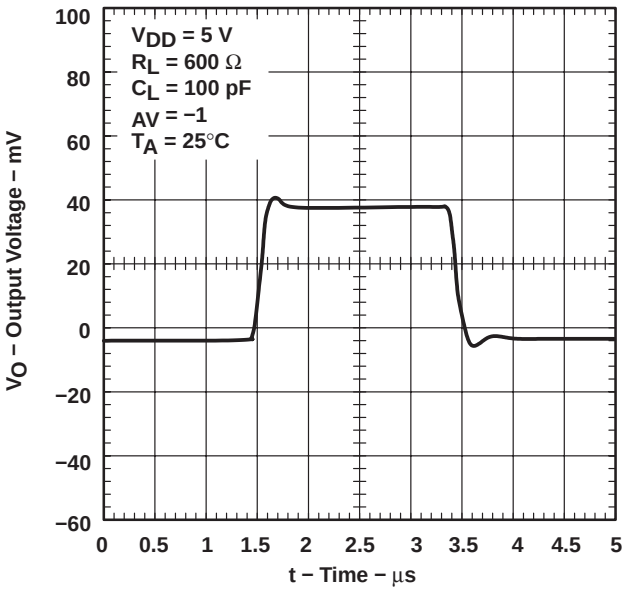


Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE

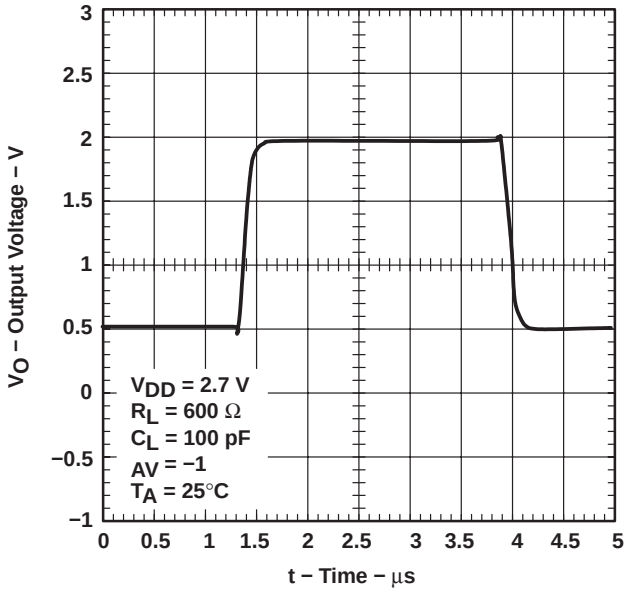


Figure 37

INVERTING LARGE-SIGNAL PULSE RESPONSE

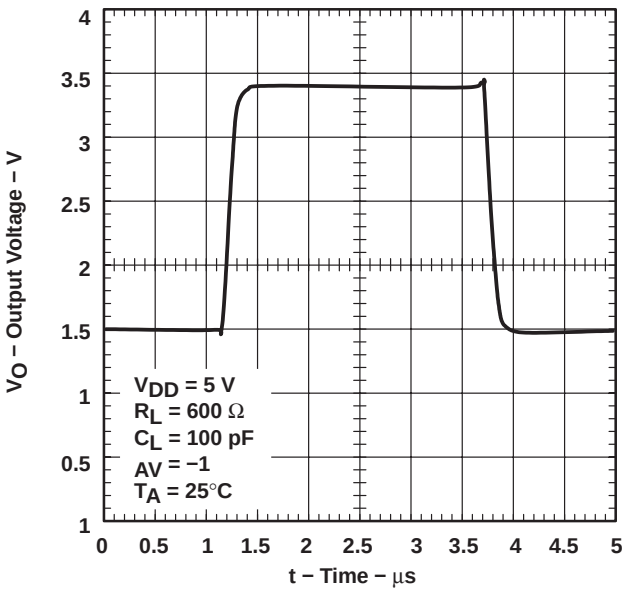


Figure 38

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

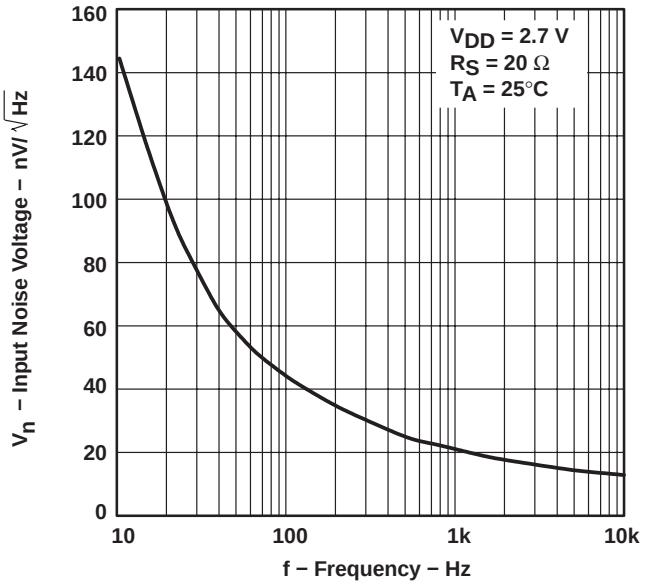


Figure 39

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

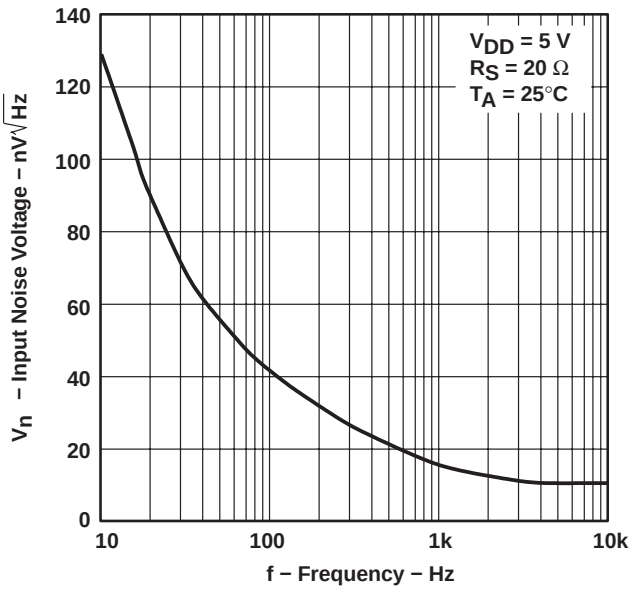


Figure 40

NOISE VOLTAGE
OVER A 10 SECOND PERIOD

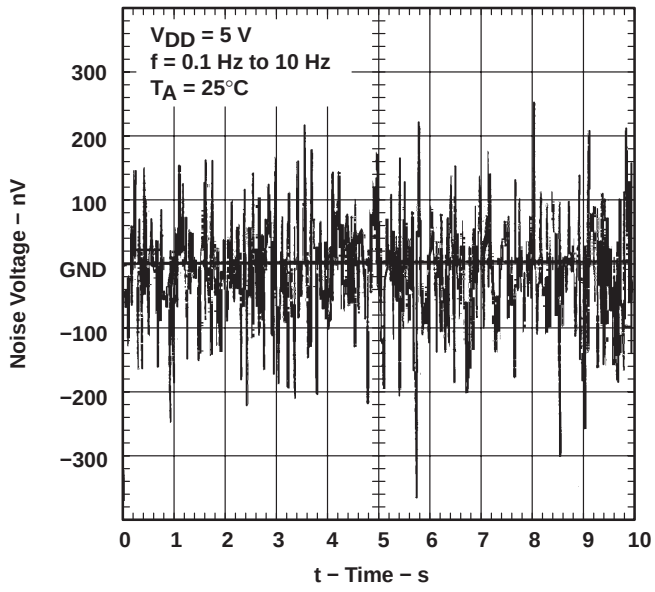


Figure 41

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

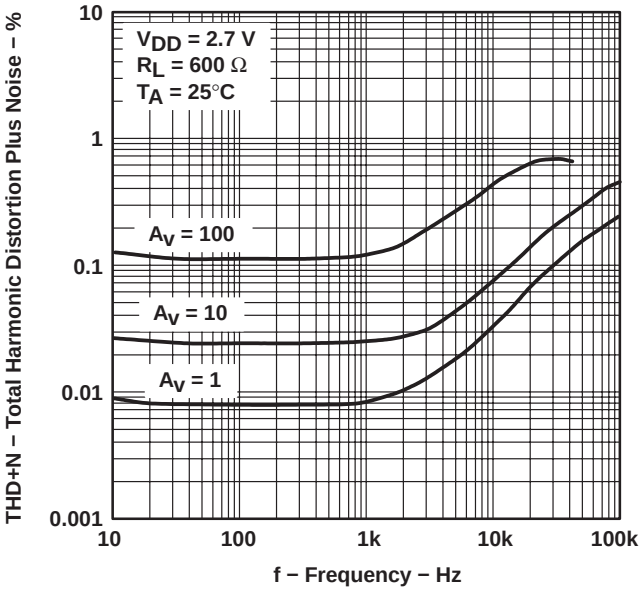


Figure 42

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

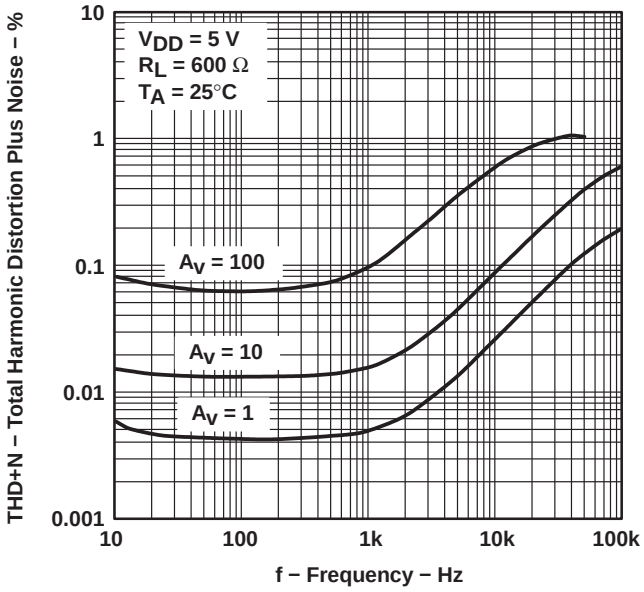


Figure 43

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

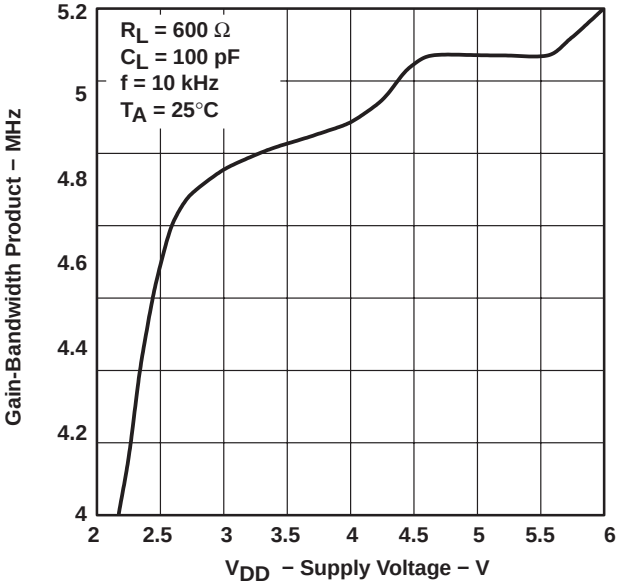


Figure 44

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

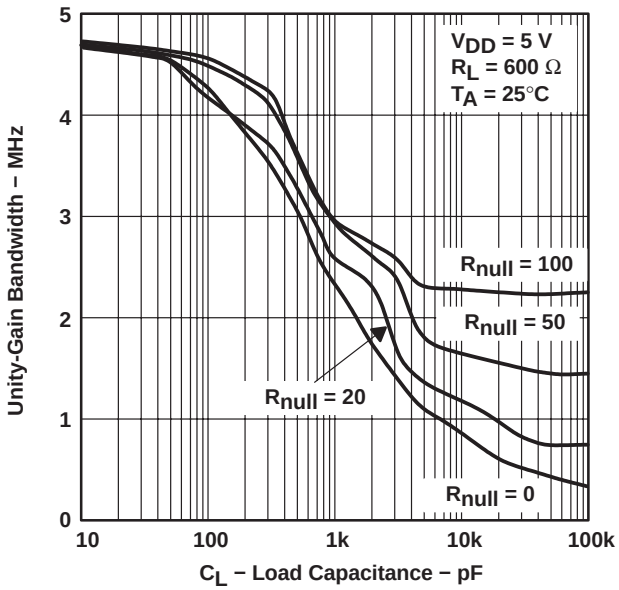


Figure 45

TYPICAL CHARACTERISTICS

PHASE MARGIN vs LOAD CAPACITANCE

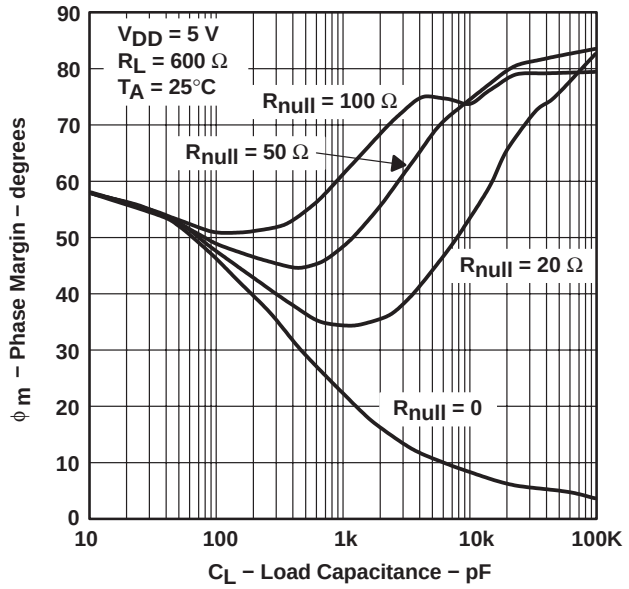


Figure 46

GAIN MARGIN vs LOAD CAPACITANCE

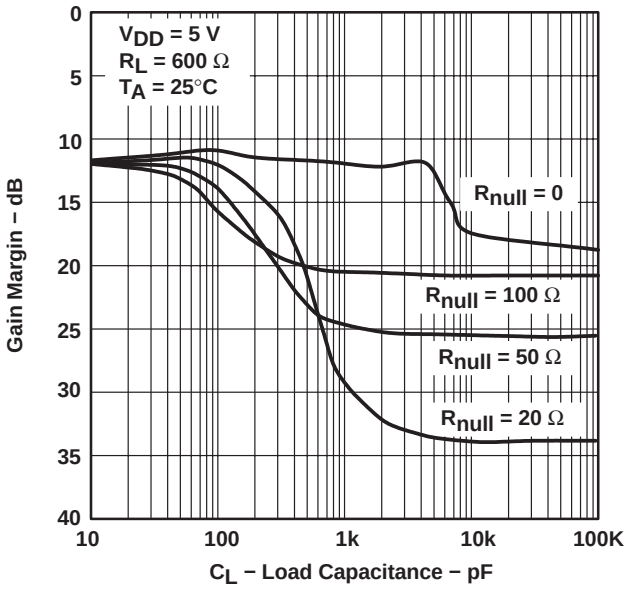


Figure 47

TLV2770 AMPLIFIER WITH SHUTDOWN PULSE TURNON/OFF CHARACTERISTICS

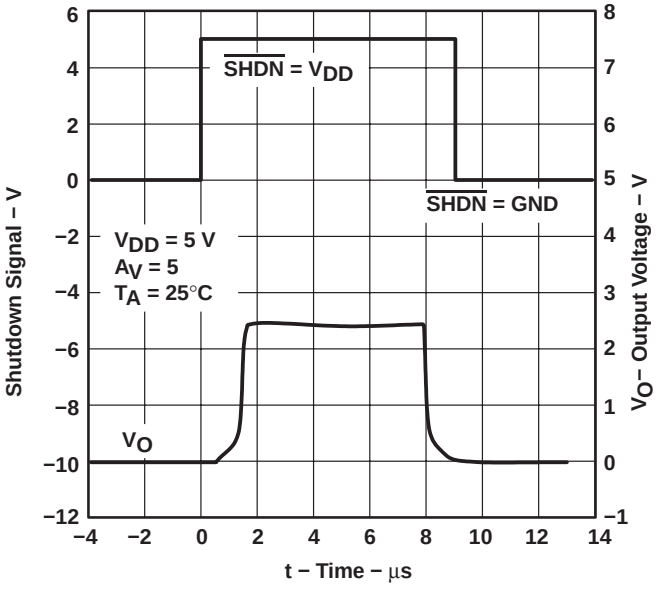


Figure 48

TLV2773 AMPLIFIER WITH SHUTDOWN PULSE TURNON/OFF CHARACTERISTICS

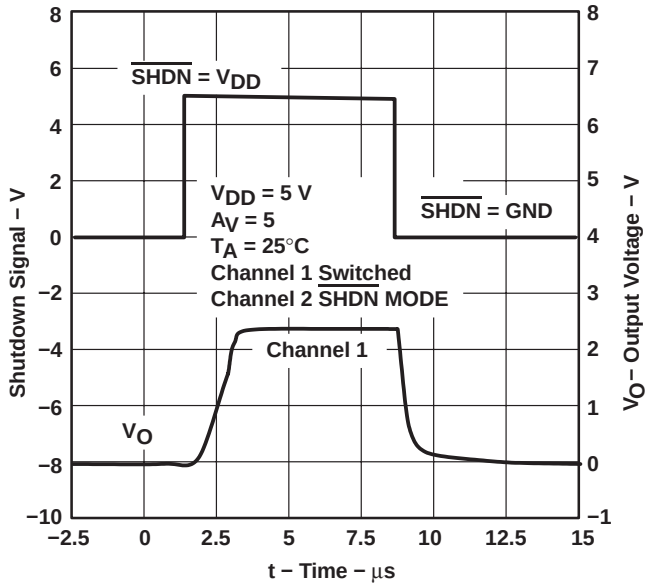


Figure 49

TYPICAL CHARACTERISTICS

TLV2775 − CHANNEL 1
AMPLIFIER WITH SHUTDOWN PULSE
TURNON/OFF CHARACTERISTICS

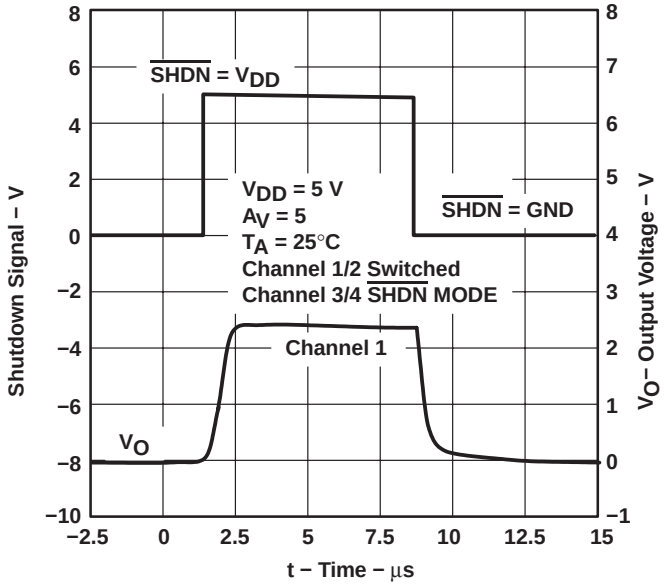


Figure 50

TLV2770
SUPPLY CURRENT WITH SHUTDOWN PULSE
TURNON/OFF CHARACTERISTICS

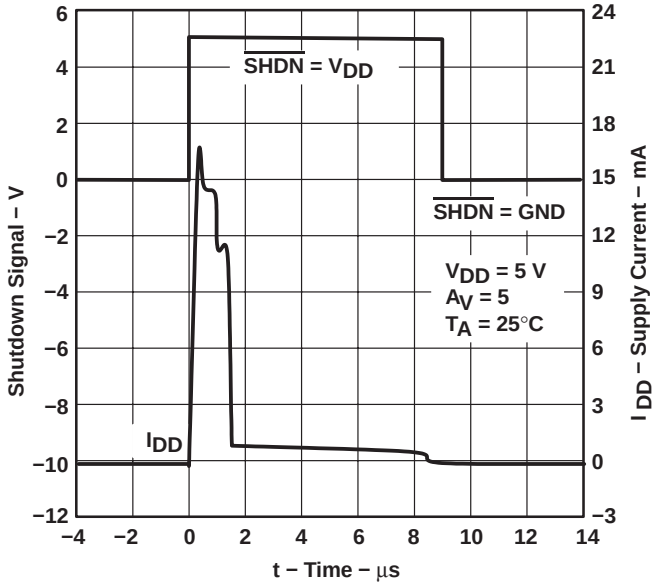


Figure 51

TLV2773
SUPPLY CURRENT WITH SHUTDOWN PULSE
TURNON/OFF CHARACTERISTICS

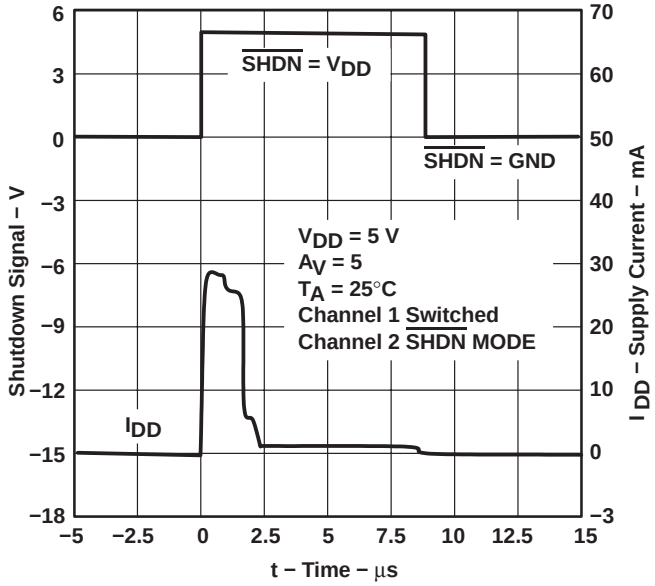


Figure 52

TLV2775
SUPPLY CURRENT WITH SHUTDOWN PULSE
TURNON/OFF CHARACTERISTICS

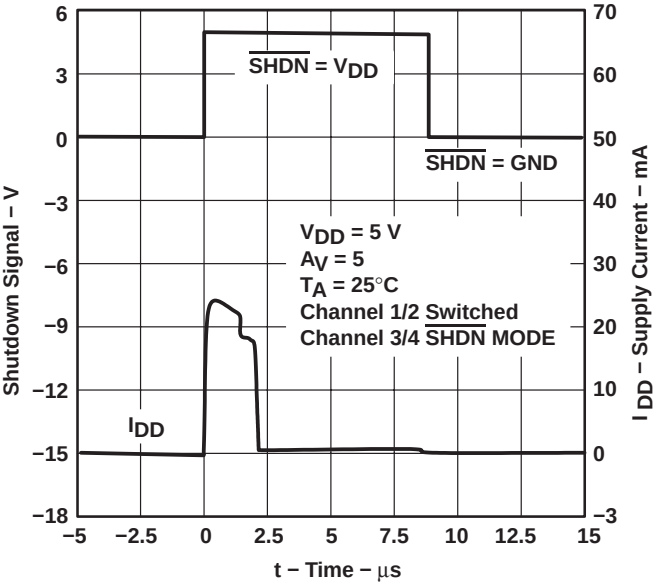


Figure 53

TYPICAL CHARACTERISTICS

SHUTDOWN SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

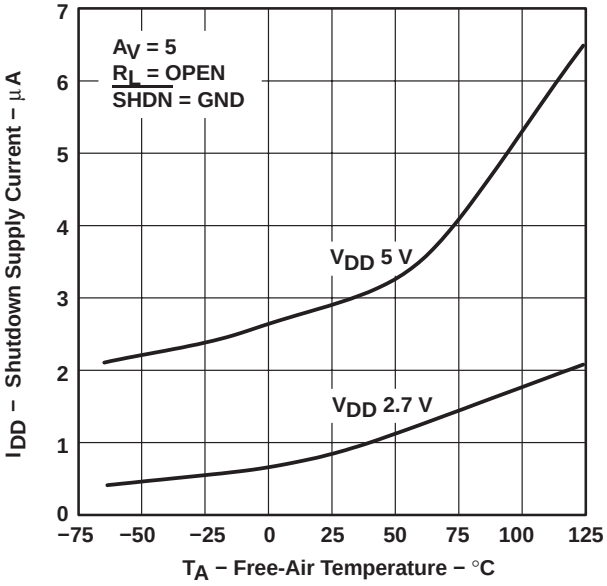


Figure 54

TLV2770
SHUTDOWN FORWARD ISOLATION
vs
FREQUENCY

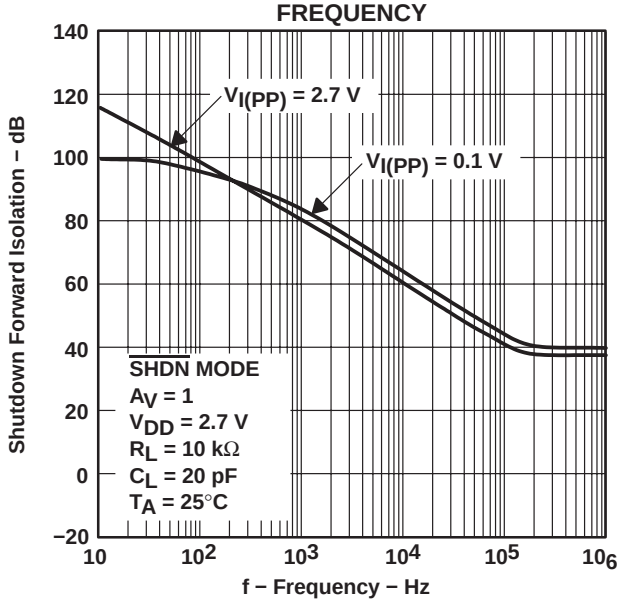


Figure 55

TLV2770
SHUTDOWN REVERSE ISOLATION
vs
FREQUENCY

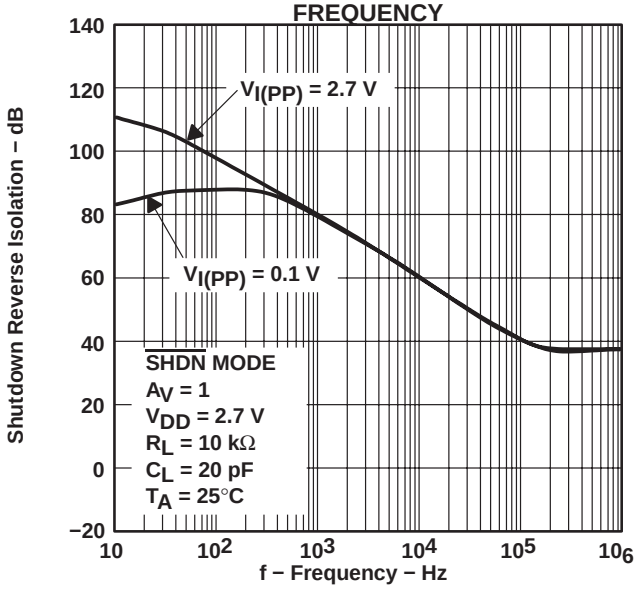


Figure 56

PARAMETER MEASUREMENT INFORMATION

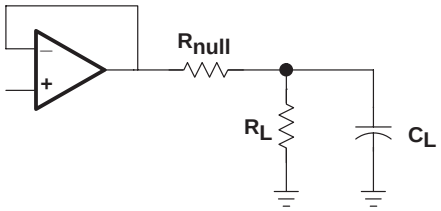


Figure 57

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 58. A minimum value of 20 Ω should work well for most applications.

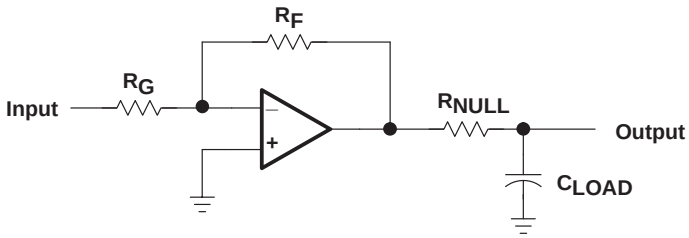
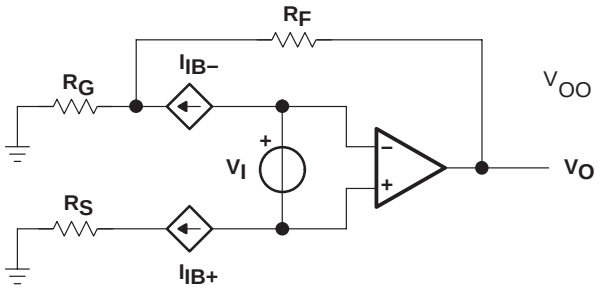


Figure 58. Driving a Capacitive Load

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

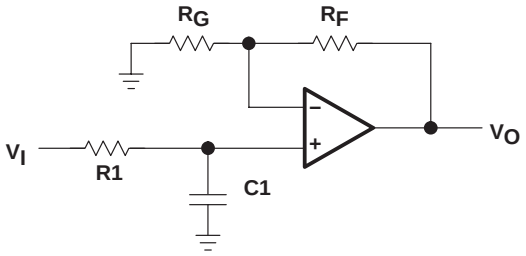


$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+} R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-} R_F$$

Figure 59. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 60).

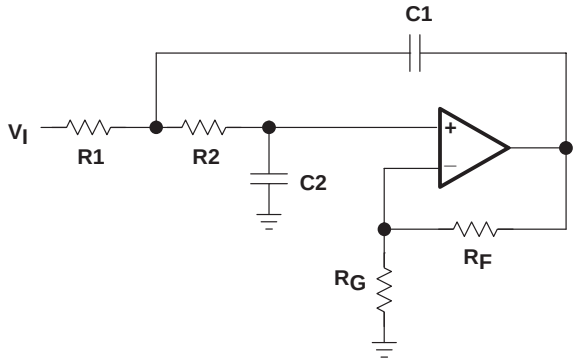


$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 60. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 61. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

using the TLV2772 as an accelerometer interface

The schematic, shown in Figure 62, shows the ACH04-08-05 interfaced to the TLV1544 10-bit analog-to-digital converter (ADC).

The ACH04-08-05 is a shock sensor designed to convert mechanical acceleration into electrical signals. The sensor contains three piezoelectric sensing elements oriented to simultaneously measure acceleration in three orthogonal, linear axes (x, y, z). The operating frequency is 0.5 Hz to 5 kHz. The output is buffered with an internal JFET and has a typical output voltage of 1.80 mV/g for the x and y axis and 1.35 mV/g for the z axis.

Amplification and frequency shaping of the shock sensor output is done by the TLV2772 rail-to-rail operational amplifier. The TLV2772 is ideal for this application as it offers high input impedance, good slew rate, and excellent dc precision. The rail-to-rail output swing and high output drive are perfect for driving the analog input of the TLV1544 ADC.

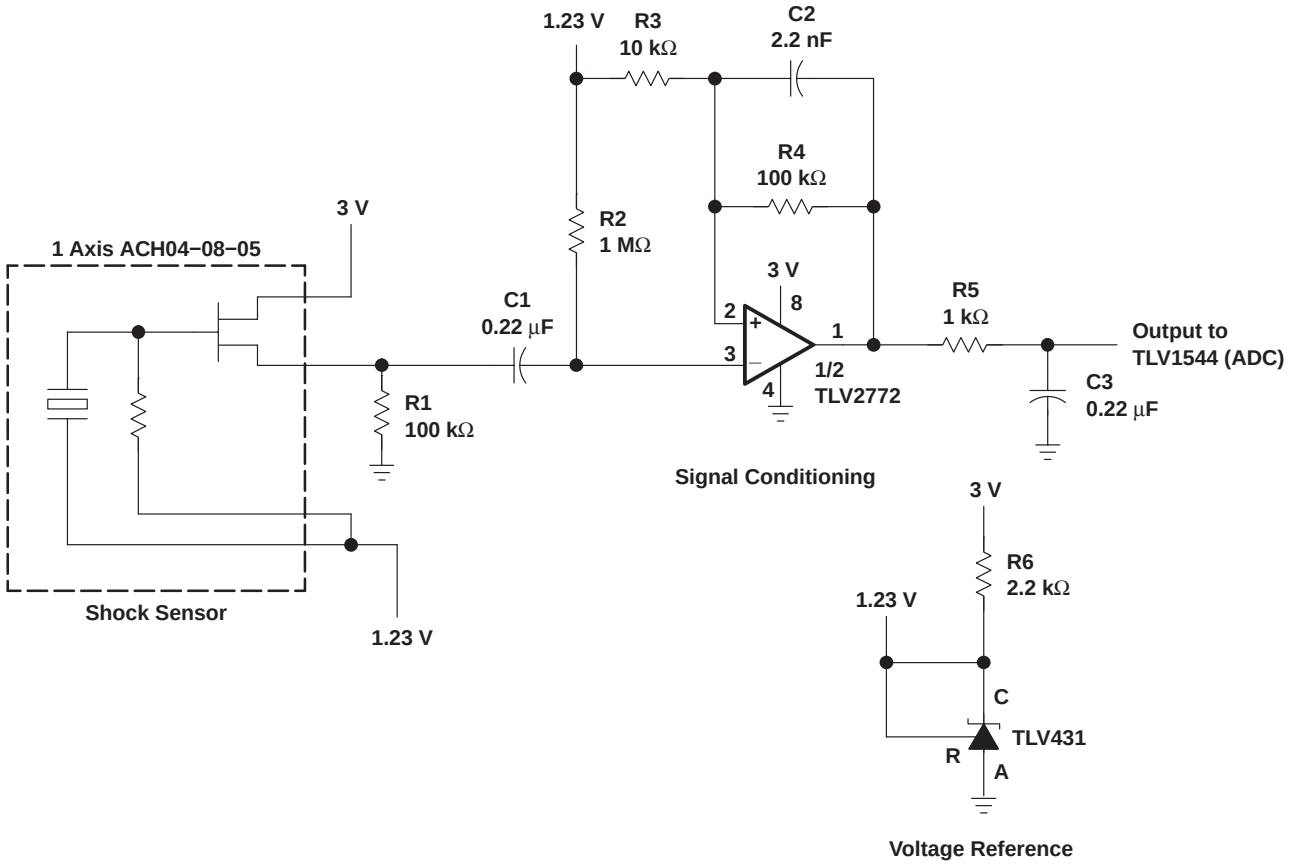


Figure 62. Accelerometer Interface Schematic

The sensor signal must be amplified and frequency-shaped to provide a signal the ADC can properly convert into the digital domain. Figure 62 shows the topology used in this application for one axis of the sensor. This system is powered from a single 3-V supply. Configuring the TLV431 with a 2.2-kΩ resistor produces a reference voltage of 1.23 V. This voltage is used to bias the operational amplifier and the internal JFETs in the shock sensor.

APPLICATION INFORMATION

gain calculation

Since the TLV2772 is capable of rail-to-rail output using a 3-V supply, V_O = 0 (min) to 3 V (max). With no signal from the sensor, nominal V_O = reference voltage = 1.23 V. Therefore, the maximum negative swing from nominal is 0 V − 1.23 V = −1.23 V and the maximum positive swing is 3 V − 1.23 V = 1.77 V. By modeling the shock sensor as a low impedance voltage source with output of 2.25 mV/g (max) in the x and y axis and 1.70 mV/g (max) in the z axis, the gain of the circuit is calculated by equation 1.

$$\text{Gain} = \frac{\text{Output Swing}}{\text{Sensor Signal} \times \text{Acceleration}} \quad (1)$$

To avoid saturation of the operational amplifier, the gain calculations are based on the maximum negative swing of −1.23 V and the maximum sensor output of 2.25 mV/g (x and y axis) and 1.70 mV/g (z axis).

$$\text{Gain (x, y)} = \frac{-1.23\ \text{V}}{2.25\ \text{mV/g} \times -50\ \text{g}} = 10.9 \quad (2)$$

and

$$\text{Gain (z)} = \frac{-1.23\ \text{V}}{1.70\ \text{mV/g} \times -50\ \text{g}} = 14.5 \quad (3)$$

By selecting R3 = 10 kΩ and R4 = 100 kΩ, in the x and y channels, a gain of 11 is realized. By selecting R3 = 7.5 kΩ and R4 = 100 kΩ, in the z channel, a gain of 14.3 is realized. The schematic shows the configuration for either the x- or y-axis.

bandwidth calculation

To calculate the component values for the frequency shaping characteristics of the signal conditioning circuit, 1 Hz and 500 Hz are selected as the minimum required 3-dB bandwidth.

To minimize the value of the input capacitor (C1) required to set the lower cutoff frequency requires a large value resistor for R2 is required. A 1-MΩ resistor is used in this example. To set the lower cutoff frequency, the required capacitor value for C1 is:

$$C1 = \frac{1}{2\pi f_{LOW} R_2} = 0.159\ \mu\text{F} \quad (4)$$

Using a value of 0.22 μF, a more common value of capacitor, the lower cutoff frequency is 0.724 Hz.

To minimize the phase shift in the feedback loop caused by the input capacitance of the TLV2772, it is best to minimize the value of the feedback resistor R4. However, to reduce the required capacitance in the feedback loop a large value for R4 is required. Therefore, a compromise for the value of R4 must be made. In this circuit, a value of 100 kΩ has been selected. To set the upper cutoff frequency, the required capacitor value for C2 is:

$$C2 = \frac{1}{2\pi f_{HIGH} R_4} = 3.18\ \mu\text{F} \quad (5)$$

Using a 2.2-nF capacitor, the upper cutoff frequency is 724 Hz.

R5 and C3 also cause the signal response to roll off. Therefore, it is beneficial to design this roll-off point to begin at the upper cutoff frequency. Assuming a value of 1 kΩ for R5, the value for C3 is calculated to be 0.22 μF.

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV277x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

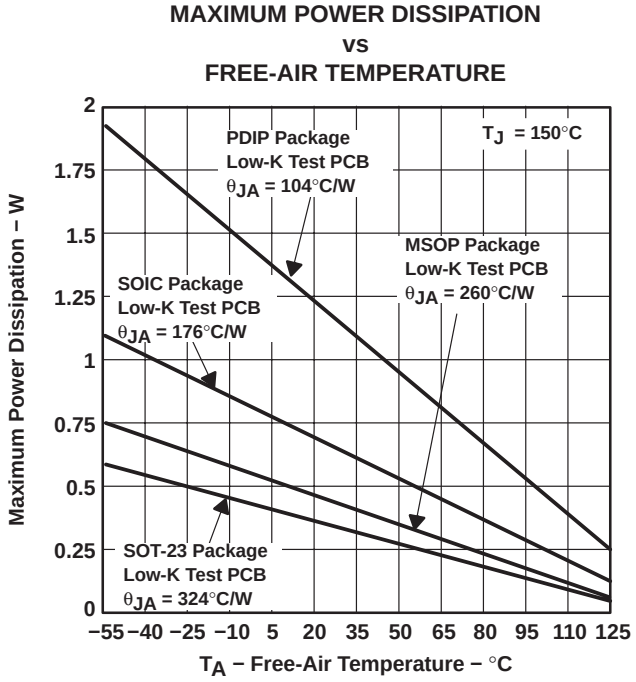
general power dissipation considerations

For a given θ_{JA}, the maximum power dissipation is shown in Figure 63 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of TLV277x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 63. Maximum Power Dissipation vs Free-Air Temperature

APPLICATION INFORMATION

shutdown function

Three members of the TLV277x family (TLV2770/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 0.8 μA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care needs to be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), the shutdown terminal needs to be pulled to $V_{DD}-$ (not GND) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 48, 49, and 50. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables. The *bump* on the rising edge of the TLV2770 output waveform is due to the start-up circuit on the bias generator. For the dual and quad (TLV2773/5), this *bump* is attributed to the bias generator's start-up circuit as well as the crosstalk between the other channel(s), which are in shutdown.

Figures 55 and 56 show the amplifier's forward and reverse isolation in shutdown. The operational amplifier is powered by ±1.35-V supplies and configured as a voltage follower ($A_V = 1$). The isolation performance is plotted across frequency for both 0.1 V_{PP} and 2.7 V_{PP} input signals. During normal operation, the amplifier would not be able to handle a 2.7-V_{PP} input signal with a supply voltage of ±1.35 V since it exceeds the common-mode input voltage range (V_{ICR}). However, this curve illustrates that the amplifier remains in shutdown even under a worst case scenario.

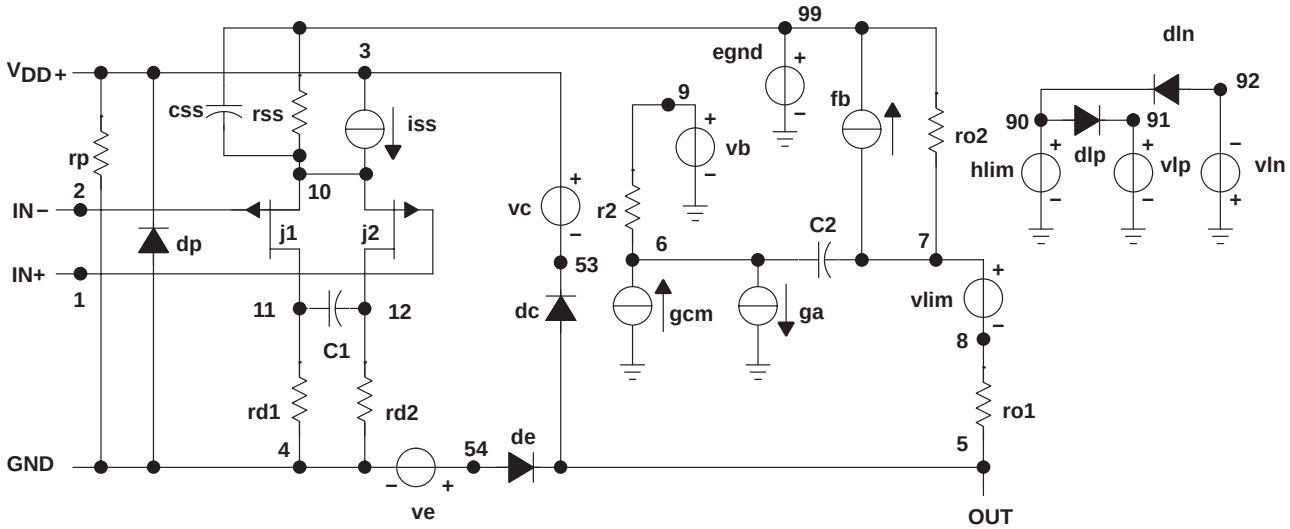
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 4) and subcircuit in Figure 64 are generated using the TLV2772 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
* TLV2772 operational amplifier macromodel subcircuit
* created using Parts release 8.0 on 12/12/97 at 10:08
* Parts is a MicroSim product.
*
* connections:   noninverting input
*                |   inverting input
*                |   |   positive power supply
*                |   |   |   negative power supply
*                |   |   |   |   output
*                |   |   |   |   |
.subckt TLV2772  1   2   3   4   5
*
c1      11   12   2.8868E-12
c2      6    7    10.000E−12
css     10   99   2.6302E−12
dc      5    53   dy
de      54   5    dy
dlp     90   91   dx
dln     92   90   dx
dp      4    3    dx
egnd    99   0    poly(2) (3,0) (4,0) 0 .5 .5
fb      7    99   poly(5) vb vc ve vlp vln 0
                  15.513E6 −1E3 1E3 16E6 −16E6
ga      6    0    11   12   188.50E−6
gcm     0    6    10   99   9.4472E−9
iss     3    10   dc       145.50E−6
hlim    90   0    vlim 1K
j1      11   2    10 jx1
j2      12   1    10 jx2
r2      6    9    100.00E3
rd1     4    11   5.3052E3
rd2     4    12   5.3052E3
ro1     8    5    17.140
ro2     7    99   17.140
rp      3    4    4.5455E3
rss     10   99   1.3746E6
vb      9    0    dc 0
vc      3    53   dc .82001
ve      54   4    dc .82001
vlim    7    8    dc 0
vlp     91   0    dc 47
vln     0    92   dc 47
.model  dx   D(Is=800.00E−18)
.model  dy   D(Is=800.00E−18 Rs=1m Cjo=10p)
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             + Vto=−.99765)
.model  jx2  PJF(Is=1.7500E−12 Beta=244.20E−6
             + Vto=−1.002350)
.ends
*$
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Figure 64. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9858802QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9858802QPA TLV2772AM	Samples
TLV2770AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2770AI	Samples
TLV2770AIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2770AI	Samples
TLV2770CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2770C	Samples
TLV2770CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2770C	Samples
TLV2770CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLV2770C	Samples
TLV2770IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ABP	Samples
TLV2770IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2770I	Samples
TLV2770IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2770I	Samples
TLV2771AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2771AI	Samples
TLV2771CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2771C	Samples
TLV2771CDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VAMC	Samples
TLV2771CDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VAMC	Samples
TLV2771CDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VAMC	Samples
TLV2771CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2771C	Samples
TLV2771ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2771I	Samples
TLV2771IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAMI	Samples
TLV2771IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAMI	Samples
TLV2771IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2771I	Samples
TLV2772AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772AI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2772AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772AI	Samples
TLV2772AIDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772AI	Samples
TLV2772AIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2772AI	Samples
TLV2772AMD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2772AM	Samples
TLV2772AMDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2772AM	Samples
TLV2772AMJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9858802QPA TLV2772AM	Samples
TLV2772AQPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772AQ	Samples
TLV2772CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2772C	Samples
TLV2772CDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AAF	Samples
TLV2772CDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AAF	Samples
TLV2772CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2772C	Samples
TLV2772CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLV2772C	Samples
TLV2772ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772I	Samples
TLV2772IDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AAG	Samples
TLV2772IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AAG	Samples
TLV2772IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772I	Samples
TLV2772IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2772IP	Samples
TLV2772MD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2772M	Samples
TLV2772QD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772Q	Samples
TLV2772QPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772Q	Samples
TLV2772QPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772Q	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2772QPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2772Q	Samples
TLV2773AIN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2773AI	Samples
TLV2773CDGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ABQ	Samples
TLV2773CDGSG4	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ABQ	Samples
TLV2773IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ABR	Samples
TLV2774AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2774A	Samples
TLV2774AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2774A	Samples
TLV2774AIN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2774A	Samples
TLV2774AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2774A	Samples
TLV2774CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2774C	Samples
TLV2774CDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2774C	Samples
TLV2774CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2774C	Samples
TLV2774CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLV2774C	Samples
TLV2774CPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2774C	Samples
TLV2774CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2774	Samples
TLV2774ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2774I	Samples
TLV2774IDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2774I	Samples
TLV2774IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2774I	Samples
TLV2774IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2774I	Samples
TLV2774IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2774	Samples
TLV2774IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2774	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2774IPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2774	Samples
TLV2775AIN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2775A	Samples
TLV2775AIPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2775AI	Samples
TLV2775CN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLV2775C	Samples
TLV2775ID	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2775I	Samples
TLV2775IDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2775I	Samples
TLV2775IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2775I	Samples
TLV2775IPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2775I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2771, TLV2772, TLV2772A, TLV2772AM, TLV2774, TLV2774A :

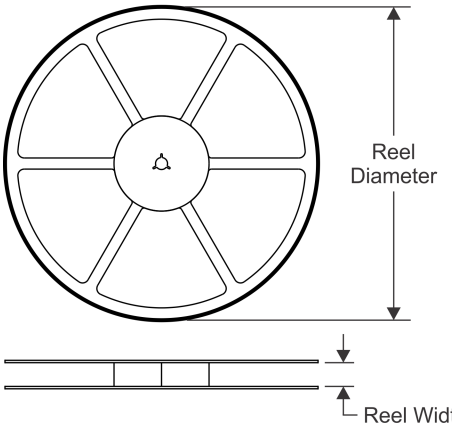
- Catalog : TLV2772A
- Automotive : TLV2771-Q1, TLV2772-Q1, TLV2772A-Q1, TLV2772A-Q1
- Enhanced Product : TLV2772A-EP, TLV2772A-EP, TLV2774-EP, TLV2774A-EP
- Military : TLV2772AM

NOTE: Qualified Version Definitions:

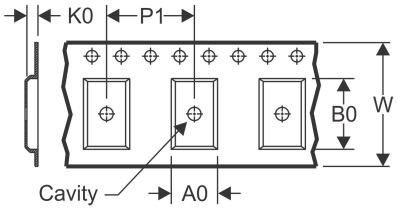
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

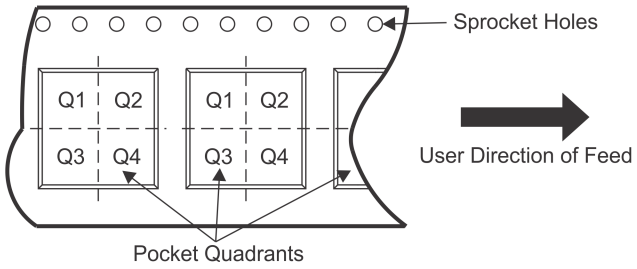


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

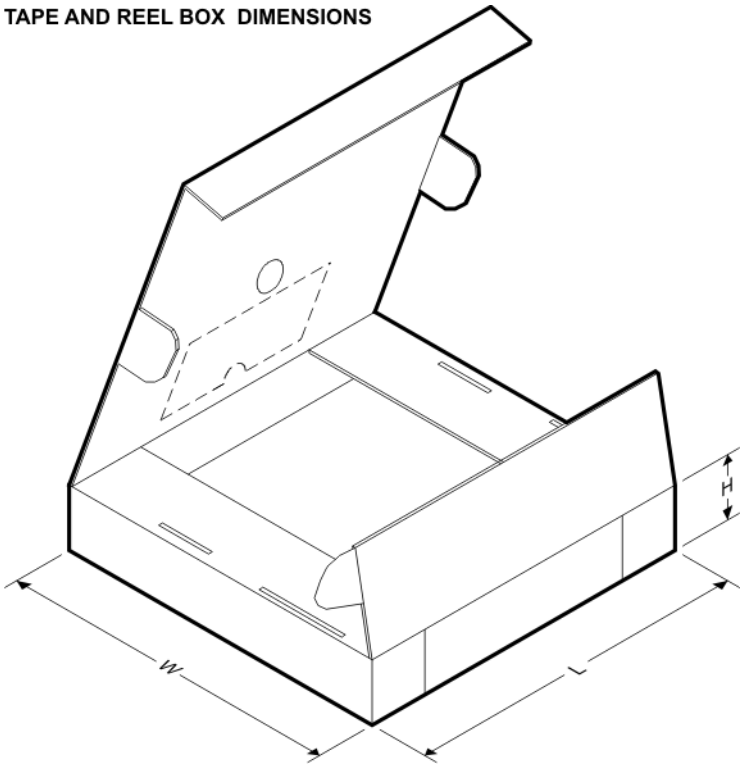


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2770CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2770IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2770IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2771AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2771CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV2771CDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV2771CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2771IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV2771IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV2771IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2772AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2772CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2772CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2772CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2772IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2772IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2772IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2772QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2772QPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2773IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2774AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2774CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2774CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2774IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2774IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2775IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLV2775IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

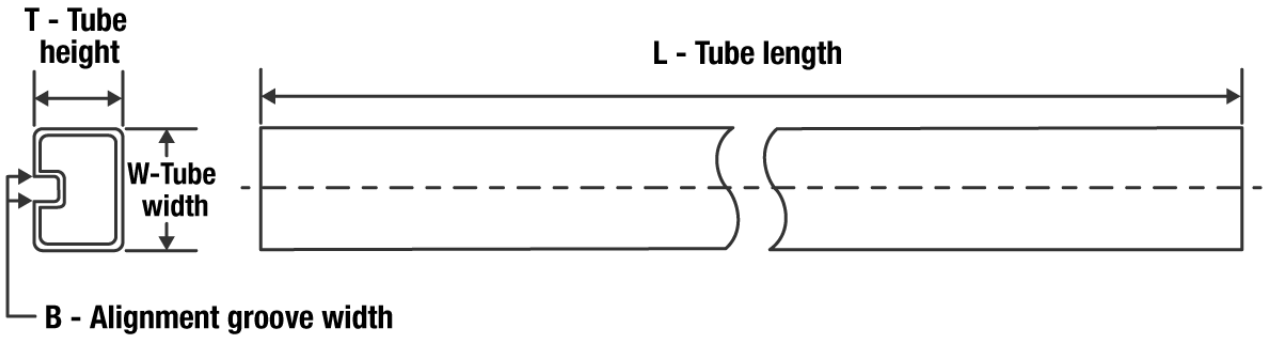


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2770CDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV2770IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2770IDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV2771AIDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV2771CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV2771CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV2771CDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV2771IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2771IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV2771IDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV2772AIDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV2772CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2772CDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV2772CDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV2772IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2772IDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV2772IDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV2772QPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TLV2772QPWRG4	TSSOP	PW	8	2000	853.0	449.0	35.0
TLV2773IDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TLV2774AIDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV2774CDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV2774CPWR	TSSOP	PW	14	2000	853.0	449.0	35.0
TLV2774IDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV2774IPWR	TSSOP	PW	14	2000	853.0	449.0	35.0
TLV2775IDR	SOIC	D	16	2500	350.0	350.0	43.0
TLV2775IPWR	TSSOP	PW	16	2000	853.0	449.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV2770AID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2770AID	D	SOIC	8	75	507	8	3940	4.32
TLV2770AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2770CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV2770CD	D	SOIC	8	75	507	8	3940	4.32
TLV2770CP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2770IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2771CD	D	SOIC	8	75	507	8	3940	4.32
TLV2771CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV2771ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2771ID	D	SOIC	8	75	507	8	3940	4.32
TLV2772AID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2772AID	D	SOIC	8	75	507	8	3940	4.32
TLV2772AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2772AMD	D	SOIC	8	75	505.46	6.76	3810	4
TLV2772AMDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLV2772AQPW	PW	TSSOP	8	150	530	10.2	3600	3.5
TLV2772CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV2772CD	D	SOIC	8	75	507	8	3940	4.32
TLV2772CDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
TLV2772CP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2772ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2772ID	D	SOIC	8	75	507	8	3940	4.32
TLV2772IDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
TLV2772IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2772MD	D	SOIC	8	75	505.46	6.76	3810	4
TLV2772QD	D	SOIC	8	75	507	8	3940	4.32
TLV2772QPW	PW	TSSOP	8	150	530	10.2	3600	3.5

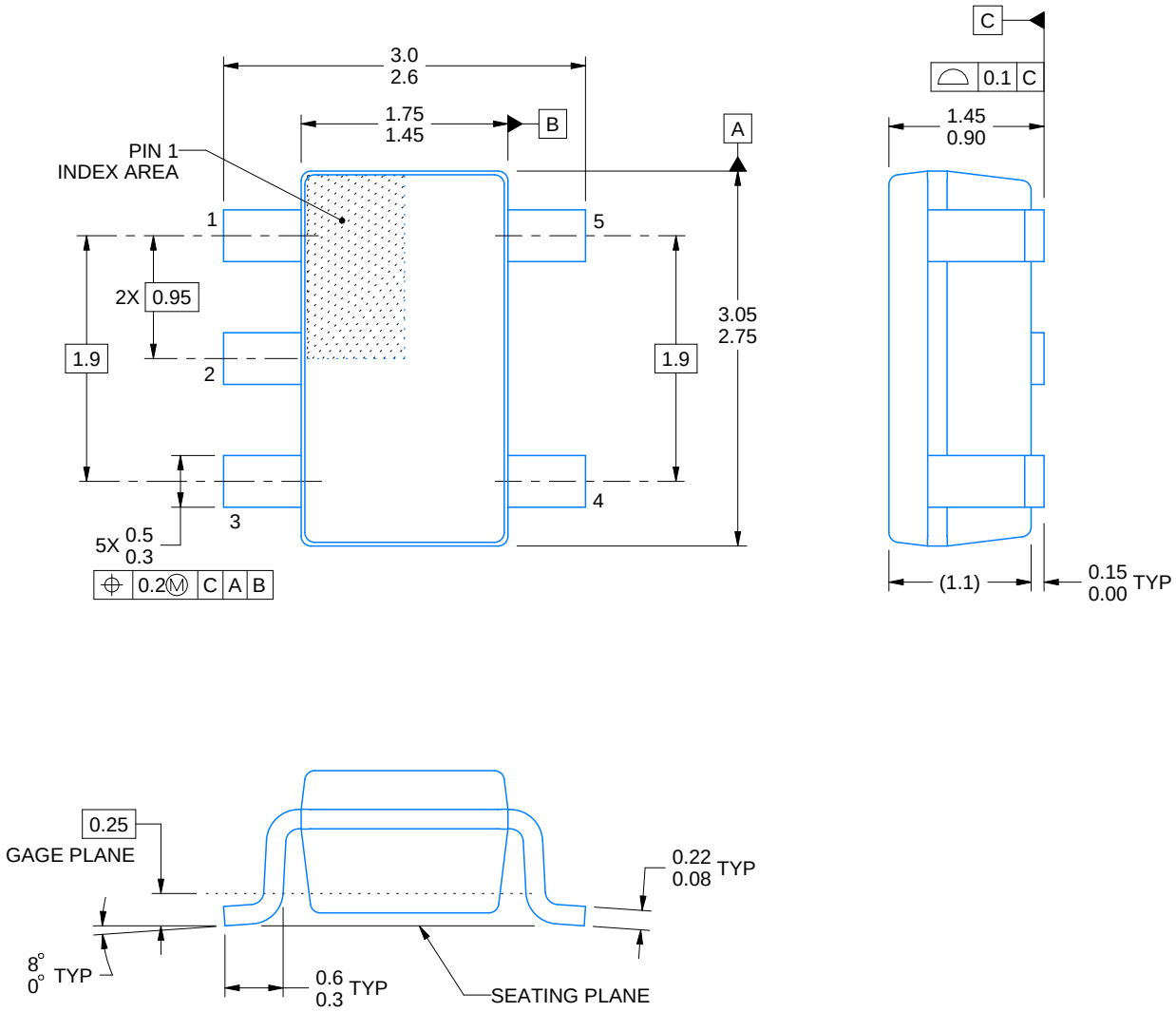
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV2773AIN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2774AID	D	SOIC	14	50	505.46	6.76	3810	4
TLV2774AIN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2774AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLV2774CD	D	SOIC	14	50	505.46	6.76	3810	4
TLV2774CDG4	D	SOIC	14	50	505.46	6.76	3810	4
TLV2774CN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2774CPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLV2774ID	D	SOIC	14	50	505.46	6.76	3810	4
TLV2774IDG4	D	SOIC	14	50	505.46	6.76	3810	4
TLV2774IN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2774IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLV2775AIN	N	PDIP	16	25	506	13.97	11230	4.32
TLV2775AIPW	PW	TSSOP	16	90	530	10.2	3600	3.5
TLV2775CN	N	PDIP	16	25	506	13.97	11230	4.32
TLV2775ID	D	SOIC	16	40	505.46	6.76	3810	4

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

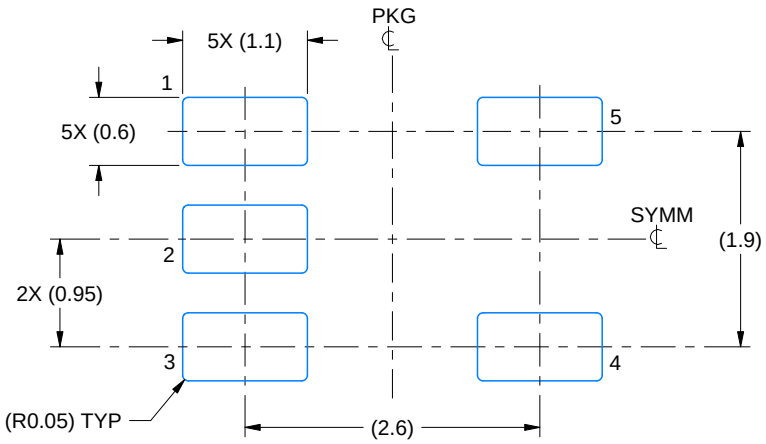
SMALL OUTLINE TRANSISTOR



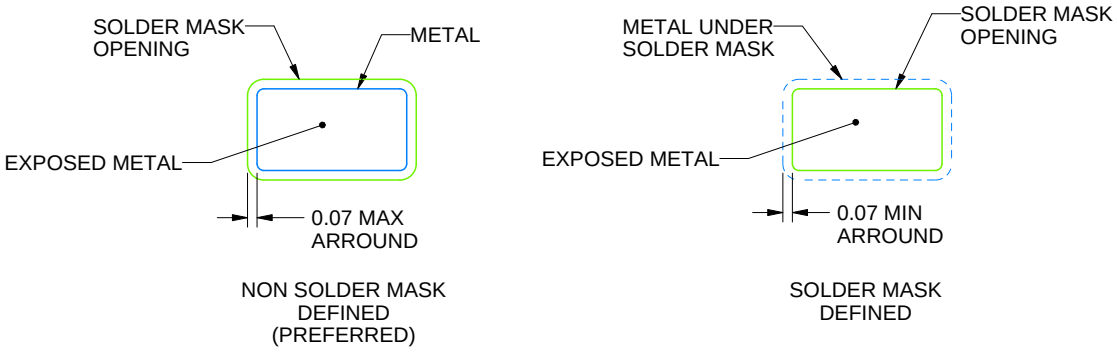
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

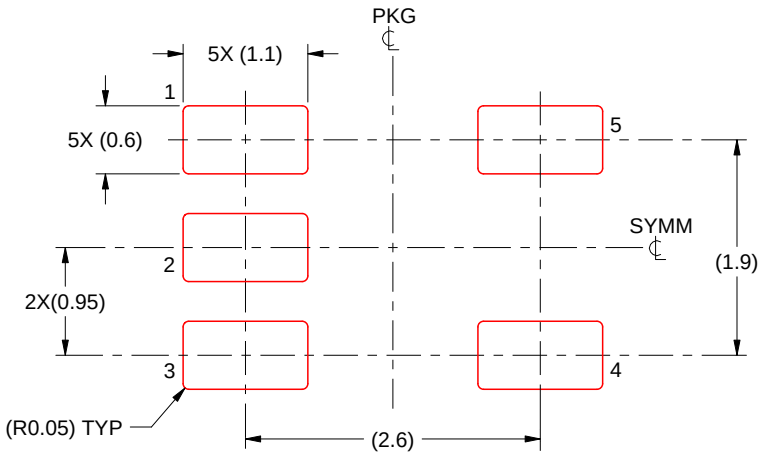


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



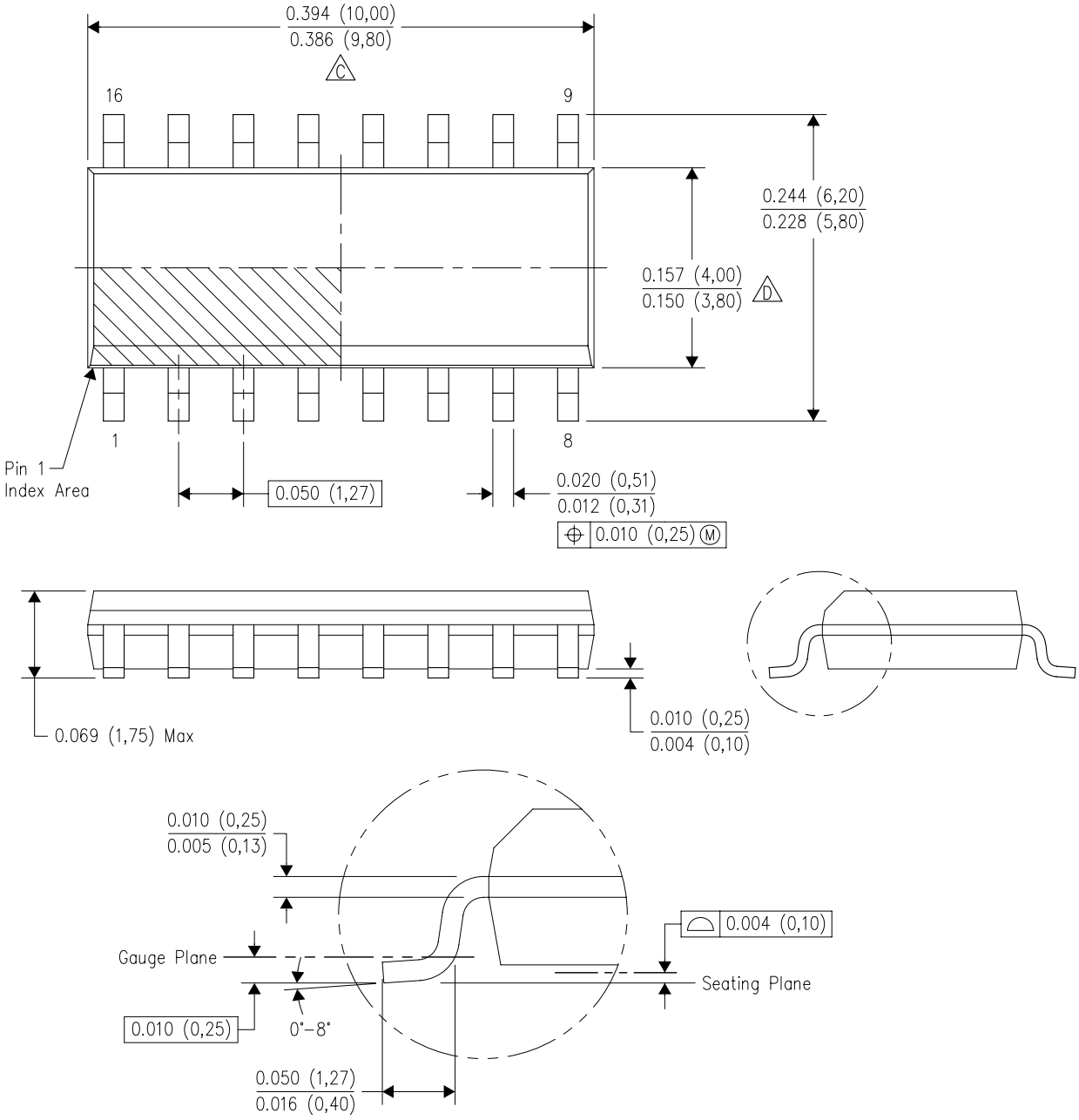
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

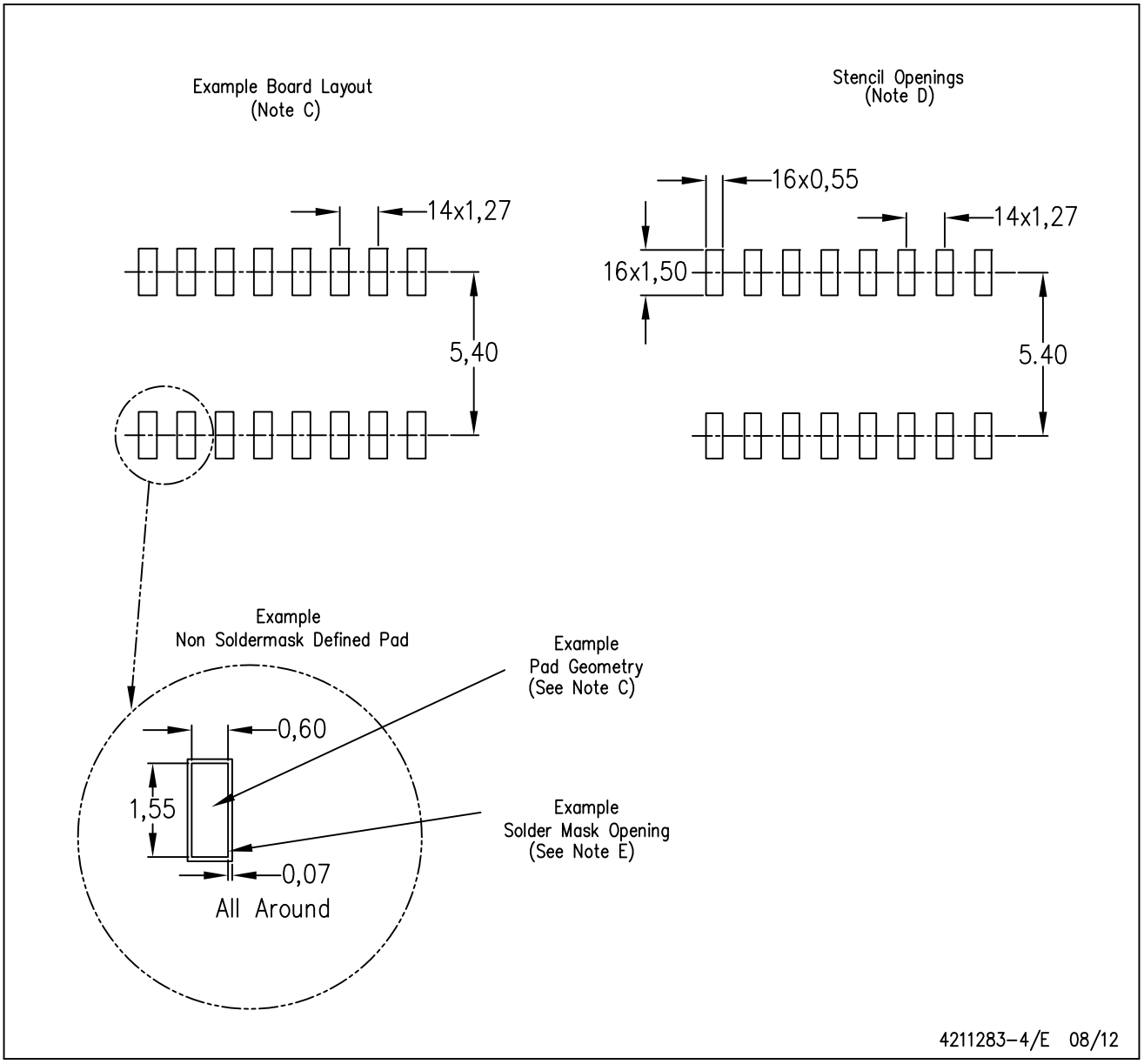
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



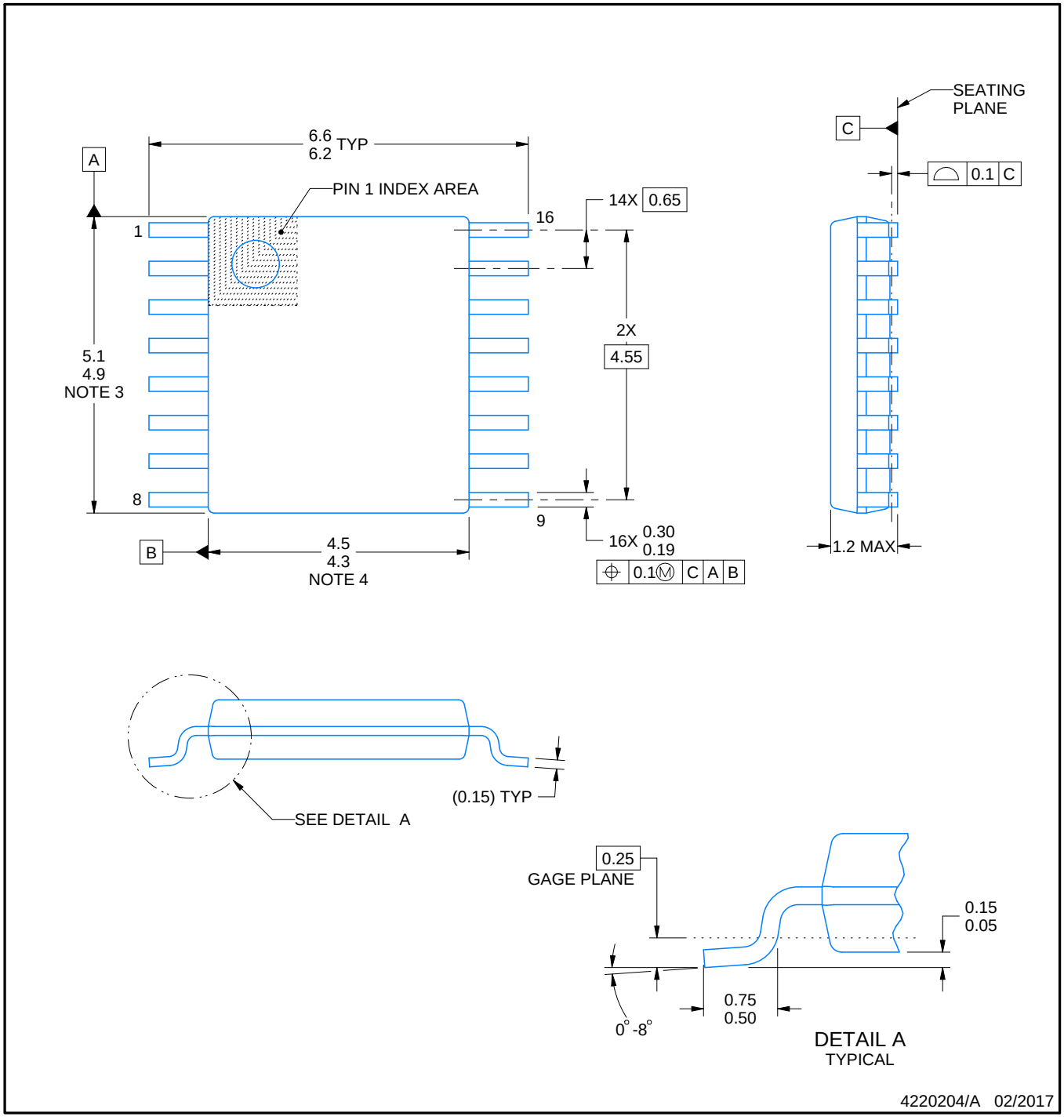
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

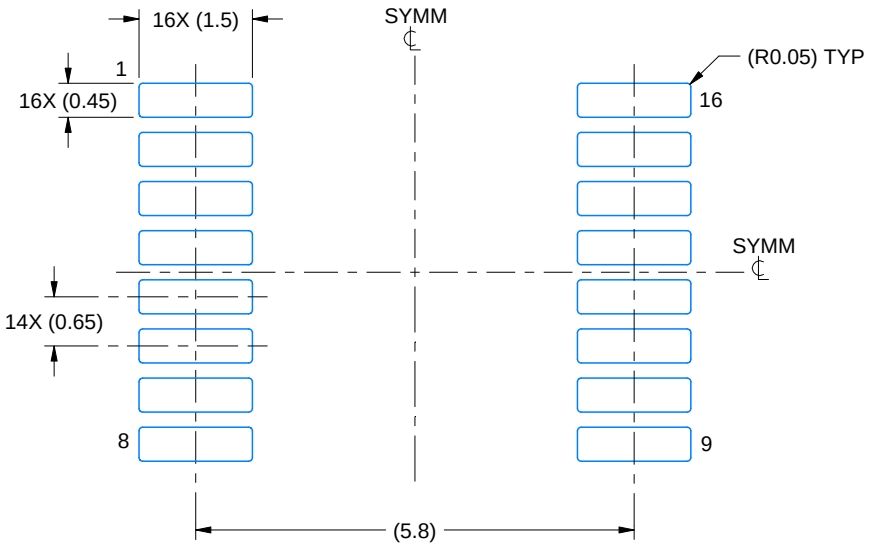
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

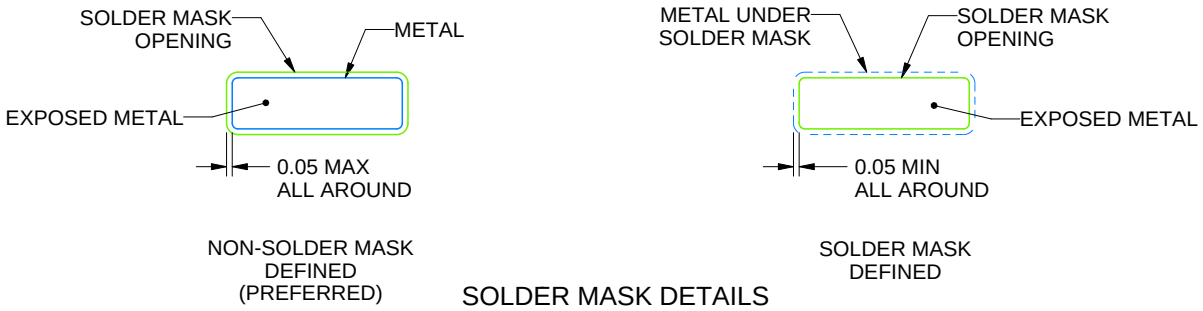


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

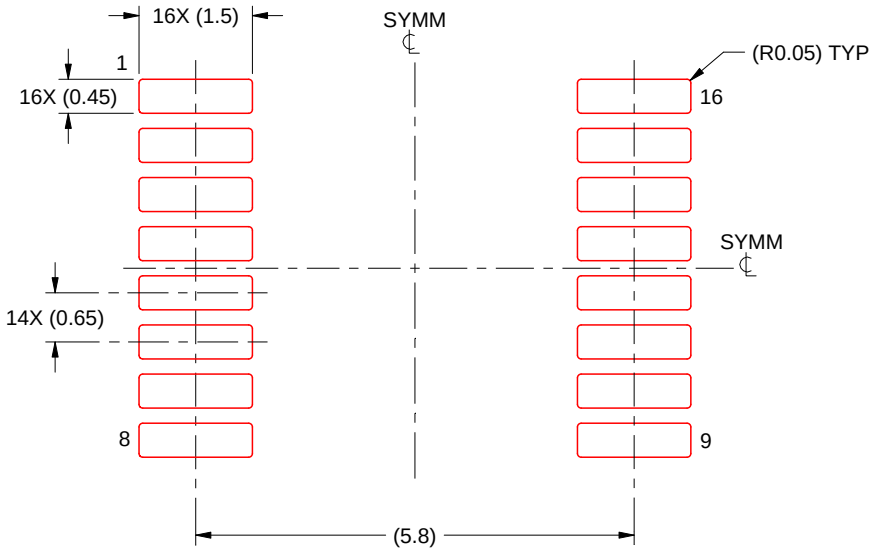


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

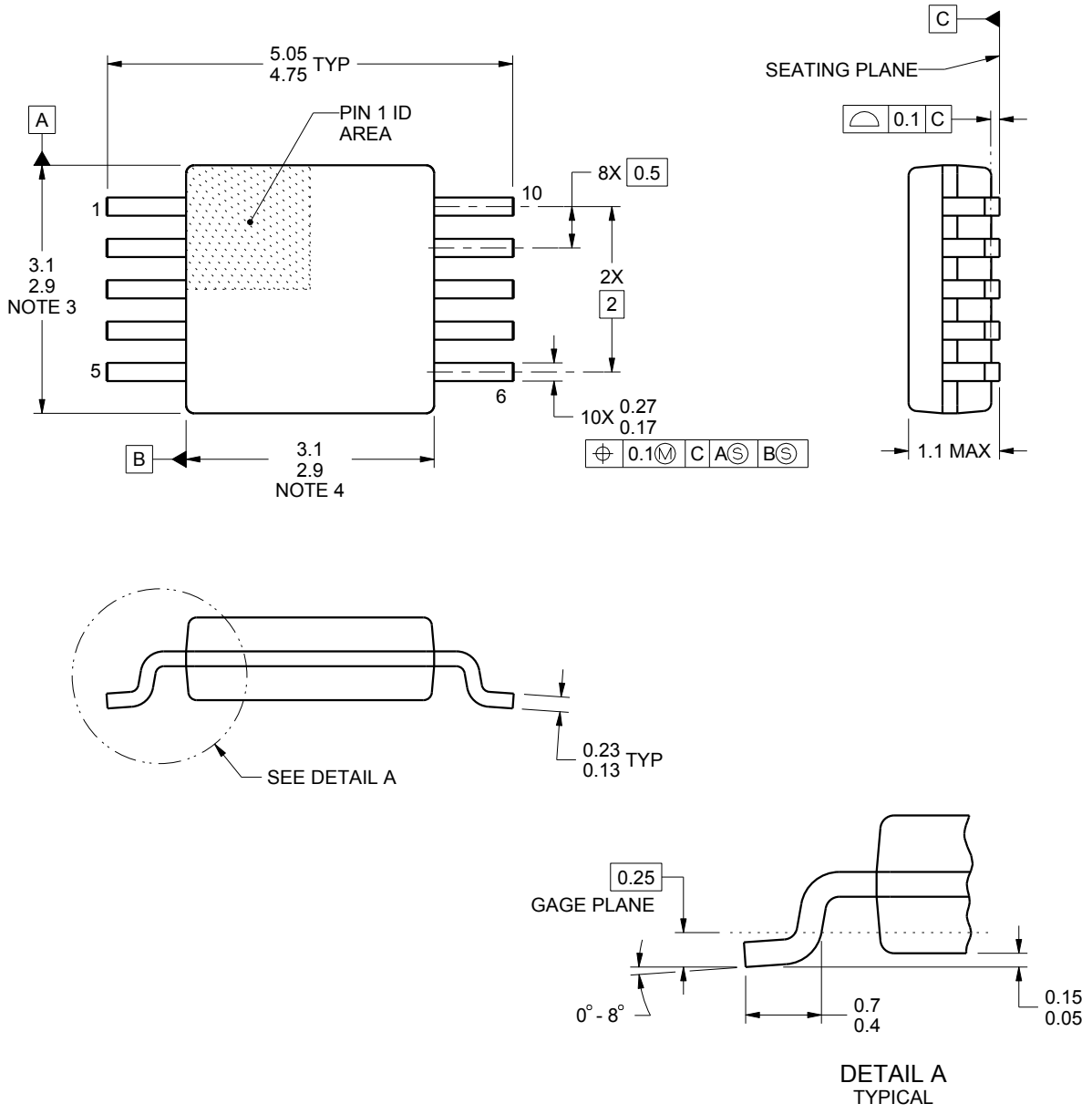
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0010A

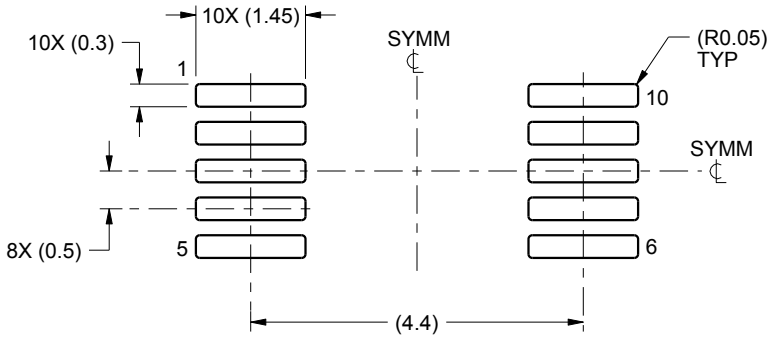
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

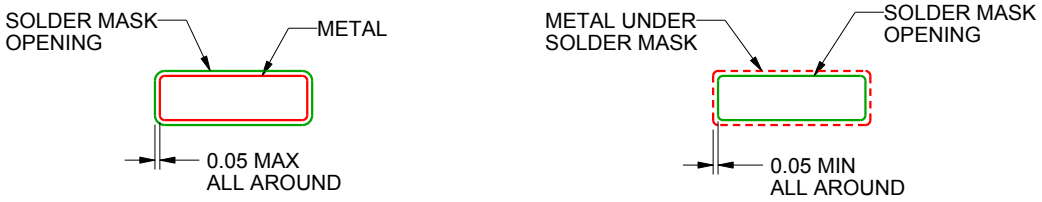


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

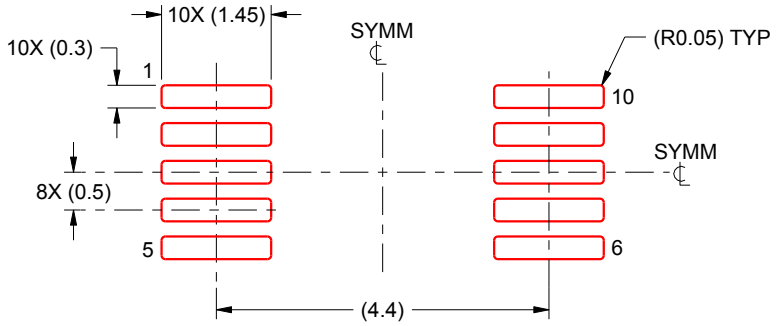


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



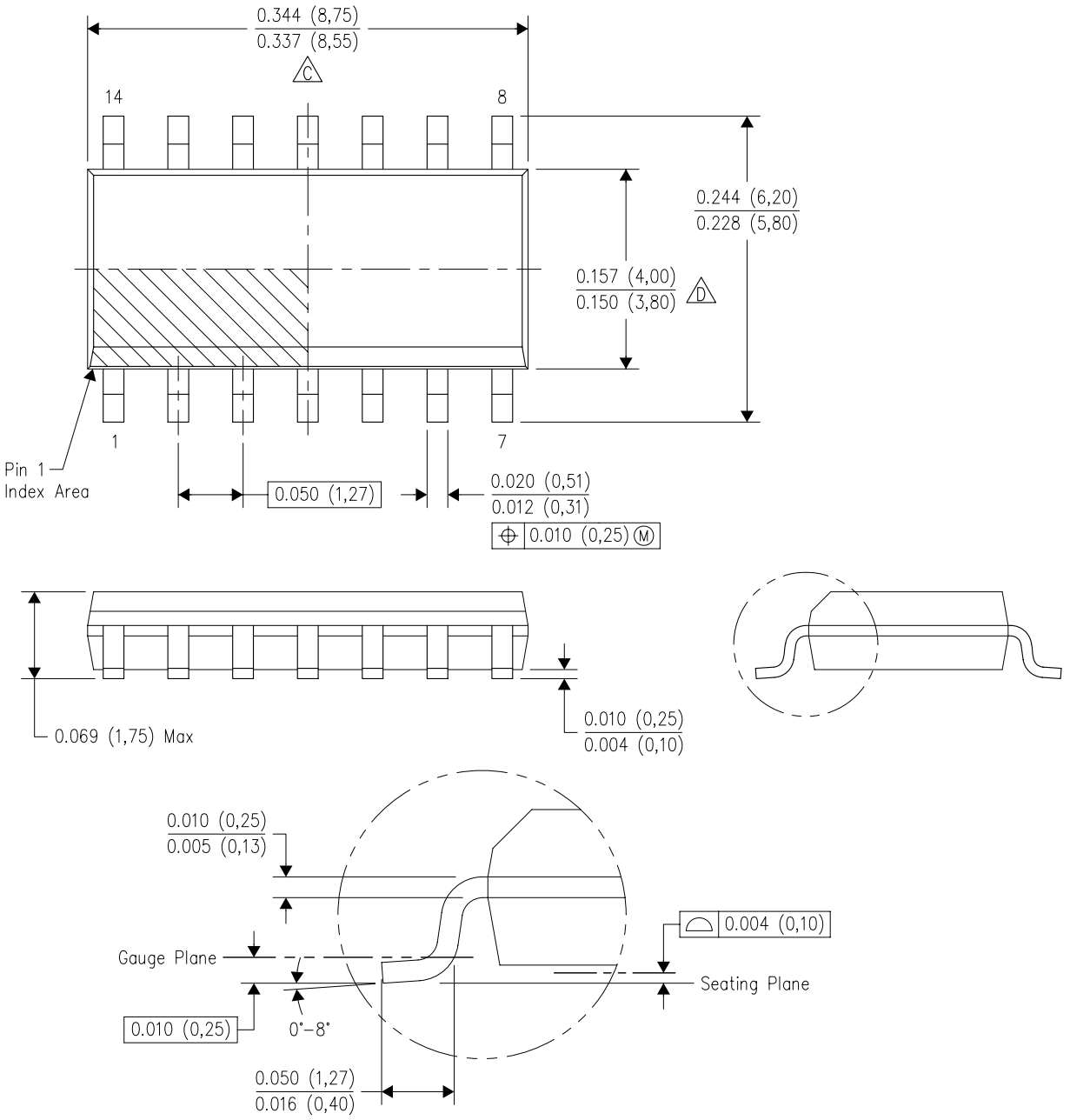
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

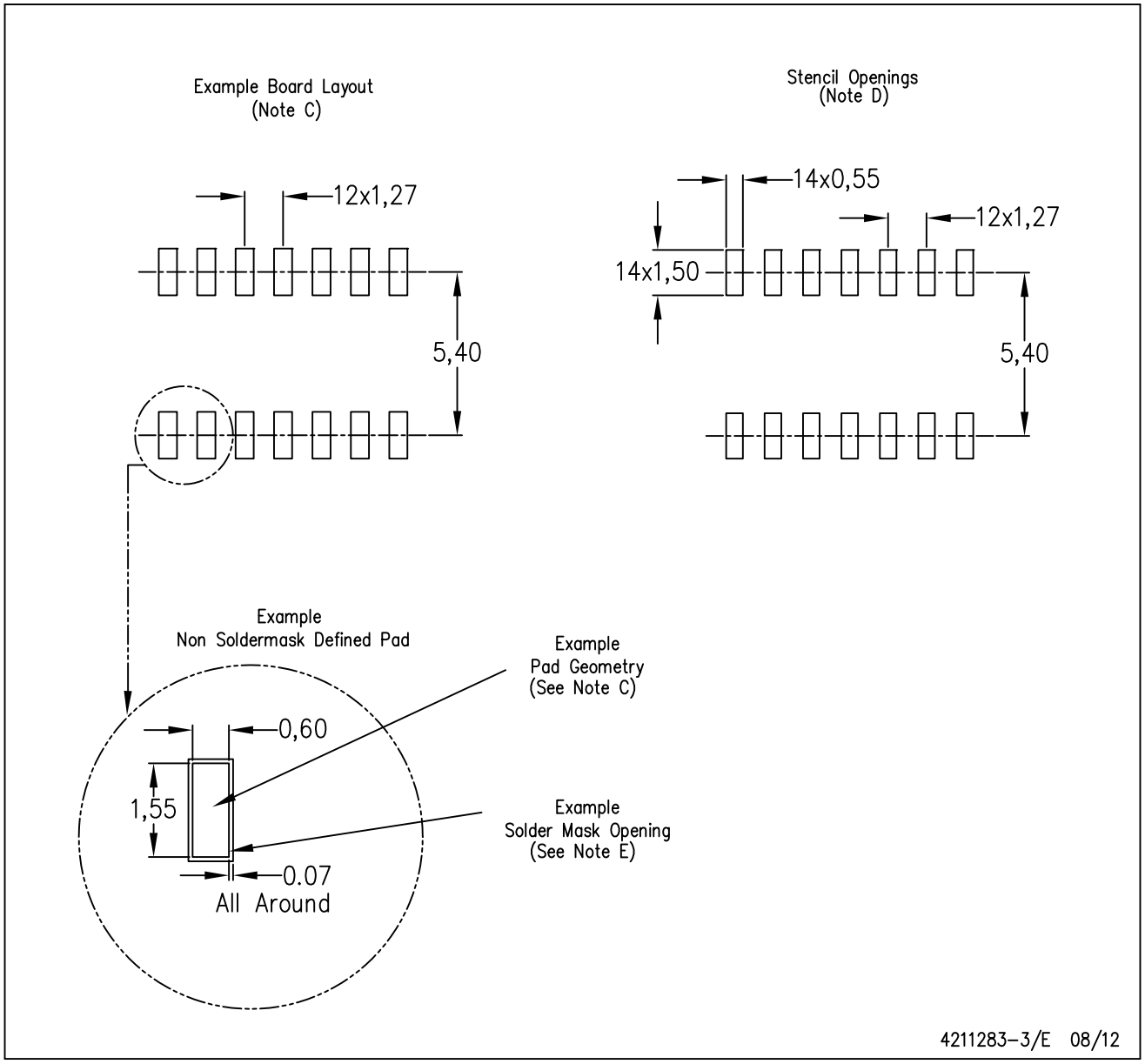
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

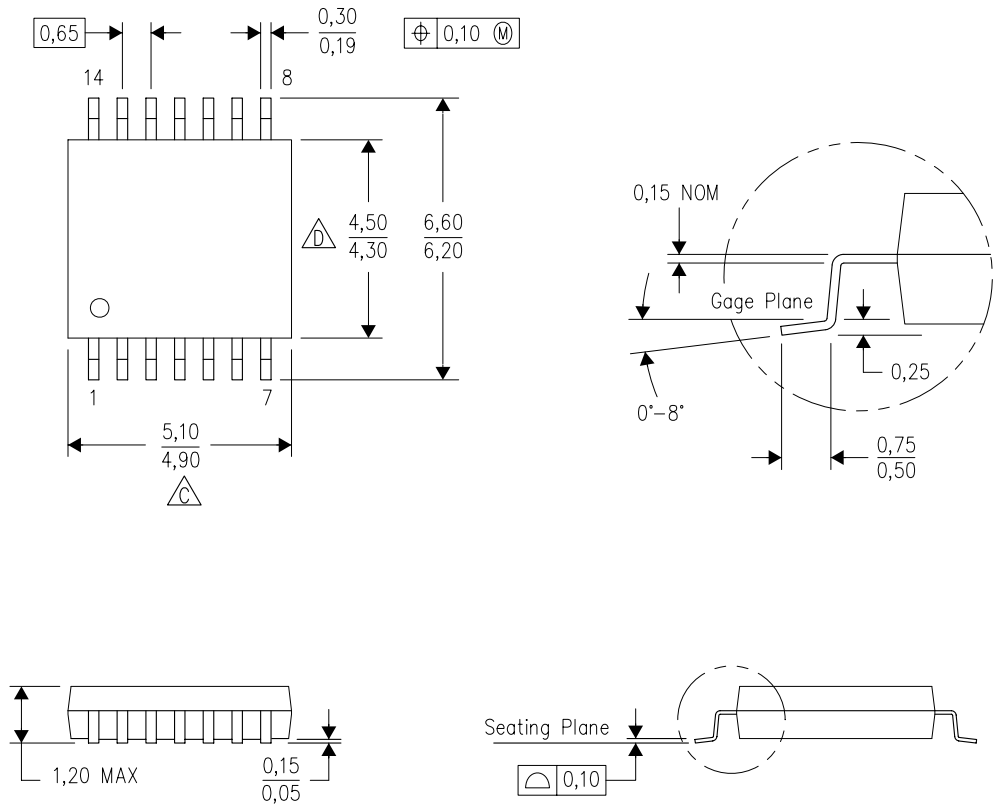
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

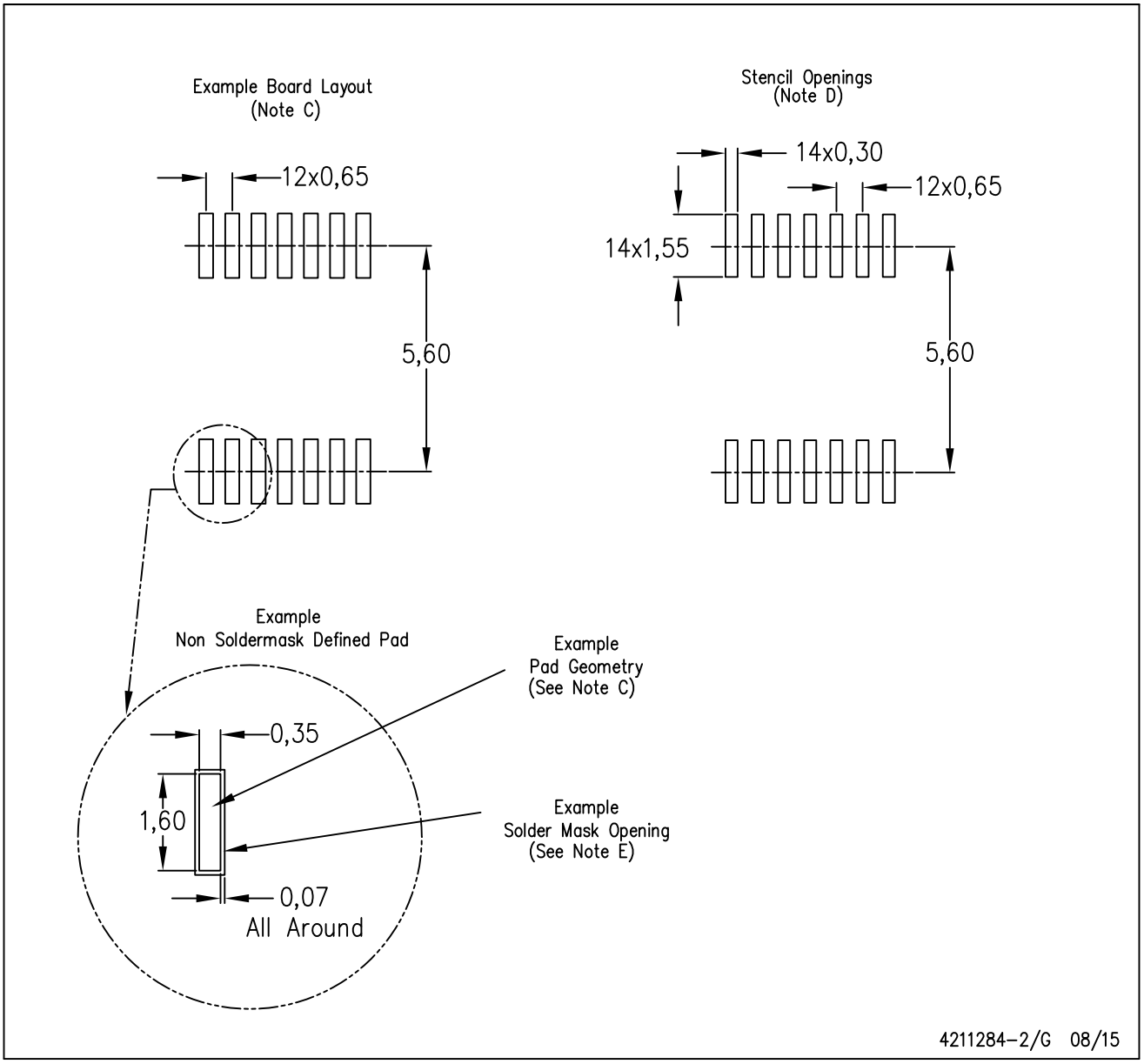
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



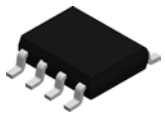
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

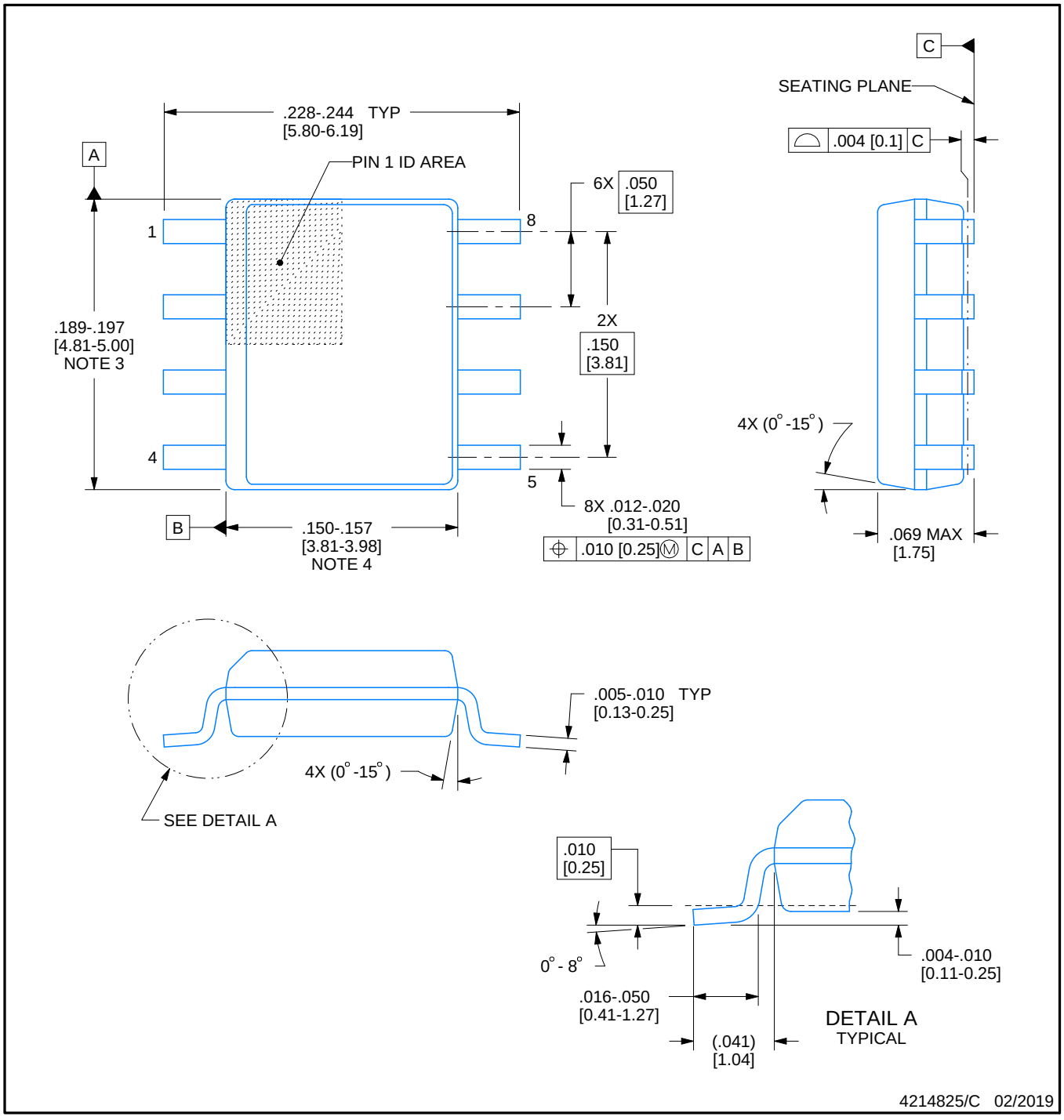


PACKAGE OUTLINE

D0008A

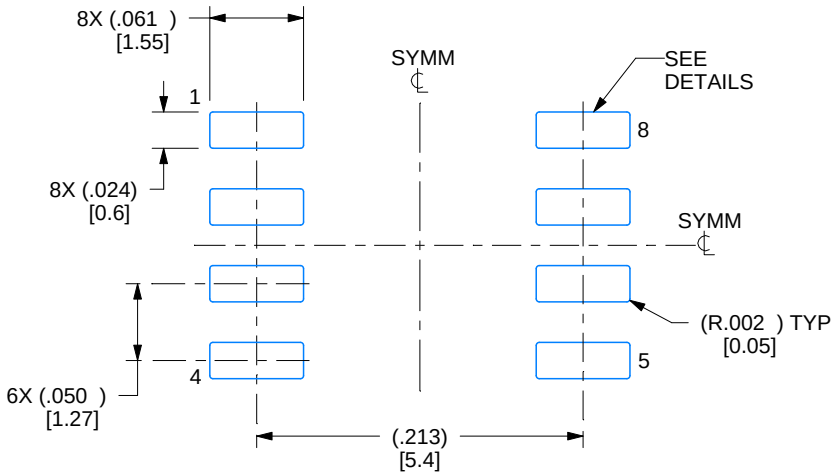
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

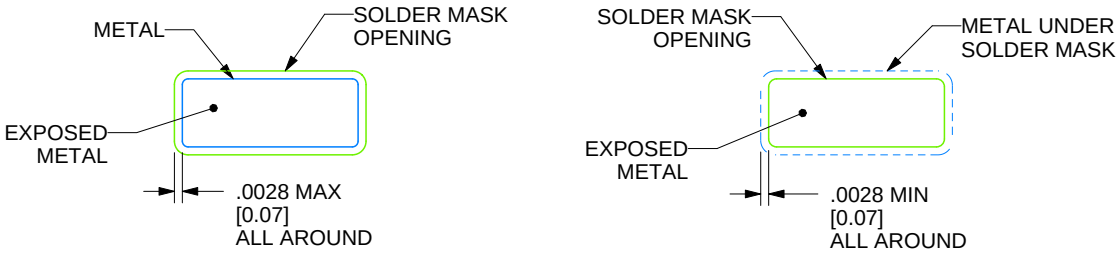


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

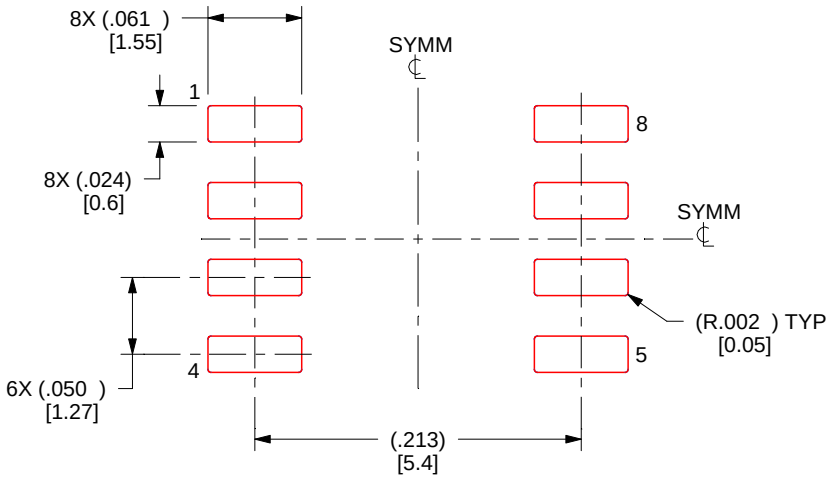
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

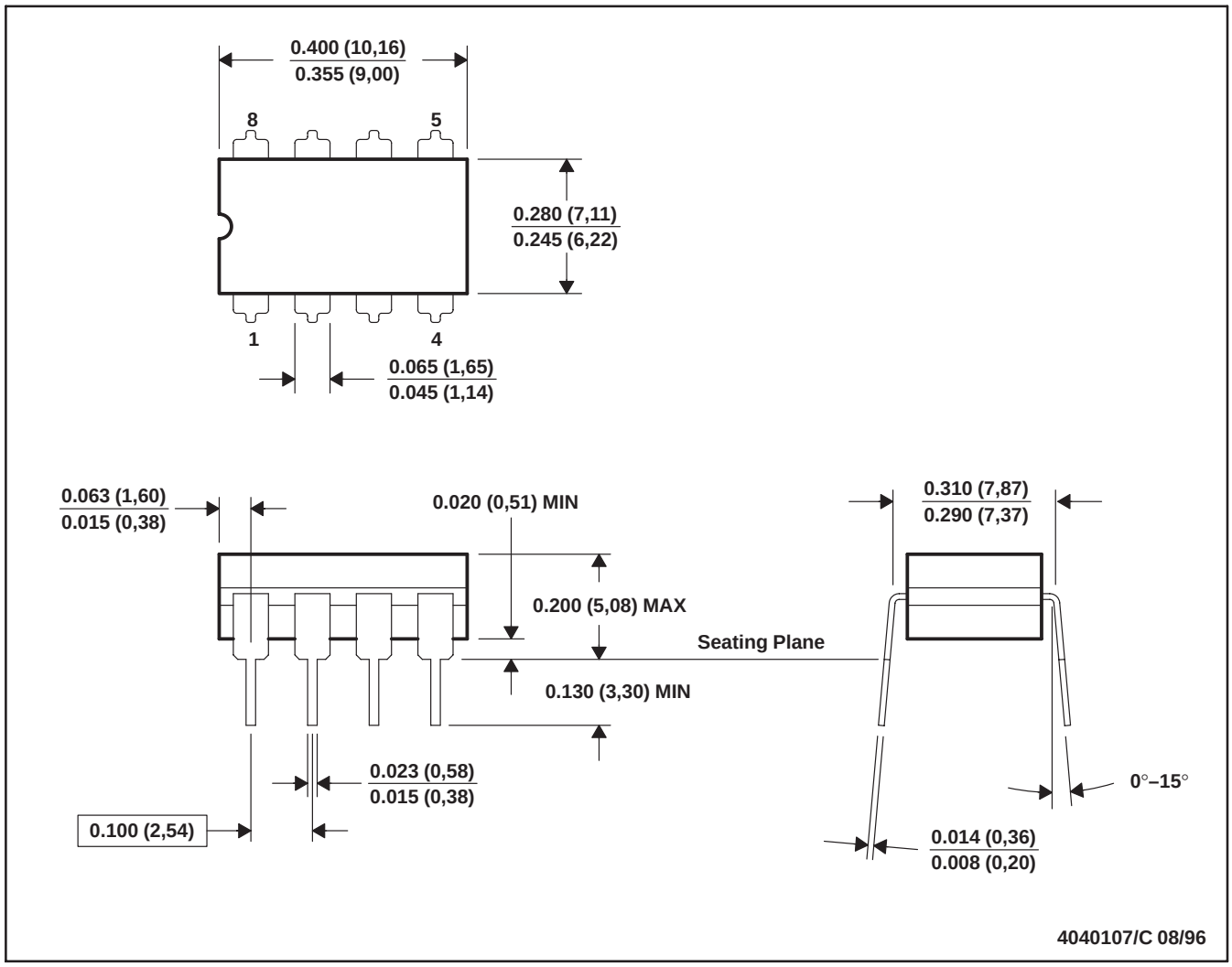
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

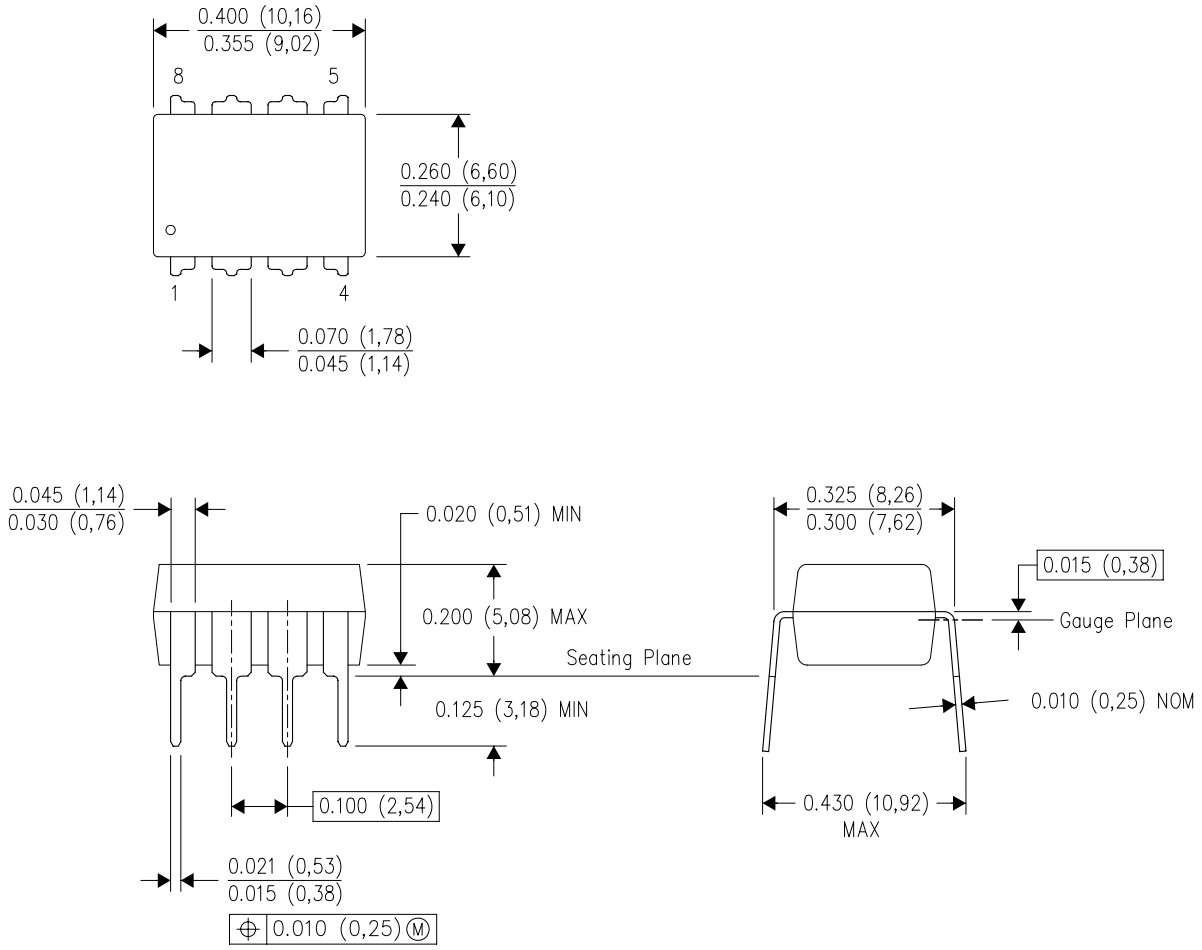
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

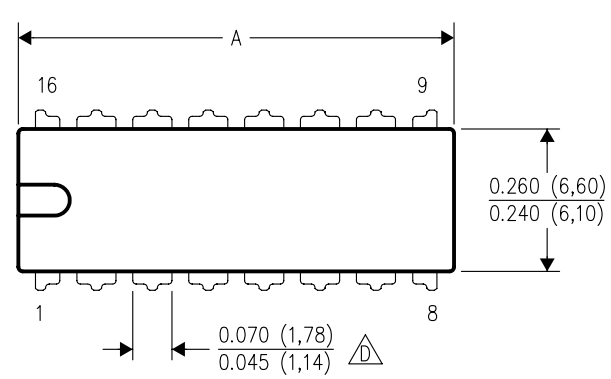


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

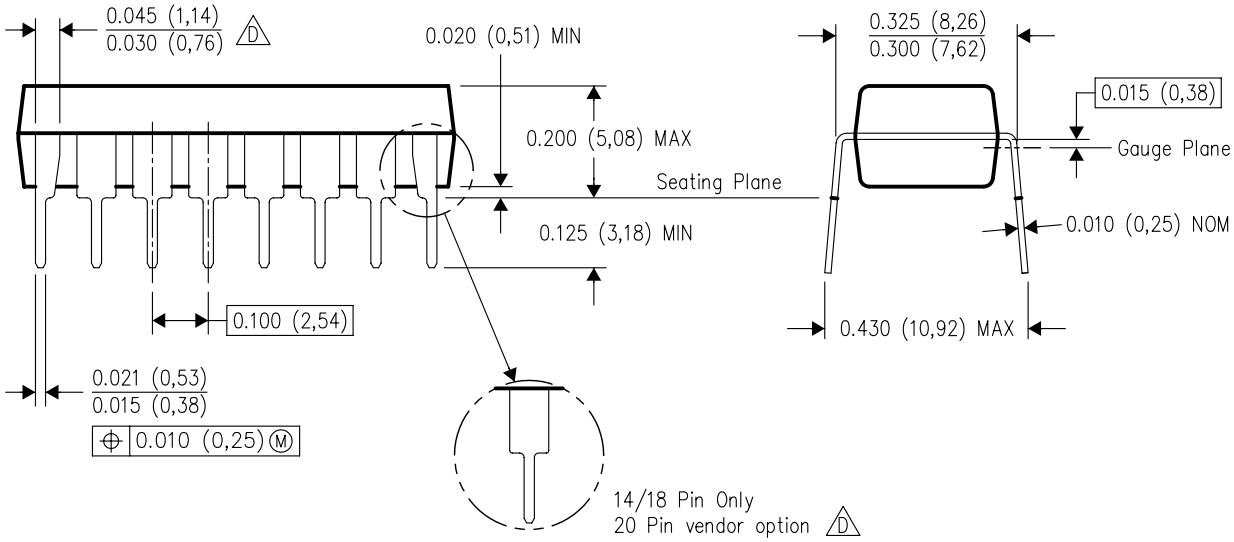
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



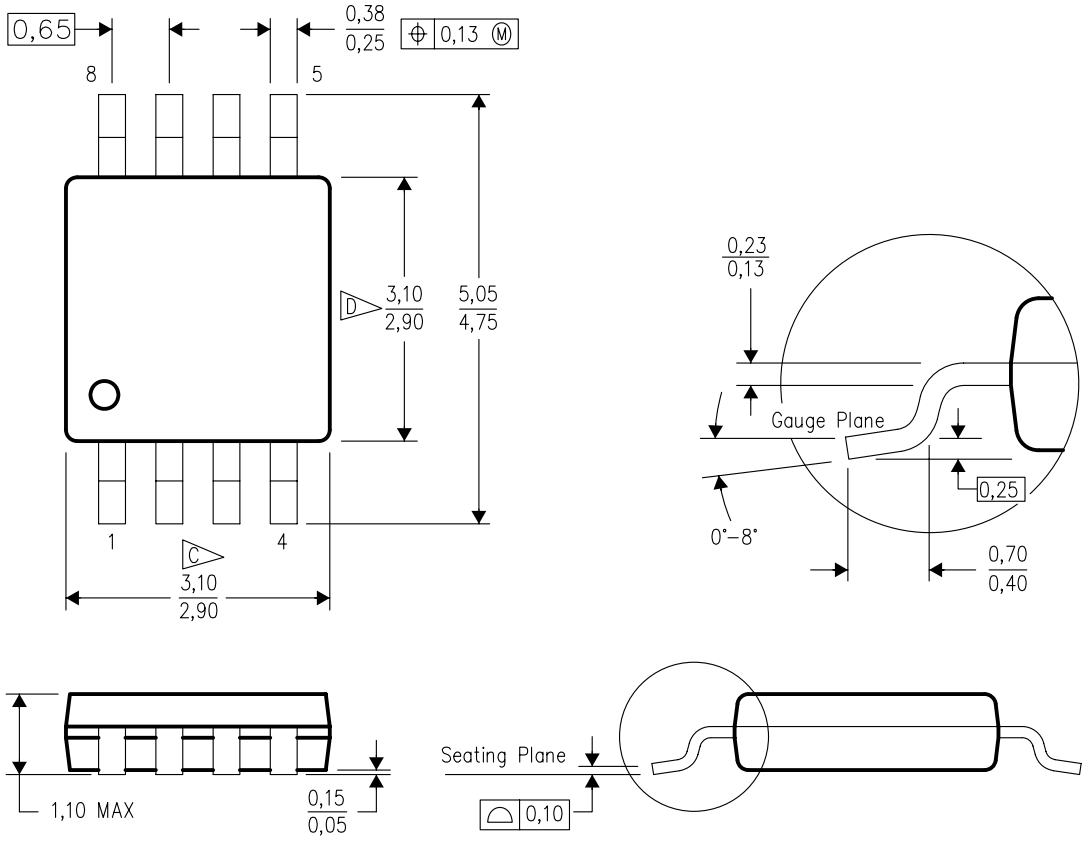
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

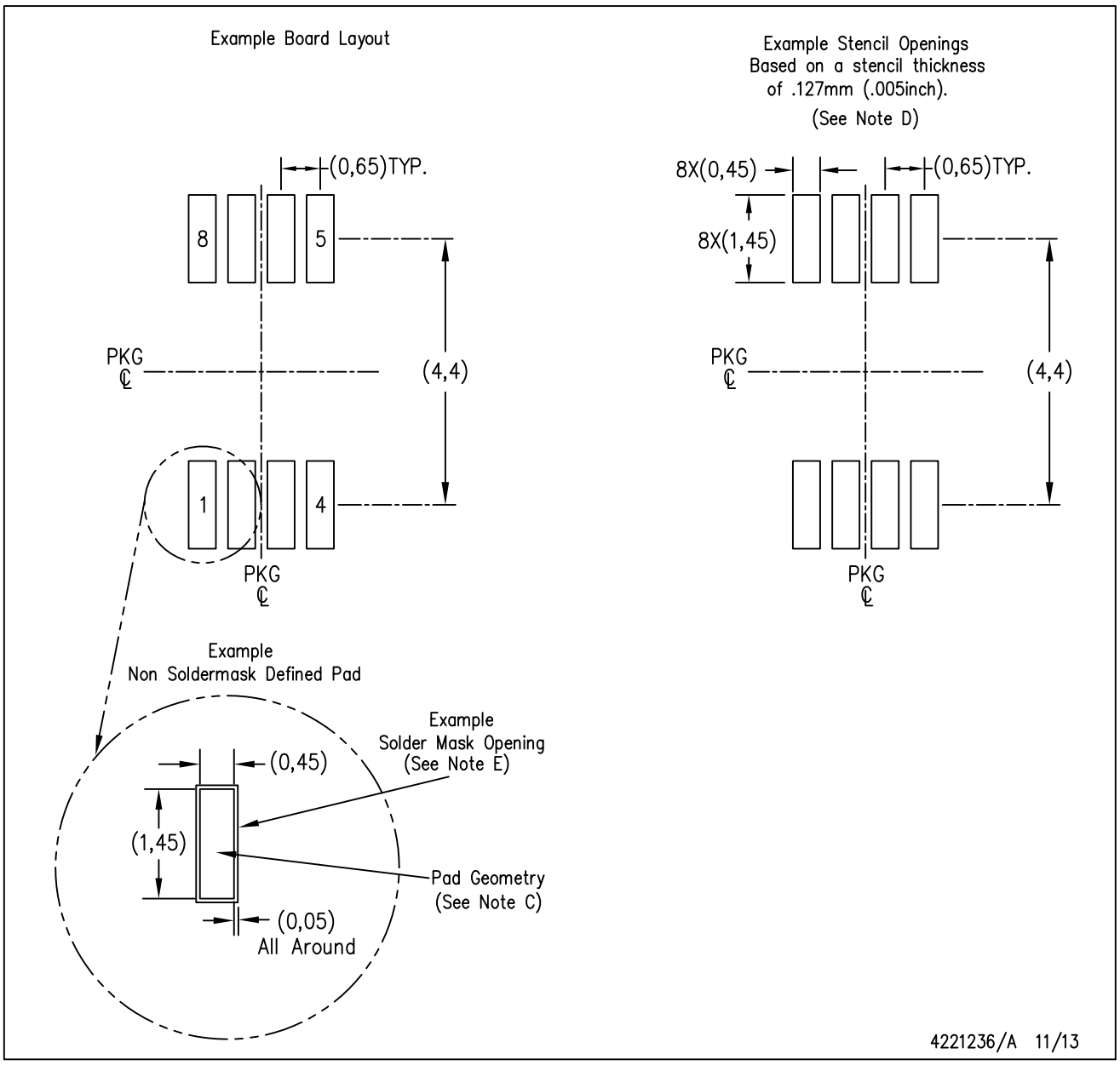
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



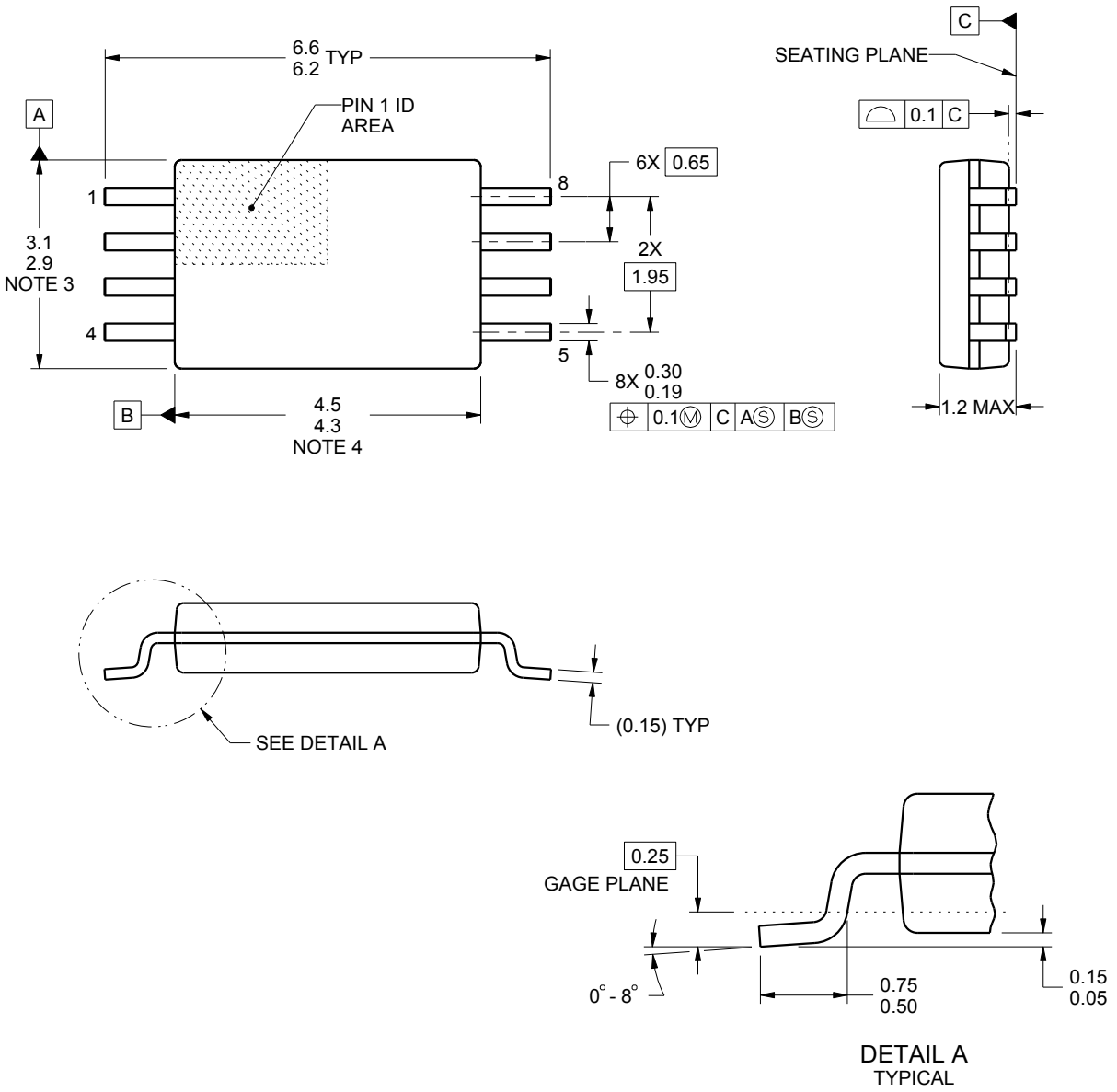
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

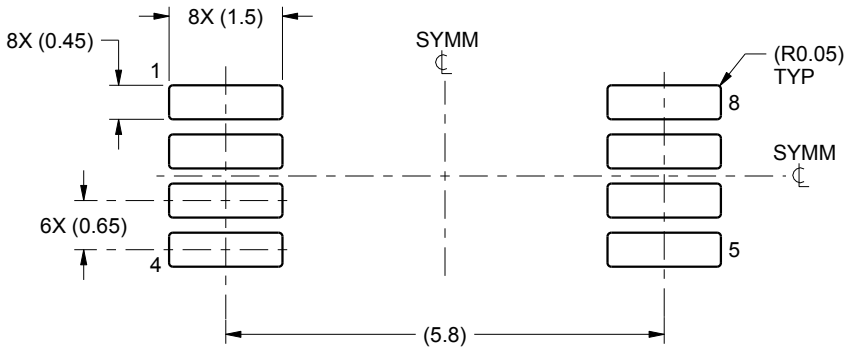
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

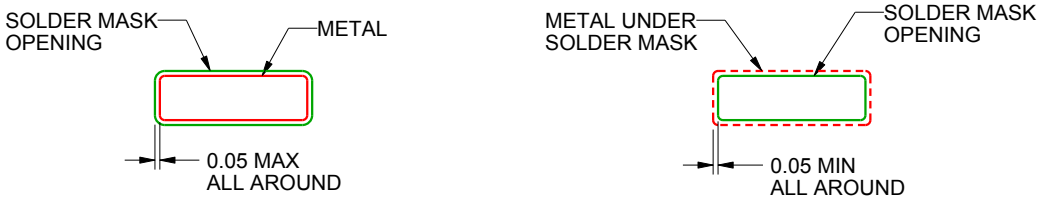


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

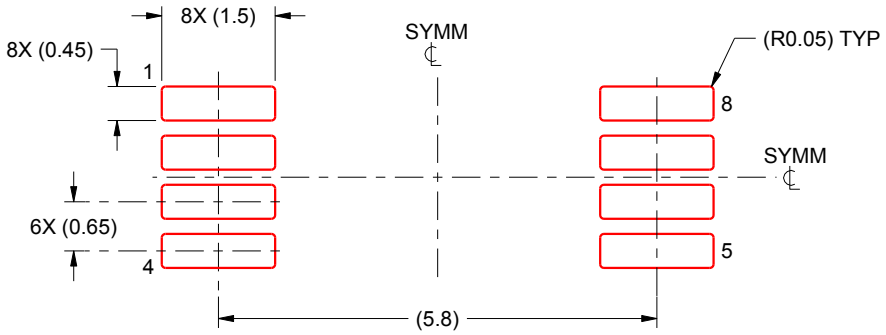


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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