SN74LVC126A Quadruple Bus Buffer Gate With 3-State Outputs

1 Features

- Operates From 1.65 V to 3.6 V
- Specified From –40°C to +125°C
- Inputs Accept Voltages up to 5.5 V
- Maximum t_{pd} of 4.7 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce), <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot), >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Applications

- AV Receivers
- Audio Docks: Portable
- Blu-ray Players and Home Theaters
- MP3 Players or Recorders
- Personal Digital Assistants (PDAs)
- Power: Telecom, Server, and AC-DC Supplies (Single-Controller, Analog, and Digital)
- Solid State Drives (SSDs): Client and Enterprise
- TVs: LCD, Digital, and High-Definition (HDTV)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

3 Description

The SN74LVC126A device is a quadruple bus buffer gate designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC126A device features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

To ensure the high-impedance state during power up or power down, OE must be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

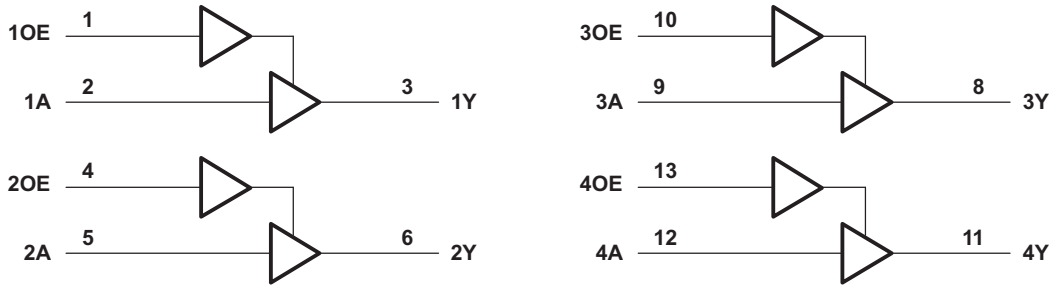
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V and 5-V system environment.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC126A-DR	SOIC (14)	8.65 mm × 3.91 mm
SN74LVC126A-DBR	SSOP (14)	6.20 mm × 5.30 mm
SN74LVC126A-DGVR	TVSOP (14)	3.60 mm × 4.40 mm
SN74LVC126A-NSR	SOP (14)	10.20 mm × 5.30 mm
SN74LVC126A-PWR	TSSOP (14)	5.00 mm × 4.40 mm
SN74LVC126A-RGYR	VQFN (14)	3.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision R (October 2016) to Revision S	Page
• Changed pin descriptions to match function in *Pin Functions* table	3

Changes from Revision Q (July 2005) to Revision R	Page
• Added *Applications* section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table; see POA at the end of the data sheet	1
• Changed temperature rating for VQFN package From: –40°C to 85°C To: –40°C to +125°C throughout the data sheet	1
• Changed values in the *Thermal Information* table: 86 to 98.4 for (D), 96 to 112.2 for (DB), 127 to 140.9 for (DGV), 76 to 93.9 for (NS), 113 to 127.7 for (PW), 47 to 35 for (RGY)	5

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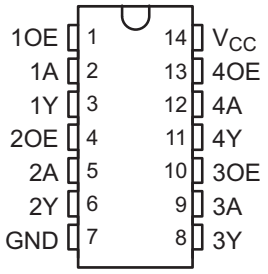
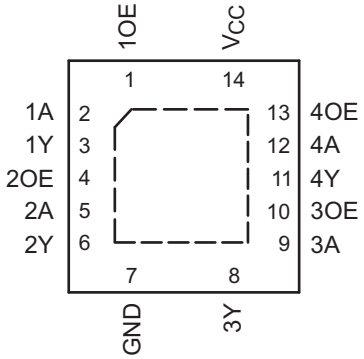
5 Pin Configuration and Functions

D, DB, DGV, NS, or PW Package
14-Pin SOIC, SSOP, TVSOP, SOP, or TSSOP
Top View



RGY Package
14-Pin VQFN With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1OE	I	Output enable 1
2	1A	I	Gate 1 input
3	1Y	O	Gate 1 output
4	2OE	I	Output enable 2
5	2A	I	Gate 2 input
6	2Y	O	Gate 2 output
7	GND	—	Ground pin
8	3Y	O	Gate 3 output
9	3A	I	Gate 3 input
10	3OE	I	Output enable 3
11	4Y	O	Gate 4 output
12	4A	I	Gate 4 input
13	4OE	I	Output Enable 4
14	V_{CC}	—	Power pin

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_{CC}		–0.5	6.5	V
Input voltage, V_I[2]		–0.5	6.5	V
Output voltage, V_O[2][3]		–0.5	V_{CC} + 0.5	V
Input clamp current, I_{IK}	$V_I < 0$		–50	mA
Output clamp current, I_{OK}	$V_O < 0$		–50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CC} or GND			±100	mA
Power dissipation, P_{tot}	T_A = –40°C to +125°C[4][5]		500	mW
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in *Recommended Operating Conditions*.
(4) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
(5) For the DB, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. This rating was tested on the D (SOIC) package.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. This rating was tested on the D (SOIC) package.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65		3.6	V
		Data retention only	1.5			
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}			V
		V_{CC} = 2.3 V to 2.7 V	1.7			
		V_{CC} = 2.7 V to 3.6 V	2			
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V			0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V			0.7	
		V_{CC} = 2.7 V to 3.6 V			0.8	
V_I	Input voltage		0		5.5	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V			–4	mA
		V_{CC} = 2.3 V			–8	
		V_{CC} = 2.7 V			–12	
		V_{CC} = 3 V			–24	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*.

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Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	NOM	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 1.65 V			4	mA
		V_{CC} = 2.3 V			8	
		V_{CC} = 2.7 V			12	
		V_{CC} = 3 V			24	
Δt/Δv	Input transition rise or fall rate				10	ns/V
T_A	Operating free-air temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN74LVC126A						UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	98.4[2]	112.2[2]	140.9[2]	93.9[2]	127.7[2]	35[3]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.2	64.2	59.9	51.7	56	43.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	59.6	70.2	52.7	69.5	11.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.1	28.3	9.1	20.7	8.9	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.4	59.1	69.5	52.3	68.9	11.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.
(3) The package ther mal impedance is calculated in accordance with JESD 51-5.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –100 µA, V_{CC} = 1.65 V to 3.6 V		T_A = 25°C	V_{CC} – 0.2			V
			T_A = –40°C to +125°C	V_{CC} – 0.3			
	I_{OH} = –4 mA, V_{CC} = 1.65 V		T_A = 25°C	1.29			
			T_A = –40°C to +85°C	1.2			
			T_A = –40°C to +125°C	1.05			
	I_{OH} = –8 mA, V_{CC} = 2.3 V		T_A = 25°C	1.9			
			T_A = –40°C to +85°C	1.7			
			T_A = –40°C to +125°C	1.55			
	I_{OH} = –12 mA	V_{CC} = 2.7 V	T_A = 25°C	2.2			
			T_A = –40°C to +125°C	2.05			
		V_{CC} = 3 V	T_A = 25°C	2.4			
			T_A = –40°C to +125°C	2.25			
	I_{OH} = –24 mA, V_{CC} = 3 V		T_A = 25°C	2.3			
			T_A = –40°C to +85°C	2.2			
			T_A = –40°C to +125°C	2			

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Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OL}	I_{OL} = 100 µA, V_{CC} = 1.65 V to 3.6 V		T_A = 25°C			0.1	V
			T_A = –40°C to +85°C			0.2	
			T_A = –40°C to +125°C			0.3	
	I_{OL} = 4 mA, V_{CC} = 1.65 V		T_A = 25°C			0.24	
			T_A = –40°C to +85°C			0.45	
			T_A = –40°C to +125°C			0.6	
	I_{OL} = 8 mA, V_{CC} = 2.3 V		T_A = 25°C			0.3	
			T_A = –40°C to +85°C			0.7	
			T_A = –40°C to +125°C			0.75	
	I_{OL} = 12 mA, V_{CC} = 2.7 V		T_A = 25°C			0.4	
			T_A = –40°C to +125°C			0.6	
	I_{OL} = 24 mA, V_{CC} = 3 V		T_A = 25°C			0.55	
			T_A = –40°C to +125°C			0.8	
I_I	V_I = 5.5 V or GND, V_{CC} = 3.6 V		T_A = 25°C			±1	µA
			T_A = –40°C to +85°C			±5	
			T_A = –40°C to +125°C			±20	
I_{OZ}	V_O = V_{CC} or GND, V_{CC} = 3.6 V		T_A = 25°C			±1	µA
			T_A = –40°C to +85°C			±10	
			T_A = –40°C to +125°C			±20	
I_{CC}	V_I = V_{CC} or GND, I_O = 0, V_{CC} = 3.6 V		T_A = 25°C			1	µA
			T_A = –40°C to +85°C			10	
			T_A = –40°C to +125°C			40	
ΔI_{CC}	One input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND, V_{CC} = 2.7 V to 3.6 V		T_A = 25°C			500	µA
			T_A = –40°C to +125°C			5000	
C_i	V_I = V_{CC} or GND, V_{CC} = 3.3 V				4.5		pF
C_o	V_O = V_{CC} or GND, V_{CC} = 3.3 V				7		pF
C_{pd} Power dissipation capacitance per gate	f = 10 MHz, T_A = 25°C	Outputs enabled	V_{CC} = 1.8 V		20		pF
			V_{CC} = 2.5 V		21		
			V_{CC} = 3.3 V		22		
		Outputs disabled	V_{CC} = 1.8 V		2		
			V_{CC} = 2.5 V		3		
			V_{CC} = 3.3 V		4		

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6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted; see *Parameter Measurement Information*)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{pd}	From A (input) to Y (output)	V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	1	4.2	9.3	ns
			T_A = –40°C to +85°C			9.8	
			T_A = –40°C to +125°C			11.3	
		V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	1	2.7	6.7	
			T_A = –40°C to +85°C			7.2	
			T_A = –40°C to +125°C			9.3	
		V_{CC} = 2.7 V	T_A = 25°C	1	2.9	5	
			T_A = –40°C to +85°C			5.2	
			T_A = –40°C to +125°C			6.5	
		V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	1	2.5	4.5	
			T_A = –40°C to +85°C			4.7	
			T_A = –40°C to +125°C			6	
t_{en}	From OE (input) to Y (output)	V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	1	4.8	9.5	ns
			T_A = –40°C to +85°C			10	
			T_A = –40°C to +125°C			11.5	
		V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	1	2.8	7.8	
			T_A = –40°C to +85°C			8.3	
			T_A = –40°C to +125°C			10.4	
		V_{CC} = 2.7 V	T_A = 25°C	1	3.1	6.1	
			T_A = –40°C to +85°C			6.3	
			T_A = –40°C to +125°C			8	
		V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	1	2.5	5.5	
			T_A = –40°C to +85°C			5.7	
			T_A = –40°C to +125°C			7.5	

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Switching Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted; see *Parameter Measurement Information*)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{dis}	From OE (input) to Y (output)	V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	1	4.4	12.1	ns
			T_A = –40°C to +85°C			12.6	
			T_A = –40°C to +125°C			14.1	
		V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	1	2.7	8.2	
			T_A = –40°C to +85°C			8.7	
			T_A = –40°C to +125°C			10.8	
		V_{CC} = 2.7 V	T_A = 25°C	1	2.7	6.5	
			T_A = –40°C to +85°C			6.7	
			T_A = –40°C to +125°C			8.5	
		V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	1.3	2.3	5.8	
			T_A = –40°C to +85°C			6	
			T_A = –40°C to +125°C			7.5	
$t_{sk(o)}$	V_{CC} = 3.3 V ± 0.3 V		T_A = –40°C to +85°C			1	ns
			T_A = –40°C to +125°C			1.5	

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6.7 Typical Characteristics

T_A = 25°C

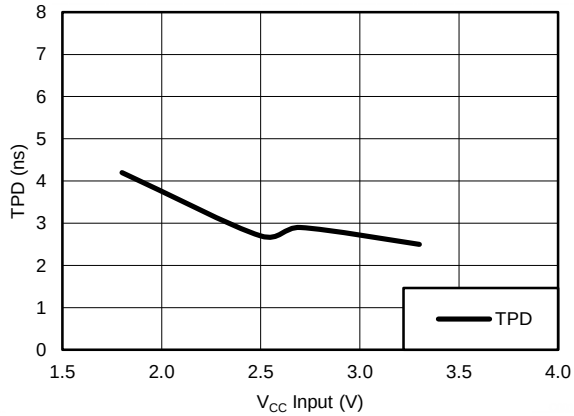

Figure 1. TPD vs V_{CC}

7 Parameter Measurement Information

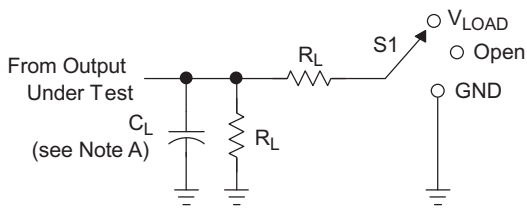

Figure 2. Load Circuit

Table 1. Timing Test Conditions

TEST	S1
t_{PLH} and t_{PHL}	Open
t_{PLZ} and t_{PZL}	V_{LOAD}
t_{PHZ} and t_{PZH}	GND

Table 2. Electrical Characteristics Test Conditions

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V

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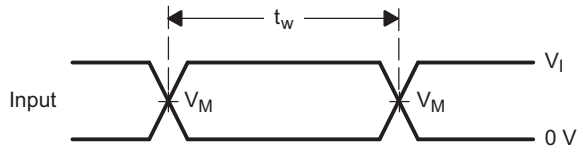


Figure 3. Voltage Waveforms, Pulse Duration

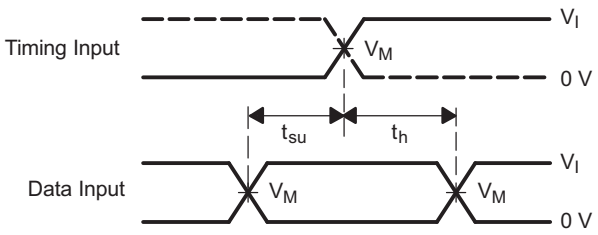


Figure 4. Voltage Waveforms, Setup and Hold Times

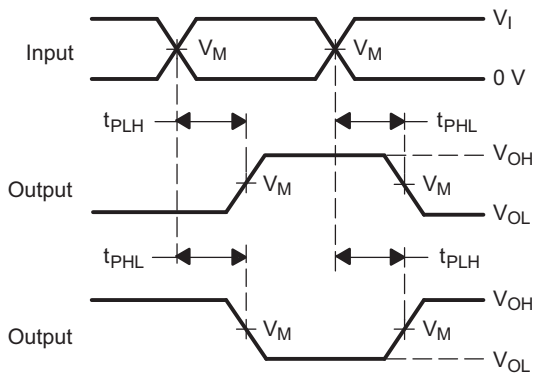
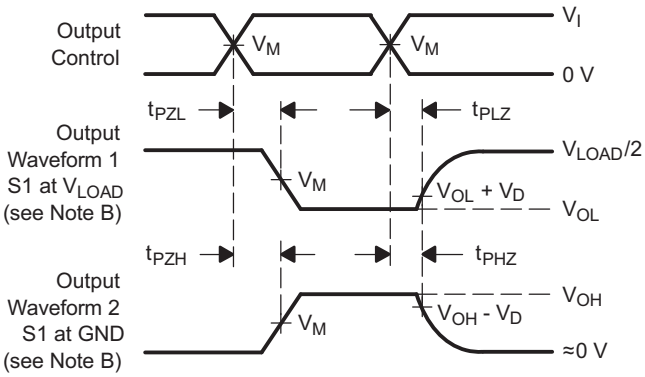


Figure 5. Voltage Waveforms, Propagation Delay Times Inverting and Noninverting Outputs



A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disables by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

H. All parameters and waveforms are not applicable to all devices.

Figure 6. Voltage Waveforms, Enable and Disable Times Low- and High-Level Enabling

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8 Detailed Description

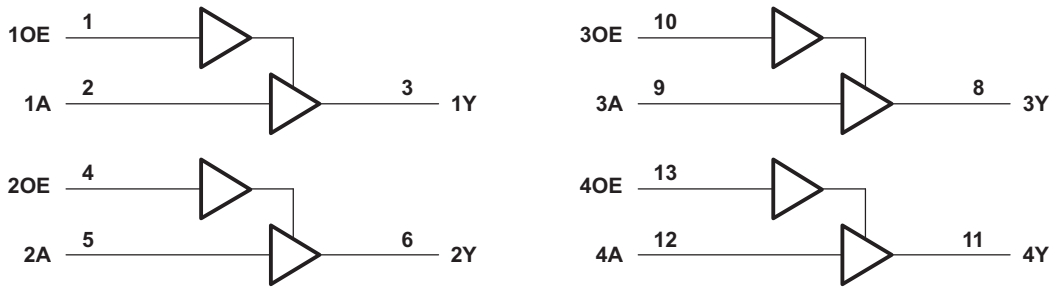
8.1 Overview

The SN74LVC126A quadruple buffer is designed for 1.65-V to 3.6-V V_{CC} operation and features tri-state outputs.

The SN74LVC126A devices perform the Boolean function Y = A in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as down-translators in a mixed 3.3-V or 5-V system environment.

8.2 Functional Block Diagram



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8.3 Feature Description

The SN74LVC126A device features four independent buffers with 3-state outputs, and is designed to operate from a V_{CC} of 1.65 V to 3.6 V. When the output enable (OE) input is low, the corresponding output is disabled and enters a high-impedance state. This device also features high-tolerance inputs, allowing for voltage translation in mixed voltage systems. Wide operating temperature range enables this device to be used in any application, including rugged or extreme environments.

8.4 Device Functional Modes

The SN74LVC126A's 3-state outputs allow the outputs to be disabled using the output enable (OE) pin. To ensure the high-impedance state during power up and power down, OE must be tied to GND through a pulldown resistor. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

Table 3. Function Table (Each Buffer)

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Hi-Z

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC126A device is a high-drive, CMOS device that can be used for a multitude of buffer-type functions. It can produce 24 mA of drive current at 3 V. Therefore, this device is ideal for driving multiple inputs and for high-speed applications up to 100 MHz. The inputs and outputs are 5.5-V tolerant allowing the device to translate up to 5.5 V or down to V_{CC}.

9.2 Typical Application

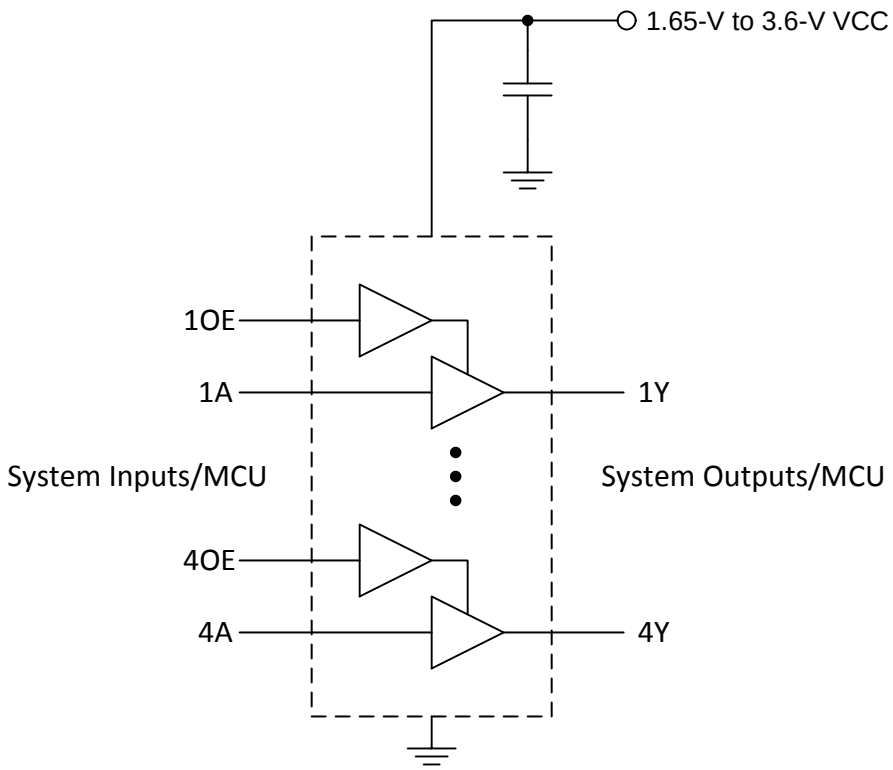

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Figure 7. Typical Buffer Application and Supply Voltage

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads; therefore, routing and load conditions must be considered to prevent ringing.

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Typical Application (continued)

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specifications: See (Δt/ΔV) in *Recommended Operating Conditions.*
   - Specified high and low levels: See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended Output Conditions
   - Load currents must not exceed 25 mA per output and 50 mA total for the part.
   - Outputs must not be pulled above 5.5 V.

9.2.3 Application Curve

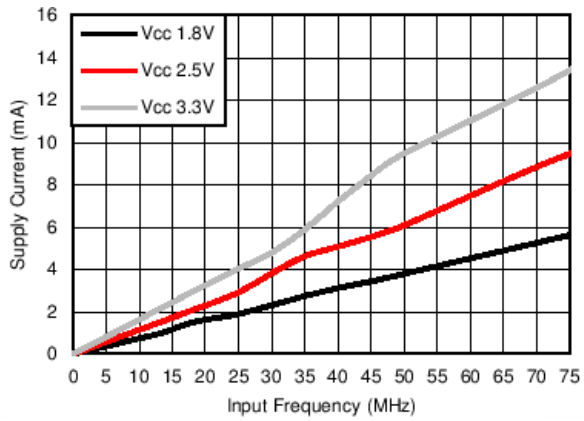

Figure 8. Supply Current vs Input Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating in the *Recommended Operating Conditions*.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple V_{CC} pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

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11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input and gate are used, or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 9 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

11.2 Layout Example

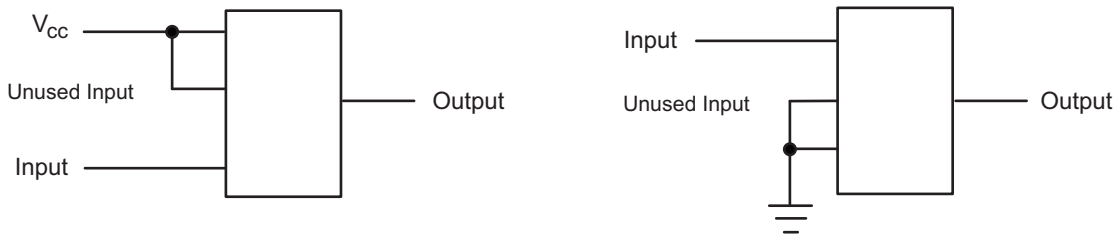

Figure 9. Layout Diagram

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC126AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126ADE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126ADG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126ADRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126ADT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126ADTG4	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126APWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126APWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC126A	Samples
SN74LVC126ARGYRG4	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC126A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC126A :

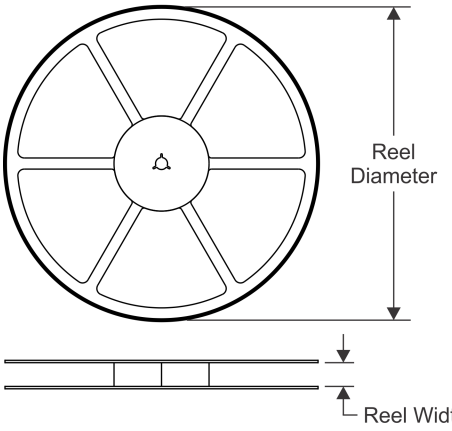
- Automotive: SN74LVC126A-Q1

NOTE: Qualified Version Definitions:

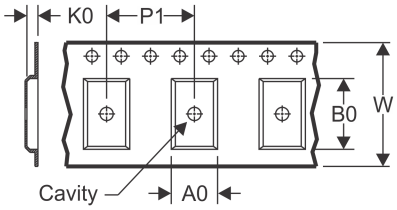
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

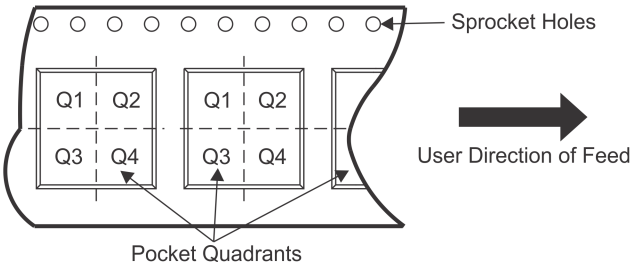


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

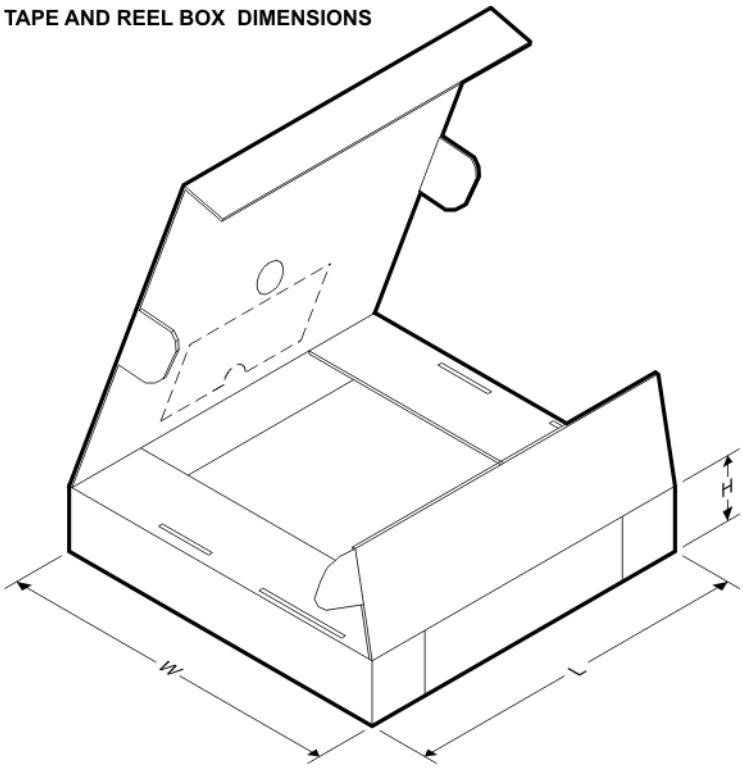
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC126ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC126ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC126ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC126ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC126ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC126APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC126APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC126ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

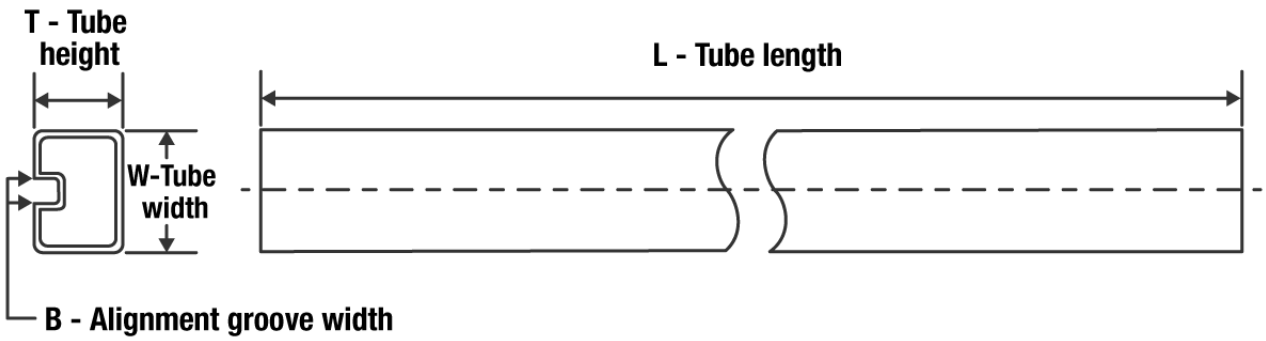
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC126ADBR	SSOP	DB	14	2000	853.0	449.0	35.0
SN74LVC126ADGVR	TVSOP	DGV	14	2000	853.0	449.0	35.0
SN74LVC126ADR	SOIC	D	14	2500	853.0	449.0	35.0
SN74LVC126ADT	SOIC	D	14	250	210.0	185.0	35.0
SN74LVC126ANSR	SO	NS	14	2000	853.0	449.0	35.0
SN74LVC126APWR	TSSOP	PW	14	2000	853.0	449.0	35.0
SN74LVC126APWT	TSSOP	PW	14	250	853.0	449.0	35.0
SN74LVC126ARGYR	VQFN	RGY	14	3000	853.0	449.0	35.0

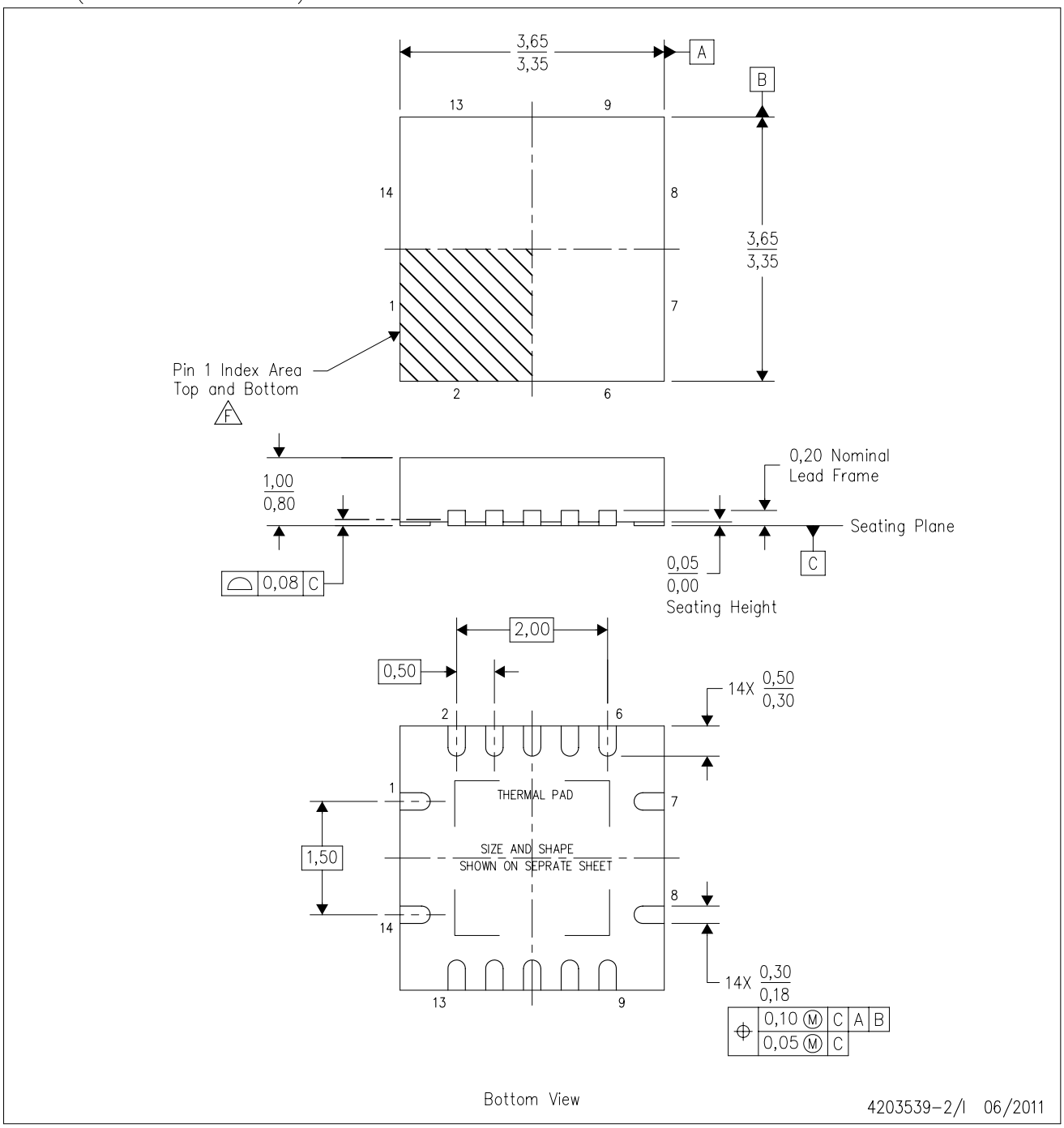
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVC126AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC126ADE4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC126ADG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC126APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC126APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5

RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.

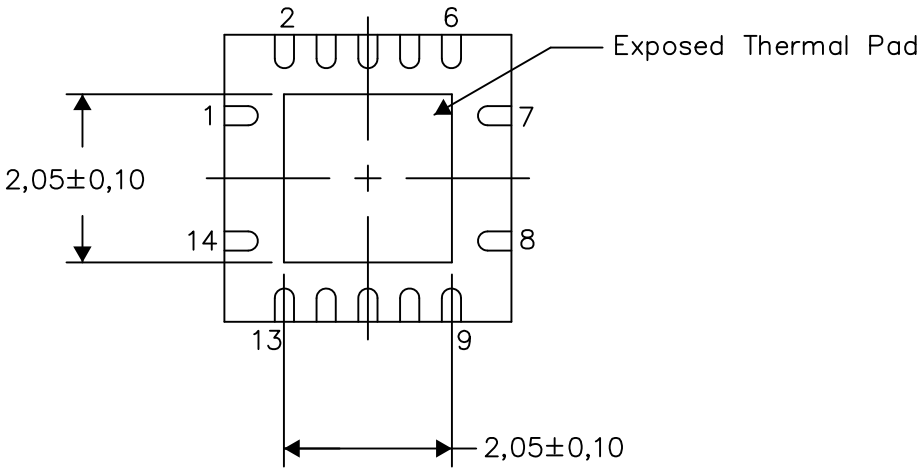
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



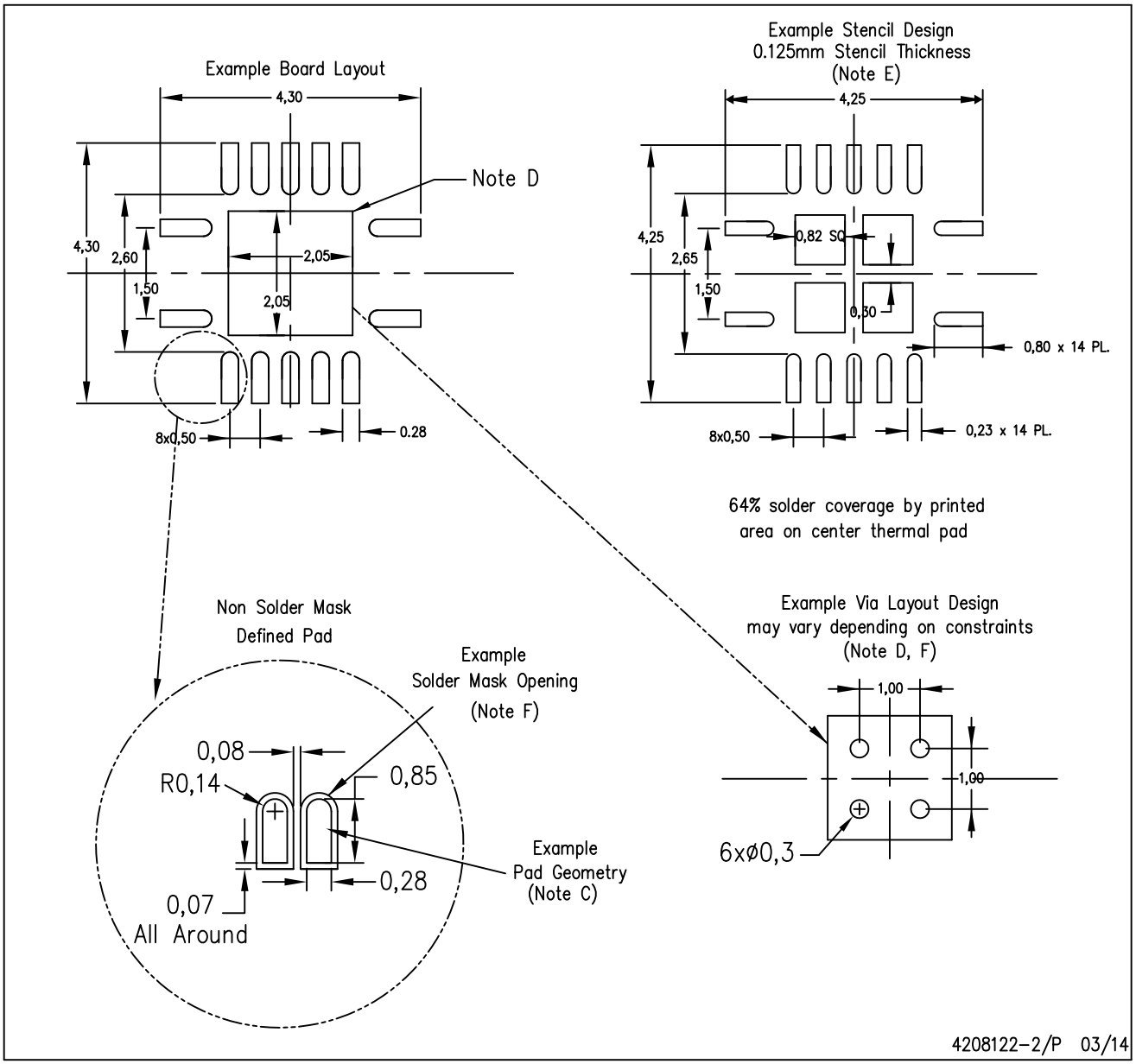
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

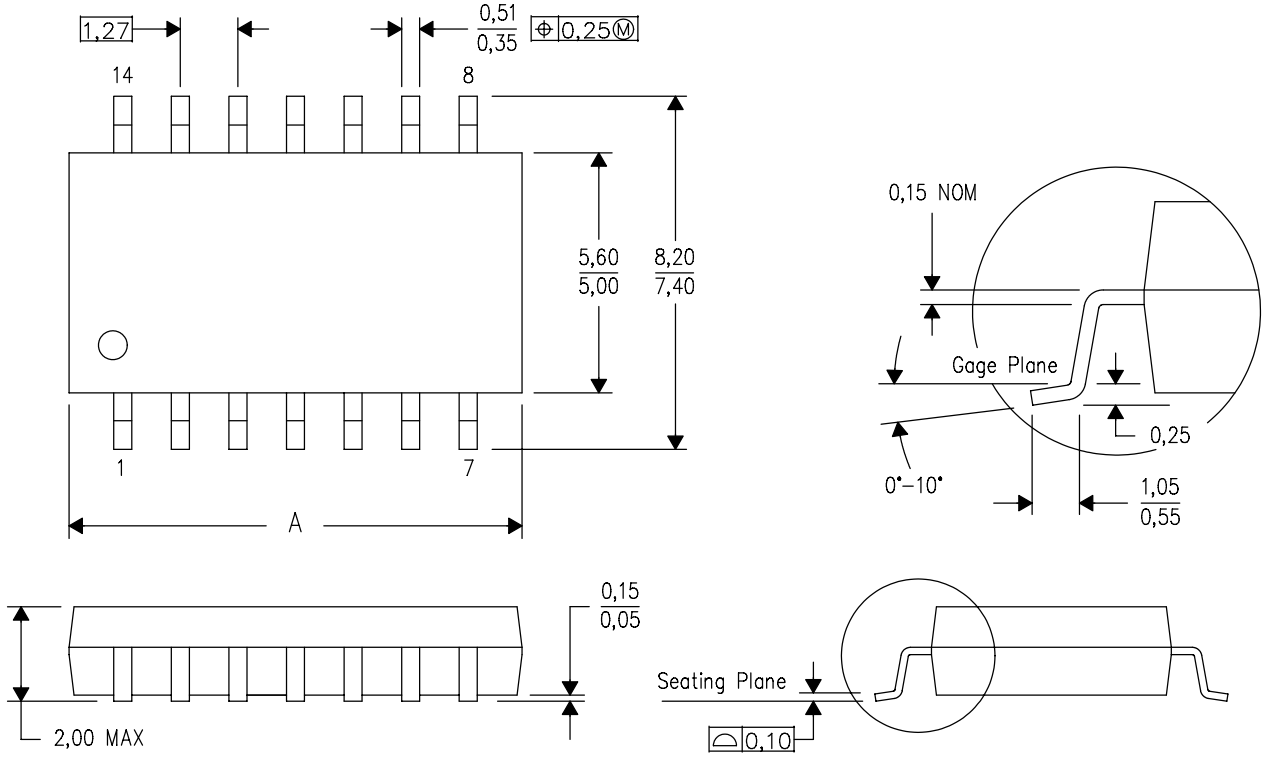


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

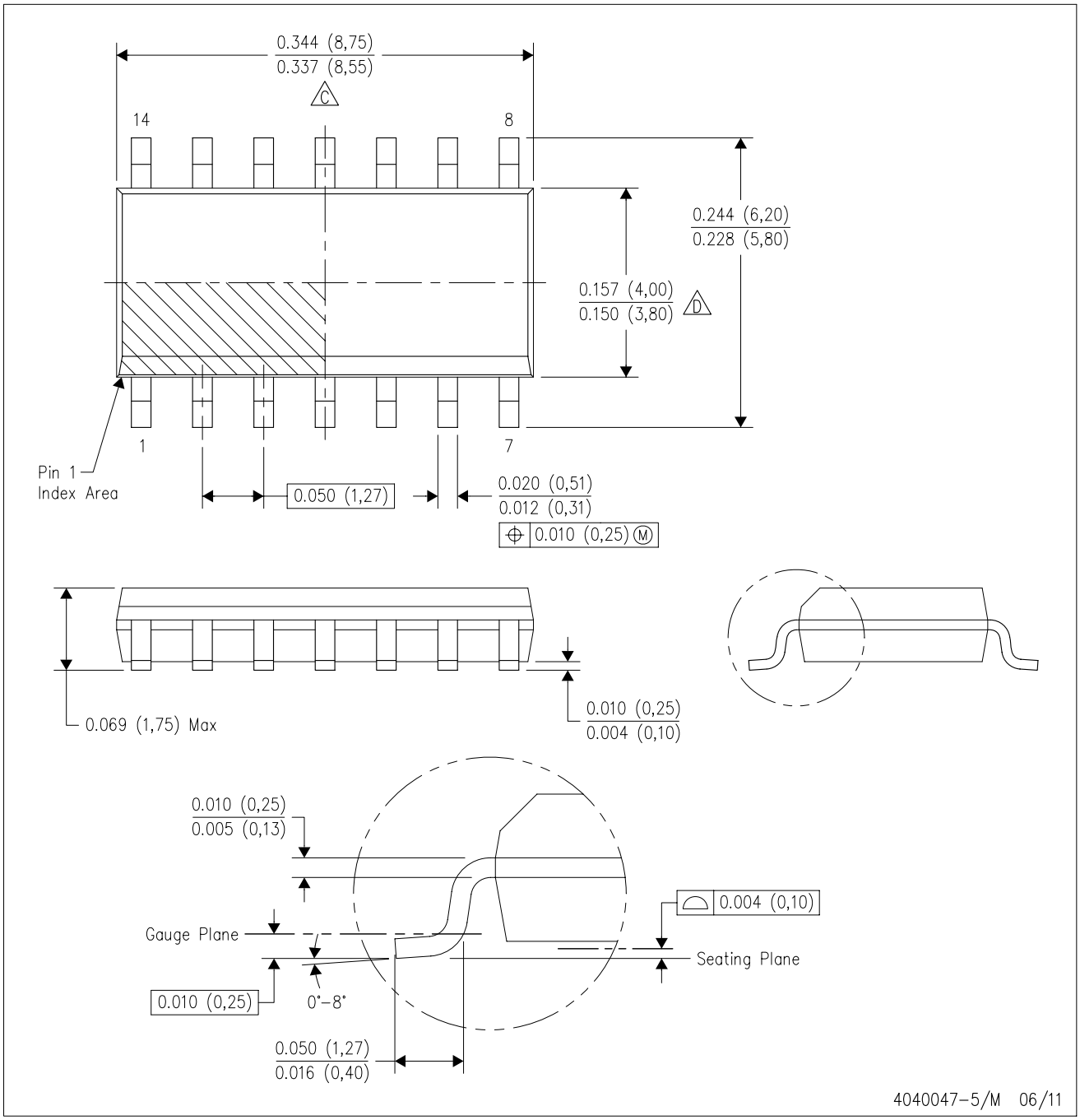


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

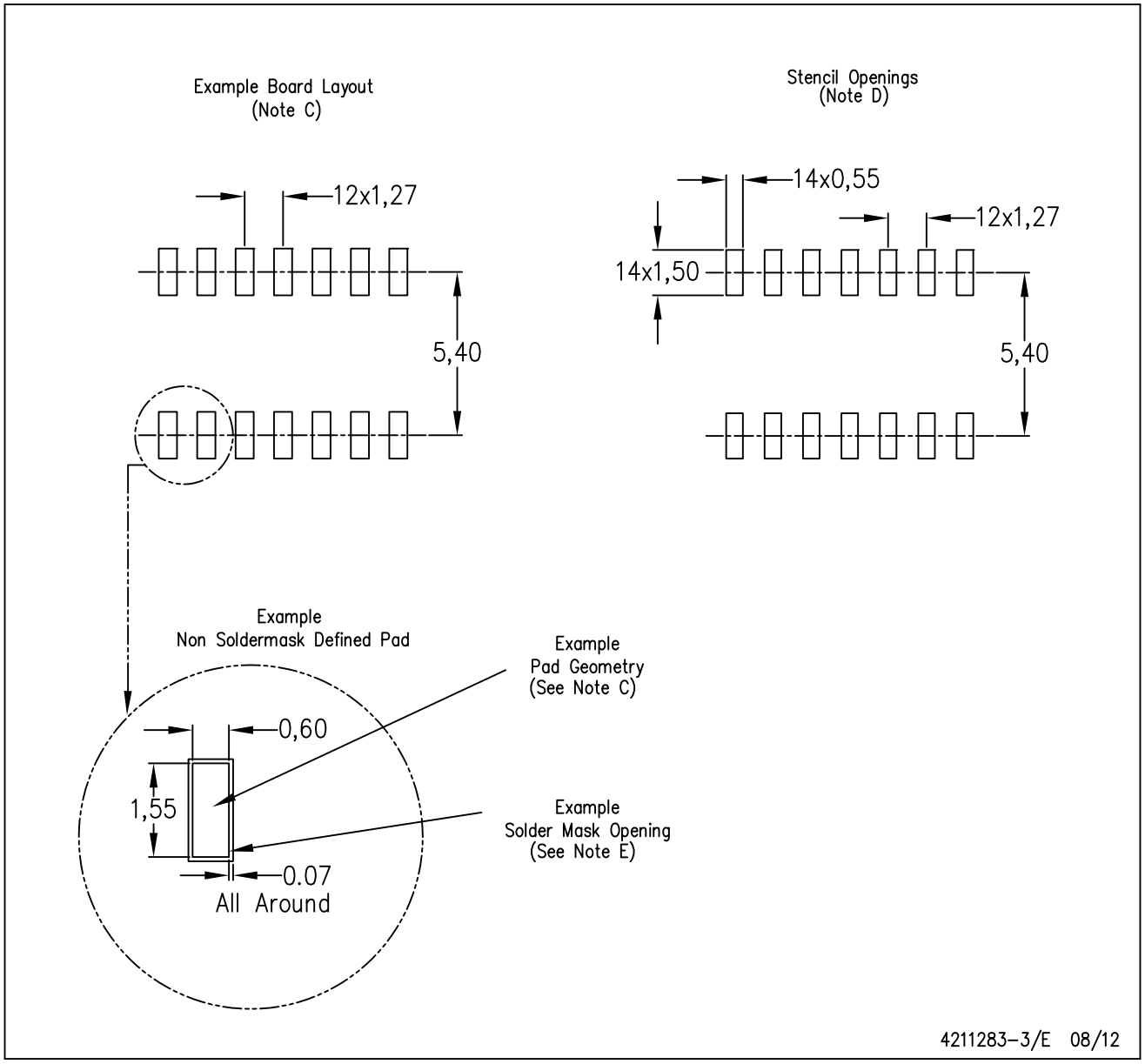
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



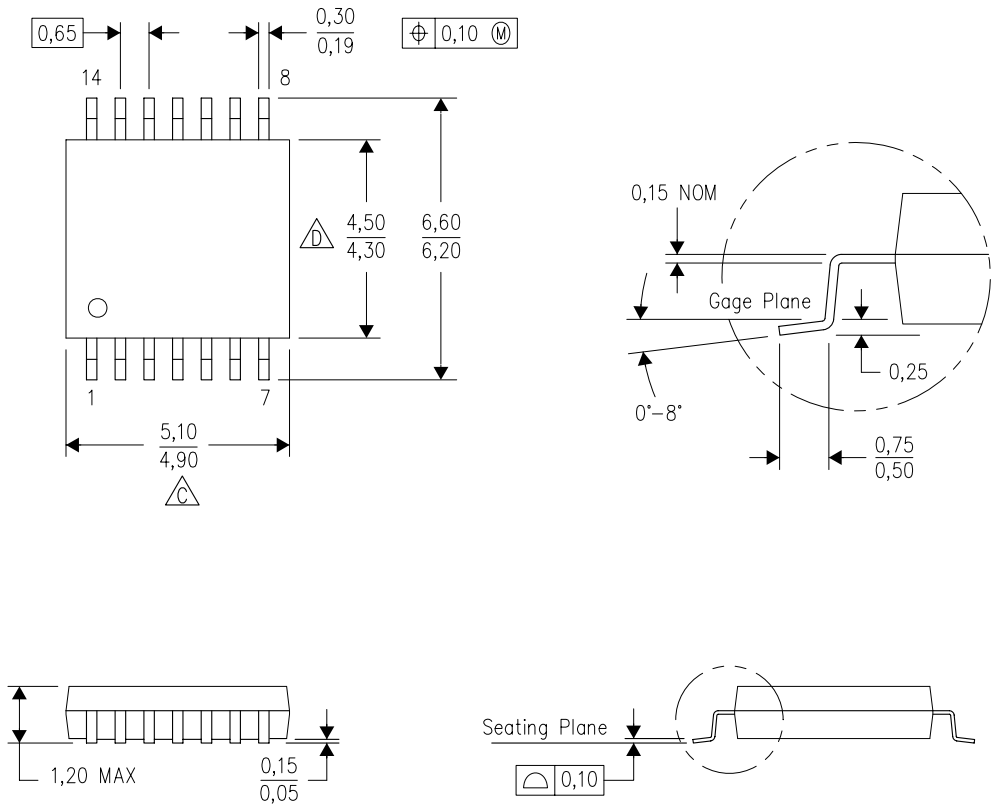
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



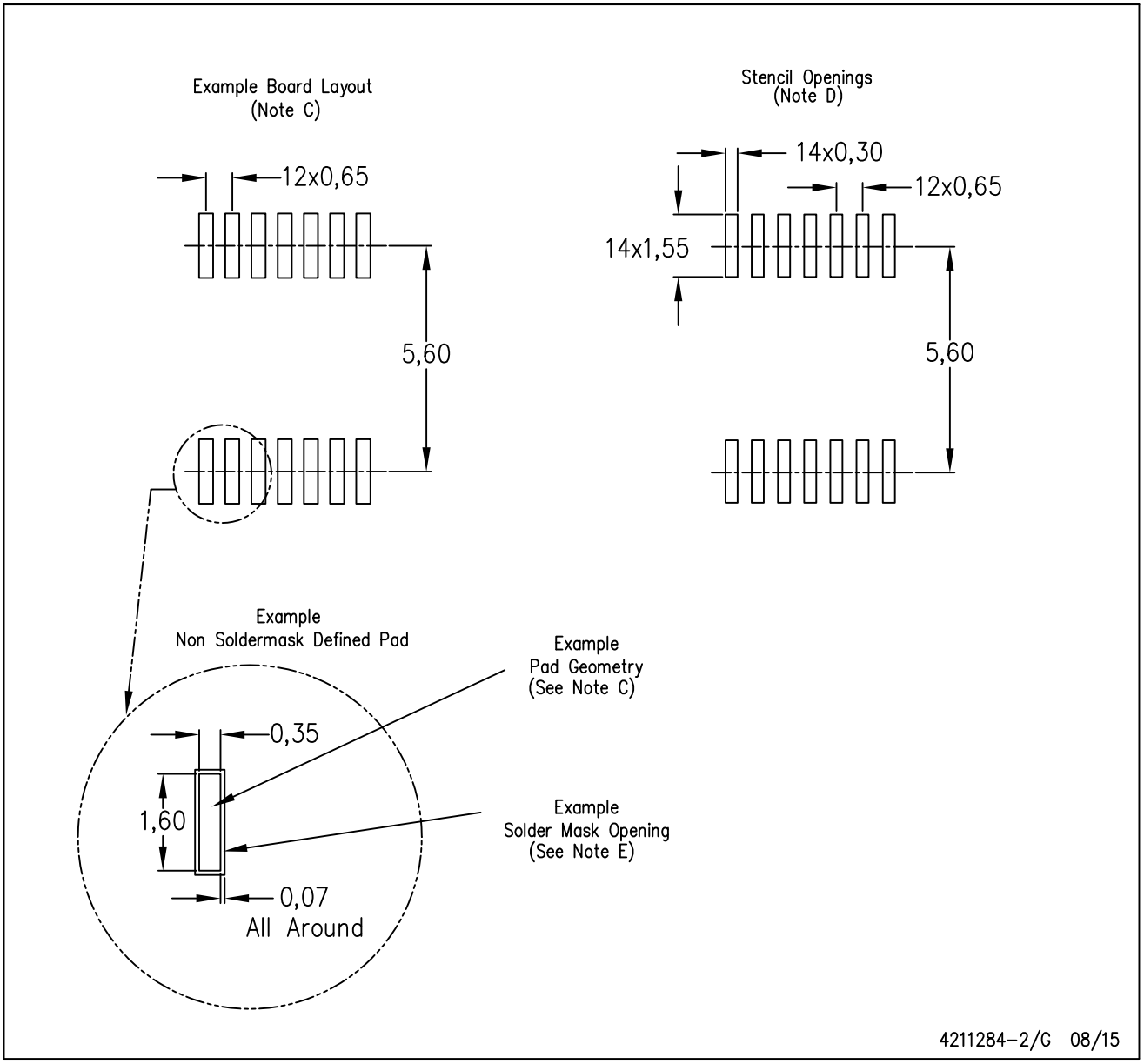
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

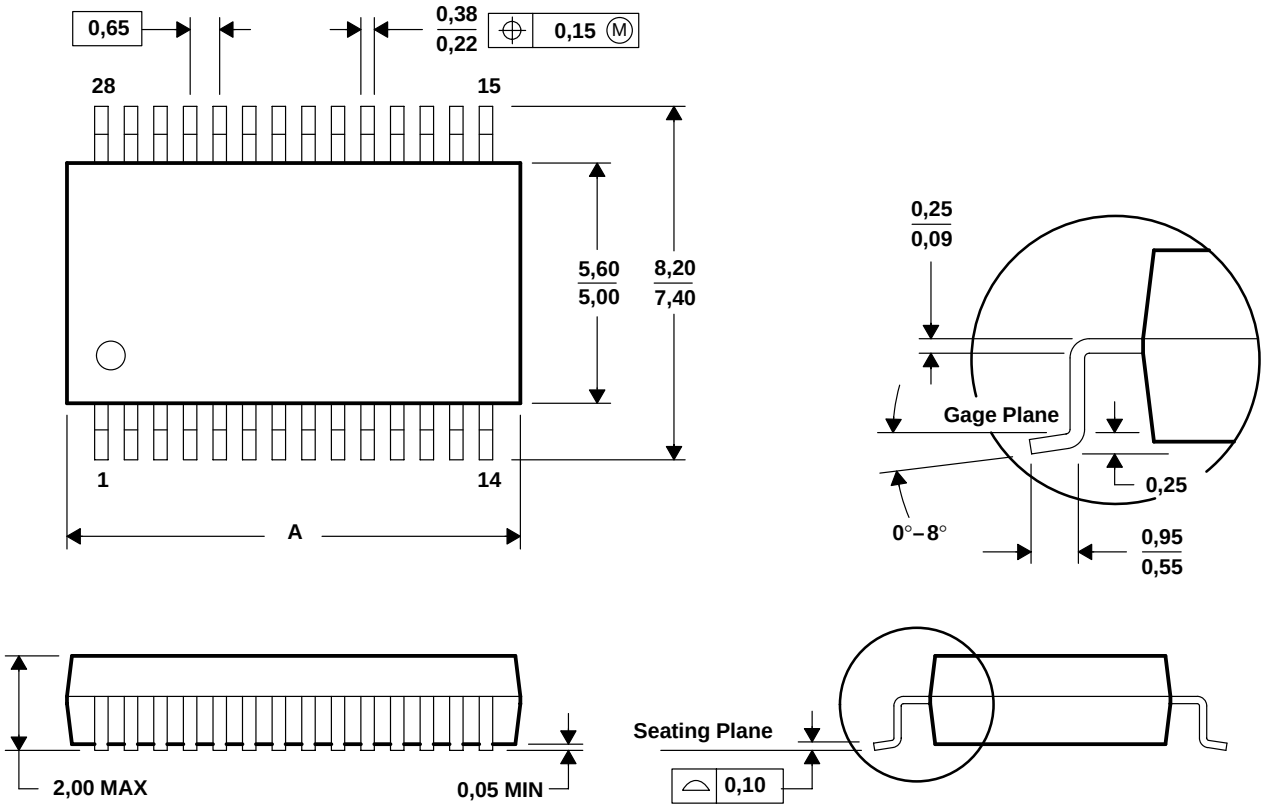
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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