



## SN74LV05A Hex Inverters With Open-Drain Outputs

### 1 Features

- 2-V to 5.5-V  $V_{CC}$  Operation
- Typical  $V_{OLP}$  (Output Ground Bounce)  
< 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  
> 2.3 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2500-V Human-Body Model
  - 200-V Machine Model
  - 2000-V Charged-Device Model

### 2 Applications

- Electronic Points of Sale
- I/O Modules: Digital PLC/DCS Inputs
- Motor Drives and Controls
- Servers
- Network Switches
- Tests and Measurements

### 3 Description

The SN74LV05A device contains six independent inverters designed for 2-V to 5.5-V  $V_{CC}$  operation.

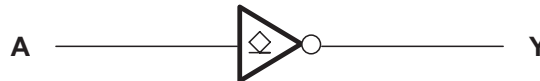
This device performs the Boolean function  $Y = \bar{A}$ .

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV05A	TVSOP (14)	3.60 mm x 4.40 mm
	SOIC (14)	8.65 mm x 3.91 mm
	SOP (14)	10.30 mm x 5.30 mm
	SSOP (14)	6.20 mm x 5.30 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Simplified Schematic



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>9 Detailed Description</b> .....	<b>8</b>
<b>2 Applications</b> .....	<b>1</b>	9.1 Overview .....	8
<b>3 Description</b> .....	<b>1</b>	9.2 Functional Block Diagram .....	8
<b>4 Simplified Schematic</b> .....	<b>1</b>	9.3 Feature Description .....	8
<b>5 Revision History</b> .....	<b>2</b>	9.4 Device Functional Modes .....	8
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	<b>10 Application and Implementation</b> .....	<b>9</b>
<b>7 Specifications</b> .....	<b>4</b>	10.1 Application Information .....	9
7.1 Absolute Maximum Ratings .....	4	10.2 Typical Application .....	9
7.2 ESD Ratings .....	4	<b>11 Power Supply Recommendations</b> .....	<b>10</b>
7.3 Recommended Operating Conditions .....	5	<b>12 Layout</b> .....	<b>11</b>
7.4 Thermal Information .....	5	12.1 Layout Guidelines .....	11
7.5 Electrical Characteristics .....	5	12.2 Layout Example .....	11
7.6 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ .....	6	<b>13 Device and Documentation Support</b> .....	<b>11</b>
7.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ .....	6	13.1 Related Links .....	11
7.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....	6	13.2 Trademarks .....	11
7.9 Noise Characteristics .....	6	13.3 Electrostatic Discharge Caution .....	11
7.10 Operating Characteristics .....	6	13.4 Glossary .....	11
7.11 Typical Characteristics .....	7	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>11</b>
<b>8 Parameter Measurement Information</b> .....	<b>7</b>		

## 5 Revision History

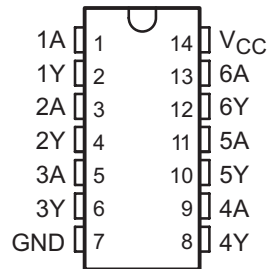
### Changes from Revision I (April 2005) to Revision J

Page

• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....	1
• Deleted <i>Ordering Information</i> table. ....	1
• MAX operating temperature to 125°C in <i>Recommended Operating Conditions</i> table. ....	5

## 6 Pin Configuration and Functions

SN74LV05A . . . D, DB, DGV, NS, OR PW PACKAGE  
(TOP VIEW)



**Pin Functions**

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	1A	I	1A Input
2	1Y	O	1Y Output
3	2A	I	2A Input
4	2Y	O	2Y Output
5	3A	I	3A Input
6	3Y	O	3Y Output
7	GND	—	Ground Pin
8	4Y	O	4Y Output
9	4A	I	4A Input
10	5Y	O	5Y Output
11	5A	I	5A Input
12	6Y	O	6Y Output
13	6A	I	6A Input
14	V <sub>CC</sub>	—	Power Pin

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V
V <sub>O</sub>	Output voltage range <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-20 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25 mA
	Continuous current through V <sub>CC</sub> or GND			±50 mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5-V maximum.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	2500
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	2000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7	
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7	
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	5.5	V
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	2	
		V <sub>CC</sub> = 3 V to 3.6 V	6	
		V <sub>CC</sub> = 4.5 V to 5.5 V	12	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V	200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V	100	
		V <sub>CC</sub> = 4.5 V to 5.5 V	20	
T <sub>A</sub>	Operating free-air temperature	−40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74LV05A					UNIT	
	D	DB	DGV	NS	PW		
	14 PINS						
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	94.9	107.4	130.4	91.4	122.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	56.3	59.9	53.4	49.0	51.3	
R <sub>θJB</sub>	Junction-to-board thermal resistance	49.2	54.7	63.5	50.2	64.4	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	20.7	21.0	7.3	15.3	6.8	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	48.9	51.2	62.8	49.8	63.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

### 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			−40°C to 85°C		−40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V			0.1		0.1		0.1	V
	I <sub>OL</sub> = 2 mA	2.3 V			0.4		0.4		0.4	
	I <sub>OL</sub> = 6 mA	3 V			0.44		0.44		0.44	
	I <sub>OL</sub> = 12 mA	4.5 V			0.55		0.55		0.6	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±1		±1		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5			20		20		20	μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0			5		5		5	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			2.5					pF

## SN74LV05A

SCLS391J – APRIL 1998 – REVISED DECEMBER 2014

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### 7.6 Switching Characteristics, $V_{CC} = 2.5 V \pm 0.2 V$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15 \text{ pF}$	3.6 <sup>(1)</sup>	10.4 <sup>(1)</sup>		1	13	1	13.5	ns
$t_{PHL}$				5.8 <sup>(1)</sup>	12.2 <sup>(1)</sup>		1	15	1	16.5	
$t_{PLH}$	A	Y	$C_L = 50 \text{ pF}$	6.1	15.2		1	18	1	18.5	ns
$t_{PHL}$				8.1	16.6		1	19.5	1	21	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

### 7.7 Switching Characteristics, $V_{CC} = 3.3 V \pm 0.3 V$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15 \text{ pF}$	2.9 <sup>(1)</sup>	7.1 <sup>(1)</sup>		1	8.5	1	9	ns
$t_{PHL}$				4 <sup>(1)</sup>	7.1 <sup>(1)</sup>		1	8.5	1	9.5	
$t_{PLH}$	A	Y	$C_L = 50 \text{ pF}$	4.7	10.6		1	12	1	12.5	ns
$t_{PHL}$				5.8	10.6		1	12	1	13	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

### 7.8 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15 \text{ pF}$	2.2 <sup>(1)</sup>	5.5 <sup>(1)</sup>		1	6.5	1	7	ns
$t_{PHL}$				2.9 <sup>(1)</sup>	5.5 <sup>(1)</sup>		1	6.5	1	7.5	
$t_{PLH}$	A	Y	$C_L = 50 \text{ pF}$	3.4	7.5		1	8.5	1	9	ns
$t_{PHL}$				4.2	7.5		1	8.5	1	9.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

### 7.9 Noise Characteristics<sup>(1)</sup>

$V_{CC} = 3.3 V$ ,  $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		SN74LV05A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.55	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.04	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		3.12		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.97	V

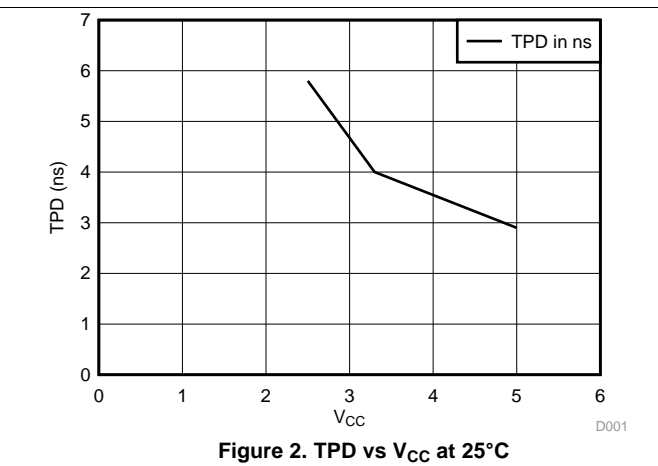
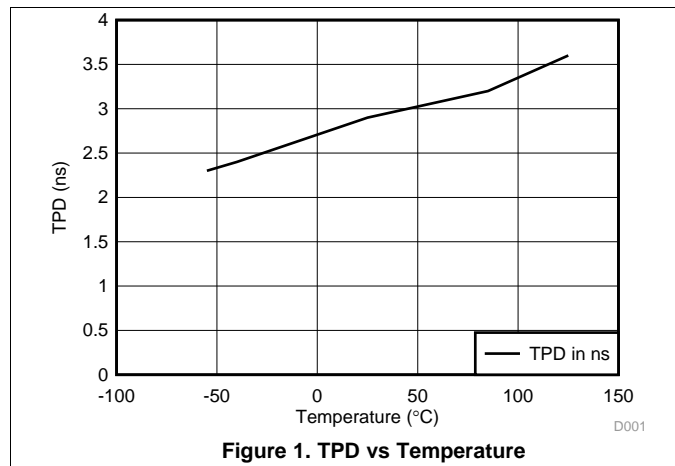
(1) Characteristics are for surface-mount packages only.

### 7.10 Operating Characteristics

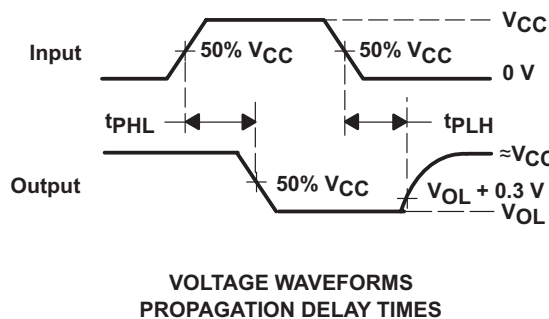
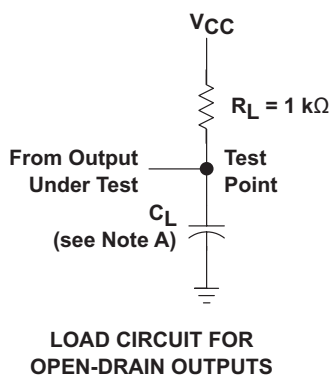
$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50 \text{ pF}$ ,	$f = 10 \text{ MHz}$	3.3 V	2.5	pF
				5 V	3	

### 7.11 Typical Characteristics



## 8 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.  
 C. The outputs are measured one at a time, with one input transition per measurement.

Figure 3. Load Circuit and Voltage Waveforms

## 9 Detailed Description

### 9.1 Overview

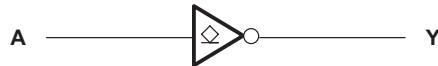
The SN74LV05A device contains six independent inverters designed for 2-V to 5.5-V  $V_{CC}$  operation.

This device performs the Boolean function  $Y = \bar{A}$ .

The open-drain outputs require pull-up resistors to perform correctly and can be connected to other open-drain outputs to implement active-low, wired-OR or active-high wired-AND functions.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 9.2 Functional Block Diagram



**Figure 4. Logic Diagram (Positive Logic)**

### 9.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down-voltage translation
  - Inputs accept voltages to 5.5 V
- $I_{off}$  feature
  - Allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V

### 9.4 Device Functional Modes

**Table 1. Function Table  
(Each Inverter)**

INPUT A	OUTPUT Y
H	L
L	H

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

SN74LV05A is a low-drive, open-drain CMOS device that can be used for a multitude of buffer type functions. The inputs are 5.5-V tolerant and the outputs are open-drain and 5.5-V tolerant, allowing it to translate up to 5.5 V or down to any other voltage between GND and 5.5 V.

### 10.2 Typical Application

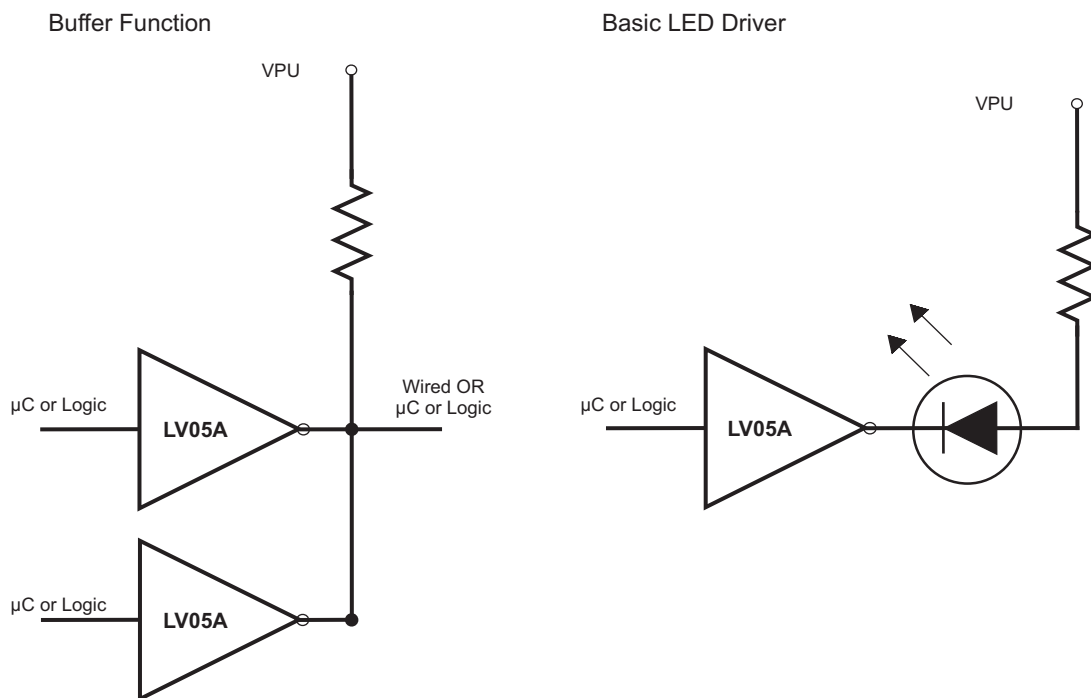


Figure 5. Typical Application Schematic

#### 10.2.1 Design Requirements

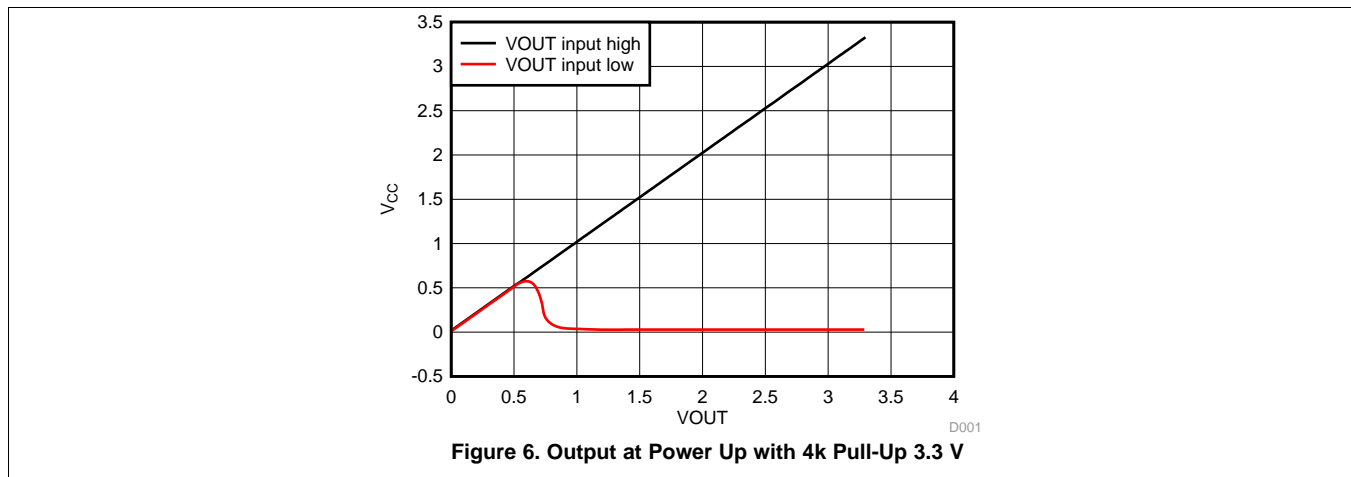
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - For rise time and fall time specifications, see  $\Delta t/\Delta V$  in the [Recommended Operating Conditions](#) table.
  - For specified High and low levels, see  $V_{IH}$  and  $V_{IL}$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommend Output Conditions
  - Load currents should not exceed 35 mA per output and 50 mA total for the part.

## Typical Application (continued)

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 7](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver.

### 12.2 Layout Example

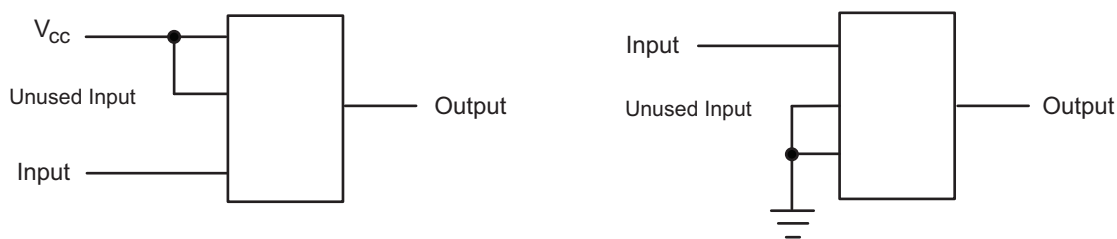


Figure 7. Layout Diagram

## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV05A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.2 Trademarks

All trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV05AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV05A	<a href="#">Samples</a>
SN74LV05ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV05A	<a href="#">Samples</a>
SN74LV05ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV05A	<a href="#">Samples</a>
SN74LV05ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV05A	<a href="#">Samples</a>
SN74LV05ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV05A	<a href="#">Samples</a>
SN74LV05APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV05A	<a href="#">Samples</a>
SN74LV05APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV05A	<a href="#">Samples</a>
SN74LV05APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV05A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV05ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV05ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV05ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV05APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV05APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV05ADGVR	TVSOP	DGV	14	2000	853.0	449.0	35.0
SN74LV05ADR	SOIC	D	14	2500	853.0	449.0	35.0
SN74LV05ANSR	SO	NS	14	2000	853.0	449.0	35.0
SN74LV05APWR	TSSOP	PW	14	2000	853.0	449.0	35.0
SN74LV05APWT	TSSOP	PW	14	250	853.0	449.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LV05AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LV05APW	PW	TSSOP	14	90	530	10.2	3600	3.5

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

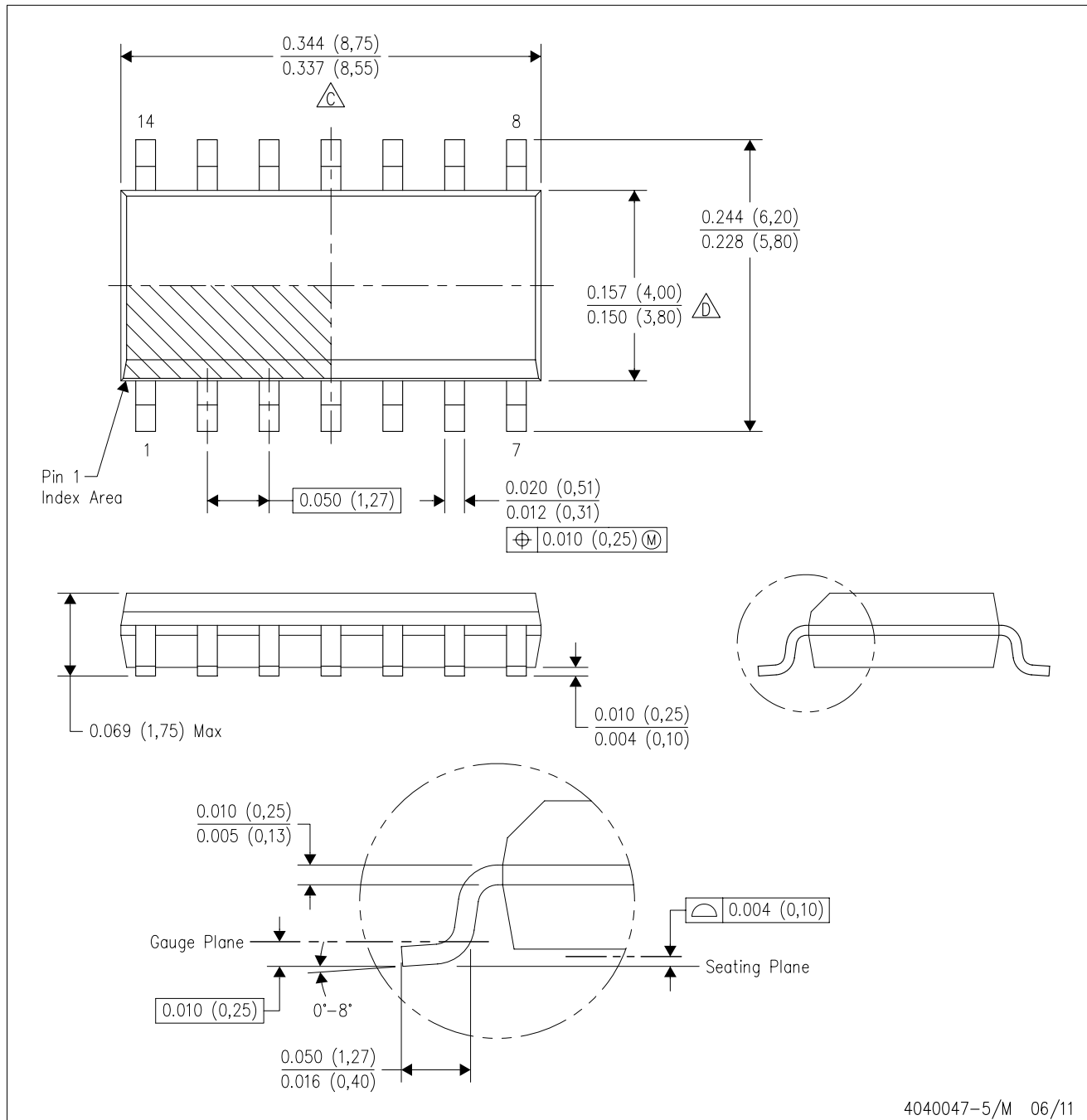


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- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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