

- Low Supply-Voltage Range, 1.8 V to 3.6 V
- Ultralow-Power Consumption:  
Active Mode: 250  $\mu$ A at 1 MHz, 2.2 V  
Standby Mode: 1.1  $\mu$ A  
Off Mode (RAM Retention): 0.1  $\mu$ A
- Five Power Saving Modes
- Wake-Up From Standby Mode in Less Than 6  $\mu$ s
- 16-Bit RISC Architecture, 125-ns Instruction Cycle Time
- 16-Bit Sigma-Delta A/D Converter With Internal Reference and Five Differential Analog Inputs
- 12-Bit D/A Converter
- Two Configurable Operational Amplifiers
- 16-Bit Timer\_A With Three Capture/Compare Registers
- Brownout Detector
- Bootstrap Loader
- Serial Onboard Programming, No External Programming Voltage Needed  
Programmable Code Protection by Security Fuse
- Integrated LCD Driver With Contrast Control for up to 56 Segments
- MSP430FG42x0 Family Members Include:  
MSP430FG4250: 16KB+256B Flash Memory  
256B RAM  
MSP430FG4260: 24KB+256B Flash Memory  
256B RAM  
MSP430FG4270: 32KB+256B Flash Memory  
256B RAM
- For Complete Module Descriptions, See *MSP430x4xx Family User's Guide*, Literature Number SLAU056
- For Additional Device Information, See *MSP430FG42x0 Device Erratasheet*, Literature Number SLAZ038

## description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6  $\mu$ s.

The MSP430FG42x0 is a microcontroller configuration with a 16-bit timer, a high-performance 16-bit sigma-delta A/D converter, 12-bit D/A converter, two configurable operational amplifiers, 32 I/O pins, and a liquid crystal display driver.

Typical applications for this device include analog and digital sensor systems, digital motor control, remote controls, thermostats, digital timers, hand-held meters, etc.

### AVAILABLE OPTIONS

| T <sub>A</sub> | PACKAGED DEVICES         |                          |
|----------------|--------------------------|--------------------------|
|                | PLASTIC 48-PIN SSOP (DL) | PLASTIC 48-PIN QFN (RGZ) |
| -40°C to 85°C  | MSP430FG4250IDL          | MSP430FG4250IRGZ         |
|                | MSP430FG4260IDL          | MSP430FG4260IRGZ         |
|                | MSP430FG4270IDL          | MSP430FG4270IRGZ         |



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

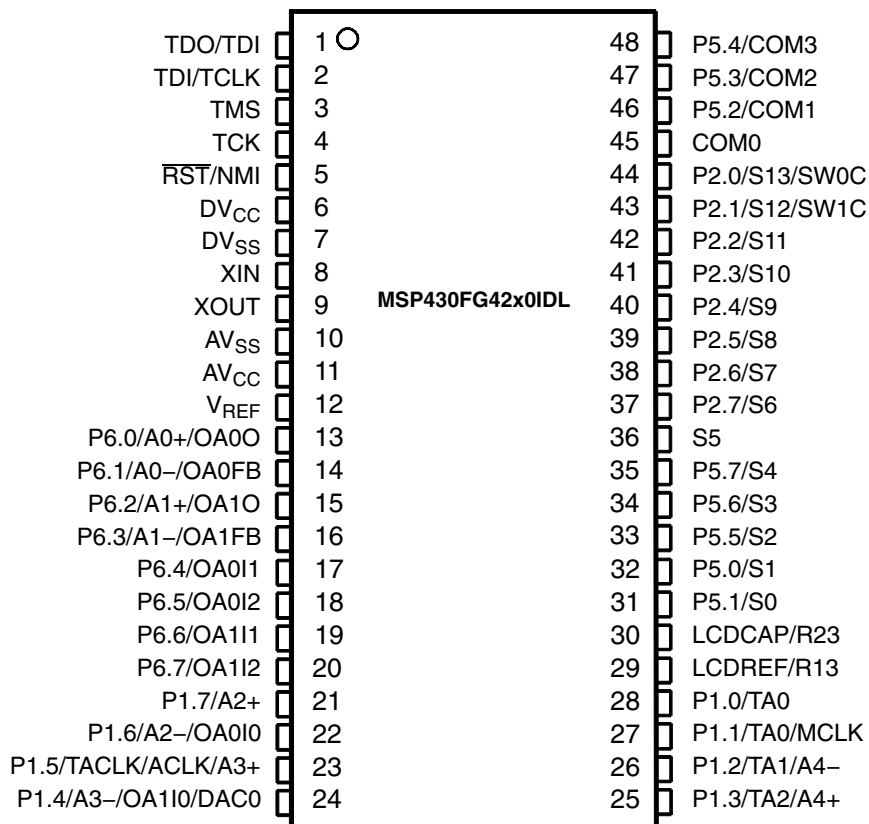


# MSP430FG42x0 MIXED SIGNAL MICROCONTROLLER

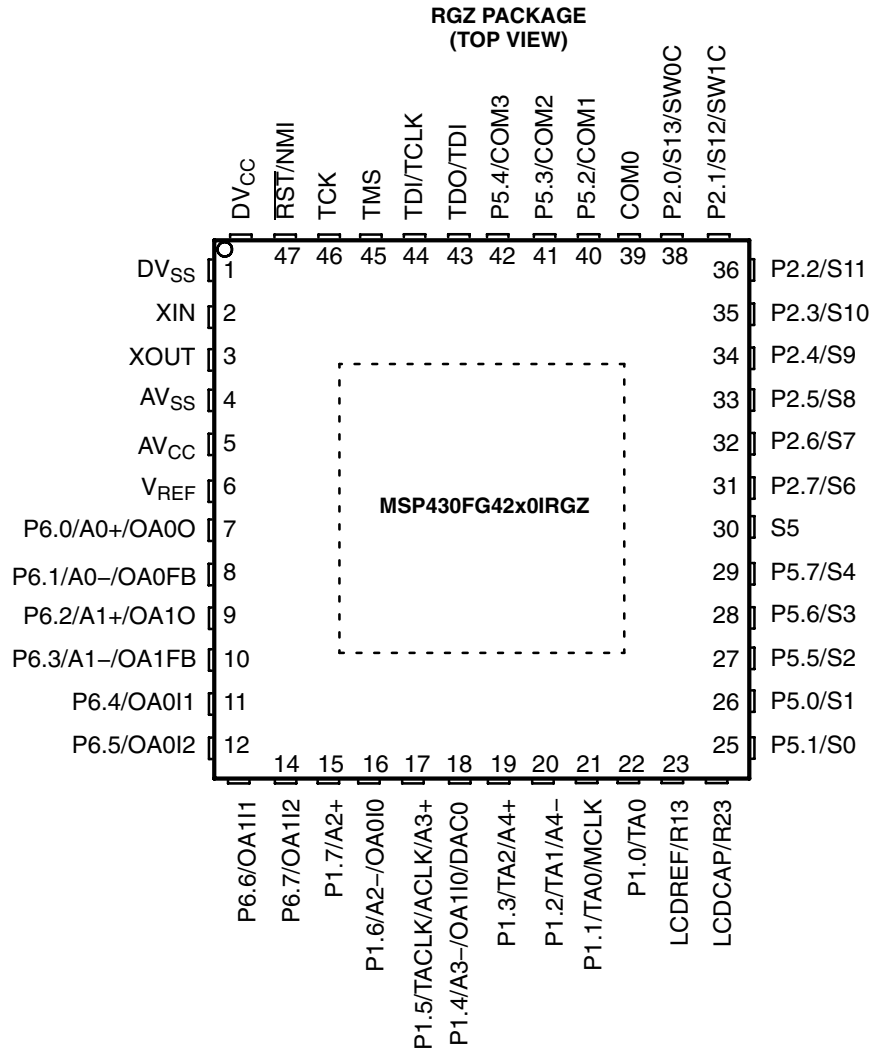
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## pin designation, DL package

### DL PACKAGE (TOP VIEW)



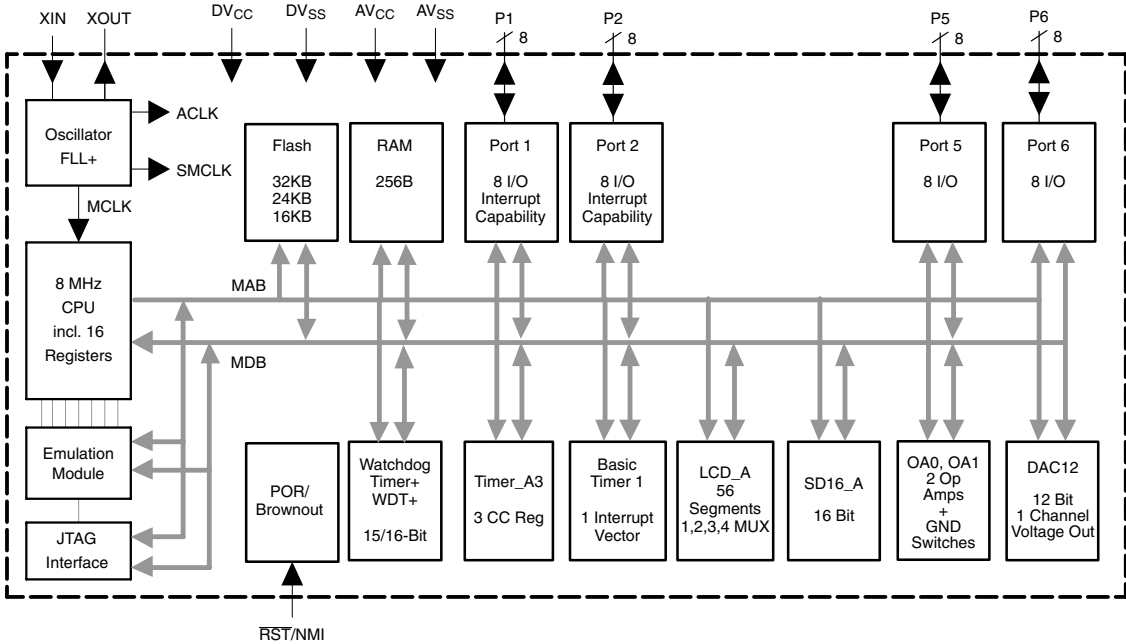
pin designation, RGZ package



# MSP430FG42x0 MIXED SIGNAL MICROCONTROLLER

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## functional block diagram



### Terminal Functions

| TERMINAL            |        |         |     | DESCRIPTION   |
|---------------------|--------|---------|-----|---|
| NAME                | DL NO. | RGZ NO. | I/O |   |
| TDO/TDI             | 1      | 43      | I/O | Test data output. TDO/TDI data output or programming data input terminal  |
| TDI/TCLK            | 2      | 44      | I   | Test data input / test clock input. The device protection fuse is connected to TDI/TCLK.                                    |
| TMS                 | 3      | 45      | I   | Test mode select. TMS is used as an input port for device programming and test.   |
| TCK                 | 4      | 46      | I   | Test clock. TCK is the clock input port for device programming and test.  |
| RST/NMI             | 5      | 47      | I   | General-purpose digital I/O / reset input / nonmaskable interrupt input   |
| DV <sub>CC</sub>    | 6      | 48      |     | Digital supply voltage, positive terminal   |
| DV <sub>SS</sub>    | 7      | 1       |     | Digital supply voltage, negative terminal   |
| XIN                 | 8      | 2       | I   | Input terminal of crystal oscillator XT1  |
| XOUT                | 9      | 3       | O   | Output terminal of crystal oscillator XT1   |
| AV <sub>SS</sub>    | 10     | 4       |     | Analog supply voltage, negative terminal  |
| AV <sub>CC</sub>    | 11     | 5       |     | Analog supply voltage, positive terminal  |
| V <sub>REF</sub>    | 12     | 6       | I/O | Analog reference voltage  |
| P6.0/A0+/OA0O       | 13     | 7       | I/O | General-purpose digital I/O / analog input A0+ / OA0 output   |
| P6.1/A0-/OA0FB      | 14     | 8       | I/O | General-purpose digital I/O / analog input A0- / OA0 feedback input   |
| P6.2/A1+/OA1O       | 15     | 9       | I/O | General-purpose digital I/O / analog input A1+ / OA1 output   |
| P6.3/A1-/OA1FB      | 16     | 10      | I/O | General-purpose digital I/O / analog input A1- / OA1 feedback input   |
| P6.4/OA0I1          | 17     | 11      | I/O | General-purpose digital I/O / OA0 input multiplexer on -terminal  |
| P6.5/OA0I2          | 18     | 12      | I/O | General-purpose digital I/O / OA0 input multiplexer on -terminal  |
| P6.6/OA1I1          | 19     | 13      | I/O | General-purpose digital I/O / OA1 input multiplexer on -terminal  |
| P6.7/OA1I2          | 20     | 14      | I/O | General-purpose digital I/O / OA1 input multiplexer on -terminal  |
| P1.7/A2+            | 21     | 15      | I/O | General-purpose digital I/O / analog input A2+  |
| P1.6/A2-/OA0I0      | 22     | 16      | I/O | General-purpose digital I/O / analog input A2- / OA0 input multiplexer on +terminal   |
| P1.5/TACLK/ACLK/A3+ | 23     | 17      | I/O | General-purpose digital I/O / Timer_A, clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8) / analog input A3+ |
| P1.4/A3-/OA1I0/DAC0 | 24     | 18      | I/O | General-purpose digital I/O / analog input A3- / OA1 input multiplexer on +terminal / DAC12 output                          |
| P1.3/TA2/A4+        | 25     | 19      | I/O | General-purpose digital I/O / Timer_A, Capture: CCI2A, compare: Out2 output / analog input A4+                              |
| P1.2/TA1/A4-        | 26     | 20      | I/O | General-purpose digital I/O / Timer_A, Capture: CCI1A, compare: Out1 output / analog input A4-                              |
| P1.1/TA0/MCLK       | 27     | 21      | I/O | General-purpose digital I/O / Timer_A. Capture: CCI0B / MCLK output. Note: TA0 is only an input on this pin / BSL Receive   |
| P1.0/TA0            | 28     | 22      | I/O | General-purpose digital I/O / Timer_A. Capture: CCI0A input, compare: Out0 output / BSL transmit                            |
| LCDREF/R13          | 29     | 23      |     | External LCD reference voltage input / input port of third most positive analog LCD level (V4 or V3)                        |
| LDCAP/R23           | 30     | 24      |     | Capacitor connection for LCD charge pump / input port of second most positive analog LCD level (V2)                         |
| P5.1/S0             | 31     | 25      | I/O | General-purpose digital I/O / LCD segment output 0  |
| P5.0/S1             | 32     | 26      | I/O | General-purpose digital I/O / LCD segment output 1  |
| P5.5/S2             | 33     | 27      | I/O | General-purpose digital I/O / LCD segment output 2  |
| P5.6/S3             | 34     | 28      | I/O | General-purpose digital I/O / LCD segment output 3  |
| P5.7/S4             | 35     | 29      | I/O | General-purpose digital I/O / LCD segment output 4  |
| S5                  | 36     | 30      | O   | LCD segment output 5  |
| P2.7/S6             | 37     | 31      | I/O | General-purpose digital I/O / LCD segment output 6  |
| P2.6/S7             | 38     | 32      | I/O | General-purpose digital I/O / LCD segment output 7  |

# MSP430FG42x0 MIXED SIGNAL MICROCONTROLLER

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## Terminal Functions (Continued)

| TERMINAL      |        |         |     | DESCRIPTION   |
|---------------|--------|---------|-----|---|
| NAME          | DL NO. | RGZ NO. | I/O |   |
| P2.5/S8       | 39     | 33      | I/O | General-purpose digital I/O / LCD segment output 8                                      |
| P2.4/S9       | 40     | 34      | I/O | General-purpose digital I/O / LCD segment output 9                                      |
| P2.3/S10      | 41     | 35      | I/O | General-purpose digital I/O / LCD segment output 10                                     |
| P2.2/S11      | 42     | 36      | I/O | General-purpose digital I/O / LCD segment output 11                                     |
| P2.1/S12/SW1C | 43     | 37      | I/O | General-purpose digital I/O / LCD segment output 12 / Low resistance switch to $V_{SS}$ |
| P2.0/S13/SW0C | 44     | 38      | I/O | General-purpose digital I/O / LCD segment output 13 / Low resistance switch to $V_{SS}$ |
| COM0          | 45     | 39      | O   | Common output. COM0–COM3 are used for LCD backplanes.                                   |
| P5.2/COM1     | 46     | 40      | I/O | General-purpose digital I/O / common output. COM0–COM3 are used for LCD backplanes.     |
| P5.3/COM2     | 47     | 41      | I/O | General-purpose digital I/O / common output. COM0–COM3 are used for LCD backplanes.     |
| P5.4/COM3     | 48     | 42      | I/O | General-purpose digital I/O / common output. COM0–COM3 are used for LCD backplanes.     |
| QFN Pad       | NA     | None    | NA  | QFN package pad connection to $DV_{SS}$ is recommended.                                 |



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## short-form description

### CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

|                          |           |
|--------------------------|-----------|
| Program Counter          | PC/R0     |
| Stack Pointer            | SP/R1     |
| Status Register          | SR/CG1/R2 |
| Constant Generator       | CG2/R3    |
| General-Purpose Register | R4        |
| General-Purpose Register | R5        |
| General-Purpose Register | R6        |
| General-Purpose Register | R7        |
| General-Purpose Register | R8        |
| General-Purpose Register | R9        |
| General-Purpose Register | R10       |
| General-Purpose Register | R11       |
| General-Purpose Register | R12       |
| General-Purpose Register | R13       |
| General-Purpose Register | R14       |
| General-Purpose Register | R15       |

### instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats. Table 2 lists the address modes.

**Table 1. Instruction Word Formats**

|                                   |                 |                       |
|-----------------------------------|-----------------|-----------------------|
| Dual operands, source-destination | e.g., ADD R4,R5 | R4 + R5 ----> R5      |
| Single operands, destination only | e.g., CALL R8   | PC -->(TOS), R8--> PC |
| Relative jump, un/conditional     | e.g., JNE       | Jump-on-equal bit = 0 |

**Table 2. Address Mode Descriptions**

| ADDRESS MODE           | S | D | SYNTAX             | EXAMPLE          | OPERATION                         |
|------------------------|---|---|--------------------|------------------|-----------------------------------|
| Register               | ● | ● | MOV Rs,Rd          | MOV R10,R11      | R10 --> R11                       |
| Indexed                | ● | ● | MOV X(Rn),Y(Rm)    | MOV 2(R5),6(R6)  | M(2+R5)--> M(6+R6)                |
| Symbolic (PC relative) | ● | ● | MOV EDE,TONI       |                  | M(EDE) --> M(TONI)                |
| Absolute               | ● | ● | MOV & MEM, & TCDAT |                  | M(MEM) --> M(TCDAT)               |
| Indirect               | ● |   | MOV @Rn,Y(Rm)      | MOV @R10,Tab(R6) | M(R10) --> M(Tab+R6)              |
| Indirect autoincrement | ● |   | MOV @Rn+,Rm        | MOV @R10+,R11    | M(R10) --> R11<br>R10 + 2 --> R10 |
| Immediate              | ● |   | MOV #X,TONI        | MOV #45,TONI     | #45 --> M(TONI)                   |

NOTE: S = source    D = destination

# MSP430FG42x0

## MIXED SIGNAL MICROCONTROLLER

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### operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled  
ACLK and SMCLK remain active, MCLK is available to modules  
FLL+ loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled  
ACLK and SMCLK remain active, MCLK is available to modules  
FLL+ loop control is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled  
MCLK, FLL+ loop control, and DCOCLK are disabled  
DCO's dc-generator remains enabled  
ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled  
MCLK, FLL+ loop control, and DCOCLK are disabled  
DCO's dc-generator is disabled  
ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled  
ACLK is disabled  
MCLK, FLL+ loop control, and DCOCLK are disabled  
DCO's dc-generator is disabled  
Crystal oscillator is stopped



**interrupt vector addresses**

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Table 3. Interrupt Sources, Flags, and Vectors of MSP430FG42x0 Configuration**

| INTERRUPT SOURCE   | INTERRUPT FLAG   | SYSTEM INTERRUPT                                | WORD ADDRESS | PRIORITY    |
|--|--|---|--------------|-------------|
| Power-Up<br>External Reset<br>Watchdog<br>Flash Memory<br>PC Out-of-Range (see Note 4) | WDTIFG<br>KEYV<br>(see Note 1)   | Reset   | 0FFFEh       | 15, highest |
| NMI<br>Oscillator Fault<br>Flash Memory Access Violation                               | NMIIFG (see Notes 1 and 3)<br>OFIFG (see Notes 1 and 3)<br>ACCVIFG (see Notes 1 and 3) | (Non)maskable<br>(Non)maskable<br>(Non)maskable | 0FFFCh       | 14          |
|  |  |   | 0FFFAh       | 13          |
| SD16_A   | SD16CCTLx SD16OVIFG,<br>SD16CCTLx SD16IFG<br>(see Notes 1 and 2)                       | Maskable  | 0FFF8h       | 12          |
|  |  |   | 0FFF6h       | 11          |
| Watchdog Timer   | WDTIFG   | Maskable  | 0FFF4h       | 10          |
|  |  |   | 0FFF2h       | 9           |
|  |  |   | 0FFF0h       | 8           |
|  |  |   | 0FFEEh       | 7           |
| Timer_A3   | TACCR0 CCIFG0 (see Note 2)   | Maskable  | 0FFECCh      | 6           |
| Timer_A3   | TACCR1 CCIFG1 and TACCR2 CCIFG2,<br>TAIFG (see Notes 1 and 2)                          | Maskable  | 0FFEAh       | 5           |
| I/O Port P1 (Eight Flags)  | P1IFG.0 to P1IFG.7 (see Notes 1 and 2)   | Maskable  | 0FFE8h       | 4           |
| DAC12  | DAC12_0IFG<br>(see Note 2)   | Maskable  | 0FFE6h       | 3           |
|  |  |   | 0FFE4h       | 2           |
| I/O Port P2 (Eight Flags)  | P2IFG.0 to P2IFG.7 (see Notes 1 and 2)   | Maskable  | 0FFE2h       | 1           |
| Basic Timer1   | BTIFG  | Maskable  | 0FFE0h       | 0, lowest   |

- NOTES:
1. Multiple source flags
  2. Interrupt flags are located in the module.
  3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
  4. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h–01FFh) or from within unused address ranges (MSP430FG4270, MSP430FG4260: from 0300h to 0BFFh and from 01100h to 07FFFh, MSP430FG4250: from 0300h to 0BFFh and from 01100h to 0BFFFh).

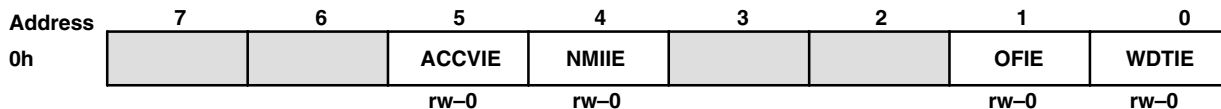
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## special function registers (SFRs)

The MSP430 SFRs are located in the lowest address space and are organized as byte-mode registers. SFRs should be accessed with byte instructions.

### interrupt enable registers 1 and 2

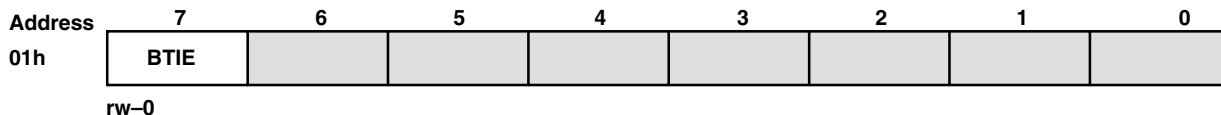


WDTIE: Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as a general-purpose timer.

OFIE: Oscillator-fault-interrupt enable

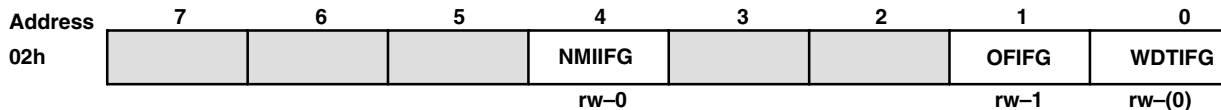
NMIIE: Nonmaskable-interrupt enable

ACCVIE: Flash access violation interrupt enable



BTIE: Basic timer interrupt enable

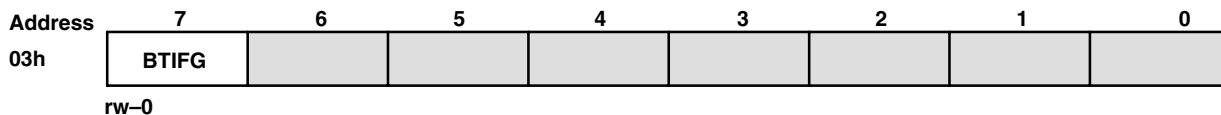
### interrupt flag registers 1 and 2



WDTIFG: Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on  $V_{CC}$  power-on or a reset condition at the  $\overline{RST}/NMI$  pin in reset mode.

OFIFG: Flag set on oscillator fault

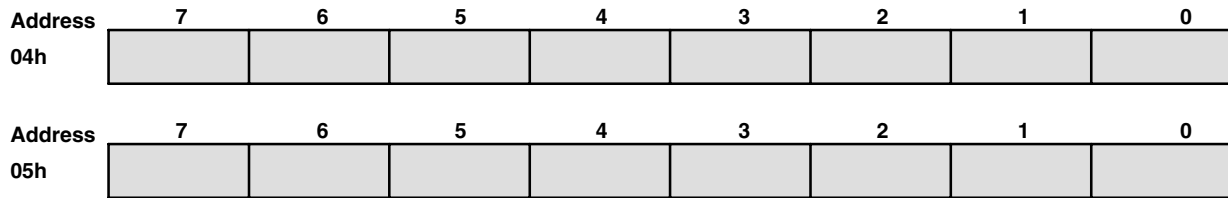
NMIIFG: Set via  $\overline{RST}/NMI$  pin



BTIFG: Basic timer flag



**module enable registers 1 and 2**



**Legend:** rw: Bit Can Be Read and Written  
 rw-0,1: Bit Can Be Read and Written. It Is Reset or Set by PUC.  
 rw-(0,1): Bit Can Be Read and Written. It Is Reset or Set by POR.  
 [Shaded Box] SFR Bit Not Present in Device

**memory organization**

|                        |           | MSP430FG4250    | MSP430FG4260    | MSP430FG4270    |
|------------------------|-----------|-----------------|-----------------|-----------------|
| Memory                 | Size      | 16KB            | 24KB            | 32KB            |
|                        | Flash     | 0FFFFh – 0FFE0h | 0FFFFh – 0FFE0h | 0FFFFh – 0FFE0h |
| Main: interrupt vector | Flash     | 0FFFFh – 0C000h | 0FFFFh – 0A000h | 0FFFFh – 08000h |
| Main: code memory      | Size      | 256 Byte        | 256 Byte        | 256 Byte        |
|                        | Flash     | 010FFh – 01000h | 010FFh – 01000h | 010FFh – 01000h |
| Information memory     | Size      | 1KB             | 1KB             | 1KB             |
| Boot memory            | ROM       | 0FFFh – 0C00h   | 0FFFh – 0C00h   | 0FFFh – 0C00h   |
|                        | Size      | 256 Byte        | 256 Byte        | 256 Byte        |
| RAM                    | Flash     | 02FFh – 0200h   | 02FFh – 0200h   | 02FFh – 0200h   |
| Peripherals            | 16-bit    | 01FFh – 0100h   | 01FFh – 0100h   | 01FFh – 0100h   |
|                        | 8-bit     | 0FFh – 010h     | 0FFh – 010h     | 0FFh – 010h     |
|                        | 8-bit SFR | 0Fh – 00h       | 0Fh – 00h       | 0Fh – 00h       |

**bootstrap loader (BSL)**

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the application report *Features of the MSP430 Bootstrap Loader*, literature number SLAA089.

| BSL Function  | DL Package Pins | RGZ Package Pins |
|---------------|-----------------|------------------|
| Data Transmit | 28 - P1.0       | 22 - P1.0        |
| Data Receive  | 27 - P1.1       | 21 - P1.1        |

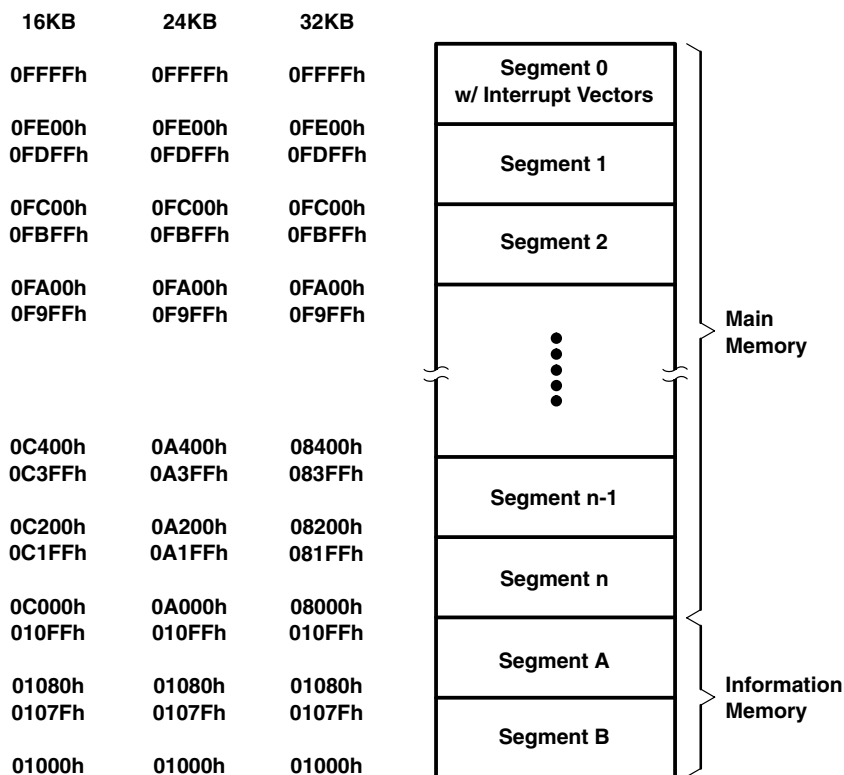
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## flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0 to n. Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



## peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x4xx Family User's Guide*, literature number SLAU056.

## oscillator and system clock

The clock system in the MSP430FG42x0 family of devices is supported by the FLL+ module, which includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high-frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low-power consumption. The FLL+ features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6  $\mu$ s. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8

## brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The CPU begins code execution after the brownout circuit releases the device reset. However,  $V_{CC}$  may not have ramped to  $V_{CC(min)}$  at that time. The user must ensure the default FLL+ settings are not changed until  $V_{CC}$  reaches  $V_{CC(min)}$ .

## digital I/O

There are four 8-bit I/O ports implemented—ports P1, P2, P5, and P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

## Basic Timer1

Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Basic Timer1 can be used to generate periodic interrupts.

## LCD driver with regulated charge pump

The LCD\_A driver generates the segment and common signals required to drive an LCD display. The LCD\_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage via an integrated charge pump. Furthermore, it is possible to control the level of the LCD voltage and thus contrast in software.

## watchdog timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

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### Timer\_A3

Timer\_A3 is a 16-bit timer/counter with three capture/compare registers. Timer\_A3 can support multiple capture/comparisons, PWM outputs, and interval timing. Timer\_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| Timer_A3 Signal Connections |           |                           |                   |              |                      |                   |           |
|-----------------------------|-----------|---------------------------|-------------------|--------------|----------------------|-------------------|-----------|
| Input Pin Number            |           | Device Input Signal       | Module Input Name | Module Block | Module Output Signal | Output Pin Number |           |
| DL                          | RGZ       |                           |                   |              |                      | DL                | RGZ       |
| 23 - P1.5                   | 17 - P1.5 | TACLK                     | TACLK             | Timer        | NA                   |                   |           |
|                             |           | ACLK                      | ACLK              |              |                      |                   |           |
|                             |           | SMCLK                     | SMCLK             |              |                      |                   |           |
| 23 - P1.5                   | 17 - P1.5 | $\overline{\text{TACLK}}$ | INCLK             |              |                      |                   |           |
| 28 - P1.0                   | 22 - P1.0 | TA0                       | CCI0A             | CCR0         | TA0                  | 28 - P1.0         | 22 - P1.0 |
| 27 - P1.1                   | 21 - P1.1 | TA0                       | CCI0B             |              |                      |                   |           |
|                             |           | DV <sub>SS</sub>          | GND               |              |                      |                   |           |
|                             |           | DV <sub>CC</sub>          | V <sub>CC</sub>   |              |                      |                   |           |
| 26 - P1.2                   | 20 - P1.2 | TA1                       | CCI1A             | CCR1         | TA1                  | 26 - P1.2         | 20 - P1.2 |
| 26 - P1.2                   | 20 - P1.2 | TA1                       | CCI1B             |              |                      |                   |           |
|                             |           | DV <sub>SS</sub>          | GND               |              |                      |                   |           |
|                             |           | DV <sub>CC</sub>          | V <sub>CC</sub>   |              |                      |                   |           |
| 25 - P1.3                   | 19 - P1.3 | TA2                       | CCI2A             | CCR2         | TA2                  | 25 - P1.3         | 19 - P1.3 |
|                             |           | ACLK (internal)           | CCI2B             |              |                      |                   |           |
|                             |           | DV <sub>SS</sub>          | GND               |              |                      |                   |           |
|                             |           | DV <sub>CC</sub>          | V <sub>CC</sub>   |              |                      |                   |           |

### SD16\_A

The SD16\_A module supports 16-bit analog-to-digital conversions. The module implements a 16-bit sigma-delta core and reference generator. In addition to external analog inputs, an internal V<sub>CC</sub> sense and temperature sensor are also available.

### DAC12

The DAC12 module is a 12-bit, R-ladder, voltage output DAC. The DAC12 may be used in 8- or 12-bit mode.



**operational amplifier (OA)**

The MSP430FG42x0 has two configurable low-current general-purpose operational amplifiers. Each OA input and output terminal is software-selectable and offers a flexible choice of connections for various applications. The OAs primarily support front-end analog signal conditioning prior to analog-to-digital conversion.

| OA Signal Connections |           |                     |                   |              |                      |                   |          |
|-----------------------|-----------|---------------------|-------------------|--------------|----------------------|-------------------|----------|
| Input Pin Number      |           | Device Input Signal | Module Input Name | Module Block | Module Output Signal | Output Pin Number |          |
| DL                    | RGZ       |                     |                   |              |                      | DL                | RGZ      |
| 22 - P1.6             | 16 - P1.6 | OA0I0               | OA0I0             | OA0          | OA0O                 | 13 - P6.0         | 7 - P6.0 |
| 17 - P6.4             | 11 - P6.4 | OA0I1               | OA0I1             |              |                      |                   |          |
| 18 - P6.5             | 12 - P6.5 | OA0I2               | OA0I2             |              |                      |                   |          |
| 14 - P6.1             | 8 - P6.1  | OA0FB               | OA0FB             |              |                      |                   |          |
| 24 - P1.4             | 18 - P1.4 | OA1I0               | OA1I0             | OA1          | OA1O                 | 15 - P6.0         | 9 - P6.0 |
| 19 - P6.6             | 13 - P6.6 | OA1I1               | OA1I1             |              |                      |                   |          |
| 20 - P6.7             | 14 - P6.7 | OA1I2               | OA1I2             |              |                      |                   |          |
| 16 - P6.1             | 10 - P6.1 | OA1FB               | OA1FB             |              |                      |                   |          |

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## peripheral file map

| PERIPHERALS WITH WORD ACCESS                                    |  |            |       |
|---|--|------------|-------|
| <b>Watchdog</b>   | Watchdog timer control                     | WDTCTL     | 0120h |
| <b>Timer_A3</b>   | Capture/compare register 2                 | TACCR2     | 0176h |
|   | Capture/compare register 1                 | TACCR1     | 0174h |
|   | Capture/compare register 0                 | TACCR0     | 0172h |
|   | Timer_A register                           | TAR        | 0170h |
|   | Capture/compare control 2                  | TACCTL2    | 0166h |
|   | Capture/compare control 1                  | TACCTL1    | 0164h |
|   | Capture/compare control 0                  | TACCTL0    | 0162h |
|   | Timer_A control                            | TACTL      | 0160h |
|   | Timer_A interrupt vector                   | TAIV       | 012Eh |
| <b>Flash</b>  | Flash control 3                            | FCTL3      | 012Ch |
|   | Flash control 2                            | FCTL2      | 012Ah |
|   | Flash control 1                            | FCTL1      | 0128h |
| <b>DAC12</b>  | DAC12_0 data                               | DAC12_0DAT | 01C8h |
|   | DAC12_0 control                            | DAC12_0CTL | 01C0h |
| <b>SD16_A</b><br>(see also<br>Peripherals With<br>Byte Access)  | General control                            | SD16CTL    | 0100h |
|   | Channel 0 control                          | SD16CCTL0  | 0102h |
|   | Interrupt vector word register             | SD16IV     | 0110h |
|   | Channel 0 conversion memory                | SD16MEM0   | 0112h |
| PERIPHERALS WITH BYTE ACCESS                                    |  |            |       |
| <b>OA/GND Switches</b>  | Switch control register                    | SWCTL      | 0CFh  |
| <b>OA1</b>  | Operational amplifier 1 control register 1 | OA1CTL1    | 0C3h  |
|   | Operational amplifier 1 control register 0 | OA1CTL0    | 0C2h  |
| <b>OA0</b>  | Operational amplifier 0 control register 1 | OA0CTL1    | 0C1h  |
|   | Operational amplifier 0 control register 0 | OA0CTL0    | 0C0h  |
| <b>SD16_A</b><br>(see also:<br>Peripherals with<br>Word Access) | Channel 0 input control                    | SD16INCTL0 | 0B0h  |
|   | Analog enable                              | SD16AE     | 0B7h  |
| <b>LCD_A</b>  | LCD voltage control 1                      | LCDVAVCTL1 | 0AFh  |
|   | LCD voltage control 0                      | LCDVAVCTL0 | 0AEh  |
|   | LCD voltage port control 1                 | LCDVAPCTL1 | 0ADh  |
|   | LCD voltage port control 0                 | LCDVAPCTL0 | 0ACh  |
|   | LCD memory 20                              | LCDM20     | 0A4h  |
|   | :  | :          | :     |
|   | LCD memory 16                              | LCDM16     | 0A0h  |
|   | LCD memory 15                              | LCDM15     | 09Fh  |
|   | :  | :          | :     |
|   | LCD memory 1                               | LCDM1      | 091h  |
|   | LCD control and mode                       | LCDACTL    | 090h  |



**peripheral file map (continued)**

| <b>PERIPHERALS WITH BYTE ACCESS (CONTINUED)</b> |                                   |                   |       |
|---|-----------------------------------|-------------------|-------|
| <b>FLL+ Clock</b>                               | FLL+ Control 1                    | FLL_CTL1          | 054h  |
|   | FLL+ Control 0                    | FLL_CTL0          | 053h  |
|   | System clock frequency control    | SCFQCTL           | 052h  |
|   | System clock frequency integrator | SCFI1             | 051h  |
|   | System clock frequency integrator | SCFI0             | 050h  |
| <b>Basic Timer1</b>                             | BT counter 2                      | BTCNT2            | 047h  |
|   | BT counter 1                      | BTCNT1            | 046h  |
|   | BT control                        | BTCTL             | 040h  |
| <b>Port P6</b>                                  | Port P6 selection                 | P6SEL             | 037h  |
|   | Port P6 direction                 | P6DIR             | 036h  |
|   | Port P6 output                    | P6OUT             | 035h  |
|   | Port P6 input                     | P6IN              | 034h  |
| <b>Port P5</b>                                  | Port P5 selection                 | P5SEL             | 033h  |
|   | Port P5 direction                 | P5DIR             | 032h  |
|   | Port P5 output                    | P5OUT             | 031h  |
|   | Port P5 input                     | P5IN              | 030h  |
| <b>Port P2</b>                                  | Port P2 selection                 | P2SEL             | 02Eh  |
|   | Port P2 interrupt enable          | P2IE              | 02Dh  |
|   | Port P2 interrupt-edge select     | P2IES             | 02Ch  |
|   | Port P2 interrupt flag            | P2IFG             | 02Bh  |
|   | Port P2 direction                 | P2DIR             | 02Ah  |
|   | Port P2 output                    | P2OUT             | 029h  |
|   | Port P2 input                     | P2IN              | 028h  |
|   | <b>Port P1</b>                    | Port P1 selection | P1SEL |
| Port P1 interrupt enable                        |                                   | P1IE              | 025h  |
| Port P1 interrupt-edge select                   |                                   | P1IES             | 024h  |
| Port P1 interrupt flag                          |                                   | P1IFG             | 023h  |
| Port P1 direction                               |                                   | P1DIR             | 022h  |
| Port P1 output                                  |                                   | P1OUT             | 021h  |
| Port P1 input                                   |                                   | P1IN              | 020h  |
| <b>Special functions</b>                        | SFR module enable 2               | ME2               | 005h  |
|   | SFR module enable 1               | ME1               | 004h  |
|   | SFR interrupt flag 2              | IFG2              | 003h  |
|   | SFR interrupt flag 1              | IFG1              | 002h  |
|   | SFR interrupt enable 2            | IE2               | 001h  |
|   | SFR interrupt enable 1            | IE1               | 000h  |



**electrical characteristics over recommended operating free-air temperature (unless otherwise noted)**

**supply current into AV<sub>CC</sub> + DV<sub>CC</sub> excluding external current**

| PARAMETER           |  | TEST CONDITIONS   |                         | MIN | NOM | MAX | UNIT |
|---------------------|--|---|-------------------------|-----|-----|-----|------|
| I <sub>(AM)</sub>   | Active mode (see Note 1),<br>f <sub>(MCLK)</sub> = f <sub>(SMCLK)</sub> = 1 MHz,<br>f <sub>(ACLK)</sub> = 32,768 Hz<br>XTS=0, SELM=(0,1)   | T <sub>A</sub> = -40°C to 85°C  | V <sub>CC</sub> = 2.2 V | 250 | 370 | μA  |      |
|                     |  |   | V <sub>CC</sub> = 3 V   | 400 | 520 |     |      |
| I <sub>(LPM0)</sub> | Low-power mode (LPM0)<br>(see Note 1 and Note 4)   | T <sub>A</sub> = -40°C to 85°C  | V <sub>CC</sub> = 2.2 V | 55  | 70  | μA  |      |
|                     |  |   | V <sub>CC</sub> = 3 V   | 95  | 110 |     |      |
| I <sub>(LPM2)</sub> | Low-power mode (LPM2),<br>f <sub>(MCLK)</sub> = f <sub>(SMCLK)</sub> = 0 MHz,<br>f <sub>(ACLK)</sub> = 32,768 Hz, SCG0 = 0<br>(see Note 2 and Note 4)  | T <sub>A</sub> = -40°C to 85°C  | V <sub>CC</sub> = 2.2 V | 11  | 14  | μA  |      |
|                     |  |   | V <sub>CC</sub> = 3 V   | 17  | 22  |     |      |
| I <sub>(LPM3)</sub> | Low-power mode (LPM3),<br>f <sub>(MCLK)</sub> = f <sub>(SMCLK)</sub> = 0 MHz,<br>f <sub>(ACLK)</sub> = 32,768 Hz, SCG0 = 1<br>Basic Timer1 enabled, ACLK selected<br>LCD_A enabled, LCDPEN = 0<br>(static mode, f <sub>LCD</sub> = f <sub>(ACLK)/32),<br/>(see Note 2, Note 3, and Note 4)</sub> | T <sub>A</sub> = -40°C<br>T <sub>A</sub> = 25°C<br>T <sub>A</sub> = 60°C<br>T <sub>A</sub> = 85°C | V <sub>CC</sub> = 2.2 V | 1.0 | 2.0 | μA  |      |
|                     |  |   |                         | 1.1 | 2.0 |     |      |
|                     |  |   |                         | 2.0 | 3.0 |     |      |
|                     |  |   |                         | 3.5 | 6.0 |     |      |
|                     |  | T <sub>A</sub> = -40°C<br>T <sub>A</sub> = 25°C<br>T <sub>A</sub> = 60°C<br>T <sub>A</sub> = 85°C | V <sub>CC</sub> = 3 V   | 1.8 | 2.8 |     |      |
|                     |  |   |                         | 1.6 | 2.7 |     |      |
|                     |  |   |                         | 2.5 | 3.5 |     |      |
|                     |  |   |                         | 4.2 | 7.5 |     |      |
| I <sub>(LPM3)</sub> | Low-power mode (LPM3),<br>f <sub>(MCLK)</sub> = f <sub>(SMCLK)</sub> = 0 MHz,<br>f <sub>(ACLK)</sub> = 32,768 Hz, SCG0 = 1<br>Basic Timer1 enabled, ACLK selected<br>LCD_A enabled, LCDPEN = 0<br>(4-mux mode, f <sub>LCD</sub> = f <sub>(ACLK)/32),<br/>(see Note 2, Note 3, and Note 4)</sub>  | T <sub>A</sub> = -40°C<br>T <sub>A</sub> = 25°C<br>T <sub>A</sub> = 85°C                          | V <sub>CC</sub> = 2.2 V | 2.5 | 3.5 | μA  |      |
|                     |  |   |                         | 2.5 | 3.5 |     |      |
|                     |  |   |                         | 3.8 | 6.0 |     |      |
|                     |  | T <sub>A</sub> = -40°C<br>T <sub>A</sub> = 25°C<br>T <sub>A</sub> = 85°C                          | V <sub>CC</sub> = 3 V   | 2.9 | 4.0 |     |      |
|                     |  |   |                         | 2.9 | 4.0 |     |      |
|                     |  |   |                         | 4.4 | 7.5 |     |      |
| I <sub>(LPM4)</sub> | Low-power mode (LPM4),<br>f <sub>(MCLK)</sub> = 0 MHz, f <sub>(SMCLK)</sub> = 0 MHz,<br>f <sub>(ACLK)</sub> = 0 Hz, SCG0 = 1<br>(see Note 2 and Note 4)  | T <sub>A</sub> = -40°C<br>T <sub>A</sub> = 25°C<br>T <sub>A</sub> = 60°C<br>T <sub>A</sub> = 85°C | V <sub>CC</sub> = 2.2 V | 0.1 | 0.5 | μA  |      |
|                     |  |   |                         | 0.1 | 0.5 |     |      |
|                     |  |   |                         | 0.7 | 1.1 |     |      |
|                     |  |   |                         | 1.7 | 3.0 |     |      |
|                     |  | T <sub>A</sub> = -40°C<br>T <sub>A</sub> = 25°C<br>T <sub>A</sub> = 60°C<br>T <sub>A</sub> = 85°C | V <sub>CC</sub> = 3 V   | 0.1 | 0.8 |     |      |
|                     |  |   |                         | 0.1 | 0.8 |     |      |
|                     |  |   |                         | 0.8 | 1.2 |     |      |
|                     |  |   |                         | 1.9 | 3.5 |     |      |

- NOTES: 1. Timer\_A is clocked by f<sub>(DCOCLK)</sub> = f<sub>(DCO)</sub> = 1 MHz. All inputs are tied to 0 V or to V<sub>CC</sub>. Outputs do not source or sink any current.  
 2. All inputs are tied to 0 V or to V<sub>CC</sub>. Outputs do not source or sink any current.  
 3. The LPM3 currents are characterized with a Micro Crystal CC4V-T1A (9 pF) crystal and OSCCAPx = 01h.  
 4. Current for brownout included.

**current consumption of active mode versus system frequency**

$$I_{(AM)} = I_{(AM)} [1 \text{ MHz}] \times f_{(\text{System})} [\text{MHz}]$$

**current consumption of active mode versus supply voltage**

$$I_{(AM)} = I_{(AM)} [3 \text{ V}] + 175 \mu\text{A/V} \times (V_{CC} - 3 \text{ V})$$

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### Schmitt-trigger inputs – Ports P1, P2, P5, and P6; $\overline{RST}/NMI$ ; JTAG: TCK, TMS, TDI/TCLK, TDO/TDI

| PARAMETER |  | TEST CONDITIONS         | MIN | TYP | MAX  | UNIT |
|-----------|--|-------------------------|-----|-----|------|------|
| $V_{IT+}$ | Positive-going input threshold voltage           | $V_{CC} = 2.2\text{ V}$ | 1.1 |     | 1.55 | V    |
|           |  | $V_{CC} = 3\text{ V}$   | 1.5 |     | 1.98 |      |
| $V_{IT-}$ | Negative-going input threshold voltage           | $V_{CC} = 2.2\text{ V}$ | 0.4 |     | 0.9  | V    |
|           |  | $V_{CC} = 3\text{ V}$   | 0.9 |     | 1.3  |      |
| $V_{hys}$ | Input voltage hysteresis ( $V_{IT+} - V_{IT-}$ ) | $V_{CC} = 2.2\text{ V}$ | 0.3 |     | 1.1  | V    |
|           |  | $V_{CC} = 3\text{ V}$   | 0.5 |     | 1    |      |

### inputs Px.x, TA<sub>x</sub>

| PARAMETER     |   | TEST CONDITIONS   | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---------------|---|---|----------|-----|-----|-----|------|
| $t_{(int)}$   | External interrupt timing                         | Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag, (see Note 1) | 2.2 V    | 62  |     |     | ns   |
|               |   |   | 3 V      | 50  |     |     |      |
| $t_{(cap)}$   | Timer_A capture timing                            | TA0, TA1, TA2   | 2.2 V    | 62  |     |     | ns   |
|               |   |   | 3 V      | 50  |     |     |      |
| $f_{(TAext)}$ | Timer_A clock frequency externally applied to pin | TACLK, INCLK: $t_{(H)} = t_{(L)}$   | 2.2 V    |     |     | 8   | MHz  |
|               |   |   | 3 V      |     |     | 10  |      |
| $f_{(TAint)}$ | Timer_A clock frequency                           | SMCLK or ACLK signal selected   | 2.2 V    |     |     | 8   | MHz  |
|               |   |   | 3 V      |     |     | 10  |      |

NOTES: 1. The external signal sets the interrupt flag every time the minimum  $t_{(int)}$  parameters are met. It may be set even with trigger signals shorter than  $t_{(int)}$ .

### leakage current – ports P1, P2, P5, and P6 (see Note 1)

| PARAMETER       |                 | TEST CONDITIONS |                           | MIN                                | TYP | MAX | UNIT |
|-----------------|-----------------|-----------------|---------------------------|------------------------------------|-----|-----|------|
| $I_{lkg(Px.y)}$ | Leakage current | Port Px         | $V_{(Px.y)}$ (see Note 2) | $V_{CC} = 2.2\text{ V}/3\text{ V}$ |     | ±50 | nA   |

NOTES: 1. The leakage current is measured with  $V_{SS}$  or  $V_{CC}$  applied to the corresponding pin(s), unless otherwise noted.  
2. The port pin must be selected as input.



**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**outputs – ports P1, P2, P5, and P6**

| PARAMETER       |                           | TEST CONDITIONS   |                       |  | MIN                   | TYP | MAX | UNIT |
|-----------------|---------------------------|---|-----------------------|--|-----------------------|-----|-----|------|
| V <sub>OH</sub> | High-level output voltage | I <sub>OH(max)</sub> = -1.5 mA, V <sub>CC</sub> = 2.2 V, See Note 1 | V <sub>CC</sub> -0.25 |  | V <sub>CC</sub>       |     | V   |      |
|                 |                           | I <sub>OH(max)</sub> = -6 mA, V <sub>CC</sub> = 2.2 V, See Note 2   | V <sub>CC</sub> -0.6  |  | V <sub>CC</sub>       |     |     |      |
|                 |                           | I <sub>OH(max)</sub> = -1.5 mA, V <sub>CC</sub> = 3 V, See Note 1   | V <sub>CC</sub> -0.25 |  | V <sub>CC</sub>       |     |     |      |
|                 |                           | I <sub>OH(max)</sub> = -6 mA, V <sub>CC</sub> = 3 V, See Note 2     | V <sub>CC</sub> -0.6  |  | V <sub>CC</sub>       |     |     |      |
| V <sub>OL</sub> | Low-level output voltage  | I <sub>OL(max)</sub> = 1.5 mA, V <sub>CC</sub> = 2.2 V, See Note 1  | V <sub>SS</sub>       |  | V <sub>SS</sub> +0.25 |     | V   |      |
|                 |                           | I <sub>OL(max)</sub> = 6 mA, V <sub>CC</sub> = 2.2 V, See Note 2    | V <sub>SS</sub>       |  | V <sub>SS</sub> +0.6  |     |     |      |
|                 |                           | I <sub>OL(max)</sub> = 1.5 mA, V <sub>CC</sub> = 3 V, See Note 1    | V <sub>SS</sub>       |  | V <sub>SS</sub> +0.25 |     |     |      |
|                 |                           | I <sub>OL(max)</sub> = 6 mA, V <sub>CC</sub> = 3 V, See Note 2      | V <sub>SS</sub>       |  | V <sub>SS</sub> +0.6  |     |     |      |

- NOTES: 1. The maximum total current, I<sub>OH(max)</sub> and I<sub>OL(max)</sub>, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.  
 2. The maximum total current, I<sub>OH(max)</sub> and I<sub>OL(max)</sub>, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

**output frequency**

| PARAMETER           |                                | TEST CONDITIONS  |   | MIN           | TYP | MAX                 | UNIT |
|---------------------|--------------------------------|--|---|---------------|-----|---------------------|------|
| f <sub>(Px.y)</sub> | (x = 1, 2, 5, 6, 0 ≤ y ≤ 7)    | C <sub>L</sub> = 20 pF,<br>I <sub>L</sub> = ±1.5 mA                        | V <sub>CC</sub> = 2.2 V / 3 V               | DC            |     | f <sub>System</sub> | MHz  |
| f <sub>(MCLK)</sub> | P1.1/TA0/MCLK                  | C <sub>L</sub> = 20 pF   |   |               |     | f <sub>System</sub> | MHz  |
| t <sub>(Xdc)</sub>  | Duty cycle of output frequency | P1.1/TA0/MCLK,<br>C <sub>L</sub> = 20 pF,<br>V <sub>CC</sub> = 2.2 V / 3 V | f <sub>(MCLK)</sub> = f <sub>(XT1)</sub>    | 40%           |     | 60%                 |      |
|                     |                                |  | f <sub>(MCLK)</sub> = f <sub>(DCOCLK)</sub> | 50%-<br>15 ns | 50% | 50%+<br>15 ns       |      |

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – ports P1, P2, P5, and P6 (continued)

TYPICAL LOW-LEVEL OUTPUT CURRENT  
vs  
LOW-LEVEL OUTPUT VOLTAGE

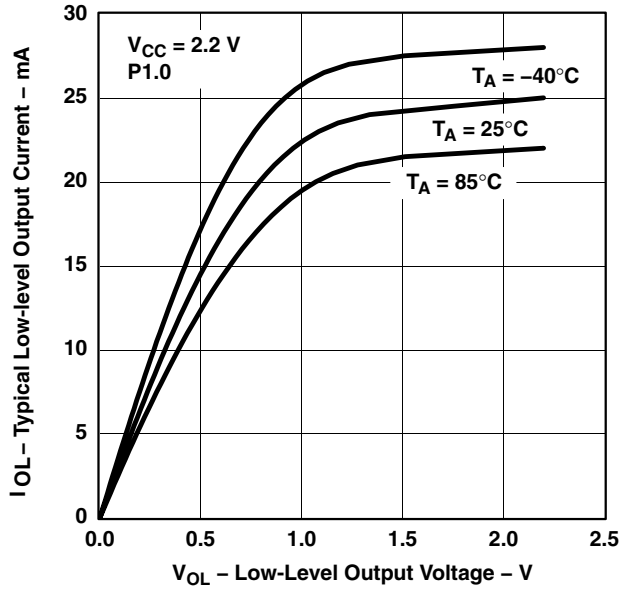


Figure 2

TYPICAL LOW-LEVEL OUTPUT CURRENT  
vs  
LOW-LEVEL OUTPUT VOLTAGE

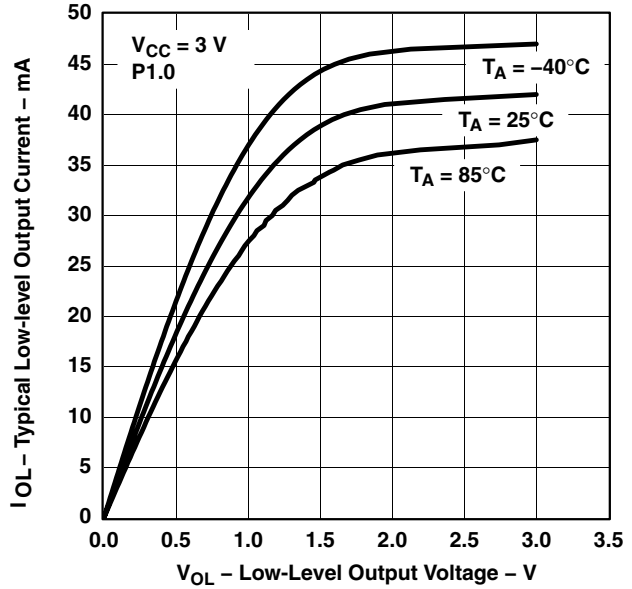


Figure 3

TYPICAL HIGH-LEVEL OUTPUT CURRENT  
vs  
HIGH-LEVEL OUTPUT VOLTAGE

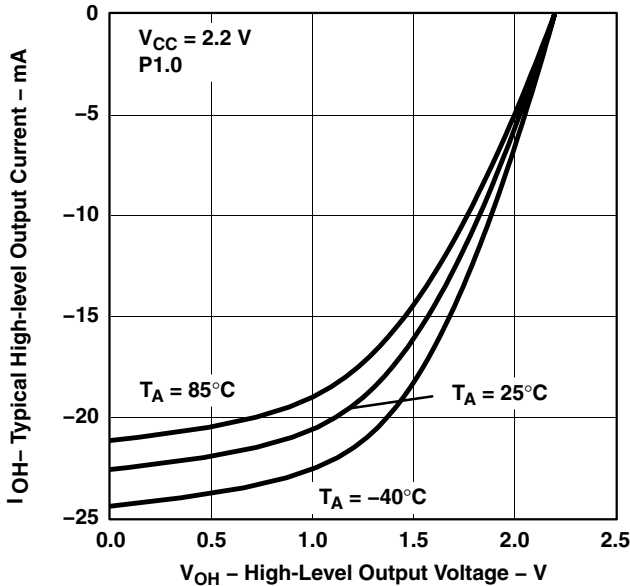


Figure 4

TYPICAL HIGH-LEVEL OUTPUT CURRENT  
vs  
HIGH-LEVEL OUTPUT VOLTAGE

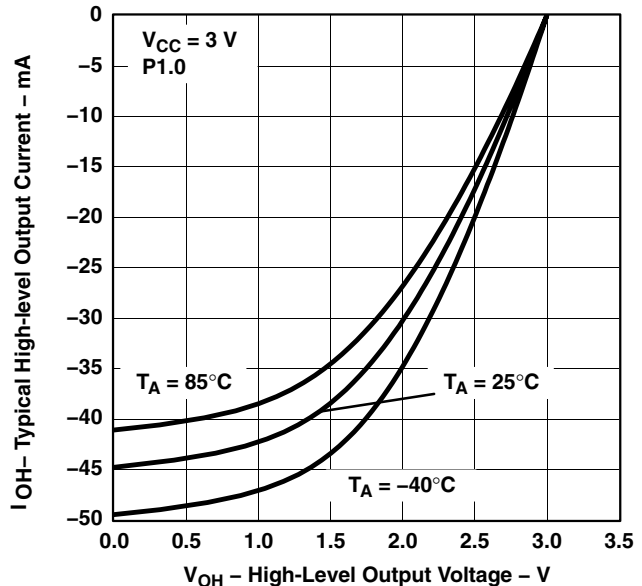


Figure 5



**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**wake-up LPM3**

| PARAMETER     |            | TEST CONDITIONS | MIN                                  | TYP | MAX | UNIT          |
|---------------|------------|-----------------|--------------------------------------|-----|-----|---------------|
| $t_{d(LPM3)}$ | Delay time | f = 1 MHz       |                                      |     | 6   | $\mu\text{s}$ |
|               |            | f = 2 MHz       | $V_{CC} = 2.2 \text{ V}/3 \text{ V}$ |     | 6   |               |
|               |            | f = 3 MHz       |                                      |     | 6   |               |

**RAM**

| PARAMETER  | TEST CONDITIONS         | MIN | TYP | MAX | UNIT |
|------------|-------------------------|-----|-----|-----|------|
| $V_{RAMh}$ | CPU halted (see Note 1) | 1.6 |     |     | V    |

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

**LCD\_A**

| PARAMETER     |                                     | TEST CONDITIONS   | VCC   | MIN  | TYP | MAX | UNIT          |
|---------------|-------------------------------------|---|-------|------|-----|-----|---------------|
| $V_{CC(LCD)}$ | Supply voltage                      | Charge pump enabled (LCDCPEN = 1, VLCDx > 0000)   |       | 2.2  |     | 3.6 | V             |
| $C_{LCD}$     | Capacitor on LCDCAP (see Note 1)    | Charge pump enabled (LCDCPEN = 1, VLCDx > 0000)   |       | 4.7  |     |     | $\mu\text{F}$ |
| $I_{CC(LCD)}$ | Average supply current (see Note 2) | $V_{LCD(typ)} = 3\text{V}$ , LCDCPEN = 1, VLCDx = 1000, all segments on<br>$f_{LCD} = f_{ACLK}/32$<br>no LCD connected (see Note 3)<br>$T_A = 25^\circ\text{C}$ | 2.2 V |      | 3.8 |     | $\mu\text{A}$ |
| $f_{LCD}$     | LCD frequency                       |   |       |      |     | 1.1 | kHz           |
| $V_{LCD}$     | LCD voltage                         | VLCDx = 0000  | 2.2 V |      | VCC |     | V             |
|               |                                     | VLCDx = 0001  |       | 2.60 |     |     |               |
|               |                                     | VLCDx = 0010  |       | 2.66 |     |     |               |
|               |                                     | VLCDx = 0011  |       | 2.72 |     |     |               |
|               |                                     | VLCDx = 0100  |       | 2.78 |     |     |               |
|               |                                     | VLCDx = 0101  |       | 2.84 |     |     |               |
|               |                                     | VLCDx = 0110  |       | 2.90 |     |     |               |
|               |                                     | VLCDx = 0111  |       | 2.96 |     |     |               |
|               |                                     | VLCDx = 1000  |       | 3.02 |     |     |               |
|               |                                     | VLCDx = 1001  |       | 3.08 |     |     |               |
|               |                                     | VLCDx = 1010  |       | 3.14 |     |     |               |
|               |                                     | VLCDx = 1011  |       | 3.20 |     |     |               |
|               |                                     | VLCDx = 1100  |       | 3.26 |     |     |               |
|               |                                     | VLCDx = 1101  |       | 3.32 |     |     |               |
| VLCDx = 1110  | 3.38                                |   |       |      |     |     |               |
| VLCDx = 1111  | 3.44                                | 3.60  |       |      |     |     |               |
| $R_{LCD}$     | LCD driver output impedance         | $V_{LCD} = 3\text{V}$ , LCDCPEN = 1, VLCDx = 1000, $I_{LOAD} = \pm 10 \mu\text{A}$  | 2.2 V |      |     | 10  | k $\Omega$    |

- NOTES: 1. Enabling the internal charge pump with an external capacitor smaller than the minimum specified might damage the device.  
2. Refer to the supply current specifications  $I_{LPM3}$  for additional current specifications with the LCD\_A module active.  
3. Connecting an actual display will increase the current consumption depending on the size of the LCD.

# MSP430FG42x0 MIXED SIGNAL MICROCONTROLLER

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

## POR/brownout reset (BOR) (see Note 1)

| PARAMETER         | TEST CONDITIONS  | MIN | TYP                       | MAX  | UNIT    |
|-------------------|--|-----|---------------------------|------|---------|
| $t_{d(BOR)}$      |  |     |                           | 2000 | $\mu s$ |
| $V_{CC(start)}$   | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 6)   |     | $0.7 \times V_{(B\_IT-)}$ |      | V       |
| $V_{(B\_IT-)}$    | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 6 through Figure 8)  |     |                           | 1.71 | V       |
| $V_{hys(B\_IT-)}$ | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 6)   | 70  | 130                       | 180  | mV      |
| $t_{(reset)}$     | Pulse length needed at $\overline{RST}/NMI$ pin to accepted reset internally, $V_{CC} = 2.2 \text{ V}/3 \text{ V}$ | 2   |                           |      | $\mu s$ |

- NOTES: 1. The current consumption of the brownout module is already included in the  $I_{CC}$  current consumption data. The voltage level  $V_{(B\_IT-)} + V_{hys(B\_IT-)}$  is  $\leq 1.8\text{V}$ .
2. During power up, the CPU begins code execution following a period of  $t_{d(BOR)}$  after  $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$ . The default FLL+ settings must not be changed until  $V_{CC} \geq V_{CC(min)}$ , where  $V_{CC(min)}$  is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout.

## typical characteristics

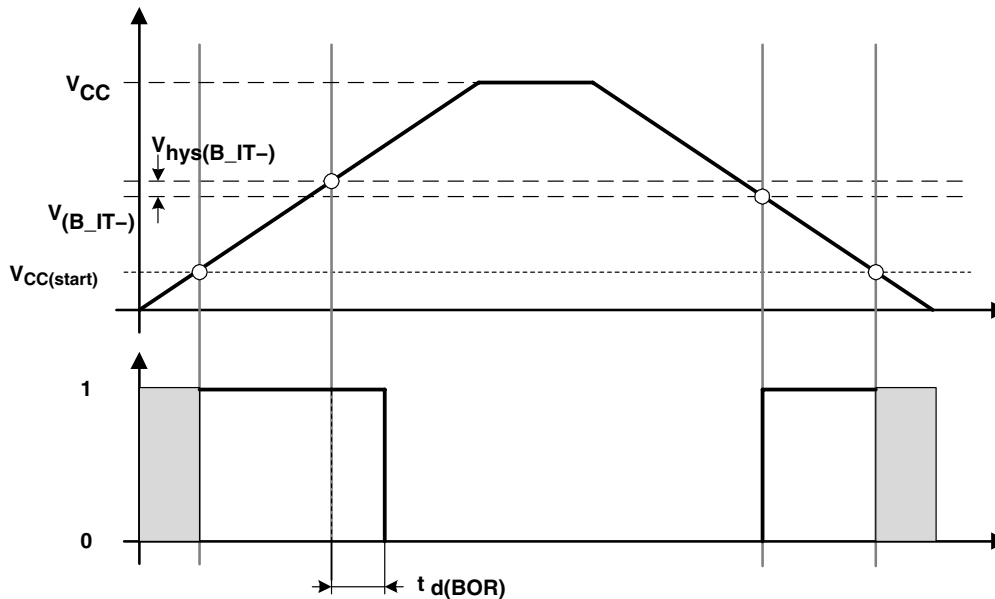


Figure 6. POR/Brownout Reset (BOR) vs Supply Voltage

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

typical characteristics (continued)

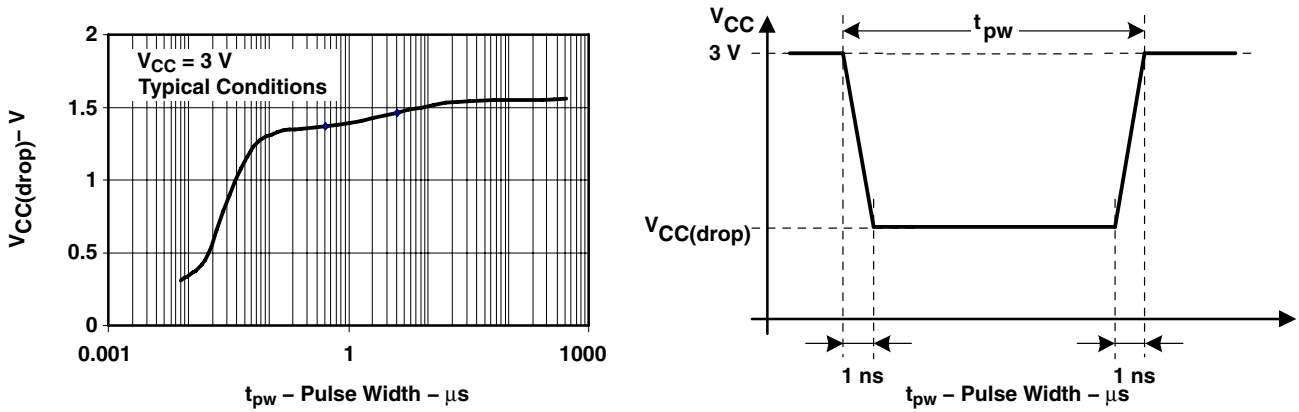


Figure 7.  $V_{CC(min)}$  Level With a Square Voltage Drop to Generate a POR/Brownout Signal

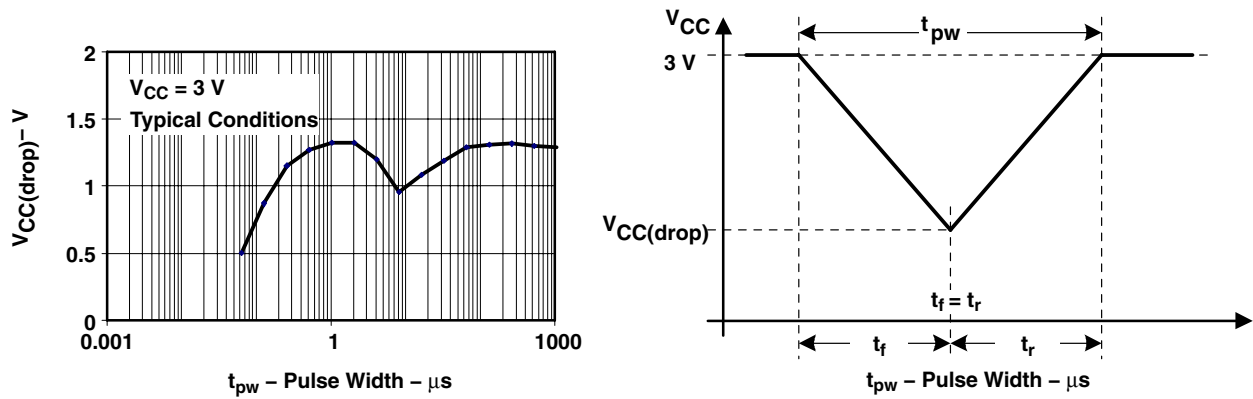


Figure 8.  $V_{CC(drop)}$  Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

## DCO

| PARAMETER             | TEST CONDITIONS  | V <sub>CC</sub> | MIN  | TYP  | MAX  | UNIT |
|-----------------------|--|-----------------|------|------|------|------|
| f <sub>(DCOCLK)</sub> | N <sub>(DCO)</sub> =01Eh, FN <sub>8</sub> =FN <sub>4</sub> =FN <sub>3</sub> =FN <sub>2</sub> =0, D = 2, DCOPLUS= 0, f <sub>Crystal</sub> = 32.768 kHz          | 2.2 V/3 V       |      | 1    |      | MHz  |
| f <sub>(DCO=2)</sub>  | FN <sub>8</sub> = FN <sub>4</sub> = FN <sub>3</sub> = FN <sub>2</sub> = 0, DCOPLUS = 1   | 2.2 V           | 0.3  | 0.65 | 1.25 | MHz  |
|                       |  | 3 V             | 0.3  | 0.7  | 1.3  |      |
| f <sub>(DCO=27)</sub> | FN <sub>8</sub> = FN <sub>4</sub> = FN <sub>3</sub> = FN <sub>2</sub> = 0, DCOPLUS = 1   | 2.2 V           | 2.5  | 5.6  | 10.5 | MHz  |
|                       |  | 3 V             | 2.7  | 6.1  | 11.3 |      |
| f <sub>(DCO=2)</sub>  | FN <sub>8</sub> = FN <sub>4</sub> = FN <sub>3</sub> = 0, FN <sub>2</sub> = 1, DCOPLUS = 1  | 2.2 V           | 0.7  | 1.3  | 2.3  | MHz  |
|                       |  | 3 V             | 0.8  | 1.5  | 2.5  |      |
| f <sub>(DCO=27)</sub> | FN <sub>8</sub> = FN <sub>4</sub> = FN <sub>3</sub> = 0, FN <sub>2</sub> = 1, DCOPLUS = 1  | 2.2 V           | 5.7  | 10.8 | 18   | MHz  |
|                       |  | 3 V             | 6.5  | 12.1 | 20   |      |
| f <sub>(DCO=2)</sub>  | FN <sub>8</sub> = FN <sub>4</sub> = 0, FN <sub>3</sub> = 1, FN <sub>2</sub> = x, DCOPLUS = 1   | 2.2 V           | 1.2  | 2    | 3    | MHz  |
|                       |  | 3 V             | 1.3  | 2.2  | 3.5  |      |
| f <sub>(DCO=27)</sub> | FN <sub>8</sub> = FN <sub>4</sub> = 0, FN <sub>3</sub> = 1, FN <sub>2</sub> = x, DCOPLUS = 1   | 2.2 V           | 9    | 15.5 | 25   | MHz  |
|                       |  | 3 V             | 10.3 | 17.9 | 28.5 |      |
| f <sub>(DCO=2)</sub>  | FN <sub>8</sub> = 0, FN <sub>4</sub> = 1, FN <sub>3</sub> = FN <sub>2</sub> = x, DCOPLUS = 1   | 2.2 V           | 1.8  | 2.8  | 4.2  | MHz  |
|                       |  | 3 V             | 2.1  | 3.4  | 5.2  |      |
| f <sub>(DCO=27)</sub> | FN <sub>8</sub> = 0, FN <sub>4</sub> = 1, FN <sub>3</sub> = FN <sub>2</sub> = x, DCOPLUS = 1   | 2.2 V           | 13.5 | 21.5 | 33   | MHz  |
|                       |  | 3 V             | 16   | 26.6 | 41   |      |
| f <sub>(DCO=2)</sub>  | FN <sub>8</sub> = 1, FN <sub>4</sub> = FN <sub>3</sub> = FN <sub>2</sub> = x, DCOPLUS = 1  | 2.2 V           | 2.8  | 4.2  | 6.2  | MHz  |
|                       |  | 3 V             | 4.2  | 6.3  | 9.2  |      |
| f <sub>(DCO=27)</sub> | FN <sub>8</sub> = 1, FN <sub>4</sub> = FN <sub>3</sub> = FN <sub>2</sub> = x, DCOPLUS = 1  | 2.2 V           | 21   | 32   | 46   | MHz  |
|                       |  | 3 V             | 30   | 46   | 70   |      |
| S <sub>n</sub>        | Step size between adjacent DCO taps:<br>S <sub>n</sub> = f <sub>DCO(Tap n+1)</sub> / f <sub>DCO(Tap n)</sub> (see Figure 10 for taps 21 to 27)                 | 1 < TAP ≤ 20    | 1.06 |      | 1.11 |      |
|                       |  | TAP = 27        | 1.07 |      | 1.17 |      |
| D <sub>t</sub>        | Temperature drift, N <sub>(DCO)</sub> = 01Eh, FN <sub>8</sub> = FN <sub>4</sub> = FN <sub>3</sub> = FN <sub>2</sub> = 0, D = 2, DCOPLUS = 0 (see Note 2)       | 2.2 V           | -0.2 | -0.3 | -0.4 | %/°C |
|                       |  | 3 V             | -0.2 | -0.3 | -0.4 |      |
| D <sub>V</sub>        | Drift with V <sub>CC</sub> variation, N <sub>(DCO)</sub> = 01Eh, FN <sub>8</sub> = FN <sub>4</sub> = FN <sub>3</sub> = FN <sub>2</sub> = 0, D = 2, DCOPLUS = 0 |                 | 0    | 5    | 15   | %/V  |

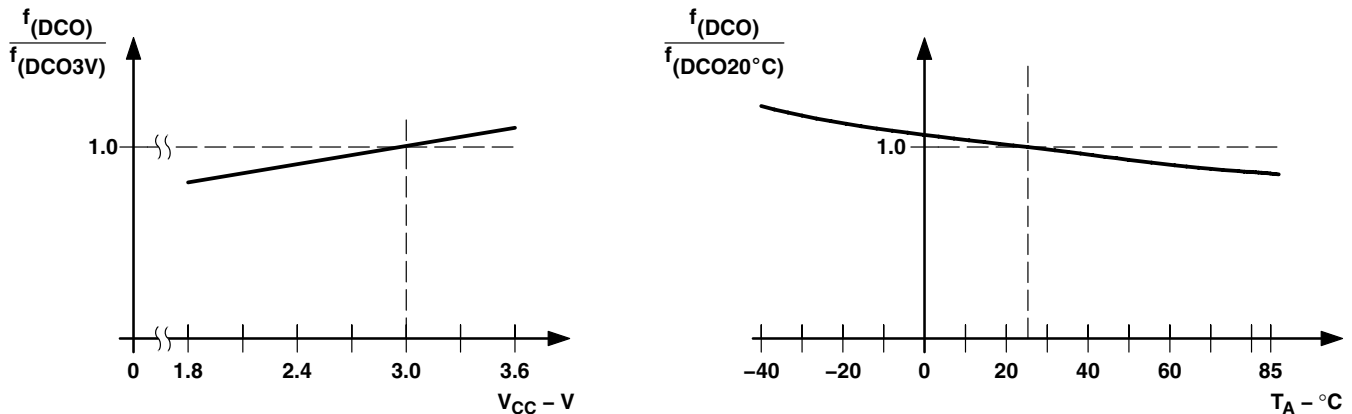


Figure 9. DCO Frequency vs Supply Voltage V<sub>CC</sub> and vs Ambient Temperature



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

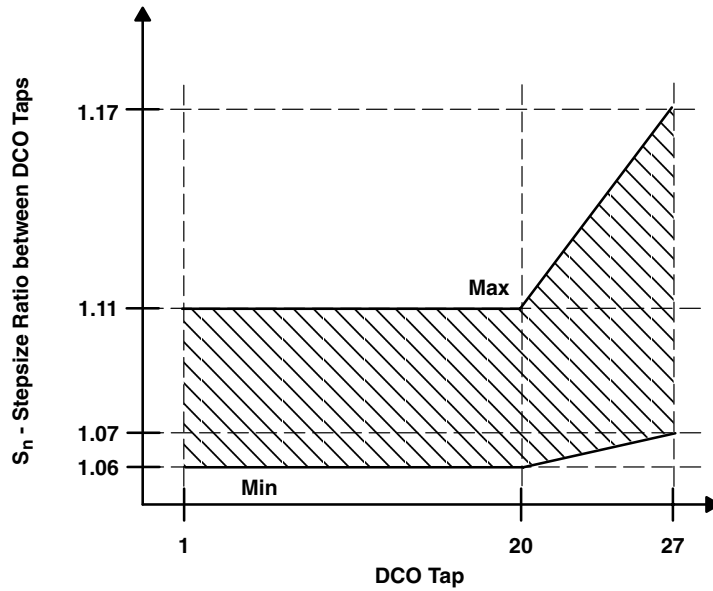


Figure 10. DCO Tap Step Size

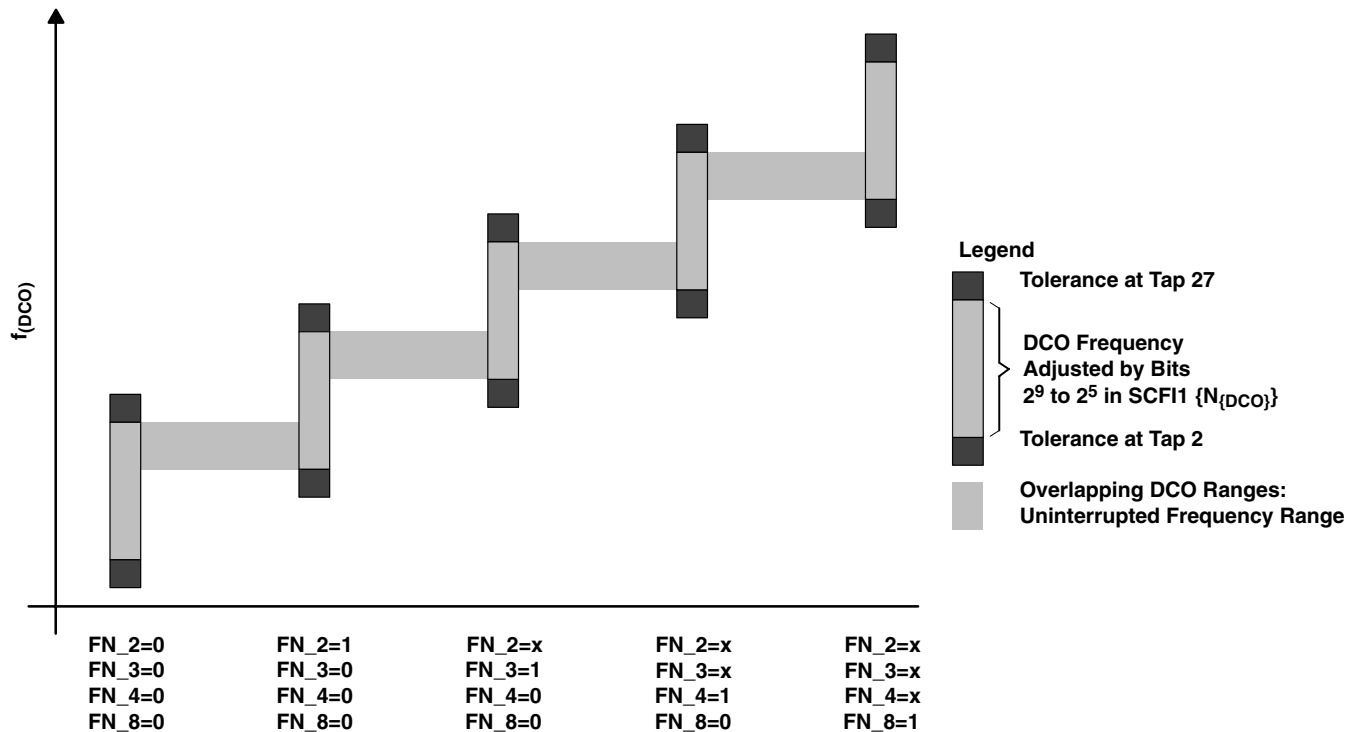


Figure 11. Five Overlapping DCO Ranges Controlled by FN\_x Bits

# MSP430FG42x0 MIXED SIGNAL MICROCONTROLLER

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

| PARAMETER         |  | TEST CONDITIONS                             | MIN                 | TYP | MAX                 | UNIT |
|-------------------|--|---|---------------------|-----|---------------------|------|
| C <sub>XIN</sub>  | Integrated input capacitance (see Note 4)  | OSCCAPx = 0h, V <sub>CC</sub> = 2.2 V / 3 V |                     | 0   |                     | pF   |
|                   |  | OSCCAPx = 1h, V <sub>CC</sub> = 2.2 V / 3 V |                     | 10  |                     |      |
|                   |  | OSCCAPx = 2h, V <sub>CC</sub> = 2.2 V / 3 V |                     | 14  |                     |      |
|                   |  | OSCCAPx = 3h, V <sub>CC</sub> = 2.2 V / 3 V |                     | 18  |                     |      |
| C <sub>XOUT</sub> | Integrated output capacitance (see Note 4) | OSCCAPx = 0h, V <sub>CC</sub> = 2.2 V / 3 V |                     | 0   |                     | pF   |
|                   |  | OSCCAPx = 1h, V <sub>CC</sub> = 2.2 V / 3 V |                     | 10  |                     |      |
|                   |  | OSCCAPx = 2h, V <sub>CC</sub> = 2.2 V / 3 V |                     | 14  |                     |      |
|                   |  | OSCCAPx = 3h, V <sub>CC</sub> = 2.2 V / 3 V |                     | 18  |                     |      |
| V <sub>IL</sub>   | Input levels at XIN                        | V <sub>CC</sub> = 2.2 V/3 V (see Note 3)    | V <sub>SS</sub>     |     | 0.2×V <sub>CC</sub> | V    |
| V <sub>IH</sub>   |  |   | 0.8×V <sub>CC</sub> |     | V <sub>CC</sub>     |      |

- NOTES:
- The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is  $(C_{XIN} \times C_{XOUT}) / (C_{XIN} + C_{XOUT})$ . This is independent of XTS\_FLL.
  - To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
    - Keep as short of a trace as possible between the 'FG42x0 and the crystal.
    - Design a good ground plane around the oscillator pins.
    - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
    - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
    - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
    - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
    - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
  - Applies only when using an external logic-level clock source. XTS\_FLL must be set. Not applicable when using a crystal or resonator.
  - External capacitance is recommended for precision real-time clock applications, OSCCAPx = 0h.



**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**SD16\_A, power supply and recommended operating conditions**

| PARAMETER  | TEST CONDITIONS  | V <sub>CC</sub>        | MIN  | TYP | MAX | UNIT    |   |                             |      |      |
|------------|--|------------------------|------|-----|-----|---------|---|-----------------------------|------|------|
| $V_{CC}$   | Analog supply voltage<br>$AV_{CC} = DV_{CC}$<br>$AV_{SS} = DV_{SS} = 0V$ |                        | 2.5  |     | 3.6 | V       |   |                             |      |      |
| $I_{SD16}$ | Analog supply current including internal reference                       | 3 V                    |      |     |     | $\mu A$ |   |                             |      |      |
|            |  |                        |      |     |     |         | SD16LP = 0,<br>$f_{SD16} = 1$ MHz,<br>SD16OSR = 256   | SD16BUFx = 00, GAIN: 1,2    | 650  | 950  |
|            |  |                        |      |     |     |         |   | SD16BUFx = 00, GAIN: 4,8,16 | 730  | 1100 |
|            |  |                        |      |     |     |         |   | SD16BUFx = 00, GAIN: 32     | 1050 | 1550 |
|            |  |                        |      |     |     |         | SD16LP = 1,<br>$f_{SD16} = 0.5$ MHz,<br>SD16OSR = 256 | SD16BUFx = 00, GAIN: 1      | 620  | 930  |
|            |  |                        |      |     |     |         |   | SD16BUFx = 00, GAIN: 32     | 700  | 1060 |
|            | SD16LP = 0,<br>$f_{SD16} = 1$ MHz,<br>SD16OSR = 256                      | SD16BUFx = 01, GAIN: 1 | 850  |     |     |         |   |                             |      |      |
|            |  | SD16BUFx = 10, GAIN: 1 | 1130 |     |     |         |   |                             |      |      |
|            |  | SD16BUFx = 11, GAIN: 1 | 1130 |     |     |         |   |                             |      |      |
| $f_{SD16}$ | Analog front-end input clock frequency                                   | 3 V                    |      |     |     | MHz     |   |                             |      |      |
|            |  |                        |      |     |     |         | SD16LP = 0 (Low power mode disabled)                  | 0.03                        | 1    | 1.1  |
|            | SD16LP = 1 (Low power mode enabled)                                      |                        | 0.03 | 0.5 |     |         |   |                             |      |      |

**SD16\_A, input range**

| PARAMETER    | TEST CONDITIONS   | V <sub>CC</sub> | MIN       | TYP              | MAX              | UNIT       |                                      |                  |           |     |
|--------------|---|-----------------|-----------|------------------|------------------|------------|--------------------------------------|------------------|-----------|-----|
| $V_{ID,FSR}$ | Differential full scale input voltage range                             |                 |           |                  |                  | mV         |                                      |                  |           |     |
|              | Bipolar mode, SD16UNI = 0   |                 |           |                  |                  |            | $-V_{REF}/2GAIN$                     | $+V_{REF}/2GAIN$ |           |     |
|              | Unipolar mode, SD16UNI = 1  |                 | 0         |                  | $+V_{REF}/2GAIN$ |            |                                      |                  |           |     |
| $V_{ID}$     | Differential input voltage range for specified performance (see Note 1) | SD16REFON=1     |           |                  |                  | mV         |                                      |                  |           |     |
|              |   |                 |           |                  |                  |            | SD16GAINx = 1                        | $\pm 500$        |           |     |
|              |   |                 |           |                  |                  |            | SD16GAINx = 2                        | $\pm 250$        |           |     |
|              |   |                 |           |                  |                  |            | SD16GAINx = 4                        | $\pm 125$        |           |     |
|              |   |                 |           |                  |                  |            | SD16GAINx = 8                        | $\pm 62$         |           |     |
|              |   |                 |           |                  |                  |            | SD16GAINx = 16                       | $\pm 31$         |           |     |
|              | SD16GAINx = 32  | $\pm 15$        |           |                  |                  |            |                                      |                  |           |     |
| $Z_I$        | Input impedance (one input pin to AV <sub>SS</sub> )                    |                 | 3 V       |                  |                  | k $\Omega$ |                                      |                  |           |     |
|              |   |                 |           |                  |                  |            | $f_{SD16} = 1$ MHz,<br>SD16BUFx = 00 | SD16GAINx = 1    | 200       |     |
|              |   |                 |           |                  |                  |            |                                      |                  |           |     |
|              |   |                 |           |                  |                  |            |                                      |                  |           |     |
|              |   |                 |           |                  |                  |            |                                      |                  |           |     |
|              |   |                 |           |                  |                  |            |                                      |                  |           |     |
|              |   |                 |           |                  |                  |            |                                      |                  |           |     |
|              |   |                 |           |                  |                  |            |                                      |                  |           |     |
| $Z_{ID}$     | Differential Input impedance (IN+ to IN-)                               |                 | 3 V       |                  |                  | k $\Omega$ |                                      |                  |           |     |
|              |   |                 |           |                  |                  |            | $f_{SD16} = 1$ MHz,<br>SD16BUFx = 00 | SD16GAINx = 1    | 300       | 400 |
|              |   |                 |           |                  |                  |            |                                      | SD16GAINx = 32   | 100       | 150 |
|              | $f_{SD16} = 1$ MHz,<br>SD16BUFx > 00                                    | SD16GAINx = 1   |           | >10              |                  | M $\Omega$ |                                      |                  |           |     |
| $V_I$        | Absolute input voltage range  |                 |           |                  |                  | V          |                                      |                  |           |     |
|              |   |                 |           |                  |                  |            | SD16BUFx = 00                        | $AV_{SS} - 0.1V$ | $AV_{CC}$ |     |
|              | SD16BUFx > 00   |                 | $AV_{SS}$ | $AV_{CC} - 1.2V$ |                  |            |                                      |                  |           |     |
| $V_{IC}$     | Common-mode input voltage range   |                 |           |                  |                  | V          |                                      |                  |           |     |
|              |   |                 |           |                  |                  |            | SD16BUFx = 00                        | $AV_{SS} - 0.1V$ | $AV_{CC}$ |     |
|              | SD16BUFx > 00   |                 | $AV_{SS}$ | $AV_{CC} - 1.2V$ |                  |            |                                      |                  |           |     |

NOTES: 1. The analog input range depends on the reference voltage applied to V<sub>REF</sub>. If V<sub>REF</sub> is sourced externally, the full-scale range is defined by V<sub>FSR+</sub> = +(V<sub>REF</sub>/2)/GAIN and V<sub>FSR-</sub> = -(V<sub>REF</sub>/2)/GAIN. The analog input range should not exceed 80% of V<sub>FSR+</sub> or V<sub>FSR-</sub>.

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

## SD16\_A, performance ( $f_{SD16} = 30\text{kHz}$ , $SD16REFON = 1$ , $SD16BUFx = 01$ )

| PARAMETER  | TEST CONDITIONS   | V <sub>CC</sub> | MIN  | TYP  | MAX  | UNIT   |
|--|---|-----------------|------|------|------|--------|
| SINAD<br>Signal-to-noise + distortion ratio      | SD16GAINx = 1, Signal Amplitude = 500mV<br>SD16OSRx = 256                     | 3 V             |      | 84   |      | dB     |
|  | SD16GAINx = 1, Signal Amplitude = 500mV<br>SD16OSRx = 512                     |                 |      |      |      |        |
|  | SD16GAINx = 1, Signal Amplitude = 500mV<br>SD16OSRx = 1024                    |                 |      |      |      |        |
| Nominal gain                                     | SD16GAINx = 1, SD16OSRx = 1024  | 3 V             | 0.97 | 1.00 | 1.02 |        |
| dG/dT<br>Gain temperature drift                  | SD16GAINx = 1, SD16OSRx = 1024 (see Note 1)                                   | 3 V             |      | 15   |      | ppm/°C |
| dG/dV <sub>CC</sub><br>Gain supply voltage drift | SD16GAINx = 1, SD16OSRx = 1024, V <sub>CC</sub> = 2.5 V to 3.6 V (see Note 2) |                 |      | 0.35 |      | %/V    |

NOTES: 1. Calculated using the box method:  $(\text{MAX}(-40\dots85^\circ\text{C}) - \text{MIN}(-40\dots85^\circ\text{C})) / \text{MIN}(-40\dots85^\circ\text{C}) / (85^\circ\text{C} - (-40^\circ\text{C}))$   
2. Calculated using the box method:  $(\text{MAX}(2.5\dots3.6\text{V}) - \text{MIN}(2.5\dots3.6\text{V})) / \text{MIN}(2.5\dots3.6\text{V}) / (3.6\text{V} - 2.5\text{V})$

## SD16\_A, performance ( $f_{SD16} = 1\text{MHz}$ , $SD16OSRx = 256$ , $SD16REFON = 1$ , $SD16BUFx = 00$ )

| PARAMETER  | TEST CONDITIONS   | V <sub>CC</sub> | MIN | TYP   | MAX   | UNIT       |
|--|---|-----------------|-----|-------|-------|------------|
| SINAD<br>Signal-to-noise + distortion ratio                  | SD16GAINx = 1, Signal Amplitude = 500mV   | 3 V             |     | 83.5  | 85    | dB         |
|  | SD16GAINx = 2, Signal Amplitude = 250mV   |                 |     | 81.5  | 84    |            |
|  | SD16GAINx = 4, Signal Amplitude = 125mV   |                 |     | 76    | 79.5  |            |
|  | SD16GAINx = 8, Signal Amplitude = 62mV  |                 |     | 73    | 76.5  |            |
|  | SD16GAINx = 16, Signal Amplitude = 31mV   |                 |     | 69    | 73    |            |
|  | SD16GAINx = 32, Signal Amplitude = 15mV   |                 |     | 62    | 69    |            |
| G<br>Nominal gain  | SD16GAINx = 1   | 3 V             |     | 0.97  | 1.00  | 1.02       |
|  | SD16GAINx = 2   |                 |     | 1.90  | 1.96  | 2.02       |
|  | SD16GAINx = 4   |                 |     | 3.76  | 3.86  | 3.96       |
|  | SD16GAINx = 8   |                 |     | 7.36  | 7.62  | 7.84       |
|  | SD16GAINx = 16  |                 |     | 14.56 | 15.04 | 15.52      |
|  | SD16GAINx = 32  |                 |     | 27.20 | 28.35 | 29.76      |
| E <sub>OS</sub><br>Offset error                              | SD16GAINx = 1   | 3 V             |     |       |       | ±0.2       |
|  | SD16GAINx = 32  |                 |     |       |       | ±1.5       |
| dE <sub>OS</sub> /dT<br>Offset error temperature coefficient | SD16GAINx = 1   | 3 V             |     |       |       | ±4    ±20  |
|  | SD16GAINx = 32  |                 |     |       |       | ±20   ±100 |
| CMRR<br>Common-mode rejection ratio                          | SD16GAINx = 1, Common-mode input signal:<br>V <sub>ID</sub> = 500 mV, f <sub>IN</sub> = 50 Hz, 100 Hz | 3 V             |     |       |       | >90        |
|  | SD16GAINx = 32, Common-mode input signal:<br>V <sub>ID</sub> = 16 mV, f <sub>IN</sub> = 50 Hz, 100 Hz |                 |     |       |       | >75        |
| AC PSRR<br>AC power supply rejection ratio                   | SD16GAINx = 1, V <sub>CC</sub> = 3 V ± 100 mV, f <sub>VCC</sub> = 50 Hz                               | 3 V             |     |       |       | >80        |



**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**SD16\_A, temperature sensor**

| PARAMETER                  |                                    | TEST CONDITIONS                                     | V <sub>CC</sub> | MIN  | TYP  | MAX  | UNIT |
|----------------------------|------------------------------------|---|-----------------|------|------|------|------|
| TC <sub>Sensor</sub>       | Sensor temperature coefficient     |   |                 | 1.18 | 1.32 | 1.46 | mV/K |
| V <sub>Offset,sensor</sub> | Sensor offset voltage              |   |                 | -100 |      | 100  | mV   |
| V <sub>Sensor</sub>        | Sensor output voltage (see Note 2) | Temperature sensor voltage at T <sub>A</sub> = 85°C | 3 V             | 435  | 475  | 515  | mV   |
|                            |                                    | Temperature sensor voltage at T <sub>A</sub> = 25°C |                 | 355  | 395  | 435  |      |
|                            |                                    | Temperature sensor voltage at T <sub>A</sub> = 0°C  |                 | 320  | 360  | 400  |      |

NOTES: 1. The following formula can be used to calculate the temperature sensor output voltage:

$$V_{\text{Sensor,typ}} = TC_{\text{Sensor}} (273 + T [^{\circ}\text{C}]) + V_{\text{Offset,sensor}} [\text{mV}]$$

2. Results based on characterization and/or production test, not TC<sub>Sensor</sub> or V<sub>Offset,sensor</sub>.

**SD16\_A, built-in voltage reference**

| PARAMETER         |  | TEST CONDITIONS   | V <sub>CC</sub> | MIN  | TYP  | MAX  | UNIT  |
|-------------------|--|---|-----------------|------|------|------|-------|
| V <sub>REF</sub>  | Internal reference voltage                                     | SD16REFON = 1, SD16VMIDON = 0                                   | 3 V             | 1.14 | 1.20 | 1.26 | V     |
| I <sub>REF</sub>  | Reference supply current                                       | SD16REFON = 1, SD16VMIDON = 0                                   | 3 V             |      | 175  | 260  | μA    |
| TC                | Temperature coefficient  | SD16REFON = 1, SD16VMIDON = 0                                   | 3 V             |      | 18   | 50   | ppm/K |
| C <sub>REF</sub>  | V <sub>REF</sub> load capacitance                              | SD16REFON = 1, SD16VMIDON = 0 (see Note 1)                      |                 |      | 100  |      | nF    |
| I <sub>LOAD</sub> | V <sub>REF(I)</sub> maximum load current                       | SD16REFON = 1, SD16VMIDON = 0                                   | 3 V             |      |      | ±200 | nA    |
| t <sub>ON</sub>   | Turn-on time   | SD16REFON = 0→1, SD16VMIDON = 0, C <sub>REF</sub> = 100 nF      | 3 V             |      | 5    |      | ms    |
| DC PSR            | DC power-supply rejection, ΔV <sub>REF</sub> /ΔV <sub>CC</sub> | SD16REFON = 1, SD16VMIDON = 0, V <sub>CC</sub> = 2.5 V to 3.6 V |                 |      | 100  |      | μV/V  |

NOTES: 1. There is no capacitance required on V<sub>REF</sub>. However, a capacitance of at least 100nF is recommended to reduce any reference voltage noise.

**SD16\_A, reference output buffer**

| PARAMETER             |  | TEST CONDITIONS  | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-----------------------|--|--|-----------------|-----|-----|-----|------|
| V <sub>REF,BUF</sub>  | Reference buffer output voltage                              | SD16REFON = 1, SD16VMIDON = 1                              | 3 V             |     | 1.2 |     | V    |
| I <sub>REF,BUF</sub>  | Reference supply + reference output buffer quiescent current | SD16REFON = 1, SD16VMIDON = 1                              | 3 V             |     | 385 | 600 | μA   |
| C <sub>REF(O)</sub>   | Required load capacitance on V <sub>REF</sub>                | SD16REFON = 1, SD16VMIDON = 1                              |                 | 470 |     |     | nF   |
| I <sub>LOAD,Max</sub> | Maximum load current on V <sub>REF</sub>                     | SD16REFON = 1, SD16VMIDON = 1                              | 3 V             |     |     | ±1  | mA   |
|                       | Maximum voltage variation vs load current                    | I <sub>LOAD</sub>   = 0 to 1 mA                            | 3 V             | -15 |     | +15 | mV   |
| t <sub>ON</sub>       | Turn-on time   | SD16REFON = 0→1, SD16VMIDON = 1, C <sub>REF</sub> = 470 nF | 3 V             |     | 100 |     | μs   |

**SD16\_A, external reference input**

| PARAMETER           |                     | TEST CONDITIONS | V <sub>CC</sub> | MIN | TYP  | MAX | UNIT |
|---------------------|---------------------|-----------------|-----------------|-----|------|-----|------|
| V <sub>REF(I)</sub> | Input voltage range | SD16REFON = 0   | 3 V             | 1.0 | 1.25 | 1.5 | V    |
| I <sub>REF(I)</sub> | Input current       | SD16REFON = 0   | 3 V             |     |      | 50  | nA   |

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## MIXED SIGNAL MICROCONTROLLER

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### 12-bit DAC, supply specifications

| PARAMETER        |   | TEST CONDITIONS  | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT |
|------------------|---|--|-----------------|------|-----|------|------|
| AV <sub>CC</sub> | Analog supply voltage                               | AV <sub>CC</sub> = DV <sub>CC</sub> ,<br>AV <sub>SS</sub> = DV <sub>SS</sub> = 0 V           |                 | 2.20 |     | 3.60 | V    |
| I <sub>DD</sub>  | Supply current<br>(see Notes 1 and 2)               | DAC12AMPx = 2, DAC12IR=0,<br>DAC12_xDAT=0800h  | 2.2V/3V         |      | 50  | 110  | μA   |
|                  |   | DAC12AMPx = 2, DAC12IR=1,<br>DAC12_xDAT = 0800h, V <sub>REF,DAC12</sub> = AV <sub>CC</sub>   |                 |      | 50  | 110  |      |
|                  |   | DAC12AMPx = 5, DAC12IR = 1,<br>DAC12_xDAT = 0800h, V <sub>REF,DAC12</sub> = AV <sub>CC</sub> |                 |      | 200 | 440  |      |
|                  |   | DAC12AMPx=7, DAC12IR = 1,<br>DAC12_xDAT = 0800h, V <sub>REF,DAC12</sub> = AV <sub>CC</sub>   |                 |      | 700 | 1500 |      |
| PSRR             | Power supply rejection ratio<br>(see Notes 3 and 4) | DAC12_xDAT = 800h, V <sub>REF,DAC12</sub> = 1.2V<br>ΔAV <sub>CC</sub> = 100 mV               | 2.7V            |      | 70  |      | dB   |

- NOTES: 1. No load at the output pin assuming that the control bits for the shared pins are set properly.  
 2. Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.  
 3. PSRR = 20 × log{ΔAV<sub>CC</sub>/ΔV<sub>DAC12\_xOUT</sub>}.  
 4. V<sub>REF</sub> is applied externally. The internal reference is not used.



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (see Figure 12)

| PARAMETER               |   | TEST CONDITIONS  | V <sub>CC</sub> | MIN | TYP  | MAX   | UNIT          |
|-------------------------|---|--|-----------------|-----|------|-------|---------------|
| Resolution              |   | 12-bit monotonic   |                 | 12  |      |       | bits          |
| INL                     | Integral nonlinearity (see Note 1)                | V <sub>REF,DAC12</sub> = 1.2 V, DAC12AMPx = 7, DAC12IR = 1 | 2.7 V           |     | ±2.0 | ±8.0  | LSB           |
| DNL                     | Differential nonlinearity (see Note 1)            | V <sub>REF,DAC12</sub> = 1.2 V, DAC12AMPx = 7, DAC12IR = 1 | 2.7 V           |     | ±0.4 | ±1.0  | LSB           |
| E <sub>O</sub>          | Offset voltage w/o calibration (see Notes 1, 2)   | V <sub>REF,DAC12</sub> = 1.2 V, DAC12AMPx = 7, DAC12IR = 1 | 2.7 V           |     |      | ±20   | mV            |
|                         | Offset voltage with calibration (see Notes 1, 2)  | V <sub>REF,DAC12</sub> = 1.2 V, DAC12AMPx = 7, DAC12IR = 1 | 2.7 V           |     |      | ±2.5  |               |
| d <sub>E(O)</sub> /dT   | Offset error temperature coefficient (see Note 1) |  | 2.7 V           |     | ±30  |       | µV/C          |
| E <sub>G</sub>          | Gain error (see Note 1)                           | V <sub>REF,DAC12</sub> = 1.2 V                             | 2.7 V           |     |      | ±3.50 | % FSR         |
| d <sub>E(G)</sub> /dT   | Gain temperature coefficient (see Note 1)         |  | 2.7 V           |     | 10   |       | ppm of FSR/°C |
| t <sub>Offset_Cal</sub> | Time for offset calibration (see Note 3)          | DAC12AMPx = 2  | 2.7 V           |     |      | 100   | ms            |
|                         |   | DAC12AMPx = 3, 5   | 2.7 V           |     |      | 32    |               |
|                         |   | DAC12AMPx = 4, 6, 7  | 2.7 V           |     |      | 6     |               |

- NOTES: 1. Parameters calculated from the best-fit curve from 0x0A to 0xFF. The best-fit curve method is used to deliver coefficients “a” and “b” of the first order equation:  $y = a + b \cdot x$ .  $V_{DAC12\_xOUT} = E_O + (1 + E_G) \cdot (V_{REF,DAC12}/4095) \cdot DAC12\_xDAT$ , DAC12IR = 1.  
 2. The offset calibration works on the output operational amplifier. Offset calibration is triggered setting bit DAC12CALON.  
 3. The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. It is recommended that the DAC12 module be configured prior to initiating calibration. Port activity during calibration may effect accuracy and is not recommended.

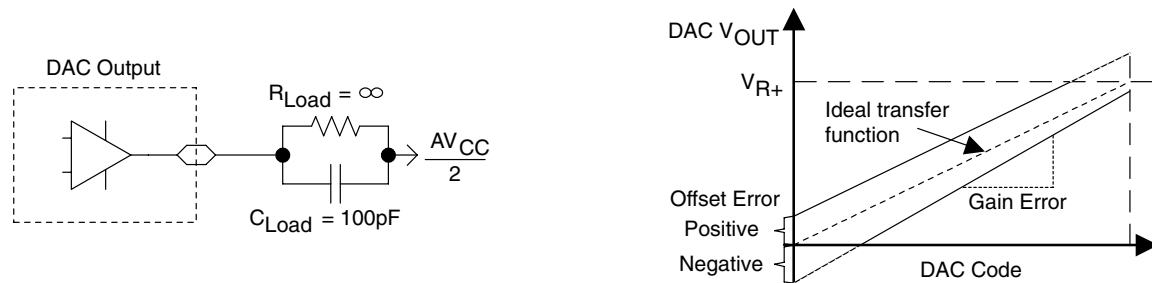


Figure 12. Linearity Test Load Conditions and Gain/Offset Definition

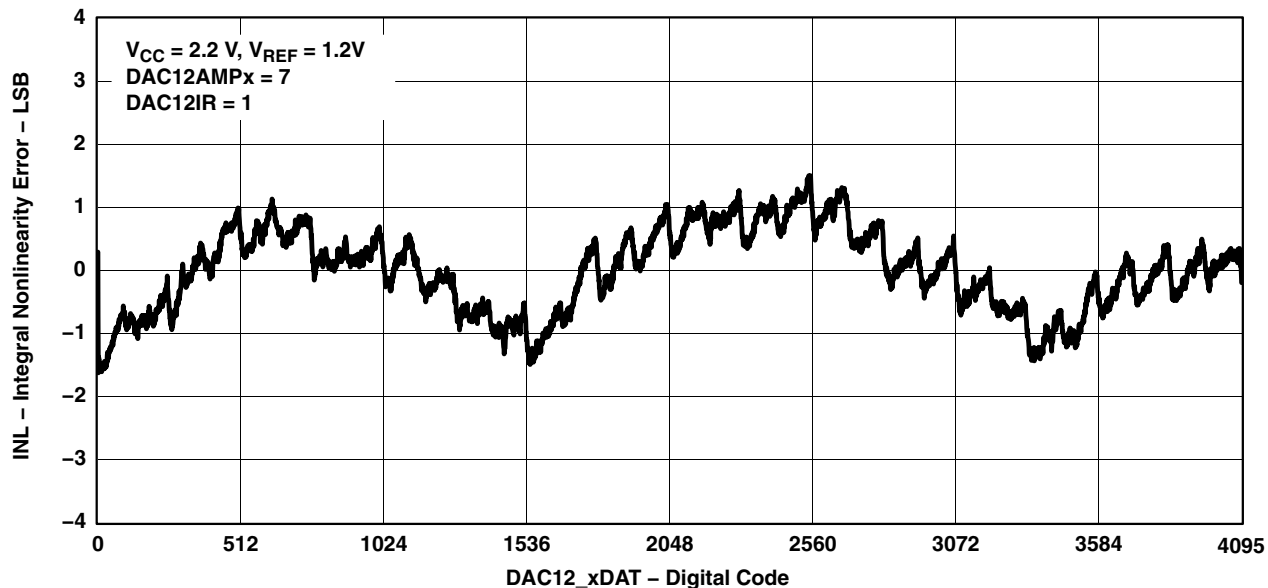
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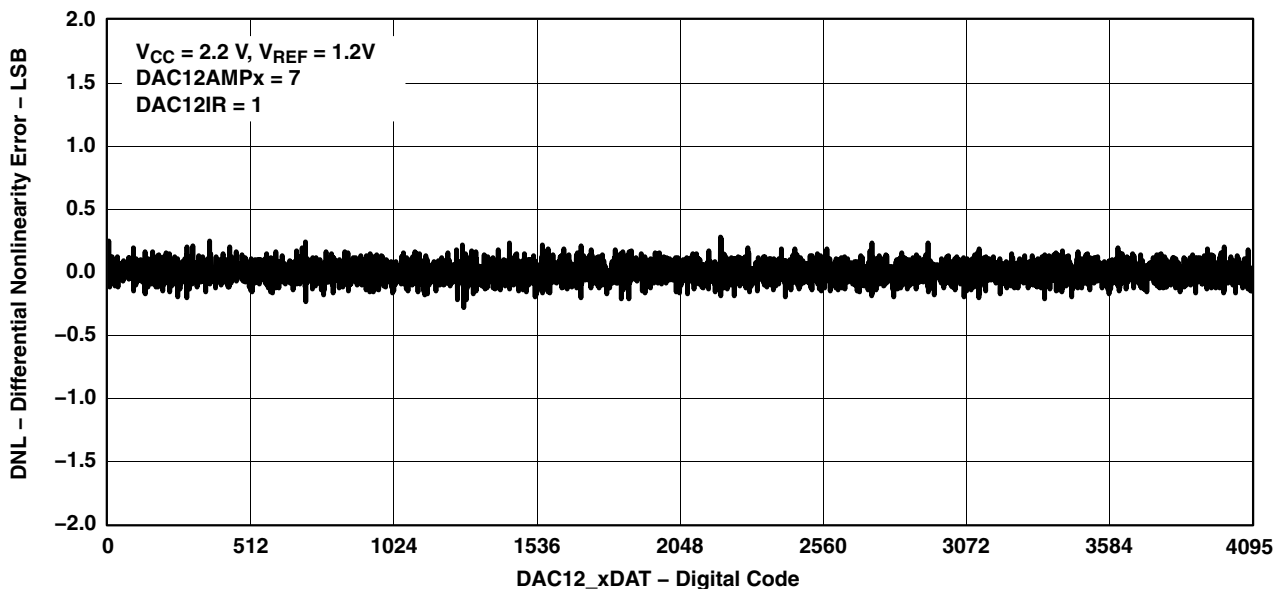
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (continued)

TYPICAL INL ERROR  
vs  
DIGITAL INPUT DATA



TYPICAL DNL ERROR  
vs  
DIGITAL INPUT DATA



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, output specifications

| PARAMETER   | TEST CONDITIONS  | V <sub>CC</sub> | MIN                    | TYP | MAX              | UNIT |
|---|--|-----------------|------------------------|-----|------------------|------|
| V <sub>O</sub><br>Output voltage range<br>(see Note 1, Figure 15) | No load, V <sub>REF,DAC12</sub> = AV <sub>CC</sub> ,<br>DAC12_xDAT = 0h, DAC12IR = 1,<br>DAC12AMPx = 7                     | 2.2V/3V         | 0                      |     | 0.005            | V    |
|   | No load, V <sub>REF,DAC12</sub> = AV <sub>CC</sub> ,<br>DAC12_xDAT = 0FFFh, DAC12IR = 1,<br>DAC12AMPx = 7                  |                 | AV <sub>CC</sub> -0.05 |     | AV <sub>CC</sub> |      |
|   | R <sub>Load</sub> = 3 kΩ, V <sub>REF,DAC12</sub> = AV <sub>CC</sub> ,<br>DAC12_xDAT = 0h, DAC12IR = 1,<br>DAC12AMPx = 7    |                 | 0                      |     | 0.1              |      |
|   | R <sub>Load</sub> = 3 kΩ, V <sub>REF,DAC12</sub> = AV <sub>CC</sub> ,<br>DAC12_xDAT = 0FFFh, DAC12IR = 1,<br>DAC12AMPx = 7 |                 | AV <sub>CC</sub> -0.13 |     | AV <sub>CC</sub> |      |
| C <sub>L(DAC12)</sub>   | Max DAC12 load capacitance   | 2.2V/3V         |                        |     | 100              | pF   |
| I <sub>L(DAC12)</sub>   | Max DAC12 load current   | 2.2V            | -0.5                   |     | +0.5             | mA   |
|   |  | 3V              | -1.0                   |     | +1.0             |      |
| R <sub>O/P(DAC12)</sub>   | R <sub>Load</sub> = 3 kΩ, V <sub>O/P(DAC12)</sub> < 0.3 V,<br>DAC12AMPx = 2, DAC12_xDAT = 0h                               | 2.2V/3V         |                        | 150 | 250              | Ω    |
|   | R <sub>Load</sub> = 3 kΩ,<br>V <sub>O/P(DAC12)</sub> > AV <sub>CC</sub> - 0.3 V<br>DAC12_xDAT = 0FFFh                      |                 |                        | 150 | 250              |      |
|   | R <sub>Load</sub> = 3 kΩ,<br>0.3 V ≤ V <sub>O/P(DAC12)</sub> ≤ AV <sub>CC</sub> - 0.3 V                                    |                 |                        | 1   | 4                |      |

NOTES: 1. Data is valid after the offset calibration of the output amplifier.

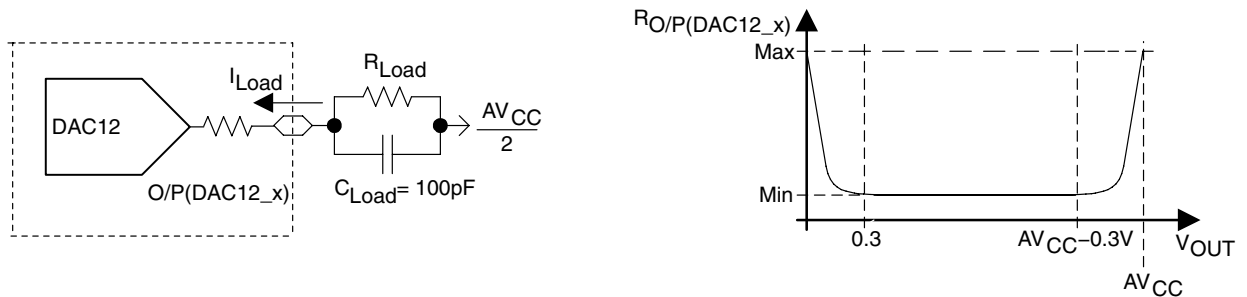


Figure 15. DAC12\_x Output Resistance Tests

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

## 12-bit DAC, reference input specifications

| PARAMETER            | TEST CONDITIONS               | V <sub>CC</sub> | MIN                 | TYP | MAX                   | UNIT |
|----------------------|-------------------------------|-----------------|---------------------|-----|-----------------------|------|
| V <sub>REF</sub>     | Reference input voltage range | 2.2V/3V         | AV <sub>CC</sub> /3 |     | AV <sub>CC</sub> +0.2 | V    |
|                      |                               |                 | AV <sub>CC</sub>    |     | AV <sub>CC</sub> +0.2 |      |
| R <sub>i(VREF)</sub> | Reference input resistance    | 2.2V/3V         | 20                  |     | 56                    | MΩ   |
|                      |                               |                 | 40                  |     |                       | 48   |

- NOTES: 1. For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV<sub>CC</sub>).  
 2. The maximum voltage applied at reference input voltage terminal V<sub>REF</sub> = [AV<sub>CC</sub> - V<sub>E(O)</sub>] / [3\*(1 + E<sub>G</sub>)].  
 3. For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV<sub>CC</sub>).  
 4. The maximum voltage applied at reference input voltage terminal V<sub>REF</sub> = [AV<sub>CC</sub> - V<sub>E(O)</sub>] / (1 + E<sub>G</sub>).

## 12-bit DAC, dynamic specifications, V<sub>REF,DAC12</sub> = AV<sub>CC</sub>, DAC12IR = 1 (see Figure 16 and Figure 17)

| PARAMETER                 | TEST CONDITIONS   | V <sub>CC</sub> | MIN                     | TYP | MAX  | UNIT |      |
|---------------------------|---|-----------------|-------------------------|-----|------|------|------|
| t <sub>ON</sub>           | DAC12_xDAT = 800h, Error <sub>V(O)</sub> < ±0.5 LSB (see Note 1, Figure 16) | 2.2V/3V         | DAC12AMPx=0 → {2, 3, 4} |     | 60   | 120  | μs   |
|                           |   |                 | DAC12AMPx=0 → {5, 6}    |     | 15   | 30   |      |
|                           |   |                 | DAC12AMPx=0 → 7         |     | 6    | 12   |      |
| t <sub>S(FS)</sub>        | DAC12_xDAT = 80h → F7Fh → 80h   | 2.2V/3V         | DAC12AMPx=2             |     | 100  | 200  | μs   |
|                           |   |                 | DAC12AMPx=3,5           |     | 40   | 80   |      |
|                           |   |                 | DAC12AMPx=4,6,7         |     | 15   | 30   |      |
| t <sub>S(C-C)</sub>       | DAC12_xDAT = 3F8h → 408h → 3F8h<br>BF8h → C08h → BF8h                       | 2.2V/3V         | DAC12AMPx=2             |     | 5    | μs   |      |
|                           |   |                 | DAC12AMPx=3,5           |     | 2    |      |      |
|                           |   |                 | DAC12AMPx=4,6,7         |     | 1    |      |      |
| SR                        | DAC12_xDAT = 80h → F7Fh → 80h   | 2.2V/3V         | DAC12AMPx=2             |     | 0.05 | 0.12 | V/μs |
|                           |   |                 | DAC12AMPx=3,5           |     | 0.35 | 0.7  |      |
|                           |   |                 | DAC12AMPx=4,6,7         |     | 1.5  | 2.7  |      |
| Glitch energy, full scale | DAC12_xDAT = 80h → F7Fh → 80h   | 2.2V/3V         | DAC12AMPx=2             |     | 10   | nV-s |      |
|                           |   |                 | DAC12AMPx=3,5           |     | 10   |      |      |
|                           |   |                 | DAC12AMPx=4,6,7         |     | 15   |      |      |

- NOTES: 1. R<sub>Load</sub> and C<sub>Load</sub> connected to AV<sub>SS</sub> (not AV<sub>CC</sub>/2) in Figure 16.  
 2. Slew rate applies to output voltage steps ≥ 200mV.

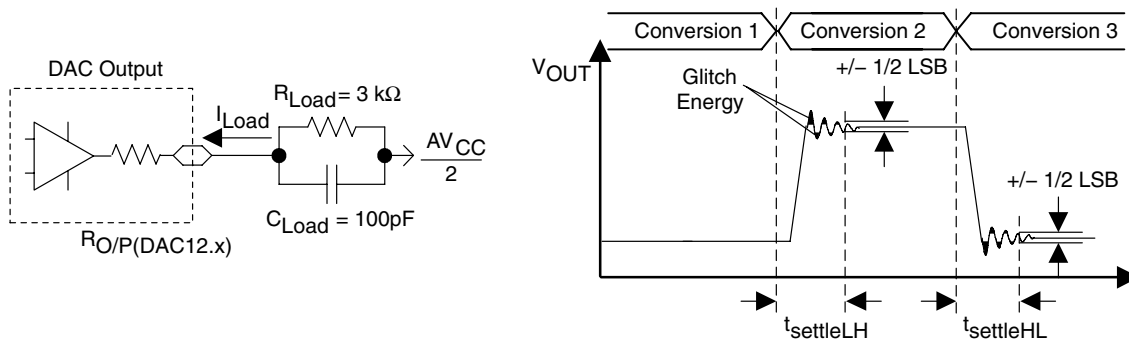


Figure 16. Settling Time and Glitch Energy Testing

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

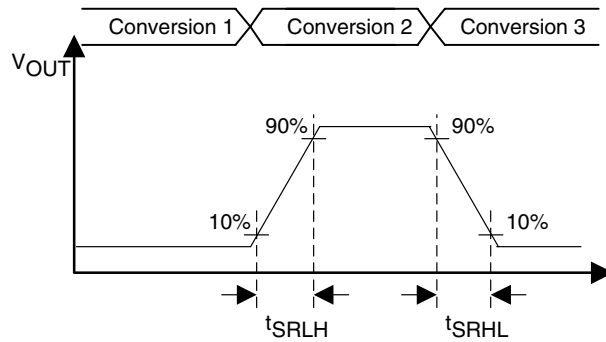


Figure 17. Slew Rate Testing

12-bit DAC, dynamic specifications (continued) ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

| PARAMETER   | TEST CONDITIONS  | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|--|----------|-----|-----|-----|------|
| $BW_{-3dB}$<br>3-dB bandwidth,<br>$V_{DC}=1.5\text{ V}$ , $V_{AC}=0.1\text{ V}_{PP}$<br>(see Figure 18) | $DAC12AMPx = \{2, 3, 4\}$ , $DAC12SREFx = 2$ ,<br>$DAC12IR = 1$ , $DAC12\_xDAT = 800h$ | 2.2V/3V  | 40  |     | kHz |      |
|   | $DAC12AMPx = \{5, 6\}$ , $DAC12SREFx = 2$ ,<br>$DAC12IR = 1$ , $DAC12\_xDAT = 800h$    |          | 180 |     |     |      |
|   | $DAC12AMPx = 7$ , $DAC12SREFx = 2$ ,<br>$DAC12IR = 1$ , $DAC12\_xDAT = 800h$           |          | 550 |     |     |      |

NOTES: 1.  $R_{LOAD} = 3\text{ k}\Omega$ ,  $C_{LOAD} = 100\text{ pF}$

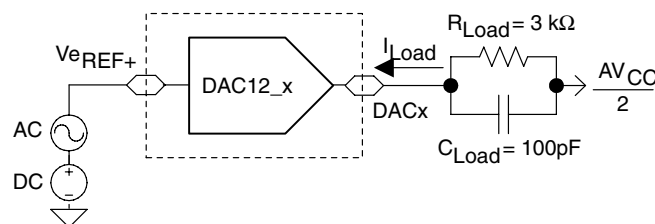


Figure 18. Test Conditions for 3-dB Bandwidth Specification

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

### operational amplifier OA, supply specifications

| PARAMETER                                   | TEST CONDITIONS | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|---|-----------------|-----------------|-----|-----|-----|------|
| V <sub>CC</sub> Supply voltage              |                 | —               | 2.2 |     | 3.6 | V    |
| I <sub>CC</sub> Supply current (see Note 1) | Fast Mode       | 2.2 V/3 V       |     | 180 | 290 | μA   |
|   | Medium Mode     |                 |     | 110 | 190 |      |
|   | Slow Mode       |                 |     | 50  | 80  |      |
| PSRR Power supply rejection ratio           | Non-inverting   | 2.2 V/3 V       |     | 70  |     | dB   |

NOTES: 1. P6SEL.x = 1 or SD16AE.x = 1 for each corresponding pin when used in OA input or OA output mode.

### operational amplifier OA, input/output specifications

| PARAMETER   | TEST CONDITIONS  | V <sub>CC</sub> | MIN                  | TYP  | MAX                  | UNIT   |
|---|--|-----------------|----------------------|------|----------------------|--------|
| V <sub>I/P</sub> Input voltage, I/P                             |  | —               | -0.1                 |      | V <sub>CC</sub> -1.2 | V      |
| I <sub>lkg</sub> Input leakage current, I/P (see Notes 1 and 2) | T <sub>A</sub> = -40°C to 55°C   | —               | -5                   | ±0.5 | 5                    | nA     |
|   | T <sub>A</sub> = 55°C to 85°C  |                 | -20                  | ±5   | 20                   | nA     |
| V <sub>n</sub> Voltage noise density, I/P                       | Fast Mode  | —               |                      | 50   |                      | nV/√Hz |
|   | Medium Mode  |                 |                      | 80   |                      |        |
|   | Slow Mode  |                 |                      | 140  |                      |        |
|   | Fast Mode  |                 |                      | 30   |                      |        |
|   | Medium Mode  |                 |                      | 50   |                      |        |
|   | Slow Mode  |                 |                      | 65   |                      |        |
| V <sub>IO</sub> Offset voltage, I/P                             |  | 2.2 V/3 V       |                      |      | ±10                  | mV     |
| Offset temperature drift, I/P                                   | see Note 3   | 2.2 V/3 V       |                      | ±10  |                      | μV/°C  |
| Offset voltage drift with supply, I/P                           | 0.3V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> -0.3 V<br>ΔV <sub>CC</sub> ≤ ± 10%, T <sub>A</sub> = 25°C | 2.2 V/3 V       |                      |      | ±1.5                 | mV/V   |
| V <sub>OH</sub> High-level output voltage, O/P                  | Fast Mode, I <sub>SOURCE</sub> ≤ -500 μA   | 2.2 V           | V <sub>CC</sub> -0.2 |      | V <sub>CC</sub>      | V      |
|   | Slow Mode, I <sub>SOURCE</sub> ≤ -150 μA   | 3 V             | V <sub>CC</sub> -0.1 |      | V <sub>CC</sub>      | V      |
| V <sub>OL</sub> Low-level output voltage, O/P                   | Fast Mode, I <sub>SOURCE</sub> ≤ +500 μA   | 2.2 V           | V <sub>SS</sub>      |      | 0.2                  | V      |
|   | Slow Mode, I <sub>SOURCE</sub> ≤ +150 μA   | 3 V             | V <sub>SS</sub>      |      | 0.1                  | V      |
| CMRR Common-mode rejection ratio                                | Non-inverting  | 2.2 V/3 V       |                      | 70   |                      | dB     |

NOTES: 1. ESD damage can degrade input current leakage.  
 2. The input bias current is overridden by the input leakage current.  
 3. Characterized and calculated using the box method, not production tested.



electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

operational amplifier OA, dynamic specifications

| PARAMETER              |  | TEST CONDITIONS  | V <sub>CC</sub> | MIN | TYP | MAX  | UNIT |
|------------------------|--|--|-----------------|-----|-----|------|------|
| SR                     | Slew rate  | Fast Mode  | —               | 1.2 |     | V/μs |      |
|                        |  | Medium Mode  |                 | 0.8 |     |      |      |
|                        |  | Slow Mode  |                 | 0.3 |     |      |      |
| Open-loop voltage gain |  |  | —               | 100 |     | dB   |      |
| φ <sub>m</sub>         | Phase margin   | C <sub>L</sub> = 50 pF   | —               | 60  |     | deg  |      |
| Gain margin            |  | C <sub>L</sub> = 50 pF   | —               | 20  |     | dB   |      |
| GBW                    | Gain-bandwidth product<br>(see Figure 19<br>and Figure 20) | Noninverting, Fast Mode, R <sub>L</sub> = 47kΩ, C <sub>L</sub> = 50pF    | 2.2 V/3 V       | 2.2 |     | MHz  |      |
|                        |  | Noninverting, Medium Mode, R <sub>L</sub> = 300kΩ, C <sub>L</sub> = 50pF |                 | 1.4 |     |      |      |
|                        |  | Noninverting, Slow Mode, R <sub>L</sub> = 300kΩ, C <sub>L</sub> = 50pF   |                 | 0.5 |     |      |      |
| t <sub>en(on)</sub>    | Enable time on   | t <sub>on</sub> , noninverting, Gain = 1                                 | 2.2 V/3 V       | 10  | 20  | μs   |      |
| t <sub>en(off)</sub>   | Enable time off  |  | 2.2 V/3 V       | 1   |     | μs   |      |

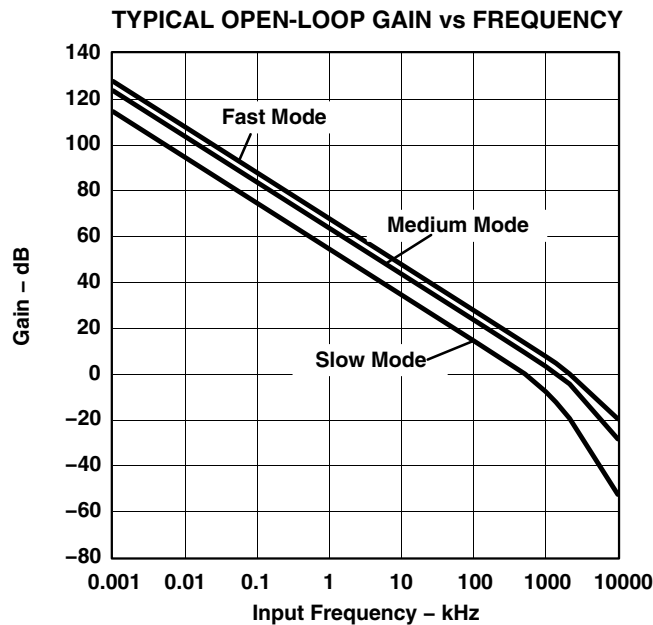


Figure 19

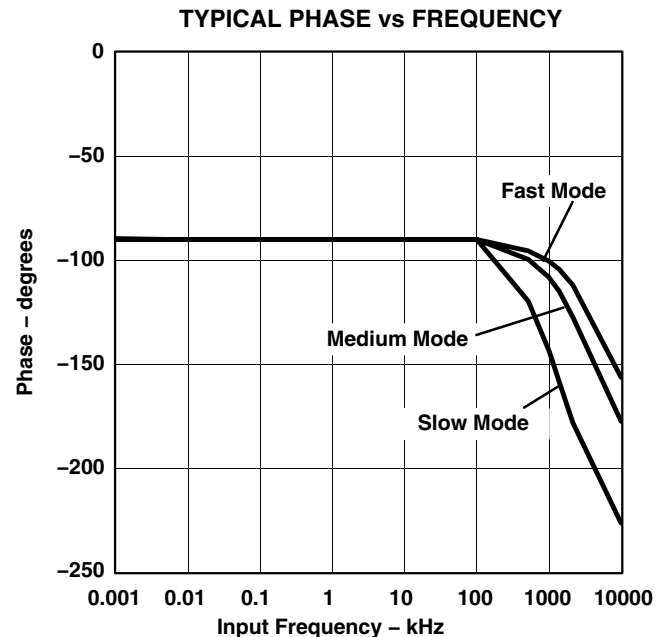


Figure 20

switches to ground

| PARAMETER        | TEST CONDITIONS                       | V <sub>CC</sub>  | MIN | TYP | MAX | UNIT |
|------------------|---------------------------------------|--|-----|-----|-----|------|
| V <sub>CC</sub>  | Supply voltage                        |  | 2.5 |     | 3.6 | V    |
| I <sub>Ikg</sub> | Input leakage current<br>(see Note 1) | T <sub>A</sub> = -40°C to +55°C                          |     | ±1  | ±10 | nA   |
|                  |                                       | T <sub>A</sub> = 55°C to 85°C                            |     |     | ±50 |      |
| I <sub>IN</sub>  | Input current                         | Input switched to Ground.                                |     | 0   | 100 | μA   |
| R <sub>ON</sub>  | On resistance                         | I <sub>IN</sub> = 100 μA, T <sub>A</sub> = -40°C to 85°C |     |     | 10  | Ω    |

NOTES: 1. ESD damage can degrade input current leakage.

# MSP430FG42x0 MIXED SIGNAL MICROCONTROLLER

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## electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

### flash memory

| PARAMETER                  |   | TEST CONDITIONS       | V <sub>CC</sub> | MIN             | TYP             | MAX | UNIT             |
|----------------------------|---|-----------------------|-----------------|-----------------|-----------------|-----|------------------|
| V <sub>CC(PGM/ERASE)</sub> | Program and erase supply voltage                    |                       |                 | 2.5             |                 | 3.6 | V                |
| f <sub>FTG</sub>           | Flash timing generator frequency                    |                       |                 | 257             |                 | 476 | kHz              |
| I <sub>PGM</sub>           | Supply current from DV <sub>CC</sub> during program |                       | 2.5V/3.6V       |                 | 3               | 5   | mA               |
| I <sub>ERASE</sub>         | Supply current from DV <sub>CC</sub> during erase   |                       | 2.5V/3.6V       |                 | 3               | 7   | mA               |
| t <sub>CPT</sub>           | Cumulative program time                             | see Note 1            | 2.5V/3.6V       |                 |                 | 10  | ms               |
| t <sub>CMErase</sub>       | Cumulative mass erase time                          | see Note 2            | 2.5V/3.6V       | 200             |                 |     | ms               |
|                            | Program/erase endurance                             |                       |                 | 10 <sup>4</sup> | 10 <sup>5</sup> |     | cycles           |
| t <sub>Retention</sub>     | Data retention duration                             | T <sub>J</sub> = 25°C |                 | 100             |                 |     | years            |
| t <sub>Word</sub>          | Word or byte program time                           | see Note 3            |                 |                 | 35              |     | t <sub>FTG</sub> |
| t <sub>Block, 0</sub>      | Block program time for 1 <sup>st</sup> byte or word |                       |                 |                 | 30              |     |                  |
| t <sub>Block, 1-63</sub>   | Block program time for each additional byte or word |                       |                 |                 | 21              |     |                  |
| t <sub>Block, End</sub>    | Block program end-sequence wait time                |                       |                 |                 | 6               |     |                  |
| t <sub>Mass Erase</sub>    | Mass erase time                                     |                       |                 |                 | 5297            |     |                  |
| t <sub>Seg Erase</sub>     | Segment erase time                                  |                       |                 |                 | 4819            |     |                  |

- NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/f<sub>FTG,max</sub> = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine (t<sub>FTG</sub> = 1/f<sub>FTG</sub>).

### JTAG interface

| PARAMETER             |   | TEST CONDITIONS | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-----------------------|---|-----------------|-----------------|-----|-----|-----|------|
| f <sub>TCK</sub>      | TCK input frequency                               | see Note 1      | 2.2 V           | 0   |     | 5   | MHz  |
|                       |   |                 | 3 V             | 0   |     | 10  | MHz  |
| R <sub>Internal</sub> | Internal pull-up resistance on TMS, TCK, TDI/TCLK | see Note 2      | 2.2 V / 3 V     | 25  | 60  | 90  | kΩ   |

- NOTES: 1. f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

### JTAG fuse (see Note 1)

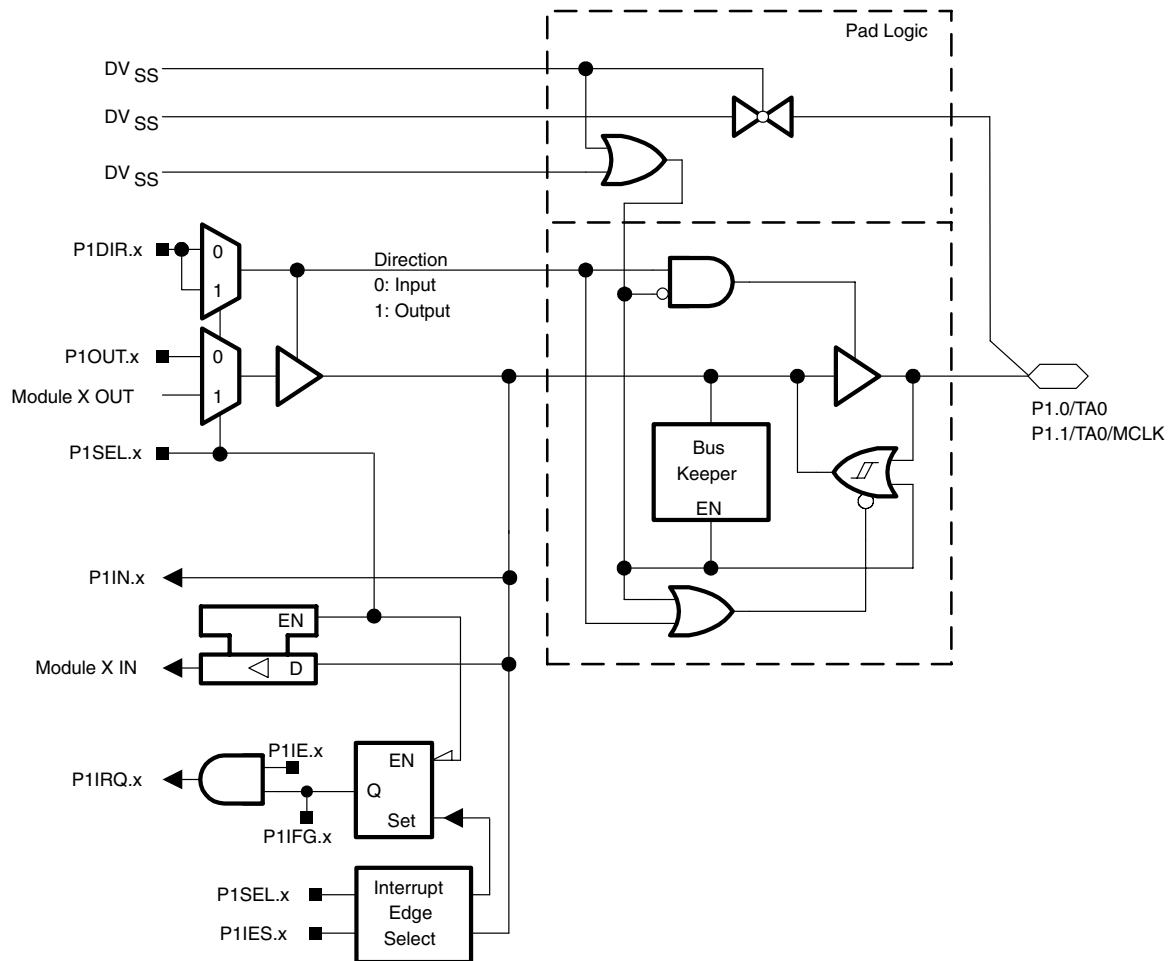
| PARAMETER           |   | TEST CONDITIONS       | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|---------------------|---|-----------------------|-----------------|-----|-----|-----|------|
| V <sub>CC(FB)</sub> | Supply voltage during fuse-blow condition           | T <sub>A</sub> = 25°C |                 | 2.5 |     |     | V    |
| V <sub>FB</sub>     | Voltage level on TDI/TCLK for fuse-blow: F versions |                       |                 | 6   |     | 7   | V    |
| I <sub>FB</sub>     | Supply current into TDI/TCLK during fuse blow       |                       |                 |     |     | 100 | mA   |
| t <sub>FB</sub>     | Time to blow fuse                                   |                       |                 |     |     | 1   | ms   |

- NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.



input/output schematics

Port P1 pin schematic: P1.0, P1.1, input/output with Schmitt trigger



Note: x = 0,1

Port P1 (P1.0, P1.1) pin functions

| PIN NAME (P1.X) | X | FUNCTION           | CONTROL BITS / SIGNALS |         |
|-----------------|---|--------------------|------------------------|---------|
|                 |   |                    | P1DIR.x                | P1SEL.x |
| P1.0/TA0        | 0 | P1.0† Input/Output | 0/1                    | 0       |
|                 |   | Timer_A3.CCI0A     | 0                      | 1       |
|                 |   | Timer_A3.TA0       | 1                      | 1       |
| P1.1/TA0/MCLK   | 1 | P1.1† Input/Output | 0/1                    | 0       |
|                 |   | Timer_A3.CCI0B     | 0                      | 1       |
|                 |   | MCLK               | 1                      | 1       |

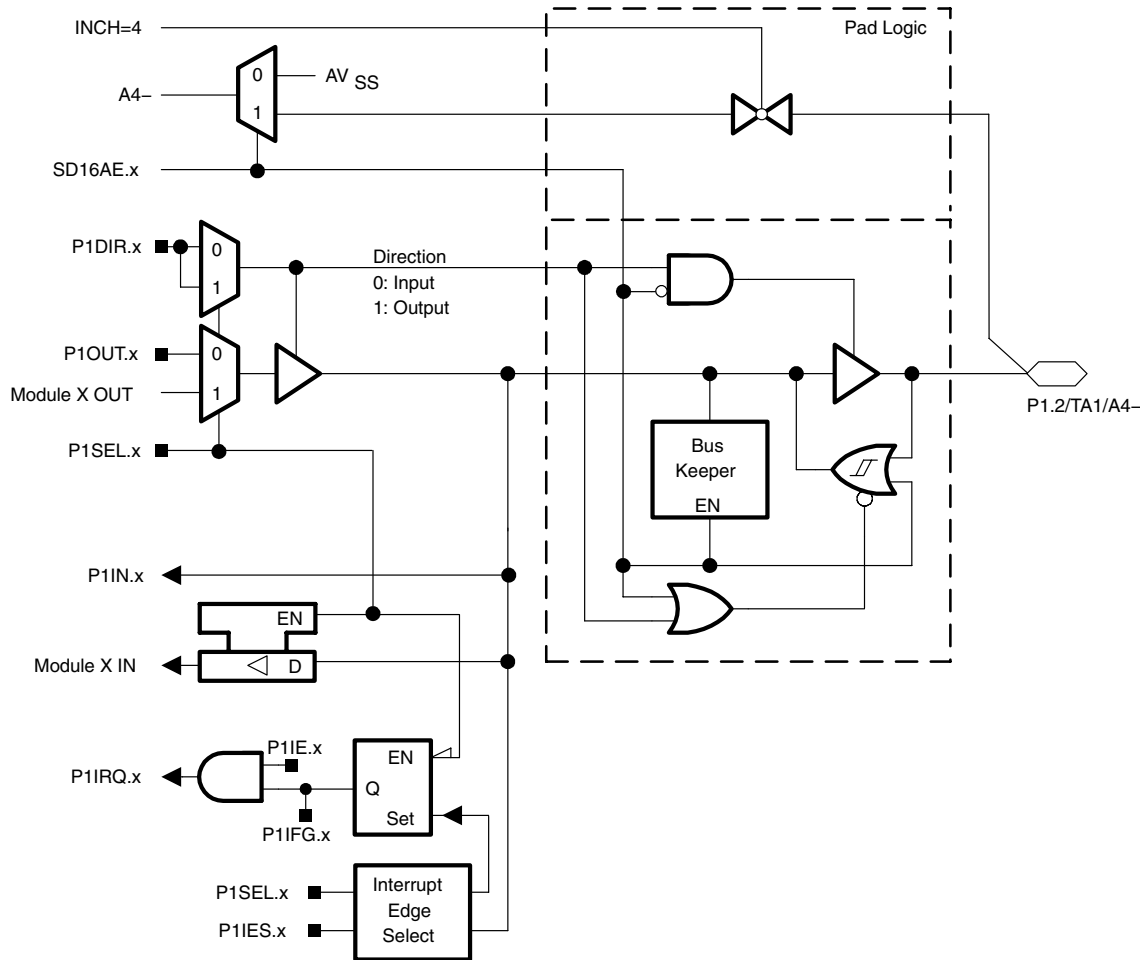
† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.  
2. X: Don't care.

# MSP430FG42x0 MIXED SIGNAL MICROCONTROLLER

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## Port P1 pin schematic: P1.2, input/output with Schmitt trigger and analog functions



Note: x = 2

### Port P1 (P1.2) pin functions

| PIN NAME (P1.X) | X | FUNCTION             | CONTROL BITS / SIGNALS |         |          |
|-----------------|---|----------------------|------------------------|---------|----------|
|                 |   |                      | P1DIR.x                | P1SEL.x | SD16AE.x |
| P1.2†/TA1/A4-   | 2 | P1.2† Input/Output   | 0/1                    | 0       | 0        |
|                 |   | Timer_A3.CCI1A       | 0                      | 1       | 0        |
|                 |   | Timer_A3.TA1         | 1                      | 1       | 0        |
|                 |   | A4- (see Notes 3, 4) | X                      | X       | 1        |

† Default after reset (PUC/POR)

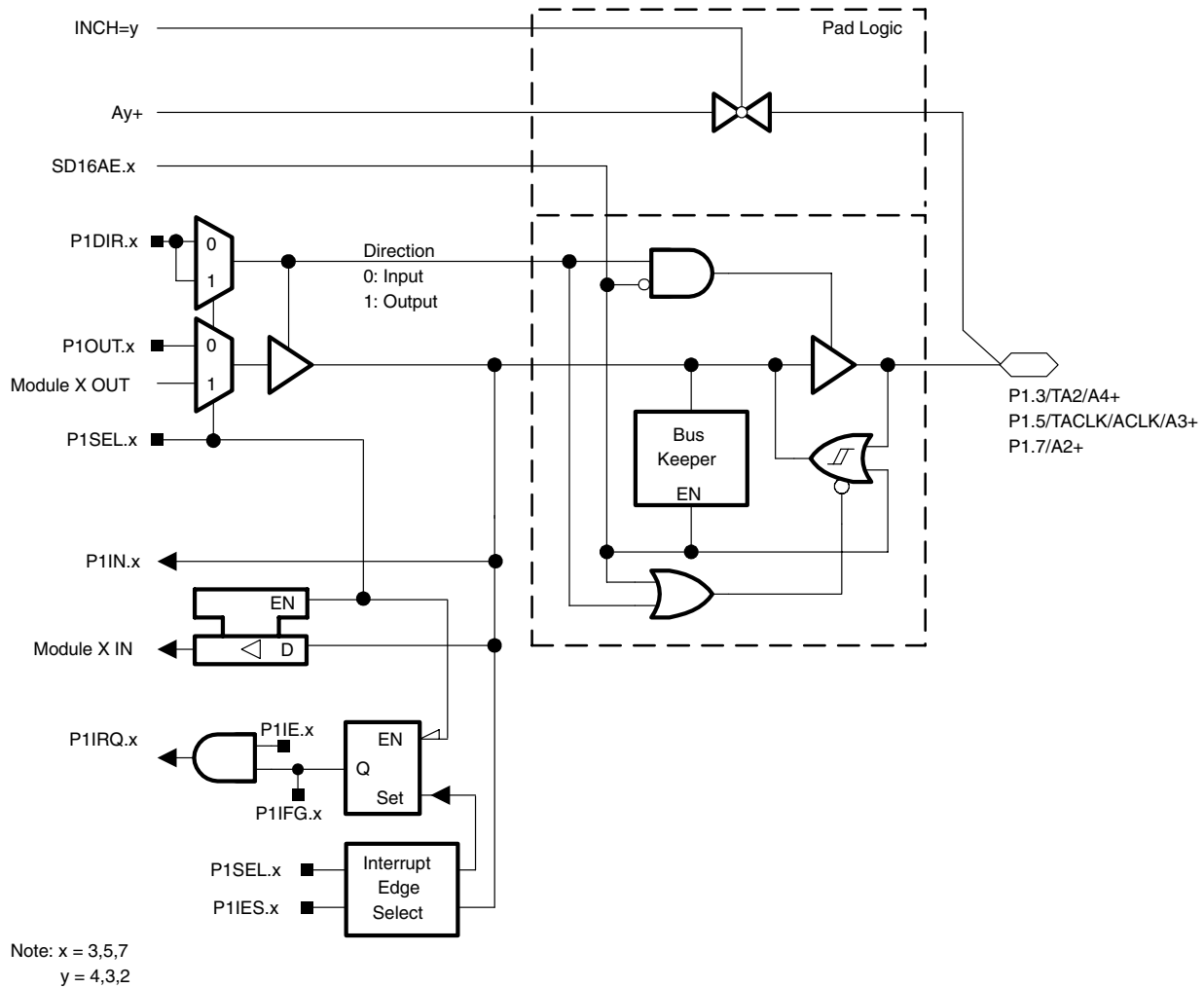
NOTES: 1. N/A: Not available or not applicable.

2. X: Don't care.

3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

4. Negative input to SD16\_A (A4-) connected to V<sub>SS</sub> if corresponding SD16AE.x bit is cleared.

Port P1 pin schematic: P1.3, P1.5, P1.7, input/output with Schmitt trigger and analog functions



# MSP430FG42x0 MIXED SIGNAL MICROCONTROLLER

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## Port P1 (P1.3, P1.5, P1.7) pin functions

| PIN NAME (P1.X)     | X | FUNCTION             | CONTROL BITS / SIGNALS |         |          |
|---------------------|---|----------------------|------------------------|---------|----------|
|                     |   |                      | P1DIR.x                | P1SEL.x | SD16AE.x |
| P1.3/TA2/A4+        | 3 | P1.3† Input/Output   | 0/1                    | 0       | 0        |
|                     |   | Timer_A3.CCI2A       | 0                      | 1       | 0        |
|                     |   | Timer_A3.TA2         | 1                      | 1       | 0        |
|                     |   | A4+ (see Note 3)     | X                      | X       | 1        |
| P1.5/TACLK/ACLK/A3+ | 5 | P1.5† Input/Output   | 0/1                    | 0       | 0        |
|                     |   | Timer_A3.TACLK/INCLK | 0                      | 1       | 0        |
|                     |   | ACLK                 | 1                      | 1       | 0        |
|                     |   | A3+ (see Note 3)     | X                      | X       | 1        |
| P1.7/A2+            | 7 | P1.5† Input/Output   | 0/1                    | 0       | 0        |
|                     |   | N/A                  | 0                      | 1       | 0        |
|                     |   | DVSS                 | 1                      | 1       | 0        |
|                     |   | A2+ (see Note 3)     | X                      | X       | 1        |

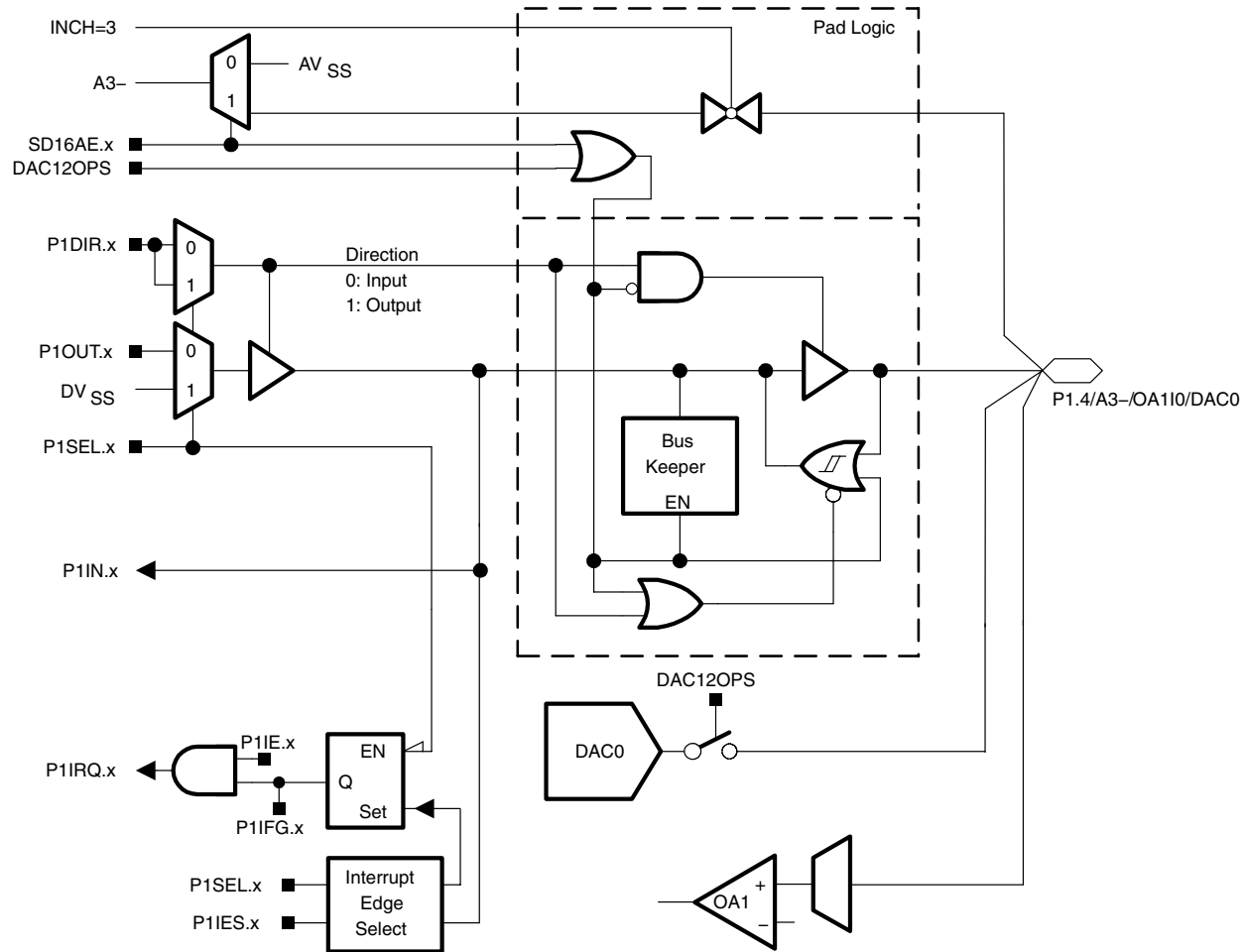
† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.

2. X: Don't care.

3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P1 pin schematic: P1.4, input/output with Schmitt trigger and analog functions



Note: x = 4

Port P1 (P1.4) pin functions

| PIN NAME (P1.X)     | X | FUNCTION             | CONTROL BITS / SIGNALS |         |          |            |          |
|---------------------|---|----------------------|------------------------|---------|----------|------------|----------|
|                     |   |                      | P1DIR.x                | P1SEL.x | SD16AE.x | OAPx (OA1) | DAC12OPS |
| P1.4/A3-/OA110/DAC0 | 4 | P1.4† Input/Output   | 0/1                    | 0       | 0        | XX         | 0        |
|                     |   | N/A                  | 0                      | 1       | 0        | XX         | 0        |
|                     |   | DVSS                 | 1                      | 1       | 0        | XX         | 0        |
|                     |   | A3- (see Notes 3, 4) | X                      | X       | 1        | XX         | 0        |
|                     |   | OA110                | X                      | X       | 1        | 00         | 0        |
|                     |   | DAC0 (see Note 5)    | X                      | X       | X        | XX         | 1        |

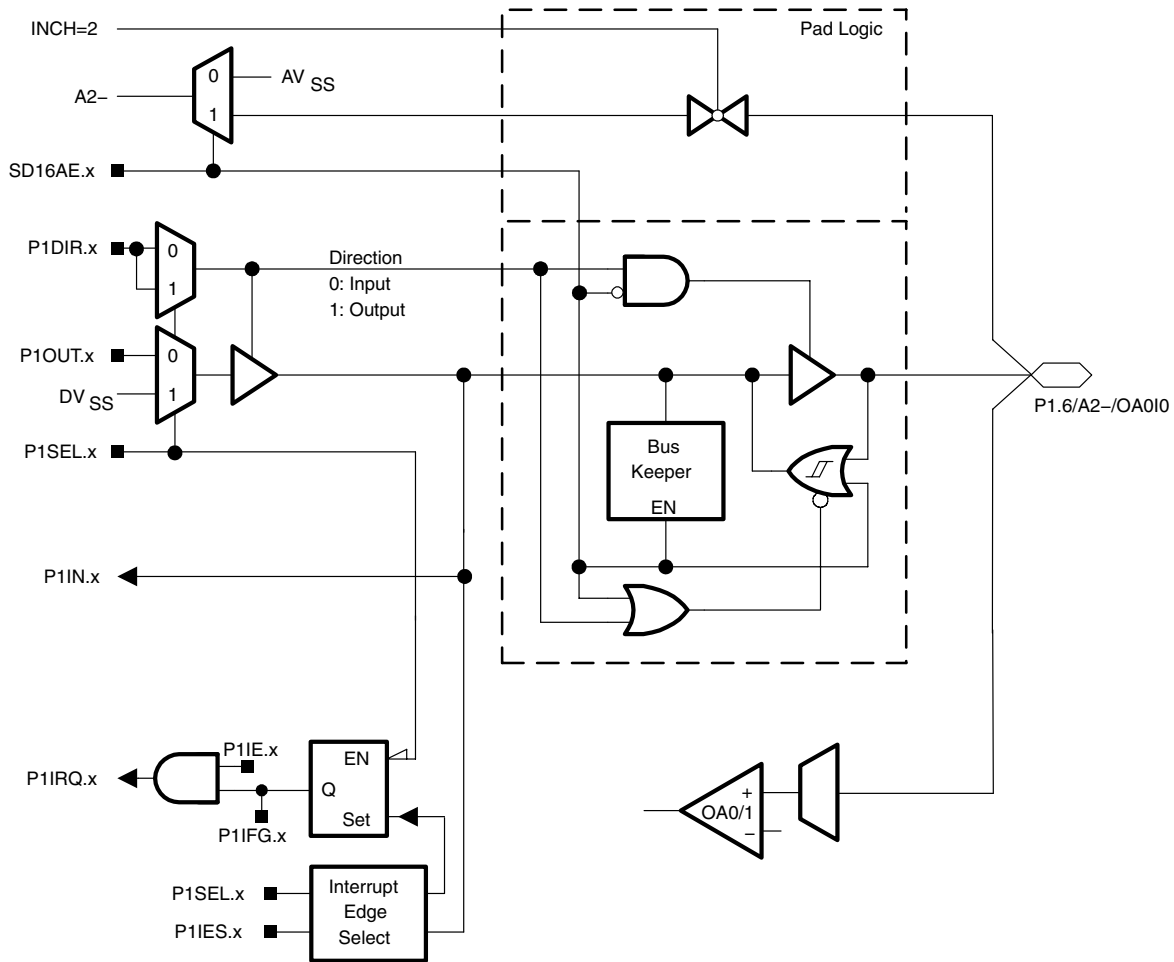
† Default after reset (PUC/POR)

- NOTES:
1. N/A: Not available or not applicable.
  2. X: Don't care.
  3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
  4. Negative input to SD16\_A (A3-) connected to AV<sub>SS</sub> if corresponding SD16AE.x bit is cleared.
  5. Setting the DAC12OPS bit also disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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## Port P1 pin schematic: P1.6, input/output with Schmitt trigger and analog functions



Note: x = 6

## Port P1 (P1.6) pin functions

| PIN NAME (P1.X) | X | FUNCTION             | CONTROL BITS / SIGNALS |         |          |            |            |
|-----------------|---|----------------------|------------------------|---------|----------|------------|------------|
|                 |   |                      | P1DIR.x                | P1SEL.x | SD16AE.x | OAPx (OA0) | OAPx (OA1) |
| P1.6/A2-/OA0/1  | 6 | P1.6† Input/Output   | 0/1                    | 0       | 0        | XX         | XX         |
|                 |   | N/A                  | 0                      | 1       | 0        | XX         | XX         |
|                 |   | DVSS                 | 1                      | 1       | 0        | XX         | XX         |
|                 |   | A2- (see Notes 3, 4) | X                      | X       | 1        | XX         | XX         |
|                 |   | OA0/1 (see Note 5)   | X                      | X       | 1        | 00 or 01   | XX         |
| X               | X |                      | 1                      | XX      | 01       |            |            |

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.

2. X: Don't care.

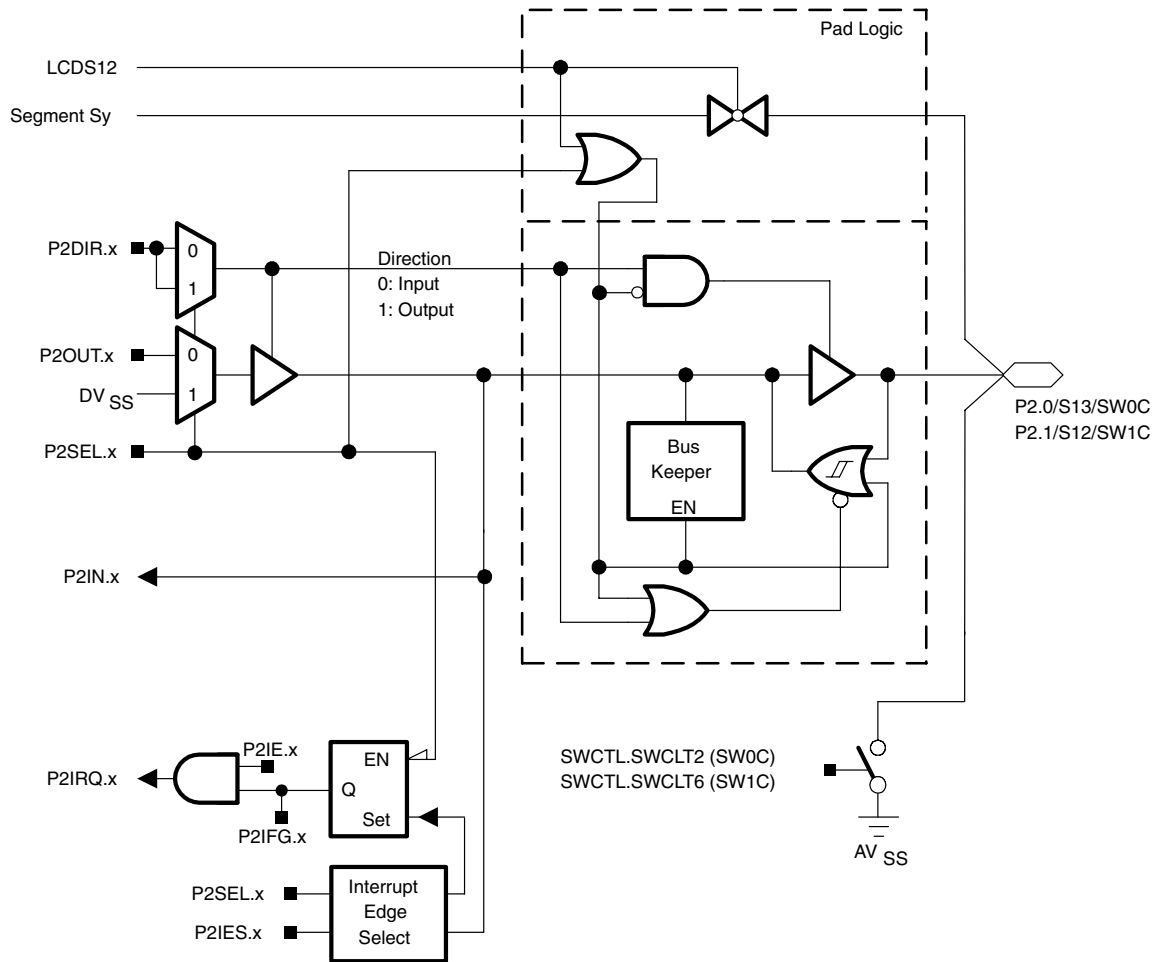
3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

4. Negative input to SD16\_A (A2-) connected to AVSS if corresponding SD16AE.x bit is cleared.

5. OA0/1 connected to pin if for OA0 the OAPx bits are cleared or set to 01, or if for OA1 the OAPx bits are set to 01.



Port P2 pin schematic: P2.0 to P2.1, input/output with Schmitt trigger, LCD and analog functions



Note: x = 0,1  
y = 13,12

Port P2 (P2.0, P2.1) pin functions

| PIN NAME (P2.X) | X | FUNCTION              | CONTROL BITS / SIGNALS |         |        |
|-----------------|---|-----------------------|------------------------|---------|--------|
|                 |   |                       | P2DIR.x                | P2SEL.x | LCDS12 |
| P2.0/S13/SW0C   | 0 | P2.0† Input/Output    | 0/1                    | 0       | 0      |
|                 |   | SW0C (see Notes 3, 4) | X                      | 1       | 0      |
|                 |   | S13                   | X                      | X       | 1      |
| P2.1/S12/SW1C   | 1 | P2.1† Input/Output    | 0/1                    | 0       | 0      |
|                 |   | SW1C (see Notes 3, 4) | X                      | 1       | 0      |
|                 |   | S12                   | X                      | X       | 1      |

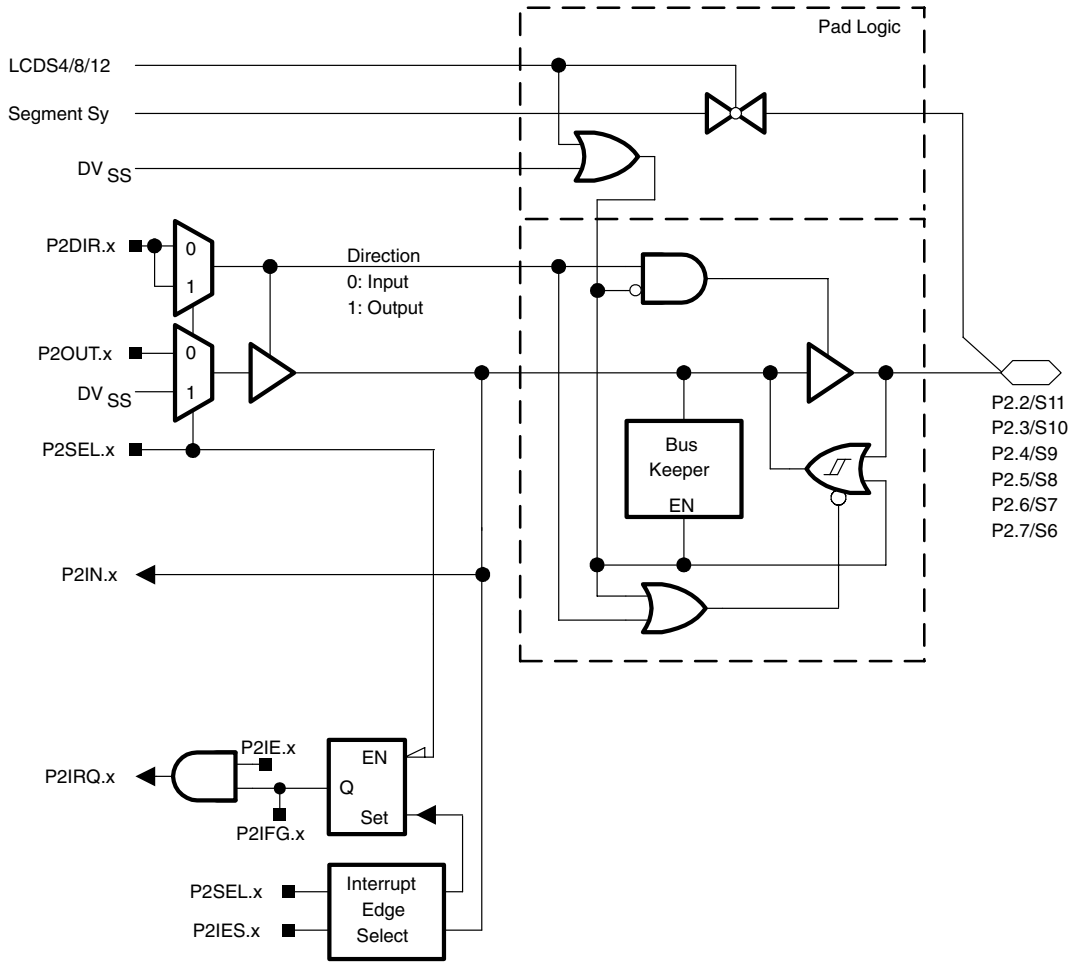
† Default after reset (PUC/POR)

- NOTES:
1. N/A: Not available or not applicable.
  2. X: Don't care.
  3. Setting the P2SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
  4. The low impedance switch to ground is closed by setting the corresponding bits in SWCTL register.

# MSP430FG42x0 MIXED SIGNAL MICROCONTROLLER

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## Port P2 pin schematic: P2.2 to P2.7, input/output with Schmitt trigger, LCD and analog functions



Note: x = 2 to 7  
y = 11 to 6

**Port P2 (P2.0 to P2.7) pin functions**

| PIN NAME (P2.X) | X | FUNCTION           | CONTROL BITS / SIGNALS |         |        |
|-----------------|---|--------------------|------------------------|---------|--------|
|                 |   |                    | P2DIR.x                | P2SEL.x | LCDS12 |
| P2.2/S11        | 2 | P2.2† Input/Output | 0/1                    | 0       | 0      |
|                 |   | N/A                | 0                      | 1       | 0      |
|                 |   | DVSS               | 1                      | 1       | 0      |
|                 |   | S11                | X                      | X       | 1      |
| P2.3/S10        | 3 | P2.3† Input/Output | 0/1                    | 0       | 0      |
|                 |   | N/A                | 0                      | 1       | 0      |
|                 |   | DVSS               | 1                      | 1       | 0      |
|                 |   | S10                | X                      | X       | 1      |
| P2.4/S9         | 4 | P2.4† Input/Output | 0/1                    | 0       | 0      |
|                 |   | N/A                | 0                      | 1       | 0      |
|                 |   | DVSS               | 1                      | 1       | 0      |
|                 |   | S9                 | X                      | X       | 1      |
| P2.5/S8         | 5 | P2.5† Input/Output | 0/1                    | 0       | 0      |
|                 |   | N/A                | 0                      | 1       | 0      |
|                 |   | DVSS               | 1                      | 1       | 0      |
|                 |   | S8                 | X                      | X       | 1      |
| P2.6/S7         | 6 | P2.6† Input/Output | 0/1                    | 0       | 0      |
|                 |   | N/A                | 0                      | 1       | 0      |
|                 |   | DVSS               | 1                      | 1       | 0      |
|                 |   | S7                 | X                      | X       | 1      |
| P2.7/S6         | 7 | P2.7† Input/Output | 0/1                    | 0       | 0      |
|                 |   | N/A                | 0                      | 1       | 0      |
|                 |   | DVSS               | 1                      | 1       | 0      |
|                 |   | S6                 | X                      | X       | 1      |

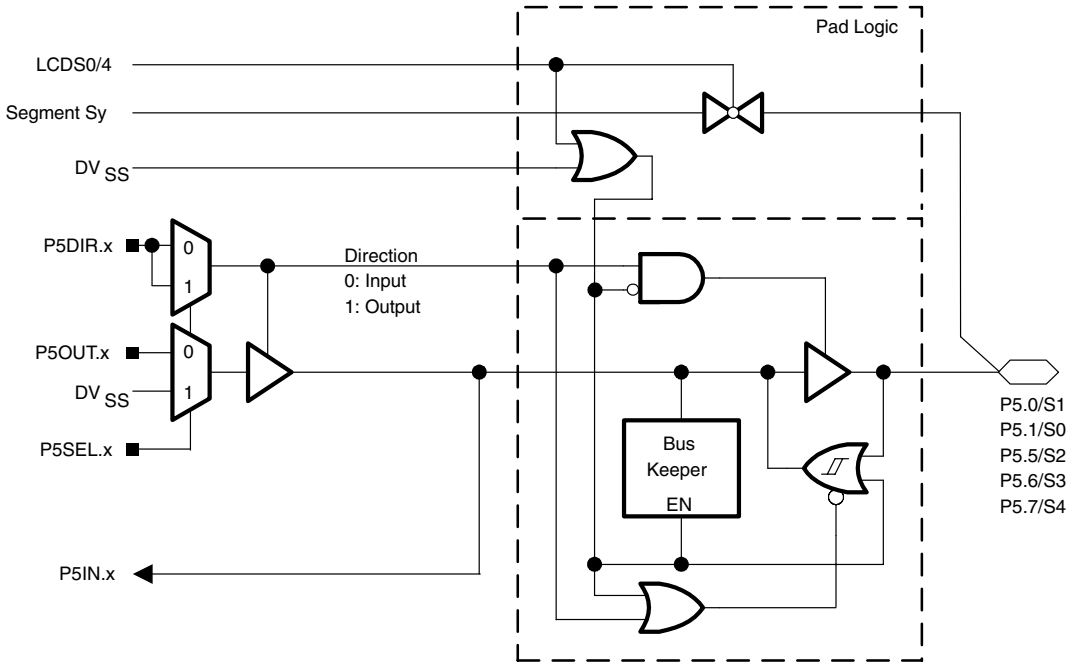
† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.  
2. X: Don't care.

# MSP430FG42x0 MIXED SIGNAL MICROCONTROLLER

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## Port P5 pin schematic: P5.0, P5.1, P5.5 to P5.7, input/output with Schmitt trigger and LCD functions



Note: x = 0,1,5,6,7  
y = 1,0,2,3,4

**Port P5 (P5.0, P5.1, P5.5, P5.6) pin functions**

| PIN NAME (P5.X) | X | FUNCTION           | CONTROL BITS / SIGNALS |         |       |
|-----------------|---|--------------------|------------------------|---------|-------|
|                 |   |                    | P5DIR.x                | P5SEL.x | LCDS0 |
| P5.0/S1         | 0 | P5.0† Input/Output | 0/1                    | 0       | 0     |
|                 |   | N/A                | 0                      | 1       | 0     |
|                 |   | DVSS               | 1                      | 1       | 0     |
|                 |   | S1                 | X                      | X       | 1     |
| P5.1/S0         | 1 | P5.1† Input/Output | 0/1                    | 0       | 0     |
|                 |   | N/A                | 0                      | 1       | 0     |
|                 |   | DVSS               | 1                      | 1       | 0     |
|                 |   | S0                 | X                      | X       | 1     |
| P5.5/S2         | 5 | P5.5† Input/Output | 0/1                    | 0       | 0     |
|                 |   | N/A                | 0                      | 1       | 0     |
|                 |   | DVSS               | 1                      | 1       | 0     |
|                 |   | S2                 | X                      | X       | 1     |
| P5.6/S3         | 6 | P5.6† Input/Output | 0/1                    | 0       | 0     |
|                 |   | N/A                | 0                      | 1       | 0     |
|                 |   | DVSS               | 1                      | 1       | 0     |
|                 |   | S3                 | X                      | X       | 1     |

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.  
2. X: Don't care.

**Port P5 (P5.7) pin functions**

| PIN NAME (P5.X) | X | FUNCTION           | CONTROL BITS / SIGNALS |         |       |
|-----------------|---|--------------------|------------------------|---------|-------|
|                 |   |                    | P5DIR.x                | P5SEL.x | LCDS4 |
| P5.7/S4         | 7 | P5.7† Input/Output | 0/1                    | 0       | 0     |
|                 |   | N/A                | 0                      | 1       | 0     |
|                 |   | DVSS               | 1                      | 1       | 0     |
|                 |   | S4                 | X                      | X       | 1     |

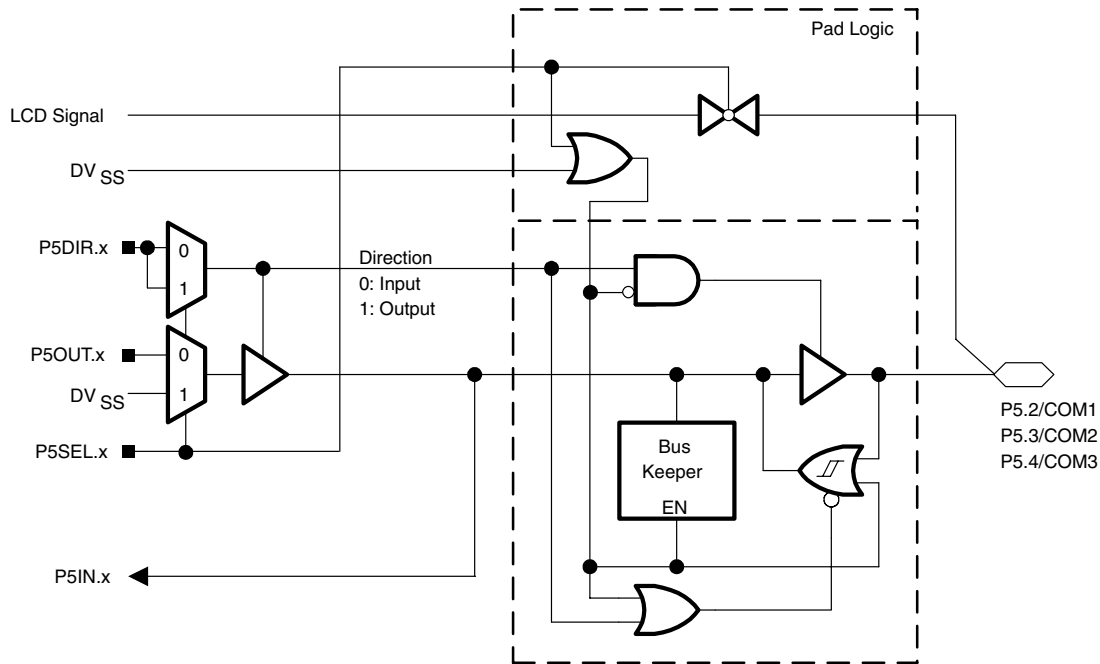
† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.  
2. X: Don't care.

# MSP430FG42x0 MIXED SIGNAL MICROCONTROLLER

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## Port P5 pin schematic: P5.2 to P5.4, input/output with Schmitt trigger and LCD functions



Note: x = 2 to 4

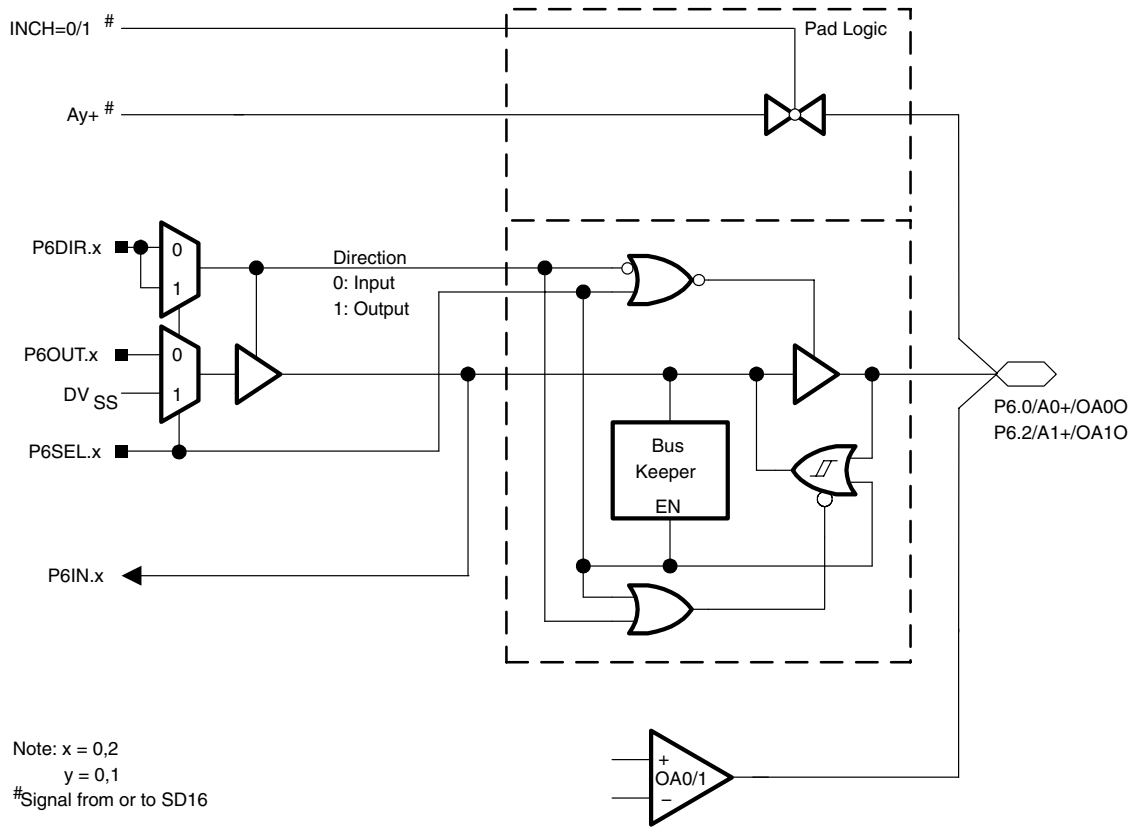
### Port P5 (P5.2 to P5.4) pin functions

| PIN NAME (P5.X) | X | FUNCTION           | CONTROL BITS / SIGNALS |         |
|-----------------|---|--------------------|------------------------|---------|
|                 |   |                    | P5DIR.x                | P5SEL.x |
| P5.2/COM1       | 2 | P5.2† Input/Output | 0/1                    | 0       |
|                 |   | COM1               | X                      | 1       |
| P5.3/COM2       | 3 | P5.3† Input/Output | 0/1                    | 0       |
|                 |   | COM2               | X                      | 1       |
| P5.4/COM3       | 4 | P5.4† Input/Output | 0/1                    | 0       |
|                 |   | COM3               | X                      | 1       |

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.  
2. X: Don't care.

Port P6 pin schematic: P6.0, P6.2, input/output with Schmitt trigger and analog functions



Note: x = 0,2  
y = 0,1  
#Signal from or to SD16

Port P6 (P6.0, P6.2) pin functions

| PIN NAME (P6.X) | X | FUNCTION              | CONTROL BITS / SIGNALS |         |
|-----------------|---|-----------------------|------------------------|---------|
|                 |   |                       | P6DIR.x                | P6SEL.x |
| P6.0/A0+/OA00   | 0 | P6.0† Input/Output    | 0/1                    | 0       |
|                 |   | A0+/OA00 (see Note 3) | X                      | 1       |
| P6.2/A1+/OA10   | 2 | P6.2† Input/Output    | 0/1                    | 0       |
|                 |   | A1+/OA10 (see Note 3) | X                      | 1       |

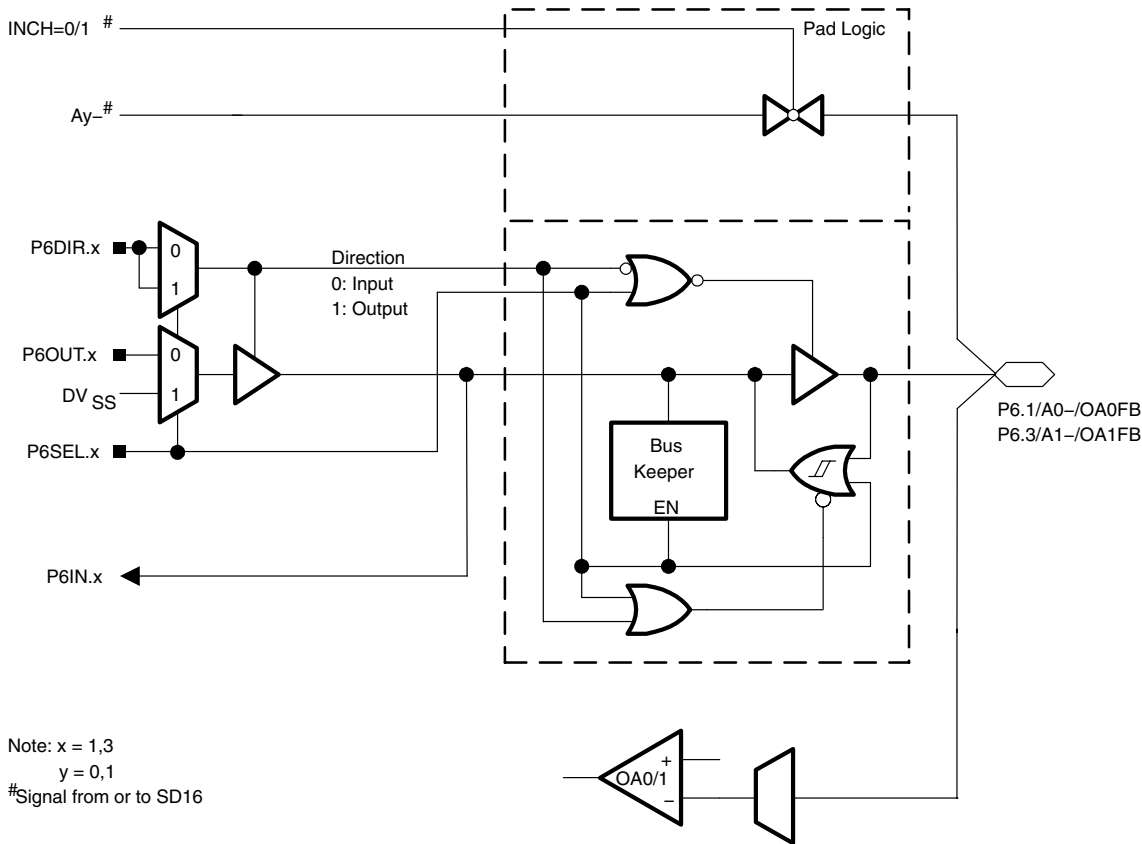
† Default after reset (PUC/POR)

- NOTES:
1. N/A: Not available or not applicable.
  2. X: Don't care.
  3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

# MSP430FG42x0 MIXED SIGNAL MICROCONTROLLER

SLAS556A – JULY 2007 – REVISED AUGUST 2007

## Port P6 pin schematic: P6.1, P6.3, input/output with Schmitt trigger and analog functions



### Port P6 (P6.1, P6.3) pin functions

| PIN NAME (P6.X) | X | FUNCTION               | CONTROL BITS / SIGNALS |         |
|-----------------|---|------------------------|------------------------|---------|
|                 |   |                        | P6DIR.x                | P6SEL.x |
| P6.1/A0-/OA0FB  | 1 | P6.1† Input/Output     | 0/1                    | 0       |
|                 |   | A0-/OA0FB (see Note 3) | X                      | 1       |
| P6.3/A1-/OA1FB  | 3 | P6.3† Input/Output     | 0/1                    | 0       |
|                 |   | A1-/OA1FB (see Note 3) | X                      | 1       |

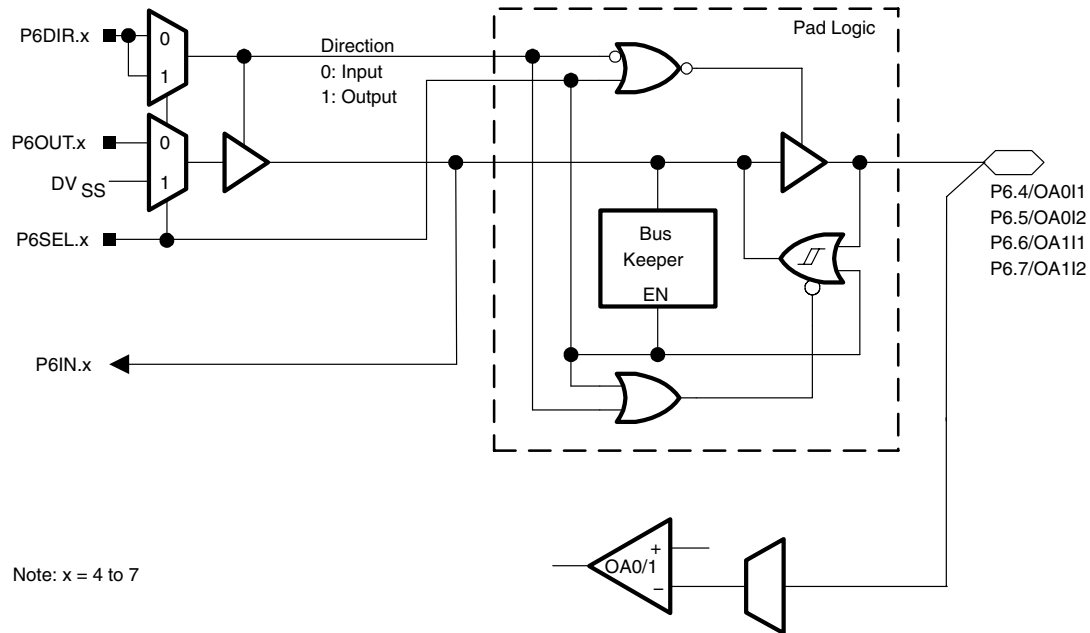
† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.

2. X: Don't care.

3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P6 pin schematic: P6.4 to P6.7, input/output with Schmitt trigger and analog functions



Port P6 (P6.4 to P6.7) pin functions

| PIN NAME (P6.X) | X | FUNCTION           | CONTROL BITS / SIGNALS |         |
|-----------------|---|--------------------|------------------------|---------|
|                 |   |                    | P6DIR.x                | P6SEL.x |
| P6.4/OA011      | 4 | P6.4† Input/Output | 0/1                    | 0       |
|                 |   | OA011 (see Note 3) | X                      | 1       |
| P6.5/OA012      | 5 | P6.5† Input/Output | 0/1                    | 0       |
|                 |   | OA012 (see Note 3) | X                      | 1       |
| P6.6/OA111      | 6 | P6.6† Input/Output | 0/1                    | 0       |
|                 |   | OA111 (see Note 3) | X                      | 1       |
| P6.7/OA112      | 7 | P6.7† Input/Output | 0/1                    | 0       |
|                 |   | OA112 (see Note 3) | X                      | 1       |

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.

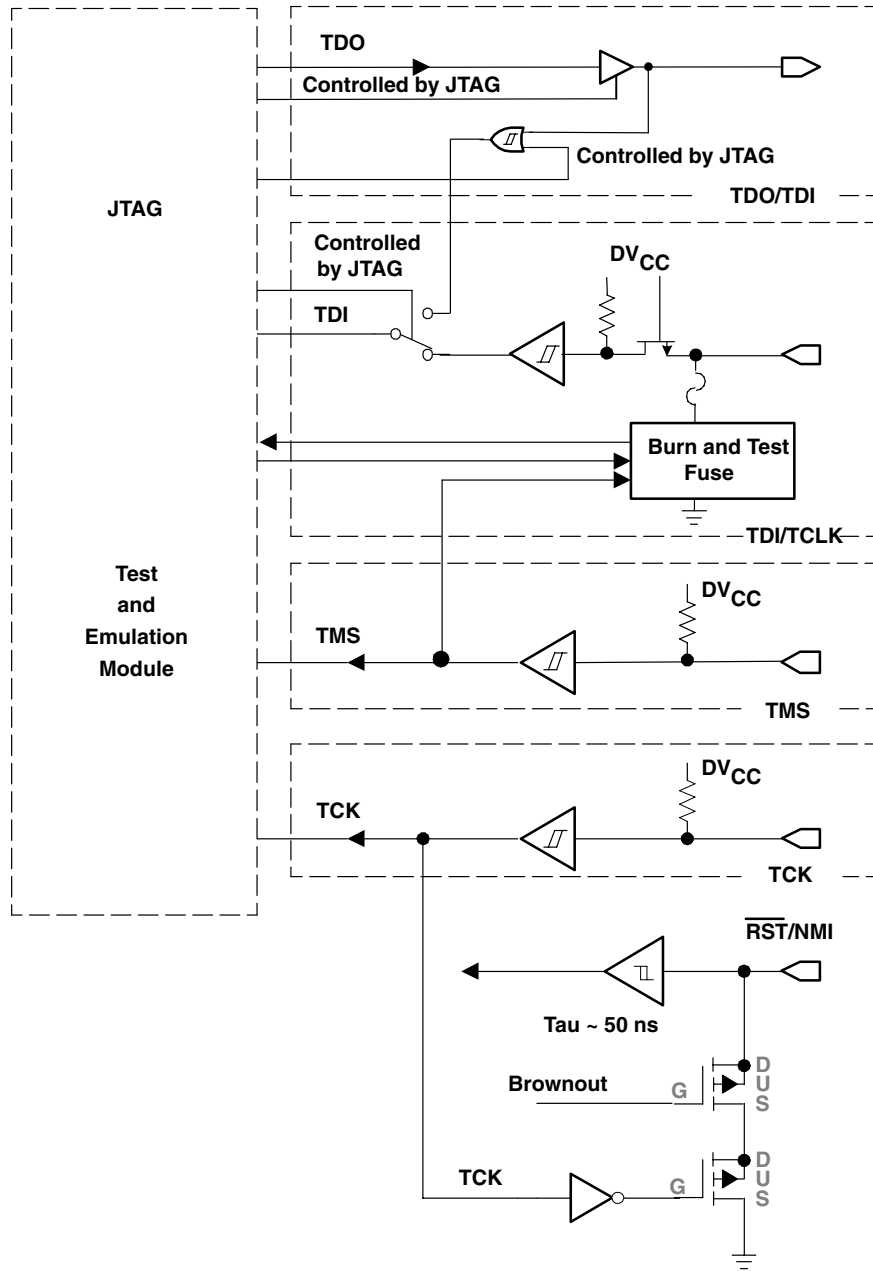
2. X: Don't care.

3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

# MSP430FG42x0 MIXED SIGNAL MICROCONTROLLER

SLAS556A – JULY 2007 – REVISED AUGUST 2007

## JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt trigger or output



## JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current ( $I_{(TF)}$ ) of 1 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 21). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and therefore do not require external termination.

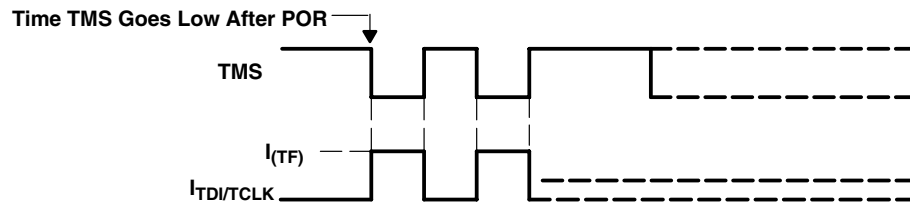


Figure 21. Fuse Check Mode Current

# MSP430FG42x0 MIXED SIGNAL MICROCONTROLLER

SLAS556A – JULY 2007 – REVISED AUGUST 2007

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## Data Sheet Revision History

| Literature Number | Summary                            |
|-------------------|------------------------------------|
| SLAS556           | Product Preview data sheet release |
| SLAS556A          | Production Data data sheet release |

NOTE: Page and figure numbers refer to the respective document revision.



## **Corrections to MSP430FG42x0 Data Sheet (SLAS556A)**

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Document Being Updated: *MSP430FG42x0 Mixed Signal Microcontroller*

Literature Number Being Updated: SLAS556A

**Page Change or Add**

- 48 At the top left of the image, *LCDS4/8/12* should be changed to **LCDS4, LCDS8**.
- 49 The table includes *LCDS12* in the "CONTROL BITS / SIGNALS" column.  
For P2.2/S11, P2.3/S10, P2.4/S9, and P2.5/S8, the correct control bit is **LCDS8**.  
For P2.6/S7 and P2.7/S6, the correct control bit is **LCDS4**.

**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430FG4250IDL   | ACTIVE        | SSOP         | DL              | 48   | 25          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | M430FG4250              | <a href="#">Samples</a> |
| MSP430FG4250IDLR  | ACTIVE        | SSOP         | DL              | 48   | 1000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | M430FG4250              | <a href="#">Samples</a> |
| MSP430FG4250IRGZR | ACTIVE        | VQFN         | RGZ             | 48   | 2500        | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | M430<br>FG4250          | <a href="#">Samples</a> |
| MSP430FG4250IRGZT | ACTIVE        | VQFN         | RGZ             | 48   | 250         | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | M430<br>FG4250          | <a href="#">Samples</a> |
| MSP430FG4260IDLR  | ACTIVE        | SSOP         | DL              | 48   | 1000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | M430FG4260              | <a href="#">Samples</a> |
| MSP430FG4260IRGZR | ACTIVE        | VQFN         | RGZ             | 48   | 2500        | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | M430<br>FG4260          | <a href="#">Samples</a> |
| MSP430FG4270IDL   | ACTIVE        | SSOP         | DL              | 48   | 25          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | M430FG4270              | <a href="#">Samples</a> |
| MSP430FG4270IDLR  | ACTIVE        | SSOP         | DL              | 48   | 1000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | M430FG4270              | <a href="#">Samples</a> |
| MSP430FG4270IRGZR | ACTIVE        | VQFN         | RGZ             | 48   | 2500        | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | M430<br>FG4270          | <a href="#">Samples</a> |
| MSP430FG4270IRGZT | ACTIVE        | VQFN         | RGZ             | 48   | 250         | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | M430<br>FG4270          | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

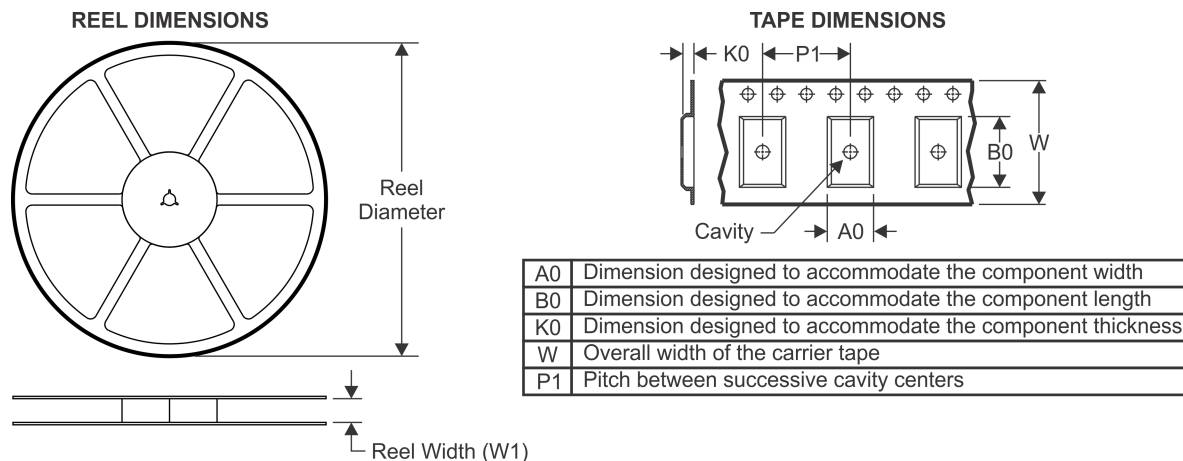
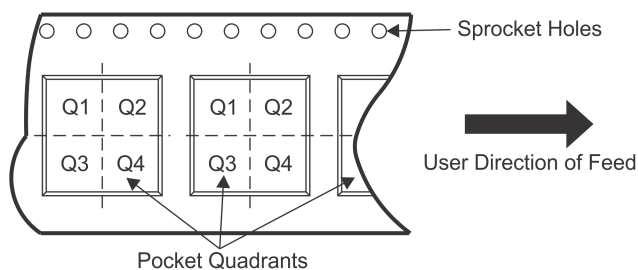
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

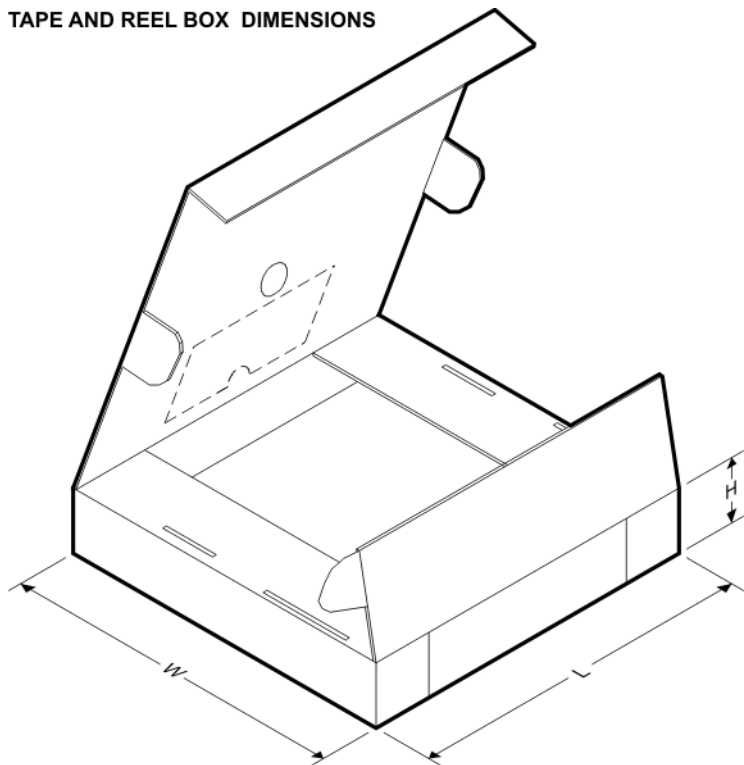
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


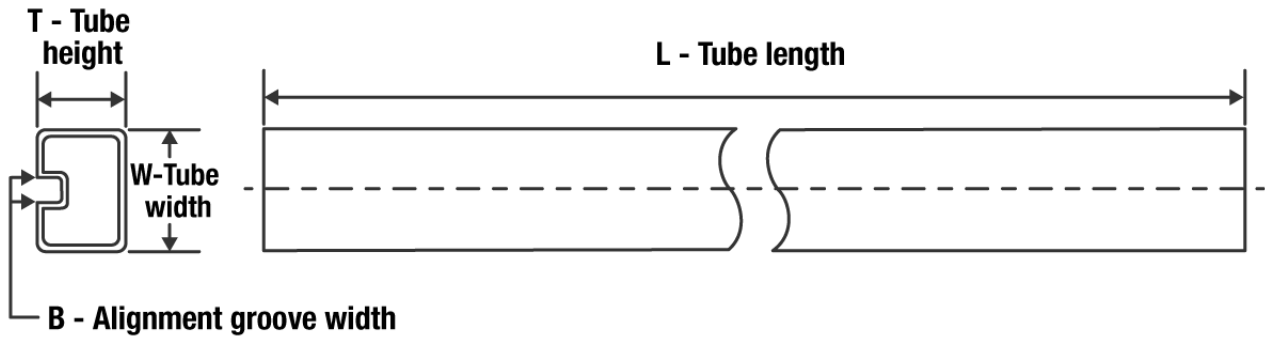
\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430FG4250IDLR  | SSOP         | DL              | 48   | 1000 | 330.0              | 32.4               | 11.35   | 16.2    | 3.1     | 16.0    | 32.0   | Q1            |
| MSP430FG4250IRGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q2            |
| MSP430FG4250IRGZT | VQFN         | RGZ             | 48   | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q2            |
| MSP430FG4260IDLR  | SSOP         | DL              | 48   | 1000 | 330.0              | 32.4               | 11.35   | 16.2    | 3.1     | 16.0    | 32.0   | Q1            |
| MSP430FG4260IRGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q2            |
| MSP430FG4270IDLR  | SSOP         | DL              | 48   | 1000 | 330.0              | 32.4               | 11.35   | 16.2    | 3.1     | 16.0    | 32.0   | Q1            |
| MSP430FG4270IRGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q2            |
| MSP430FG4270IRGZT | VQFN         | RGZ             | 48   | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430FG4250IDLR  | SSOP         | DL              | 48   | 1000 | 367.0       | 367.0      | 55.0        |
| MSP430FG4250IRGZR | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| MSP430FG4250IRGZT | VQFN         | RGZ             | 48   | 250  | 210.0       | 185.0      | 35.0        |
| MSP430FG4260IDLR  | SSOP         | DL              | 48   | 1000 | 367.0       | 367.0      | 55.0        |
| MSP430FG4260IRGZR | VQFN         | RGZ             | 48   | 2500 | 853.0       | 449.0      | 35.0        |
| MSP430FG4270IDLR  | SSOP         | DL              | 48   | 1000 | 367.0       | 367.0      | 55.0        |
| MSP430FG4270IRGZR | VQFN         | RGZ             | 48   | 2500 | 853.0       | 449.0      | 35.0        |
| MSP430FG4270IRGZT | VQFN         | RGZ             | 48   | 250  | 210.0       | 185.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| MSP430FG4250IDL | DL           | SSOP         | 48   | 25  | 473.7  | 14.24  | 5110   | 7.87   |
| MSP430FG4270IDL | DL           | SSOP         | 48   | 25  | 473.7  | 14.24  | 5110   | 7.87   |

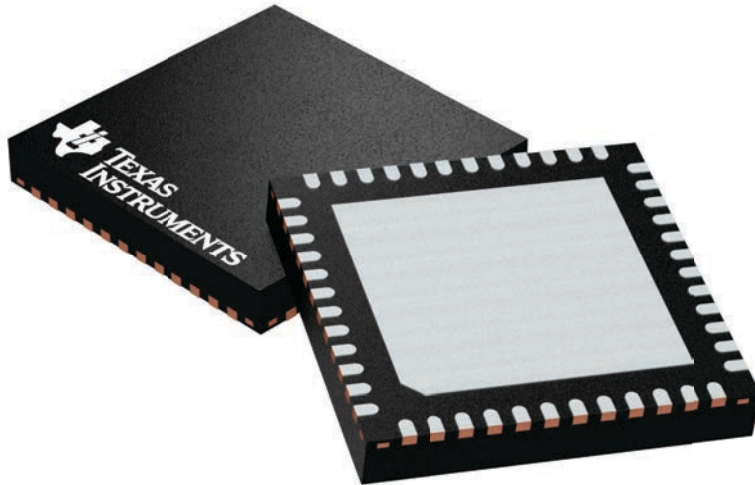
## GENERIC PACKAGE VIEW

**RGZ 48**

**VQFN - 1 mm max height**

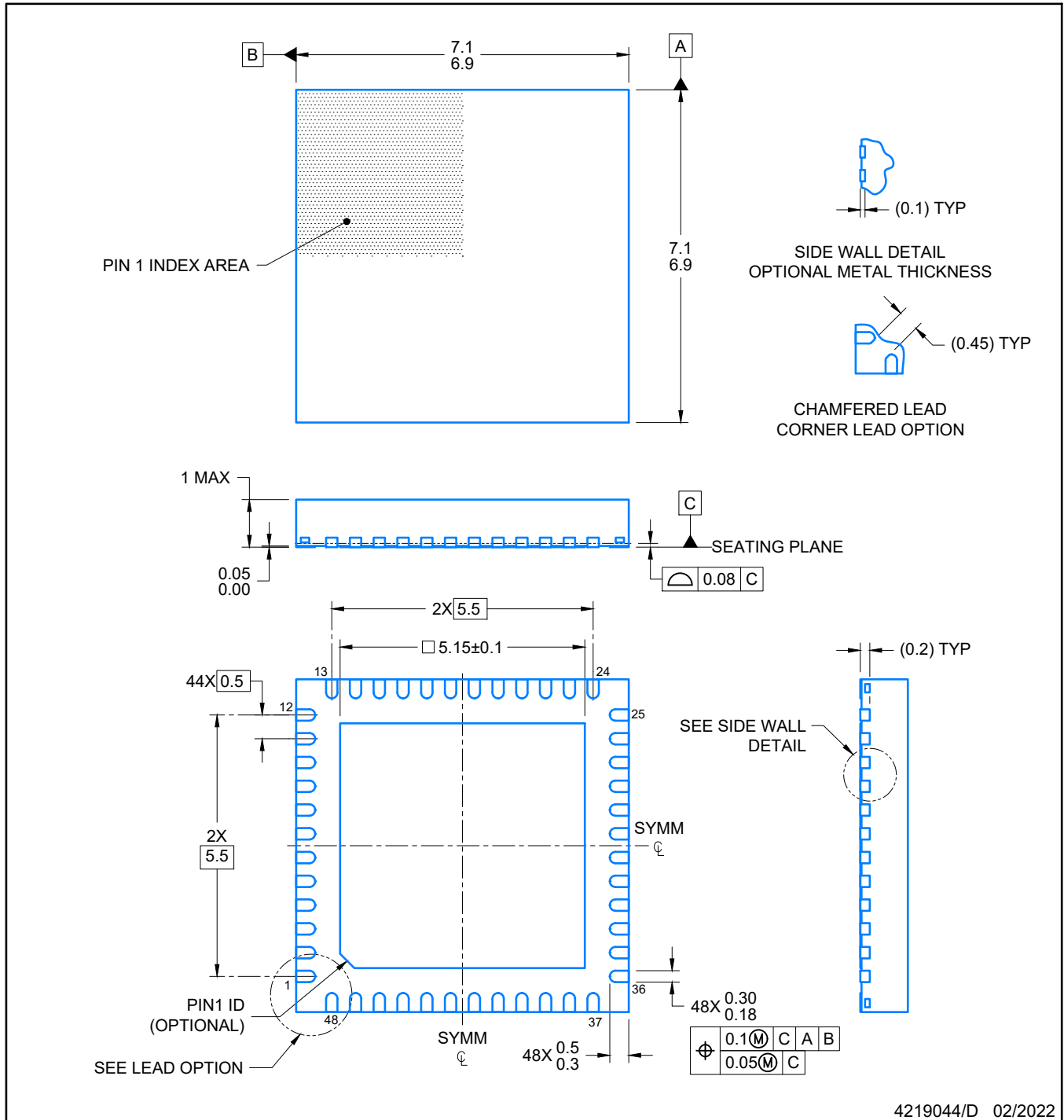
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



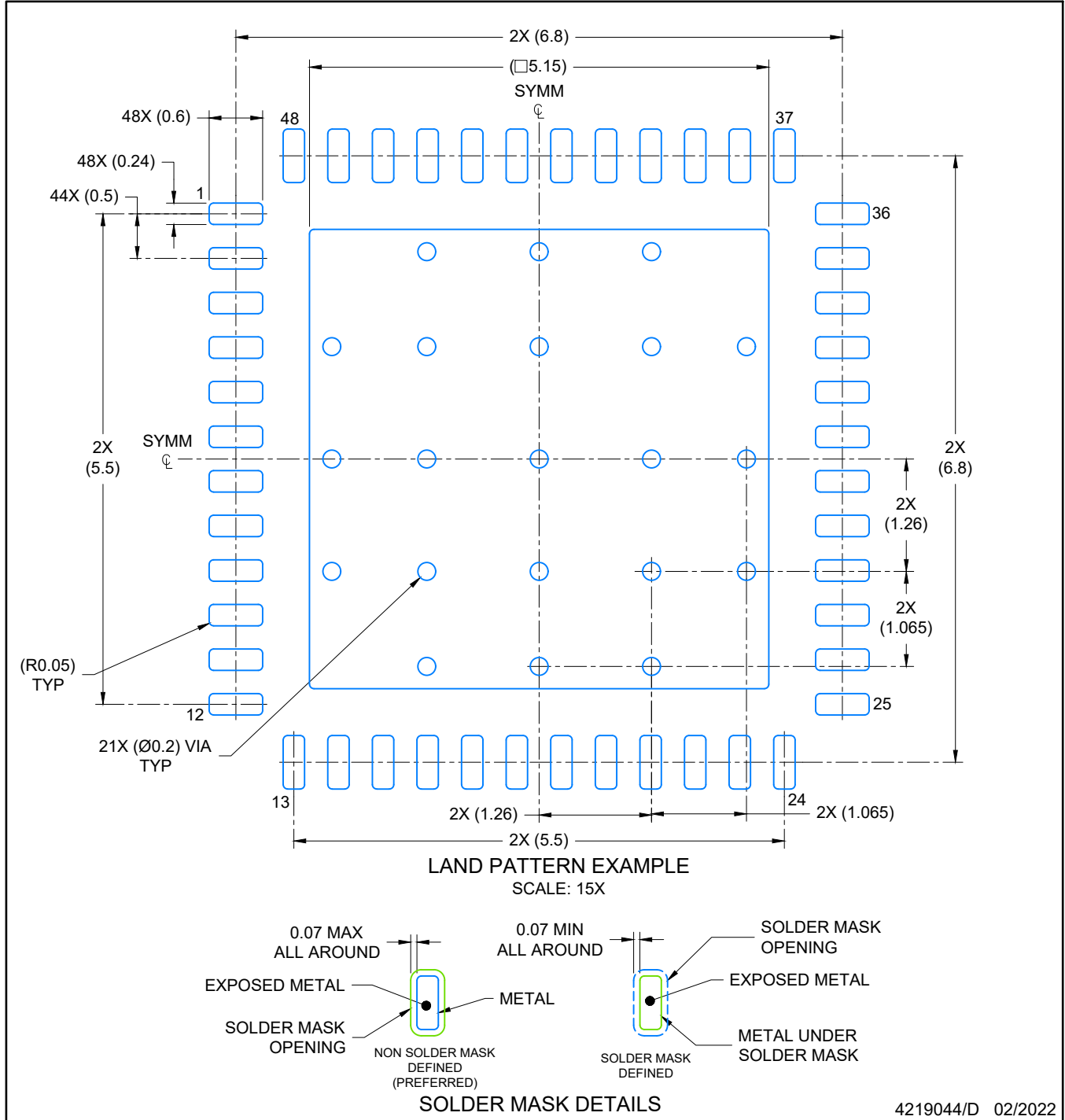
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224671/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

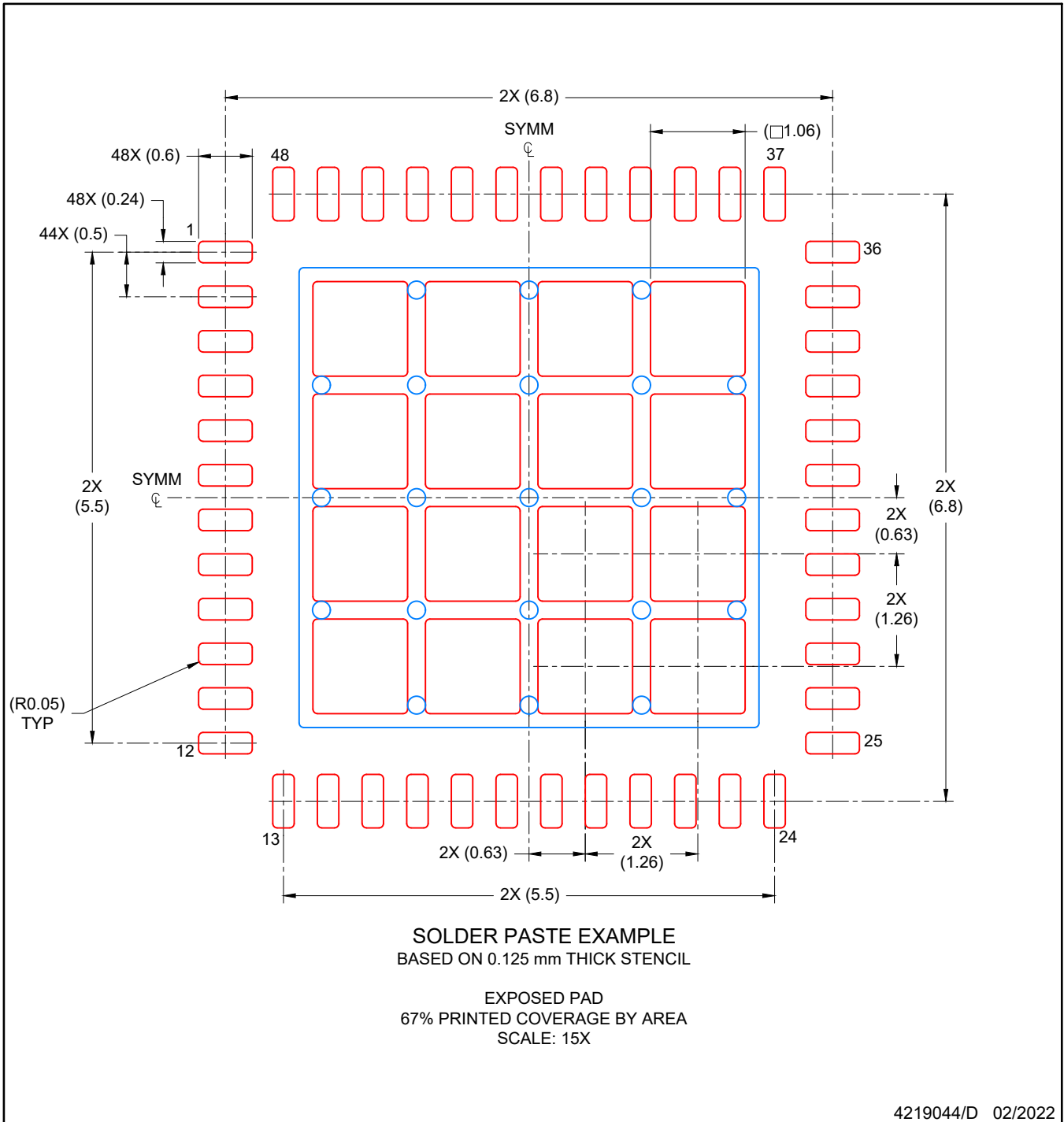
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGZ0048A

VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



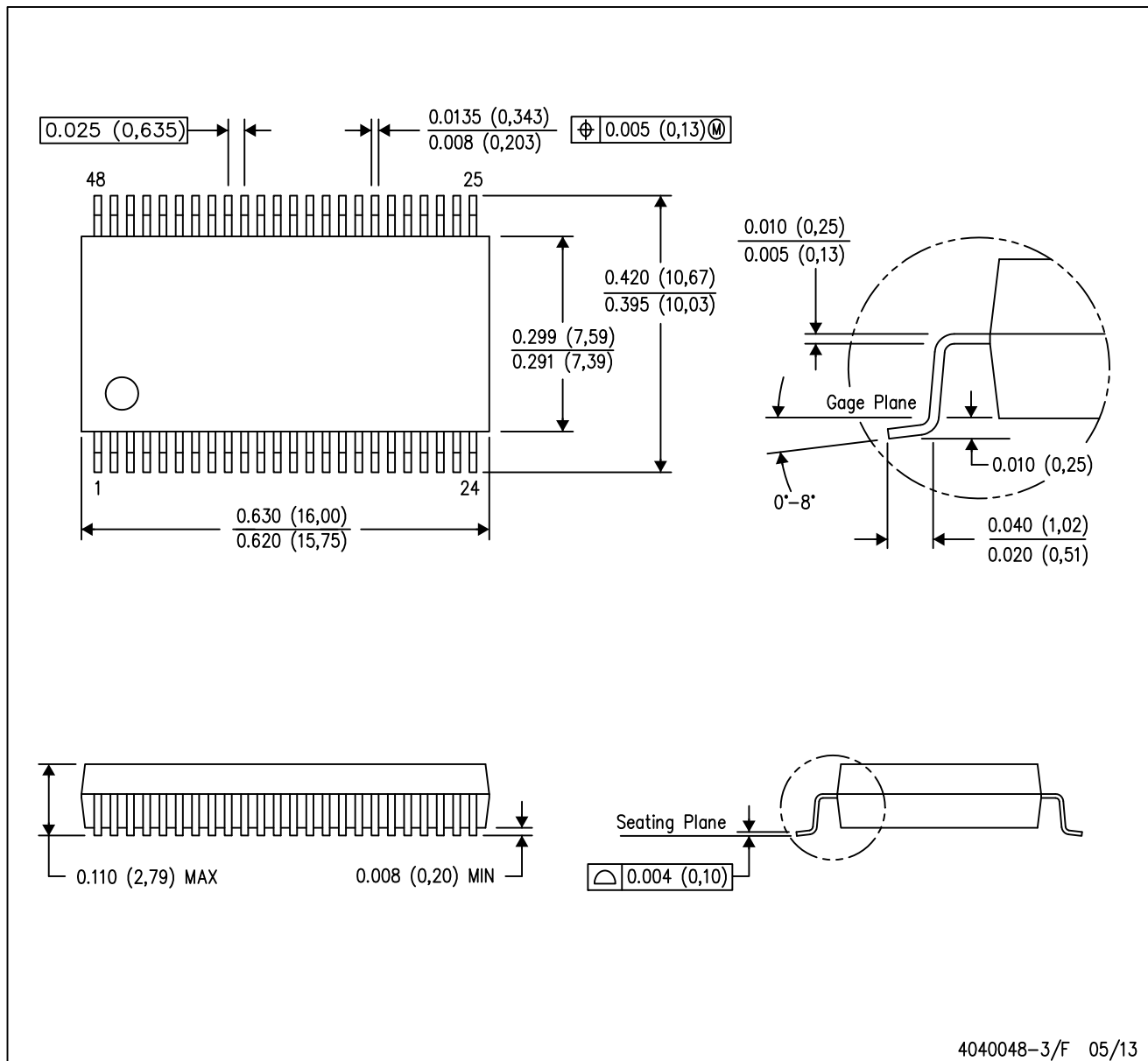
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

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