

## SNx4LVC14A Hex Schmitt-trigger inverters

### 1 Features

- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000-V human-body model (A114-A)
  - 200-V machine model (A115-A)
  - 1000-V charged-device model (C101)
- Operate from 1.65 V to 3.6 V  $V_{CC}$
- Specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , and  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Inputs accept voltages to 5.5 V
- Max  $t_{pd}$  of 6.4 ns at 3.3 V
- Typical  $V_{OLP}$  (output ground bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $>2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}\text{C}$
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

### 2 Applications

- Barcode scanner
- Cable solutions
- E-books
- Embedded PCs
- Field transmitter: temperature or pressure sensors
- Fingerprint biometrics
- HVAC: heating, ventilating, and air conditioning
- Network-attached storage (NAS)
- Server motherboard and PSU
- Software defined radio (SDR)
- TV: High-definition (HDTV), LCD, and digital
- Video communications systems
- Wireless data access cards, headsets, keyboards, mice, and LAN cards

### 3 Description

The SN54LVC14A hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC14A hex Schmitt-trigger inverter is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The devices contain six independent inverters and perform the Boolean function  $Y = \bar{A}$ .

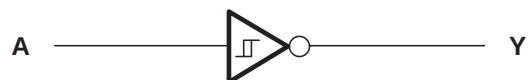
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V or 5-V system environment.

#### Device Information<sup>(1)</sup>

| PART NUMBER   | PACKAGE    | BODY SIZE (NOM)    |
|---------------|------------|--------------------|
| SN54LVC14AFK  | LCCC (20)  | 8.90 mm × 8.90 mm  |
| SN54LVC14AJ   | CDIP (14)  | 20.00 mm × 7.00 mm |
| SN54LVC14AW   | CFP (14)   | 9.21 mm × 6.30 mm  |
| SN74LVC14ANS  | SO (14)    | 10.20 mm × 5.30 mm |
| SN74LVC14AD   | SOIC (14)  | 8.65 mm × 6.00 mm  |
| SN74LVC14ADB  | SSOP (14)  | 6.20 mm × 5.30 mm  |
| SN74LVC14APW  | TSSOP (14) | 5.00 mm × 4.40 mm  |
| SN74LVC14ADGV | TVSOP (14) | 4.40 mm × 3.60 mm  |
| SN74LVC14ARGY | VQFN (14)  | 3.50 mm × 3.50 mm  |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



## Table of Contents

|                                            |           |                                                            |           |
|--------------------------------------------|-----------|------------------------------------------------------------|-----------|
| <b>1 Features</b>                          | <b>1</b>  | 8.1 Overview                                               | 10        |
| <b>2 Applications</b>                      | <b>1</b>  | 8.2 Functional Block Diagram                               | 10        |
| <b>3 Description</b>                       | <b>1</b>  | 8.3 Feature Description                                    | 10        |
| <b>4 Revision History</b>                  | <b>2</b>  | 8.4 Device Functional Modes                                | 11        |
| <b>5 Pin Configuration and Functions</b>   | <b>3</b>  | <b>9 Application and Implementation</b>                    | <b>12</b> |
| <b>6 Specifications</b>                    | <b>4</b>  | 9.1 Application Information                                | 12        |
| 6.1 Absolute Maximum Ratings               | 4         | 9.2 Typical Application                                    | 12        |
| 6.2 ESD Ratings                            | 4         | <b>10 Power Supply Recommendations</b>                     | <b>14</b> |
| 6.3 Recommended Operating Conditions:      |           | <b>11 Layout</b>                                           | <b>14</b> |
| SN54LVC14A                                 | 4         | 11.1 Layout Guidelines                                     | 14        |
| 6.4 Recommended Operating Conditions:      |           | 11.2 Layout Examples                                       | 14        |
| SN74LVC14A                                 | 5         | <b>12 Device and Documentation Support</b>                 | <b>15</b> |
| 6.5 Thermal Information                    | 5         | 12.1 Related Documentation                                 | 15        |
| 6.6 Electrical Characteristics, SN54LVC14A | 5         | 12.2 Related Links                                         | 15        |
| 6.7 Electrical Characteristics, SN74LVC14A | 6         | 12.3 Receiving Notification of Documentation Updates       | 15        |
| 6.8 Switching Characteristics, SN54LVC14A  | 7         | 12.4 Community Resources                                   | 15        |
| 6.9 Switching Characteristics, SN74LVC14A  | 7         | 12.5 Trademarks                                            | 15        |
| 6.10 Operating Characteristics             | 8         | 12.6 Electrostatic Discharge Caution                       | 15        |
| 6.11 Typical Characteristics               | 8         | 12.7 Glossary                                              | 15        |
| <b>7 Parameter Measurement Information</b> | <b>9</b>  | <b>13 Mechanical, Packaging, and Orderable Information</b> | <b>15</b> |
| <b>8 Detailed Description</b>              | <b>10</b> |                                                            |           |

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

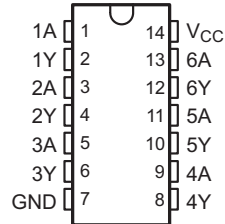
| Changes from Revision AA (June 2015) to Revision AB                                                                                                                                             | Page |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Changed order of the 'Features' list                                                                                                                                                          | 1    |
| • Deleted "I <sub>off</sub> Support Live Insertion, Partial-Power-Down Mode and Back Drive protection" from Features list                                                                       | 1    |
| • Deleted <i>Device Options</i> table, see <i>Mechanical, Packaging, and Orderable Information</i> at the end of the data sheet                                                                 | 1    |
| • Added $V_O > V_{CC}$ to Output clamp current in <i>Absolute Maximum Ratings</i>                                                                                                               | 4    |
| • Changed MAX value for Output clamp current, I <sub>OK</sub> from: –50 to: ±50                                                                                                                 | 4    |
| • Changed values in the <i>Thermal Information</i> table to align with JEDEC standards                                                                                                          | 5    |
| • Added <i>Feature Description</i> sections for <i>Balanced High-Drive CMOS Push-Pull Outputs</i> , <i>Standard CMOS Inputs</i> , <i>Clamp Diodes</i> , and <i>Over-Voltage Tolerant Inputs</i> | 10   |
| • Added <i>Related Documentation</i> and <i>Receiving Notification of Documentation Updates</i> sections                                                                                        | 15   |

| Changes from Revision Z (January 2014) to Revision AA                                                                                                                                                                                                                                                                                                                                                                                                 | Page |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1    |
| • Moved T <sub>stg</sub> to <i>Absolute Maximum Ratings</i> table                                                                                                                                                                                                                                                                                                                                                                                     | 4    |

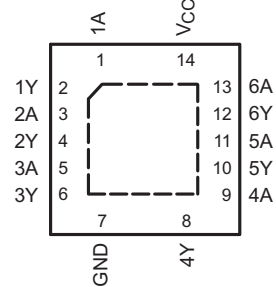
| Changes from Revision Y (October 2010) to Revision Z | Page |
|------------------------------------------------------|------|
| • Updated document to new TI data sheet format       | 1    |
| • Updated <i>Features</i>                            | 1    |
| • Added Military Disclaimer to <i>Features</i> list  | 1    |

## 5 Pin Configuration and Functions

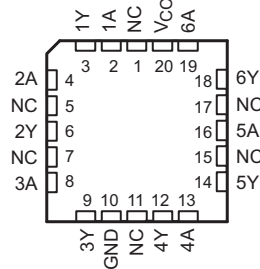
**D, DB, DGV, NS, J, W, or PW Package  
14-Pin SOIC, SSOP, TVSOP, SO, CDIP, CFP, or TSSOP  
Top View**



**RGY Package  
14-Pin VQFN  
Top View**



**FK Package  
20-Pin LCCC  
Top View**



### Pin Functions

| PIN             |                                               |      | I/O | DESCRIPTION     |
|-----------------|-----------------------------------------------|------|-----|-----------------|
| NAME            | SOIC, SSOP, TVSOP, SO, CDIP, CFP, TSSOP, VQFN | LCCC |     |                 |
| 1A              | 1                                             | 2    | I   | Data Input      |
| 2A              | 3                                             | 4    | I   | Data Input      |
| 3A              | 5                                             | 8    | I   | Data Input      |
| 4A              | 9                                             | 13   | I   | Data Input      |
| 5A              | 11                                            | 16   | I   | Data Input      |
| 6A              | 13                                            | 19   | I   | Data Input      |
| GND             | 7                                             | 10   | —   | Ground          |
| V <sub>CC</sub> | 14                                            | 20   | —   | Positive supply |
| 1Y              | 2                                             | 3    | O   | Data Output     |
| 2Y              | 4                                             | 6    | O   | Data Output     |
| 3Y              | 6                                             | 9    | O   | Data Output     |
| 4Y              | 8                                             | 12   | O   | Data Output     |
| 5Y              | 10                                            | 14   | O   | Data Output     |
| 6Y              | 12                                            | 18   | O   | Data Output     |
| NC              | —                                             | 1    | —   | No Connect      |
|                 |                                               | 5    |     |                 |
|                 |                                               | 7    |     |                 |
|                 |                                               | 11   |     |                 |
|                 |                                               | 15   |     |                 |
|                 |                                               | 17   |     |                 |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                   |                                                        | MIN  | MAX                   | UNIT |
|------------------|---------------------------------------------------|--------------------------------------------------------|------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage                                    |                                                        | −0.5 | 6.5                   | V    |
| V <sub>I</sub>   | Input voltage <sup>(2)</sup>                      |                                                        | −0.5 | 6.5                   | V    |
| V <sub>O</sub>   | Output voltage <sup>(2)(3)</sup>                  |                                                        | −0.5 | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Input clamp current                               | V <sub>I</sub> < 0                                     | −50  |                       | mA   |
| I <sub>OK</sub>  | Output clamp current                              | V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> | ±50  |                       | mA   |
| I <sub>O</sub>   | Continuous output current                         |                                                        | ±50  |                       | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND |                                                        | ±100 |                       | mA   |
| P <sub>tot</sub> | Power dissipation                                 | T <sub>A</sub> = −40°C to +125°C <sup>(4)(5)</sup>     | 500  |                       | mW   |
| T <sub>stg</sub> | Storage temperature                               |                                                        | −65  | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.
- (4) For the D package: above 70°C, the value of P<sub>tot</sub> derates linearly with 8 mW/K.
- (5) For the DB, DGV, NS, and PW packages: above 60°C, the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.

### 6.2 ESD Ratings

|                    |                         | VALUE                                                                          | UNIT  |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | +2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | +1000 |
|                    |                         | Machine Model                                                                  | 200   |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions: SN54LVC14A

See <sup>(1)</sup>

|                 |                           |                         | SN54LVC14A    |                 | UNIT |
|-----------------|---------------------------|-------------------------|---------------|-----------------|------|
|                 |                           |                         | −55 TO +125°C |                 |      |
|                 |                           |                         | MIN           | MAX             |      |
| V <sub>CC</sub> | Supply voltage            | Operating               | 2             | 3.6             | V    |
|                 |                           | Data retention only     | 1.5           |                 |      |
| V <sub>I</sub>  | Input voltage             |                         | 0             | 5.5             | V    |
| V <sub>O</sub>  | Output voltage            |                         | 0             | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current | V <sub>CC</sub> = 2.7 V | −12           |                 | mA   |
|                 |                           | V <sub>CC</sub> = 3 V   | −24           |                 |      |
| I <sub>OL</sub> | Low-level output current  | V <sub>CC</sub> = 2.7 V | 12            |                 | mA   |
|                 |                           | V <sub>CC</sub> = 3 V   | 24            |                 |      |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

## 6.4 Recommended Operating Conditions: SN74LVC14A

See <sup>(1)</sup>

|                 |                           |                          | SN74LVC14A            |                 |              |                 |               |                 | UNIT |
|-----------------|---------------------------|--------------------------|-----------------------|-----------------|--------------|-----------------|---------------|-----------------|------|
|                 |                           |                          | T <sub>A</sub> = 25°C |                 | –40 TO +85°C |                 | –40 TO +125°C |                 |      |
|                 |                           |                          | MIN                   | MAX             | MIN          | MAX             | MIN           | MAX             |      |
| V <sub>CC</sub> | Supply voltage            | Operating                | 1.65                  | 3.6             | 1.65         | 3.6             | 1.65          | 3.6             | V    |
|                 |                           | Data retention only      | 1.5                   |                 | 1.5          |                 | 1.5           |                 |      |
| V <sub>I</sub>  | Input voltage             |                          | 0                     | 5.5             | 0            | 5.5             | 0             | 5.5             | V    |
| V <sub>O</sub>  | Output voltage            |                          | 0                     | V <sub>CC</sub> | 0            | V <sub>CC</sub> | 0             | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current | V <sub>CC</sub> = 1.65 V | –4                    |                 | –4           |                 | –4            |                 | mA   |
|                 |                           | V <sub>CC</sub> = 2.3 V  | –8                    |                 | –8           |                 | –8            |                 |      |
|                 |                           | V <sub>CC</sub> = 2.7 V  | –12                   |                 | –12          |                 | –12           |                 |      |
|                 |                           | V <sub>CC</sub> = 3 V    | –24                   |                 | –24          |                 | –24           |                 |      |
| I <sub>OL</sub> | Low-level output current  | V <sub>CC</sub> = 1.65 V | 4                     |                 | 4            |                 | 4             |                 | mA   |
|                 |                           | V <sub>CC</sub> = 2.3 V  | 8                     |                 | 8            |                 | 8             |                 |      |
|                 |                           | V <sub>CC</sub> = 2.7 V  | 12                    |                 | 12           |                 | 12            |                 |      |
|                 |                           | V <sub>CC</sub> = 3 V    | 24                    |                 | 24           |                 | 24            |                 |      |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

## 6.5 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74LVC14A |           |             |         |            |            | UNIT |
|-------------------------------|----------------------------------------------|------------|-----------|-------------|---------|------------|------------|------|
|                               |                                              | D (SOIC)   | DB (SSOP) | DGV (TVSOP) | NS (SO) | PW (TSSOP) | RGY (LCCC) |      |
|                               |                                              | 14 PINS    |           |             |         |            | 20 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 117.6      | 131.8     | 153.5       | 115.7   | 145.9      | 93.8       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 78.2       | 83.9      | 75.2        | 72.2    | 73.4       | 106.7      | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 71.9       | 79.2      | 86.6        | 74.4    | 87.7       | 69.8       | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 39.3       | 41.7      | 19.9        | 33.7    | 18.9       | 22.0       | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 71.6       | 78.6      | 85.9        | 74.1    | 87.1       | 70.0       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | —          | —         | —           | —       | —          | 49.4       | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Electrical Characteristics, SN54LVC14A

over operating free-air temperature range (unless otherwise noted)

| PARAMETER       |                                                 | TEST CONDITIONS | V <sub>CC</sub> | SN54LVC14A    |     |     | UNIT |
|-----------------|-------------------------------------------------|-----------------|-----------------|---------------|-----|-----|------|
|                 |                                                 |                 |                 | –55 TO +125°C |     |     |      |
|                 |                                                 |                 |                 | MIN           | TYP | MAX |      |
| V <sub>T+</sub> | Positive-going threshold                        |                 | 2.7 V           | 0.8           | 2   | V   |      |
|                 |                                                 |                 | 3 V             | 0.9           | 2   |     |      |
|                 |                                                 |                 | 3.6 V           | 1.1           | 2   |     |      |
| V <sub>T–</sub> | Negative-going threshold                        |                 | 2.7 V           | 0.4           | 1.4 | V   |      |
|                 |                                                 |                 | 3 V             | 0.6           | 1.5 |     |      |
|                 |                                                 |                 | 3.6 V           | 0.8           | 1.7 |     |      |
| ΔV <sub>T</sub> | Hysteresis (V <sub>T+</sub> – V <sub>T–</sub> ) |                 | 2.7 V           | 0.3           | 1.1 | V   |      |
|                 |                                                 |                 | 3 V             | 0.3           | 1.2 |     |      |
|                 |                                                 |                 | 3.6 V           | 0.3           | 1.2 |     |      |

## Electrical Characteristics, SN54LVC14A (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS                                                                 | V <sub>CC</sub> | SN54LVC14A            |     |     | UNIT |
|------------------|---------------------------------------------------------------------------------|-----------------|-----------------------|-----|-----|------|
|                  |                                                                                 |                 | –55 TO +125°C         |     |     |      |
|                  |                                                                                 |                 | MIN                   | TYP | MAX |      |
| V <sub>OH</sub>  | I <sub>OH</sub> = –100 μA                                                       | 2.7 V to 3.6 V  | V <sub>CC</sub> – 0.2 |     |     | V    |
|                  | V <sub>OL</sub>                                                                 | 2.7 V           | 2.2                   |     |     |      |
|                  |                                                                                 | I <sub>I</sub>  | 2.4                   |     |     |      |
|                  | I <sub>CC</sub>                                                                 |                 | 3 V                   | 2.2 |     |      |
| ΔI <sub>CC</sub> | I <sub>OL</sub> = 100 μA                                                        | 2.7 V to 3.6 V  | 0.2                   |     |     | V    |
|                  | C <sub>i</sub>                                                                  | 2.7 V           | 0.4                   |     |     |      |
|                  | I <sub>OL</sub> = 24 mA                                                         | 3 V             | 0.55                  |     |     |      |
|                  | V <sub>I</sub> = 5.5 V or GND                                                   | 3.6 V           | ±5                    |     |     | μA   |
|                  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                     | 3.6 V           | 10                    |     |     | μA   |
|                  | One input at V <sub>CC</sub> – 0.6 V,<br>Other inputs at V <sub>CC</sub> or GND | 2.7 V to 3.6 V  | 500                   |     |     | μA   |
|                  | V <sub>I</sub> = V <sub>CC</sub> or GND                                         | 3.3 V           | 5 <sup>(1)</sup>      |     |     | pF   |

(1)  $T_A = 25^\circ C$

## 6.7 Electrical Characteristics, SN74LVC14A

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                          | TEST CONDITIONS | V <sub>CC</sub> | SN74LVC14A            |     |      |              |      |               | UNIT |     |
|--------------------------------------------------------------------|-----------------|-----------------|-----------------------|-----|------|--------------|------|---------------|------|-----|
|                                                                    |                 |                 | T <sub>A</sub> = 25°C |     |      | –40 TO +85°C |      | –40 TO +125°C |      |     |
|                                                                    |                 |                 | MIN                   | TYP | MAX  | MIN          | MAX  | MIN           |      | MAX |
| V <sub>T+</sub><br>Positive-going threshold                        |                 | 1.65 V          | 0.4                   |     | 1.3  | 0.4          | 1.3  | 0.4           | 1.3  | V   |
|                                                                    |                 | 1.95 V          | 0.6                   |     | 1.5  | 0.6          | 1.5  | 0.6           | 1.5  |     |
|                                                                    |                 | 2.3 V           | 0.8                   |     | 1.7  | 0.8          | 1.7  | 0.8           | 1.7  |     |
|                                                                    |                 | 2.5 V           | 0.8                   |     | 1.7  | 0.8          | 1.7  | 0.8           | 1.7  |     |
|                                                                    |                 | 2.7 V           | 0.8                   |     | 2    | 0.8          | 2    | 0.8           | 2    |     |
|                                                                    |                 | 3 V             | 0.9                   |     | 2    | 0.9          | 2    | 0.9           | 2    |     |
|                                                                    |                 | 3.6 V           | 1.1                   |     | 2    | 1.1          | 2    | 1.1           | 2    |     |
| V <sub>T–</sub><br>Negative-going threshold                        |                 | 1.65 V          | 0.15                  |     | 0.85 | 0.15         | 0.85 | 0.15          | 0.85 | V   |
|                                                                    |                 | 1.95 V          | 0.25                  |     | 0.95 | 0.25         | 0.95 | 0.25          | 0.95 |     |
|                                                                    |                 | 2.3 V           | 0.4                   |     | 1.2  | 0.4          | 1.2  | 0.4           | 1.2  |     |
|                                                                    |                 | 2.5 V           | 0.4                   |     | 1.2  | 0.4          | 1.2  | 0.4           | 1.2  |     |
|                                                                    |                 | 2.7 V           | 0.4                   |     | 1.4  | 0.4          | 1.4  | 0.4           | 1.4  |     |
|                                                                    |                 | 3 V             | 0.6                   |     | 1.5  | 0.6          | 1.5  | 0.6           | 1.5  |     |
|                                                                    |                 | 3.6 V           | 0.8                   |     | 1.7  | 0.8          | 1.7  | 0.8           | 1.7  |     |
| ΔV <sub>T</sub><br>Hysteresis (V <sub>T+</sub> – V <sub>T–</sub> ) |                 | 1.65 V          | 0.1                   |     | 1.15 | 0.1          | 1.15 | 0.1           | 1.15 | V   |
|                                                                    |                 | 1.95 V          | 0.15                  |     | 1.25 | 0.15         | 1.25 | 0.15          | 1.25 |     |
|                                                                    |                 | 2.3 V           | 0.25                  |     | 1.3  | 0.25         | 1.3  | 0.25          | 1.3  |     |
|                                                                    |                 | 2.5 V           | 0.25                  |     | 1.3  | 0.25         | 1.3  | 0.25          | 1.3  |     |
|                                                                    |                 | 2.7 V           | 0.3                   |     | 1.1  | 0.3          | 1.1  | 0.3           | 1.1  |     |
|                                                                    |                 | 3 V             | 0.3                   |     | 1.2  | 0.3          | 1.2  | 0.3           | 1.2  |     |
|                                                                    |                 | 3.6 V           | 0.3                   |     | 1.2  | 0.3          | 1.2  | 0.3           | 1.2  |     |

## Electrical Characteristics, SN74LVC14A (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS                                                              | V <sub>CC</sub> | SN74LVC14A            |     |     |                       |     |                       | UNIT |
|------------------|------------------------------------------------------------------------------|-----------------|-----------------------|-----|-----|-----------------------|-----|-----------------------|------|
|                  |                                                                              |                 | T <sub>A</sub> = 25°C |     |     | –40 TO +85°C          |     | –40 TO +125°C         |      |
|                  |                                                                              |                 | MIN                   | TYP | MAX | MIN                   | MAX | MIN MAX               |      |
| V <sub>OH</sub>  | I <sub>OH</sub> = –100 µA                                                    | 1.65 V to 3.6 V | V <sub>CC</sub> – 0.2 |     |     | V <sub>CC</sub> – 0.2 |     | V <sub>CC</sub> – 0.3 | V    |
|                  | I <sub>OH</sub> = –4 mA                                                      | 1.65 V          | 1.29                  |     |     | 1.2                   |     | 1.05                  |      |
|                  | I <sub>OH</sub> = –8 mA                                                      | 2.3 V           | 1.9                   |     |     | 1.7                   |     | 1.65                  |      |
|                  | I <sub>OH</sub> = –12 mA                                                     | 2.7 V           | 2.2                   |     |     | 2.2                   |     | 2.05                  |      |
|                  | I <sub>OH</sub> = –24 mA                                                     | 3 V             | 2.4                   |     |     | 2.4                   |     | 2.25                  |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = 100 µA                                                     | 1.65 V to 3.6 V | 0.1                   |     |     | 0.2                   |     | 0.3                   | V    |
|                  | I <sub>OL</sub> = 4 mA                                                       | 1.65 V          | 0.24                  |     |     | 0.45                  |     | 0.6                   |      |
|                  | I <sub>OL</sub> = 8 mA                                                       | 2.3 V           | 0.3                   |     |     | 0.7                   |     | 0.75                  |      |
|                  | I <sub>OL</sub> = 12 mA                                                      | 2.7 V           | 0.4                   |     |     | 0.4                   |     | 0.6                   |      |
|                  | I <sub>OL</sub> = 24 mA                                                      | 3 V             | 0.55                  |     |     | 0.55                  |     | 0.8                   |      |
| I <sub>I</sub>   | V <sub>I</sub> = 5.5 V or GND                                                | 3.6 V           | ±1                    |     |     | ±5                    |     | ±20                   | µA   |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                  | 3.6 V           | 1                     |     |     | 10                    |     | 40                    | µA   |
| ΔI <sub>CC</sub> | One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND | 2.7 V to 3.6 V  | 500                   |     |     | 500                   |     | 5000                  | µA   |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           | 5                     |     |     |                       |     |                       | pF   |

## 6.8 Switching Characteristics, SN54LVC14A

over operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER       | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> | SN54LVC14A    |     | UNIT |
|-----------------|-----------------|----------------|-----------------|---------------|-----|------|
|                 |                 |                |                 | –55 TO +125°C |     |      |
|                 |                 |                |                 | MIN           | MAX |      |
| t <sub>pd</sub> | A               | Y              | 2.7 V           | 7.5           |     | ns   |
|                 |                 |                | 3.3 V ± 0.3 V   | 1             | 6.4 |      |

## 6.9 Switching Characteristics, SN74LVC14A

over operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER          | FROM (INPUT) | TO (OUTPUT) | V <sub>CC</sub> | SN74LVC14A            |     |      |              |     |               | UNIT |
|--------------------|--------------|-------------|-----------------|-----------------------|-----|------|--------------|-----|---------------|------|
|                    |              |             |                 | T <sub>A</sub> = 25°C |     |      | –40 TO +85°C |     | –40 TO +125°C |      |
|                    |              |             |                 | MIN                   | TYP | MAX  | MIN          | MAX | MIN MAX       |      |
| t <sub>pd</sub>    | A            | Y           | 1.8 V ± 0.15 V  | 1                     | 5   | 10.5 | 1            | 11  | 1 13          | ns   |
|                    |              |             | 2.5 V ± 0.2 V   | 1                     | 3.4 | 7.3  | 1            | 7.8 | 1 10          |      |
|                    |              |             | 2.7 V           | 1                     | 3.6 | 7.3  | 1            | 7.5 | 1 9.5         |      |
|                    |              |             | 3.3 V ± 0.3 V   | 1                     | 3.2 | 6.2  | 1            | 6.4 | 1 8           |      |
| t <sub>sk(o)</sub> |              |             | 3.3 V ± 0.3 V   | 1                     |     |      | 1            |     | 1.5           | ns   |

## 6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER                              | TEST CONDITIONS     | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | UNIT |
|----------------------------------------|---------------------|-------------------------|-------------------------|-------------------------|------|
|                                        |                     | TYP                     | TYP                     | TYP                     |      |
| $C_{pd}$ Power dissipation capacitance | $f = 10\text{ MHz}$ | 11                      | 12                      | 15                      | pF   |

## 6.11 Typical Characteristics

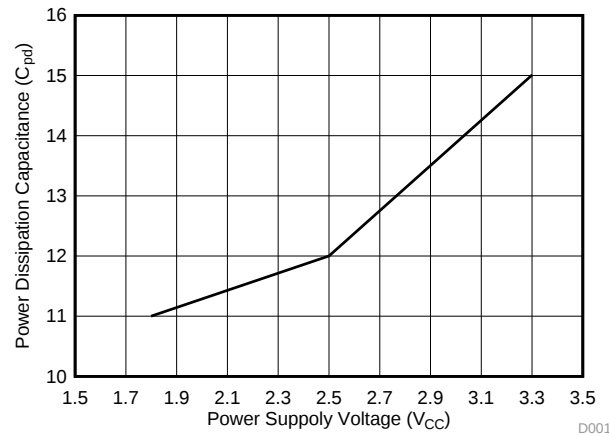
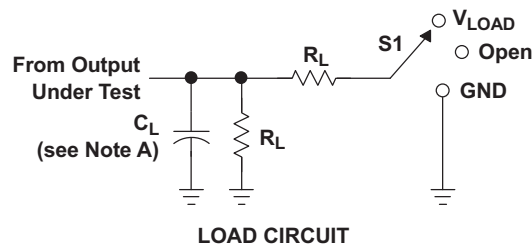


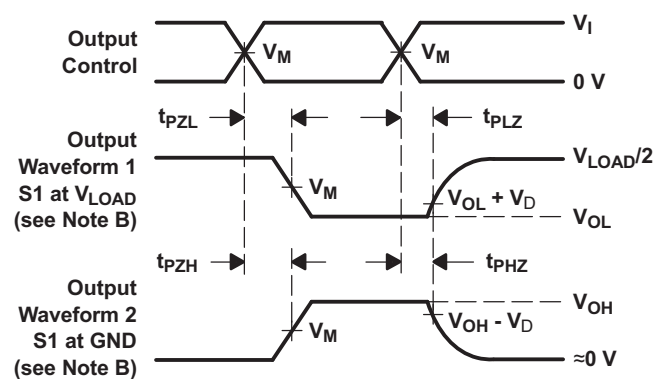
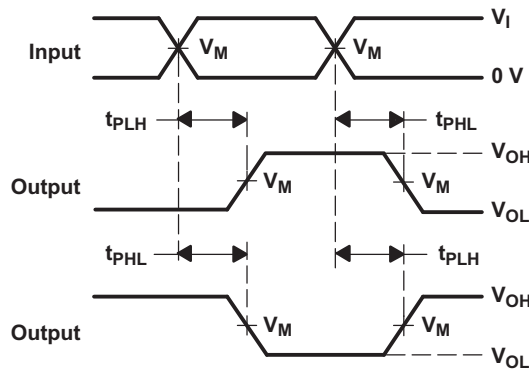
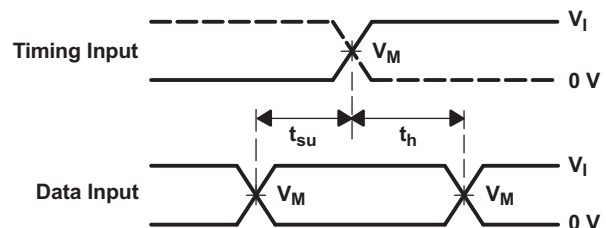
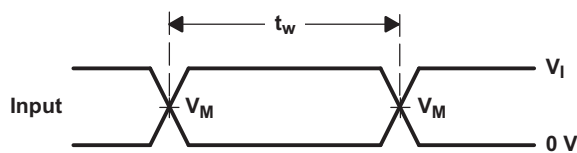
Figure 1. Power Dissipation Capacitance vs. Power Supply Voltage

## 7 Parameter Measurement Information



| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$ | $V_D$  |
|----------------------------------|----------|----------------------|------------|-------------------|-------|-------|--------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |       |        |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 kW  | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 W | 0.15 V |
| 2.7 V                            | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 W | 0.3 V  |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 W | 0.3 V  |



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ W}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

The SN54LVC14A hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC14A hex Schmitt-trigger inverter is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The devices contain six independent inverters and perform the Boolean function  $Y = \overline{A}$ .

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V or 5-V system environment.

### 8.2 Functional Block Diagram



**Figure 3. Logic Diagram, Each Inverter (Positive Logic)**

### 8.3 Feature Description

#### 8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

#### 8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modelled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics, SN54LVC14A](#) and [Electrical Characteristics, SN74LVC14A](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics, SN54LVC14A](#) and [Electrical Characteristics, SN74LVC14A](#), using ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by  $\Delta t/\Delta v$  in [Recommended Operating Conditions: SN54LVC14A](#) and [Recommended Operating Conditions: SN74LVC14A](#) to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

#### 8.3.3 Clamp Diodes

The inputs to this device have negative clamping diodes. The outputs to this device have both positive and negative clamping diodes as shown in [Figure 4](#).

#### CAUTION

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## Feature Description (continued)

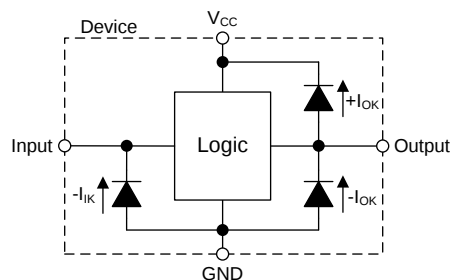


Figure 4. Electrical Placement of Clamping Diodes for Each Input and Output

### 8.3.4 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Absolute Maximum Ratings](#).

### 8.4 Device Functional Modes

Table 1 lists the functional modes for the SN54LVC14A and SN74LVC14A devices.

Table 1. Function Table (Each Inverter)

| INPUT<br>A | OUTPUT<br>Y |
|------------|-------------|
| H          | L           |
| L          | H           |

## 9 Application and Implementation

### NOTE

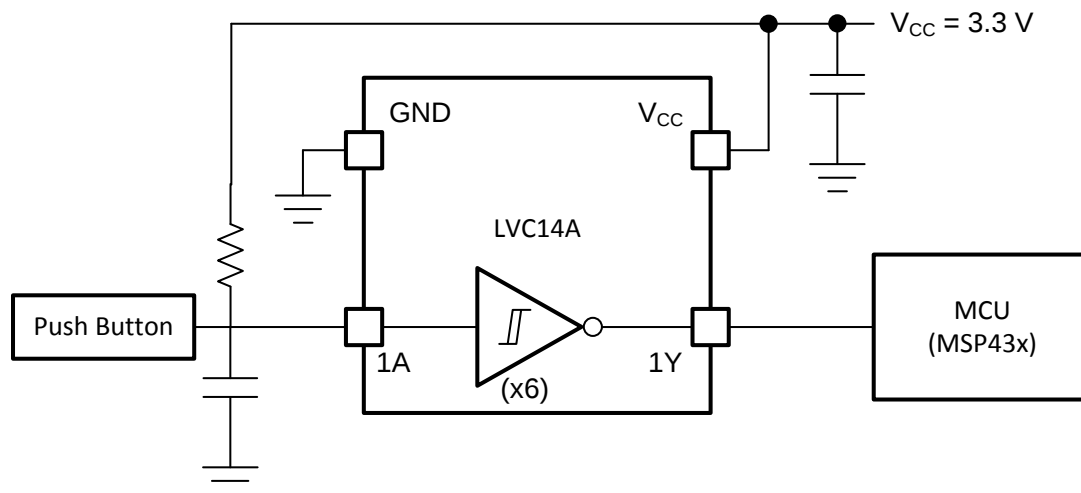
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

Physically interactive interface elements like push buttons or rotary knobs offer simple and easy ways to interact with an electronic system. Many of these physical interface elements often have issues with bouncing, or where the physical conductive contact can connect and disconnect multiple times during a button push or release. This bouncing can cause one or more faulty transient signals to be passed during this transitional period. These faulty signals can be observed in many common applications: for example, a television remote with bouncing error can adjust the TV channel multiple times despite the button being pushed only once. To mitigate these faulty signals, use a Schmitt-trigger, or a device with hysteresis, to remove these faulty signals. Hysteresis allows a device to "remember" its history, and in this case, the LVC14A uses this memory to debounce the physical element's signal, or filter the faulty transient signals and pass only the valid signal each time the element is used. In this example, we show a push button signal passed through an LVC14A that is debounced and inverted to the MCU for push detection.

### 9.2 Typical Application

The signal effects of the debounce circuit can be seen when comparing [Figure 6](#) and [Figure 7](#). In [Figure 6](#), the input is a very poor quality signal due to the error in the physical push button. If the MCU attempts to sample this input to detect a push, there is high probability that multiple push events will be falsely detected. Once the debounce circuit has been implemented, the input is cleaned up, and the MCU can perform push detection without any error, as seen in [Figure 7](#).



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**Figure 5. Debouncer Application Diagram**

#### 9.2.1 Design Requirements

The SN74LVC14A device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

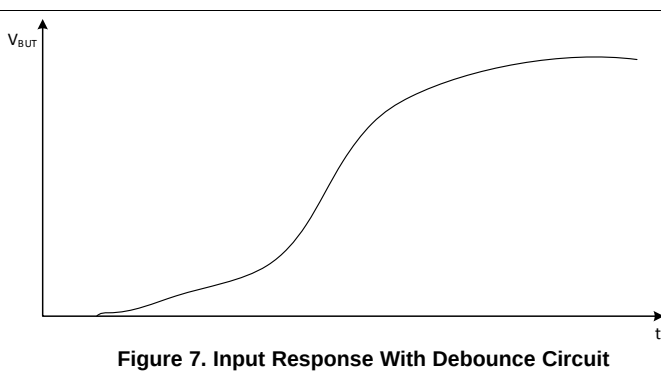
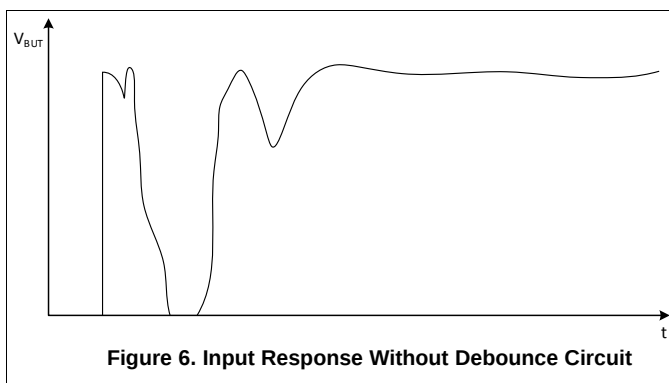
The SN74LVC14A allows for performing logical Boolean functions with hysteresis using digital signals. All input signals should remain as close as possible to either 0 V or  $V_{CC}$  for optimal operation.

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

1. Recommended input conditions:
  - For rise time and fall time specifications, see  $\Delta t/\Delta v$  in the [Recommended Operating Conditions: SN74LVC14A](#) table.
  - For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in the [Recommended Operating Conditions: SN74LVC14A](#) table.
  - Inputs and outputs are overvoltage tolerant and can therefore go as high as 3.6 V at any valid  $V_{CC}$ .
2. Recommended output conditions:
  - Load currents should not exceed  $\pm 50$  mA.
3. Frequency selection criterion:
  - Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the section.

### 9.2.3 Application Curves



## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu$ F bypass capacitor is recommended. If multiple pins are labeled  $V_{CC}$ , then a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins are tied together internally. For devices with dual supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu$ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

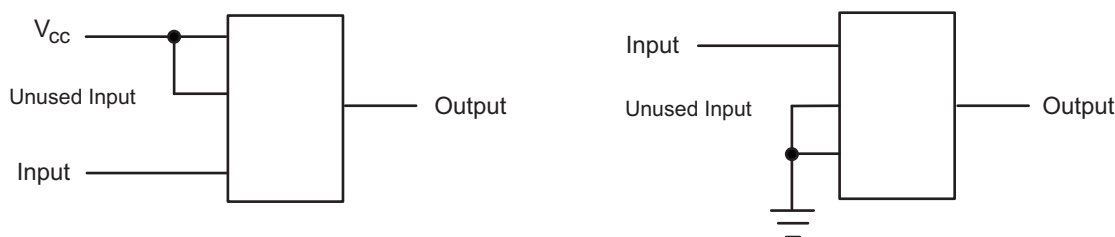
## 11 Layout

### 11.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions (or parts of functions) of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or when only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected, because the undefined voltages at the outside connections result in undefined operational states. Figure 8 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted, which does not disable the input section of the I/Os. Therefore, the I/Os cannot float when disabled.

### 11.2 Layout Examples



**Figure 8. Layout Diagrams**

## 12 Device and Documentation Support

### 12.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#), SCBA004.

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 2. Related Links**

| PARTS      | PRODUCT FOLDER             | ORDER NOW                  | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54LVC14A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| SN74LVC14A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

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All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                  | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|------------------------------------------|-------------------------|
| 5962-9761501Q2A  | ACTIVE        | LCCC         | FK                 | 20   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-<br>9761501Q2A<br>SNJ54LVC<br>14AFK | <a href="#">Samples</a> |
| 5962-9761501QCA  | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9761501QC<br>A<br>SNJ54LVC14AJ      | <a href="#">Samples</a> |
| 5962-9761501QDA  | ACTIVE        | CFP          | W                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9761501QD<br>A<br>SNJ54LVC14AW      | <a href="#">Samples</a> |
| 5962-9761501V2A  | ACTIVE        | LCCC         | FK                 | 20   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-<br>9761501V2A<br>SNV54LVC<br>14AFK | <a href="#">Samples</a> |
| 5962-9761501VCA  | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9761501VC<br>A<br>SNV54LVC14AJ      | <a href="#">Samples</a> |
| 5962-9761501VDA  | ACTIVE        | CFP          | W                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9761501VD<br>A<br>SNV54LVC14AW      | <a href="#">Samples</a> |
| SN74LVC14AD      | ACTIVE        | SOIC         | D                  | 14   | 50             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LVC14A                                   | <a href="#">Samples</a> |
| SN74LVC14ADBR    | ACTIVE        | SSOP         | DB                 | 14   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LC14A                                    | <a href="#">Samples</a> |
| SN74LVC14ADBRE4  | ACTIVE        | SSOP         | DB                 | 14   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LC14A                                    | <a href="#">Samples</a> |
| SN74LVC14ADE4    | ACTIVE        | SOIC         | D                  | 14   | 50             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LVC14A                                   | <a href="#">Samples</a> |
| SN74LVC14ADG4    | ACTIVE        | SOIC         | D                  | 14   | 50             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LVC14A                                   | <a href="#">Samples</a> |
| SN74LVC14ADGVR   | ACTIVE        | TVSOP        | DGV                | 14   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LC14A                                    | <a href="#">Samples</a> |
| SN74LVC14ADR     | ACTIVE        | SOIC         | D                  | 14   | 2500           | RoHS & Green        | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | LVC14A                                   | <a href="#">Samples</a> |
| SN74LVC14ADRE4   | ACTIVE        | SOIC         | D                  | 14   | 2500           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LVC14A                                   | <a href="#">Samples</a> |
| SN74LVC14ADRG3   | ACTIVE        | SOIC         | D                  | 14   | 2500           | RoHS & Green        | SN                                   | Level-1-260C-UNLIM   | -40 to 125   | LVC14A                                   | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                  | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|------------------------------------------|-------------------------|
| SN74LVC14ADRG4   | ACTIVE        | SOIC         | D                  | 14   | 2500           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LVC14A                                   | <a href="#">Samples</a> |
| SN74LVC14ADT     | ACTIVE        | SOIC         | D                  | 14   | 250            | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LVC14A                                   | <a href="#">Samples</a> |
| SN74LVC14ANSR    | ACTIVE        | SO           | NS                 | 14   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LVC14A                                   | <a href="#">Samples</a> |
| SN74LVC14APW     | ACTIVE        | TSSOP        | PW                 | 14   | 90             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LC14A                                    | <a href="#">Samples</a> |
| SN74LVC14APWG4   | ACTIVE        | TSSOP        | PW                 | 14   | 90             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LC14A                                    | <a href="#">Samples</a> |
| SN74LVC14APWR    | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | RoHS & Green        | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | LC14A                                    | <a href="#">Samples</a> |
| SN74LVC14APWRE4  | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LC14A                                    | <a href="#">Samples</a> |
| SN74LVC14APWRG3  | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | RoHS & Green        | SN                                   | Level-1-260C-UNLIM   | -40 to 125   | LC14A                                    | <a href="#">Samples</a> |
| SN74LVC14APWRG4  | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LC14A                                    | <a href="#">Samples</a> |
| SN74LVC14APWT    | ACTIVE        | TSSOP        | PW                 | 14   | 250            | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LC14A                                    | <a href="#">Samples</a> |
| SN74LVC14APWTG4  | ACTIVE        | TSSOP        | PW                 | 14   | 250            | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LC14A                                    | <a href="#">Samples</a> |
| SN74LVC14ARGYR   | ACTIVE        | VQFN         | RGY                | 14   | 3000           | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | LC14A                                    | <a href="#">Samples</a> |
| SN74LVC14ARGYRG4 | ACTIVE        | VQFN         | RGY                | 14   | 3000           | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | LC14A                                    | <a href="#">Samples</a> |
| SNJ54LVC14AFK    | ACTIVE        | LCCC         | FK                 | 20   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-<br>9761501Q2A<br>SNJ54LVC<br>14AFK | <a href="#">Samples</a> |
| SNJ54LVC14AJ     | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9761501QC<br>A<br>SNJ54LVC14AJ      | <a href="#">Samples</a> |
| SNJ54LVC14AW     | ACTIVE        | CFP          | W                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9761501QD<br>A<br>SNJ54LVC14AW      | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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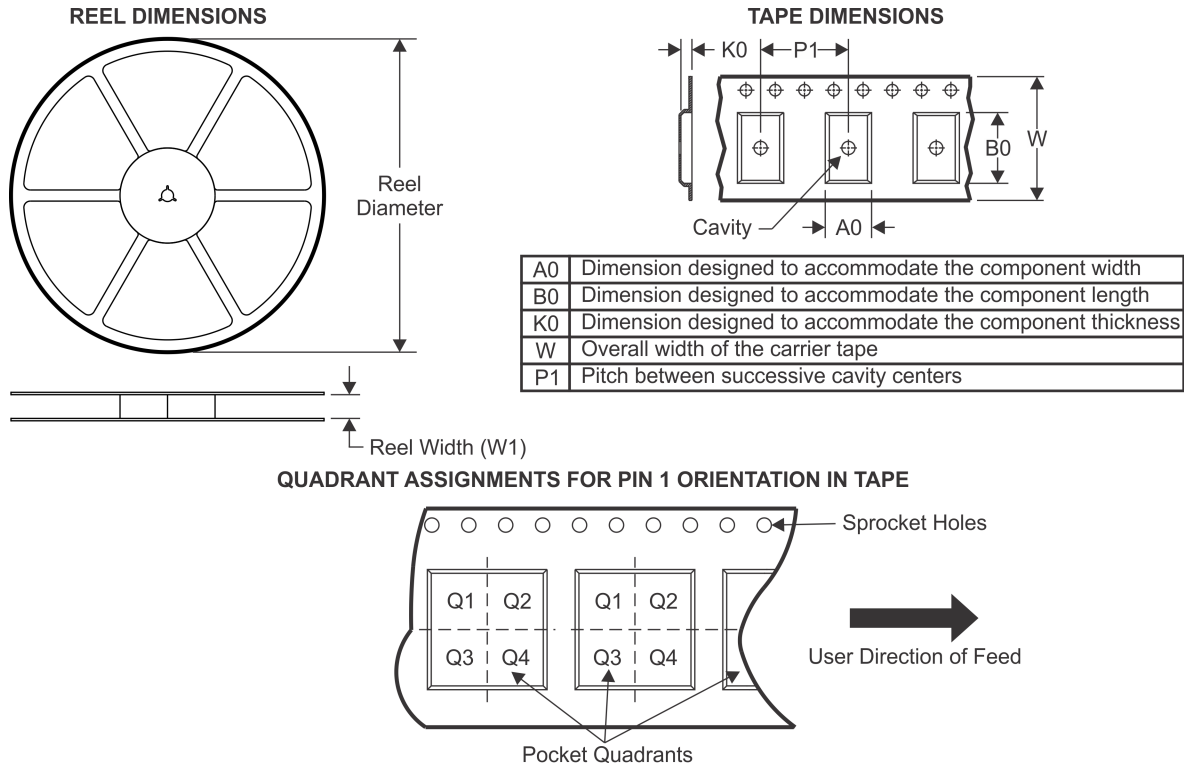
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVC14A, SN54LVC14A-SP, SN74LVC14A :**

- Catalog : [SN74LVC14A](#), [SN54LVC14A](#)
- Automotive : [SN74LVC14A-Q1](#), [SN74LVC14A-Q1](#)
- Enhanced Product : [SN74LVC14A-EP](#), [SN74LVC14A-EP](#)
- Military : [SN54LVC14A](#)
- Space : [SN54LVC14A-SP](#)

**NOTE: Qualified Version Definitions:**

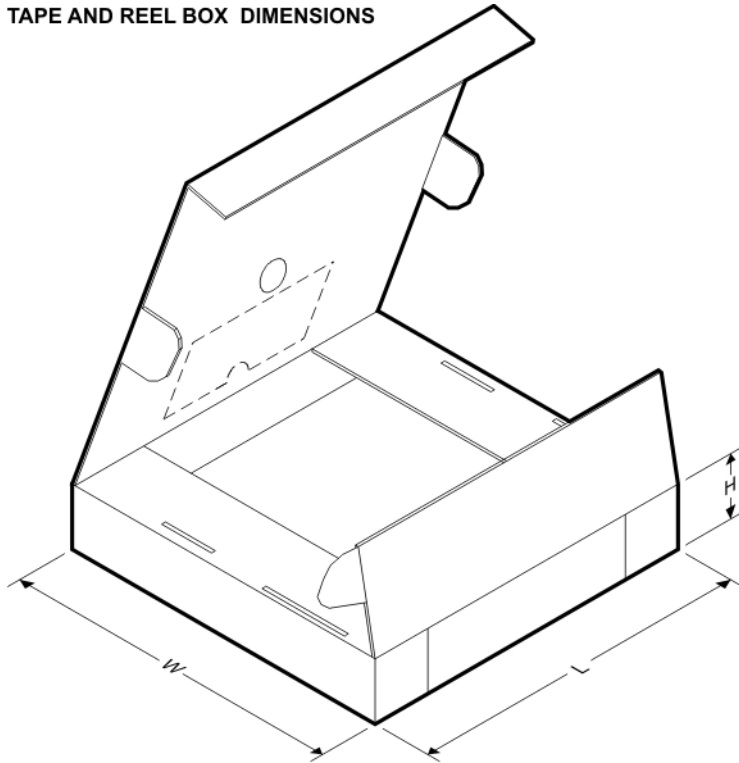
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC14ADBR   | SSOP         | DB              | 14   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74LVC14ADGVR  | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC14ADR    | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC14ADR    | SOIC         | D               | 14   | 2500 | 330.0              | 16.8               | 6.5     | 9.5     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC14ADR    | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC14ADRG3  | SOIC         | D               | 14   | 2500 | 330.0              | 16.8               | 6.5     | 9.5     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC14ADRG4  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC14ADRG4  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC14ADT    | SOIC         | D               | 14   | 250  | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC14ANSR   | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LVC14APWR   | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC14APWR   | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC14APWRG3 | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC14APWRG4 | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC14APWT   | TSSOP        | PW              | 14   | 250  | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC14ARGYR  | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC14ADBR   | SSOP         | DB              | 14   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74LVC14ADGVR  | TVSOP        | DGV             | 14   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74LVC14ADR    | SOIC         | D               | 14   | 2500 | 853.0       | 449.0      | 35.0        |
| SN74LVC14ADR    | SOIC         | D               | 14   | 2500 | 364.0       | 364.0      | 27.0        |
| SN74LVC14ADR    | SOIC         | D               | 14   | 2500 | 340.5       | 336.1      | 32.0        |
| SN74LVC14ADRG3  | SOIC         | D               | 14   | 2500 | 364.0       | 364.0      | 27.0        |
| SN74LVC14ADRG4  | SOIC         | D               | 14   | 2500 | 853.0       | 449.0      | 35.0        |
| SN74LVC14ADRG4  | SOIC         | D               | 14   | 2500 | 340.5       | 336.1      | 32.0        |
| SN74LVC14ADT    | SOIC         | D               | 14   | 250  | 210.0       | 185.0      | 35.0        |
| SN74LVC14ANSR   | SO           | NS              | 14   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74LVC14APWR   | TSSOP        | PW              | 14   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74LVC14APWR   | TSSOP        | PW              | 14   | 2000 | 364.0       | 364.0      | 27.0        |
| SN74LVC14APWRG3 | TSSOP        | PW              | 14   | 2000 | 364.0       | 364.0      | 27.0        |
| SN74LVC14APWRG4 | TSSOP        | PW              | 14   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74LVC14APWT   | TSSOP        | PW              | 14   | 250  | 853.0       | 449.0      | 35.0        |
| SN74LVC14ARGYR  | VQFN         | RGY             | 14   | 3000 | 853.0       | 449.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9761501Q2A | FK           | LCCC         | 20   | 1   | 506.98 | 12.06  | 2030   | NA     |
| 5962-9761501V2A | FK           | LCCC         | 20   | 1   | 506.98 | 12.06  | 2030   | NA     |
| 5962-9761501VDA | W            | CFP          | 14   | 1   | 506.98 | 26.16  | 6220   | NA     |
| SN74LVC14AD     | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74LVC14ADE4   | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74LVC14ADG4   | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74LVC14APW    | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| SN74LVC14APWG4  | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| SNJ54LVC14AFK   | FK           | LCCC         | 20   | 1   | 506.98 | 12.06  | 2030   | NA     |

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |

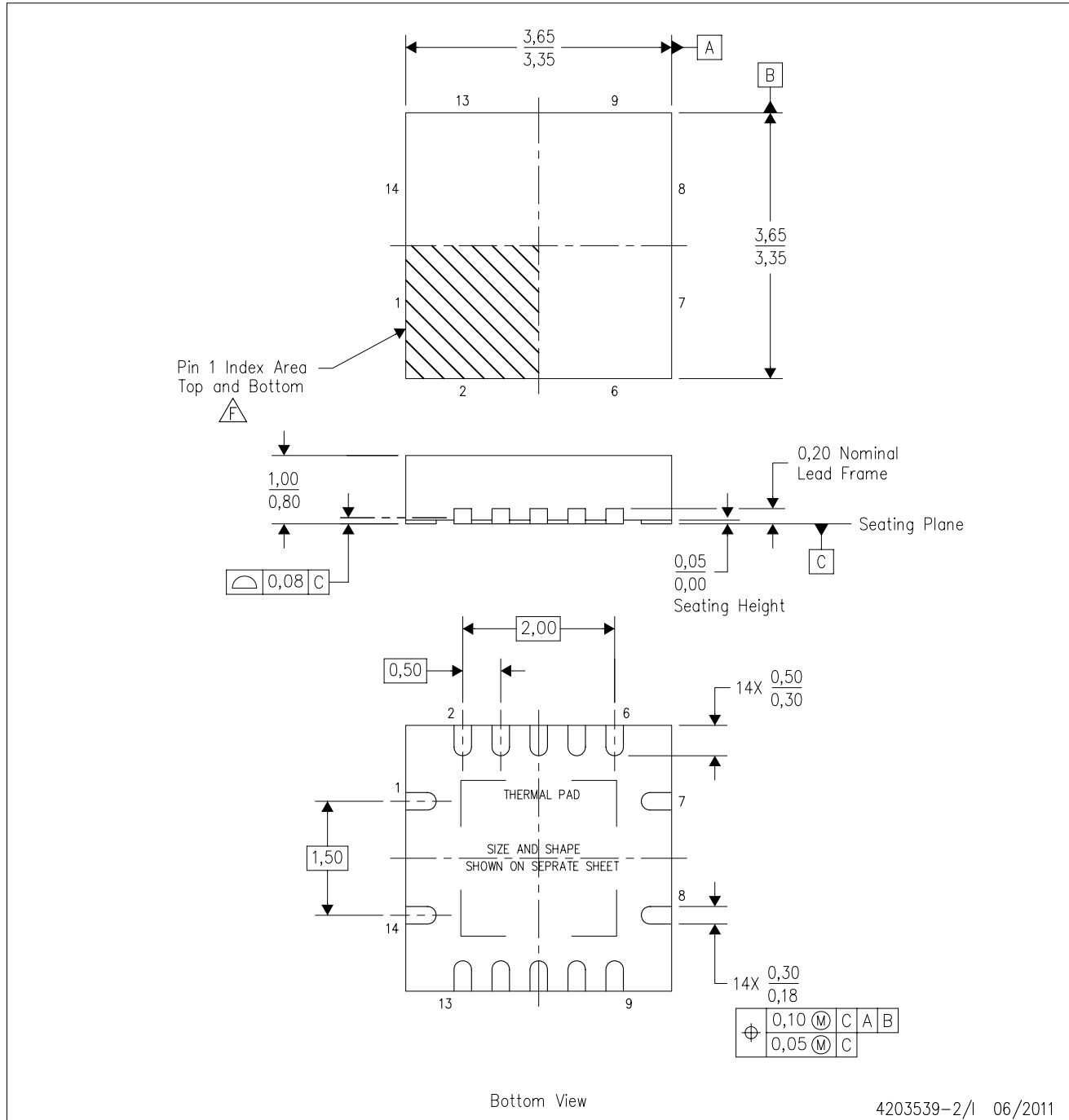


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

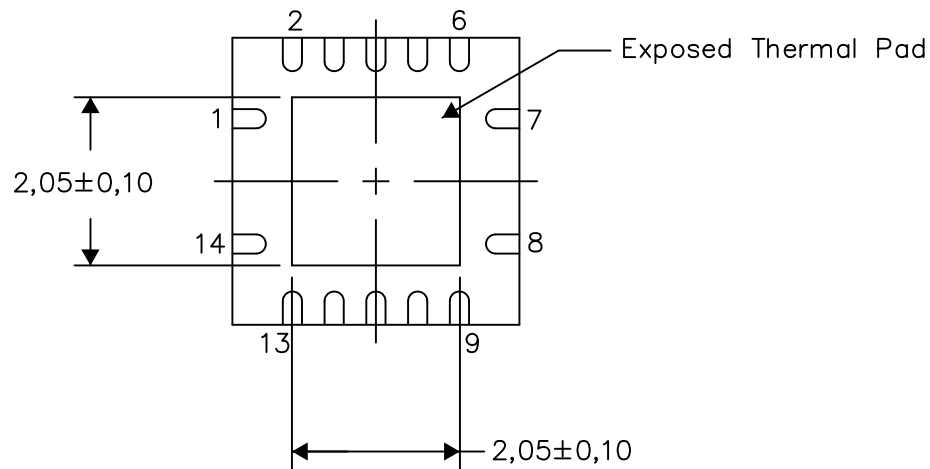
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

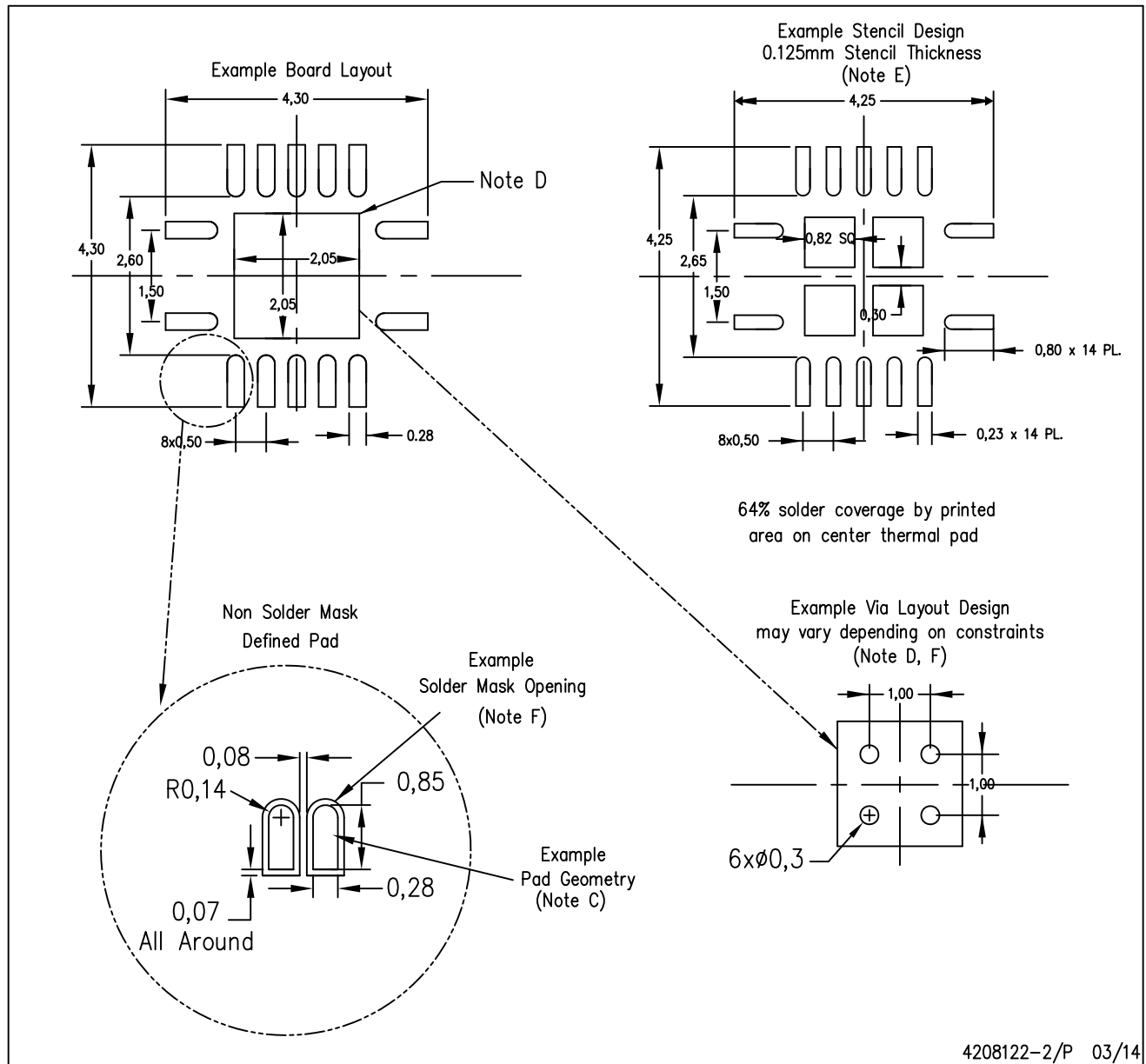
Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

**J 14**

## GENERIC PACKAGE VIEW

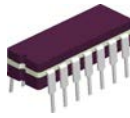
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE

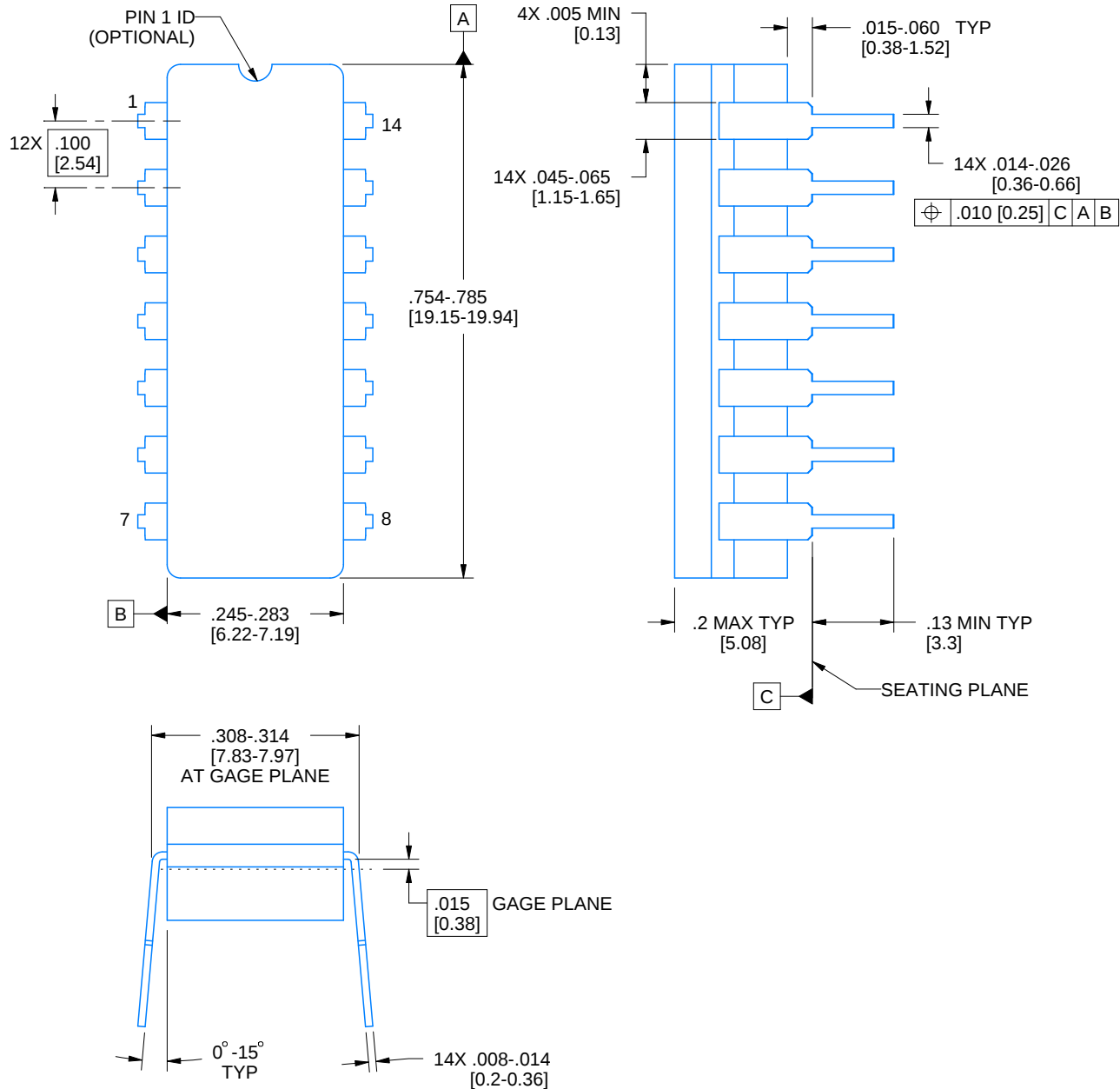


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



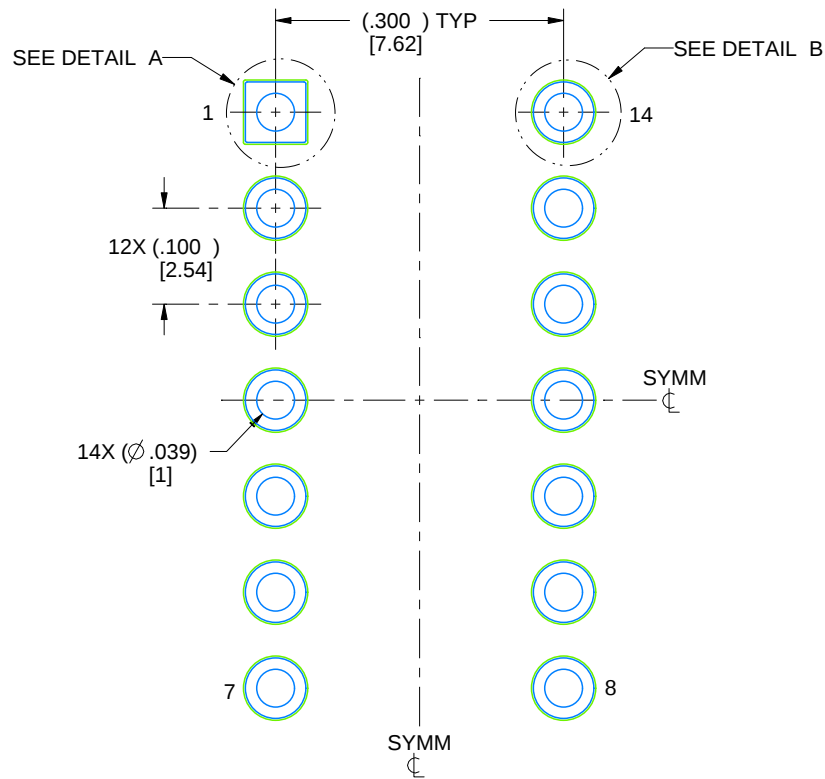
**TEXAS  
INSTRUMENTS**  
www.ti.com

# EXAMPLE BOARD LAYOUT

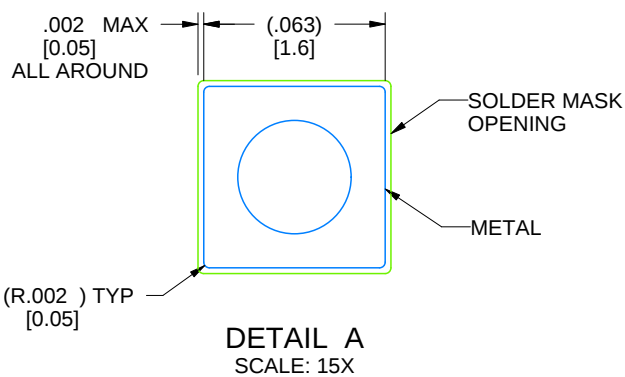
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

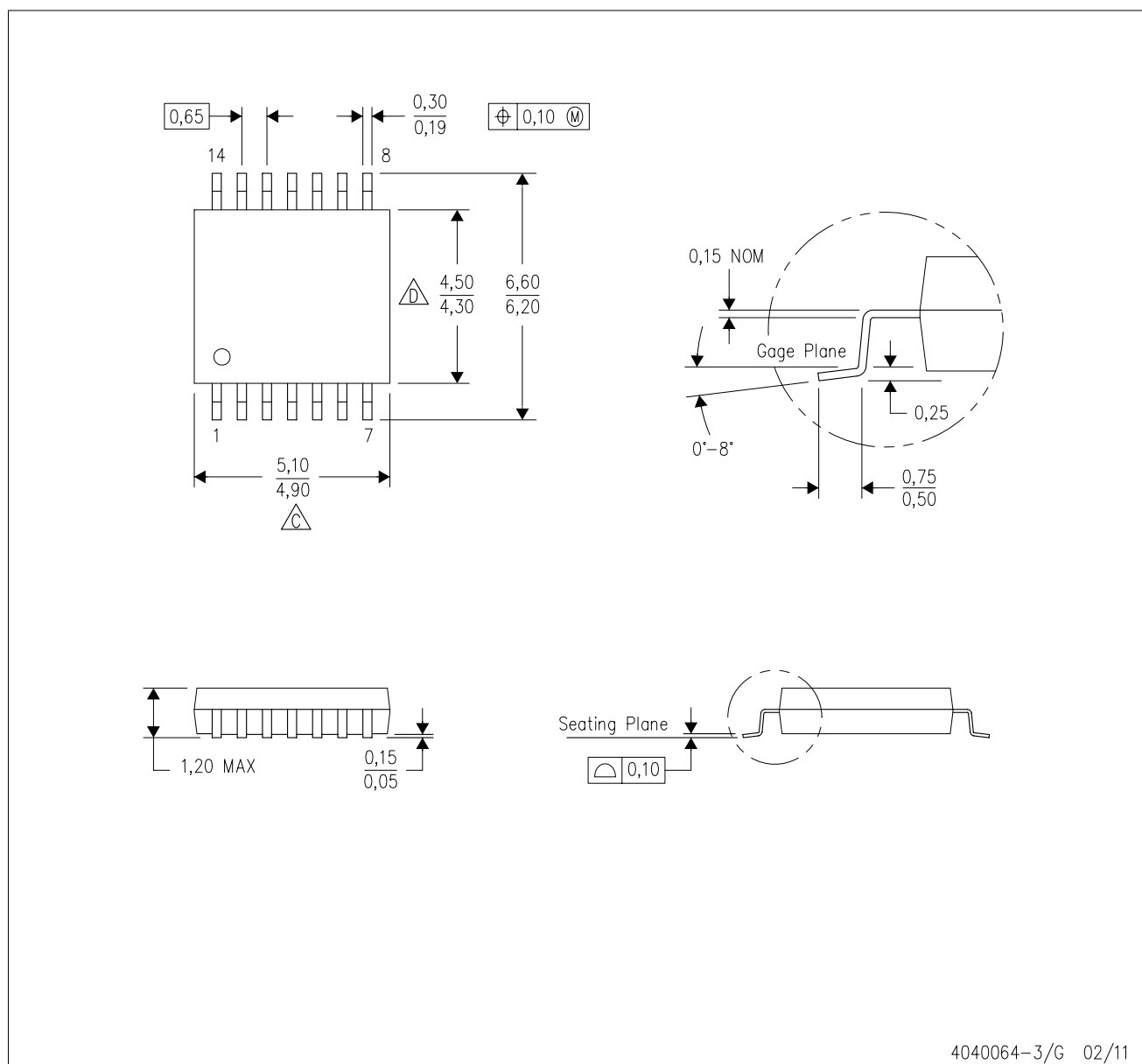
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

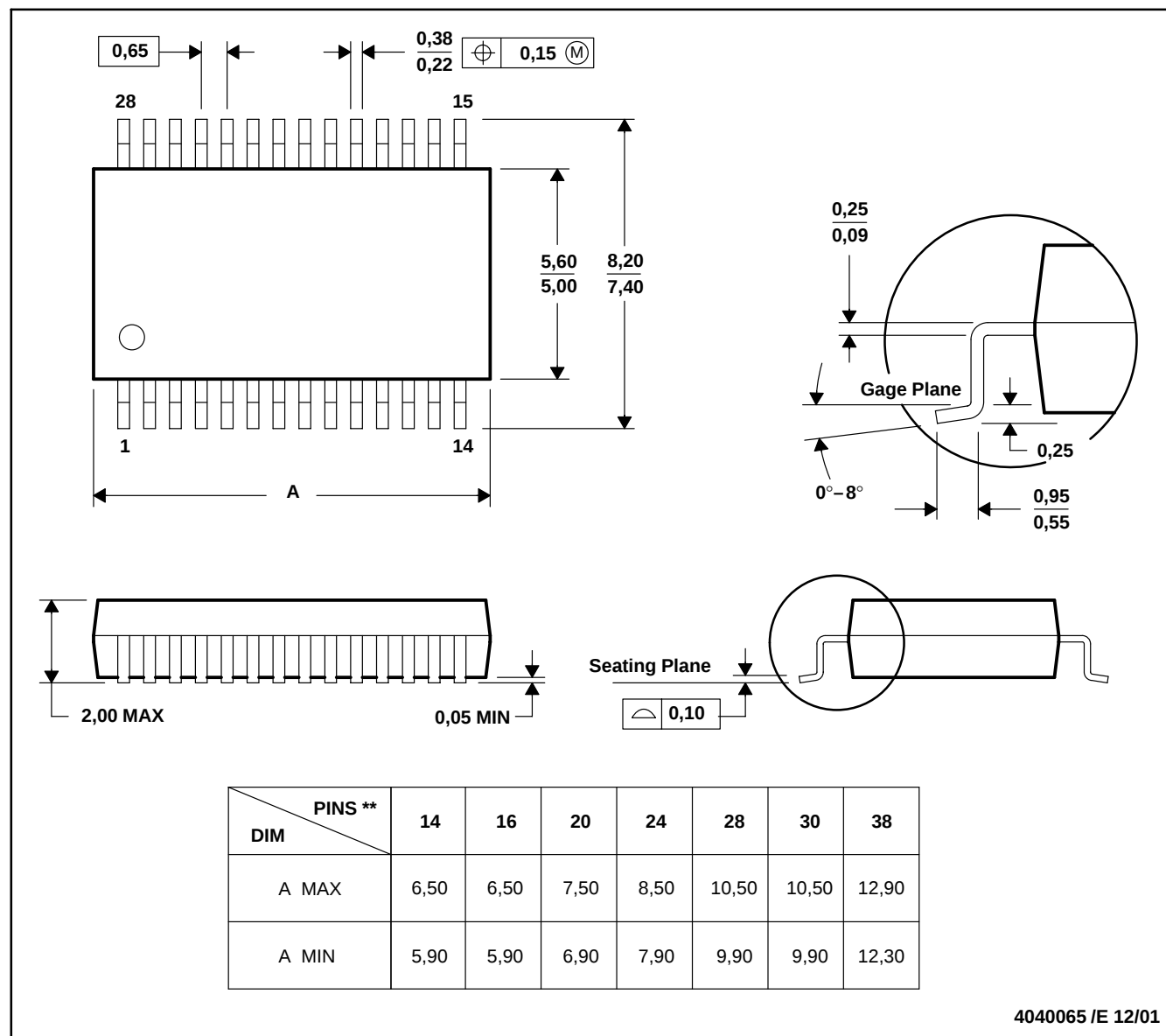


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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