

# CSD22205L –8V P 沟道 NexFET™ 功率 MOSFET

## 1 特性

- 低电阻
- 1.2mm × 1.2mm 小尺寸封装
- 扁平设计，高度为 0.35mm
- 无铅
- 栅源电压钳位
- 栅极 ESD 保护
- 符合 RoHS 标准
- 无卤素

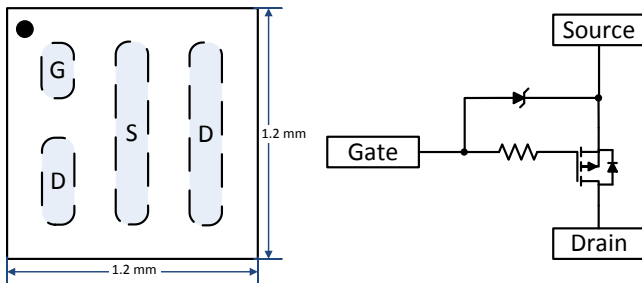
## 2 应用

- 电池管理
- 负载开关
- 电池保护

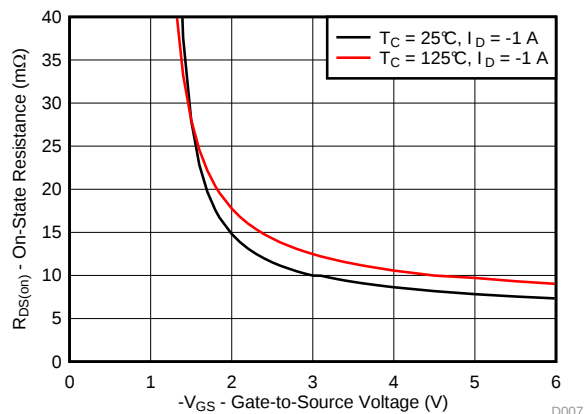
## 3 说明

该 –8V、8.2mΩ、1.2mm × 1.2mm 基板栅格阵列 (LGA) NexFET™ 器件旨在以超薄且具有出色散热特性的最小外形尺寸封装提供最低的导通电阻和栅极电荷。基板栅格阵列 (LGA) 封装是一种带有金属接触板（而非焊球）的器件芯片级封装。

顶视图和电路配置



$R_{DS(on)}$  与  $V_{GS}$  之间的关系



产品概要

| $T_A = 25^\circ\text{C}$ |               | 值                       | 单位   |
|--------------------------|---------------|-------------------------|------|
| $V_{DS}$                 | 漏源电压          | -8                      | V    |
| $Q_g$                    | 总栅极电荷 (-4.5V) | 6.5                     | nC   |
| $Q_{gd}$                 | 栅极电荷 (栅极到漏极)  | 1.0                     | nC   |
| $R_{DS(on)}$             | 漏源导通电阻        | $V_{GS} = -1.5\text{V}$ | 30   |
|                          |               | $V_{GS} = -1.8\text{V}$ | 20   |
|                          |               | $V_{GS} = -2.5\text{V}$ | 11.5 |
|                          |               | $V_{GS} = -4.5\text{V}$ | 8.2  |
| $V_{GS(th)}$             | 阈值电压          | -0.7                    | V    |

器件信息(1)

| 器件         | 数量   | 包装介质   | 封装                              | 发货   |
|------------|------|--------|---------------------------------|------|
| CSD22205L  | 3000 | 7 英寸卷带 | 1.20mm × 1.20mm<br>基板栅格阵列<br>封装 | 卷带封装 |
| CSD22205LT | 250  |        |                                 |      |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

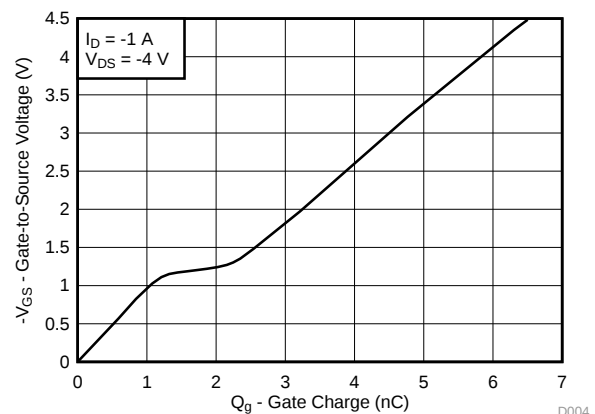
绝对最大额定值

| $T_A = 25^\circ\text{C}$ |                       | 值            | 单位               |
|--------------------------|-----------------------|--------------|------------------|
| $V_{DS}$                 | 漏源电压                  | -8           | V                |
| $V_{GS}$                 | 栅源电压                  | -6           | V                |
| $I_D$                    | 持续漏极电流 <sup>(1)</sup> | -7.4         | A                |
| $I_{DM}$                 | 脉冲漏极电流 <sup>(2)</sup> | -71          | A                |
| $P_D$                    | 功率耗散 <sup>(1)</sup>   | 0.6          | W                |
| $T_J$ ,<br>$T_{stg}$     | 工作结温、<br>储存温度         | -55 至<br>150 | $^\circ\text{C}$ |

(1)  $R_{\theta JA} = 225^\circ\text{C/W}$ （覆铜面积最小时的值）。

(2) 脉宽  $\leq 100\mu\text{s}$ ，占空比  $\leq 1\%$ 。

$R_{DS(on)}$  与  $V_{GS}$  之间的关系



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## 4 修订历史记录

| Changes from Original (May 2017) to Revision A                                                                                                                                                             | Page |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| <ul style="list-style-type: none"> <li>Changed the units for timing parameters from <math>\mu\text{s}</math> : to ns (nanoseconds) in the <a href="#">Electrical Characteristics</a> table.....</li> </ul> | 3    |

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

| PARAMETER               |                                  | TEST CONDITIONS                                                                                   | MIN                                           | TYP  | MAX   | UNIT |
|-------------------------|----------------------------------|---------------------------------------------------------------------------------------------------|-----------------------------------------------|------|-------|------|
| STATIC CHARACTERISTICS  |                                  |                                                                                                   |                                               |      |       |      |
| BV <sub>DSS</sub>       | Drain-to-source voltage          | V <sub>GS</sub> = 0 V, I <sub>D</sub> = −250 μA                                                   | −8                                            |      |       | V    |
| I <sub>DSS</sub>        | Drain-to-source leakage current  | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = −6.4 V                                                   | −100                                          |      |       | nA   |
| I <sub>GSS</sub>        | Gate-to-source leakage current   | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = −6 V                                                     | −100                                          |      |       | nA   |
| V <sub>GS(th)</sub>     | Gate-to-source threshold voltage | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = −250 μA                                      | −0.4                                          | −0.7 | −1.05 | V    |
| R <sub>DS(on)</sub>     | Drain-to-source on-resistance    | V <sub>GS</sub> = −1.5 V, I <sub>D</sub> = −0.2 A                                                 | 30                                            |      |       | mΩ   |
|                         |                                  | V <sub>GS</sub> = −1.8 V, I <sub>D</sub> = −1 A                                                   | 20      40                                    |      |       |      |
|                         |                                  | V <sub>GS</sub> = −2.5 V, I <sub>D</sub> = −1 A                                                   | 11.5      15.0                                |      |       |      |
|                         |                                  | V <sub>GS</sub> = −4.5 V, I <sub>D</sub> = −1 A                                                   | 8.2      9.9                                  |      |       |      |
|                         |                                  |                                                                                                   |                                               |      |       |      |
| g <sub>fs</sub>         | Transconductance                 | V <sub>DS</sub> = −0.8 V, I <sub>D</sub> = −1 A                                                   | 10.4                                          |      |       | S    |
| DYNAMIC CHARACTERISTICS |                                  |                                                                                                   |                                               |      |       |      |
| C <sub>ISS</sub>        | Input capacitance                | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = −4 V, f = 1 MHz                                          | 1070      1390                                |      |       | pF   |
| C <sub>OSS</sub>        | Output capacitance               |                                                                                                   | 560      730                                  |      |       | pF   |
| C <sub>RSS</sub>        | Reverse transfer capacitance     |                                                                                                   | 190      250                                  |      |       | pF   |
| R <sub>G</sub>          | Series gate resistance           |                                                                                                   | 30                                            |      |       | Ω    |
| Q <sub>g</sub>          | Gate charge total (−4.5 V)       | V <sub>DS</sub> = −4 V, I <sub>D</sub> = −1 A                                                     | 6.5      8.5                                  |      |       | nC   |
| Q <sub>gd</sub>         | Gate charge gate-to-drain        |                                                                                                   | 1.0                                           |      |       | nC   |
| Q <sub>gs</sub>         | Gate charge gate-to-source       |                                                                                                   | 1.2                                           |      |       | nC   |
| Q <sub>g(th)</sub>      | Gate charge at V <sub>th</sub>   |                                                                                                   | 0.7                                           |      |       | nC   |
| Q <sub>OSS</sub>        | Output charge                    |                                                                                                   | V <sub>DS</sub> = −4 V, V <sub>GS</sub> = 0 V | 4.1  |       |      |
| t <sub>d(on)</sub>      | Turnon delay time                | V <sub>DS</sub> = −4 V, V <sub>GS</sub> = −4.5 V,<br>I <sub>D</sub> = −1 A , R <sub>G</sub> = 0 Ω | 30                                            |      |       | ns   |
| t <sub>r</sub>          | Rise time                        |                                                                                                   | 14                                            |      |       | ns   |
| t <sub>d(off)</sub>     | Turnoff delay time               |                                                                                                   | 70                                            |      |       | ns   |
| t <sub>f</sub>          | Fall time                        |                                                                                                   | 32                                            |      |       | ns   |
|                         |                                  |                                                                                                   |                                               |      |       |      |
| DIODE CHARACTERISTICS   |                                  |                                                                                                   |                                               |      |       |      |
| V <sub>SD</sub>         | Diode forward voltage            | I <sub>S</sub> = −1 A, V <sub>GS</sub> = 0 V                                                      | −0.68      −1.0                               |      |       | V    |
| Q <sub>rr</sub>         | Reverse recovery charge          | V <sub>DS</sub> = −4 V, I <sub>F</sub> = −1 A,<br>di/dt = 200 A/μs                                | 16                                            |      |       | nC   |
| t <sub>rr</sub>         | Reverse recovery time            |                                                                                                   | 38                                            |      |       | ns   |

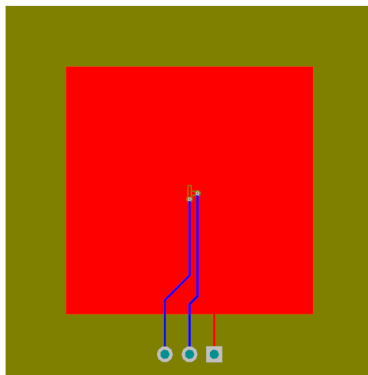
### 5.2 Thermal Information

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

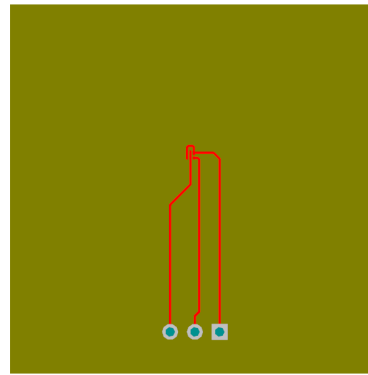
| THERMAL METRIC  |                                                       | MIN | TYP | MAX | UNIT                      |
|-----------------|-------------------------------------------------------|-----|-----|-----|---------------------------|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance <sup>(1)</sup> |     | 75  |     | $^\circ\text{C}/\text{W}$ |
|                 | Junction-to-ambient thermal resistance <sup>(2)</sup> |     | 225 |     |                           |

(1) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.



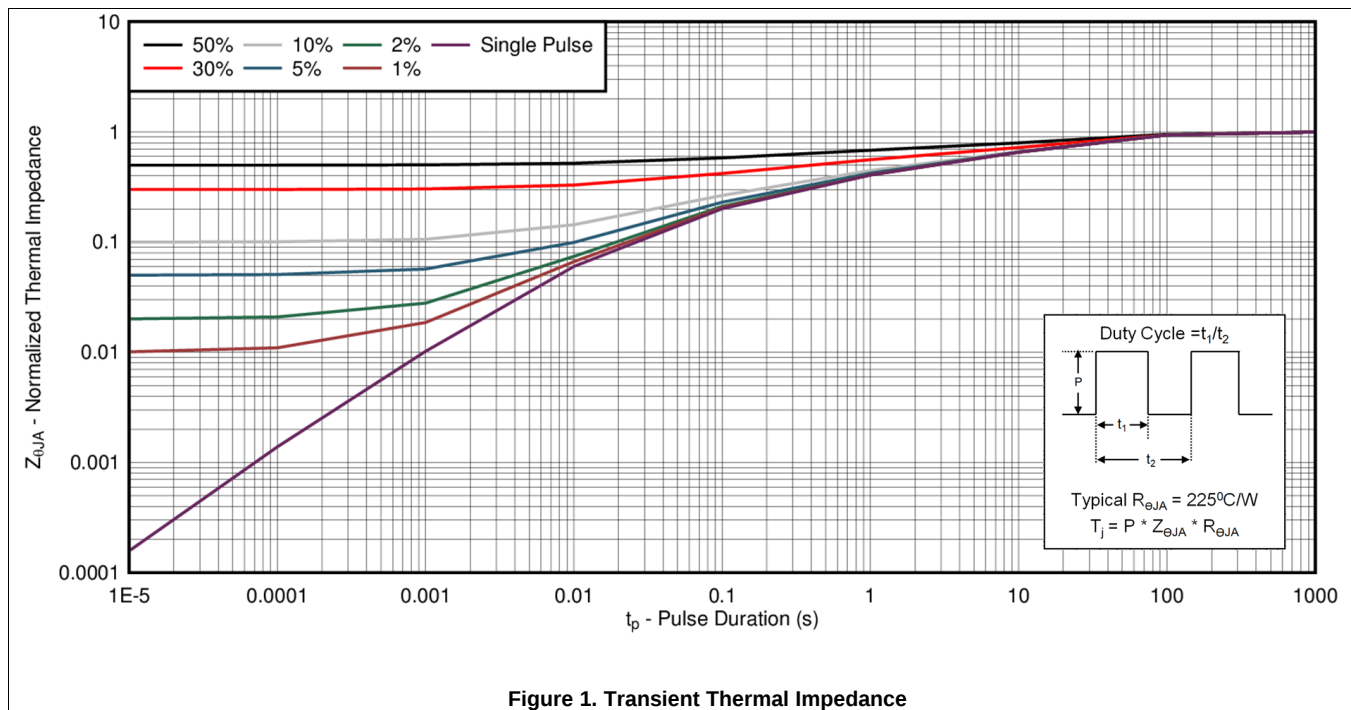
Typ  $R_{\theta JA} = 75^{\circ}\text{C/W}$   
when mounted on 1 in<sup>2</sup>  
of 2-oz Cu.



Typ  $R_{\theta JA} = 225^{\circ}\text{C/W}$  when  
mounted on  
minimum pad area  
of 2-oz Cu.

### 5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$  (unless otherwise stated)



## Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

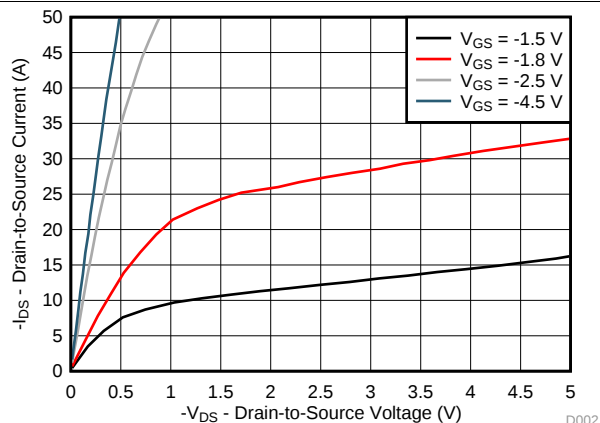


Figure 2. Saturation Characteristics

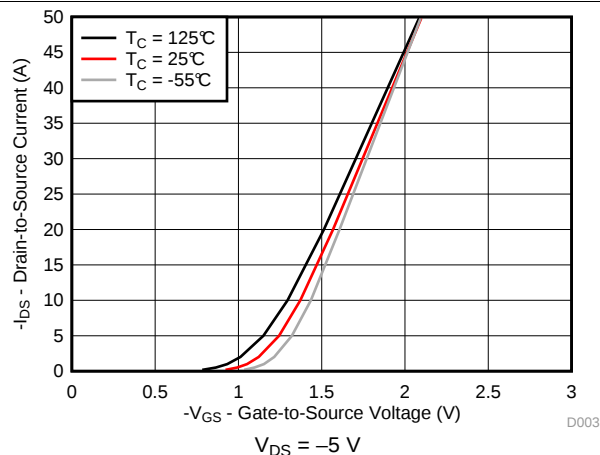


Figure 3. Transfer Characteristics

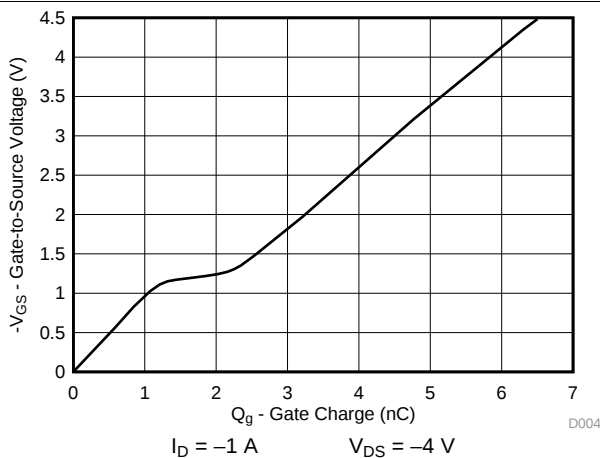


Figure 4. Gate Charge

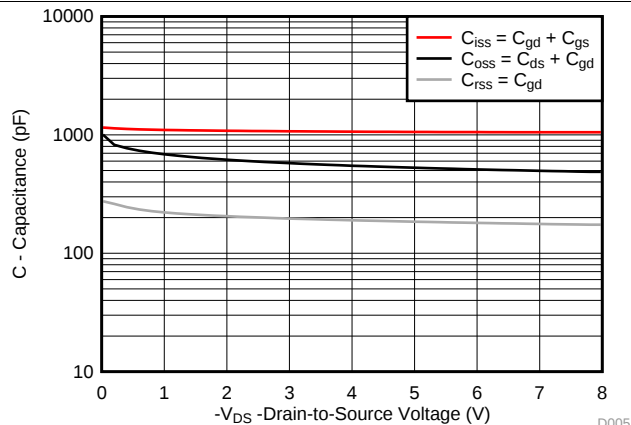


Figure 5. Capacitance

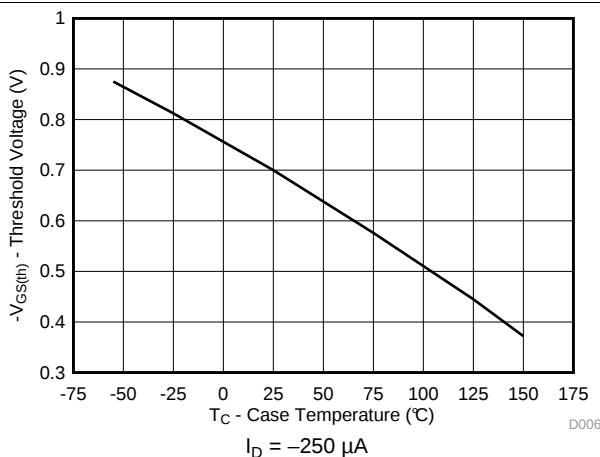


Figure 6. Threshold Voltage vs Temperature

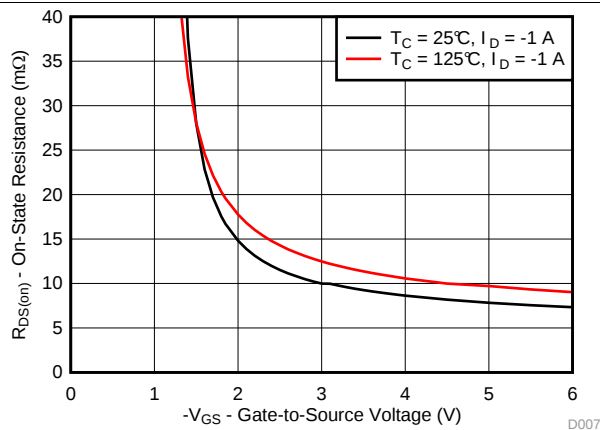


Figure 7. On-State Resistance vs Gate-to-Source Voltage

## Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

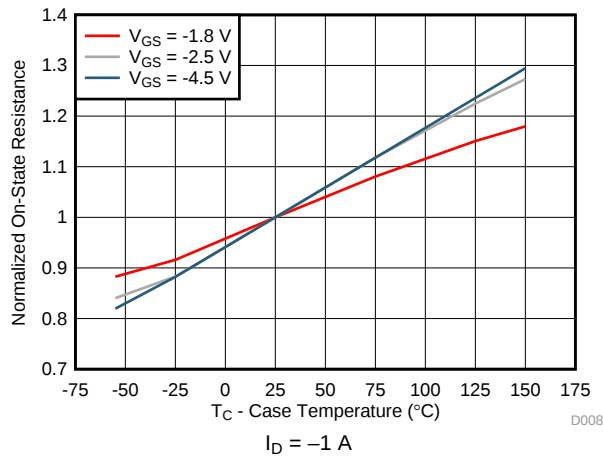


Figure 8. Normalized On-State Resistance vs Temperature

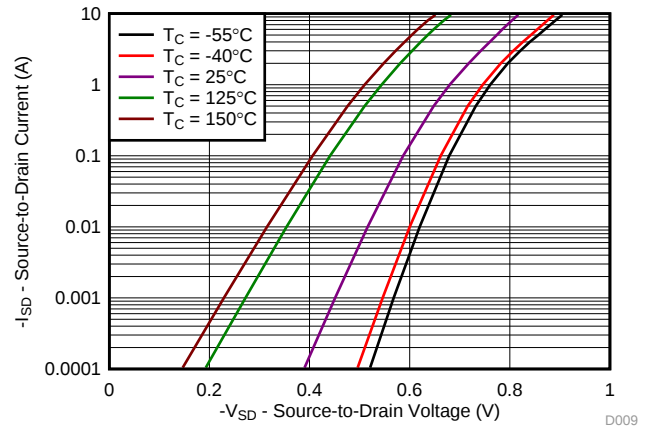


Figure 9. Typical Diode Forward Voltage

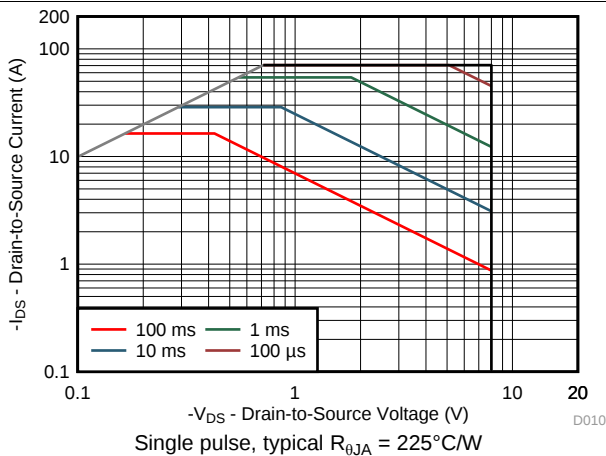


Figure 10. Maximum Safe Operating Area

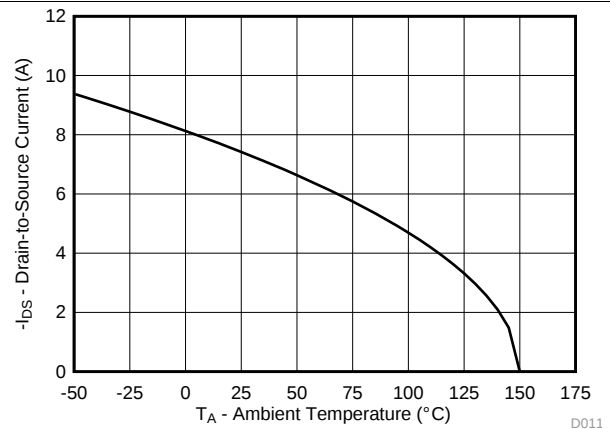


Figure 11. Maximum Drain Current vs Temperature

## 6 器件和文档支持

### 6.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。请单击右上角的通知我进行注册，即可收到所有产品更改信息每周摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 6.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

**TI E2E™ 在线社区** TI 的工程师对工程师 (E2E) 社区。此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](http://e2e.ti.com) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** TI 参考设计支持 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 6.3 商标

NexFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 6.5 Glossary

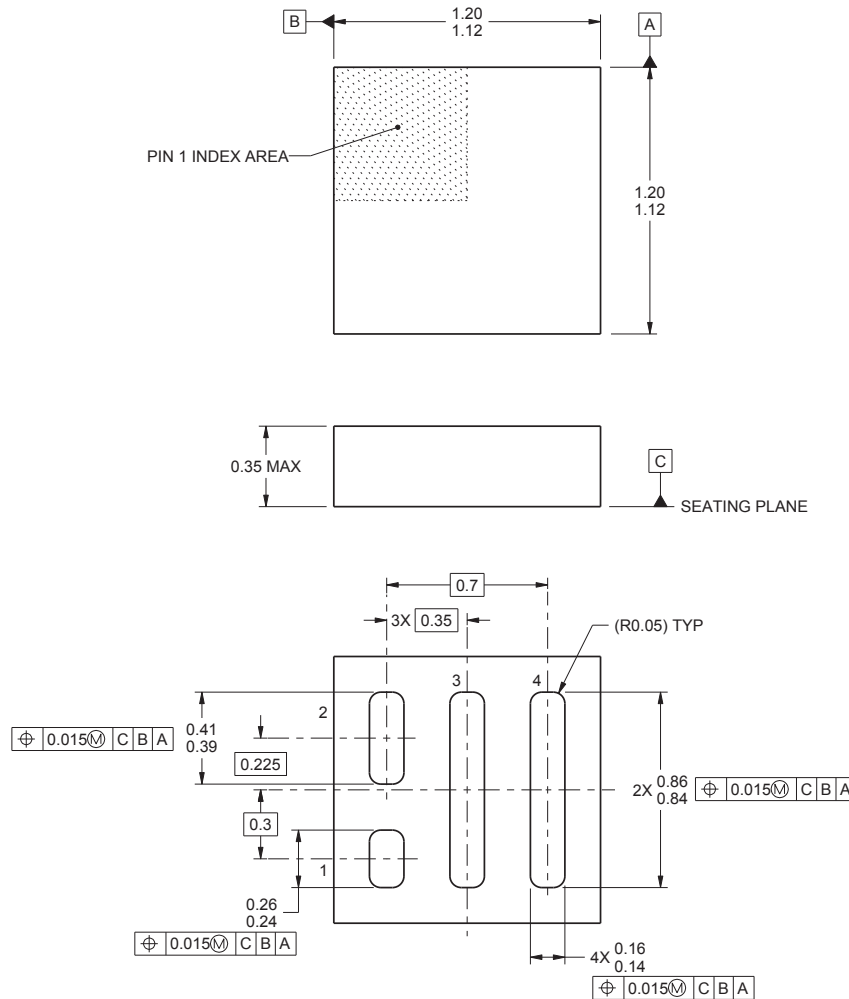
**SLYZ022** — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

### 7.1 CSD22205L 封装尺寸



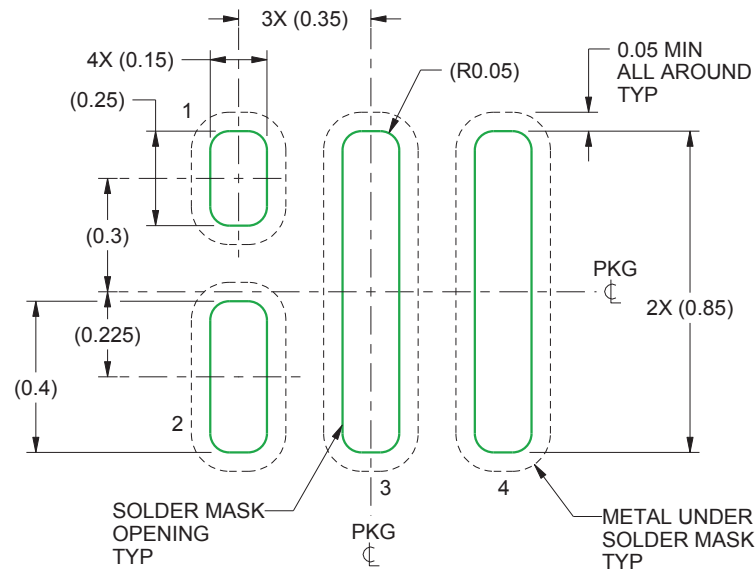
4222872/A 04/2016

1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 此封装为无铅凸点设计。凸点涂料可能有所不同。要确定确切的涂料，请参阅器件数据表或联系当地的 TI 代表。

表 1. 引脚配置表

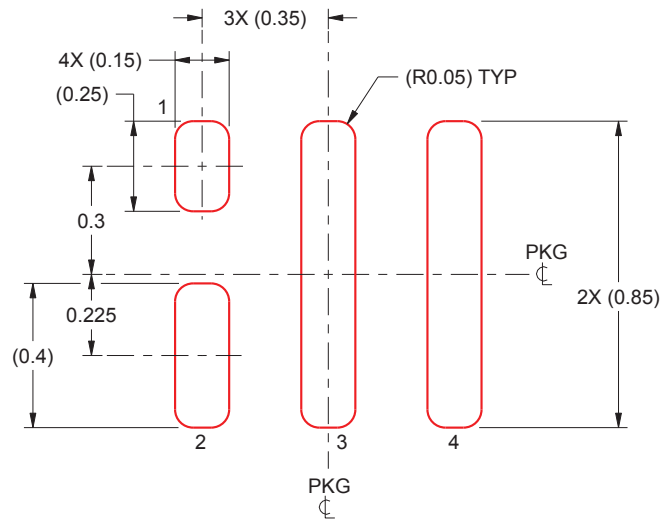
| 位置 | 名称 |
|----|----|
| 1  | 栅极 |
| 2  | 漏极 |
| 3  | 源极 |
| 4  | 漏极 |

## 7.2 焊盘布局建议



NOTE: 有关更多信息，请参阅《[QFN/SON PCB 连接](#)》(SLUA271)。

## 7.3 模版建议



NOTE: 具有漏斗形壁和圆角的激光切割孔可提供更佳的锡膏脱离。IPC-7525 可能提供替代设计建议。

如需了解针对 PCB 设计的建议电路布局，请参阅《[通过 PCB 布局技巧来减少振铃](#)》(SLPA005)。

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CSD22205L        | ACTIVE        | PICOSTAR     | YMG                | 4    | 3000           | RoHS & Green    | NIAU                                 | Level-1-260C-UNLIM   | -55 to 150   | 205                     | <a href="#">Samples</a> |
| CSD22205LT       | ACTIVE        | PICOSTAR     | YMG                | 4    | 250            | RoHS & Green    | NIAU                                 | Level-1-260C-UNLIM   | -55 to 150   | 205                     | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

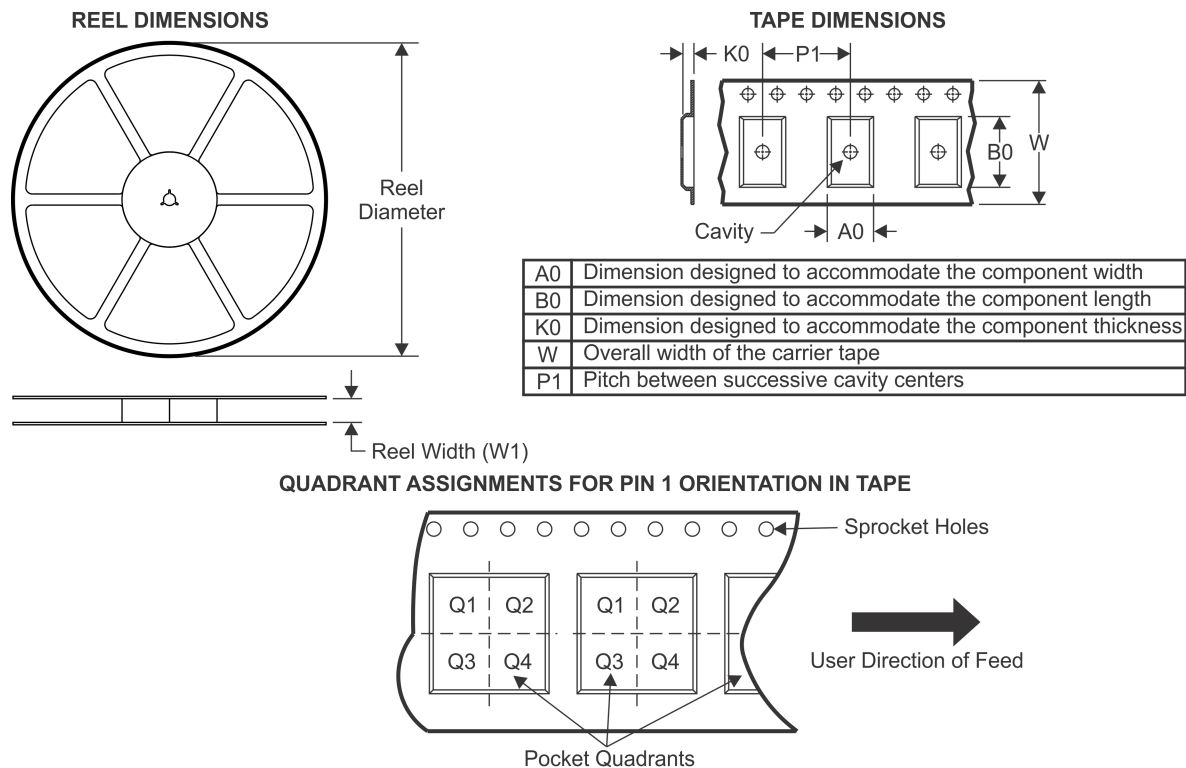
<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

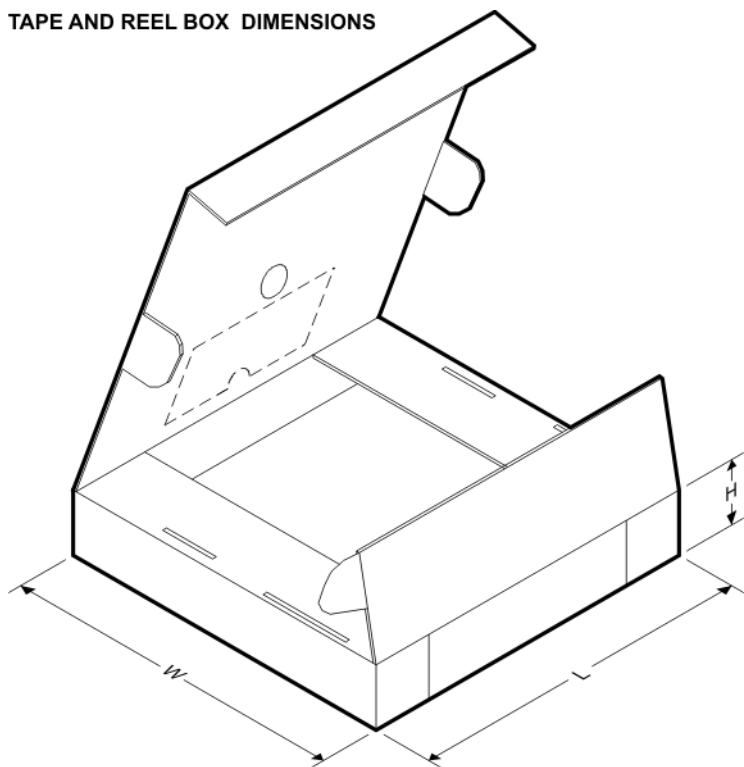


**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CSD22205L  | PICOST AR    | YMG             | 4    | 3000 | 180.0              | 8.4                | 1.26    | 1.26    | 0.42    | 4.0     | 8.0    | Q1            |
| CSD22205LT | PICOST AR    | YMG             | 4    | 250  | 180.0              | 8.4                | 1.26    | 1.26    | 0.42    | 4.0     | 8.0    | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CSD22205L  | PICOSTAR     | YMG             | 4    | 3000 | 182.0       | 182.0      | 20.0        |
| CSD22205LT | PICOSTAR     | YMG             | 4    | 250  | 182.0       | 182.0      | 20.0        |

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