

SN54AS825A, SN74AS825A 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS020B – JUNE 1984 – REVISED AUGUST 1995

- Functionally Equivalent to AMD's AM29825
- Improved I_{OH} Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs Reduce dc Loading Effects
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

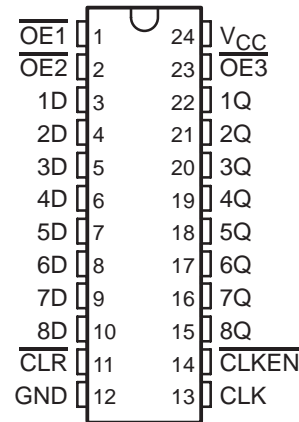
With the clock-enable (\overline{CLKEN}) input low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock (CLK) input. Taking \overline{CLKEN} high disables the clock buffer, latching the outputs. These devices have noninverting data (D) inputs. Taking the clear (\overline{CLR}) input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-enable ($\overline{OE1}$, $\overline{OE2}$, and $\overline{OE3}$) inputs can be used to place the eight outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

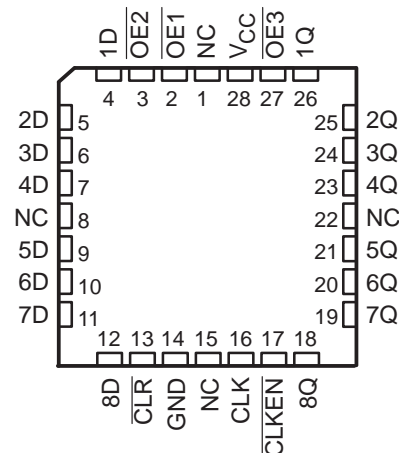
The output enables do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS825A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS825A is characterized for operation from 0°C to 70°C .

SN54AS825A . . . JT PACKAGE
SN74AS825A . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS825A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SN54AS825A, SN74AS825A 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

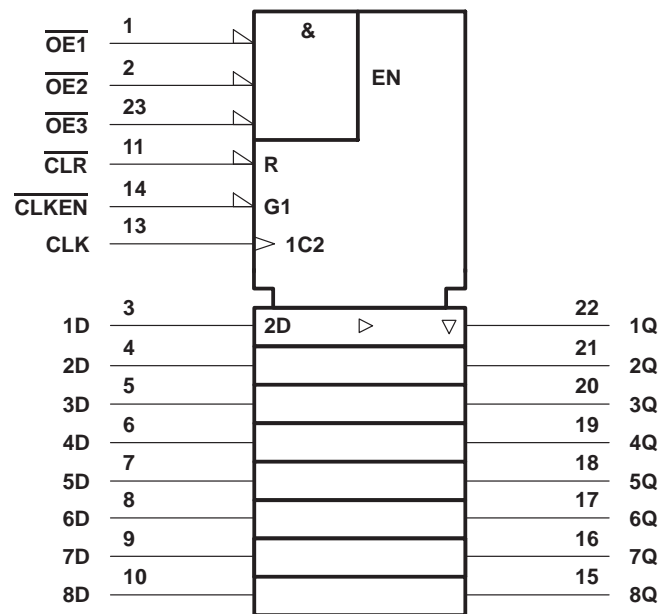
SDAS020B – JUNE 1984 – REVISED AUGUST 1995

FUNCTION TABLE
(each flip-flop)

INPUTS					OUTPUT
\overline{OE}^\dagger	\overline{CLR}	\overline{CLKEN}	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

$^\dagger \overline{OE} = H$ if any of $\overline{OE1}$, $\overline{OE2}$, or $\overline{OE3}$ are high.
 $\overline{OE} = L$ if all of $\overline{OE1}$, $\overline{OE2}$, or $\overline{OE3}$ are low.

logic symbol ‡

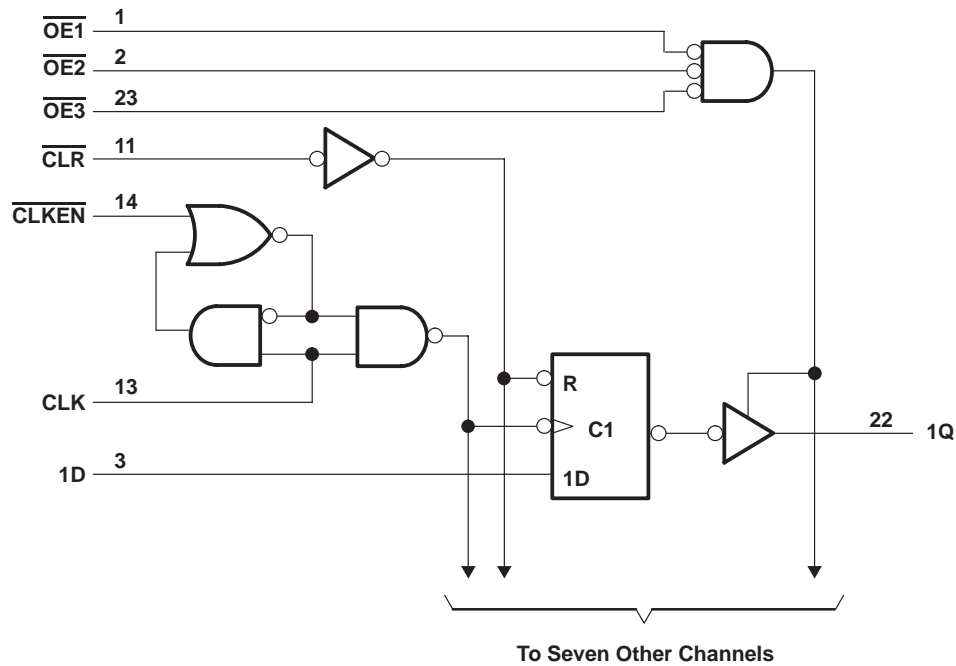


‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for the DW, JT, and NT packages.

SN54AS825A, SN74AS825A 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS020B – JUNE 1984 – REVISED AUGUST 1995

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54AS825A	-55°C to 125°C
SN74AS825A	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



SN54AS825A, SN74AS825A 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS020B – JUNE 1984 – REVISED AUGUST 1995

recommended operating conditions

		SN54AS825A			SN74AS825A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-24			-24	mA
I_{OL}	Low-level output current			32			48	mA
t_w^*	Pulse duration	\overline{CLR} low		7		4		ns
		CLK high or low		9.5		8		
t_{su}^*	Setup time before CLK \uparrow	\overline{CLR} inactive		8		8		ns
		Data		7		6		
		\overline{CLKEN} high or low		10		6		
t_h^*	Hold time after CLK \uparrow	\overline{CLKEN} low or data		0		0		ns
T_A	Operating free-air temperature	-55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS825A			SN74AS825A			UNIT
			MIN	TYPT \dagger	MAX	MIN	TYPT \dagger	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$,	$I_{OH} = -2\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -15\text{ mA}$	2.4	3.2		2.4	3.2		
		$I_{OH} = -24\text{ mA}$	2			2			
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 32\text{ mA}$		0.3	0.5				V
		$I_{OL} = 48\text{ mA}$				0.35	0.5		
I_{OZH}	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.7\text{ V}$			50			50	μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$			-50			-50	μA
I_I	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			20			20	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$			-0.5			-0.5	mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.25\text{ V}$	-30		-112	-30		-112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high		45	73		45	73	mA
		Outputs low		56	90		56	90	
		Outputs disabled		59	95		59	95	

\dagger All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

\ddagger The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



SN54AS825A, SN74AS825A 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS020B – JUNE 1984 – REVISED AUGUST 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54AS825A		SN74AS825A		
			MIN	MAX	MIN	MAX	
t _{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t _{PHL}			3.5	13.5	3.5	13	
t _{PHL}	$\overline{\text{CLR}}$	Any Q	3.5	16.5	3.5	15.5	ns
t _{PZH}	$\overline{\text{OE}}$	Any Q	4	12	4	11	ns
t _{PZL}			4	13	4	12	
t _{PHZ}	$\overline{\text{OE}}$	Any Q	1	10	1.5	8	ns
t _{PLZ}			1	10	1.5	8	

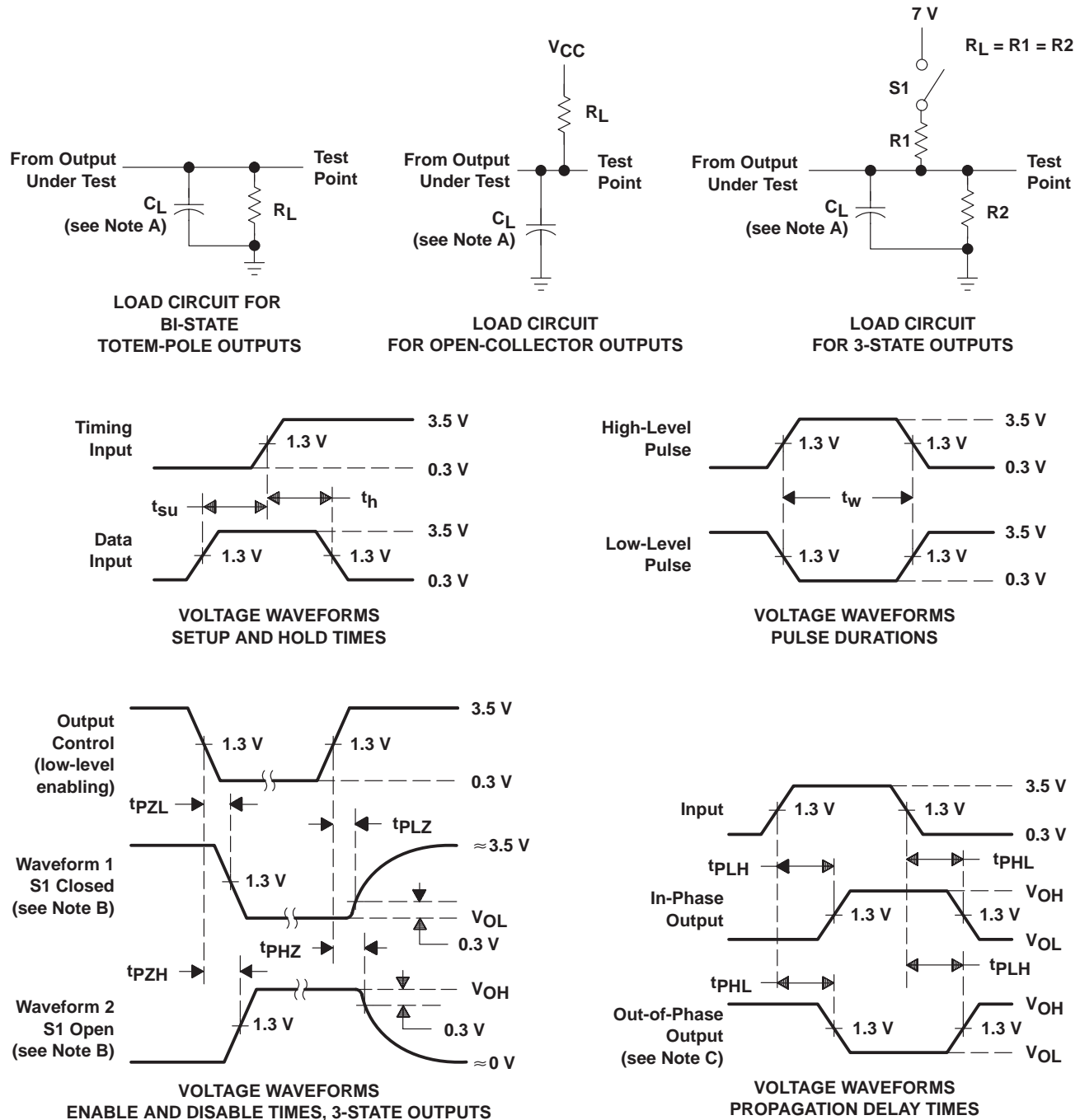
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54AS825A, SN74AS825A 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS020B – JUNE 1984 – REVISED AUGUST 1995



PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9078003M3A	ACTIVE	LCCC	FK	28	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9078003M3A SNJ54AS 825AFK	
SNJ54AS825AFK	ACTIVE	LCCC	FK	28	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9078003M3A SNJ54AS 825AFK	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated