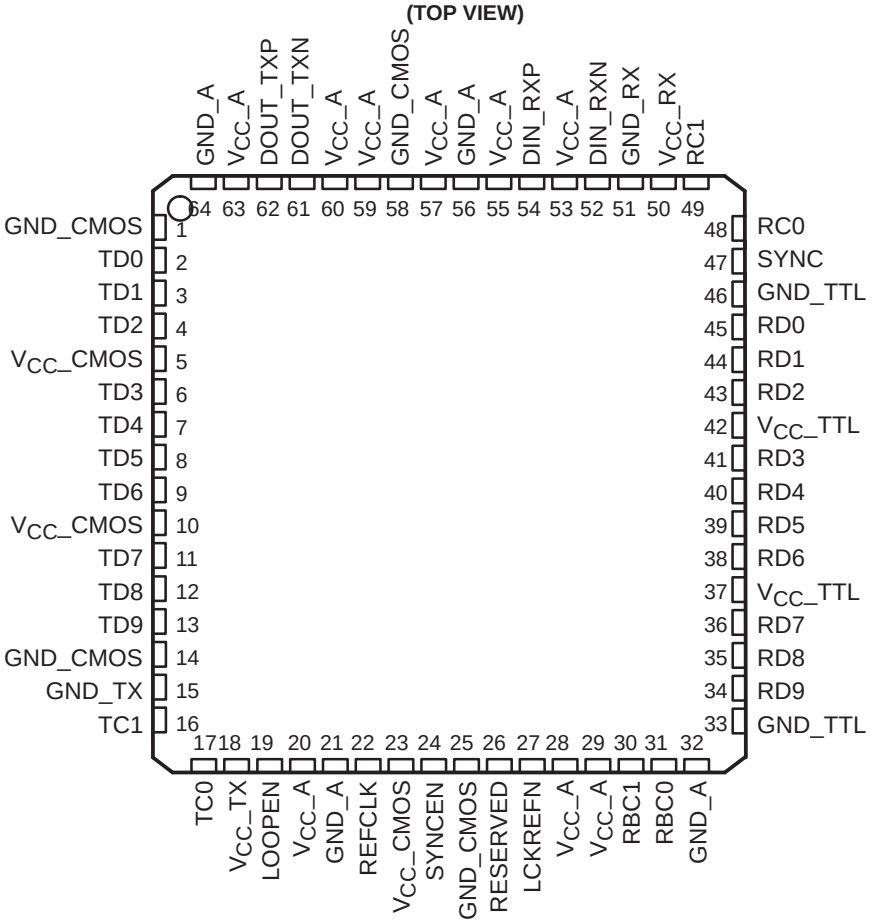
- **1.25 Gigabits Per Second (Gbps) Gigabit Ethernet Transceiver**
- **Based on the P802.3Z Specification**
- **Transmits Serial Data up to 1.25 Gbps**
- **Operates With 3.3-V Supply Voltage**
- **5-V Tolerant on TTL Inputs**
- **Interfaces to Electrical Cables/Backplane or Optical Modules**
- **PECL Voltage Differential Signaling Load, 1 V Typ With 50 Ω − 75 Ω**
- **Receiver Differential Input Voltage 200 mV Minimum**
- **Low Power Consumption**
- **64-Pin Quad Flat Pack With Thermally Enhanced Package**

description

The TNETE2201B gigabit Ethernet transceiver provides for ultra high-speed bidirectional point-to-point data transmission. This device is based on the timing requirements of the proposed 10-bit interface specification by the P802.3z Gigabit Task Force.

PHD, PJD, OR PJW PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date.7 Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1999 − 2007, Texas Instruments Incorporated

description (continued)

The intended application of this device is to provide building blocks for developing point-to-point baseband data transmission over controlled-impedance media of approximately 50 Ω to 75 Ω. The transmission media can be printed-circuit board traces, back planes, cables, or fiber optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

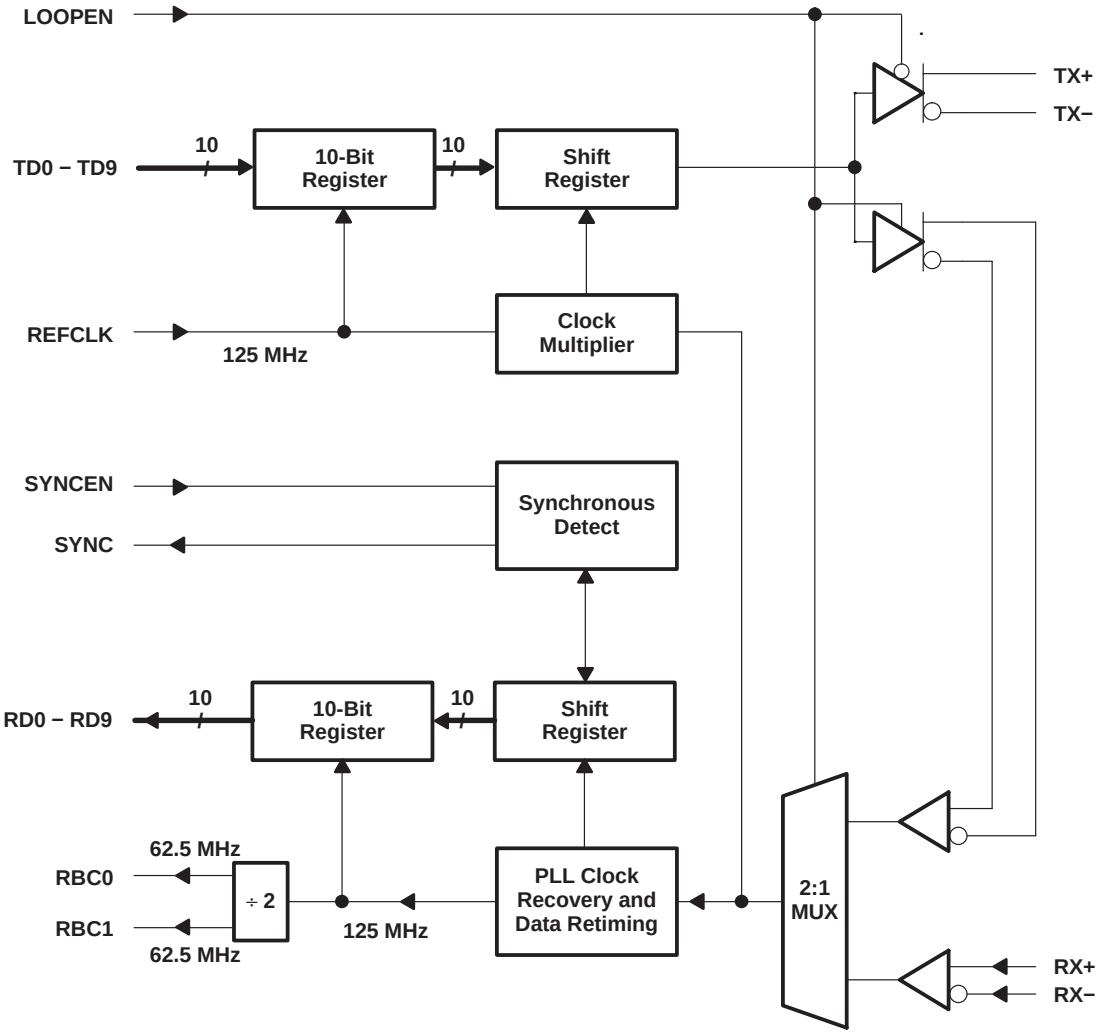
The TNETE2201B performs the data serialization and deserialization (SERDES) functions for the gigabit ethernet physical layer interface. The transceiver operates at 1.25 Gbps (typical), providing up to 1000 Mbps of bandwidth over a copper or optical media interface. The serializer/transmitter accepts 8b/10b parallel encoded data bytes. The parallel data bytes are serialized and transmitted differentially nonreturn-to-zero (NRZ) at pseudo-ECL (PECL) voltage levels. The deserializer/receiver extracts clock information from the input serial stream and deserializes the data, outputting a parallel 10-bit data byte. The 10-bit data bytes are output with respect to two receive byte clocks (RBC0, RBC1), allowing a protocol device to clock the parallel bytes in RBC clock rising edges.

The transceiver automatically locks onto incoming data without the need to prelock. However, the transceiver can be commanded to lock to the externally supplied reference clock (REFCLK) as a reset function, if needed.

The TNETE2201B provides an internal loopback capability for self-test purposes. Serial data from the serializer is passed directly to the deserializer allowing the protocol device a functional self-check of the physical interface.

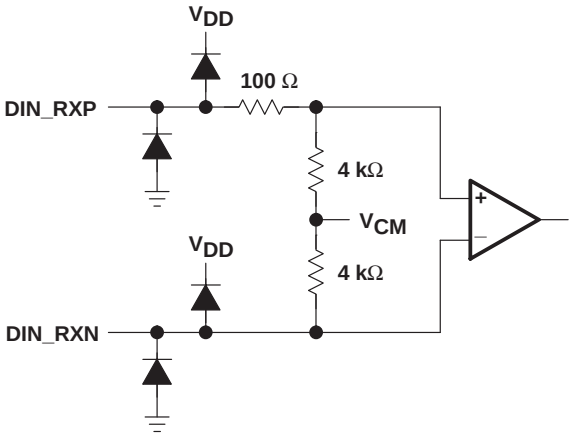
The TNETE2201B is characterized for operation from 0°C to 70°C.

functional block diagram

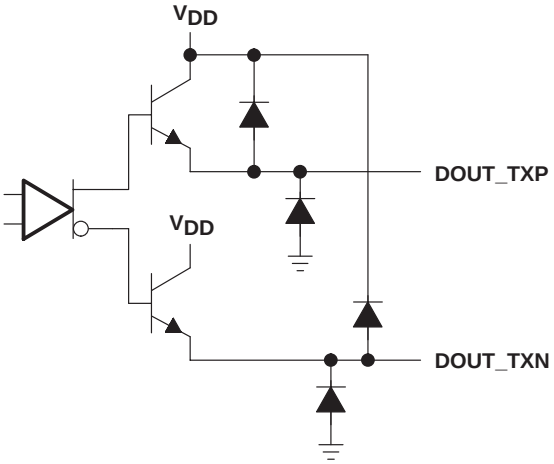


I/O structures

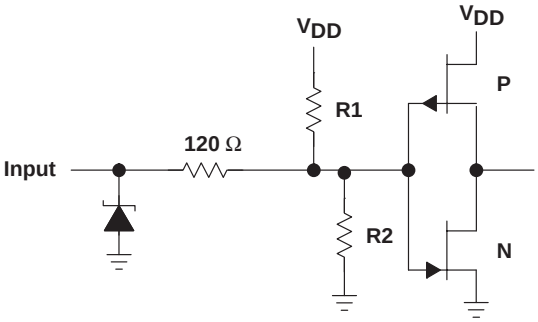
PECL inputs (DIN_RXP, DIN_RXN)



PECL outputs (DIN_TXP, DIN_TXN)

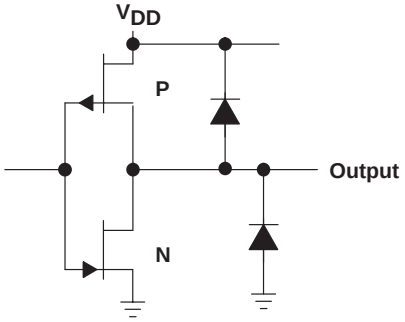


CMOS inputs (TD0 − TD9, LOOPEN, REFCLK, SYNCEN, LCKREFN)



TERMINALS	R1	R2
REFCLK, TD0 − TD9	Open Circuit	Open Circuit
LOOPEN	Open Circuit	400 kΩ
SYNCEN, LCKREFN	400 kΩ	Open Circuit

CMOS outputs (RD0 − RD9, RBC0, RBC1, SYNC)



Terminal Functions

TERMINAL			DESCRIPTION
NAME	NO.	TYPE	
I/O and DATA			
DOUT_TXP DOUT_TXN	62 61	Output	Differential output transmit. DOUT_TXP and DOUT_TXN are differential serial outputs that interface to a copper or an optical I/F module. These terminals transmit NRZ data at a rate of 1.25 Gbps. DOUT_TXP and DOUT_TXN are held static when LOOPEN is high and are active when LOOPEN is low.
DIN_RXP DIN_RXN	54 52	Input	Differential input receive. DIN_RXP and DIN_RXN together are the differential serial input interface from a copper or an optical I/F module. These terminals receive NRZ data at a rate of 1.25 Gbps and are active when LOOPEN is held low.
LCKREFN	27	Input	Lock to reference. When LCKREFN is asserted low, the receive PLL phase locks to the supplied REFCLK signal. LCKREFN prelocks or resets the receive PLL.
LOOPEN	19	Input	Loop enable. When LOOPEN is high (active), the internal loop-back path is activated. The transmitted serial data is directly routed to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The DOUT_TXP and DOUT_TXN outputs are held static during the loop-back test. LOOPEN is held low during standard operational state with external serial outputs and inputs active.
RBC0 RBC1	31 30	Output	Receive byte clock. RBC0 and RBC1 are 62.5-MHz recovered clocks used for synchronizing the 10-bit output data on RD0 − RD9. The 10-bit output data words are valid on the rising edges of RBC0 and RBC1. These clocks are adjusted to half-word boundaries in conjunction with synchronous detect. The clocks are always expanded during data realignment and never slivered or truncated. RBC0 registers bytes 1 and 3 of received data. RBC1 registers bytes 0 and 2 of received data.
RC1, RC0	49 48	Analog	Receive capacitor. RC0 and RC1 are external capacitor connections used for the receiver internal PLL filter. The recommend value for this external capacitor is 2 nF (a value of 0.1 µF can also be used, see Note 1).
RD0 − RD9	45,44,43,41 40,39,38,36 35,34	Output	Receive data. These outputs carry 10-bit parallel data output from the transceiver to the protocol layer. The data is referenced to terminals RBC0 and RBC1. Received data byte 0, which contains the K28.5 character, is byte aligned to the rising edge of RBC1. RD0 is the first bit received.
REFCLK	22	Input	Reference clock. REFCLK is an external 125 MHz input clock that synchronizes the receiver and transmitter interfaces. The transmitter uses this clock to register the 10-bit input data (TD0..TD9) for serialization. REFCLK is also used as a RX PLL preset or reference when LCKREFN is enabled.
SYNC	47	Output	Synchronous detect. SYNC is asserted high upon detection of the K28.5 character in the serial data path. SYNC is a high level for 1/2 REFCLK period. SYNC pulses are output only when SYNCEN is activated (asserted high). Note: SYNC is active on byte0 and, therefore, active on rising edge of RCB1.
SYNCEN	24	Input	Synchronous function enable. When SYNCEN is asserted high, the internal synchronization function is activated. When this function is enabled, the transceiver detects the K28.5 character (0011111010 negative beginning disparity) in the serial data stream and realigns data on byte boundaries if required. When SYNCEN is low, serial input data is unframed in RD0 − RD9.
TC1 TC0	16 17	Analog	Transmit capacitor. TC0 and TC1 are external capacitor connections used for the transmitter internal PLL filter. The recommended value of this external capacitor is 2 nF (a value of 0.1 µF can also be used, see Note 1).
TD0 − TD9	2,3,4,6 7,8,9,11 12,13	Input	Transmit data. These inputs carry 10-bit parallel data output from a protocol device to the transceiver for serialization and transmission. This 10-bit parallel data is clocked into the transceiver on the rising edge of REFCLK and transmitted as a serial stream with TD0 sent as the first bit.

NOTE 1: A filter capacitor value of 0.1 µF can be used with the following consideration: The tracking bandwidth of the PLL will be reduced due to the larger filter capacitor. This reduces the transmit and receive PLL's ability to reject low-frequency noise or wonder in the voltage supply or datastream. Care must be taken in the filtering of the supply V_{CC}_TX (terminal 18) and V_{CC}_RX (terminal 50) to reject power supply noise.

Terminal Functions (Continued)

TERMINAL			DESCRIPTION
NAME	NO.	TYPE	
POWER			
V_{CC}_A	20,28,29,53 55,57,59,60 63	Supply	Analog power. V_{CC}_A provides a supply reference voltage for the high-speed analog circuits.
V_{CC}_CMOS	5,10,23,	Supply	Digital PECL logic power. V_{CC}_CMOS provides an isolated low-noise power supply for the logic circuits.
V_{CC}_RX	50	Supply	Receiver power. V_{CC}_RX provides a low-noise supply reference voltage for the receiver high-speed analog circuits.
V_{CC}_TTL	42,37	Supply	TTL power. V_{CC}_TTL provides a supply reference voltage for the receiver TTL circuits.
V_{CC}_TX	18	Supply	Transmitter power. V_{CC}_TX provides a low-noise supply reference voltage for the transmitter high-speed analog circuits.
GROUND			
GND_A	21,32,56,64	Ground	Analog ground. GND_A provides a ground reference for the high-speed analog circuits.
GND_CMOS	1,14, 25,58	Ground	Digital PECL logic ground. GND_CMOS provides an isolated low-noise ground for the logic circuits.
GND_RX	51	Ground	Receiver ground. GND_RX provides a ground reference for the receiver circuits.
GND_TTL	33,46	Ground	TTL circuit ground. GND_TTL provides a ground for TTL interface circuits.
GND_TX	15	Ground	Transmitter ground. GND_TX provides a ground reference for the transmitter circuits.
MISCELLANEOUS			
RESERVED	26		Reserved. Internally pulled to GND, leave open or assert low.

detailed description

data transmission

The transmitter registers incoming 10-bit-wide data words (8b/10b encoded data, TD0...TD9) on the rising edge of REFCLK (125 MHz). The reference clock is also used by the serializer, which multiplies the clock by a factor of 10 providing a 1.25 Gbaud signal that is fed to the shift register. The data is then transmitted differentially at PECL voltage levels. The 8b/10b encoded data is transmitted sequentially bit 0 through 9.

transmission latency

The data transmission latency of the TNETE2201B is defined as the delay from the initial 10-bit word load to the serial transmission of bit 9. The typical transmission latency is 9 ns.

data reception

The receiver of the TNETE2201B deserializes 1.25 Gbps differential serial data. The 8b/10b data (or equivalent) is retimed based on an extracted clock from the serial data. The serial data is then aligned to the 10-bit word boundaries and presented to the protocol controller along with two receive byte clocks (RBC0, RBC1). RBC0 and RBC1 are 180 degrees out of phase and are generated by dividing down the recovered 1.25 Gbps (625 MHz) clock by 10 providing for two 62.5-MHz signals. The receiver presents the protocol device byte 0 of the received data valid on the rising edge of RBC1.

NOTE:
This allows the option of byte alignment without the use of the synchronous detection (SYNC) function by the protocol device.

The receiver PLL can lock to the incoming 1.25 GHz data without the need for a lock-to-reference preset. The received serial data rate (RX+ and RX−) should be 1.25 Gbps ±0.01% (100 ppm) for proper operation.

data reception (continued)

During a bus error condition or word alignment, the receive byte clocks RBC0 and RBC1 are stretched (never truncated). When the incoming serial data does not meet its frequency requirements, then the receive byte clock frequency is maintained at 62.5 MHz.

receive PLL operation

The receive PLL provides automatic locking to the incoming data. At power up, the maximum initial lock time is 500 µs. The PLL can also be initiated or set to phase lock to the externally supplied reference clock by enabling lock-to-reference (LCKREFN). The lock-to-reference causes the receive PLL to lock to 10× the reference clock (REFCLK) input providing a PLL preset and reset capability.

If during normal operation a transient occurs, which is defined as any arbitrary phase shift in the incoming data and/or a frequency wander of up to 200 ppm, then the PLL recovers lock within 2.4 µs. Any condition exceeding these values is considered a power-up scenario and the PLL recovers lock within 500 µs with a 0.1 µF capacitor the PLL recovers lock within 10 ms on power up (see the following note).

NOTE:

A filter capacitor value of 0.1 µF can be used with the following consideration: The tracking bandwidth of the PLL will be reduced due to the larger filter capacitor. This reduces the transmit and receive PLL's ability to reject low-frequency noise or wonder in the voltage supply or datastream. Care must be taken in the filtering of the supply V_{CC}_TX (terminal 18) and V_{CC}_RX (terminal 50) to reject power supply noise.

receiver word alignment

The TNETE2201B uses a 10-bit K28.5 character (comma character) word alignment scheme. The following sections explain how this scheme works and how it realigns itself.

comma character on expected boundary

The TNETE2201B provides 10-bit K28.5 character recognition and word alignment. The 10-bit word alignment is enabled by forcing SYCNEN high. This enables the function that examines and compares ten bits of serial input data to the K28.5 synchronization character. The K28.5 character is defined in the fibre channel standard as a pattern consisting of 0011111010 (a negative number beginning disparity) with the 7 MSBs (0011111) referred to as the comma character. The K28.5 character was implemented specifically for aligning data words. As long as the K28.5 character falls within the expected 10-bit word boundary, the received 10-bit data is properly aligned and data realignment is not required. Figure 1 shows the timing characteristics of RBC0, RBC1, SYNC and RD0 − RD9 while synchronized.

NOTE:

The K28.5 character is valid on the rising edge of RBC1.

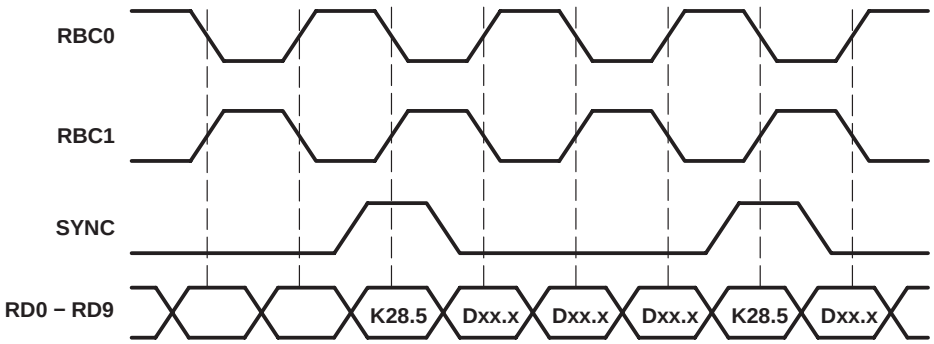


Figure 1. Synchronous Timing Characteristics Waveforms

comma character not on expected boundary

When synchronization is enabled and a K28.5 character straddles the expected 10-bit word boundary, then word realignment is necessary. Realignment or shifting the 10-bit word boundary truncates the character following the misaligned K28.5, but the following K28.5 and all subsequent data is aligned properly as shown in Figure 2. The 10b specification requires that RCLK cycles can not be truncated and can only be stretched or stalled in their current state during realignment. With this design the maximum stretch that occurs is an extra 10 bit times. This occurs during a worst case scenario when the K28.5 is aligned to the falling edge of RBC1 instead of the rising edge. This system transmits a minimum of three consecutively ordered K28.5 data sets between frames and ensures that the receiver sees at least two of K28.5 sets (the fabric is allowed to drop one). Figure 2 shows the timing characteristics of the data realignment.

Systems that do not require framed data can disable byte alignment by tying SYNCEN low.

When a synchronization character is detected the SYNC signal is asserted high and is aligned with the K28.5 character. The duration of the SYNC-signal pulse is equal to the duration of the data which is half an RCLK period.

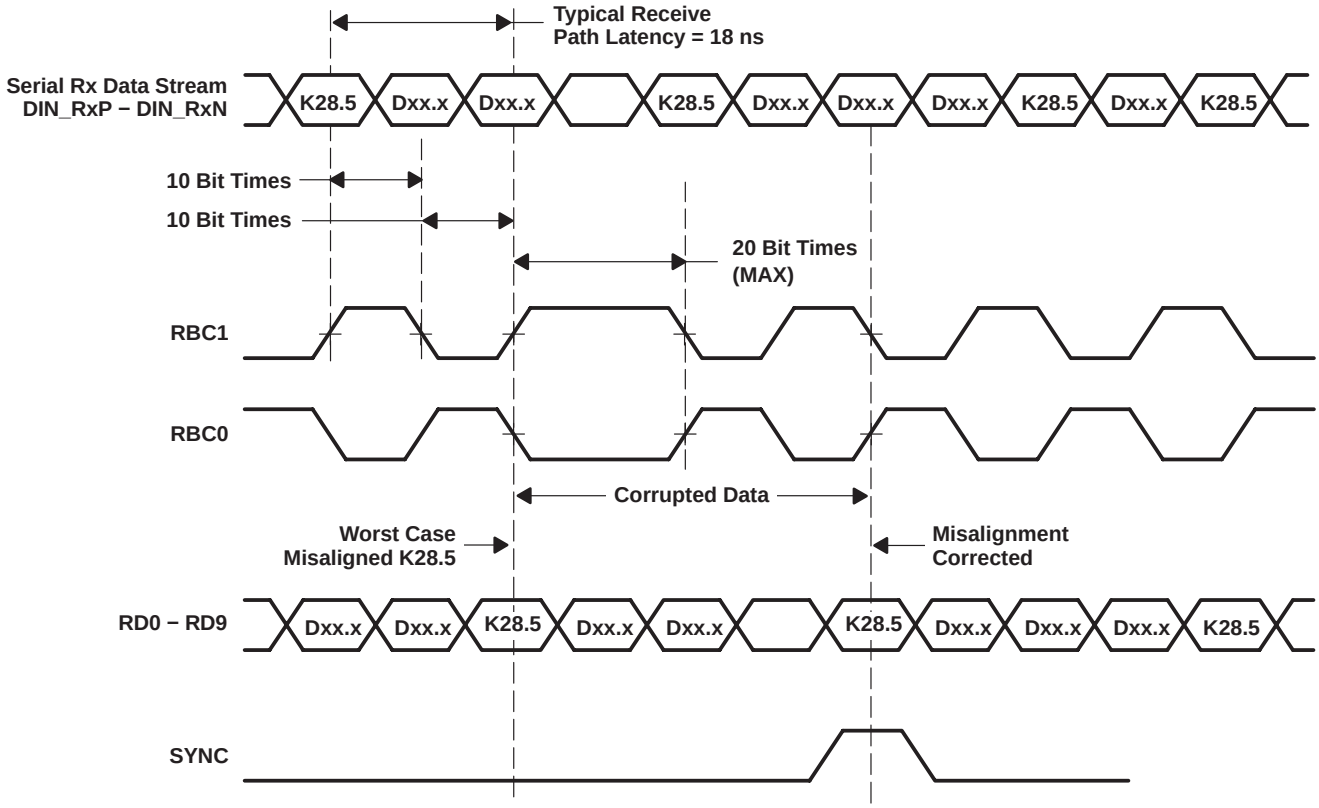


Figure 2. Word Realignment Timing Characteristics Waveforms

data reception latency

The serial-to-parallel data latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word with RD0 received as first bit. The receive latency is typically 18 ns.

loop-back testing

The transceiver can provide a self-test function by enabling (LOOPEN to high level) the internal loop-back path. Enabling LOOPEN causes serially transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. The external differential output is held in a static state during loop-back testing.

absolute maximum ratings†

Supply voltage, V_{CC} (see Note 2) . . . . . −0.5 to 4.0 V
Input voltage, V_I (TTL, PECL) . . . . . −0.5 to 4.0 V
Output current I_O, (TTL) . . . . . 50 mA
Output current I_O, (PECL) . . . . . −50 mA
Voltage range at any terminal . . . . . −0.5 to V_{CC} + 0.5 V
Electrostatic discharge, 5-V tolerant input terminals (see Note 3) . . . . . Class 1, A:1 kV, B:150 V
Electrostatic discharge, all other terminals (see Note 3) . . . . . Class 1, A:2 kV, B:200 V
Characterized free-air operating temperature range . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. All voltage values, except differential I/O bus voltages, are with respect to network ground.
3. This parameter is tested in accordance with MIL-PRF-38535.

recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3.14	3.3	3.47	V
Supply current, I_{CC} (static)	Static pattern†		180	260	mA
Power dissipation, P_D (static)	Outputs open, Static pattern†		590	900	mW
Supply current, I_{CC} (dynamic)	K28.5		240	330	mA
Power dissipation, P_D (dynamic)	Outputs open, K28.5		790	1150	mW
Operating free-air temperature, T_A		0		70	°C

† Power (static pattern) = 125 MHz to the receiver and 5 ones and 5 zeros to the transmitter.

reference clock (REFCLK) timing requirements over recommended operating conditions (unless otherwise noted)†

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Frequency		TYP − 0.01%	125	TYP + 0.01%	MHz
Accuracy		−100		100	ppm
Duty cycle		40%	50%	60%	
Jitter	Random and deterministic			40	ps

† This clock should be crystal referenced to meet the requirements of the this table. The maximum rate of frequency change specified is valid after 10 seconds from power on.

electrical characteristics over recommended operating conditions (unless otherwise noted)

TTL Signals: TD0 .. TD9, REFCLK, LOOPEN, SYNCEN, SYNC, RD0 .. RD9, RBC0, RBC1, LCKREFN

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN,	I_{OH} = −400 µA	2.4	3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN,	I_{OL} = 1 mA		0.25	0.4	V
V_{IH}	High-level input voltage				2		5.5	V
V_{IL}	Low-level input voltage						0.8	V
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.4 V			40	µA
		REFCLK	V_{CC} = MAX,	V_I = 2.4 V			900	µA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V	−40			µA
		REFCLK	V_{CC} = MAX,	V_I = 0.4 V	−900			µA
c_i	Input capacitance						4	pF

TRANSMITTER SECTION

differential electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OD} \rvert_P$	Driver differential output voltage (peak) ($\lvert T_XP - T_XN \rvert$)	R_L = 75 Ω,	See Figure 3	550		1100	mV
		R_L = 50 Ω,	See Figure 3	550		1100	
V_{OC}	Driver common-mode output voltage	R_L = 75 Ω			2100		mV

differential switching characteristics over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Serial data deterministic jitter (peak-to-peak)	Differential output jitter			80	ps
	Serial data total jitter (peak-to-peak)	Differential output jitter			192	ps
t_{r3}	Differential signal rise time (20% to 80%)	R_L = 75 Ω, C_L = 5 pF, See Figure 3			300	ps
t_{f3}	Differential signal fall time (20% to 80%)				300	ps

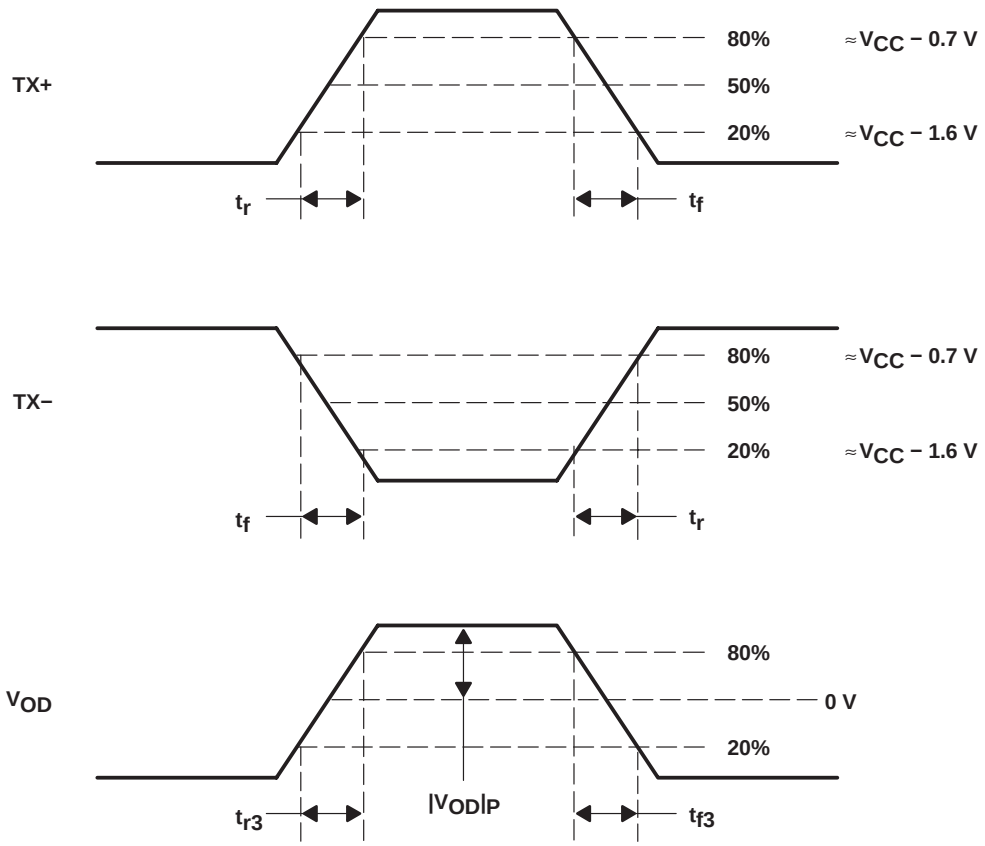


Figure 3. Differential and Common-Mode Output Voltage Definitions

transmitter timing requirements over recommended operating conditions (unless otherwise noted)

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{su1}	Setup time, TD0 − TD9 valid to REFCLK ↑	See Figure 4	2			ns
t_{h1}	Hold time, REFCLK ↑ to TD0 − TD9 invalid	See Figure 4	1			ns
	Parallel-to-serial data latency			9		ns

transmit interface timing

The transmit interface is defined in the 10 b spec as the 10-bit parallel data input to the physical layer for serial transmission. The timing values are specified from REFCLK midpoint to valid input signal levels or from valid input signal levels to REFCLK midpoint.

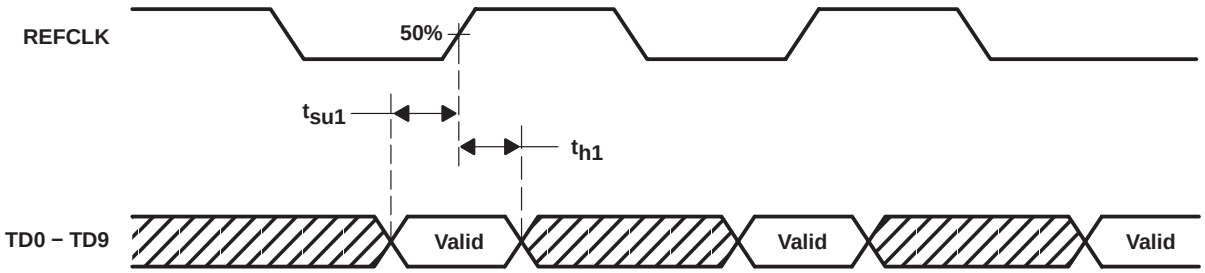


Figure 4. Transmit 10-Bit Interface Timing Waveforms

RECEIVER SECTION

differential electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{ID}\|_P$	Receive input voltage (peak) ($\|R_XP - R_XN\|$)	See Figure 5	200		1300	mV

receiver and phase-locked loop performance characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT†
Jitter tolerance	See P802.3Z specification			74.9%	UI
Data acquisition lock time	From power up at 2 nF capacitor value			500	µs
	From power up at 0.1 µF capacitor value (See Note 4)			10	ms
Data relock time	From synchronization loss			2500	ns

† UI is the unit interval of a single bit (800 ps).

NOTE 4: A filter capacitor value of 0.1 µF can be used with the following consideration: The tracking bandwidth of the PLL will be reduced due to the larger filter capacitor. This reduces the transmit and receive PLL's ability to reject low-frequency noise or wonder in the voltage supply or datastream. Care must be taken in the filtering of the supply V_{CC}_TX (terminal 18) and V_{CC}_RX (terminal 50) to reject power supply noise.

receive clock timing requirements over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	Clock frequency, RBC0			62.5		MHz
f_{clk}	Clock frequency, RBC1 (180 deg out of phase with RBC0)			62.5		MHz
t_{r4}	Data rise time	See Figure 6	0.7		4	ns
t_{f4}	Data fall time	See Figure 6	0.7		4	ns
t_{r5}	Rise time, single-ended output signal on RBC0 or RBC1	See Figure 6	0.7		2	ns
t_{f5}	Fall time, single-ended output signal on RBC0 or RBC1	See Figure 6	0.7		2	ns
	Duty cycle, RBC0 or RBC1		40%		60%	
$t_{(skew)}$	Skew time, RBC1 ↑ to RBC0 ↑	See Figure 7	7.5	8	8.5	ns
t_{su2}	Setup time, RD0 − RD9, SYNC valid to RBC0 ↑	See Figure 7	2.5			ns
t_{su3}	Setup time, RD0 − RD9, SYNC valid to RBC1 ↑	See Figure 7	2.5			ns
t_{su4}	Setup time, RBC1 ↑ to RD0 − RD9, SYNC invalid	See Figure 7	1.5			ns
t_{su5}	Setup time, RBC1 ↑ to RD0 − RD9, SYNC invalid	See Figure 7	1.5			ns
	Serial-to-parallel data latency			18		ns

† $t_{(drift)}$ is the minimum time for RBC0 or RBC1 to drift from 63.5 MHz to 64.5 MHz or from 60 MHz to 59 MHz from the RCLK lock value. This is applicable under all input signal conditions with PLL locked to the REFCLK of DATA signals.

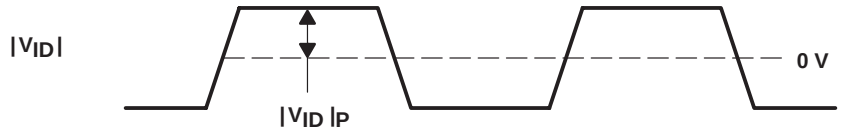


Figure 5. Differential Input Voltage (Peak-to-Peak) Timing Waveform

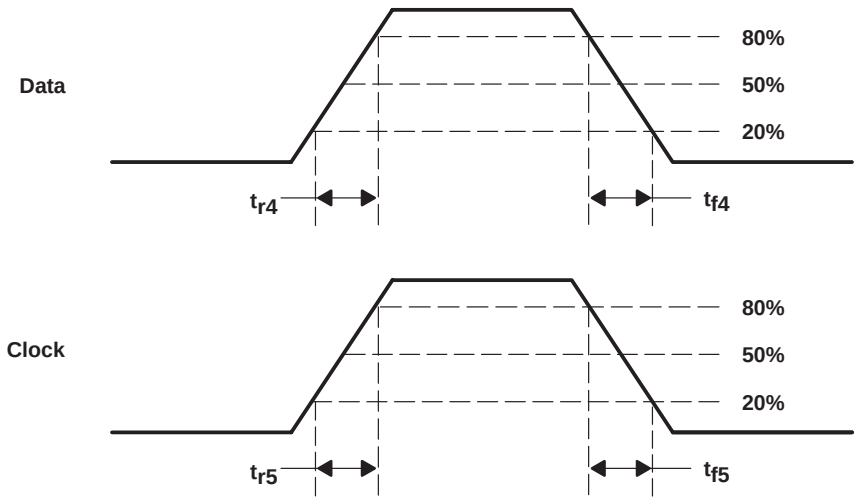


Figure 6. Receiver Data Measurement Levels

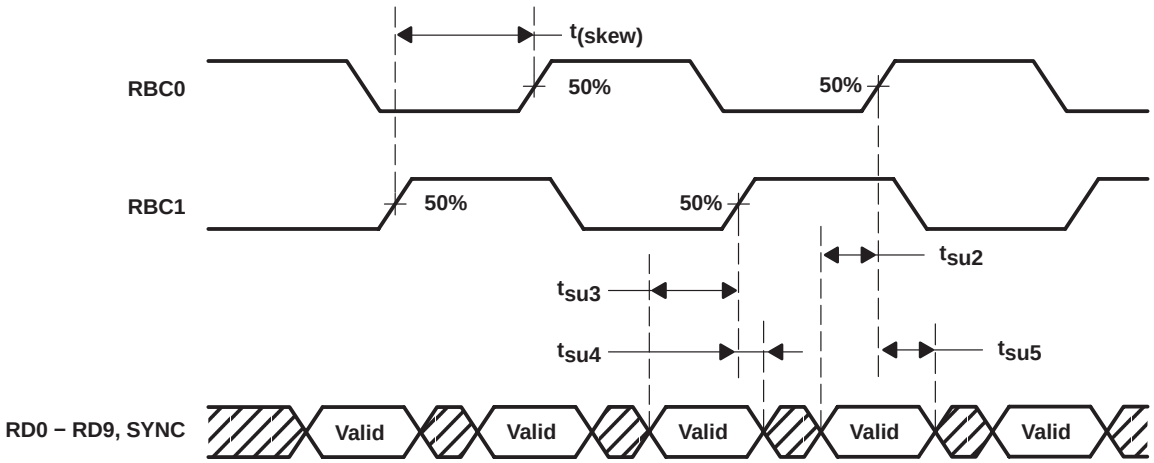
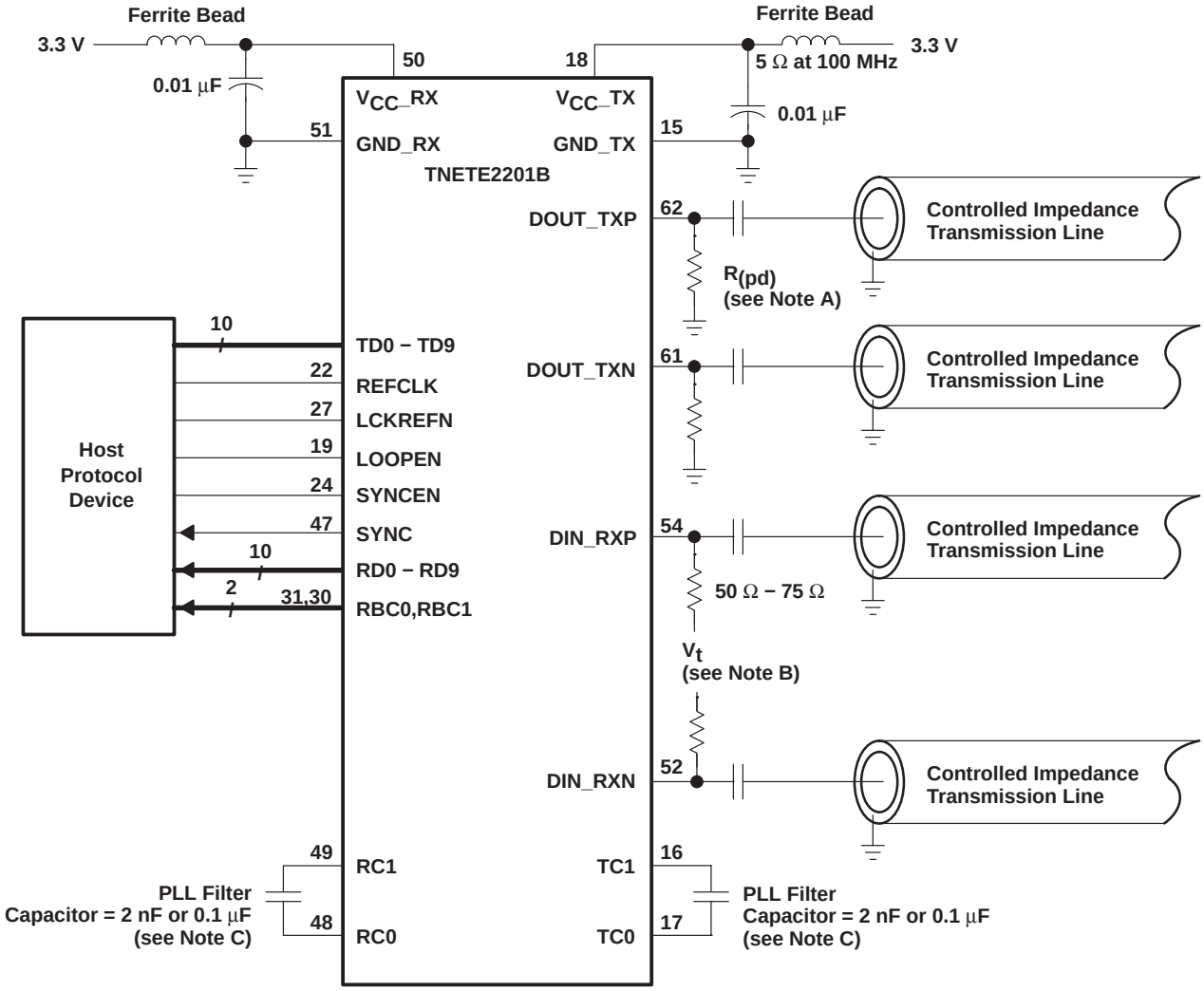


Figure 7. Receiver Interface Timing Waveforms

APPLICATION INFORMATION



NOTES: A. R(pd) − This value is set to match the falling edge to rising edge transistion times, typically 150 Ω. to 220 Ω..

B. V_t (termination voltage): $V_t = V_{CC} - 1.3$ V, if ac coupled
$V_t = V_{CC} - 2$ V, if directly coupled.

C. A filter capacitor value of 0.1 µF can be used with the following consideration: The tracking bandwidth of the PLL will be reduced due to the larger filter capacitor. This reduces the transmit and receive PLL's ability to reject low-frequency noise or wonder in the voltage supply or datastream. Care must be taken in the filtering of the supply V_{CC}_TX (terminal 18) and V_{CC}_RX (terminal 50) to reject power supply noise.

Figure 8. Typical Application Circuit

MECHANICAL INFORMATION

The TNETE2201B incorporates the latest development in TI's package line. The new patent-pending design, designated the PWP, delivers thermal performance comparing to a heat-spreader design in a true low-profile package. The PWP for the TNETE2201B is designed to maximize heat transfer away from the die through the top of the chip. As seen in Figures 9 and 10 the bottom of the leadframe is deep downset towards the top of the chip, providing a thermal path away from the die and board. All this has been accomplished without exceeding the 1.15 mm height of the TQFP. This package in the 10mm × 10mm TQFP (PJD) provides a thermal resistance $R_{\theta JA}$ of 40°C/W and the package in the 14mm × 14mm TQFP (PHD) provides a $R_{\theta JA}$ of 40°C/W.

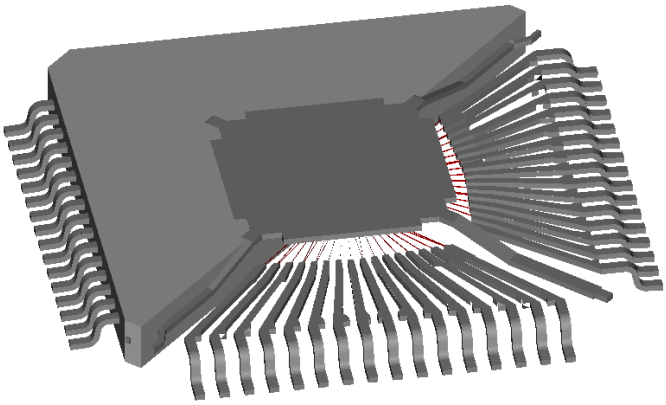


Figure 9. Heat-Spreader Design

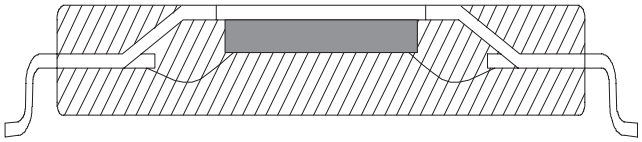


Figure 10. Leadframe Downset

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TNETE2201BPHD	ACTIVE	HTQFP	PHD	64	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TNETE2201B	Samples
TNETE2201BPJD	ACTIVE	HTQFP	PJD	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TNETE2201B	Samples
TNETE2201BPJW	ACTIVE	HTQFP	PJW	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TNETE2201B	Samples
TNETE2201BPJWG4	ACTIVE	HTQFP	PJW	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TNETE2201B	Samples
TNETE2201BPJWR	ACTIVE	HTQFP	PJW	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TNETE2201B	Samples
TNETE2201BPJWRG4	ACTIVE	HTQFP	PJW	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TNETE2201B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

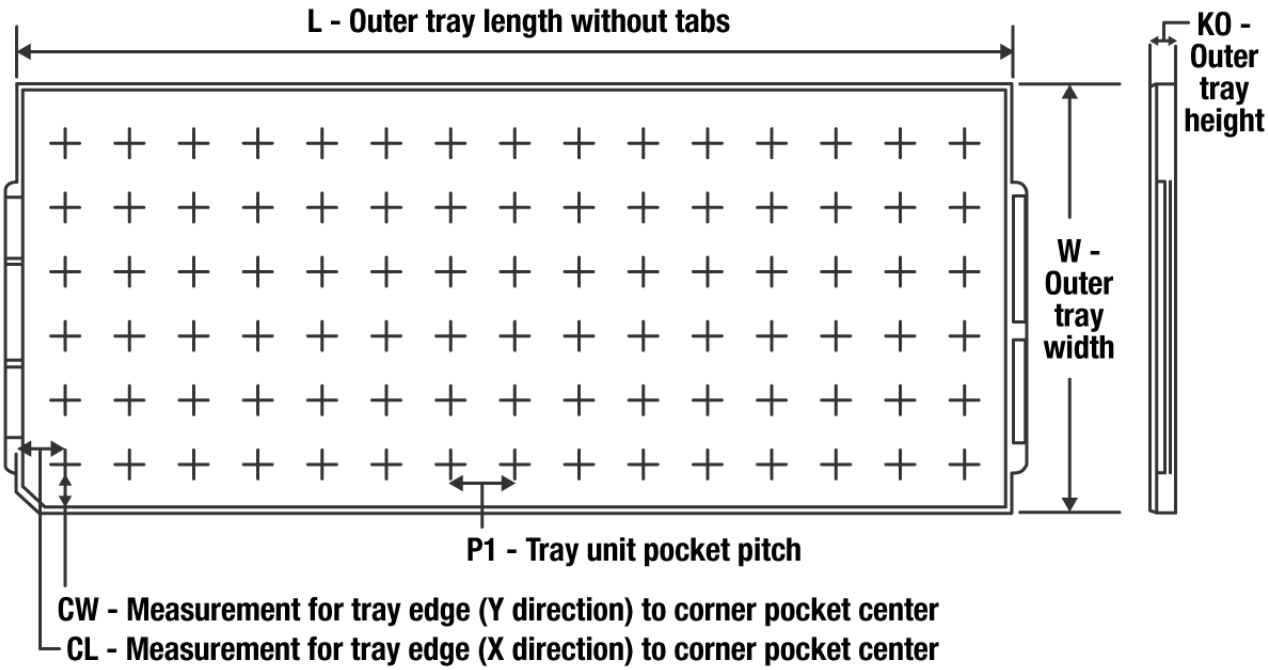
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TNETE2201BPHD	PHD	HTQFP	64	90	6 X 15	150	315	135.9	7620	20.3	15.4	15.45
TNETE2201BPJD	PJD	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
TNETE2201BPJW	PJW	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
TNETE2201BPJWG4	PJW	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

GENERIC PACKAGE VIEW

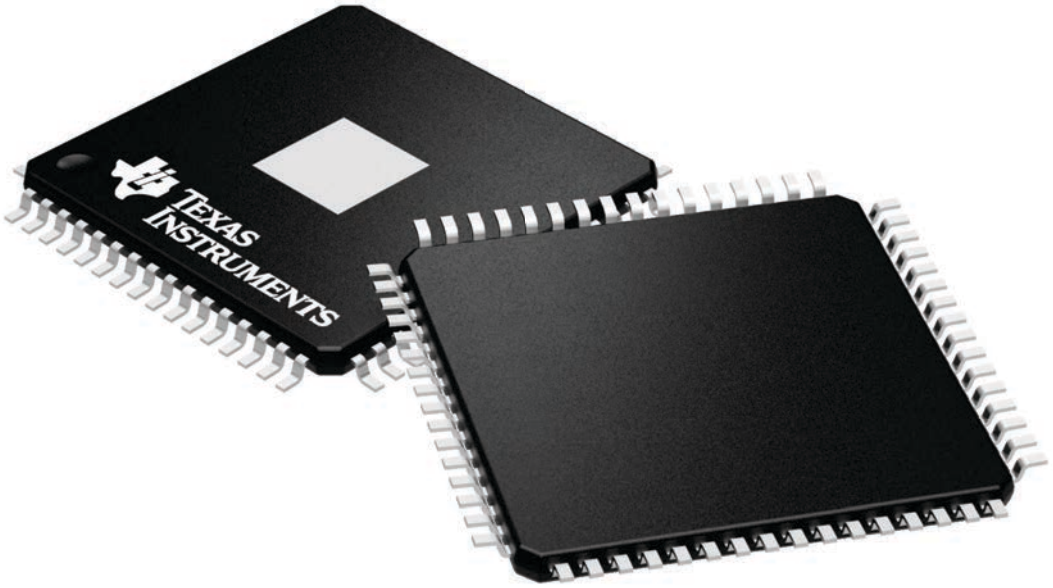
PHD 64

HTQFP - 1.20 mm max height

14 x 14, 0.8 mm pitch

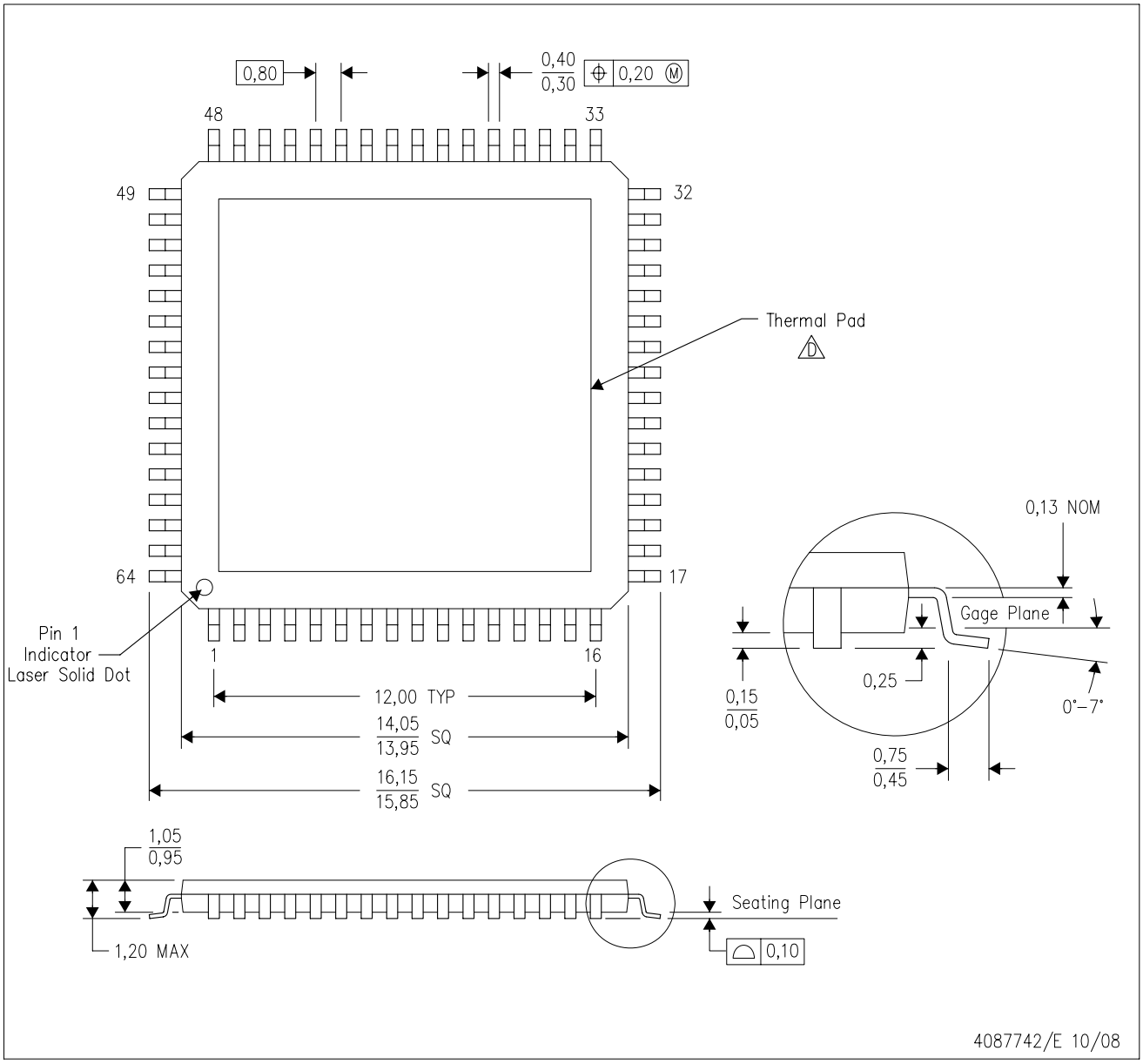
QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224851/A

PHD (S-PQFP-G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

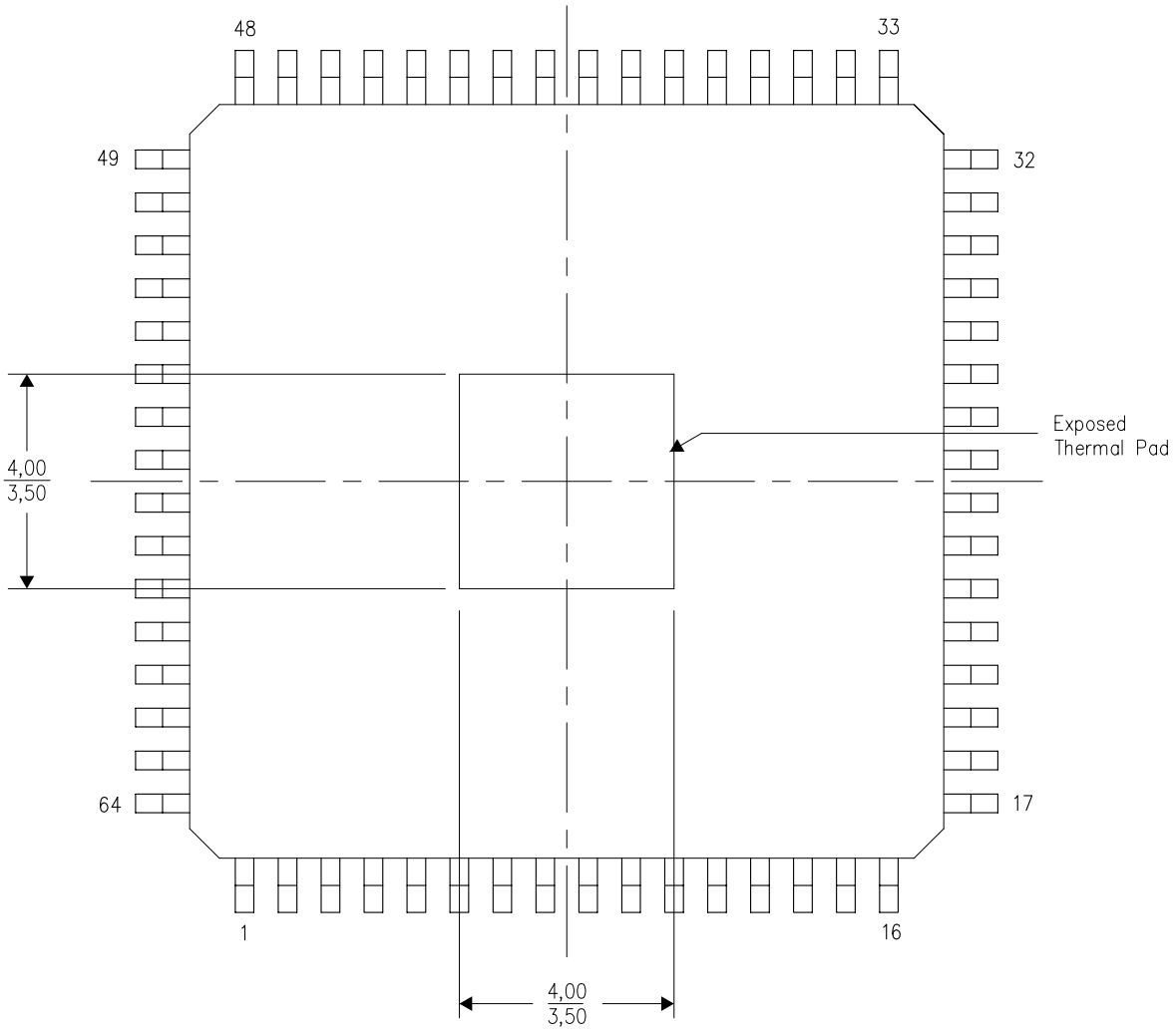
PHD (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

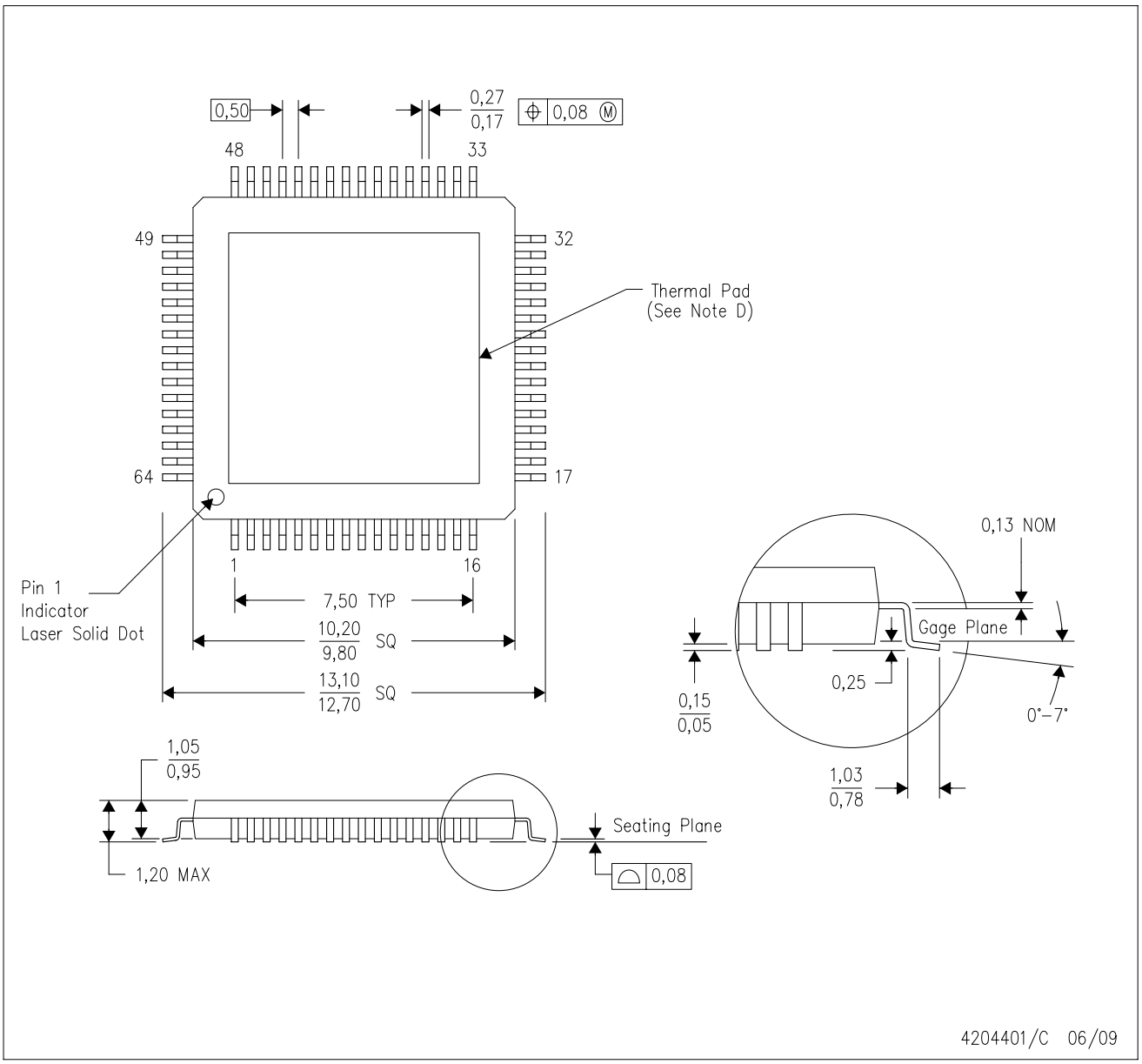
Exposed Thermal Pad Dimensions

4206328–2/H 04/11

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PJW (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. The package thermal performance may be enhanced by attaching an external heatsink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS–026

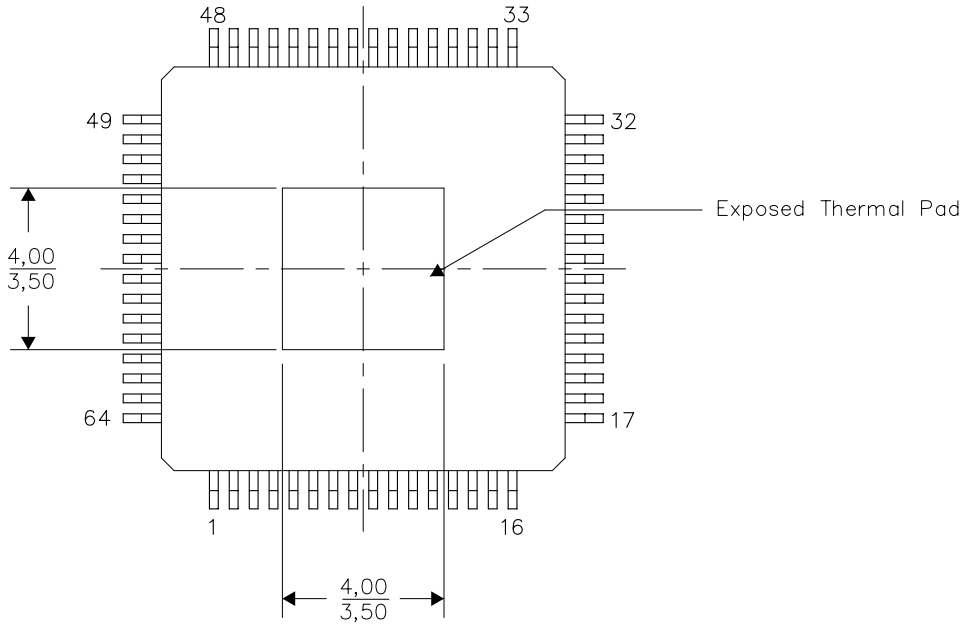
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

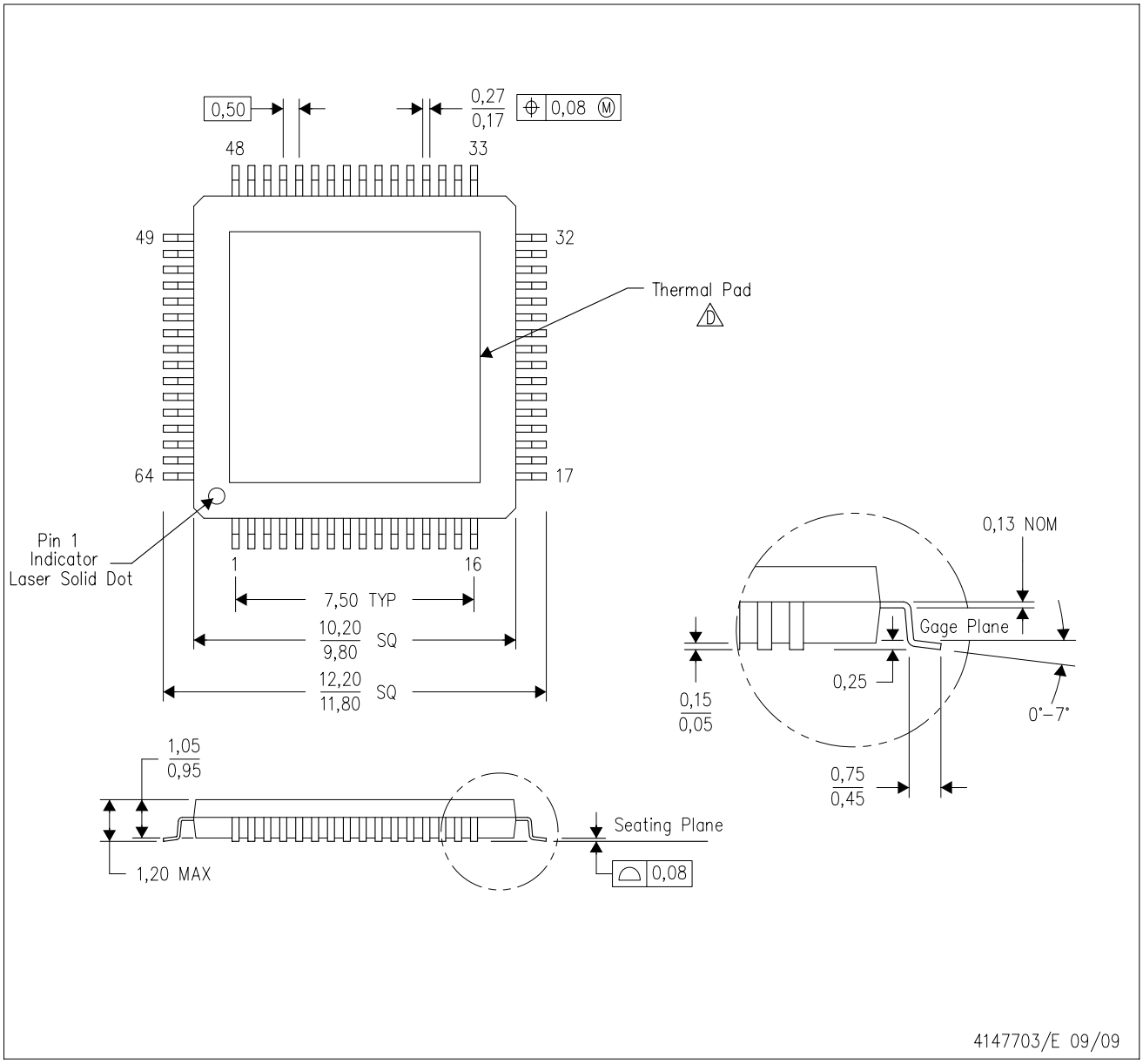


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PJD (S-PQFP-G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

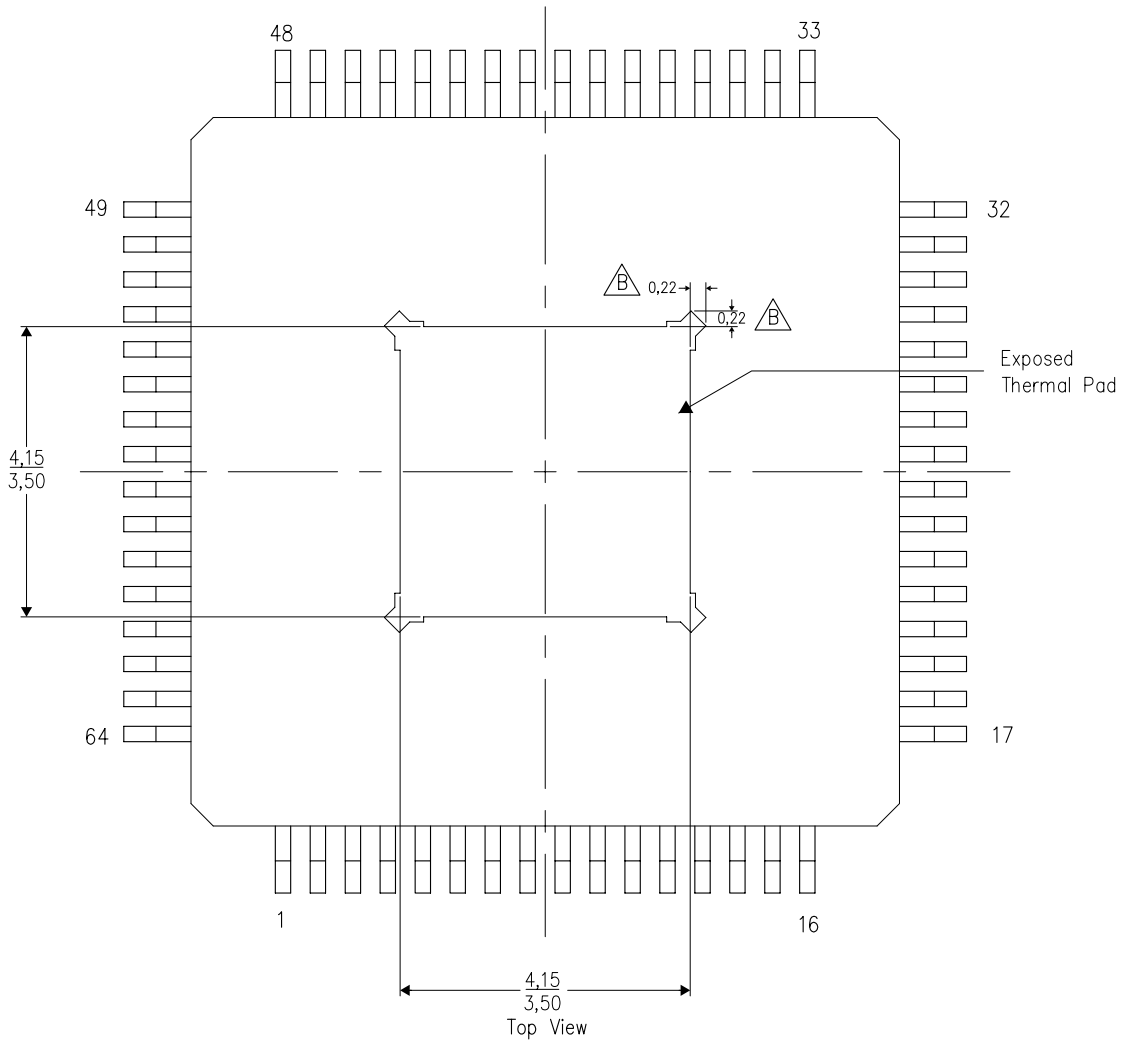
PJD (S-PQFP-G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

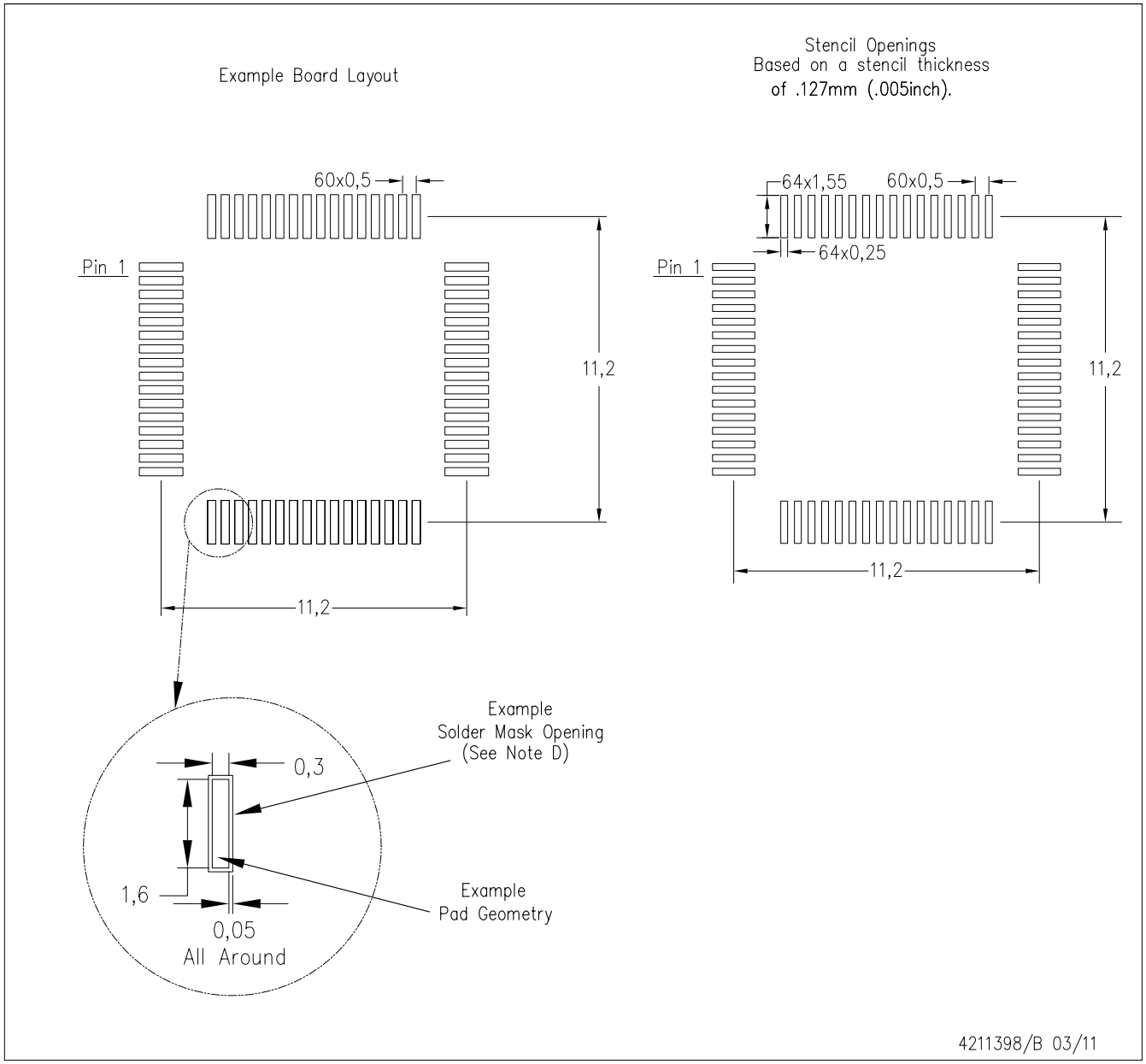


Exposed Thermal Pad Dimensions 4206330-2/B 10/10

NOTE: A. All linear dimensions are in millimeters
B. Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PJD (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated