TCAN1051-Q1, TCAN1051V-Q1, TCAN1051H-Q1, TCAN1051HV-Q1
TCAN1051G-Q1, TCAN1051GV-Q1, TCAN1051HG-Q1, TCAN1051HGV-Q1
ZHCSGC4D – MARCH 2016 – REVISED APRIL 2021

TCAN1051-Q1 具有 CAN FD 和故障保护功能的汽车类 CAN 收发器

1 特性

- AEC Q100 标准：符合汽车应用要求
  - 温度等级 1：-40°C 至 125°C，T_A
  - HBM 分级等级：±16kV
  - CDM 分级等级：±1500V
- 符合 ISO 11898-2:2016 和 ISO 11898-5:2007 物理层标准
- 提供功能安全型
  - 可帮助进行功能安全系统设计的文档
- “Turbo”CAN：
  - 所有器件均支持经典 CAN 和 2Mbps CAN FD（灵活数据速率），而“G”选项支持 5Mbps
  - 具有较短的对称传播延迟时间和快速循环次数，可增加时序裕量
  - 在有负载 CAN 网络中实现更快的数据速率
- EMC 性能：支持 SAE J2962-2 和 IEC 62228-3（最高 500kbps）无需共模扼流圈
- I/O 电压范围支持 3.3V 和 5V MCU
- 未供电时具有理想无源行为
  - 总线和逻辑引脚处于高阻态（无负载）
  - 在总线和 RXD 输出上实现上电/断电无干扰运行
- 保护特性
  - IEC ESD 保护高达 ±15kV
  - 总线故障保护：±58V（非 H 型号）和 ±70V（H 型号）
  - V_{CC} 和 V_{IO}（仅限 V 型号）电源终端具有欠压保护
  - 驱动器显性超时 (TXD DTO) - 数据速率低至 10kbps
  - 热关断保护 (TSD)
- 接收器共模输入电压：±30V
- 典型循环延迟：110ns
- 结温范围为 –55°C 至 150°C
- 采用 SOIC (8) 封装和无引线 VSON (8) 封装 (3.0mm x 3.0mm)，具有改进的自动光学检查 (AOI) 功能

2 应用

- 汽车和运输
- 所有器件均支持高负载 CAN 网络
- 重型机械 ISOBUS 应用 – ISO 11783

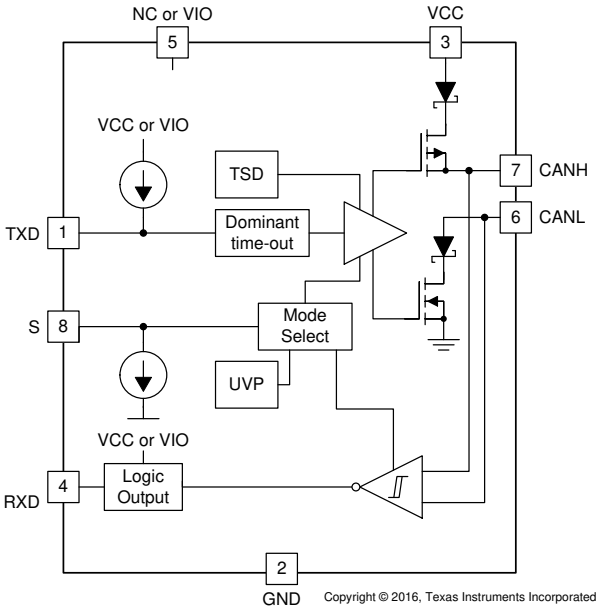
3 说明

这款 CAN 收发器系列符合 ISO1189-2 (2016) 高速 CAN（控制器局域网络）物理层标准。所有器件均设计用于数据速率高达 2Mbps（兆位每秒）的 CAN FD 网络。器件型号包含“G”后缀的器件旨在实现高达 5Mbps 的数据速率，器件型号包含“V”后缀的器件配有提供 I/O 电平的辅助电源输入，用于设置输入引脚阈值和 RXD 输出电平。该系列器件具有静音模式，通常也称作仅侦听模式。此外，所有器件都提供多种保护特性来提高器件和网络的耐用性。

器件信息

器件型号	封装(1)	封装尺寸
TCAN1051x-Q1	SOIC (8)	4.90mm × 3.91mm
	VSON (8)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



A. 引脚 5 的功能取决于器件；在不含 V 后缀的器件上为无连接 (NC) 引脚，在包含 V 后缀的器件上为用于 I/O 电平转换的 V_{IO} 引脚

B. RXD 逻辑输出在不含“V”后缀的器件上驱动为 V_{CC}，而在包含“V”后缀的器件上驱动为 V_{IO}。

功能方框图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

Changes from Revision C (May 2017) to Revision D (April 2021) **Page**

- 添加了*特性*：EMC 性能： ... 1
- 更新了整个文档中的表格、图和交叉参考的编号格式 ... 1
- 添加了*特性* “提供功能安全型” ... 1
- Deleted "Base" from the D and DRB pin images in the *Pin Configurations and Functions* ... 5
- Deleted "Product Preview" from the DRB pin images in the *Pin Configurations and Functions* ... 5
- Added footnote to the GND pin in the *Pin Functions* table ... 5
- Changed I_{CC} Normal Mode Max value From: 180 To 110 in the *Electrical Characteristics* table ... 9
- Added SR, Differential output slew rate to the *Switching Characteristics* table ... 12

Changes from Revision B (May 2016) to Revision C (May 2017) **Page**

- 向汽车应用*特性* 添加了条目 ... 1
- 删除了特性“符合 2015 年 12 月 17 日发布的 ISO 11898-2 物理层更新草案” ... 1
- 将*特性* 从“符合发布的 ISO 11898-2:2007 和 ISO 11898-2:2003 物理层标准”更改为“符合 ISO 11898-2:2016 和 ISO 11898-5:2007 物理层标准” ... 1
- 将“特性”从“所有器件均支持 2Mbps CAN FD..”更改为“所有器件均支持经典 CAN 和 2Mbps CAN FD..” ... 1
- 添加了*特性* “可采用 SOIC(8) 封装和无引线 VSON(8) 封装...” ... 1
- 将*应用* 从“重型机械 ISO11783”更改为“重型机械 ISOBUS 应用 – ISO 11783” ... 1
- 更改了*功能方框图*，删除了显性超时功能框 ... 1
- Changed "D Package for (HV) and (HGV)" To: "DRB Package for (HV) and (HGV)" ... 5
- Added Storage temperature range to the *Absolute Maximum Ratings* table ... 6
- Changed the *ESD Ratings* table to show the D(SOIC) and DRB (VSON) values ... 6
- Changed Human Body Model (HBM) From: ±10000 To: ±16000 in the *ESD Ratings* table ... 6
- Changed Charged Device Model (CDM) From: ±750 To: ±1500 in the *ESD Ratings* table ... 6
- Changed TBD to values for the DRB (VSON) Package in the *ESD Ratings* table ... 6
- Added the *Power Rating* table ... 8
- Changed V_{SYM} in the *DRIVER ELECTRICAL CHARACTERISTICS* table ... 9
- Changed V_{SYM_DC} in the *DRIVER ELECTRICAL CHARACTERISTICS* table ... 9

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- Deleted "V_I = 0.4 sin (4E6 π t) + 2.5 V" from the Test Condition of C_I in the *RECEIVER ELECTRICAL CHARACTERISTICS* table....9
- Deleted "V_I = 0.4 sin (4E6 π t)" from the Test Condition of C_{ID} in the *RECEIVER ELECTRICAL CHARACTERISTICS* table....9
- Added "-30 V ≤ V_{CM} ≤ +30" to the Test Condition of R_{ID} and R_{IN} in the *RECEIVER ELECTRICAL CHARACTERISTICS* table table....9
- Changed the *Functional Block Diagram*, removed the Dominant time-out box....18
- Changed 表 8-2, BUS OUTPUT colum....20

Changes from Revision A (April 2016) to Revision B (May 2016) **Page**

- 添加了*特性* “符合发布的 ISO 11898-2:2007 和 ISO 11898-2:2003 物理层标准” 1
- 将*特性* 从“符合 ISO11898-2 (2016) 标准的要求”更改为“符合 2015 年 12 月 17 日发布的 ISO 11898-2 物理层更新草案” 1
- 更改了*应用* 列表....1
- 向*器件信息* 表中添加了 VSON (8) 引脚封装....1
- Added the VSON (8) pin package to the *Pin Configuration and Functions* 5
- Added $V_{(Diff)}$ to the *节 6.1* table 6
- Added the DRB package to the *Thermal Information* table 8

Changes from Revision * (March 2016) to Revision A (April 2016) **Page**

- 将器件状态从“产品预发布”更改为“量产” 1
- Added the VSON (8) pin package to the *Pin Configuration and Functions* 5

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Device Comparison Table

DEVICE NUMBER	BUS FAULT PROTECTION	5-Mbps FLEXIBLE DATA RATE	3-V LEVEL SHIFTER INTEGRATED	PIN 8 MODE SELECTION
TCAN1051-Q1 (Base)	±58 V			Silent Mode
TCAN1051G-Q1	±58 V	X		
TCAN1051GV-Q1	±58 V	X	X	
TCAN1051V-Q1	±58 V		X	
TCAN1051H-Q1	±70 V			
TCAN1051HG-Q1	±70 V	X		
TCAN1051HGV-Q1	±70 V	X	X	
TCAN1051HV-Q1	±70 V		X	

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5 Pin Configuration and Functions

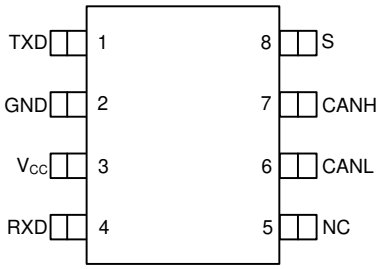


图 5-1. D Package for (H), (G) and (HG) Devices 8 PIN (SOIC) Top View

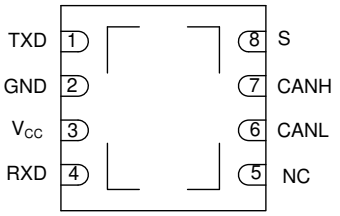


图 5-2. DRB Package for (H), (G), and (HG) Devices 8 PIN (VSON) Top View

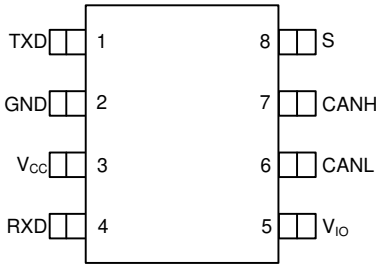


图 5-3. D Package for (V), (GV), (HV), and (HGV) Devices 8 PIN (SOIC) Top View

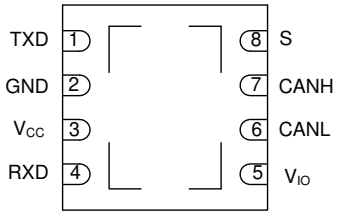


图 5-4. DRB Package for (V), (GV), (HV) and (HGV) Devices 8 PIN (VSON) Top View

表 5-1. Pin Functions

PINS			TYPE	DESCRIPTION
NAME	(H), (G), (HG)	(V), (GV), (HV), (HGV)		
TXD	1	1	DIGITAL INPUT	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
GND(1)	2	2	GND	Ground connection
VCC	3	3	POWER	Transceiver 5-V supply voltage
RXD	4	4	DIGITAL OUTPUT	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
NC	5	—	—	No Connect
V_{IO}	—	5	POWER	Transceiver I/O level shifting supply voltage (Devices with "V" suffix only)
CANL	6	6	BUS I/O	Low level CAN bus input/output line
CANH	7	7	BUS I/O	High level CAN bus Input/output line
S	8	8	DIGITAL INPUT	Silent Mode control input (active high)

(1) For DRB (VSON) package options, the thermal pad may be connected to GND in order to optimize the thermal characteristics of the package.

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6 Specifications

over operating free-air temperature range (unless otherwise noted) (1) (2)

6.1 Absolute Maximum Ratings

			MIN	MAX	UNIT
V_{CC}	5-V Bus Supply Voltage Range	All Devices	–0.3	7	V
V_{IO}	I/O Level-Shifting Voltage Range	Devices with the "V" Suffix	–0.3	7	V
V_{BUS}	CAN Bus I/O voltage range (CANH, CANL)	Devices without the "H" Suffix	–58	58	V
$V_{(Diff)}$	Max differential voltage between CANH and CANL	Devices without the “H” suffix	–58	58	V
V_{BUS}	CAN Bus I/O voltage range (CANH, CANL)	Devices with the "H" Suffix	-70	70	V
$V_{(Diff)}$	Max differential voltage between CANH and CANL	Devices with the “H” suffix	–70	70	V
$V_{(Logic_Input)}$	Logic input terminal voltage range (TXD, S)	All Devices	–0.3	+7 and $V_I \leqslant V_{IO}$ + 0.3	V
$V_{(Logic_Output)}$	Logic output terminal voltage range (RXD)		–0.3	+7 and $V_I \leqslant V_{IO}$ + 0.3	V
$I_{O(RXD)}$	RXD (Receiver) output current		–8	8	mA
T_J	Virtual junction temperature range (see 节 6.5)		–55	150	°C
T_{STG}	Storage temperature range (see 节 6.5)		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated condition for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

	TEST CONDITIONS	VALUE	UNIT
D (SOIC) Package			
Human Body Model (HBM) ESD stress voltage	All terminals(1)	±6000	V
	CAN bus terminals (CANH, CANL) to GND(2)	±16000	
Charged Device Model (CDM) ESD stress voltage	All terminals(3)	±1500	V
Machine Model	All terminals(4)	±200	V
DRB (VSON) Package			
Human Body Model (HBM) ESD stress voltage	All terminals(1)	±6000	V
	CAN bus terminals (CANH, CANL) to GND(2)	±16000	
Charged Device Model (CDM) ESD stress voltage	All terminals(3)	±1500	V
Machine Model	All terminals(4)	±200	V

(1) Tested in accordance to JEDEC Standard 22, Test Method A114.
(2) Test method based upon JEDEC Standard 22 Test Method A114, CAN bus is stressed with respect to GND.
(3) Tested in accordance to JEDEC Standard 22, Test Method C101.
(4) Tested in accordance to JEDEC Standard 22, Test Method A115.

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6.3 ESD Ratings, Specifications

	TEST CONDITIONS		VALUE	UNIT
D (SOIC) Package				
System Level Electro-Static Discharge (ESD)	CAN bus terminals (CANH, CANL) to GND	SAE J2962-2 per ISO 10605: Powered Air Discharge	±15000	V
		SAE J2962-2 per ISO 10605: Powered Contact Discharge	±8000	
System Level Electro-Static Discharge (ESD)	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4-2: Unpowered Contact Discharge	±15000	V
		IEC 61000-4-2: Powered Contact Discharge	±8000	
System Level Electrical fast transient (EFT)	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4-4: Criteria A	±4000	V
ISO7637 Transients according to GIFT - ICT CAN EMC test spec(1)	CAN bus terminals (CANH, CANL) to GND	Pulse 1	−100	V
		Pulse 2	+75	
		Pulse 3a	−150	
		Pulse 3b	+100	
ISO7637-3 Transients	CAN bus terminals (CANH, CANL) to GND	Direct Coupling Capacitor "Slow Transient Pulse" with100 nF coupling capacitor - Powered	±85	V
DRB (VSON) Package				
System Level Electro-Static Discharge (ESD)	CAN bus terminals (CANH, CANL) to GND	SAE J2962-2 per ISO 10605: Powered Air Discharge	±15000	V
		SAE J2962-2 per ISO 10605: Powered Contact Discharge	±8000	
System Level Electro-Static Discharge (ESD)	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4-2: Unpowered Contact Discharge	±14000	V
		IEC 61000-4-2: Powered Contact Discharge	±8000	
System Level Electrical fast transient (EFT)	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4 Criteria A	±4000	V
ISO7637 Transients according to GIFT - ICT CAN EMC test spec(1)	CAN bus terminals (CANH, CANL) to GND	Pulse 1	−100	V
		Pulse 2	+75	
		Pulse 3a	−150	
		Pulse 3b	+100	
ISO7637-3 Transients	CAN bus terminals (CANH, CANL) to GND	Direct Coupling Capacitor "Slow Transient Pulse" with100 nF coupling capacitor - Powered	±85	V

(1) ISO7637 is a system level transient test. Results given here are specific to the GIFT-ICT CAN EMC Test specification conditions. Different system level configurations may lead to different results.

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6.4 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	5-V Bus Supply Voltage Range	4.5	5.5	V
V_{IO}	I/O Level-Shifting Voltage Range	2.8	5.5	
$I_{OH(RXD)}$	RXD terminal HIGH level output current	–2		mA
$I_{OL(RXD)}$	RXD terminal LOW level output current		2	

6.5 Thermal Information

Thermal Metric(1)		TEST CONDITIONS	TCAN1051-Q1		
			D (SOIC)	DRB (VSON)	Unit
			8 Pins	8 Pins	
$R_{\theta JA}$	Junction-to-air thermal resistance	High-K thermal resistance	105.8	40.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		46.8	49.7	°C/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance		48.3	15.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		8.7	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		46.2	15.9	°C/W
T_{TSD}	Thermal shutdown temperature		170	170	°C
T_{TSD_HYS}	Thermal shutdown hysteresis		5	5	°C

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Power Rating

PARAMETER		TEST CONDITIONS	POWER DISSIPATION	UNIT
P_D	Average power dissipation	V_{CC} = 5 V, V_{IO} = 5 V (if applicable), T_J = 27°C, R_L = 60 Ω, S at 0 V, Input to TXD at 250 kHz, C_{L_RXD} = 15 pF. Typical CAN operating conditions at 500 kbps with 25% transmission (dominant) rate.	52	mW
		V_{CC} = 5.5 V, V_{IO} = 5.5 V (if applicable), T_J = 150°C, R_L = 50 Ω, S at 0 V, Input to TXD at 500 kHz, C_{L_RXD} = 15 pF. Typical high load CAN operating conditions at 1 Mbps with 50% transmission (dominant) rate and loaded network.	124	mW

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6.7 Electrical Characteristics

Over recommended operating conditions, T_A = –55°C to 125°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Supply Characteristics							
I_{CC}	5-V Supply current	Normal mode (dominant)	See 图 7-1, TXD = 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open, S = 0V		40	70	mA
			See 图 7-1, TXD = 0 V, R_L = 50 Ω, C_L = open, R_{CM} = open, S = 0V		45	80	
		Normal mode (dominant – bus fault)	See 图 7-1, TXD = 0 V, S = 0V, CANH = -12V, R_L = open, C_L = open, R_{CM} = open			110	
		Normal mode (recessive)	See 图 7-1, TXD = V_{CC}, R_L = 50 Ω, C_L = open, R_{CM} = open, S = 0V		1.5	2.5	
		Silent mode	See 图 7-1, TXD = V_{CC}, R_L = 50 Ω,C_L = open, R_{CM} = open, S = V_{CC}		1.5	2.5	
I_{IO}	I/O supply current	Normal and Silent modes	RXD Floating, TXD = S = 0 or 5.5 V		90	300	µA
UV_{VCC}	Rising undervoltage detection on V_{CC} for protected mode		All devices		4.2	4.4	V
	Falling undervoltage detection on V_{CC} for protected mode			3.8	4.0	4.25	
$V_{HYS(UVVCC)}$	Hysteresis voltage on UV_{VCC}				200		mV
UV_{VIO}	Undervoltage detection on V_{IO} for protected mode		Devices with the "V" Suffix (I/O level-shifting)	1.3		2.75	V
$V_{HYS(UVVIO)}$	Hysteresis voltage on UV_{VIO} for protected mode				80		mV
S Terminal (Mode Select Input)							
V_{IH}	High-level input voltage		Devices with the "V" suffix (I/O level-shifting)	0.7 x V_{IO}			V
			Devices without the "V" suffix (5-V only)	2			
V_{IL}	Low-level input voltage		Devices with the "V" suffix (I/O level-shifting)			0.3 x V_{IO}	
			Devices without the "V" suffix (5-V only)			0.8	
I_{IH}	High-level input leakage current		S = V_{CC} or V_{IO} = 5.5 V			30	µA
I_{IL}	Low-level input leakage current		S = 0 V, V_{CC} = V_{IO} = 5.5 V	–2	0	2	
$I_{lkg(OFF)}$	Unpowered leakage current		S = 5.5 V, V_{CC} = V_{IO} = 0 V	-1		1	
TXD Terminal (CAN Transmit Data Input)							
V_{IH}	High-level input voltage		Devices with the "V" suffix (I/O level-shifting)	0.7 x V_{IO}			V
			Devices without the "V" suffix (5-V only)	2			
V_{IL}	Low-level input voltage		Devices with the "V" suffix (I/O level-shifting)			0.3 x V_{IO}	
			Devices without the "V" suffix (5-V only)			0.8	
I_{IH}	High-level input leakage current		TXD = V_{CC} = V_{IO} = 5.5 V	–2.5	0	1	µA
I_{IL}	Low-level input leakage current		TXD = 0 V, V_{CC} = V_{IO} = 5.5 V	–100	-25	–7	
$I_{lkg(OFF)}$	Unpowered leakage current		TXD = 5.5 V, V_{CC} = V_{IO} = 0 V	–1	0	1	
C_I	Input capacitance		V_{IN} = 0.4 * sin(4E6 * π * t) + 2.5 V		5		pF

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6.7 Electrical Characteristics (continued)

Over recommended operating conditions, T_A = –55°C to 125°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
RXD Terminal (CAN Receive Data Output)							
V_{OH}	High-level output voltage		Devices with the "V" suffix (I/O level-shifting), See 图 7-2, I_O = –2 mA	0.8 × V_{IO}			V
			Devices without the "V" suffix (5-V only), See 图 7-2, I_O = –2 mA	4	4.6		
V_{OL}	Low-level output voltage		Devices with the "V" suffix (I/O level-shifting), See 图 7-2, I_O = +2 mA			0.2 x V_{IO}	
			Devices without the "V" suffix (5-V only), See 图 7-2, I_O = +2 mA		0.2	0.4	
$I_{lkg(OFF)}$	Unpowered leakage current		RXD = 5.5 V, V_{CC} = 0 V, V_{IO} = 0 V	–1	0	1	µA
Driver Electrical Characteristics							
$V_{O(DOM)}$	Bus output voltage (dominant	CANH	See 图 8-2 and 图 7-1, TXD = 0 V, S = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	2.75		4.5	V
		CANL		0.5		2.25	
$V_{O(REC)}$	Bus output voltage (recessive)	CANH and CANL	See 图 8-2 and 图 7-1, TXD = V_{CC}, V_{IO} = V_{CC}, S = V_{CC} or 0 V (2), R_L = open (no load), R_{CM} = open	2	0.5 × V_{CC}	3	
$V_{OD(DOM)}$	Differential output voltage (dominant)	CANH - CANL	See 图 8-2 and 图 7-1, TXD = 0 V, S = 0 V, 45 Ω ≤ R_L < 50 Ω, C_L = open, R_{CM} = open	1.4		3	
			See 图 8-2 and 图 7-1, TXD = 0 V, S = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	1.5		3	
			See 图 8-2 and 图 7-1, TXD = 0 V, S = 0 V, R_L = 2240 Ω, C_L = open, R_{CM} = open	1.5		5	
$V_{OD(REC)}$	Differential output voltage (recessive)	CANH - CANL	See 图 8-2 and 图 7-1, TXD = V_{CC}, S = 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open	–120		12	mV
			See 图 8-2 and 图 7-1, TXD = V_{CC}, S = 0 V, R_L = open (no load), C_L = open, R_{CM} = open	–50		50	
V_{SYM}	Transient symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$) / V_{CC}		See 图 7-1 and 图 9-2, S at 0 V, R_{term} = 60 Ω, C_{split} = 4.7 nF, C_L = open, R_{CM} = open, T_{XD} = 250 kHz, 1 MHz	0.9		1.1	V/V
V_{SYM_DC}	DC Output symmetry (dominant or recessive) (V_{CC} – $V_{O(CANH)}$ – $V_{O(CANL)}$)		See 图 7-1 and 图 8-2, S = 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open	–0.4		0.4	V
$I_{OS(SS_DOM)}$	Short-circuit steady-state output current, dominant		See 图 8-2 and 图 7-7, 图 7-7, S at 0 V, V_{CANH} = -5 V to 40 V, CANH = open, TXD = 0 V	–100			mA
			See 图 8-2 and 图 7-7, S at 0 V, V_{CANL} = -5 V to 40 V, CANH = open, TXD = 0 V			100	
$I_{OS(SS_REC)}$	Short-circuit steady-state output current, recessive		See 图 8-2 and 图 7-7, –27 V ≤ V_{BUS} ≤ 32 V, Where V_{BUS} = CANH = CANL, TXD = V_{CC}, all modes	–5		5	mA

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6.7 Electrical Characteristics (continued)

Over recommended operating conditions, T_A = –55°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Receiver Electrical Characteristics						
V_{CM}	Common mode range, normal mode	See 图 7-2, 表 8-5 and 表 7-1, S = 0 or V_{CC} or V_{IO}	-30		+30	V
V_{IT+}	Positive-going input threshold voltage, all modes	See 图 7-2, 表 8-5 and 表 7-1, S = 0 or V_{CC} or V_{IO}, -20 V ≤ V_{CM} ≤ +20 V			900	mV
V_{IT-}	Negative-going input threshold voltage, all modes		500			
V_{IT+}	Positive-going input threshold voltage, all modes	See 图 7-2, 表 8-5 and 表 7-1, S = 0 or V_{CC} or V_{IO}, -30 V ≤ V_{CM} ≤ +30 V			1000	
V_{IT-}	Negative-going input threshold voltage, all modes		400			
V_{HYS}	Hysteresis voltage (V_{IT+} - V_{IT-})	See 图 7-2, 表 8-5 and 表 7-1, S = 0 or V_{CC} or V_{IO}		120		mV
$I_{lkg(IOFF)}$	Power-off (unpowered) bus input leakage current	CANH = CANL = 5 V, V_{CC} = V_{IO} = 0 V			4.8	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{CC}, V_{IO} = V_{CC}		24	30	pF
C_{ID}	Differential input capacitance	TXD = V_{CC}, V_{IO} = V_{CC}		12	15	pF
R_{ID}	Differential input resistance	TXD = V_{CC} = V_{IO} = 5 V, S = 0 V, -30 V ≤ V_{CM} ≤ +30 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)		15		40	kΩ
$R_{IN(M)}$	Input resistance matching: [1 – $R_{IN(CANH)}$ / $R_{IN(CANL)}$] × 100%	V_{CANH} = V_{CANL} = 5 V	–2%		+2%	

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and V_{IO} = 5 V, R_L = 60 Ω.
(2) For the bus output voltage (recessive) will be the same if the device is in Normal mode with S terminal LOW or if the device is in Silent mode with the S terminal is HIGH.

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6.8 Switching Characteristics

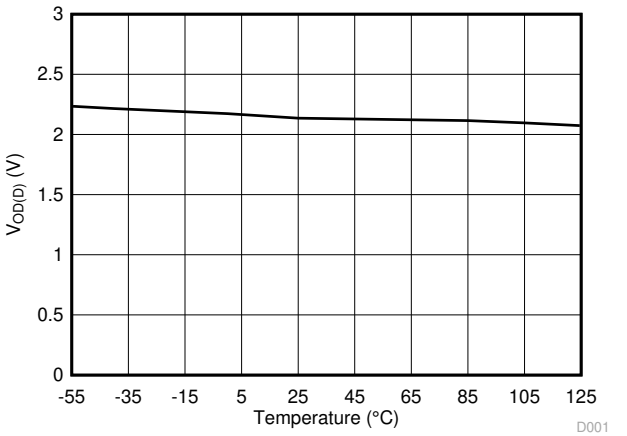
Over recommended operating conditions with T_A = -55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	See 图 7-4, S = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		100	160	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive			110	175	
t_{MODE}	Mode change time, from Normal to Silent or from Silent to Normal	See 图 7-3		1	10	µs
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	See 图 7-1, S = 0 V, R_L = 60 Ω, C_L = 100 pF, R_{CM} = open		75		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			55		
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHR} - t_{pLD} \rvert$)			20		
t_R	Differential output signal rise time			45		
t_F	Differential output signal fall time			45		
SR	Differential output slew rate, dominant-to-recessive transition				70	V/µs
t_{TXD_DTO}	Dominant timeout	See 图 7-6, S = 0 V, R_L = 60 Ω, C_L = open	1.2		3.8	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high output (Dominant to Recessive)	See 图 7-2, S = 0 V, $C_{L(RXD)}$ = 15 pF		65		ns
t_{pDL}	Propagation delay time, bus dominant input to low output (Recessive to Dominant)			50		ns
t_R	RXD Output signal rise time			10		ns
t_F	RXD Output signal fall time			10		ns
FD Timing Parameters						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns, all devices	See 图 7-5 , S = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	435		530	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns, G device variants only		155		210	
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns, all devices		400		550	
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns, G device variants only		120		220	
Δt_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns, all devices		-65		40	
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns, G device variants only		-45		15	

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and V_{IO} = 5 V (if applicable), R_L = 60 Ω

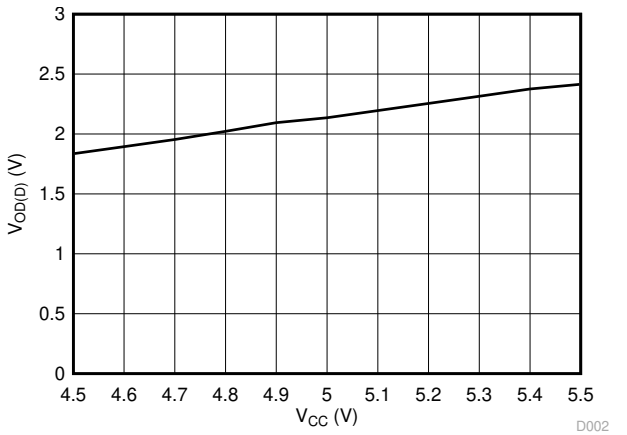
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6.9 Typical Characteristics



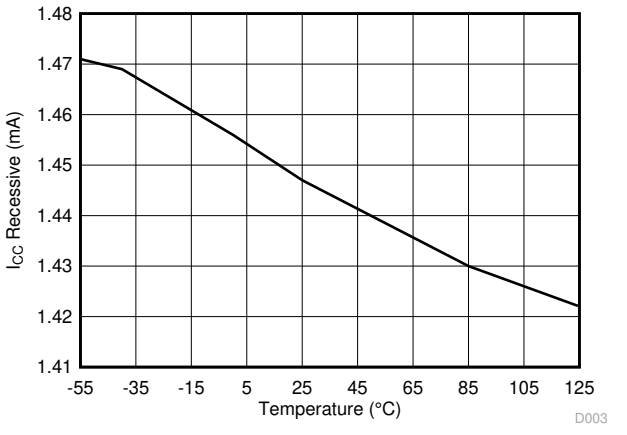
V_{CC} = 5 V　V_{IO} = 3.3 V　R_L = 60 Ω
C_L = Open　RCM = Open　S = 0 V

图 6-1. $V_{OD(D)}$ over Temperature



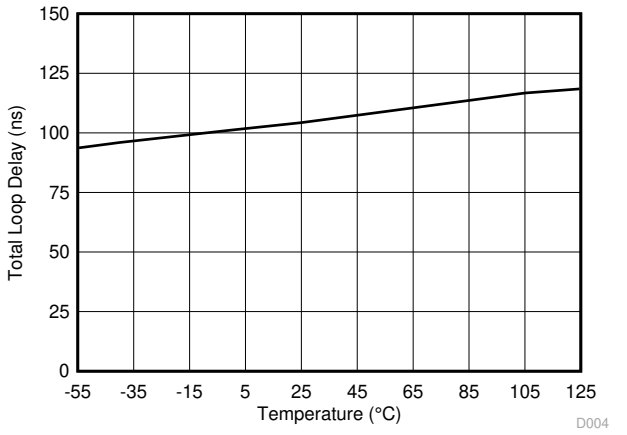
V_{IO} = 5 V　S = 0 V　R_L = 60 Ω
C_L = Open　RCM = Open　Temp = 25°C

图 6-2. $V_{OD(D)}$ over V_{CC}



V_{CC} = 5 V　V_{IO} = 3.3 V　R_L = 60 Ω
C_L = Open　RCM = Open　S = 0 V

图 6-3. I_{CC} Recessive over Temperature

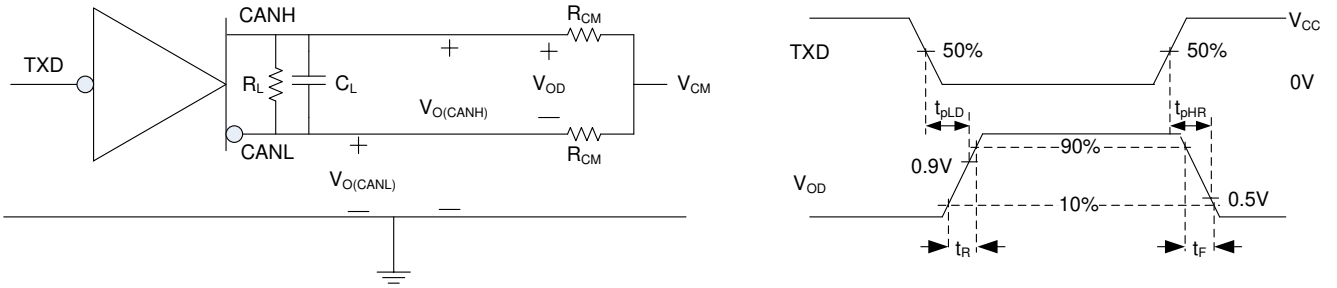


V_{CC} = 5 V　V_{IO} = 3.3 V　R_L = 60 Ω
C_L = 100 pF　C_{L_RXD} = 15 pF　S = 0 V

图 6-4. Total Loop Delay over Temperature

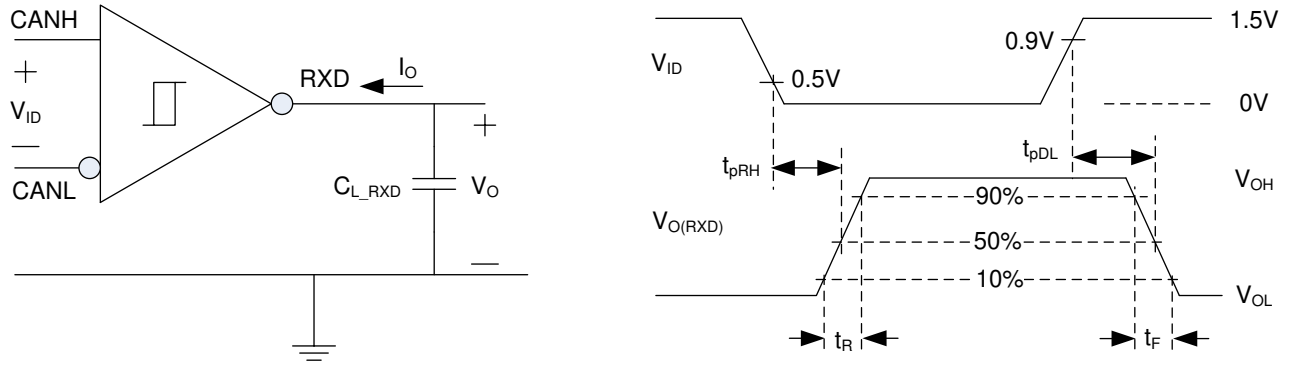
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7 Parameter Measurement Information



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图 7-1. Driver Test Circuit and Measurement



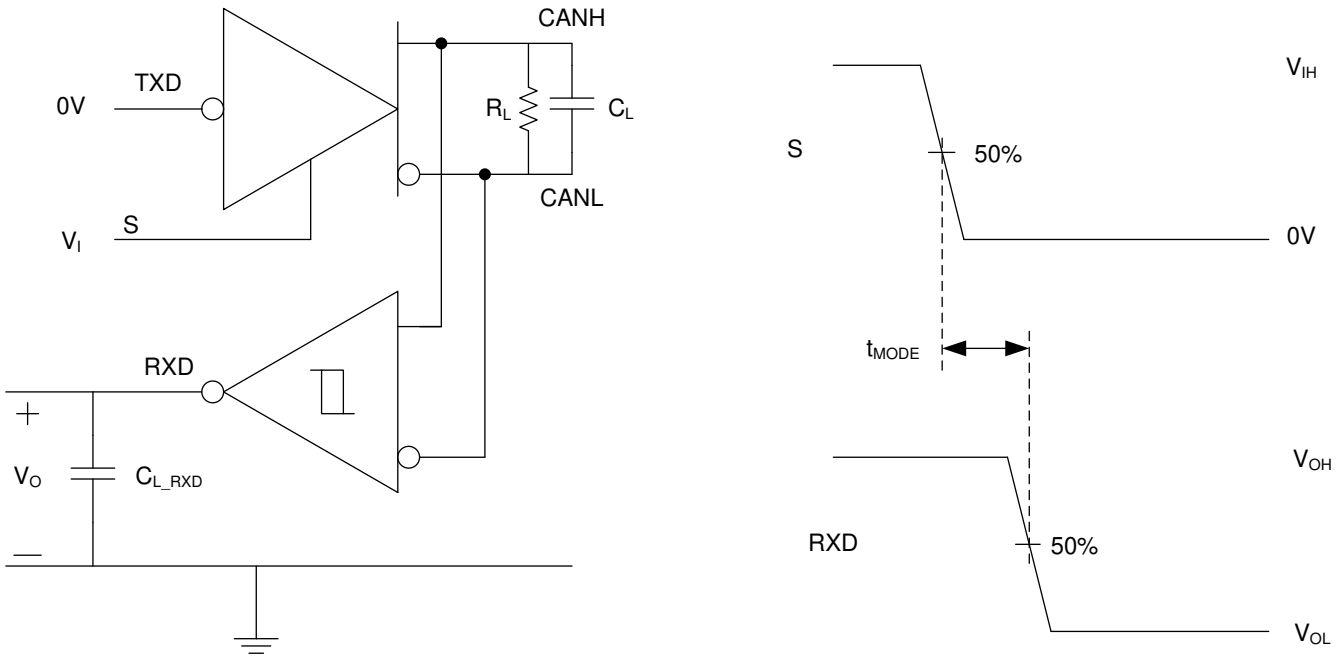
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图 7-2. Receiver Test Circuit and Measurement

表 7-1. Receiver Differential Input Voltage Threshold Test

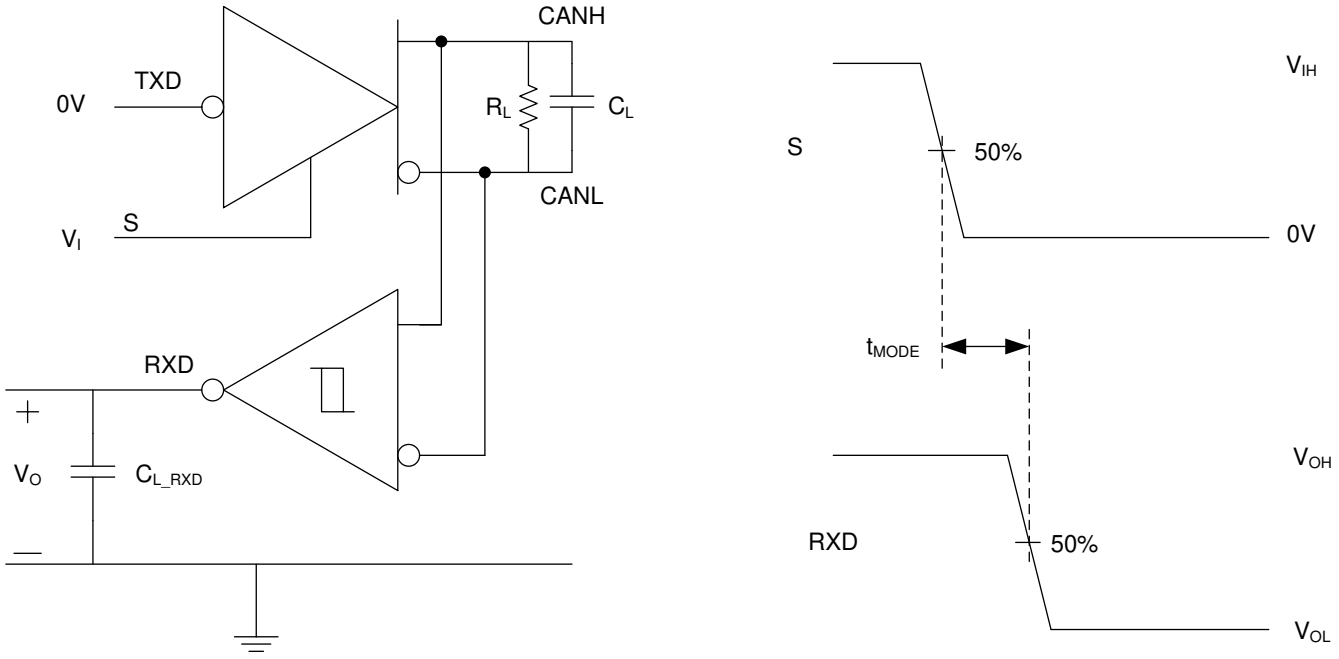
INPUT (See Receiver Test Circuit and Measurement			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	RXD	
-29.5 V	-30.5 V	1000 mV	L	V_{OL}
30.5 V	29.5 V	1000 mV	L	
-19.55 V	-20.45 V	900 mV	L	
20.45 V	19.55 V	900 mV	L	
-19.75 V	-20.25 V	500 mV	H	V_{OH}
20.25 V	19.75 V	500 mV	H	
-29.8 V	-30.2 V	400 mV	H	
30.2 V	29.8 V	400 mV	H	
Open	Open	X	H	

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图 7-3. t_{MODE} Test Circuit and Measurement



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图 7-4. $T_{PROP(LOOP)}$ Test Circuit and Measurement

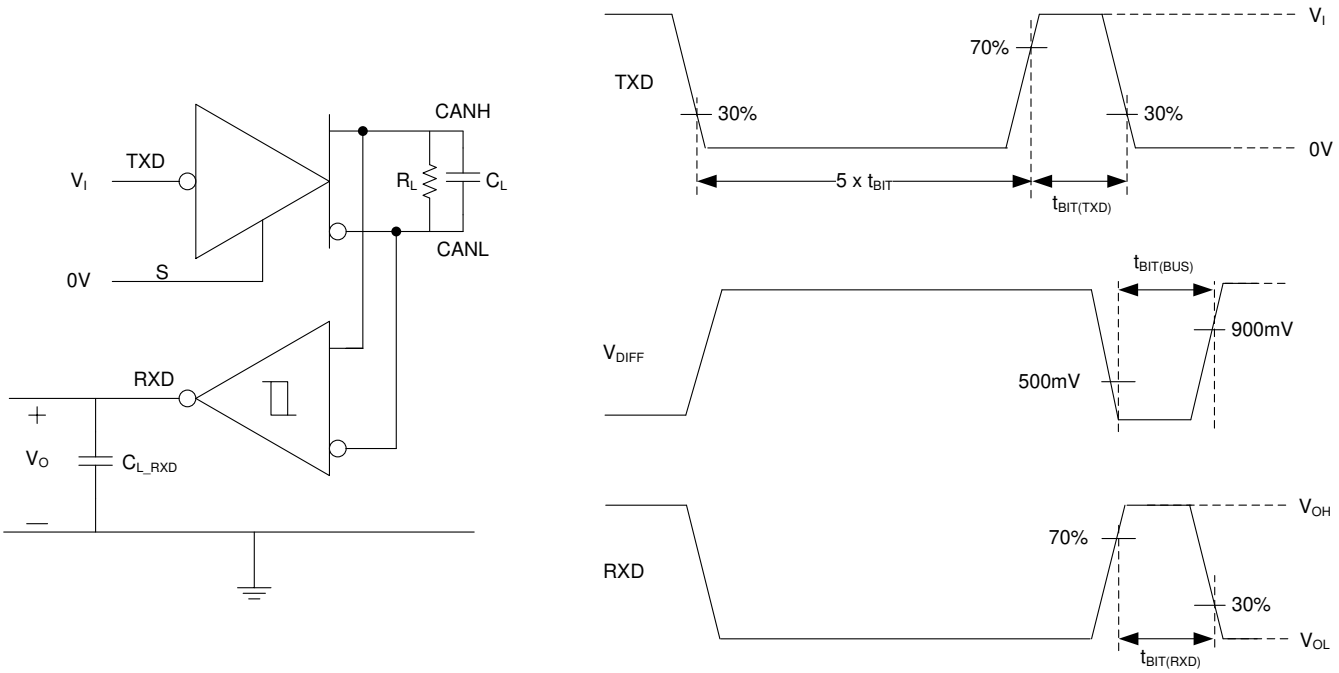
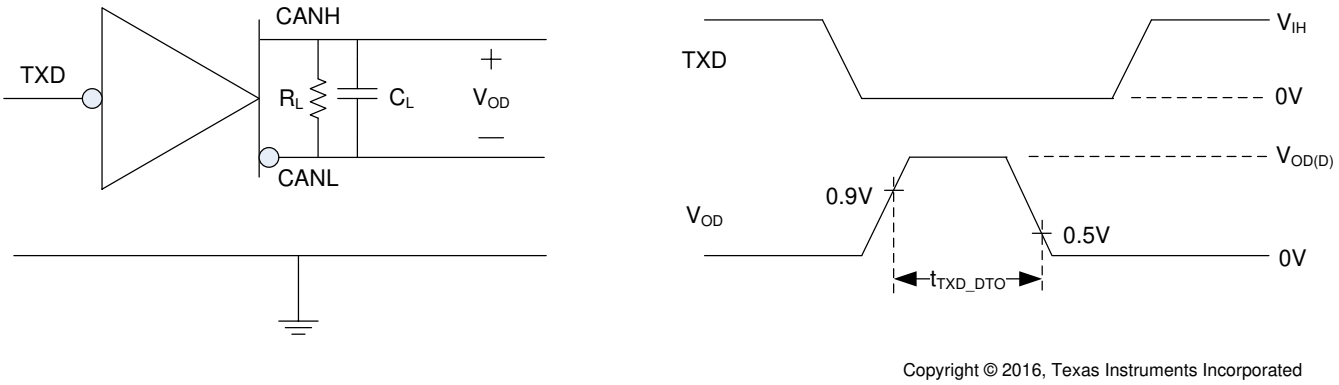


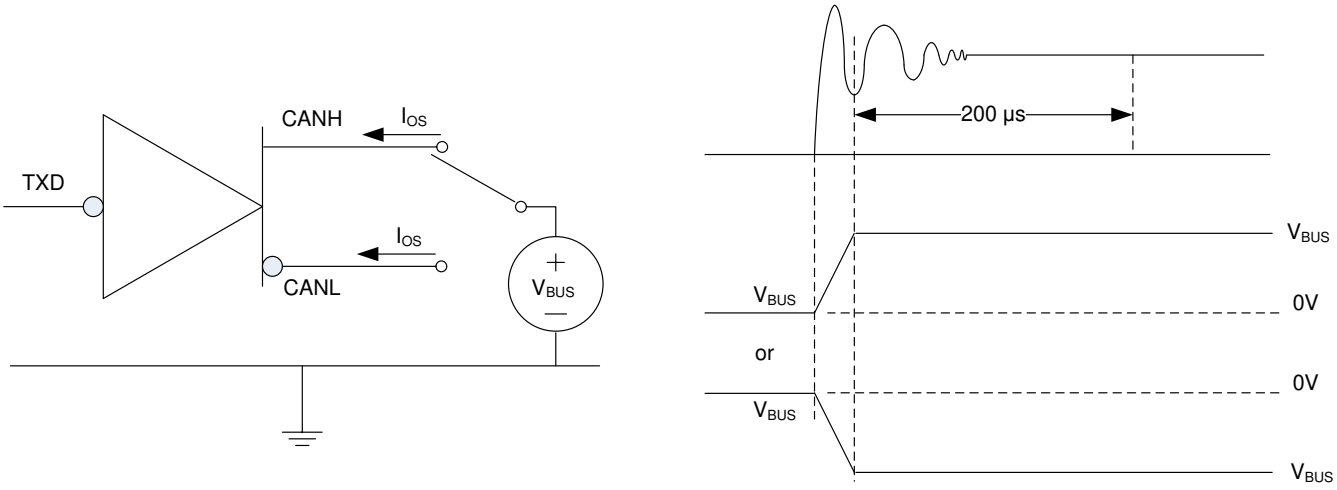
图 7-5. CAN FD Timing Parameter Measurement



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图 7-6. TXD Dominant Timeout Test Circuit and Measurement

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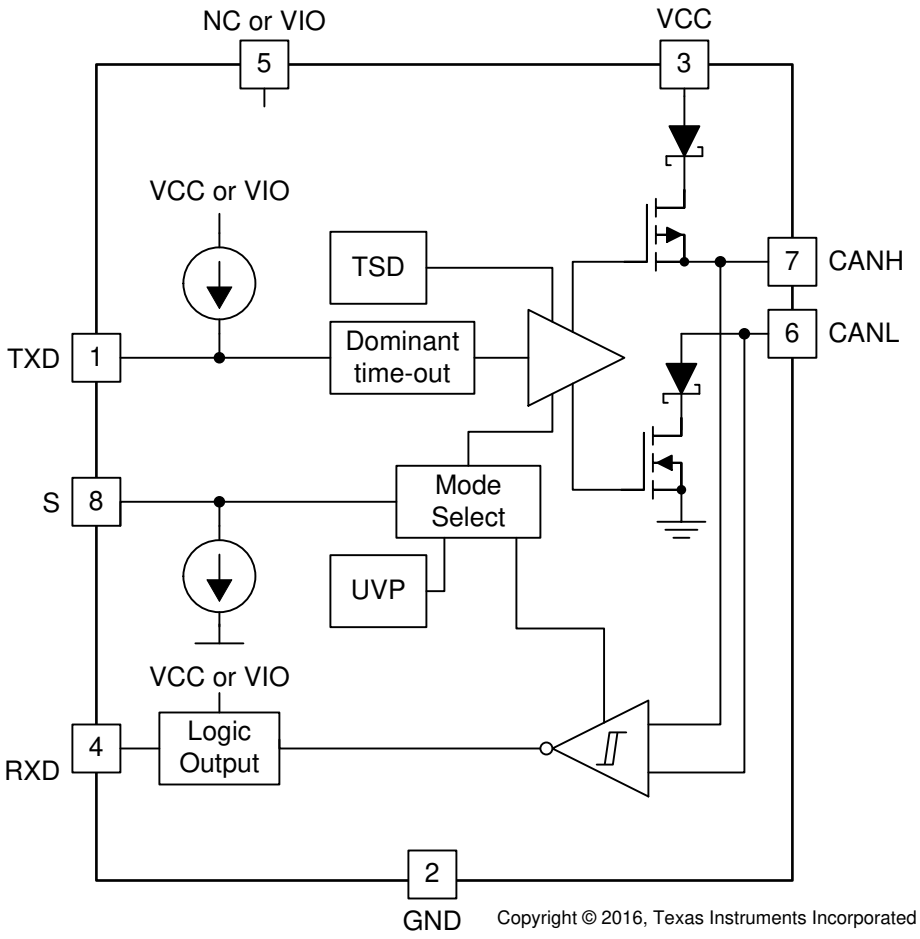
图 7-7. Driver Short Circuit Current Test and Measurement

8 Detailed Description

8.1 Overview

These CAN transceivers meet the ISO11898-2 (2016) High Speed CAN (Controller Area Network) physical layer standard. They are designed for data rates in excess of 1 Mbps for CAN FD and enhanced timing margin / higher data rates in long and highly-loaded networks. These devices provide many protection features to enhance device and CAN robustness.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 TXD Dominant Timeout (DTO)

During normal mode (the only mode where the CAN driver is active), the TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The DTO circuit timer starts on a falling edge on TXD. The DTO circuit disables the CAN bus driver if no rising edge is seen before the timeout period expires. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on the TXD terminal, thus clearing the TXD DTO condition. The receiver and RXD terminal still reflect activity on the CAN bus, and the bus terminals are biased to the recessive level during a TXD dominant timeout.

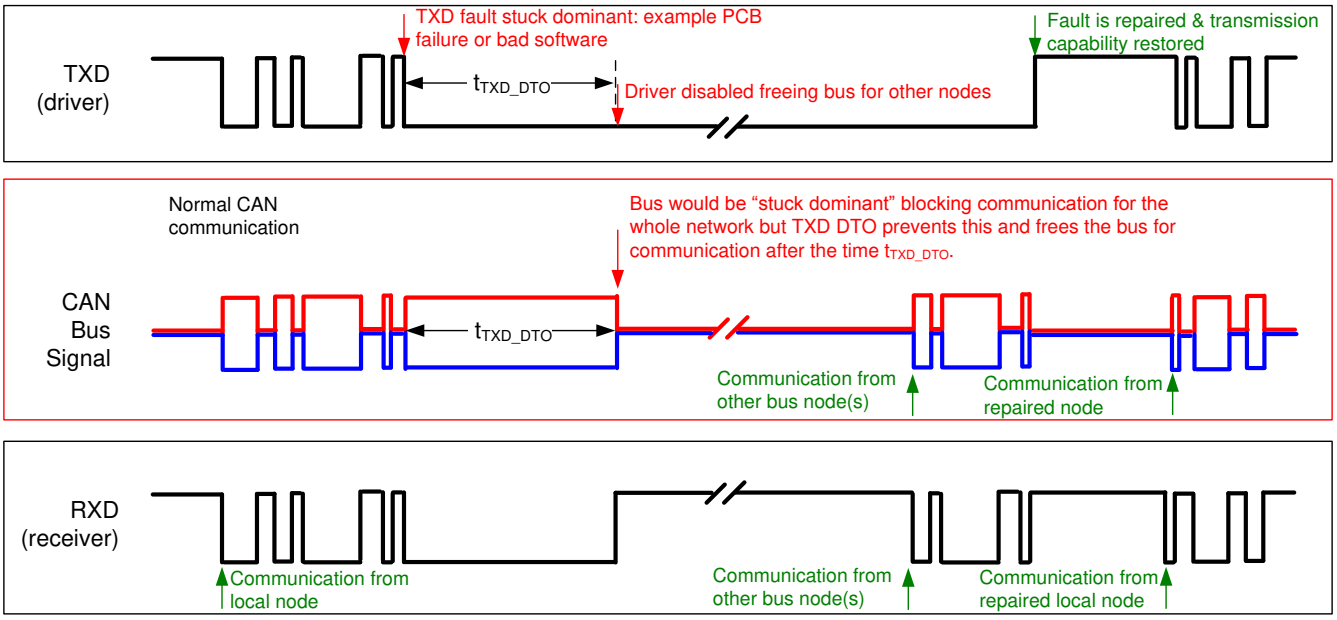


图 8-1. Example Timing Diagram for TXD DTO

Note

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate by: Minimum Data Rate = 11 / t_{TXD_DTO}.

8.3.2 Thermal Shutdown (TSD)

If the junction temperature of the device exceeds the thermal shutdown threshold (T_{TSD}), the device turns off the CAN driver circuits thus blocking the TXD-to-bus transmission path. The CAN bus terminals are biased to the recessive level during a thermal shutdown, and the receiver-to-RXD path remains operational. The shutdown condition is cleared when the junction temperature drops at least the thermal shutdown hysteresis temperature (T_{TSD_HYS}) below the thermal shutdown temperature (T_{TSD}) of the device.

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8.3.3 Undervoltage Lockout

The supply terminals have undervoltage detection that places the device in protected mode. This protects the bus during an undervoltage event on either the V_{CC} or V_{IO} supply terminals.

表 8-1. Undervoltage Lockout 5 V Only Devices (Devices without the "V" Suffix)

V_{CC}	DEVICE STATE(1)	BUS OUTPUT	RXD
> UV_{VCC}	Normal	Per TXD	Mirrors Bus(2)
< UV_{VCC}	Protected	High Impedance	High Impedance

(1) See the V_{IT} section of the Electrical Characteristics.
(2) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

表 8-2. Undervoltage Lockout I/O Level Shifting Devices (Devices with the "V" Suffix)

V_{CC}	V_{IO}	DEVICE STATE	BUS OUTPUT	RXD
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors Bus(1)
< UV_{VCC}	> UV_{VIO}	Protected	High Impedance	High (Recessive)
> UV_{VCC}	< UV_{VIO}	Protected	High Impedance	High Impedance
< UV_{VCC}	< UV_{VIO}	Protected	High Impedance	High Impedance

(1) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

Note

After an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically resumes normal operation within 50 µs.

8.3.4 Unpowered Device

The device is designed to be 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation. The logic terminals also have extremely low leakage currents when the device is unpowered to avoid loading down other circuits that may remain powered.

8.3.5 Floating Terminals

These devices have internal pull ups on critical terminals to place the device into known states if the terminals float. The TXD terminal is pulled up to V_{CC} or V_{IO} to force a recessive input level if the terminal floats. The S terminal is also pulled down to force the device into Normal mode if the terminal floats.

8.3.6 CAN Bus Short Circuit Current Limiting

The device has two protection features that limit the short circuit current when a CAN bus line is short-circuit fault condition: driver current limiting (both dominant and recessive states) and TXD dominant state time out to prevent permanent higher short circuit current of the dominant state during a system fault. During CAN communication the bus switches between dominant and recessive states, thus the short circuit current may be viewed either as the instantaneous current during each bus state or as an average current of the two states. For system current (power supply) and power considerations in the termination resistors and common-mode choke ratings, use the average short circuit current. Determine the ratio of dominant and recessive bits by the data in the CAN frame plus the following factors of the protocol and PHY that force either recessive or dominant at certain times:

- Control fields with set bits
- Bit stuffing
- Interframe space
- TXD dominant time out (fault case limiting)

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These ensure a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits. The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated with the following formula:

$$I_{OS(AVG)} = \%Transmit \times [(\%REC_Bits \times I_{OS(SS)_REC}) + (\%DOM_Bits \times I_{OS(SS)_DOM})] + [\%Receive \times I_{OS(SS)_REC}] \quad (1)$$

Where:

- $I_{OS(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)_DOM}$ is the dominant steady state short circuit current

Note

Consider the short circuit current and possible fault cases of the network when sizing the power ratings of the termination resistance and other network components.

8.3.7 Digital Inputs and Outputs

8.3.7.1 5-V V_{CC} Only Devices (Devices without the "V" Suffix):

The 5-V V_{CC} only devices are supplied by a single 5-V rail. The digital inputs have TTL input thresholds and are therefore 5 V and 3.3 V compatible. The RXD outputs on these devices are driven to the V_{CC} rail for logic high output. Additionally, the TXD pin is internally pulled up to V_{CC}, and the S pin is pulled low to GND. The internal bias of the mode pins may only place the device into a known state if the terminals float, they may not be adequate for system-level biasing during transients or noisy enviroments.

Note

TXD pull up strength and CAN bit timing require special consideration when these devices are used with CAN controllers with an open-drain TXD output. An adequate external pull up resistor must be used to ensure that the CAN controller output of the micrcontroller maintains adequate bit timing to the TXD input.

8.3.7.2 5 V V_{CC} with V_{IO} I/O Level Shifting (Devices with the "V" Suffix):

These devices use a 5 V V_{CC} power supply for the CAN driver and high speed receiver blocks. These transceivers have a second power supply for I/O level-shifting (V_{IO}). This supply is used to set the CMOS input thresholds of the TXD and S pins and the RXD high level output voltage. Additionally, the TXD pin is internally pulled up to V_{IO}, and the S pin is pulled low to GND.

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8.4 Device Functional Modes

The device has two main operating modes: Normal mode and Silent mode. Operating mode selection is made via the S input terminal.

表 8-3. Operating Modes

S Terminal	MODE	DRIVER	RECEIVER	RXD Terminal
LOW	Normal Mode	Enabled (ON)	Enabled (ON)	Mirrors Bus State(1)
HIGH	Silent Mode	Disabled (OFF)	Enabled (ON)	Mirrors Bus State(1)

(1) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

8.4.1 CAN Bus States

The CAN bus has two states during powered operation of the device: *dominant* and *recessive*. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the TXD and RXD terminal. A recessive bus state is when the bus is biased to V_{CC} / 2 via the high-resistance internal input resistors R_{IN} of the receiver, corresponding to a logic high on the TXD and RXD terminals.

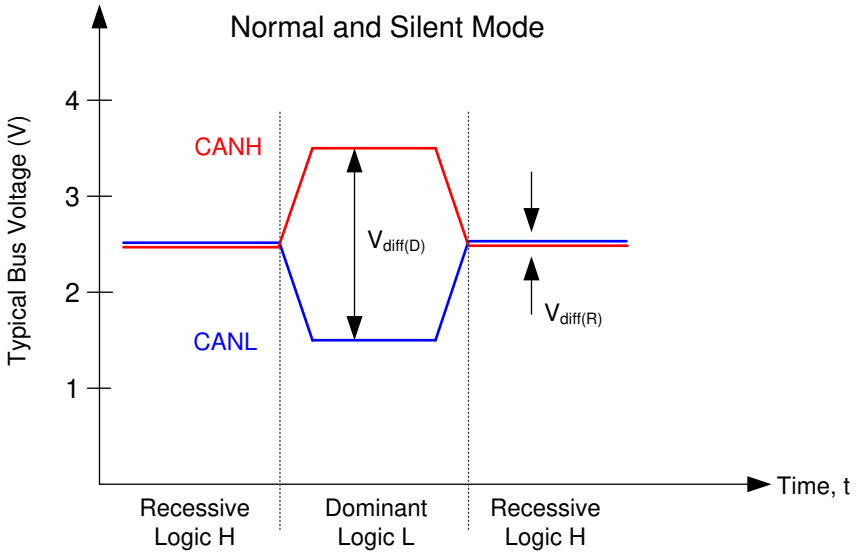


图 8-2. Bus States (Physical Bit Representation)

8.4.2 Normal Mode

Select the *Normal mode* of device operation by setting S terminal low. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver translates a digital input on TXD to a differential output on CANH and CANL. The receiver translates the differential signal from CANH and CANL to a digital output on RXD.

8.4.3 Silent Mode

Activate *Silent mode* by setting S terminal high. The CAN driver is disabled, preventing communication from the TXD pin to the CAN bus. The high speed receiver remains active so that CAN bus communication continues to be relayed to the RXD output pin.

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8.4.4 Driver and Receiver Function Tables

表 8-4. Driver Function Table

DEVICE	INPUTS		OUTPUTS		DRIVEN BUS STATE
	S (1)	TXD(1) (2)	CANH(1)	CANL(1)	
All Devices	L or open	L	H	L	Dominant
		H or Open	Z	Z	Recessive
	H	X	Z	Z	Recessive

(1) H = high level, L = low level, X = irrelevant, Z = common mode (recessive) bias to V_{CC} / 2. See CAN Bus States for bus state and common mode bias information.
(2) Devices have an internal pull up to V_{CC} or V_{IO} on TXD terminal. If the TXD terminal is open, the terminal is pulled high and the transmitter remain in recessive (non-driven) state.

表 8-5. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD TERMINAL(1)
Normal or Silent	$V_{ID} \geqslant V_{IT+(MAX)}$	Dominant	L(2)
	$V_{IT-(MIN)} < V_{ID} < V_{IT+(MAX)}$	?	?(2)
	$V_{ID} \leqslant V_{IT-(MIN)}$	Recessive	H(2)
	Open ($V_{ID} \approx 0$ V)	Open	H

(1) H = high level, L = low level, ? = indeterminate.
(2) See *Receiver Electrical Characteristics* section for input thresholds.

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9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

These CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. Below are typical application configurations for both 5 V and 3.3 V microprocessor applications. The bus termination is shown for illustrative purposes.

9.2 Typical Applications

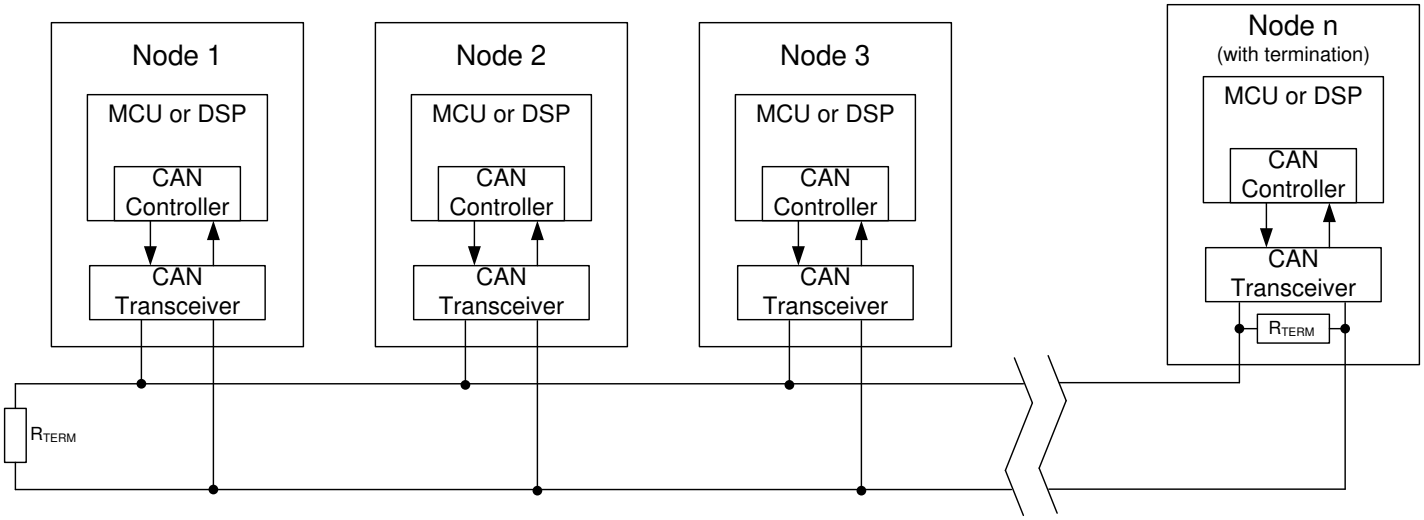


图 9-1. Typical CAN Bus Application

9.2.1 Design Requirements

9.2.1.1 Bus Loading, Length and Number of Nodes

The ISO 11898-2 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the TCAN1051 family of transceivers.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2. They have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, DeviceNet and NMEA2000.

The TCAN1051 family is specified to meet the 1.5 V requirement with a 50Ω load, incorporating the worst case including parallel transceivers. The differential input resistance of the TCAN1051 family is a minimum of 30 kΩ. If 100 TCAN1051 family transceivers are in parallel on a bus, this is equivalent to a 300Ω differential load worst case. That transceiver load of 300 Ω in parallel with the 60Ω gives an equivalent loading of 50 Ω. Therefore, the TCAN1051 family theoretically supports up to 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 m by careful system

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design and datarate tradeoffs. For example CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

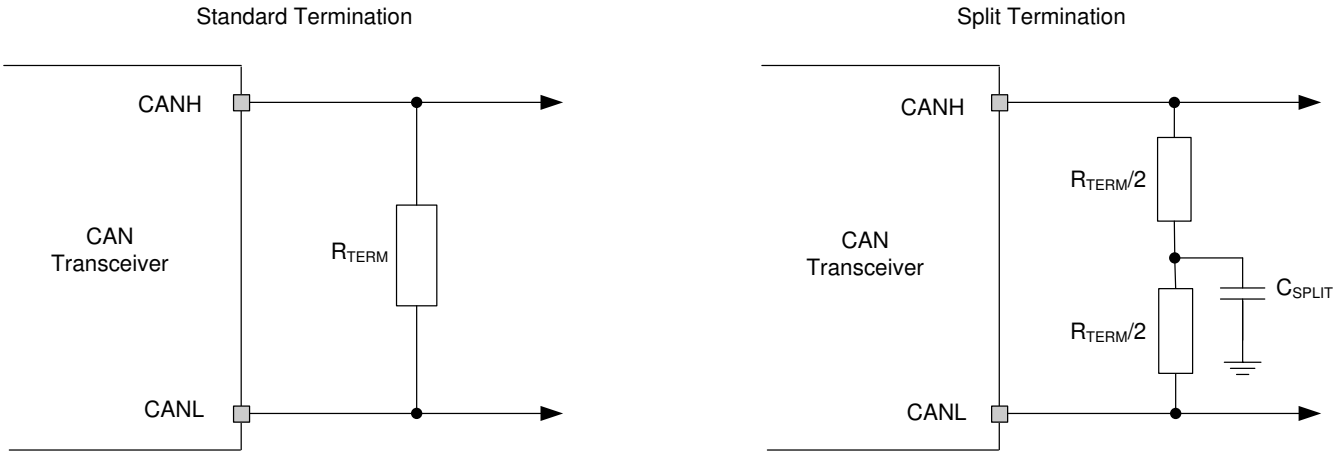
This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. In using this flexibility comes the responsibility of good network design and balancing these tradeoffs.

9.2.2 Detailed Design Procedures

9.2.2.1 CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that two terminations always exist on the network.

Termination may be a single 120-Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. (See 图 9-2). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.



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图 9-2. CAN Bus Termination Concepts

The TCAN1051 family of transceivers have variants for both 5-V only applications and applications where level shifting is needed for a 3.3-V micrcontroller.

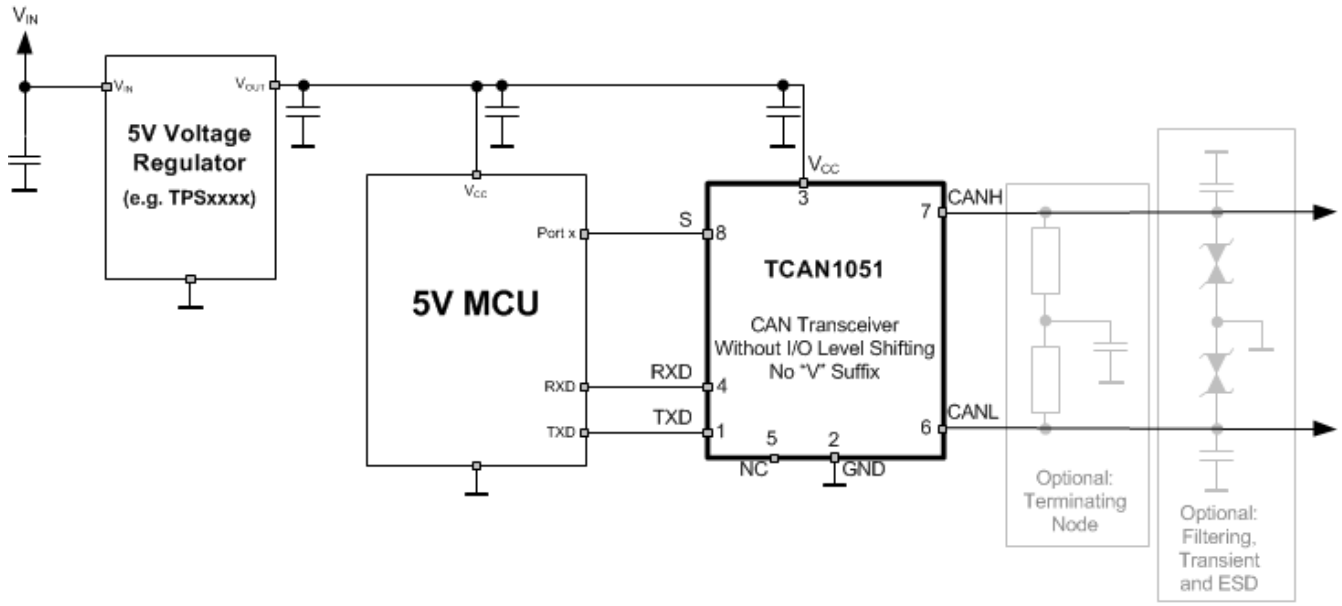


图 9-3. Typical CAN Bus Application Using 5 V CAN Controller

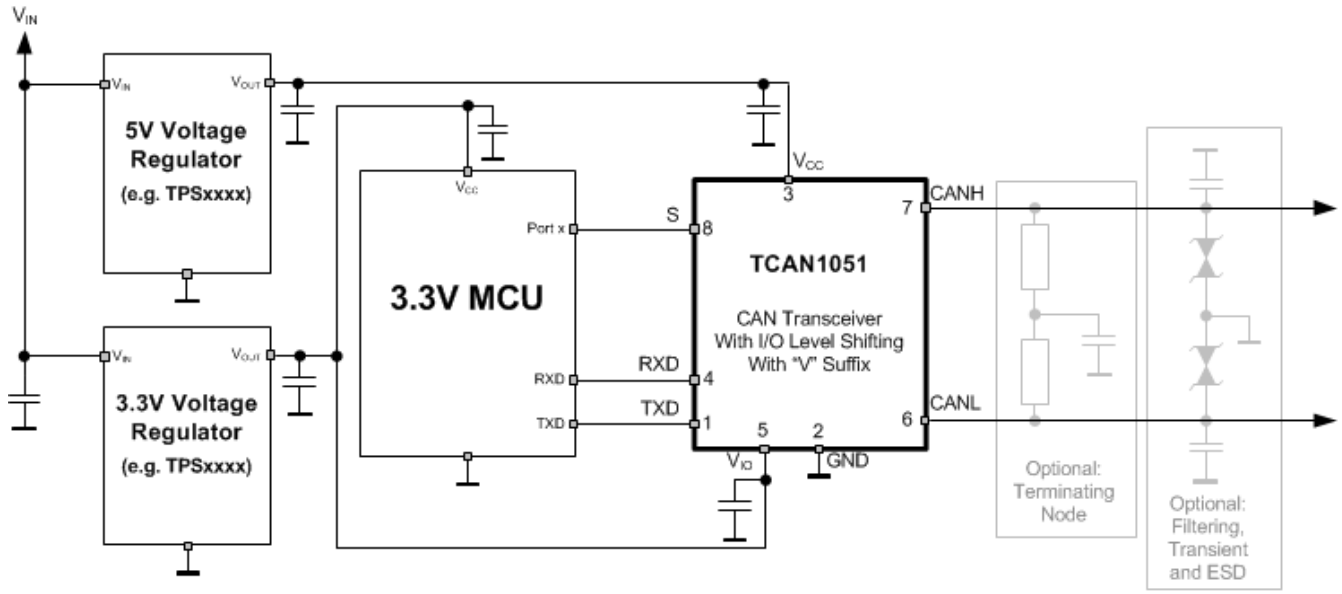
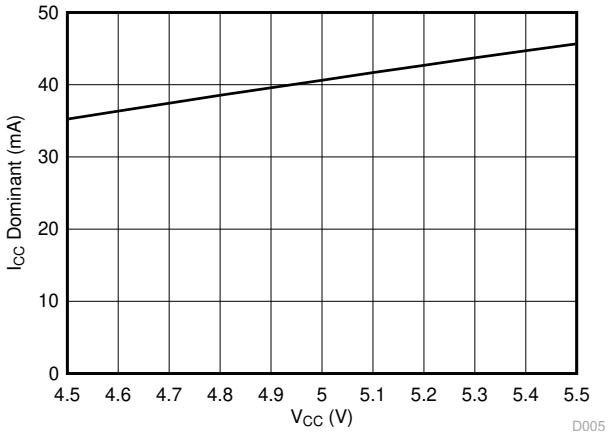


图 9-4. Typical CAN Bus Application Using 3.3 V CAN Controller

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9.2.3 Application Curves



V_{CC} = 4.5 V to 5.5 V V_{IO} = 3.3 V R_L = 60 Ω
C_L = Open Temp = 25°C S = 0 V

图 9-5. I_{CC} Dominant Current over V_{CC} Supply Voltage

10 Power Supply Recommendations

These devices are designed to operate from a V_{CC} input supply voltage range between 4.5 V and 5.5 V. Some devices have an output level shifting supply input, V_{IO}, designed for a range between 3 V and 5.5 V. Both supply inputs must be well regulated. A bulk capacitance, typically 4.7 µF, should be placed near the CAN transceiver's main V_{CC} supply output, and in addition a bypass capacitor, typically 0.1 µF, should be placed as close to the device V_{CC} and V_{IO} supply terminals. This helps to reduce supply voltaeg ripple present on the outputs of the switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes and traces.

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Layout

Robust and reliable bus node design often requires the use of external transient protection device in order to protect against EFT and surge transients that may occur in industrial enviroments. Because ESD and transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design. The TCAN1051 family comes with high on-chip IEC ESD protection, but if higher levels of system level immunity are desired external TVS diodes can be used. TVS diodes and bus filtering capacitors should be placed as close to the on-board connectors as possible to prevent noisy transient events from propagating further into the PCB and system.

11.1 Layout Guidelines

- Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. In this layout example a transient voltage suppression (TVS) device, D1, has been used for added protection. The production solution can be either bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C4 and C5. Additionally (not shown) a series common mode choke (CMC) can be placed on the CANH and CANL lines between the transceiver U1 and connector J1.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Use supply (V_{CC}) and ground planes to provide low inductance.

Note

High-frequency currents follows the path of least impedance and not the path of least resistance.

- Use at least two vias for supply (V_{CC}) and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver, examples are C1, C2 on the V_{CC} supply and C6 and C7 on the V_{IO} supply.
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R6 and R7, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to ensure the terminating node is not removed from the bus thus also removing the termination. See the application section for information on power ratings needed for the termination resistor(s).
- To limit current of digital lines, serial resistors may be used. Examples are R2, R3, and R4. These are not required.
- Terminal 1: R1 is shown optionally for the TXD input of the device. If an open drain host processor is used, this is mandatory to ensure the bit timing into the device is met.
- Terminal 5: For "V" variants of the TCAN1051 family, bypass capacitors should be placed as close to the pin as possible (example C6 and C7). For device options without V_{IO} I/O level shifting, this pin is not internally connected and can be left floating or tied to any existing net, for example a split pin connection.
- Terminal 8: is shown assuming the mode terminal, S, will be used. If the device will only be used in normal mode, R4 is not needed and R5 could be used for the pull down resistor to GND.

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11.2 Layout Example

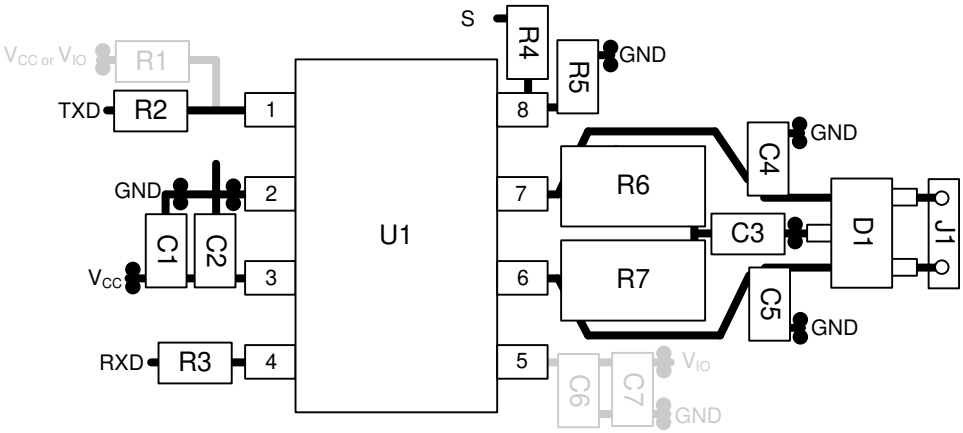


图 11-1. Layout Example

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11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN1051DQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051DRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051DRBTQ1	ACTIVE	SON	DRB	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051DRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051GDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051GDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051GDRBTQ1	ACTIVE	SON	DRB	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051GDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051GVDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051GVDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051GVDRBTQ1	ACTIVE	SON	DRB	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051GVDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051HDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051HDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051HDRBTQ1	ACTIVE	SON	DRB	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051HDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051HGDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051HGDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051HGDRBTQ1	ACTIVE	SON	DRB	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051	Samples
TCAN1051HGDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN1051HGVDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051HGVDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051HGVDRBTQ1	ACTIVE	SON	DRB	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051HGVDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051HVDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051HVDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051HVDRBTQ1	ACTIVE	SON	DRB	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051HVDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051VDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051VDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051VDRBTQ1	ACTIVE	SON	DRB	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	1051V	Samples
TCAN1051VDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1051V	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TCAN1051H-Q1, TCAN1051HG-Q1, TCAN1051HGV-Q1, TCAN1051HV-Q1 :

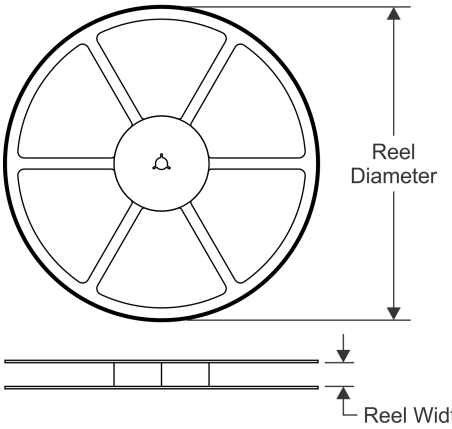
- Catalog : TCAN1051H, TCAN1051HG, TCAN1051HGV, TCAN1051HV

NOTE: Qualified Version Definitions:

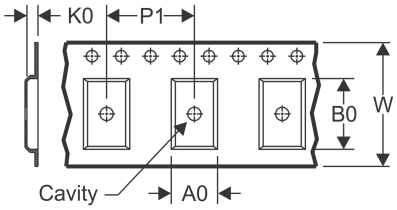
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

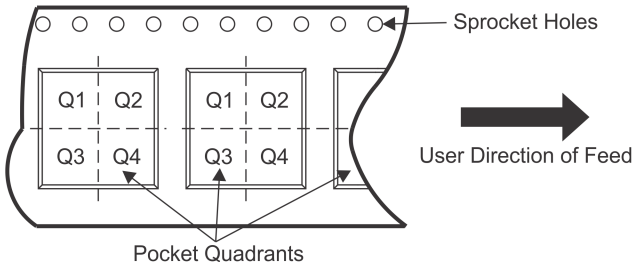


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

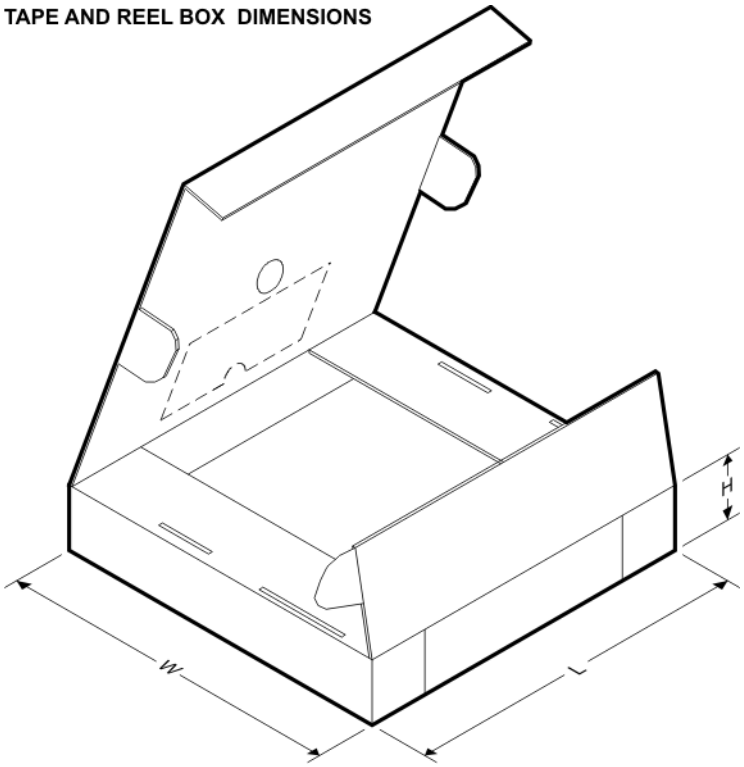


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1051DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051DRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051DRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1051DRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1051GDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051GDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051GDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1051GDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1051GVDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051GVDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051GVDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1051GVDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1051HDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051HDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051HDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1051HDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1051HGDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051HGDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1051HGDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1051HGVDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051HGVDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051HGVDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1051HGVDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1051HVDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051HVDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051HVDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1051HVDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1051VDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051VDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1051VDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

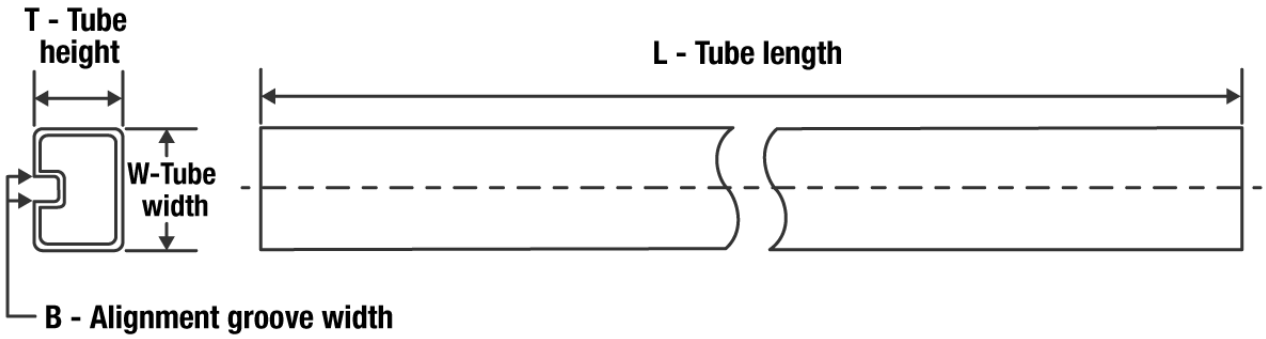


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1051DRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1051DRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1051DRQ1	SOIC	D	8	2500	853.0	449.0	35.0
TCAN1051DRQ1	SOIC	D	8	2500	340.5	336.1	25.0
TCAN1051GDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1051GDRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1051GDRQ1	SOIC	D	8	2500	853.0	449.0	35.0
TCAN1051GDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
TCAN1051GVDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1051GVDRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1051GVDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
TCAN1051GVDRQ1	SOIC	D	8	2500	853.0	449.0	35.0
TCAN1051HDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1051HDRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1051HDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
TCAN1051HDRQ1	SOIC	D	8	2500	853.0	449.0	35.0
TCAN1051HGDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1051HGDRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1051HGDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
TCAN1051HGVDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1051HGVDRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1051HGVDRQ1	SOIC	D	8	2500	853.0	449.0	35.0
TCAN1051HGVDRQ1	SOIC	D	8	2500	340.5	338.1	20.6
TCAN1051HVDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1051HVDRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1051HVDRQ1	SOIC	D	8	2500	853.0	449.0	35.0
TCAN1051HVDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
TCAN1051VDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1051VDRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1051VDRQ1	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TCAN1051DQ1	D	SOIC	8	75	507	8	3940	4.32
TCAN1051GDQ1	D	SOIC	8	75	507	8	3940	4.32
TCAN1051GVDQ1	D	SOIC	8	75	507	8	3940	4.32
TCAN1051HDQ1	D	SOIC	8	75	507	8	3940	4.32
TCAN1051HGDQ1	D	SOIC	8	75	507	8	3940	4.32
TCAN1051HGVDQ1	D	SOIC	8	75	507	8	3940	4.32
TCAN1051HVDQ1	D	SOIC	8	75	507	8	3940	4.32
TCAN1051VDQ1	D	SOIC	8	75	507	8	3940	4.32

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

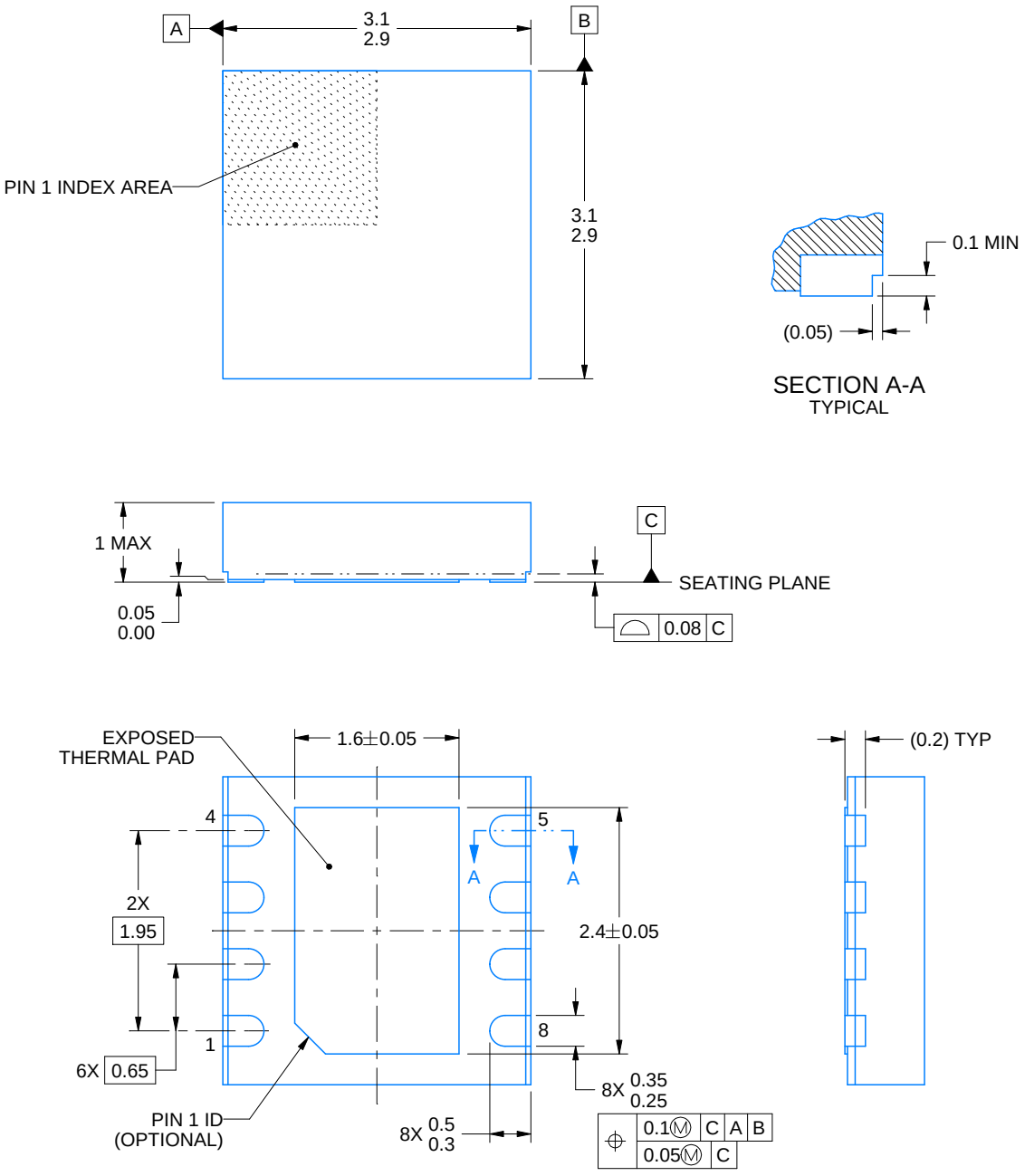
4203482/L

DRB0008F

PACKAGE OUTLINE

VSON - 1 mm max height

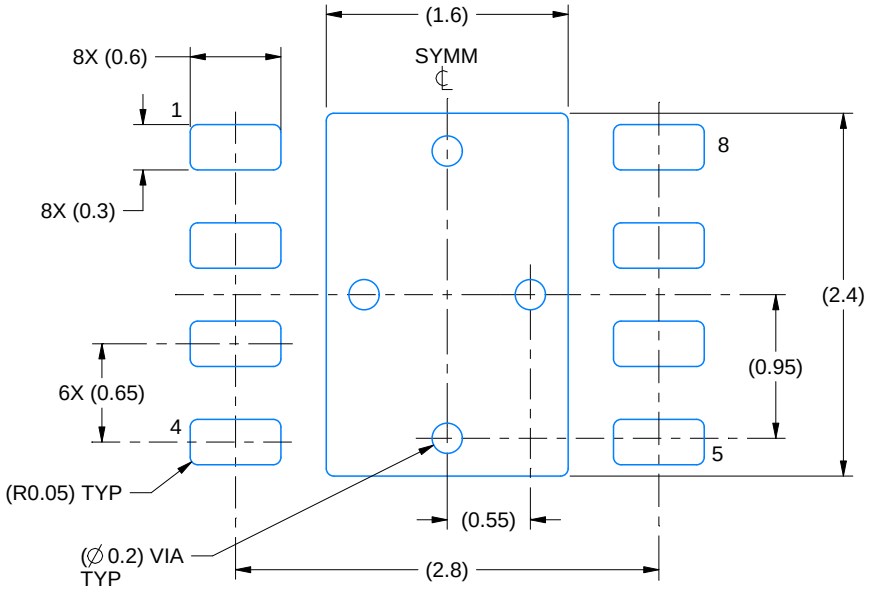
PLASTIC SMALL OUTLINE - NO LEAD



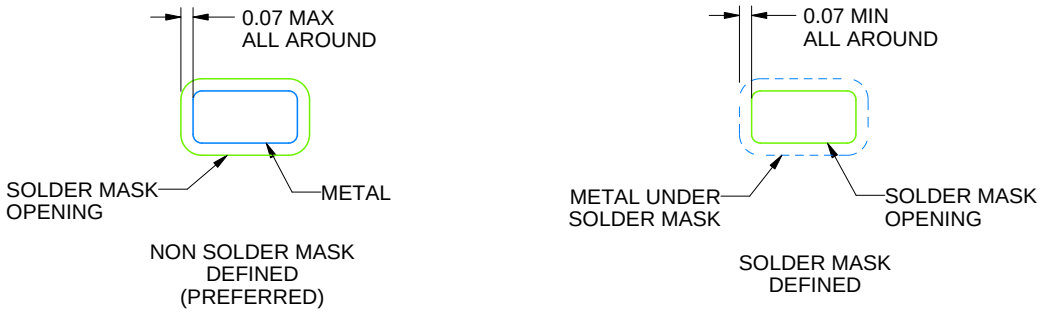
4222121/C 10/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

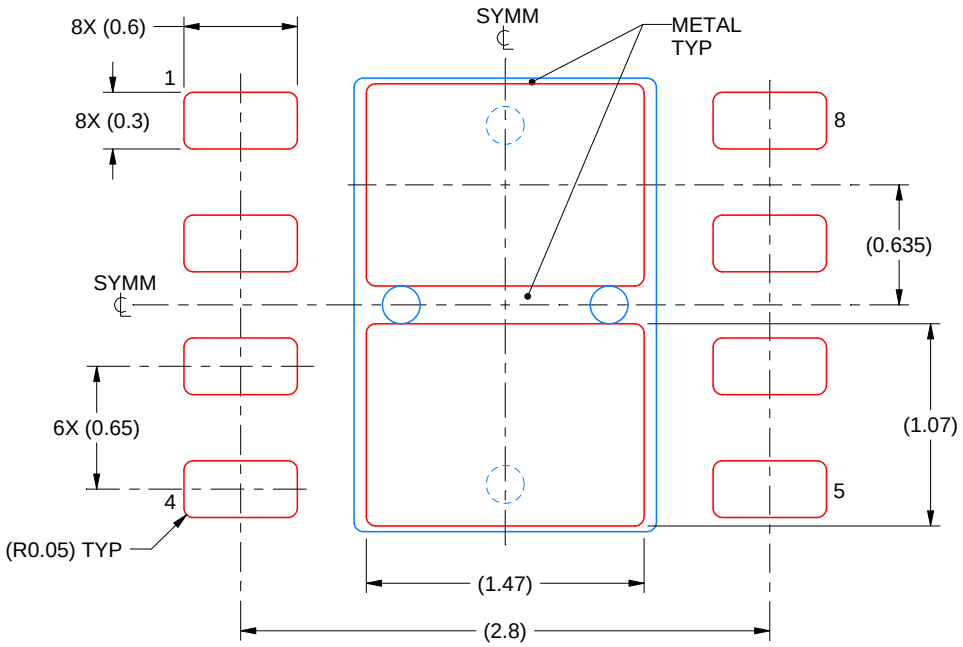


SOLDER MASK DETAILS

4222121/C 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



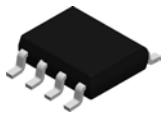
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222121/C 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

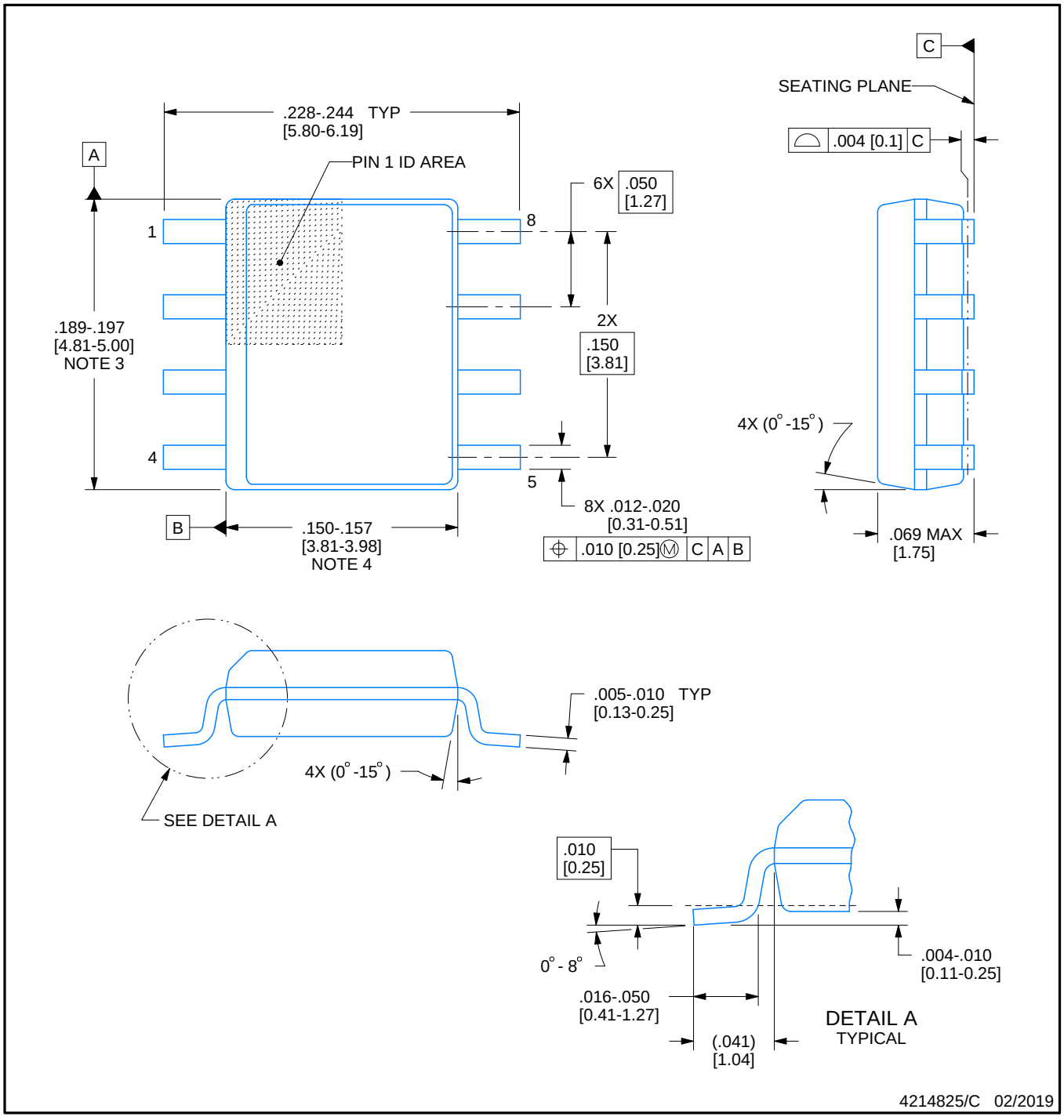


PACKAGE OUTLINE

D0008A

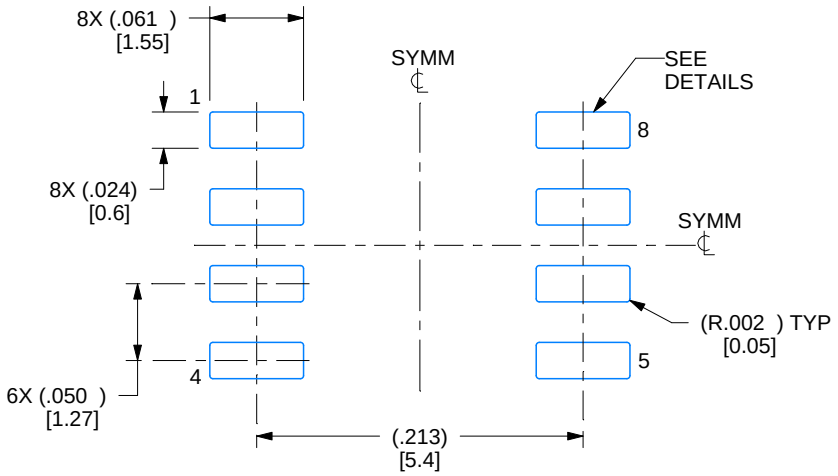
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

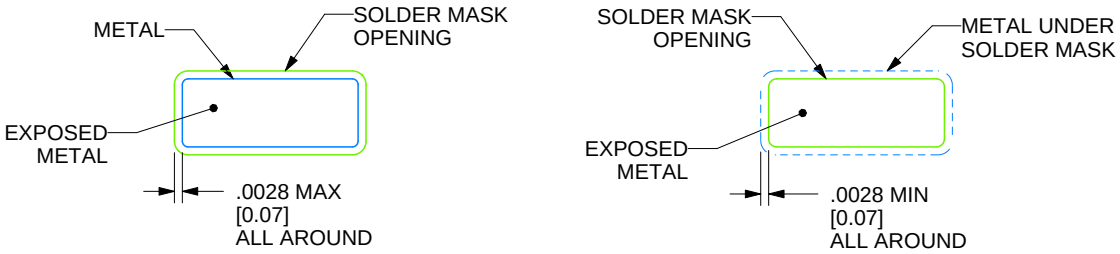


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

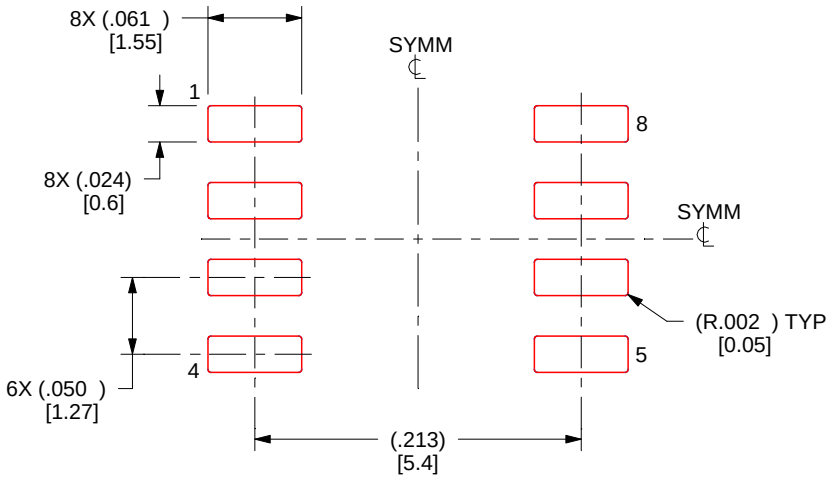
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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