HIGH-SPEED FULLY DIFFERENTIAL I/O AMPLIFIERS

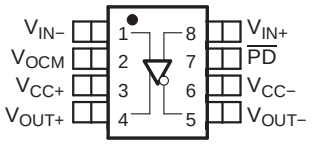
FEATURES

- **High Performance**
  - **160 MHz –3 dB Bandwidth (V_{CC} = ±15 V)**
  - **450 V/µs Slew Rate**
  - **–79 dB, Third Harmonic Distortion at 1 MHz**
  - **6.5 nV/√Hz Input-Referred Noise**
- **Differential Input/Differential Output**
  - **Balanced Outputs Reject Common-Mode Noise**
  - **Reduced Second Harmonic Distortion Due to Differential Output**
- **Wide Power-Supply Range**
  - **V_{CC} = 5-V Single Supply to ±15-V Dual Supply**
- **$I_{CC(SD)}$ = 880 µA in Shutdown Mode (THS4140)**

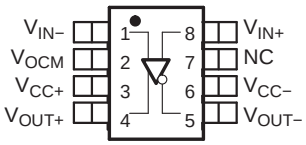
KEY APPLICATIONS

- **Single-Ended to Differential Conversion**
- **Differential ADC Driver**
- **Differential Antialiasing**
- **Differential Transmitter And Receiver**
- **Output Level Shifter**

THS4140
D, DGN, OR DGK PACKAGE
(TOP VIEW)



THS4141
D, DGN, OR DGK PACKAGE
(TOP VIEW)



HIGH-SPEED DIFFERENTIAL I/O FAMILY

DEVICE	NUMBER OF CHANNELS	SHUTDOWN
THS4140	1	X
THS4141	1	–

DESCRIPTION

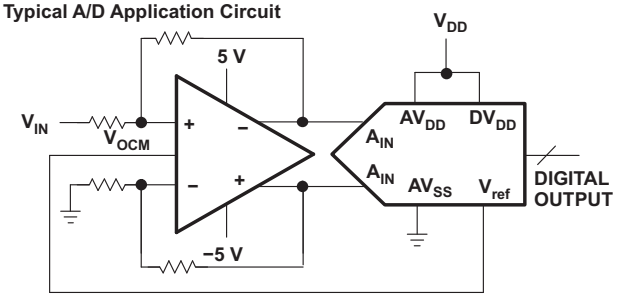
The THS414x is one in a family of fully differential input/differential output devices fabricated using Texas Instruments' state-of-the-art BiComI complementary bipolar process.

The THS414x is made of a true, fully differential signal path from input to output. This design leads to an excellent common-mode noise rejection and improved total harmonic distortion.

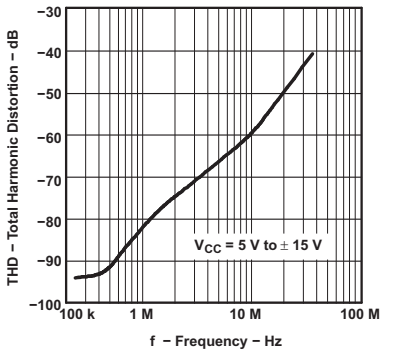
RELATED DEVICES

DEVICE	DESCRIPTION
THS412x	100 MHz, 43 V/µs, 3.7 nV/√Hz
THS413x	150 MHz, 51 V/µs, 1.3 nV/√Hz
THS415x	150 MHz, 650 V/µs, 7.6 nV/√Hz

Typical A/D Application Circuit



TOTAL HARMONIC DISTORTION vs FREQUENCY



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. AVAILABLE OPTIONS

T_A	PACKAGED DEVICES(1)					EVALUATION MODULES
	SMALL OUTLINE (D)	MSOP PowerPAD™		MSOP		
		(DGN)	SYMBOL	(DGK)	SYMBOL	
0°C to 70°C	THS4140CD	THS4140CDGN	AOF	THS4140CDGK	ATR	THS4140EVM
	THS4141CD	THS4141CDGN	AOI	THS4141CDGK	ATS	THS4141EVM
–40°C to 85°C	THS4140ID	THS4140IDGN	AOG	THS4140IDGK	ASQ	–
	THS4141ID	THS4141IDGN	AOK	THS4141IDGK	ASR	–

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{CC}	Supply voltage	$V_{CC–}$ to V_{CC+}	±16.5 V
V_I	Input voltage		$\pm V_{CC}$
I_O	Output current(2)		150 mA
V_{ID}	Differential input voltage		±6 V
	Continuous total power dissipation		See Dissipation Rating Table
T_J	Maximum junction temperature(3)		150°C
	Maximum junction temperature, continuous operation, long term reliability(4)		125°C
T_A	Operating free-air temperature	C suffix	0°C to 70°C
		I suffix	–40°C to 85°C
T_{stg}	Storage temperature		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 Inch) from case for 10 seconds		300°C
	ESD ratings	HBM	2500 V
		CDM	1500 V
		MM	200 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The THS414x may incorporate a PowerPad™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 and SLMA004 for more information about utilizing the PowerPad™ thermally enhanced package.
(3) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.
(4) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA}(1) (°C/W)	θ_{JC} (°C/W)	POWER RATING(2)	
			T_A = 25°C	T_A = 85°C
D	97.5	38.3	1.02 W	410 mW
DGN	58.4	4.7	1.71 W	685 mW
DGK	260	54.2	385 mW	154 mW

(1) This data was taken using the JEDEC standard High-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long term reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage, V_{CC-} to V_{CC+}	Dual supply	±2.5		±15	V
		Single supply	5		30	
T_A	Operating free-air temperature	C suffix	0		70	°C
		I suffix	–40		85	

ELECTRICAL CHARACTERISTICS

V_{CC} = ±5 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small signal bandwidth (–3 dB)	V_{CC} = ±5,	Gain = 1, R_f = 390 Ω		150		MHz
		V_{CC} = ±15,	Gain = 1, R_f = 390 Ω		160		MHz
SR	Slew rate(2)	Gain = 1			450		V/µs
t_s	Settling time to 0.1%	Differential step voltage = 2 V_{PP}, Gain = 1			96		ns
	Settling time to 0.01%				304		
DISTORTION PERFORMANCE							
Second harmonic distortion, differential in/differential out		1 MHz	V_O = 2 V_{PP}		–85		dB
		8 MHz	V_O = 2 V_{PP}		–65		
Third harmonic distortion, differential in/differential out		1 MHz	V_O = 2 V_{PP}		–79		dB
		8 MHz	V_O = 2 V_{PP}		–55.5		
THD	Total harmonic distortion Differential input, differential output Gain = 1, R_f = 390 Ω, R_L = 800 Ω, V_O = 2 V_{PP}	V_{CC} = 5	f = 1 MHz		–78		dB
		V_{CC} = ±5	f = 1 MHz		–78		
		V_{CC} = ±15	f = 1 MHz		–79		
Spurious free dynamic range (SFDR)					–79		dB
Intermodulation distortion		5 MHz			–103		dBc
Third-order intercept		20 MHz			37		dB
NOISE PERFORMANCE							
V_n	Input voltage noise	f = 10 kHz			6.5		nV/√Hz
I_n	Input current noise	f = 10 kHz			1.25		pA/√Hz
DC PERFORMANCE							
Open loop gain		T_A = 25°C		63	67		dB
		T_A = full range		60			
V_{OS}	Input offset voltage, differential	T_A = 25°C			1	7	mV
	Input offset voltage, referred to V_{OCM}	T_A = full range				8.5	
		T_A = 25°C			0.5	8	
	Offset drift	T_A = full range			7		µV/°C
I_{IB}	Input bias curent	T_A = full range			5.1	15	µA
I_{OS}	Input offset current				0.1	1	µA
	Offset drift				0.3		nA/°C

(1) The full range temperature is 0°C to 70°C for the C suffix, and –40°C to 85°C for the I suffix.
(2) Slew rate is measured from an output level range of 25% to 75%.

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = ±5 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS							
CMRR	Common-mode rejection ratio	T_A = full range		75	84		dB
V_{ICR}	Common-mode input voltage range			–3.77 to 4.3	–4 to 4.5		V
R_I	Input resistance, closed loop	Measured into each input terminal			14.4		MΩ
C_I	Input capacitance				3.9		pF
r_o	Output resistance	Open loop			43		Ω
OUTPUT CHARACTERISTICS							
Output voltage swing		V_{CC} = 5 V	T_A = 25°C	1.2 to 3.8	0.9 to 4.1		V
			T_A = full range	1.3 to 3.7			
		V_{CC} = ±5 V	T_A = 25°C	±3.7	±3.9		
			T_A = full range	±3.6			
		V_{CC} = ±15 V	T_A = 25°C	±12	±12.9		
			T_A = full range	±11			
I_O	Output current, R_L = 7Ω	V_{CC} = 5 V	T_A = 25°C	35	45		mA
			T_A = full range	25			
		V_{CC} = ±5 V	T_A = 25°C	45	60		
			T_A = full range	35			
		V_{CC} = ±15 V	T_A = 25°C	65	85		
			T_A = full range	50			
POWER SUPPLY							
V_{CC}	Supply voltage range	Single supply		4		33	V
		Split supply		±2		±16.5	
I_{CC}	Quiescent current	V_{CC} = ±5 V	T_A = 25°C		13.2	16	mA
			T_A = full range			18	
		V_{CC} = ±15 V	T_A = 25°C		15		
$I_{CC(SD)}$	Quiescent current (shutdown) (THS4140) (3)	T_A = 25°C			0.88	1.2	mA
		T_A = full range				1.4	
PSRR	Power supply rejection ratio (dc)	T_A = 25°C		70	90		dB
		T_A = full range		65			

(3) For detailed information on the behavior of the power-down circuit, see the *power-down mode* description in the *Principles of Operation* section of this data sheet.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
PSRR	Power supply rejection ratio	vs Frequency (differential out)	1
	Small signal frequency response		2
	Large signal frequency response		3
CMMR	Common-mode rejection ratio	vs Frequency	4
	Small signal frequency response		5
SR	Slew rate		6
	Second harmonic distortion	vs Frequency	7
		vs Output voltage	8, 9
	Third harmonic distortion	vs Frequency	10, 11
		vs Output voltage	12, 13
	Settling time		14
V_n	Voltage noise	vs Frequency	15
	Single-ended output voltage	vs Common-mode output voltage	16
V_O	Output voltage	vs Differential load resistance	17
z_o	Output impedance	vs Frequency	18
	Input bias current	vs Supply voltage	19
	Output current range	vs Supply voltage	20

POWER SUPPLY REJECTION RATIO vs FREQUENCY (DIFFERENTIAL OUT)

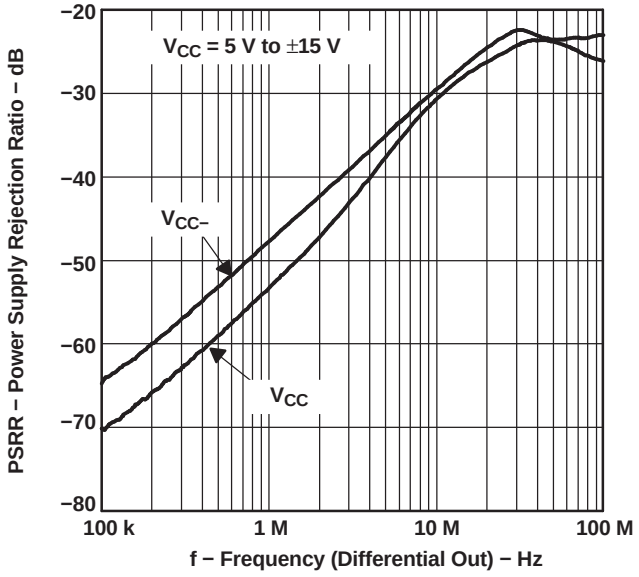


Figure 1.

SMALL SIGNAL FREQUENCY RESPONSE

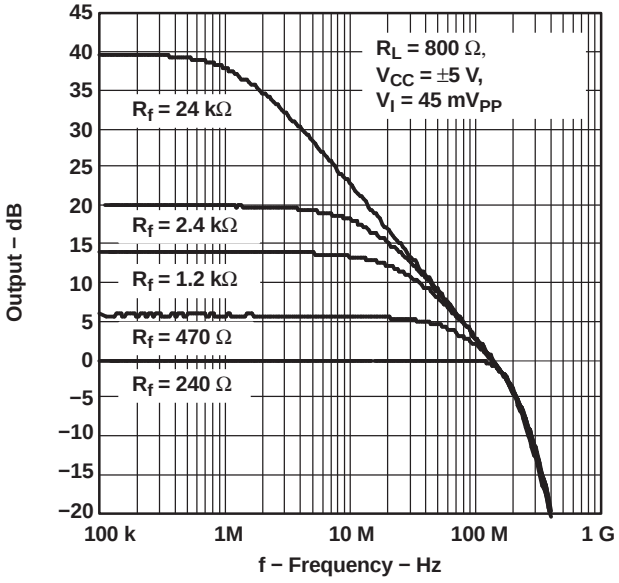


Figure 2.

TYPICAL CHARACTERISTICS (continued)

LARGE SIGNAL FREQUENCY RESPONSE

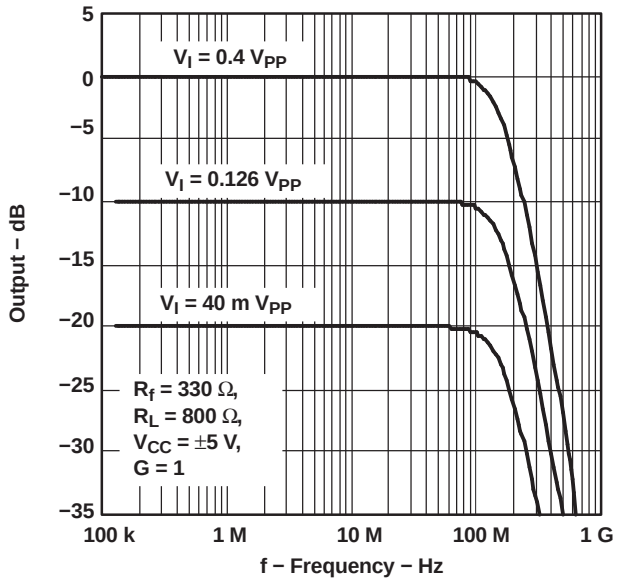


Figure 3.

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

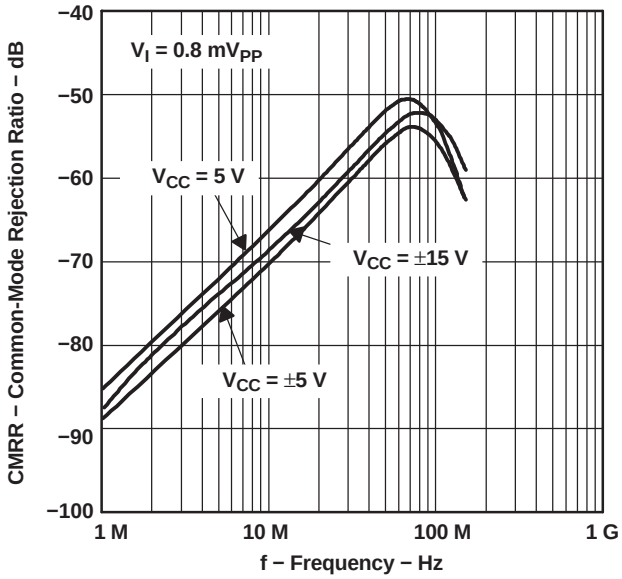


Figure 4.

SMALL SIGNAL FREQUENCY RESPONSE

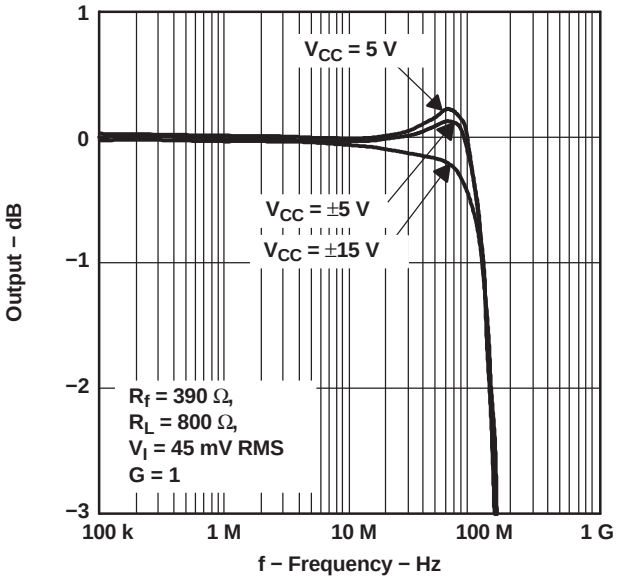


Figure 5.

SLEW RATE

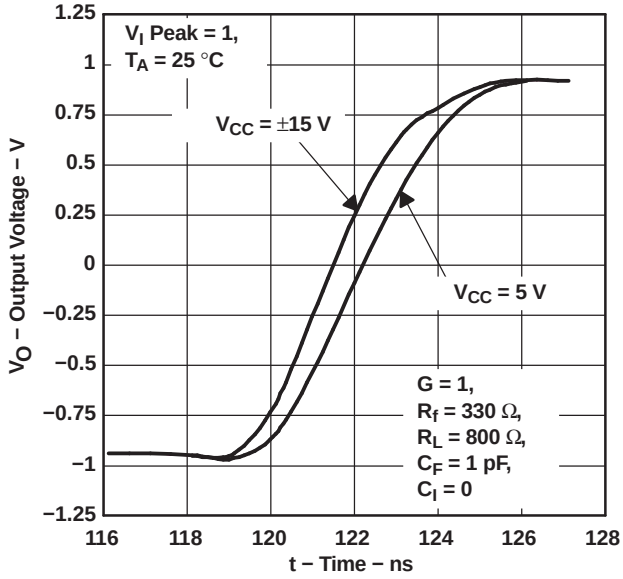


Figure 6.

TYPICAL CHARACTERISTICS (continued)

SECOND HARMONIC DISTORTION
vs
FREQUENCY

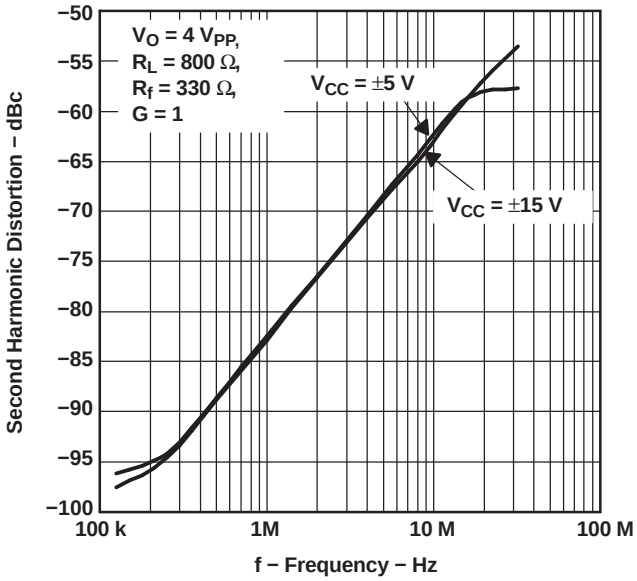


Figure 7.

SECOND HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

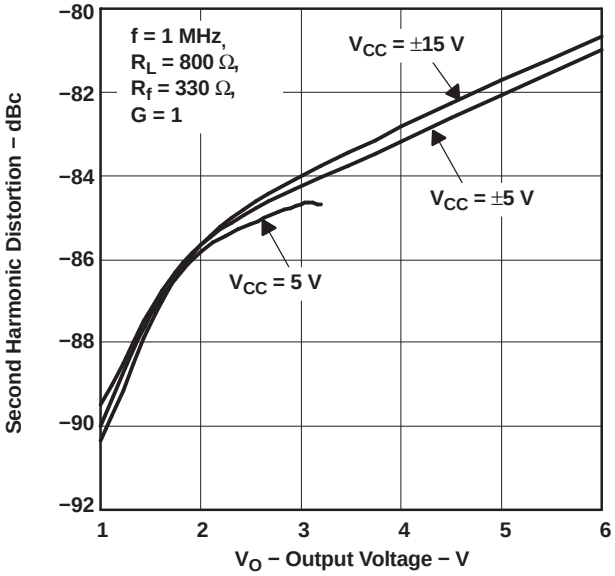


Figure 8.

SECOND HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

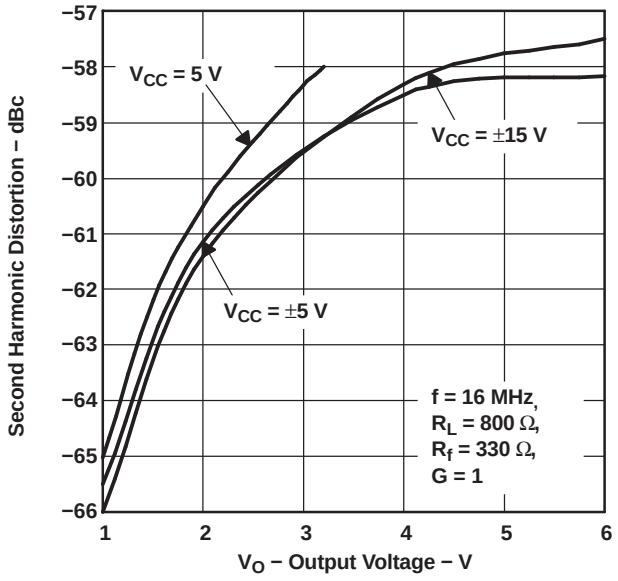


Figure 9.

THIRD HARMONIC DISTORTION
vs
FREQUENCY

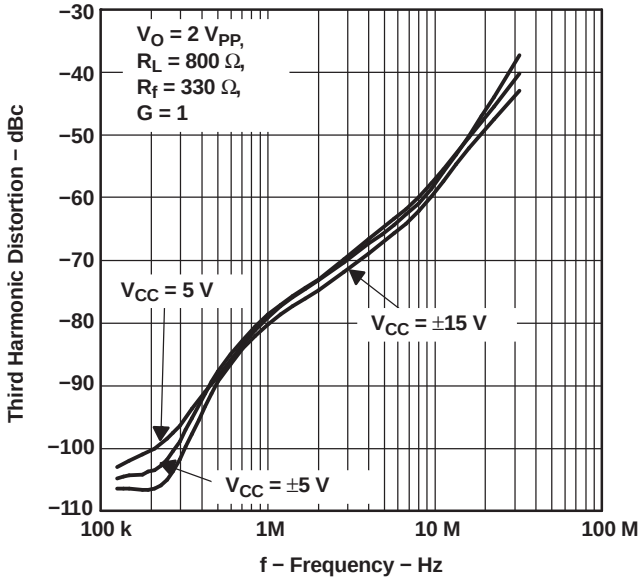


Figure 10.

TYPICAL CHARACTERISTICS (continued)

THIRD HARMONIC DISTORTION
vs
FREQUENCY

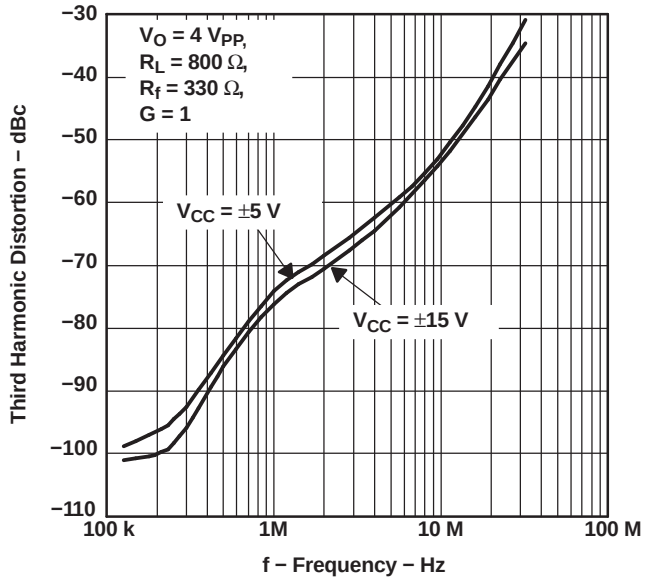


Figure 11.

THIRD HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

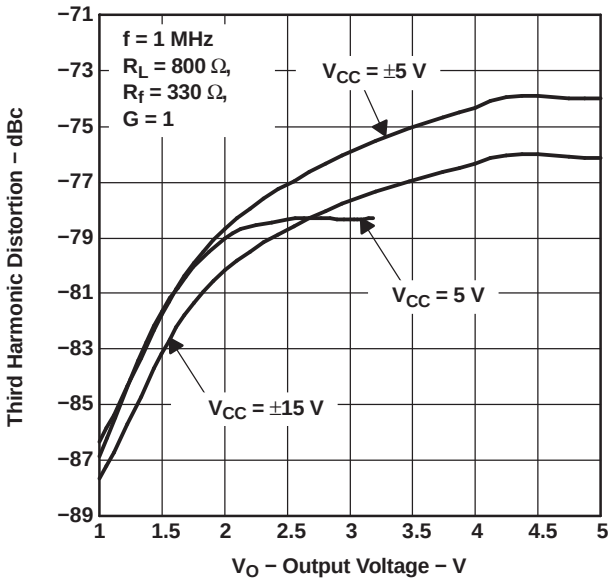


Figure 12.

THIRD HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

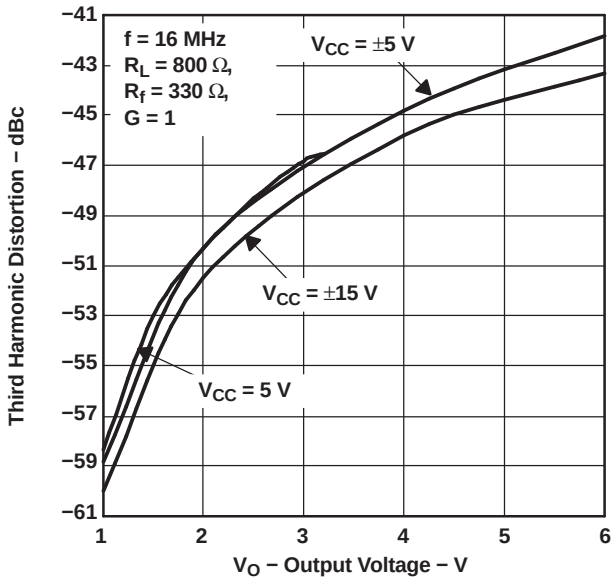


Figure 13.

SETTLING TIME

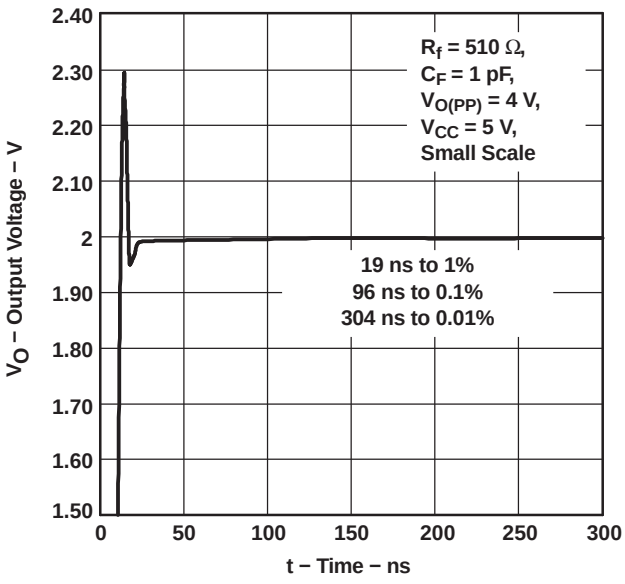


Figure 14.

TYPICAL CHARACTERISTICS (continued)

VOLTAGE NOISE vs FREQUENCY

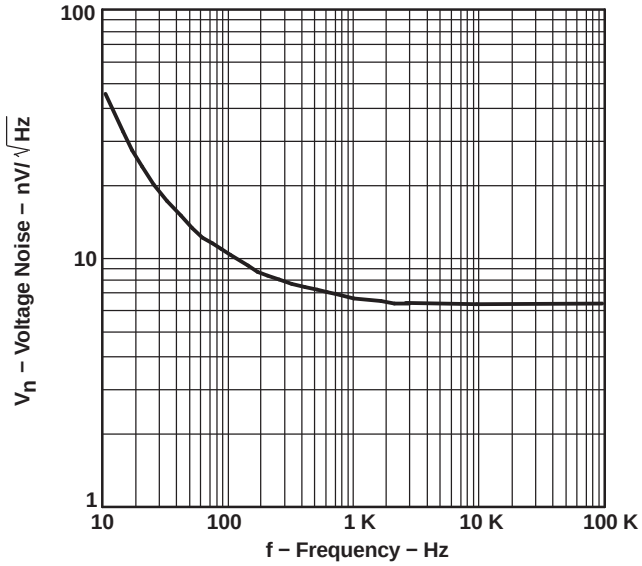


Figure 15.

SINGLE-ENDED INPUT OFFSET VOLTAGE vs COMMON-MODE OUTPUT VOLTAGE

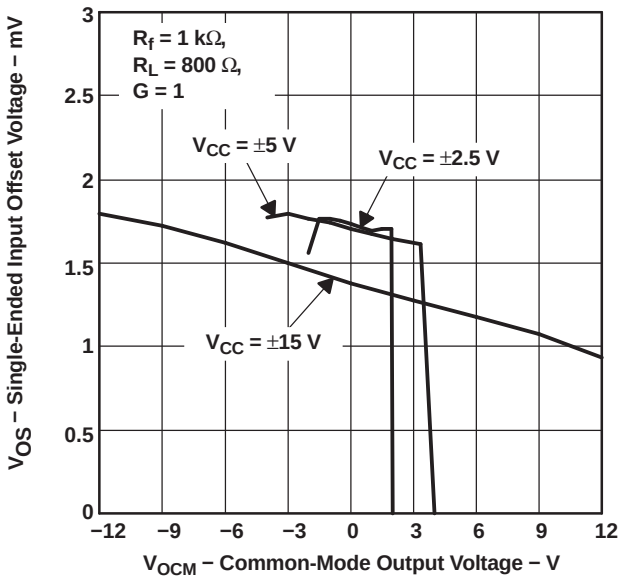


Figure 16.

OUTPUT VOLTAGE vs DIFFERENTIAL LOAD RESISTANCE

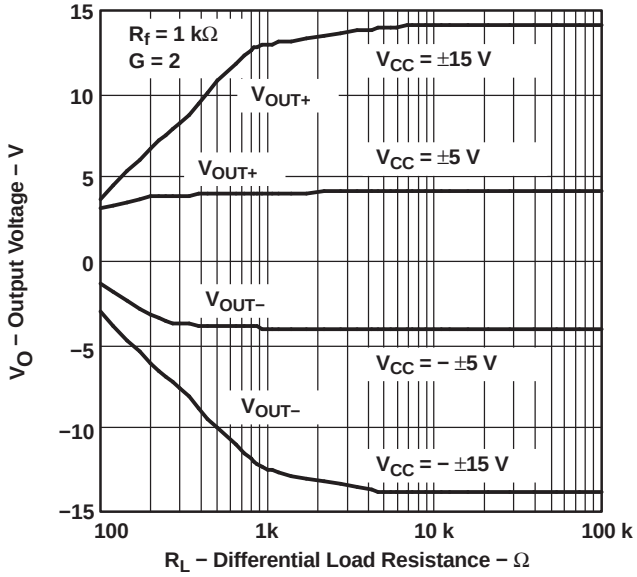


Figure 17.

OUTPUT IMPEDANCE vs FREQUENCY

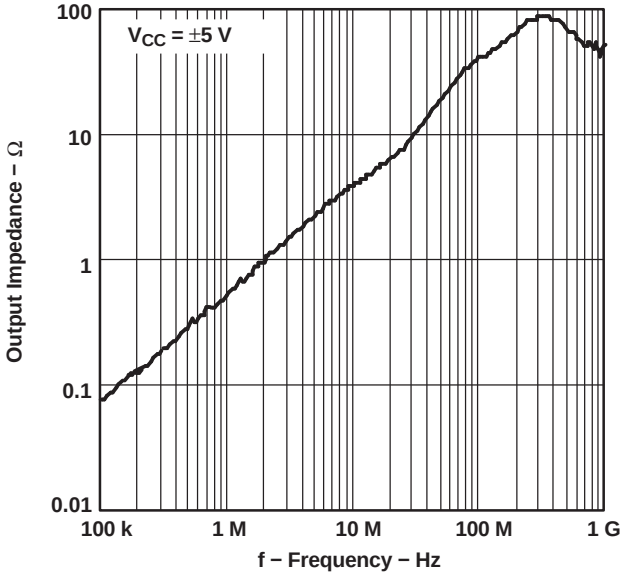


Figure 18.

TYPICAL CHARACTERISTICS (continued)

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

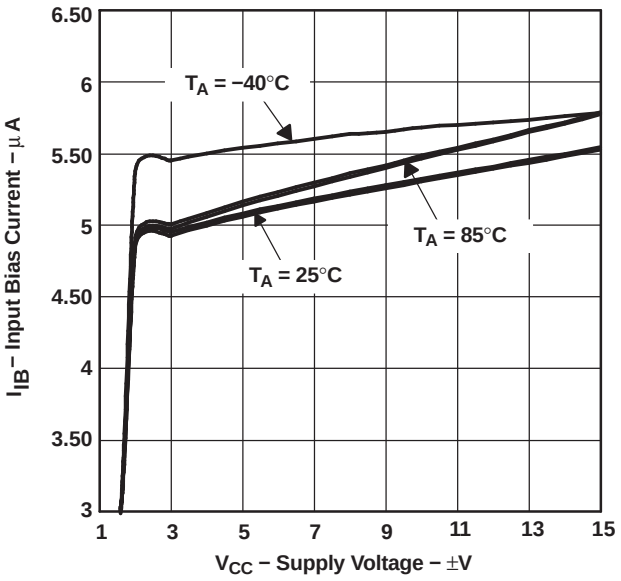


Figure 19.

OUTPUT CURRENT RANGE vs SUPPLY VOLTAGE

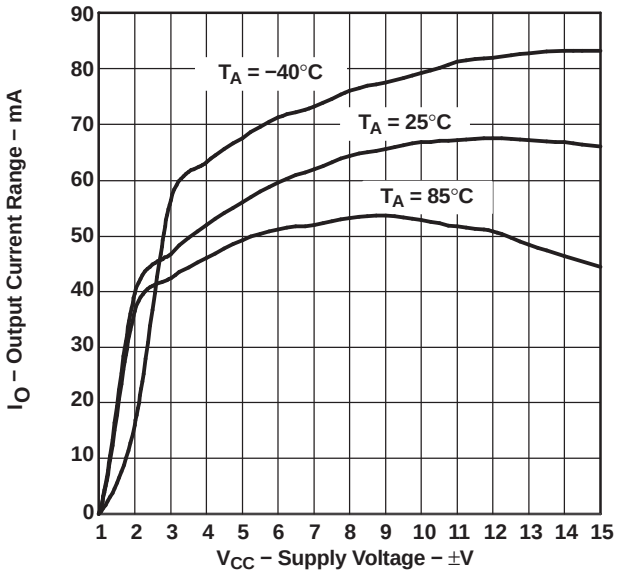


Figure 20.

APPLICATION INFORMATION

RESISTOR MATCHING

Resistor matching is important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion will diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

V_{OCM} sets the dc level of the output signals. If no voltage is applied to the V_{OCM} pin, it will be set to the midrail voltage internally defined as:

$$\frac{\left(V_{CC+}\right) + \left(V_{CC-}\right)}{2}$$

In the differential mode, the V_{OCM} on the two outputs cancel each other. Therefore, the output in the differential mode is the same as the input in the gain of 1. V_{OCM} has a high bandwidth capability up to the typical operation range of the amplifier. For the prevention of noise going through the device, use a 0.1 µF capacitor on the V_{OCM} pin as a bypass capacitor. Figure 21 shows the simplified diagram of the THS414x.

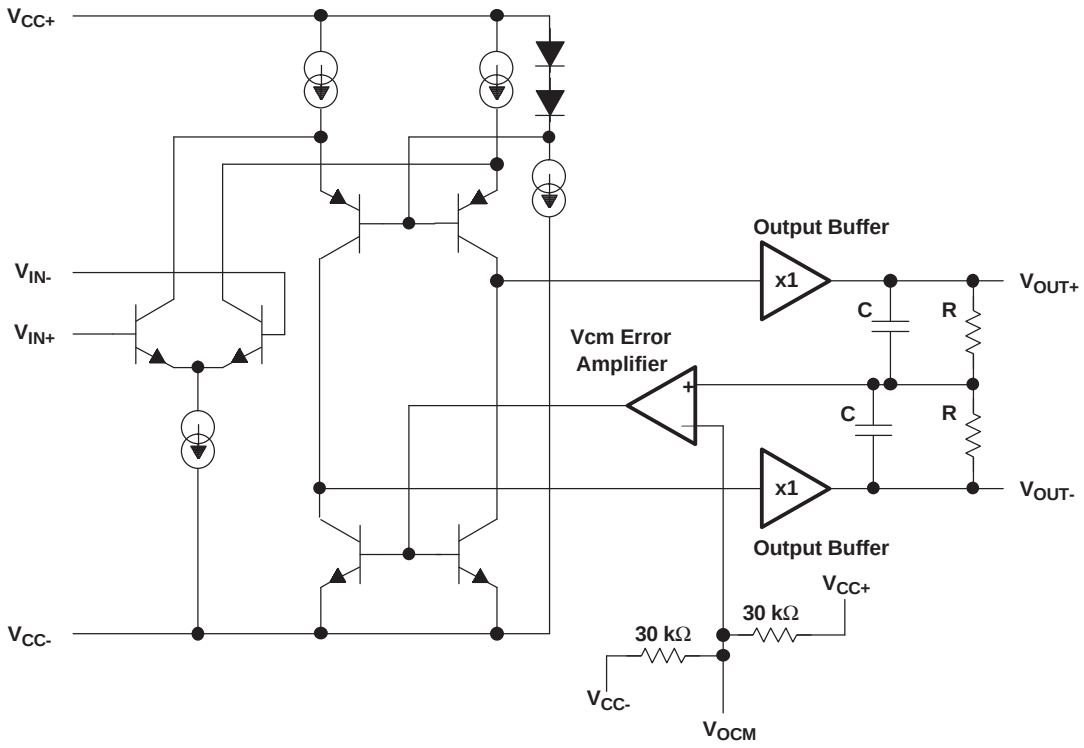


Figure 21. THS414x Simplified Diagram

APPLICATION INFORMATION (continued)

DATA CONVERTERS

Data converters are one of the most popular applications for the fully differential amplifiers. Figure 22 shows a typical configuration of a fully differential amplifier attached to a differential ADC.

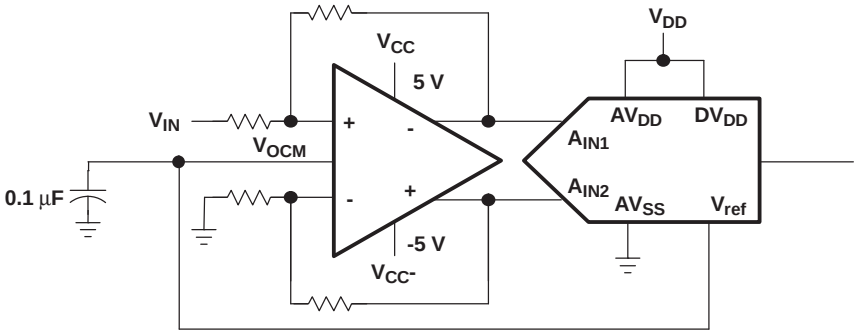


Figure 22. Fully Differential Amplifier Attached to a Differential ADC

Fully differential amplifiers can operate with a single supply. V_{OCM} defaults to the midrail voltage, $V_{CC}/2$. The differential output may be fed into a data converter. This method eliminates the use of a transformer in the circuit. If the ADC has a reference voltage output (V_{ref}), then it is recommended to connect it directly to the V_{OCM} of the amplifier using a bypass capacitor for stability. For proper operation, the input common-mode voltage to the input terminal of the amplifier should not exceed the common-mode input voltage range.

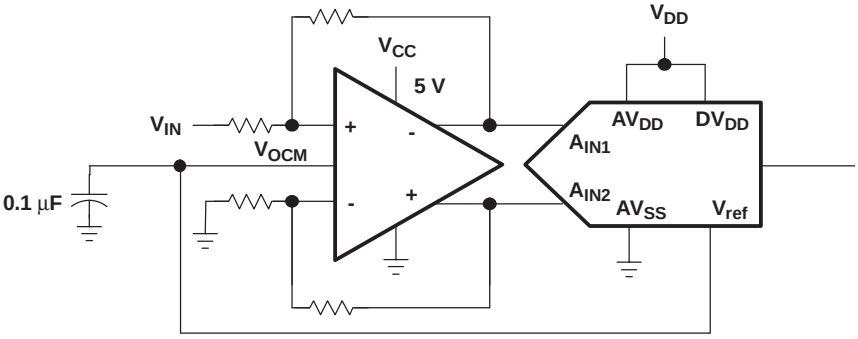


Figure 23. Fully Differential Amplifier Using a Single Supply

Some single supply applications may require the input voltage to exceed the common-mode input voltage range. In such cases, the following circuit configuration is suggested to bring the common-mode input voltage within the specifications of the amplifier.

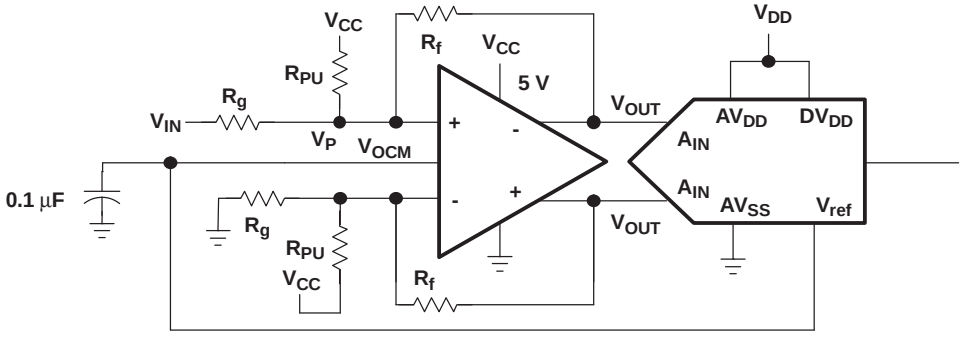


Figure 24. Circuit With Improved Common-Mode Input Voltage

APPLICATION INFORMATION (continued)

The following equation is used to calculate R_{PU}:

$$R_{PU} = \frac{V_P - V_{CC}}{\left(V_{IN} - V_P\right)\frac{1}{RG} + \left(V_{OUT} - V_P\right)\frac{1}{RF}} \quad (1)$$

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS414x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 25. A minimum value of 20 Ω should work well for most applications. For example, in 50-Ω transmission systems, setting the series resistor value to 50 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

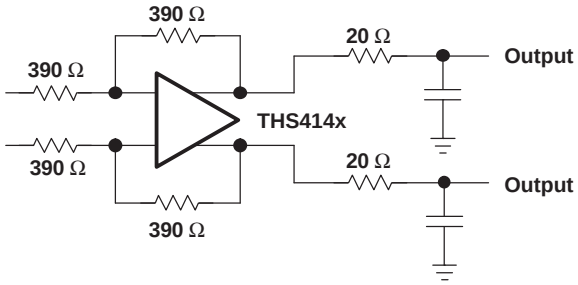


Figure 25. Driving a Capacitive Load

ACTIVE ANTIALIAS FILTERING

For signal conditioning in ADC applications, it is important to limit the input frequency to the ADC. Low-pass filters can prevent the aliasing of the high frequency noise with the frequency of operation. Figure 26 presents a method by which the noise may be filtered in the THS414x.

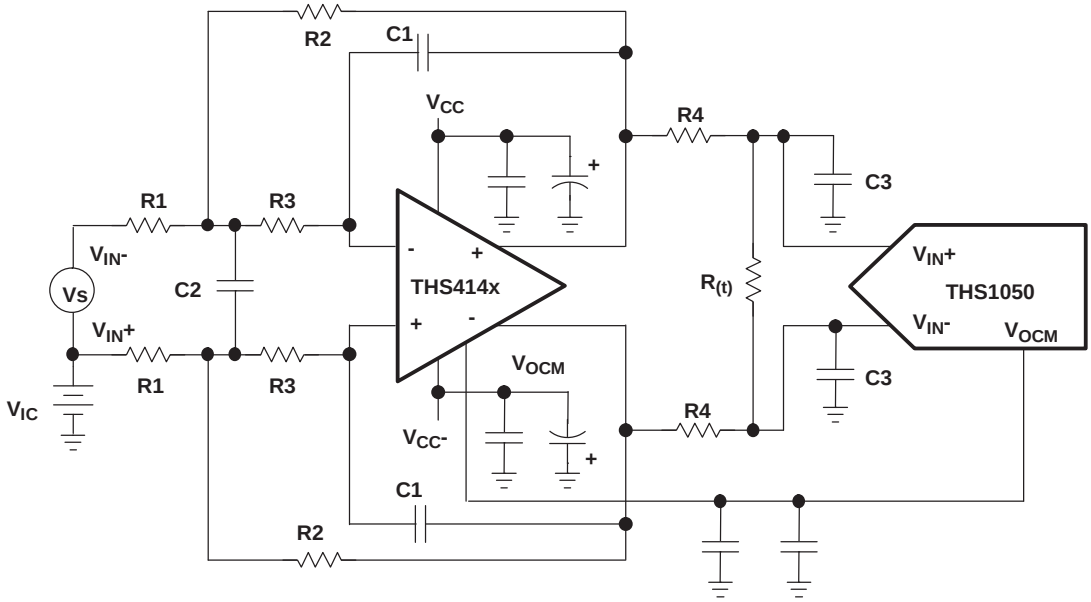


Figure 26. Antialias Filtering

APPLICATION INFORMATION (continued)

The transfer function for this filter circuit is:

$$H_d(f) = \left(\frac{K}{-\left(\frac{f}{FSF \times fc}\right)^2 + \frac{1}{Q}\frac{jf}{FSF \times fc} + 1} \right) \times \left(\frac{\frac{Rt}{2R4 + Rt}}{1 + \frac{j2\pi fR4RtC3}{2R4 + Rt}} \right) \quad \text{Where } K = \frac{R2}{R1} \tag{2}$$

$$FSF \times fc = \frac{1}{2\pi\sqrt{2 \times R2R3C1C2}} \text{ and } Q = \frac{\sqrt{2 \times R2R3C1C2}}{R3C1 + R2C1 + KR3C1} \tag{3}$$

K sets the pass band gain, fc is the cutoff frequency for the filter, FSF is a frequency-scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2} \text{ and } Q = \frac{\sqrt{Re^2 + |Im|^2}}{2Re} \tag{4}$$

Where Re is the real part, and Im is the imaginary part of the complex pole pair. Setting R2 = R, R3 = mR, C1 = C, and C2 = nC results in:

$$FSF \times fc = \frac{1}{2\pi RC\sqrt{2 \times mn}} \text{ and } Q = \frac{\sqrt{2 \times mn}}{1 + m(1 + K)} \tag{5}$$

Start by determining the ratios, m and n, required for the gain and Q of the filter type being designed, then select C and calculate R for the desired fc.

PRINCIPLES OF OPERATION

THEORY OF OPERATION

The THS414x is a fully differential amplifier. Differential amplifiers are typically *differential in/single out*, whereas fully differential amplifiers are *differential in/differential out*.

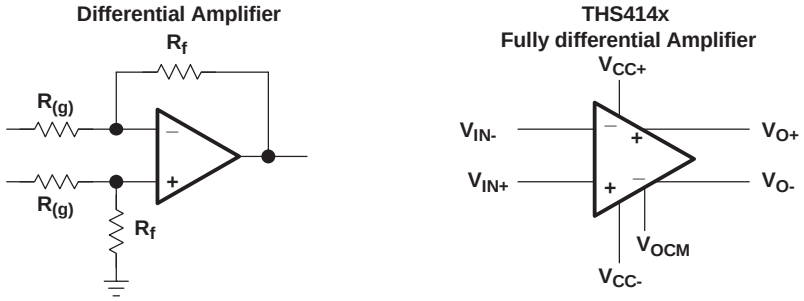


Figure 27. Differential Amplifier Versus a Fully Differential Amplifier

To understand the THS414x fully differential amplifiers, the definition for the pinouts of the amplifier are provided.

Input voltage definition $V_{ID} = (V_{I+}) - (V_{I-})$ $V_{IC} = \dfrac{(V_{I+}) + (V_{I-})}{2}$ (6)

Output voltage definition $V_{OD} = (V_{O+}) - (V_{O-})$ $V_{OC} = \dfrac{(V_{O+}) + (V_{O-})}{2}$ (7)

Transfer function $V_{OD} = V_{ID} \times A_{(f)}$ (8)

Output common mode voltage $V_{OC} = V_{OCM}$ (9)

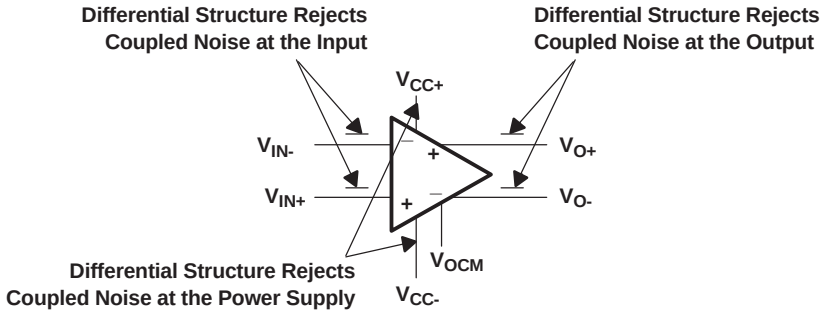
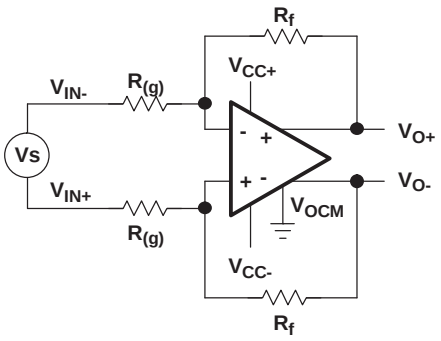


Figure 28. Definition of the Fully Differential Amplifier

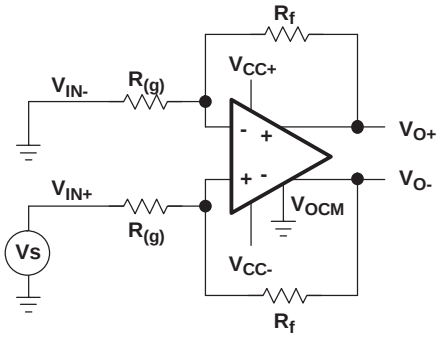
PRINCIPLES OF OPERATION (continued)

The following schematics depict the differences between the operation of the THS414x, fully differential amplifier, in two different modes. Fully differential amplifiers can work with differential input or can be implemented as single in/differential out.



Note: For proper operation, maintain symmetry by setting
$R_f1 = R_f2 = R_f$ and $R_{(g)}1 = R_{(g)}2 = R_{(g)}$
$\Rightarrow A = R_f/R_{(g)}$

Figure 29. Amplifying Differential Signals



RECOMMENDED RESISTOR VALUES

GAIN	$R_{(g)}$ Ω	R_f Ω
1	390	390
2	374	750
5	402	2010
10	402	4020

Figure 30. Single In With Differential Out

If each output is measured independently, each output is one-half of the input signal when gain is 1. The following equations express the transfer function for each output:

$$V_O = \frac{1}{2} V_I \quad (10)$$

The second output is equal and opposite in sign:

$$V_O = -\frac{1}{2} V_I \quad (11)$$

Fully differential amplifiers may be viewed as two inverting amplifiers. In this case, the equation of an inverting amplifier holds true for gain calculations. One advantage of fully differential amplifiers is that they offer twice as much dynamic range compared to single-ended amplifiers. For example, a 1-V_{PP} ADC can only support an input signal of 1 V_{PP}. If the output of the amplifier is 2 V_{PP}, then it will not be practical to feed a 2-V_{PP} signal into the targeted ADC. Using a fully differential amplifier enables the user to break down the output into two 1-V_{PP} signals with opposite signs and feed them into the differential input nodes of the ADC. In practice, the designer has been able to feed a 2-V peak-to-peak signal into a 1-V differential ADC with the help of a fully differential amplifier. The final result indicates twice as much dynamic range. Figure 31 illustrates the increase in dynamic range. The gain factor should be considered in this scenario. The THS414x fully differential amplifier offers an improved CMRR and PSRR due to its symmetrical input and output. Furthermore, second harmonic distortion is improved. Second harmonics tend to cancel because of the symmetrical output.

PRINCIPLES OF OPERATION (continued)

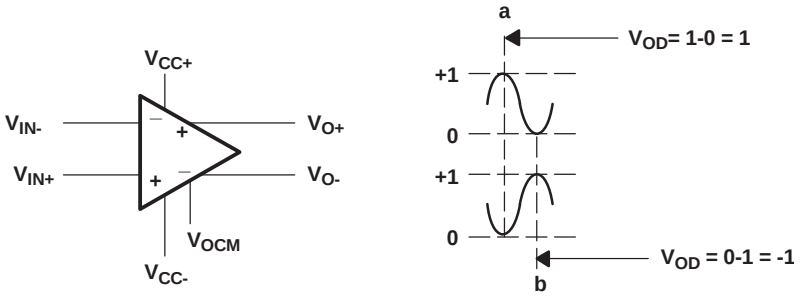


Figure 31. Fully Differential Amplifier With Two 1-V_{PP} Signals

Similar to the standard inverting amplifier configuration, input impedance of a fully differential amplifier is selected by the input resistor, $R_{(g)}$. If input impedance is a constraint in design, the designer may choose to implement the differential amplifier as an instrumentation amplifier. This configuration improves the input impedance of the fully differential amplifier. Figure 32 depicts the general format of instrumentation amplifiers.

The general transfer function for this circuit is:

$$\frac{V_{OD}}{V_{IN1} - V_{IN2}} = \frac{R_f}{R_{(g)}}\left(1 + \frac{2R2}{R1}\right) \quad (12)$$

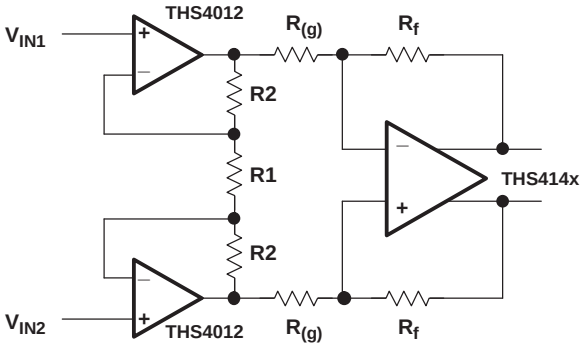


Figure 32. Instrumentation Amplifier

PRINCIPLES OF OPERATION (continued)

CIRCUIT LAYOUT CONSIDERATIONS

To achieve the levels of high frequency performance of the THS414x, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS414x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches (2,54 mm) between the device power terminals and the ceramic capacitors.
- Sockets—Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

PRINCIPLES OF OPERATION (continued)

POWER-DOWN MODE

The power-down mode is used when power saving is required. The power-down terminal ($\overline{PD}$) found on the THS414x is an active low terminal. If it is left as a no-connect terminal, the device will always stay on due to an internal 50 kΩ resistor to V_{CC}. The threshold voltage for this terminal is approximately 1.4 V above V_{CC-}. This means that if the $\overline{PD}$ terminal is 1.4 V above V_{CC-}, the device is active. If the $\overline{PD}$ terminal is less than 1.4 V above V_{CC-}, the device is off. For example, if V_{CC-} = –5 V, then the device is on when PD reaches 3.6 V, (–5 V + 1.4 V = –3.6 V). By the same calculation, the device is off below –3.6 V. It is recommended to pull the terminal to V_{CC-} in order to turn the device off. Figure 33 shows the simplified version of the power-down circuit. While in the power-down state, the amplifier goes into a high-impedance state. The amplifier output impedance is typically greater than 1 MΩ in the power-down state.

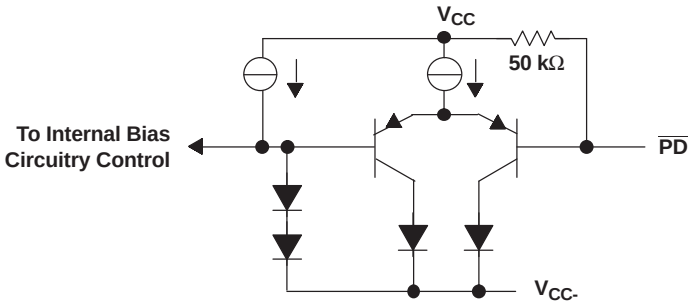


Figure 33. Simplified Power-Down Circuit

Due to the similarity of the standard inverting amplifier configuration, the output impedance appears to be very low while in the power-down state. This is because the feedback resistor (R_f) and the gain resistor ($R_{(g)}$) are still connected to the circuit. Therefore, a current path is allowed between the input of the amplifier and the output of the amplifier. An example of the closed-loop output impedance is shown in Figure 34.

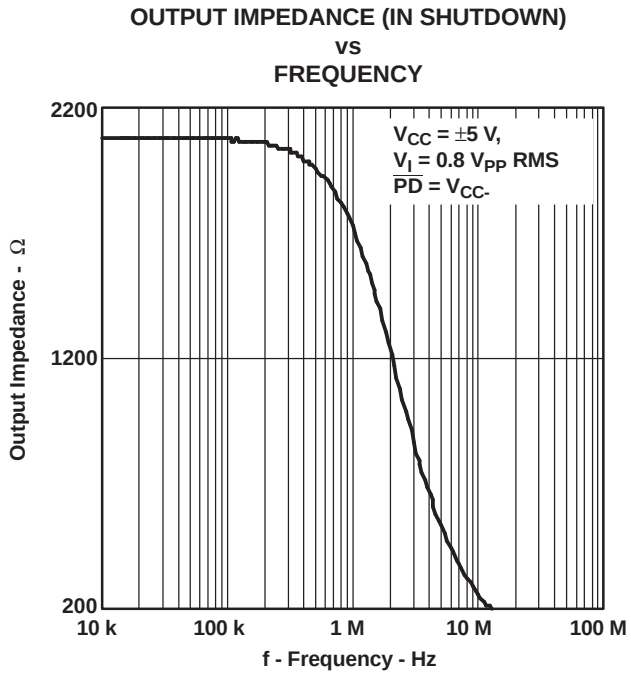


Figure 34.

PRINCIPLES OF OPERATION (continued)

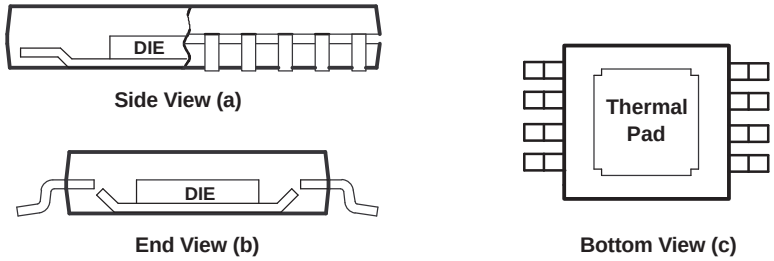
GENERAL PowerPAD DESIGN CONSIDERATIONS

The THS414x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 35(a) and Figure 35(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 35(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the, heretofore, awkward mechanical methods of heatsinking.

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package (SLMA002).* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.



A. The thermal pad is electrically isolated from all terminals in the package.

Figure 35. Views of Thermally Enhanced DGN Package

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4140CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4140C	Samples
THS4140CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AOF	Samples
THS4140ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4140I	Samples
THS4140IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4140I	Samples
THS4140IDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASQ	Samples
THS4140IDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOG	Samples
THS4140IDGNG4	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOG	Samples
THS4140IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AOG	Samples
THS4141CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4141C	Samples
THS4141CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AOI	Samples
THS4141CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AOI	Samples
THS4141ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4141I	Samples
THS4141IDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASR	Samples
THS4141IDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOK	Samples
THS4141IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

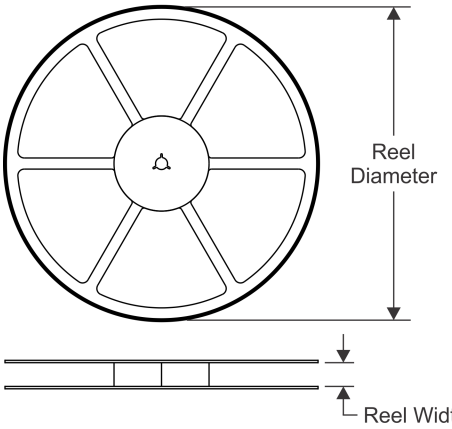
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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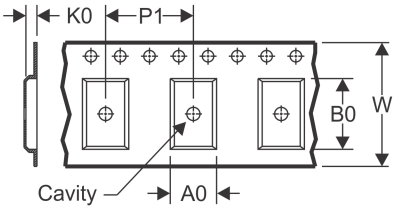
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

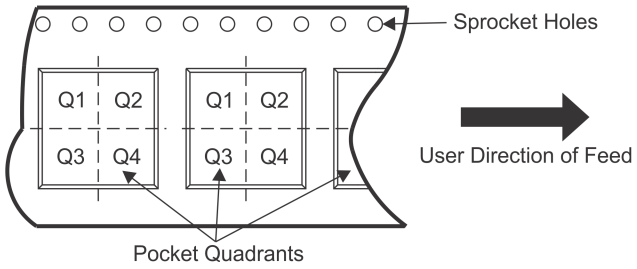


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

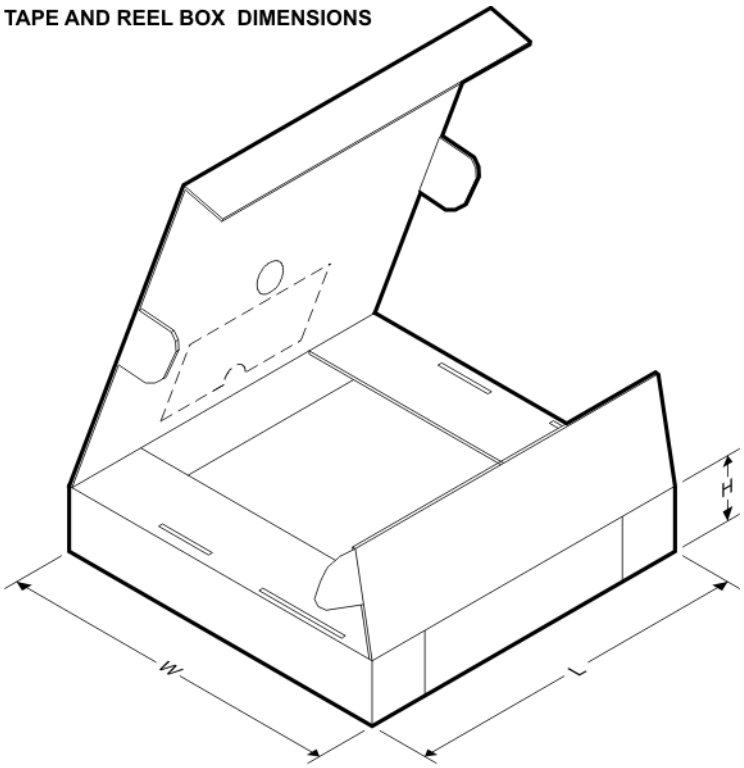
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4140IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4141CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4141IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

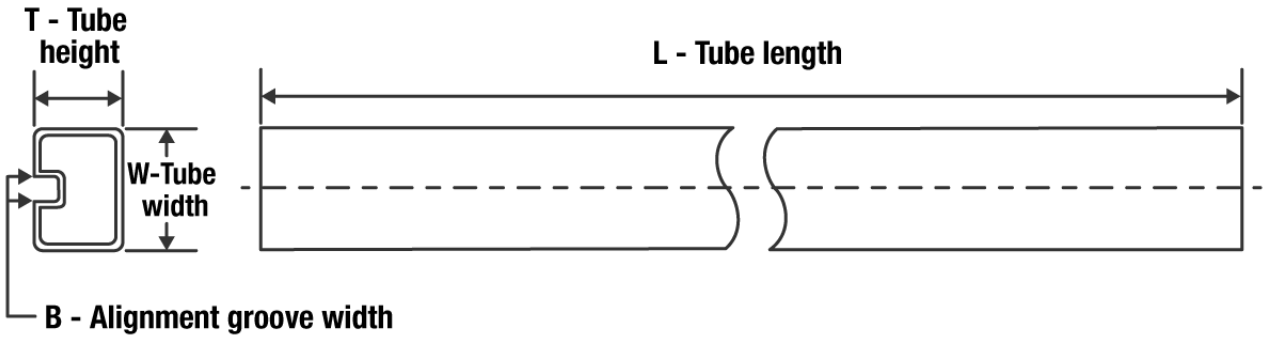
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4140IDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS4141CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4141IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS4140CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4140ID	D	SOIC	8	75	505.46	6.76	3810	4
THS4140IDG4	D	SOIC	8	75	505.46	6.76	3810	4
THS4140IDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS4140IDGNG4	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS4141CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4141ID	D	SOIC	8	75	505.46	6.76	3810	4

GENERIC PACKAGE VIEW

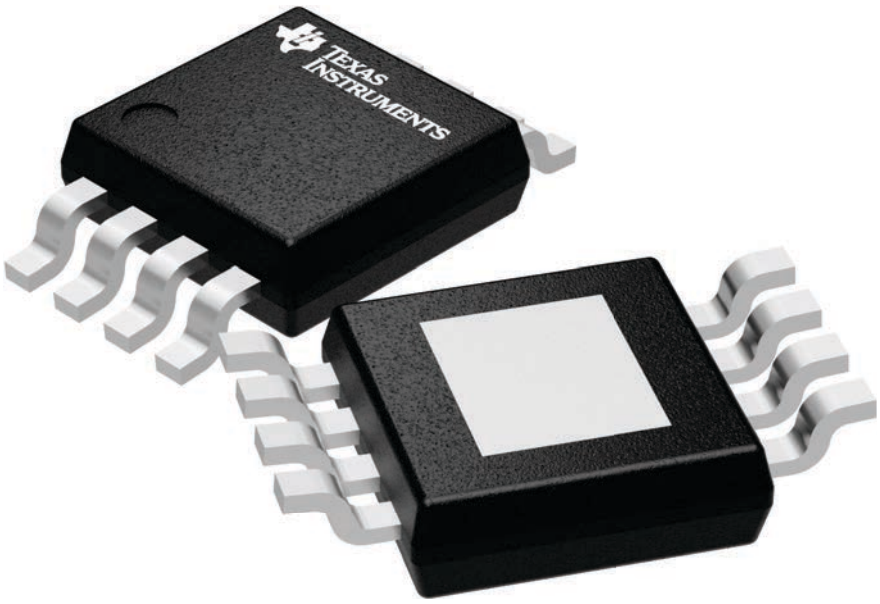
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

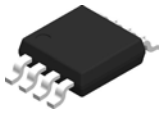
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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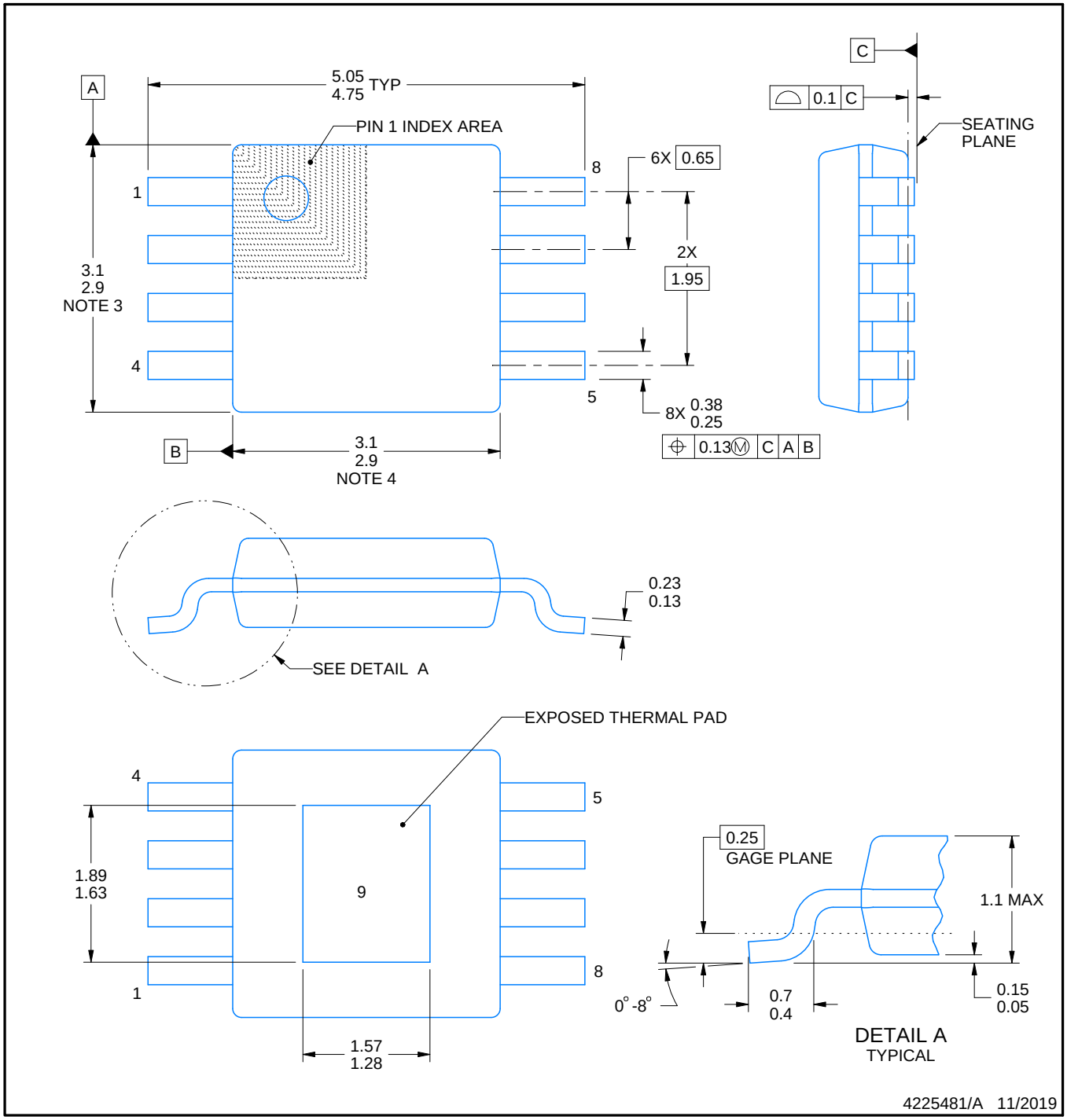
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

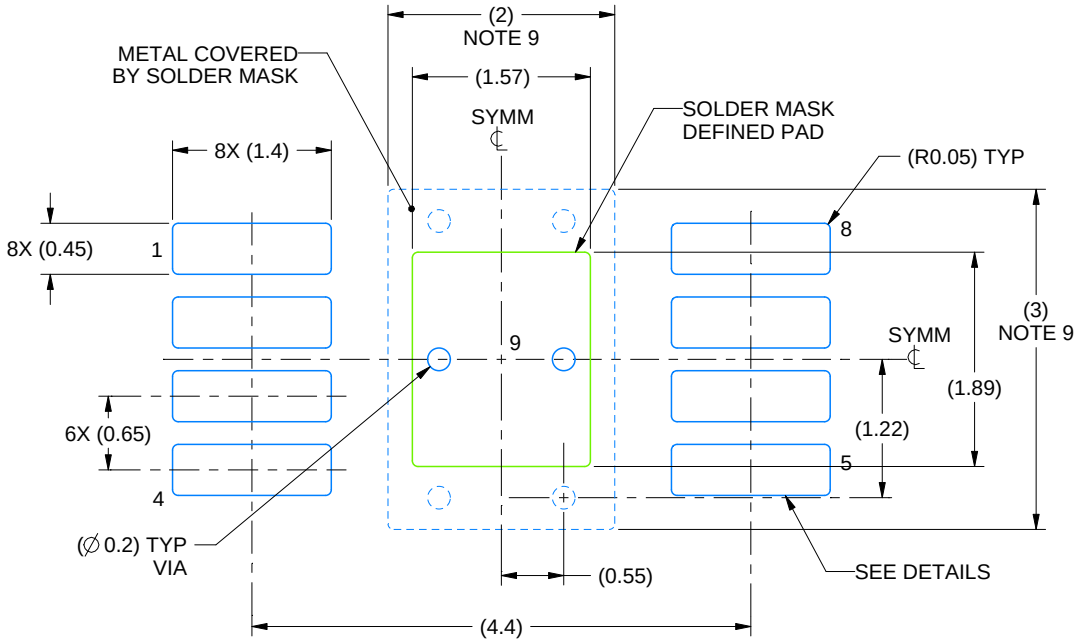
SMALL OUTLINE PACKAGE



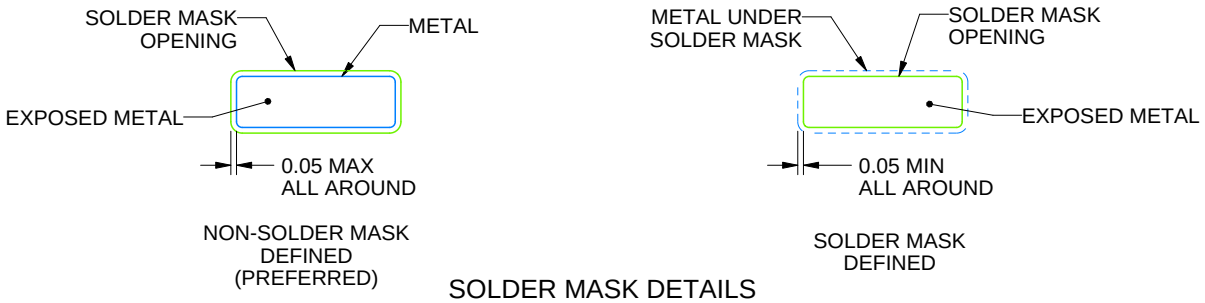
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

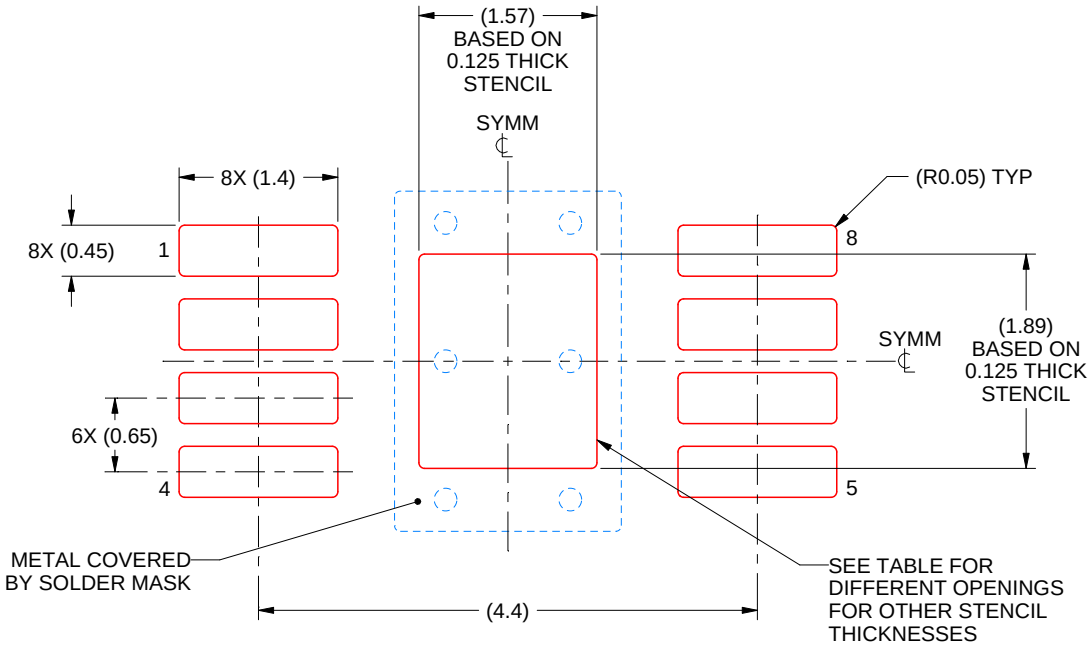


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

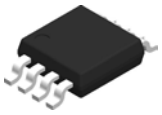
4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

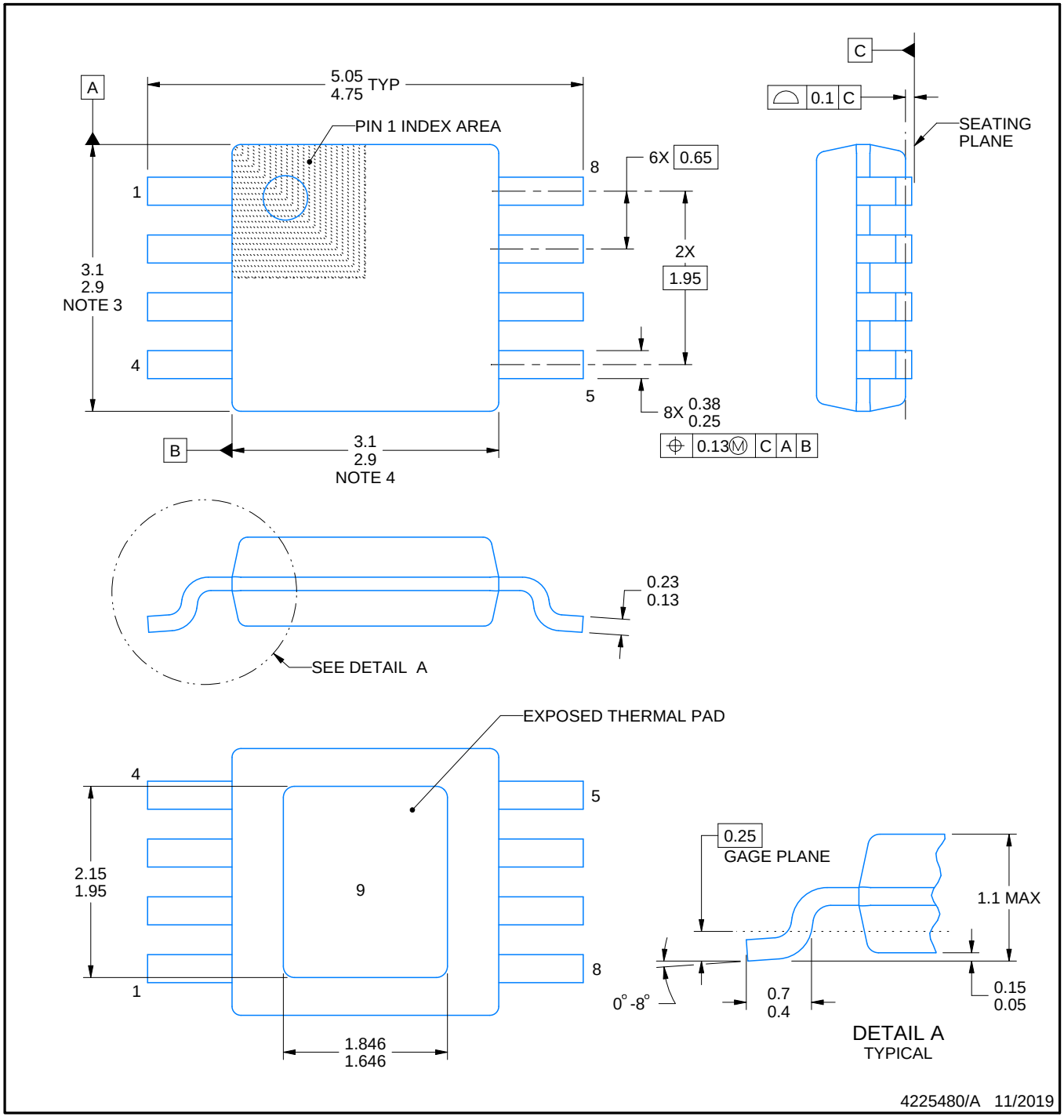
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

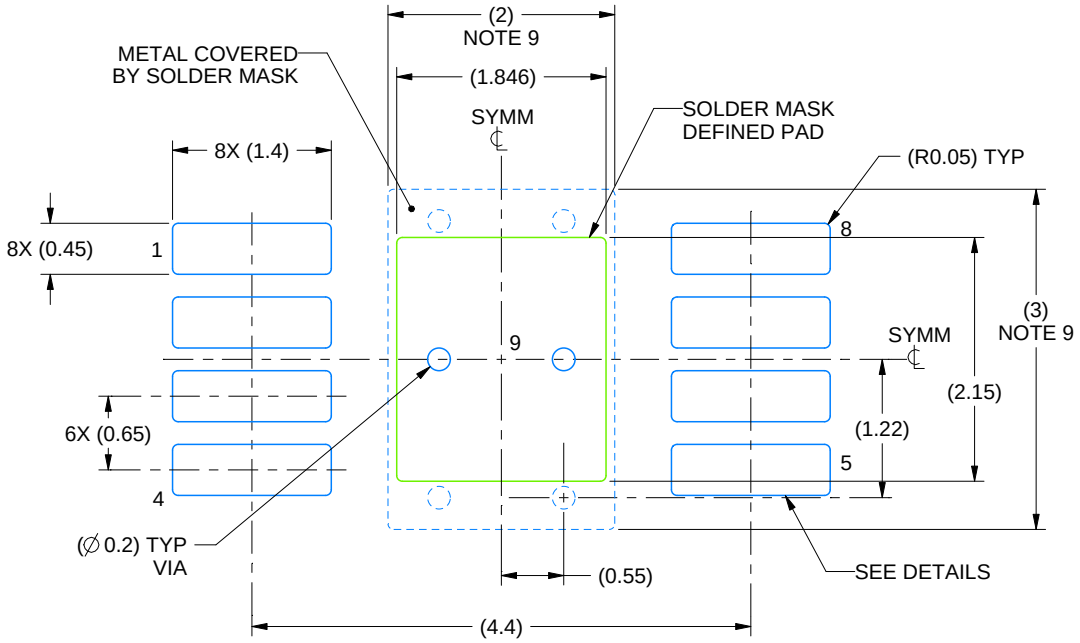
SMALL OUTLINE PACKAGE



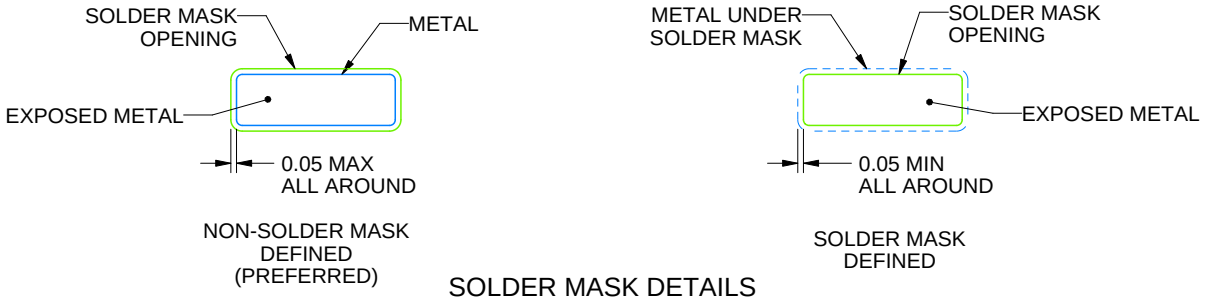
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

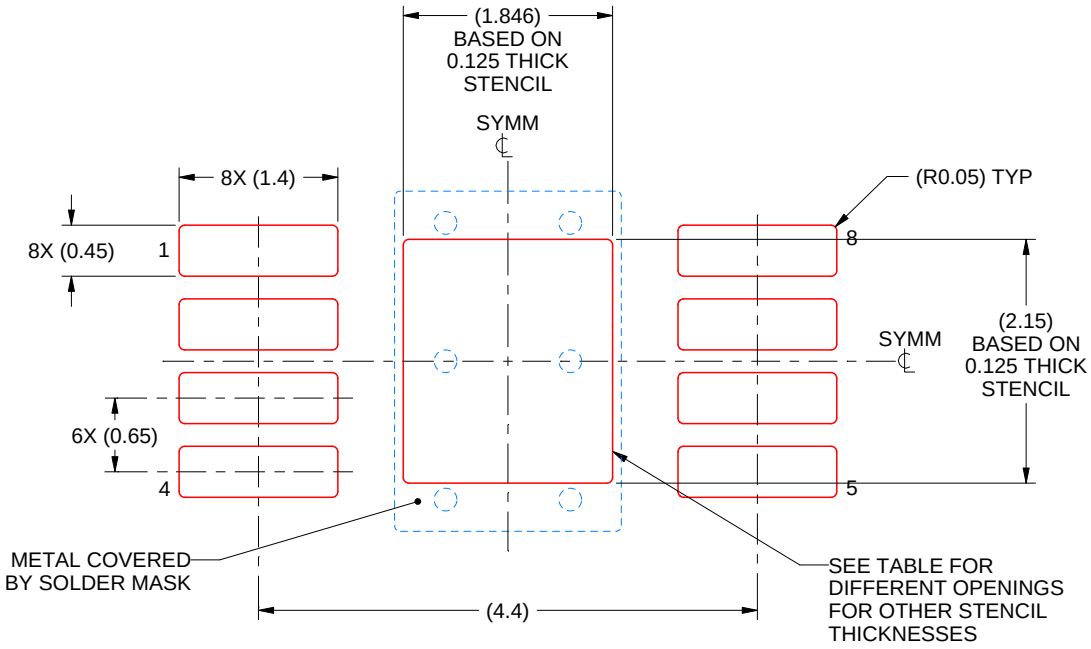


SOLDER MASK DETAILS

4225480/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



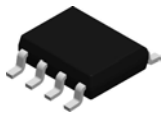
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.06 X 2.40
0.125	1.846 X 2.15 (SHOWN)
0.15	1.69 X 1.96
0.175	1.56 X 1.82

4225480/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

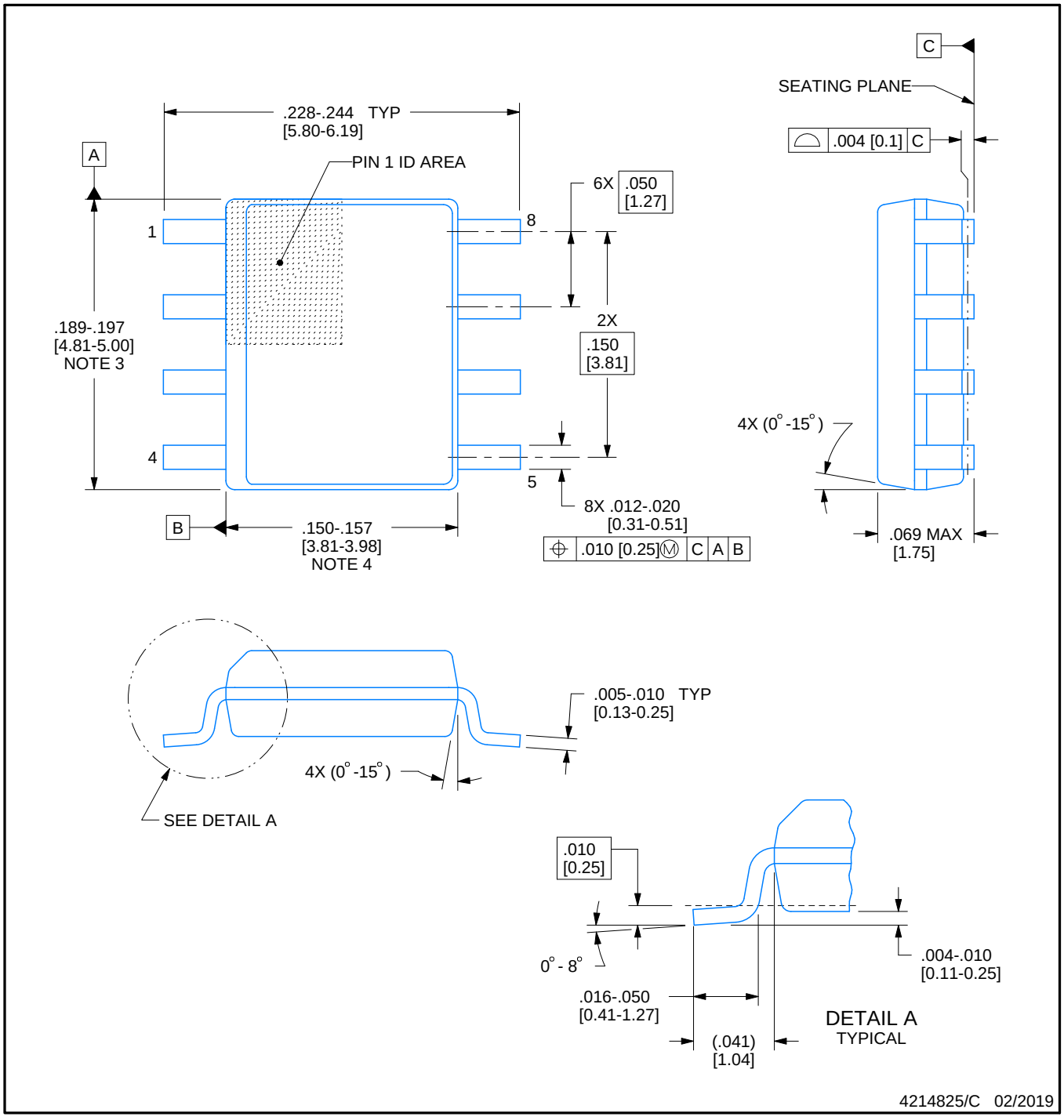


PACKAGE OUTLINE

D0008A

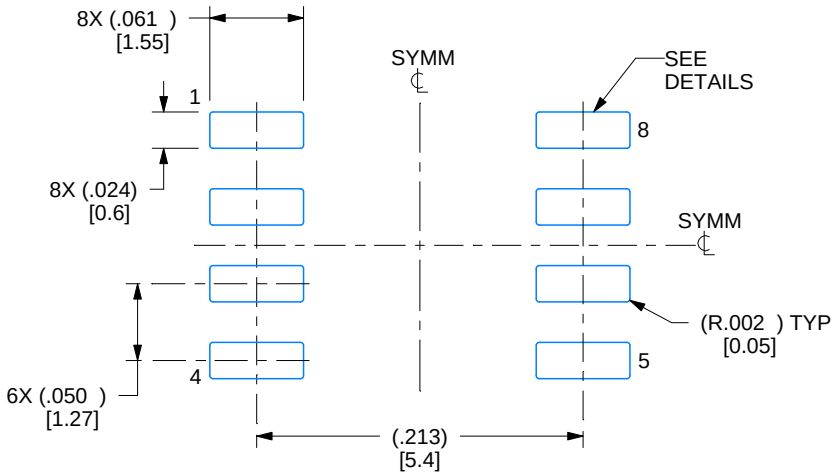
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

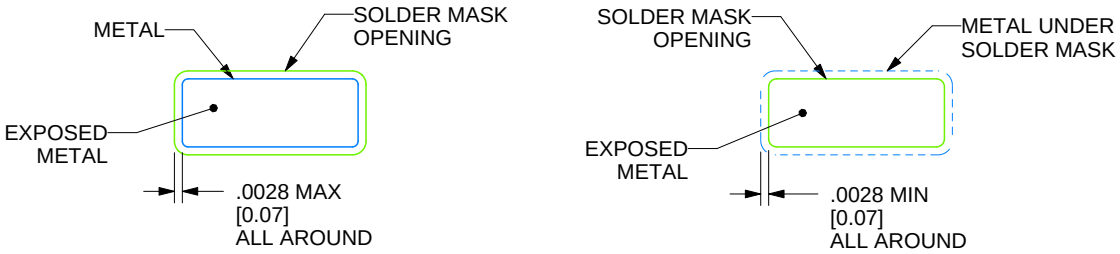


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

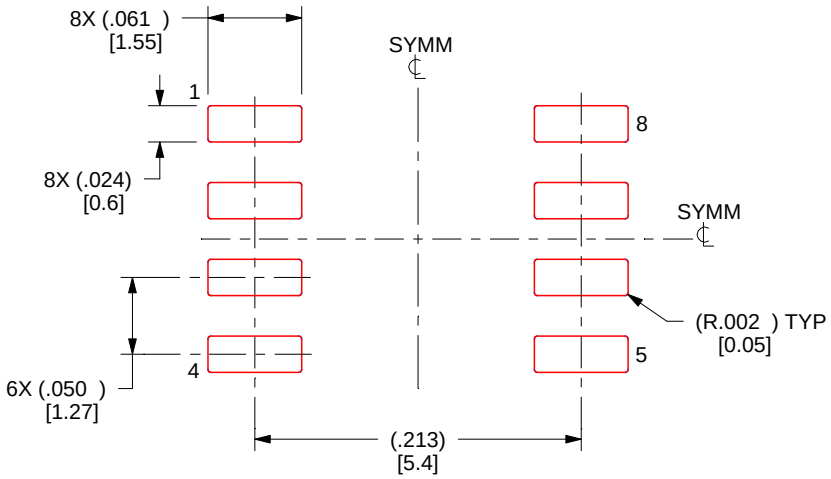
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



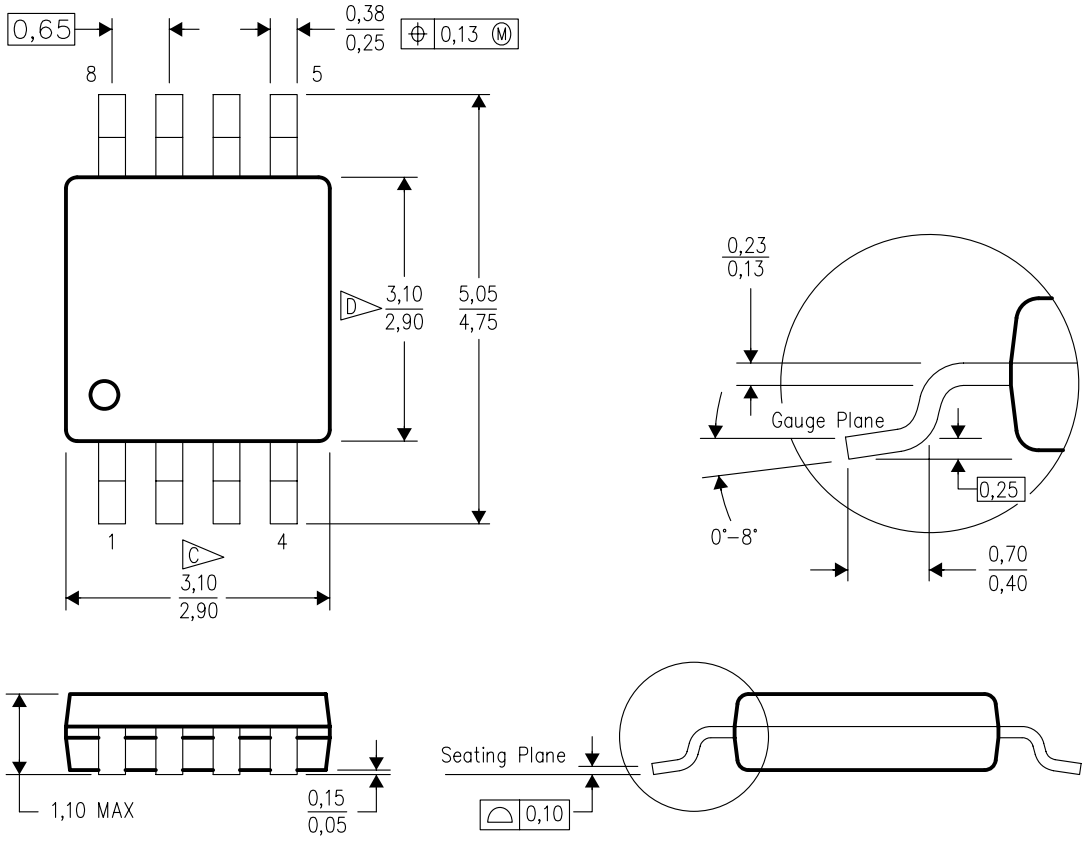
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

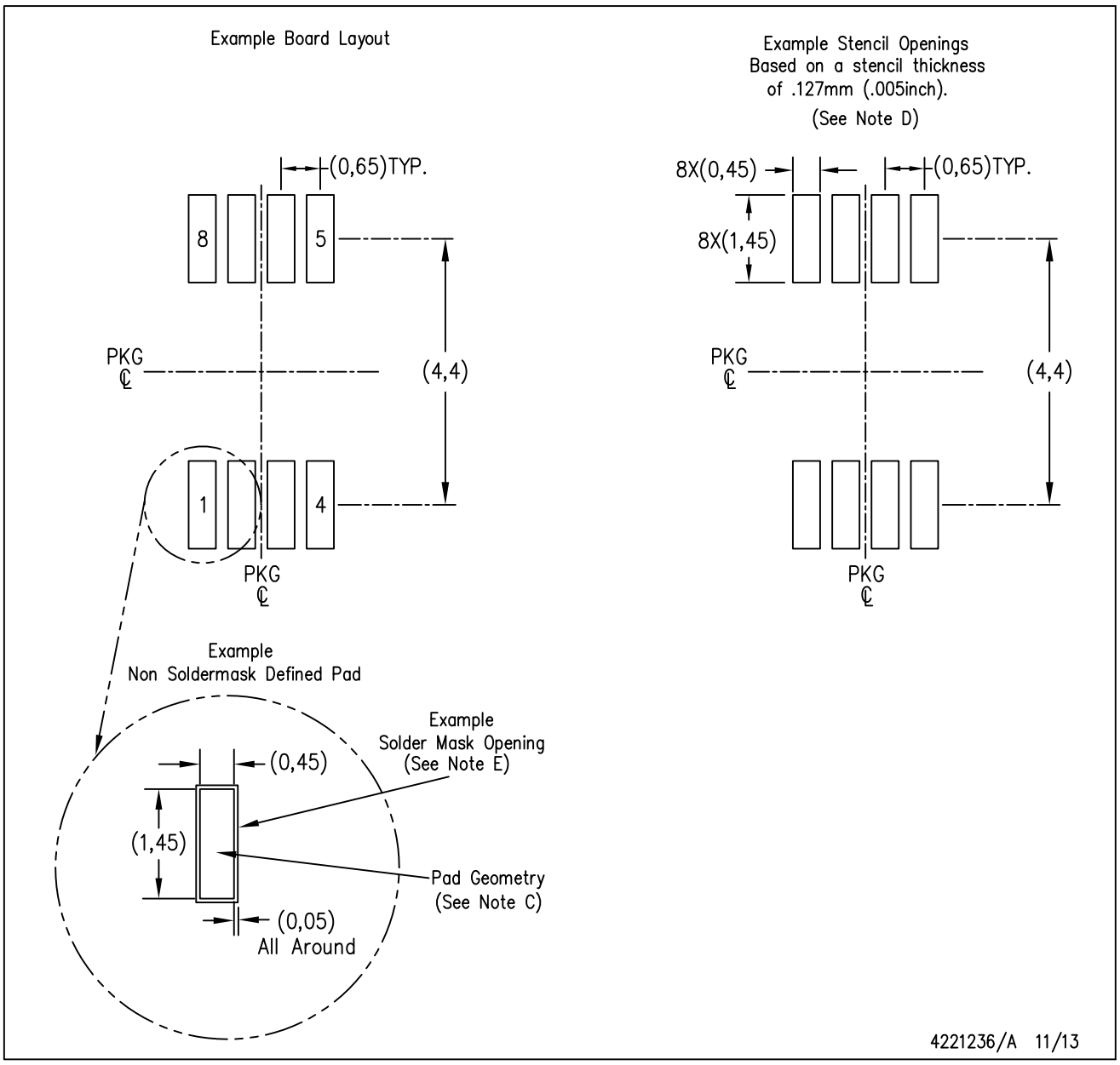
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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