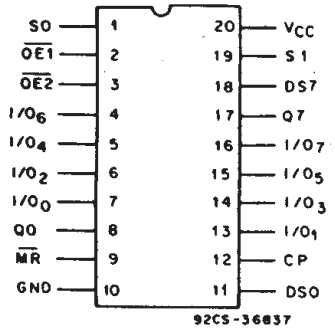
CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS288



TERMINAL ASSIGNMENT

8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

CD54/74AC/ACT299 - Asynchronous Reset
CD54/74AC/ACT323 - Synchronous Reset

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  6 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF

The RCA CD54/74AC299 and CD54/74AC323 and the CD54/74ACT299 and CD54/74ACT323 are 3-state, 8-input universal shift/storage registers with common parallel I/O pins. These devices use the RCA ADVANCED CMOS technology. These registers have four synchronous-operating modes controlled by the two select inputs as shown in the Mode Select (S0, S1) table. The Mode Select, the Serial Data (DSO, DS7), and the Parallel Data (I/O_0 - I/O_7) respond only to the LOW-TO-HIGH transition of the clock (CP) pulse. S0, S1 and Data inputs must be present one setup time prior to the positive transition of the clock.

With the CD54/74AC/ACT299, the Master Reset ($\overline{MR}$) is an asynchronous active-LOW input. When $\overline{MR}$ is LOW, the register is cleared regardless of the status of all other inputs. With the CD54/74AC/ACT323, the Master Reset ($\overline{MR}$) clears the register in sync with the clock input. The register can be expanded by cascading same units by tying the serial output (QO) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DSO) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DSO of the first stage.

The 3-state input/output (I/O) port has three modes of operation:

1. Both Output Enable ($\overline{OE1}$ and $\overline{OE2}$) inputs are LOW and S0 or S1 or both are LOW; the data in the register is present at the eight outputs.
2. When both S0 and S1 are HIGH, I/O terminals are in the high-impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of $\overline{OE1}$ and $\overline{OE2}$.
3. Either one of the two Output Enable inputs being HIGH will force I/O terminals to be in the off state. It is noted that each I/O terminal is a 3-state output and a CMOS buffer input.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

The CD74AC/ACT299 and CD74AC/ACT323 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT299 and CD54AC/ACT323, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

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File Number 1958

This data sheet is applicable to the CD54/74AC299, CD74AC323, CD54/74ACT299, and CD54ACT323. The CD54AC323 and CD74ACT323 were not acquired from Harris Semiconductor.

CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

MODE SELECT — FUNCTION TABLE
REGISTER OPERATING MODES

FUNCTION	INPUTS							REGISTER OUTPUTS				
	$\overline{MR}$	CP	S0	S1	DS0	DS7	I/O_n	Q0	Q1	...	Q6	Q7
Reset (Clear)	L	X*	X	X	X	X	X	L	L	...	L	L
Shift Right	H	⎍	h	l	l	X	X	L	q_0	...	q_5	q_6
	H	⎍	h	l	h	X	X	H	q_0	...	q_5	q_6
Shift Left	H	⎍	l	h	X	l	X	q_1	q_2	...	q_7	L
	H	⎍	l	h	X	h	X	q_1	q_2	...	q_7	H
Hold (do nothing)	H	⎍	l	l	X	X	X	q_0	q_1	...	q_6	q_7
Parallel Load	H	⎍	h	h	X	X	l	L	L	...	L	L
	H	⎍	h	h	X	X	h	H	H	...	H	H

*On CD54/74AC/ACT323, CP must be in transition from the LOW-to-HIGH state to Reset (Clear).

MODE SELECT — FUNCTION TABLE
3-STATE I/O PORT OPERATING MODE

FUNCTION	INPUTS					INPUTS/OUTPUTS
	$\overline{OE1}$	$\overline{OE2}$	S0	S1	Qn (Register)	$I/O_0 \ldots I/O_7$
Read Register	L	L	L	X	L	L
	L	L	L	X	H	H
	L	L	X	L	L	L
	L	L	X	L	H	H
Load Register	X	X	H	H	$Qn = I/O_n$	I/O_n = Inputs
Disable I/O	H	X	X	X	X	(Z)
	X	H	X	X	X	(Z)

H = Input voltage high level.
h = Input voltage high one set-up time prior clock transition.
L = Input voltage low level.
l = Input voltage low one set-up time prior clock transition.
q_n = Lower case letters indicate the state of the referenced output one set-up time prior clock transition.
X = Voltage level on logic status don't care.
Z = Output in high-impedance state.
⎍ = Low-to-high clock transition.

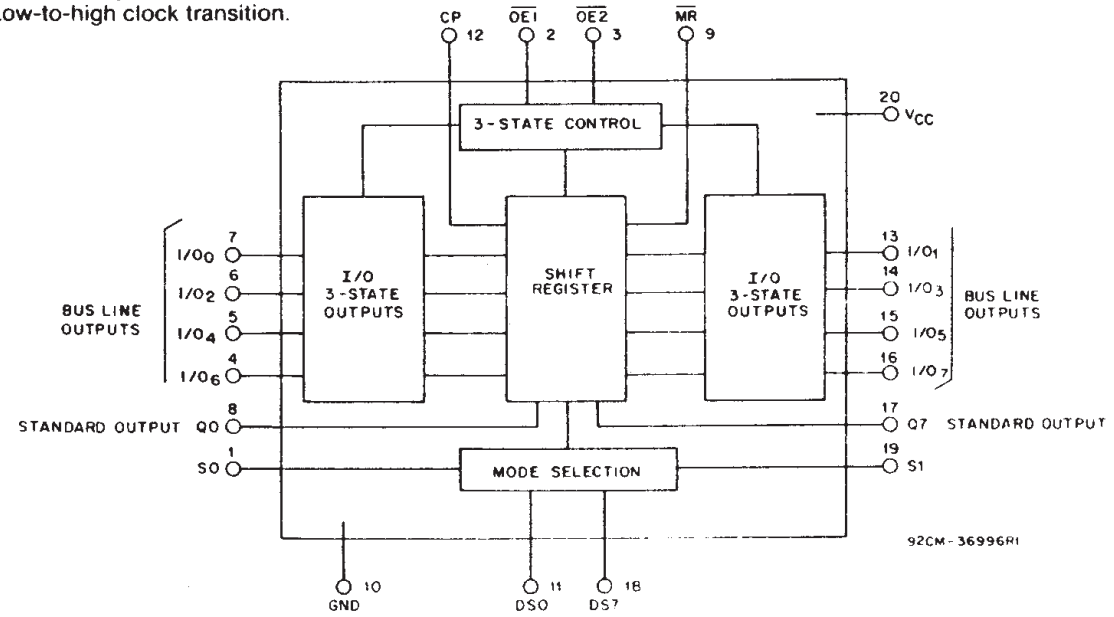


Fig. 1 - Functional diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
	#, *	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
	#, *	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-Stage Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O= V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*	
	299	323
S1, S0, $\overline{OE1}$, $\overline{OE2}$	0.83	0.83
I/O_0 - I/O_7, CP, DS0, DS7	0.67	0.67
$\overline{MR}$	1.33	0.67

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Setup Time S1, S0, to CP	t_{SU}	1.5	99	—	113	—	ns
		3.3*	11.1	—	12.6	—	
		5†	7.9	—	9	—	
Hold Time S1, S0 to CP	t_H	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	
Setup Time (I/O)n, DS0, DS7 to CP	t_{SU}	1.5	49	—	56	—	ns
		3.3	5.5	—	6.3	—	
		5	3.9	—	4.5	—	
Hold Time (I/O)n, DS0, DS7 to CP	t_{SU}	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	
Setup Time $\overline{MR}$ to CP (323)	t_{SU}	1.5	61	—	69	—	ns
		3.3	6.8	—	7.8	—	
		5	4.8	—	5.5	—	
Hold Time $\overline{MR}$ to CP (323)	t_H	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	
Maximum CP Frequency	f_{MAX}	1.5	9	—	8	—	MHz
		3.3	78	—	68	—	
		5	108	—	95	—	
CP Pulse Width	t_W	1.5	57	—	65	—	ns
		3.3	6.4	—	7.3	—	
		5	4.6	—	5.2	—	
$\overline{MR}$ Pulse Width	t_W	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	
Recovery Time $\overline{MR}$ to CP 299	t_{REC}	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	

*3.3 V: min. is @ 3 V
†5 V: min is @ 4.5 V

CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q0, Q7	t_{PLH}	1.5	—	147	—	162	ns
	t_{PHL}	3.3*	4.7	16.5	4.5	18.1	
		5†	3.3	11.7	3.2	12.9	
CP to (I/O)n	t_{PLH}	1.5	—	154	—	169	ns
	t_{PHL}	3.3	4.9	17.2	4.7	18.9	
		5	3.5	12.3	3.4	13.5	
$\overline{MR}$ to Q0, Q7 (299 only)	t_{PLH}	1.5	—	127	—	140	ns
	t_{PHL}	3.3	4	14.3	3.9	15.7	
		5	2.9	10.2	2.8	11.2	
$\overline{MR}$ to (I/O)n	t_{PLH}	1.5	—	158	—	174	ns
	t_{PHL}	3.3	5	17.7	4.9	19.5	
		5	3.6	12.6	3.5	13.9	
Enable and Disable Times	t_{PZL}	1.5	—	169	—	186	ns
	t_{PZH}	3.3	5.8	20.4	5.6	22.4	
	t_{PLZ}	5	3.8	13.5	3.7	14.9	
	t_{PHZ}						
Power Dissipation Capacitance	C_{PD}§	—	280 Typ.		280 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per function.
$P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Setup Time S1, S0 to CP	t_{SU}	5*	7.9	—	9	—	ns
Hold Time S1, S0 to CP	t_H	5	0	—	0	—	ns
Setup Time (I/O)n, DS0, DS7 to CP	t_{SU}	5	3.9	—	4.5	—	ns
Hold Time (I/O)n, DS0, DS7 to CP	t_H	5	0	—	0	—	ns
Setup Time $\overline{MR}$ to CP (323)	t_{SU}	5*	4.8	—	5.5	—	ns
Hold Time $\overline{MR}$ to CP (323)	t_H	5	0	—	0	—	ns
Maximum CP Frequency	f_{max}	5	103	—	90	—	MHz
CP Pulse Width	t_w	5	4.8	—	5.5	—	ns
$\overline{MR}$ Pulse Width	t_w	5	4.4	—	5	—	ns
Recovery Time $\overline{MR}$ to CP (299)	t_{REC}	5	4.4	—	5	—	ns

*5 V: min. is @ 4.5 V

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CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q0, Q7	t_{PLH} t_{PHL}	5*	3.3	11.7	3.2	12.9	ns
CP to (I/O)n	t_{PLH} t_{PHL}	5	3.7	13.2	3.6	14.5	ns
$\overline{MR}$ to Q0, Q7 (299 only)	t_{PLH} t_{PHL}	5	3.1	11.1	3.1	12.2	ns
$\overline{MR}$ to (I/O)n	t_{PLH} t_{PHL}	5	4.8	16.9	4.7	18.6	ns
Enable and Disable Times	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	5	3.8	13.5	3.7	14.9	ns
Power Dissipation Capacitance	C_{PD}§	—	280 Typ.		280 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per function.
$P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC}\Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

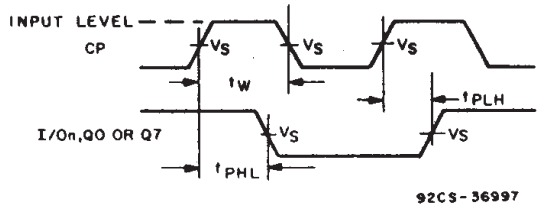


Fig. 2 - Clock prerequisite and propagation delays.

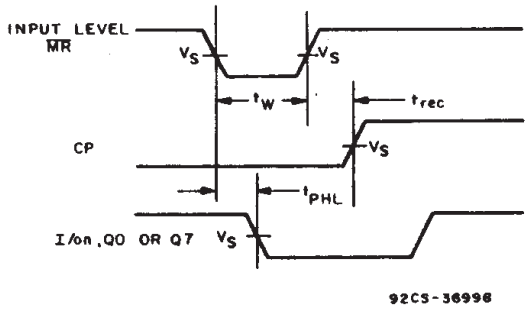


Fig. 3 - Master Reset prerequisite and propagation delays.

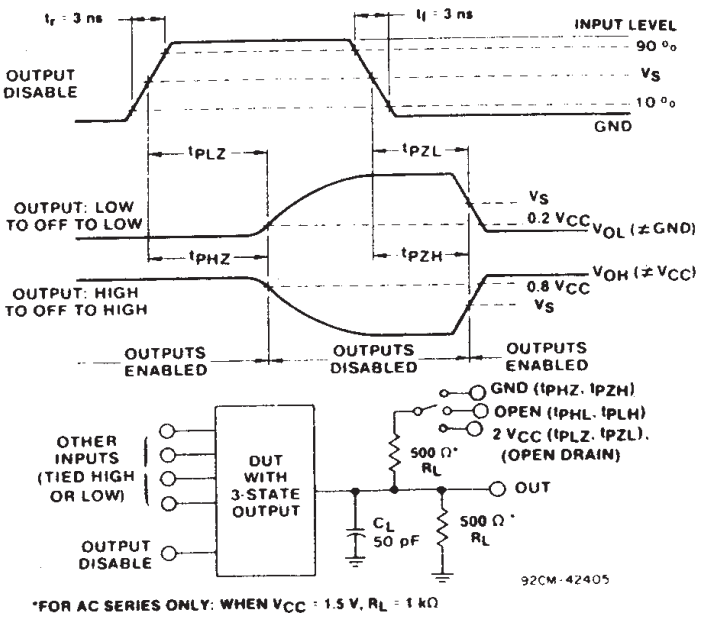


Fig. 4 - Three-state propagation delay times and test circuit.

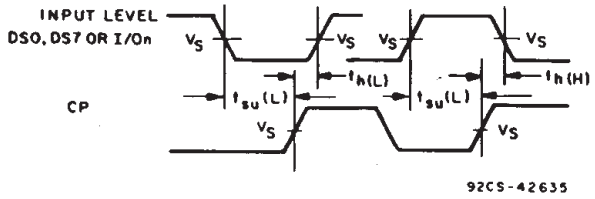


Fig. 5 - Data prerequisite times.

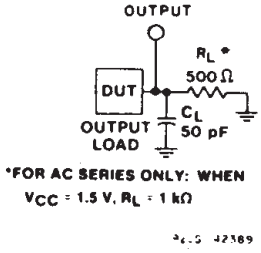


Fig. 6 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54AC299F3A	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54AC299F3A	Samples
CD54ACT299F3A	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54ACT299F3A	Samples
CD74AC299M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC299M	Samples
CD74AC323M	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC323M	Samples
CD74ACT299M	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT299M	Samples
CD74ACT299M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT299M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54AC299, CD54ACT299, CD74AC299, CD74ACT299 :

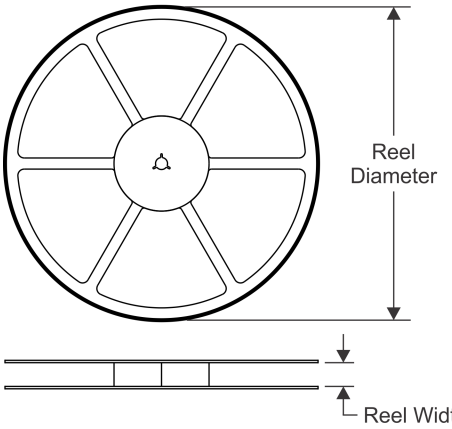
- Catalog : CD74AC299, CD74ACT299
- Military : CD54AC299, CD54ACT299

NOTE: Qualified Version Definitions:

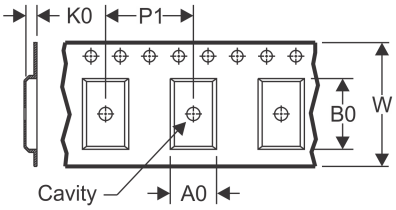
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

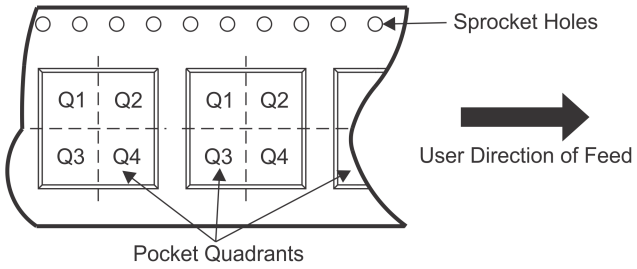


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

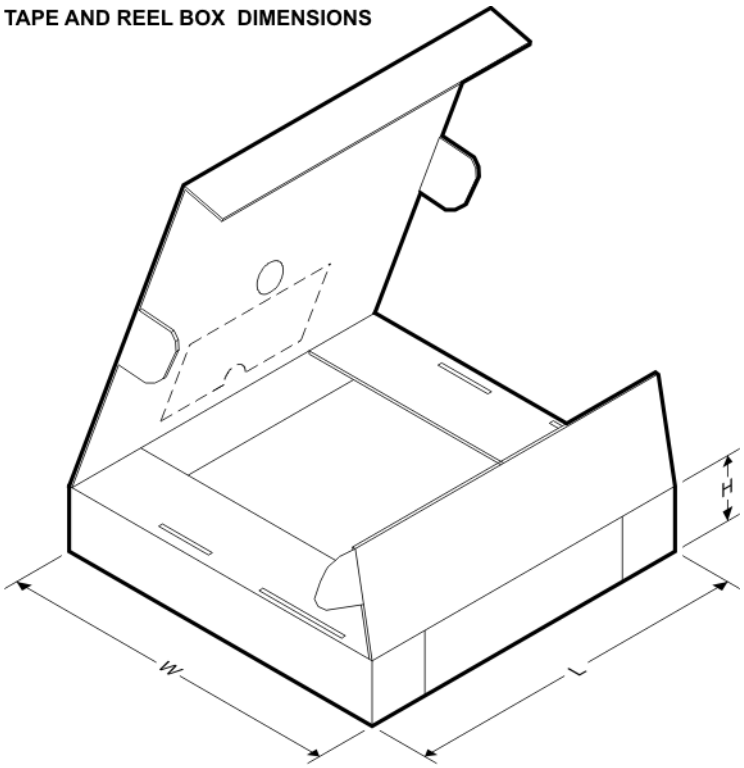
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC299M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74ACT299M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

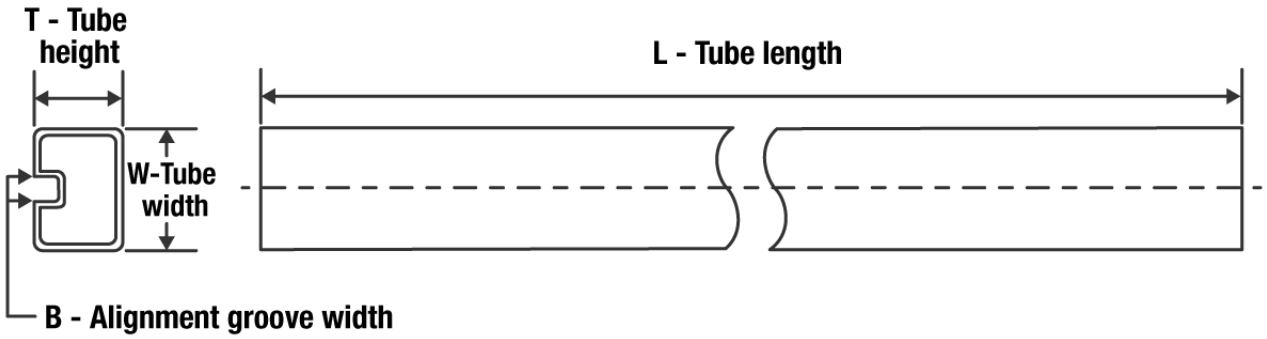
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC299M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74ACT299M96	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE



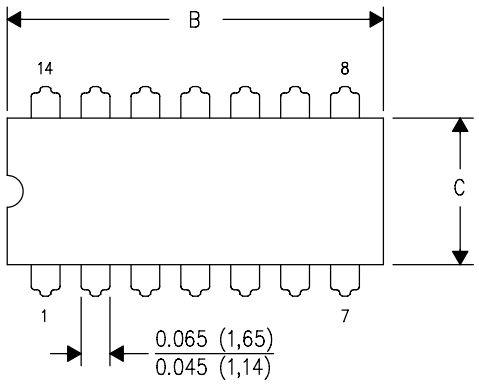
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74AC323M	DW	SOIC	20	25	507	12.83	5080	6.6
CD74ACT299M	DW	SOIC	20	25	507	12.83	5080	6.6

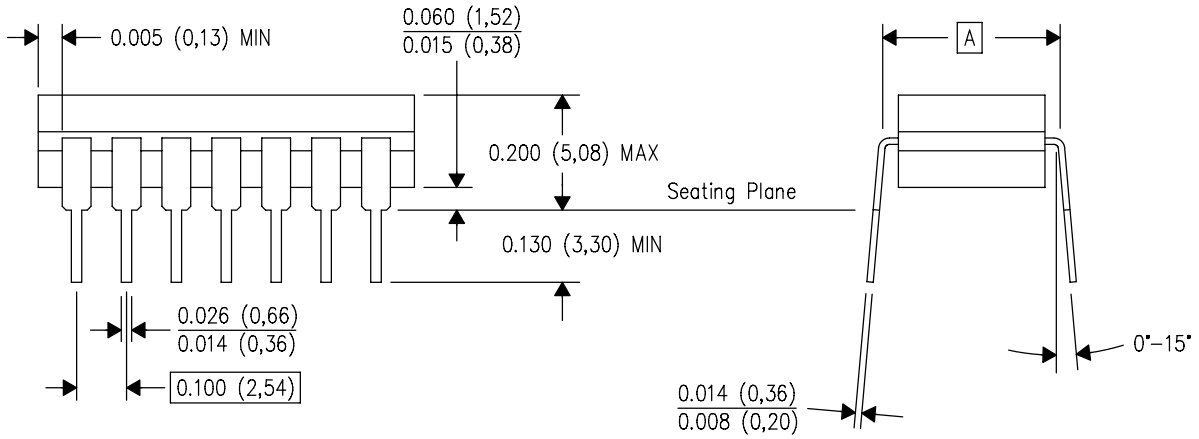
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE

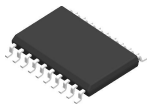


DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

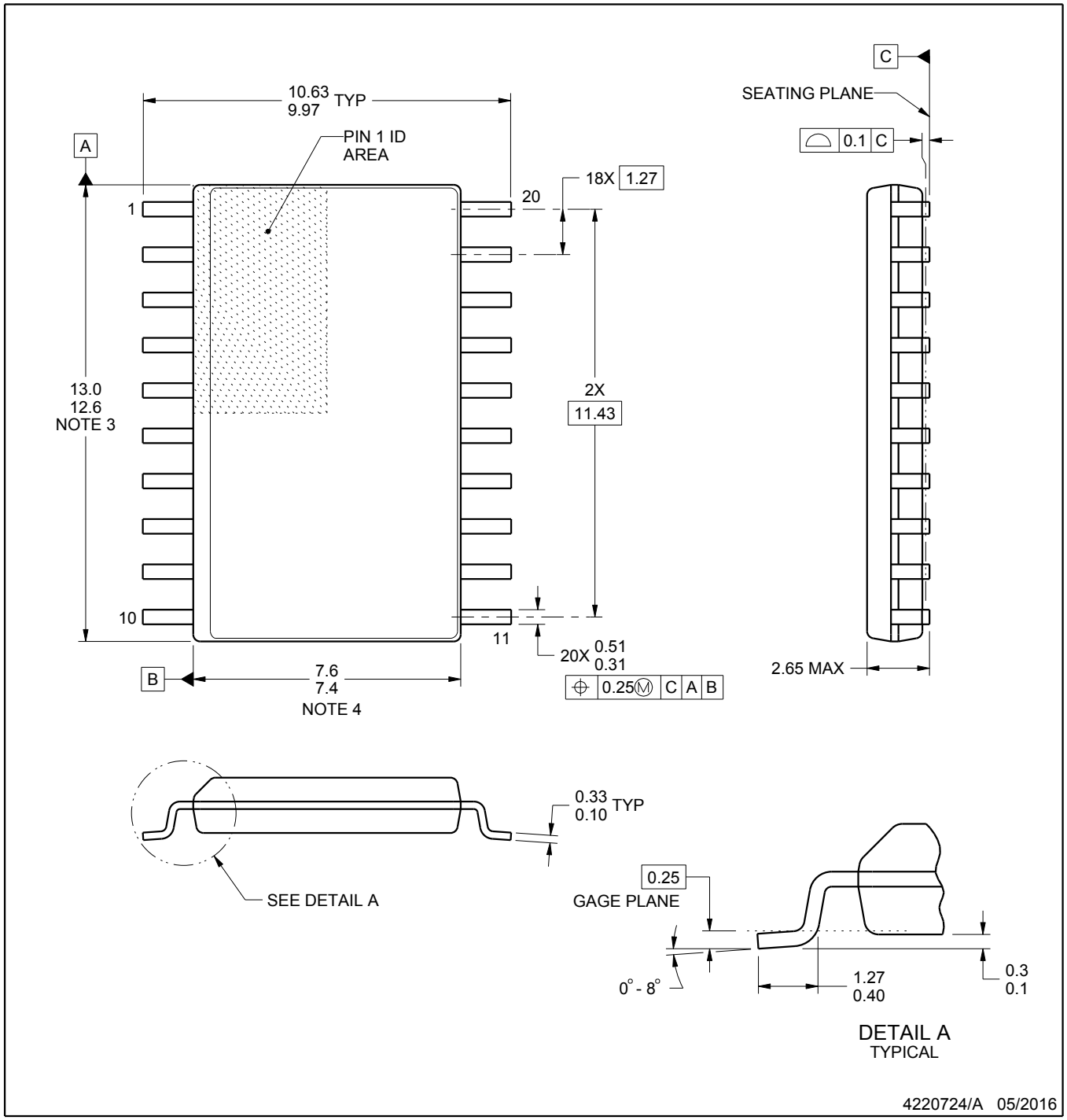


PACKAGE OUTLINE

DW0020A

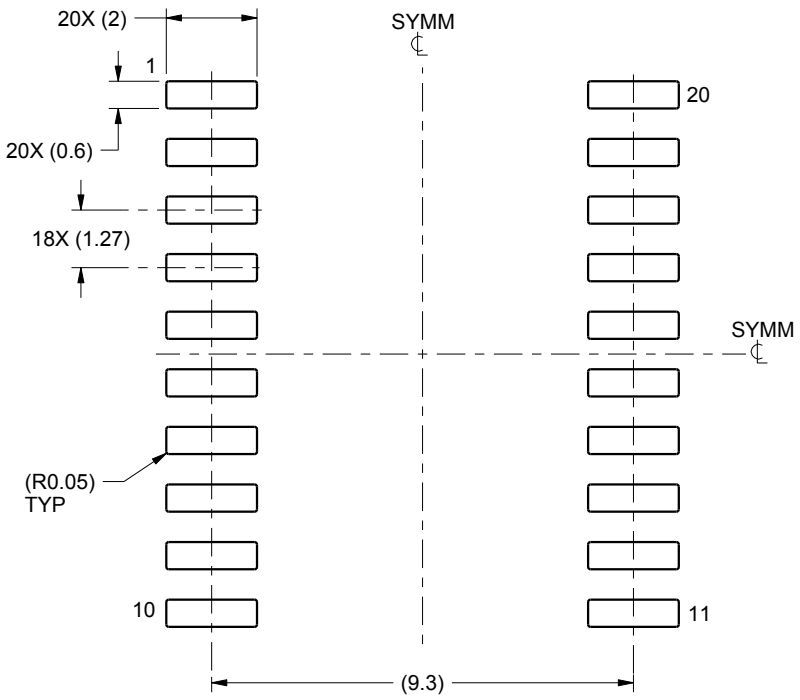
SOIC - 2.65 mm max height

SOIC

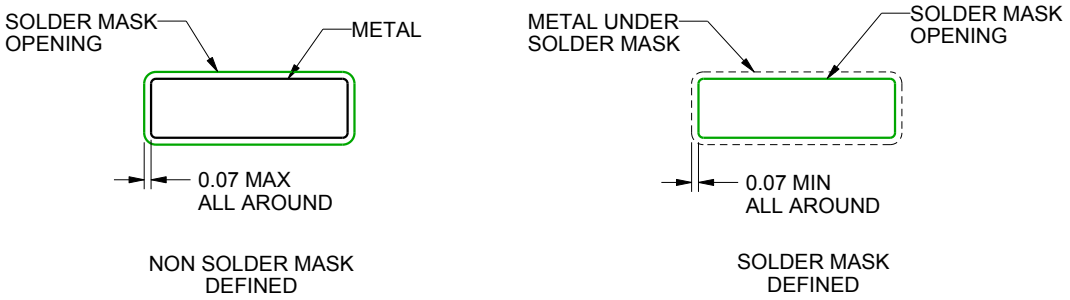


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

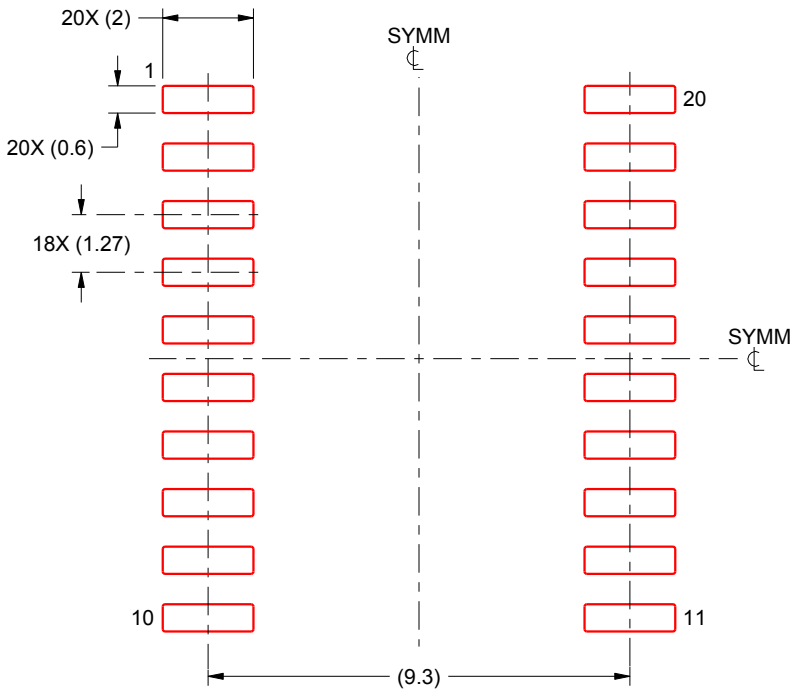


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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