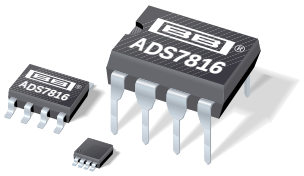
BURR-BROWN®



ADS7816

12-Bit High Speed Micro Power Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **200kHz SAMPLING RATE**
- **MICRO POWER:**
  1.9mW at 200kHz
  150μW at 12.5kHz
- **POWER DOWN: 3μA Max**
- **8-PIN MINI-DIP, SOIC, AND MSOP**
- **DIFFERENTIAL INPUT**
- **SERIAL INTERFACE**

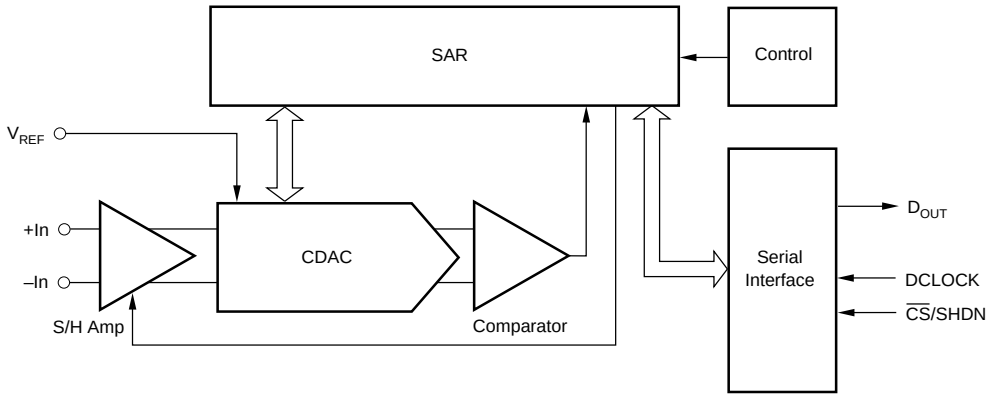
APPLICATIONS

- **BATTERY OPERATED SYSTEMS**
- **REMOTE DATA ACQUISITION**
- **ISOLATED DATA ACQUISITION**

DESCRIPTION

The ADS7816 is a 12-bit, 200kHz sampling analog-to-digital converter. It features low power operation with automatic power down, a synchronous serial interface, and a differential input. The reference voltage can be varied from 100mV to 5V, with a corresponding resolution from 24μV to 1.22mV.

Low power, automatic power down, and small size make the ADS7816 ideal for battery operated systems or for systems where a large number of signals must be acquired simultaneously. It is also ideal for remote and/or isolated data acquisition. The ADS7816 is available in an 8-pin plastic mini-DIP, an 8-lead SOIC, or an 8-lead MSOP package.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

At –40°C to +85°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, f_{CLK} = 16 • f_{SAMPLE}, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7816 MIN	ADS7816 TYP	ADS7816 MAX	ADS7816B MIN	ADS7816B TYP	ADS7816B MAX	ADS7816C MIN	ADS7816C TYP	ADS7816C MAX	UNITS
ANALOG INPUT											
Full-Scale Input Span	+In – (–In)	0		V_{REF}	*		*	*		*	V
Absolute Input Voltage	+In	–0.2		V_{CC} +0.2	*		*	*		*	V
	–In	–0.2		+0.2	*		*	*		*	V
Capacitance			25			*			*		pF
Leakage Current			±1			*			*		µA
SYSTEM PERFORMANCE											
Resolution			12			*			*		Bits
No Missing Codes		11			12			*			Bits
Integral Linearity Error			±0.5	±2		±0.5	±2		±0.5	±1	LSB[1]
Differential Linearity Error			±0.5	±2		±0.5	±1		±0.25	±0.75	LSB
Offset Error				±4			*			*	LSB
Gain Error				±4			*			*	LSB
Noise			33			*			*		µVrms
Power Supply Rejection			82			*			*		dB
SAMPLING DYNAMICS											
Conversion Time				12			*			*	Clk Cycles
Acquisition Time		1.5			*			*			Clk Cycles
Throughput Rate				200			*			*	kHz
DYNAMIC CHARACTERISTICS											
Total Harmonic Distortion	V_{IN} = 5.0Vp-p at 1kHz		–84			*			*		dB
	V_{IN} = 5.0Vp-p at 5kHz		–82			*			*		dB
SINAD	V_{IN} = 5.0Vp-p at 1kHz		72			*			*		dB
Spurious Free Dynamic Range	V_{IN} = 5.0Vp-p at 1kHz		86			*			*		dB
REFERENCE INPUT											
Voltage Range		0.1		5	*		*	*		*	V
Resistance	$\overline{CS}$ = GND, f_{SAMPLE} = 0Hz		5			*			*		GΩ
	$\overline{CS}$ = V_{CC}		5			*			*		GΩ
Current Drain	At Code 710h		38	100		*	*		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.4	20		*	*		*	*	µA
	$\overline{CS}$ = V_{CC}		0.001	3		*	*		*	*	µA
DIGITAL INPUT/OUTPUT											
Logic Family			CMOS			*			*		
Logic Levels:											
V_{IH}	I_{IH} = +5µA	3		$+V_{CC}$ +0.3	*		*	*		*	V
V_{IL}	I_{IL} = +5µA	–0.3		0.8	*		*	*		*	V
V_{OH}	I_{OH} = –250µA	3.5			*			*			V
V_{OL}	I_{OL} = 250µA			0.4			*			*	V
Data Format			Straight Binary			*			*		
POWER SUPPLY REQUIREMENTS											
V_{CC}	Specified Performance	4.50		5.25	*		*	*		*	V
Quiescent Current			380	700		*	*		*	*	µA
	f_{SAMPLE} = 12.5kHz[2, 3]		30			*			*		µA
	f_{SAMPLE} = 12.5kHz[3]		280	400		*			*		µA
Power Down	$\overline{CS}$ = V_{CC}, f_{SAMPLE} = 0Hz			3			*			*	µA
TEMPERATURE RANGE											
Specified Performance		–40		+85	*		*	*		*	°C

* Specifications same as grade to the left.

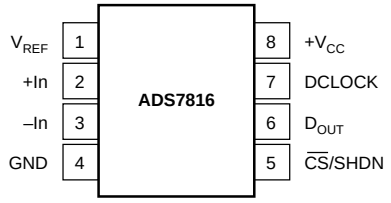
NOTE: (1) LSB means Least Significant Bit, with V_{REF} equal to +5V, one LSB is 1.22mV. (2) f_{CLK} = 3.2MHz, $\overline{CS}$ = V_{CC} for 251 clock cycles out of every 256. (3) See the Power Dissipation section for more information regarding lower sample rates.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_{CC}$	+6V
Analog Input	–0.3V to ($+V_{CC}$ + 0.3V)
Logic Input	–0.3V to ($+V_{CC}$ + 0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+125°C
External Reference Voltage	+5.5V

NOTE: (1) Stresses above these ratings may permanently damage the device.

PIN CONFIGURATION



8-Pin PDIP,
8-Lead SOIC,
8-Lead MSOP

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION
1	V_{REF}	Reference Input.
2	+In	Non Inverting Input.
3	–In	Inverting Input. Connect to ground or to remote ground sense point.
4	GND	Ground.
5	$\overline{CS}$/SHDN	Chip Select when LOW, Shutdown Mode when HIGH.
6	D_{OUT}	The serial output data word is comprised of 12 bits of data. In operation the data is valid on the falling edge of DCLOCK. The second clock pulse after the falling edge of $\overline{CS}$ enables the serial output. After one null bit the data is valid for the next 12 edges.
7	DCLOCK	Data Clock synchronizes the serial data transfer and determines conversion speed.
8	$+V_{CC}$	Power Supply.

PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB)	TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER[1]
ADS7816P	±2	±2	–40°C to +85°C	Plastic DIP	006
ADS7816U	±2	±2	–40°C to +85°C	SOIC	182
ADS7816E	±2	±2	–40°C to +85°C	MSOP	337
ADS7816PB	±2	±1	–40°C to +85°C	Plastic DIP	006
ADS7816UB	±2	±1	–40°C to +85°C	SOIC	182
ADS7816EB	±2	±1	–40°C to +85°C	MSOP	337
ADS7816PC	±1	±0.75	–40°C to +85°C	Plastic DIP	006
ADS7816UC	±1	±0.75	–40°C to +85°C	SOIC	182
ADS7816EC	±1	±0.75	–40°C to +85°C	MSOP	337

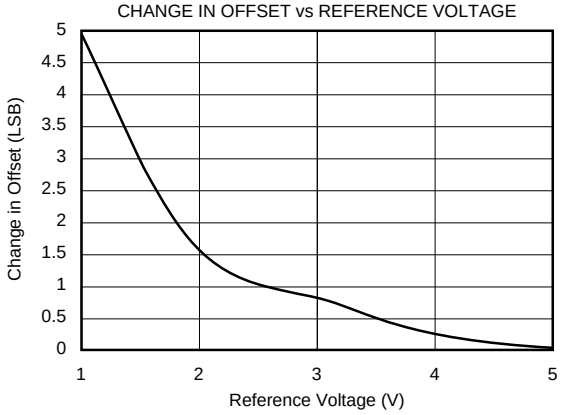
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

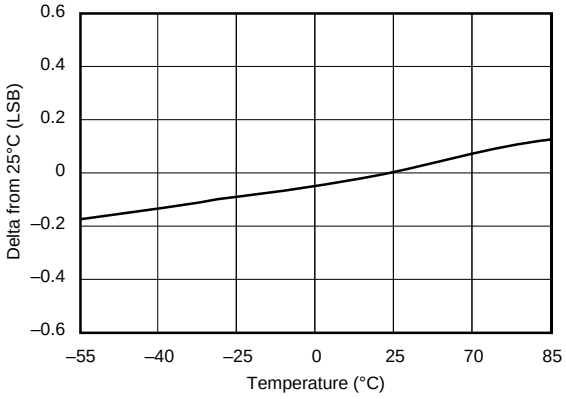
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{CC} = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE}, unless otherwise specified.

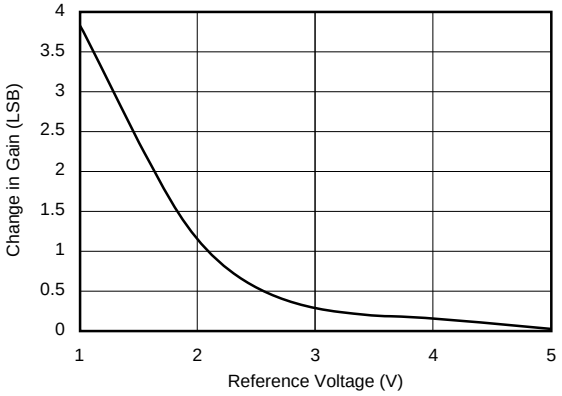
CHANGE IN OFFSET vs REFERENCE VOLTAGE



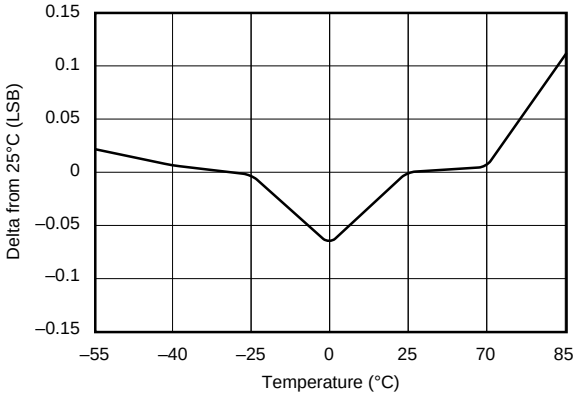
CHANGE IN OFFSET vs TEMPERATURE



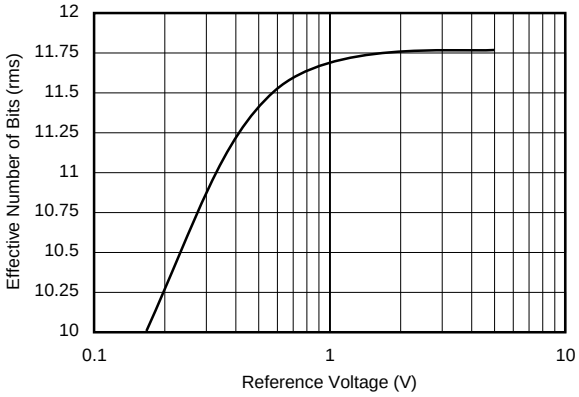
CHANGE IN GAIN vs REFERENCE VOLTAGE



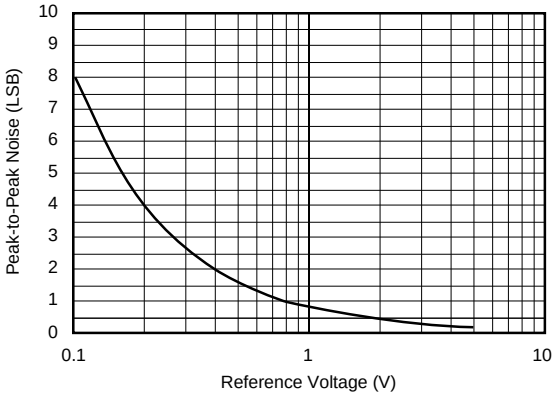
CHANGE IN GAIN vs TEMPERATURE



EFFECTIVE NUMBER OF BITS
vs REFERENCE VOLTAGE



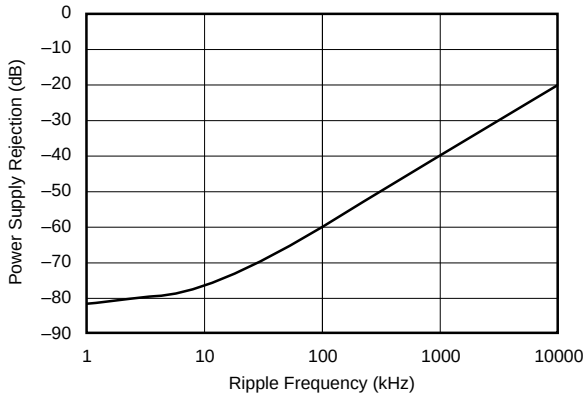
PEAK-TO-PEAK NOISE vs REFERENCE VOLTAGE



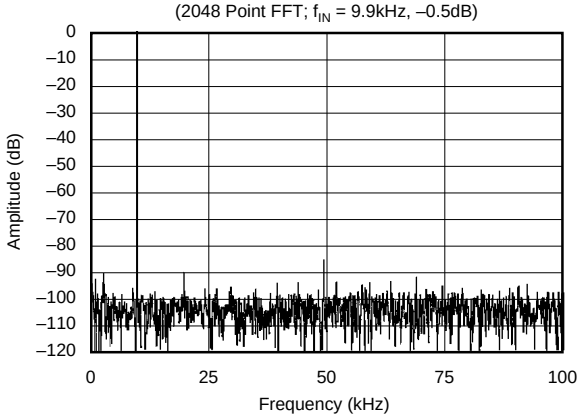
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_{CC} = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE}, unless otherwise specified.

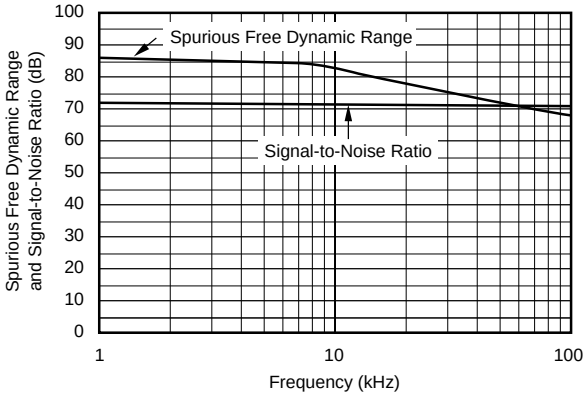
POWER SUPPLY REJECTION vs RIPPLE FREQUENCY



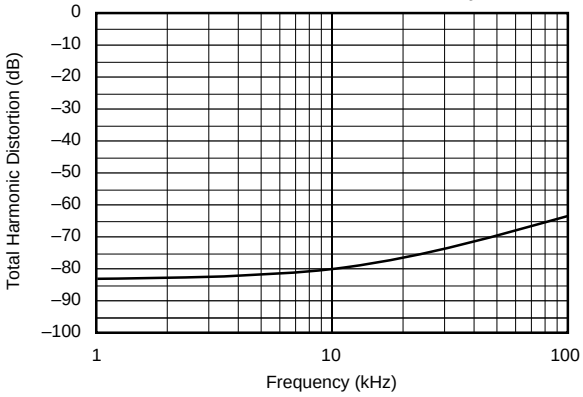
FREQUENCY SPECTRUM
(2048 Point FFT; f_{IN} = 9.9kHz, –0.5dB)



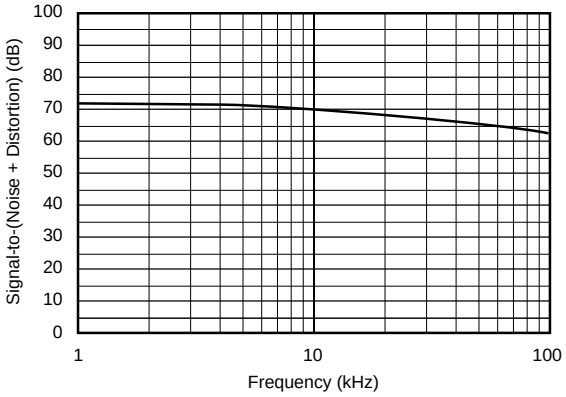
SPURIOUS FREE DYNAMIC RANGE and
SIGNAL-TO-NOISE RATIO vs FREQUENCY



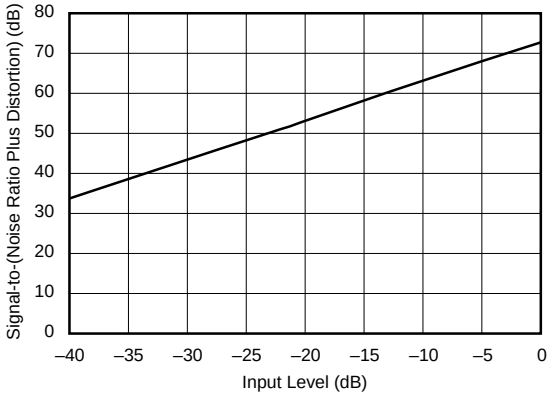
TOTAL HARMONIC DISTORTION vs FREQUENCY



SIGNAL-TO-(NOISE + DISTORTION) vs FREQUENCY



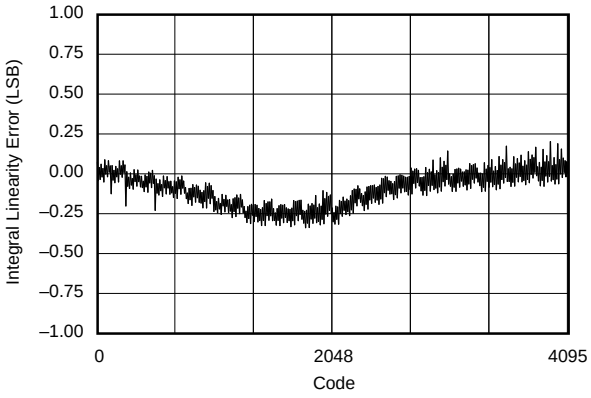
SIGNAL-TO-(NOISE + DISTORTION) vs INPUT LEVEL



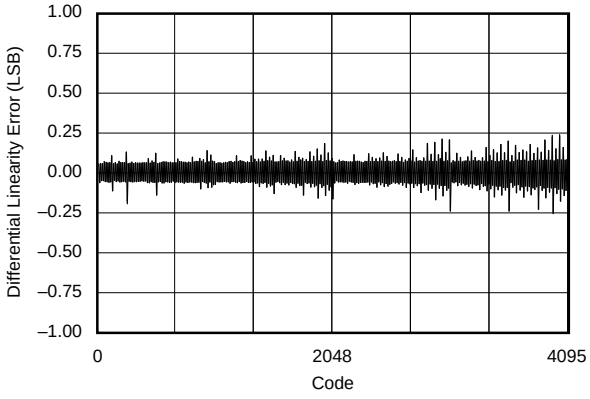
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_{CC} = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE}, unless otherwise specified.

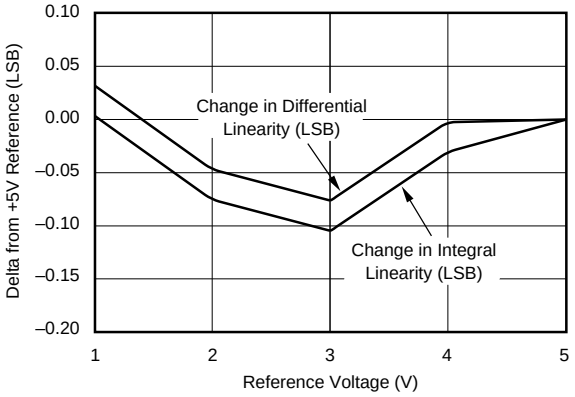
INTEGRAL LINEARITY ERROR vs CODE



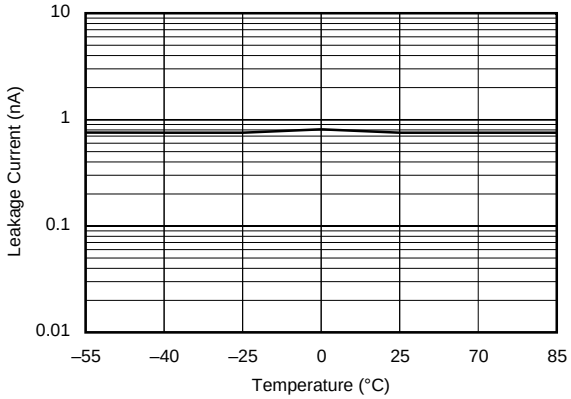
DIFFERENTIAL LINEARITY ERROR vs CODE



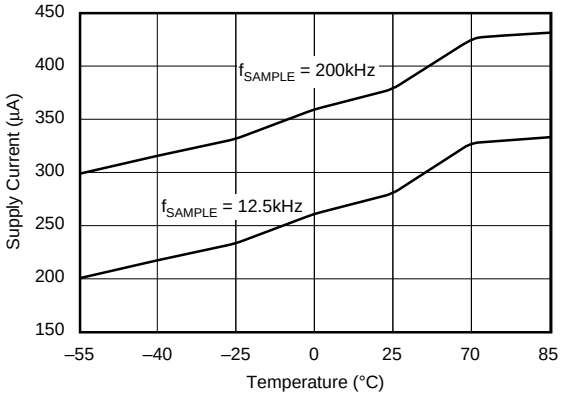
CHANGE IN INTEGRAL LINEARITY AND DIFFERENTIAL LINEARITY vs REFERENCE VOLTAGE



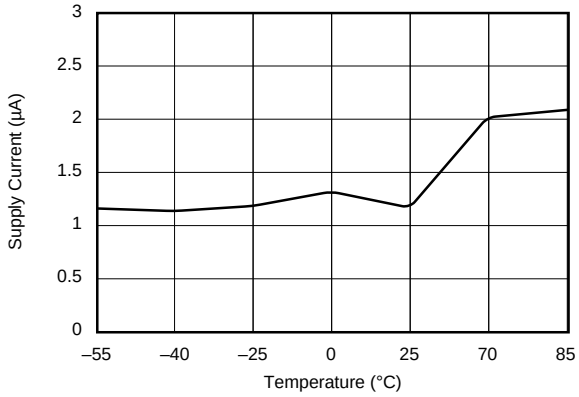
INPUT LEAKAGE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



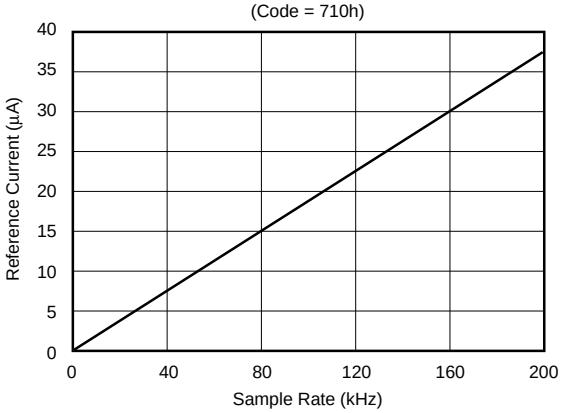
POWER DOWN SUPPLY CURRENT vs TEMPERATURE



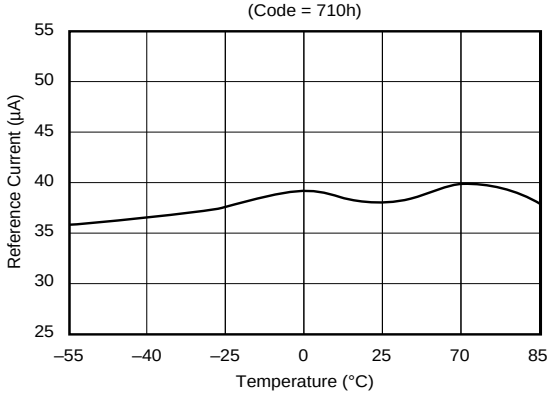
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_{CC} = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE}, unless otherwise specified.

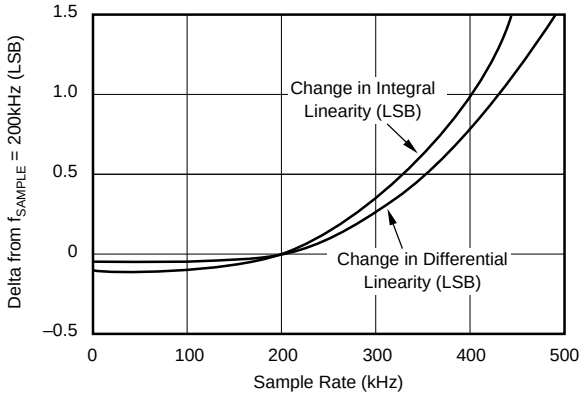
REFERENCE CURRENT vs SAMPLE RATE
(Code = 710h)



REFERENCE CURRENT vs TEMPERATURE
(Code = 710h)



CHANGE IN INTEGRAL LINEARITY and DIFFERENTIAL
LINEARITY vs SAMPLE RATE



THEORY OF OPERATION

The ADS7816 is a classic successive approximation register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution which inherently includes a sample/hold function. The converter is fabricated on a 0.6µ CMOS process. The architecture and process allow the ADS7816 to acquire and convert an analog signal at up to 200,000 conversions per second while consuming very little power.

The ADS7816 requires an external reference, an external clock, and a single +5V power source. The external reference can be any voltage between 100mV and V_{CC}. The value of the reference voltage directly sets the range of the analog input. The reference input current depends on the conversion rate of the ADS7816.

The external clock can vary between 10kHz (625Hz throughput) and 3.2MHz (200kHz throughput). The duty cycle of the clock is essentially unimportant as long as the minimum high and low times are at least 150ns. The minimum clock frequency is set by the leakage on the capacitors internal to the ADS7816.

The analog input is provided to two input pins: +In and –In. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The digital result of the conversion is clocked out by the DCLOCK input and is provided serially, most significant bit first, on the D_{OUT} pin. The digital data that is provided on the D_{OUT} pin is for the conversion currently in progress—there is no pipeline delay. It is possible to continue to clock the ADS7816 after the conversion is complete and to obtain the serial data least significant bit first. See the Digital Interface section for more information.

ANALOG INPUT

The +In and –In input pins allow for a differential input signal. Unlike some converters of this type, the –In input is not resampled later in the conversion cycle. When the converter goes into the hold mode, the voltage difference between +In and –In is captured on the internal capacitor array.

The range of the –In input is limited to ±200mV. Because of this, the differential input can be used to reject only small signals that are common to both inputs. Thus, the –In input is best used to sense a remote signal ground that may move slightly with respect to the local ground potential.

The input current on the analog inputs depends on a number of factors: sample rate, input voltage, source impedance, and power down mode. Essentially, the current into the ADS7816 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (25pF) to a 12-bit settling level within 1.5 clock cycles. When the converter goes into the hold mode or while it is in the power down mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the –In input should not exceed GND ±200mV. The +In input should always remain within the range of GND –200mV to V_{CC} +200mV. Outside of these ranges, the converter's linearity may not meet specifications.

REFERENCE INPUT

The external reference sets the analog input range. The ADS7816 will operate with a reference in the range of 100mV to V_{CC}. There are several important implications of this.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced. The typical performance curves of "Change in Offset vs Reference Voltage" and "Change in Gain vs Reference Voltage" provide more information.

The noise inherent in the converter will also appear to increase with lower LSB size. With a 5V reference, the internal noise of the converter typically contributes only 0.16 LSB peak-to-peak of potential error to the output code. When the external reference is 100mV, the potential error contribution from the internal noise will be 50 times larger—8 LSBs. The errors due to the internal noise are gaussian in nature and can be reduced by averaging consecutive conversion results.

For more information regarding noise, consult the typical performance curves "Effective Number of Bits vs Reference Voltage" and "Peak-to-Peak Noise vs Reference Voltage." The effective number of bits (ENOB) figure is calculated based on the converter's signal-to-(noise + distortion) ratio with a 1kHz, 0dB input signal. SINAD is related to ENOB as follows: SINAD = 6.02 • ENOB +1.76.

With lower reference voltages, extra care should be taken to provide a clean layout including adequate bypassing, a clean power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter will also be more sensitive to external sources of error such as nearby digital signals and electromagnetic interference.

The current that must be provided by the external reference will depend on the conversion result. The current is lowest at full-scale (FFFh) and is typically 25µA at a 200kHz conversion rate (25°C). For the same conditions, the current will increase as the input approaches zero, reaching 50µA at an output result of 000h. The current does not increase linearly, but depends, to some degree, on the bit pattern of the digital output.

The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce the overall current drain from the reference. The reference current changes only slightly with temperature. See the curves, "Reference Current vs Sample Rate" and "Reference Current vs Temperature" in the Typical Performance Curves section for more information.

DIGITAL INTERFACE

SERIAL INTERFACE

The ADS7816 communicates with microprocessors and other digital systems via a synchronous 3-wire serial interface as shown in Figure 1 and Table I. The DCLOCK signal synchronizes the data transfer with each bit being transmitted on the falling edge of DCLOCK. Most receiving systems will capture the bitstream on the rising edge of DCLOCK. However, if the minimum hold time for D_{OUT} is acceptable, the system can use the falling edge of DCLOCK to capture each bit.

A falling $\overline{CS}$ signal initiates the conversion and data transfer. The first 1.5 to 2.0 clock periods of the conversion cycle are used to sample the input signal. After the second falling DCLOCK edge, D_{OUT} is enabled and will output a LOW value for one clock period. For the next 12 DCLOCK periods, D_{OUT} will output the conversion result, most significant bit first. After the least significant bit (B0) has been output, subsequent clocks will repeat the output data but in a least significant bit first format.

After the most significant bit (B11) has been repeated, D_{OUT} will tri-state. Subsequent clocks will have no effect on the converter. A new conversion is initiated only when $\overline{CS}$ has been taken HIGH and returned LOW.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample TIme	1.5		2.0	Clk Cycles
t_{CONV}	Conversion Time		12		Clk Cycles
t_{CYC}	Throughput Rate			200	kHz
t_{CSD}	$\overline{CS}$ Falling to DCLOCK LOW			0	ns
t_{SUCS}	$\overline{CS}$ Falling to DCLOCK Rising	30			ns
t_{hDO}	DCLOCK Falling to Current D_{OUT} Not Valid	15			ns
t_{dDO}	DCLOCK Falling to Next D_{OUT} Valid		85	150	ns
t_{dis}	$\overline{CS}$ Rising to D_{OUT} Tri-State		25	50	ns
t_{en}	DCLOCK Falling to D_{OUT} Enabled		50	100	ns
t_f	D_{OUT} Fall Time		70	100	ns
t_r	D_{OUT} Rise Time		60	100	ns

TABLE I. Timing Specifications –40°C to +85°C.

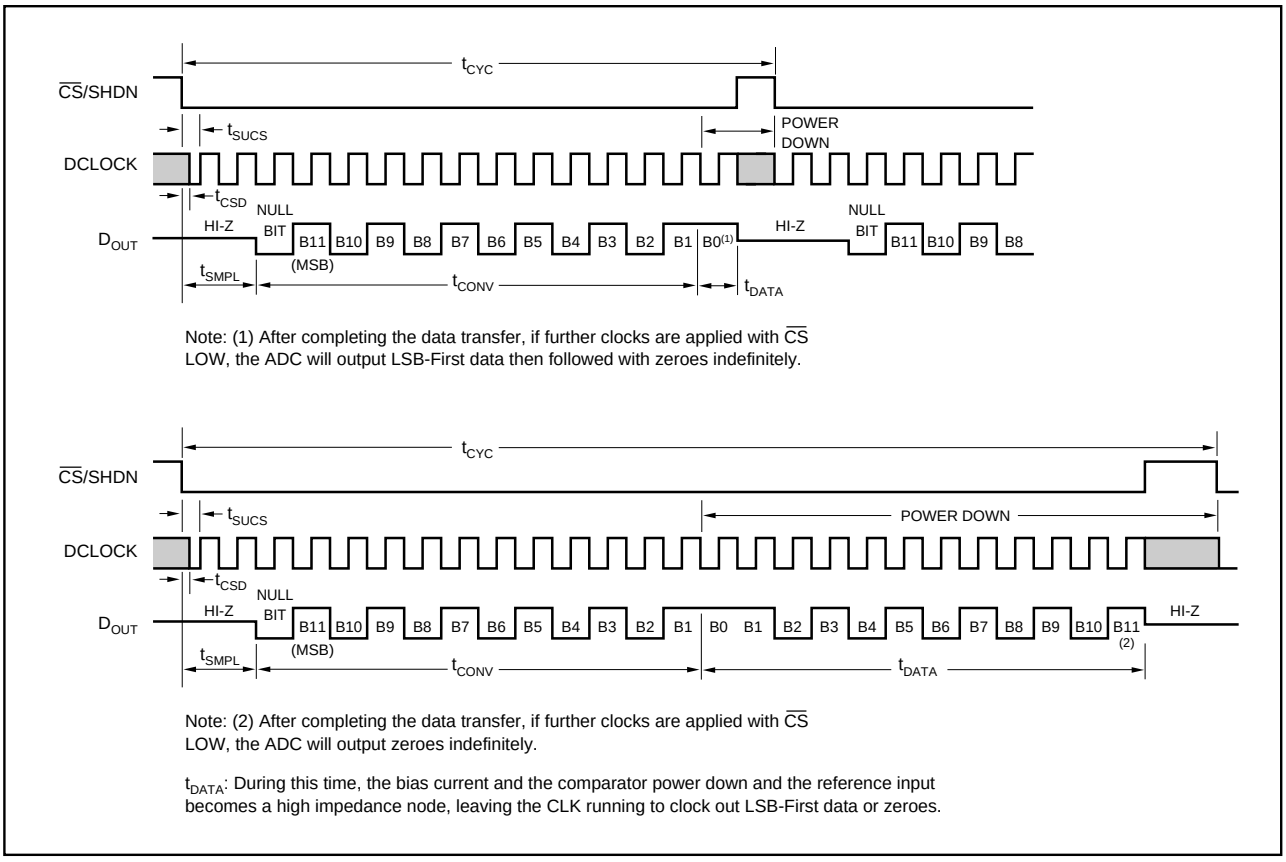


FIGURE 1. ADS7816 Basic Timing Diagrams.

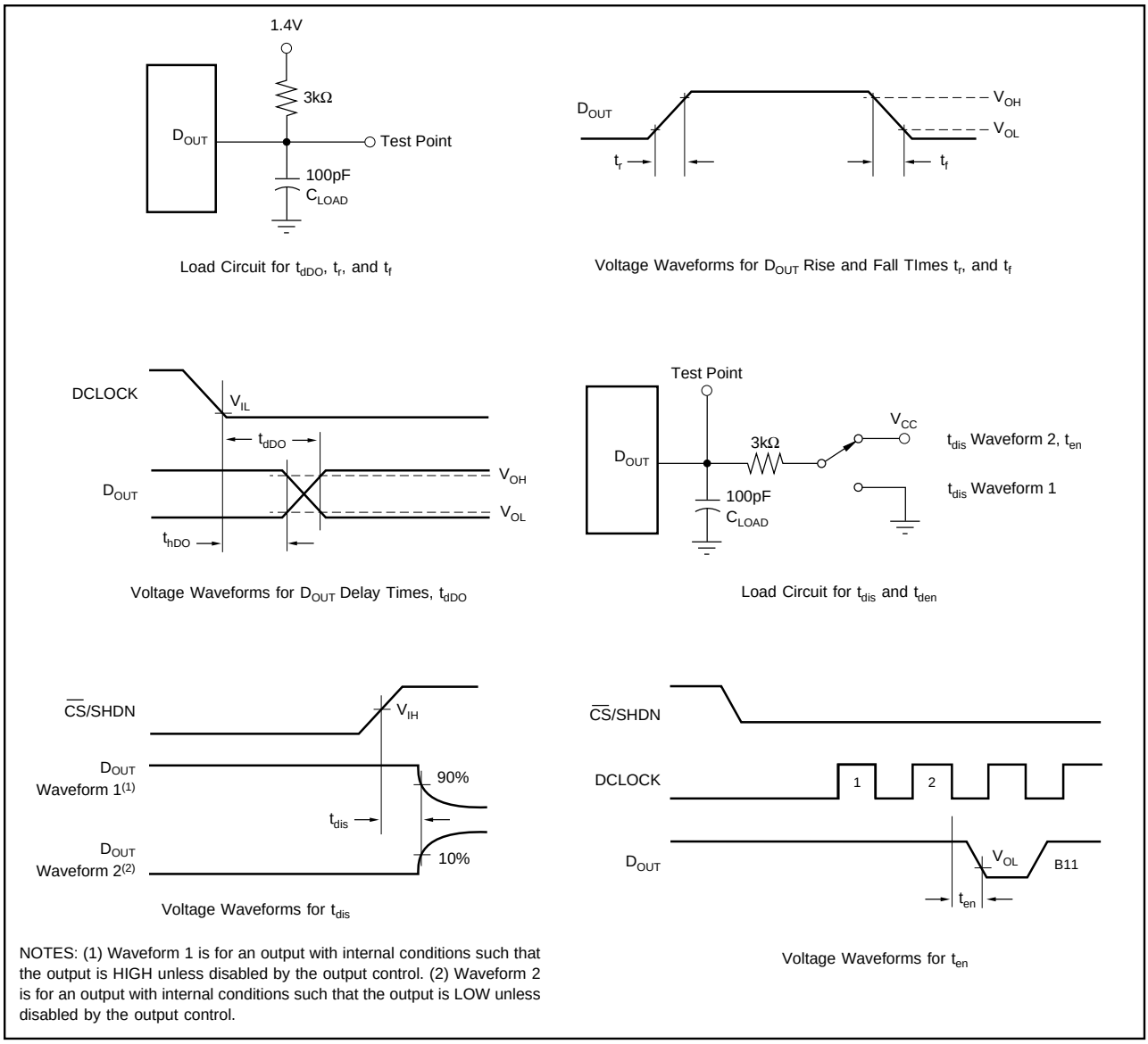


FIGURE 2. Timing Diagrams and Test Circuits for the Parameters in Table I.

DATA FORMAT

The output data from the ADS7816 is in Straight Binary format as shown in Table II. This table represents the ideal output code for the given input voltage and does not include the effects of offset, gain error, or noise.

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT: STRAIGHT BINARY	
		BINARY CODE	HEX CODE
Full Scale Range	V_{REF}	1111 1111 1111	FFF
Least Significant Bit (LSB)	V_{REF}/4096	0000 0000 0001	001
Full Scale	V_{REF} –1 LSB	1111 1111 1111	FFF
Midscale	V_{REF}/2	1000 0000 0000	800
Midscale – 1 LSB	V_{REF}/2 – 1 LSB	0111 1111 1111	7FF
Zero	0V	0000 0000 0000	000

Table II. Ideal Input Voltages and Output Codes.

POWER DISSIPATION

The architecture of the converter, the semiconductor fabrication process, and a careful design allow the ADS7816 to convert at up to a 200kHz rate while requiring very little power. Still, for the absolute lowest power dissipation, there are several things to keep in mind.

The power dissipation of the ADS7816 scales directly with conversion rate. The first step to achieving the lowest power dissipation is to find the lowest conversion rate that will satisfy the requirements of the system.

In addition, the ADS7816 is in power down mode under two conditions: when the conversion is complete and whenever $\overline{CS}$ is HIGH (see Figure 1). Ideally, each conversion should occur as quickly as possible, preferably, at a 3.2MHz clock rate. This way, the converter spends the longest possible time in the power down mode. This is very important as the

converter not only uses power on each DCLOCK transition (as is typical for digital CMOS components) but also uses some current for the analog circuitry, such as the comparator. The analog section dissipates power continuously, until the power down mode is entered.

Figure 3 shows the current consumption of the ADS7816 versus sample rate. For this graph, the converter is clocked at 3.2MHz regardless of the sample rate—$\overline{CS}$ is HIGH for the remaining sample period. Figure 4 also shows current consumption versus sample rate. However, in this case, the DCLOCK period is 1/16th of the sample period—$\overline{CS}$ is HIGH for one DCLOCK cycle out of every 16.

There is an important distinction between the power down mode that is entered after a conversion is complete and the full power down mode which is enabled when $\overline{CS}$ is HIGH. While both power down the analog section, the digital section is powered down only when $\overline{CS}$ is HIGH. Thus, if $\overline{CS}$ is left LOW at the end of a conversion and the converter is continually clocked, the power consumption will not be as low as when $\overline{CS}$ is HIGH. See Figure 5 for more information.

By lowering the reference voltage, the ADS7816 requires less current to completely charge its internal capacitors on both the analog input and the reference input. This reduction in power dissipation should be weighed carefully against the resulting increase in noise, offset, and gain error as outlined in the Reference section. The power dissipation of the ADS7816 is reduced roughly 10% when the reference voltage and input range are changed from 5V to 100mV.

SHORT CYCLING

Another way of saving power is to utilize the $\overline{CS}$ signal to short cycle the conversion. Because the ADS7816 places the latest data bit on the D_{OUT} line as it is generated, the converter can easily be short cycled. This term means that the conversion can be terminated at any time. For example, if only 8-bits of the conversion result are needed, then the conversion can be terminated (by pulling $\overline{CS}$ HIGH) after the 8th bit has been clocked out.

This technique can be used to lower the power dissipation (or to increase the conversion rate) in those applications where an analog signal is being monitored until some condition becomes true. For example, if the signal is outside a predetermined range, the full 12-bit conversion result may not be needed. If so, the conversion can be terminated after the first n-bits, where n might be as low as 3 or 4. This results in lower power dissipation in both the converter and the rest of the system, as they spend more time in the power down mode.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7816 circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high. At 200kHz conversion rate, the ADS7816 makes a bit decision every 312ns. That is, for each subsequent bit deci-

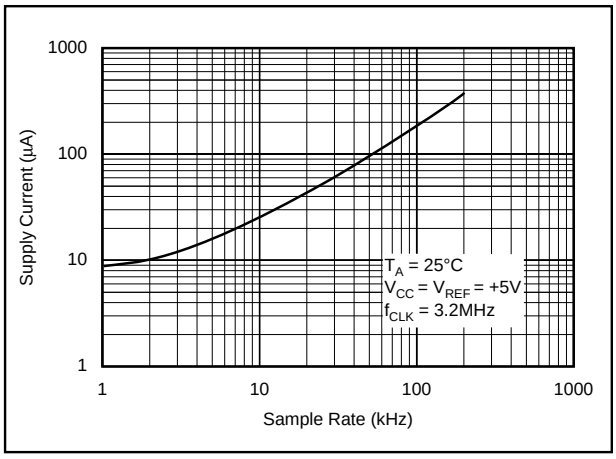


FIGURE 3. Maintaining f_{CLK} at the Highest Possible Rate Allows Supply Current to Drop Directly with Sample Rate.

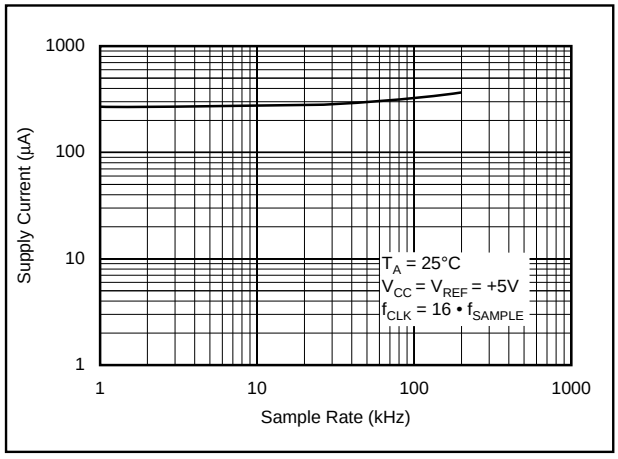


FIGURE 4. Scaling f_{CLK} Reduces Supply Current Only Slightly with Sample Rate.

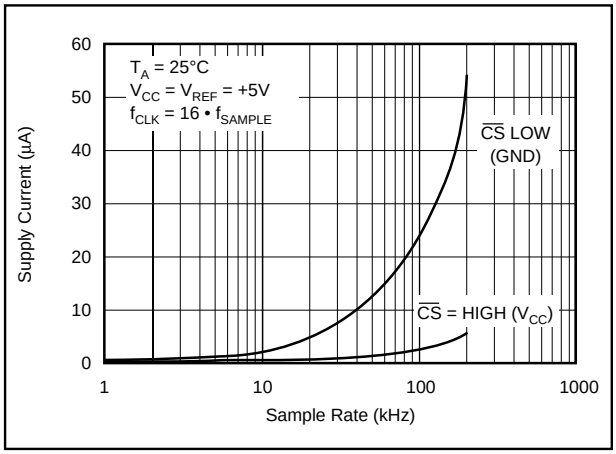


FIGURE 5. Shutdown Current is Considerably Lower with $\overline{CS}$ HIGH than when $\overline{CS}$ is LOW.

sion, the digital output must be updated with the results of the last bit decision, the capacitor array appropriately switched and charged, and the input to the comparator settled to a 12-bit level all within one clock cycle.

The basic SAR architecture is sensitive to spikes on the power supply, reference, and ground connections that occur just prior to latching the comparator output. Thus, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such spikes might originate from switching power supplies, digital logic, and high power devices, to name a few. This particular source of error can be very difficult to track down if the glitch is almost synchronous to the converter's DCLOCK signal—as the phase difference between the two changes with time and temperature, causing sporadic misoperation.

With this in mind, power to the ADS7816 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the ADS7816 package as possible. In addition, a 1 to 10µF capacitor and a 10Ω series resistor may be used to lowpass filter a noisy supply.

The reference should be similarly bypassed with a 0.1µF capacitor. Again, a series resistor and large capacitor can be used to lowpass filter the reference voltage. If the reference voltage originates from an op amp, be careful that the op-amp can drive the bypass capacitor without oscillation (the series resistor can help in this case). Keep in mind that while the ADS7816 draws very little current from the reference on average, there are higher instantaneous current demands placed on the external reference circuitry.

Also, keep in mind that the ADS7816 offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high frequency noise can be filtered out as described in the previous paragraph, voltage variation due to the line frequency (50Hz or 60Hz), can be difficult to remove.

The GND pin on the ADS7816 should be placed on a clean ground point. In many cases, this will be the "analog" ground. Avoid connecting the GND pin too close to the grounding point for a microprocessor, microcontroller, or digital signal processor. If needed, run a ground trace directly from the converter to the power supply connection point. The ideal layout will include an analog ground plane for the converter and associated analog circuitry.

The –In input pin should be connected directly to ground. In those cases where the ADS7816 is a large distance from the signal source and/or the circuit environment contains large EMI or RFI sources, the –In input should be connected to the ground nearest the signal source. This should be done with a signal trace that is adjacent to the +In input trace. If appropriate, coax cable or twisted-pair wire can be used.

APPLICATION CIRCUITS

Figures 6, 7, and 8 show some typical application circuits for the ADS7816. Figure 6 uses an ADS7816 and a multiplexer to provide for a flexible data acquisition circuit. A resistor string provides for various voltages at the multiplexer input. The selected voltage is buffered and driven into V_{REF}. As shown in Figure 6, the input range of the ADS7816 is programmable to 100mV, 200mV, 300mV, or 400mV. The 100mV range would be useful for sensors such as the thermocouple shown.

Figure 7 is more complex variation of Figure 6 with increased flexibility. In this circuit, a digital signal processor designed for audio applications is put to use in running three ADS7816s and a DAC56. The DAC56 provides a variable voltage for V_{REF}—enabling the input range of the ADS7816s to be programmed from 100mV to 3V.

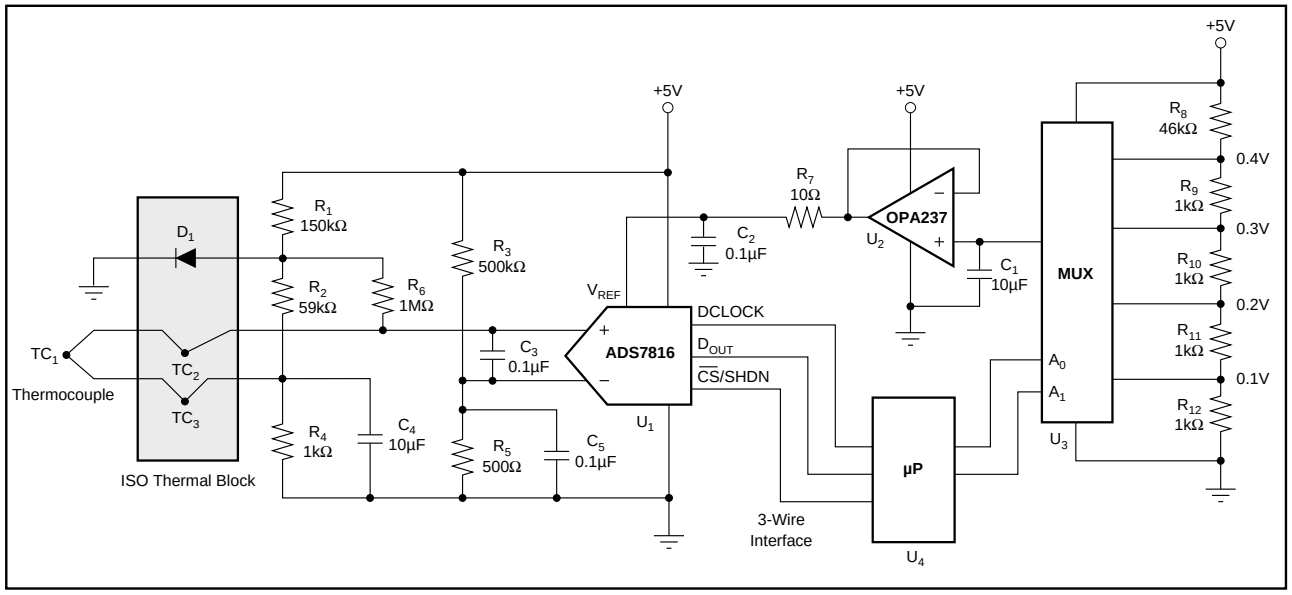


FIGURE 6. Thermocouple Application Using a MUX to Scale the Input Range of the ADS7816.

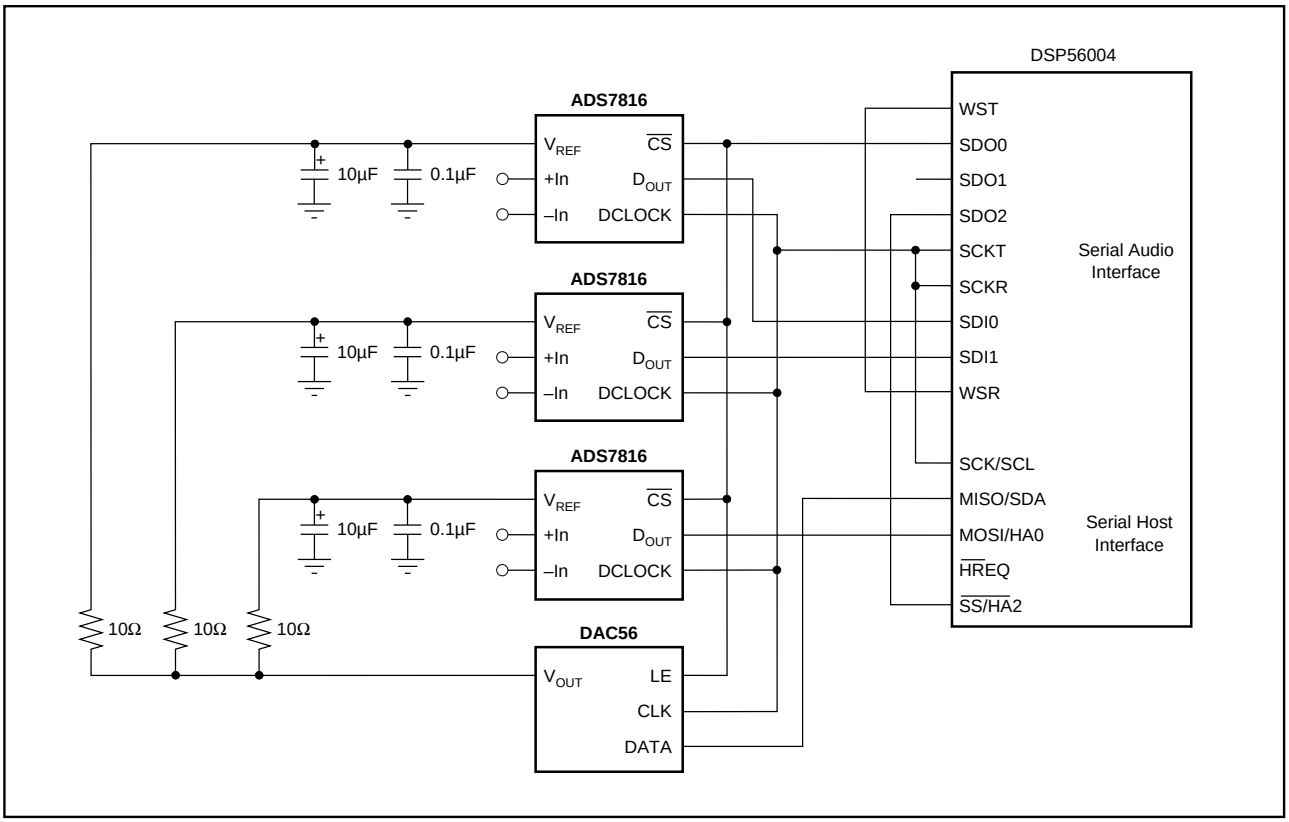


FIGURE 7. Flexible Data Acquisition System.

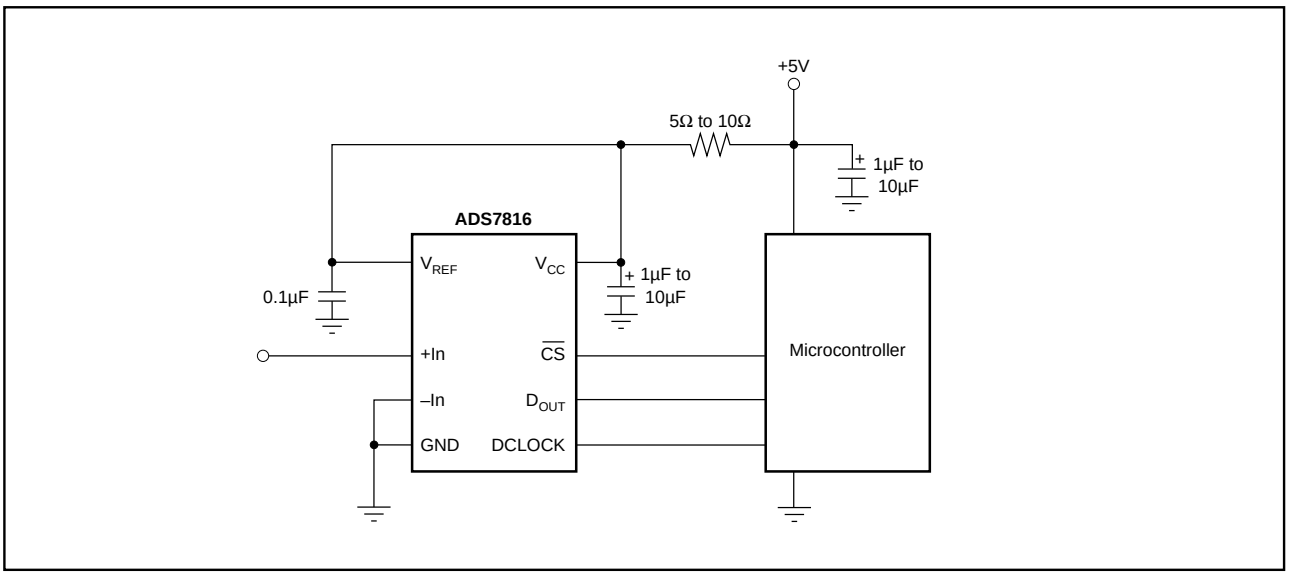


FIGURE 8. Basic Data Acquisition System.

The ADS7816s and the DSP56004 can all be placed into a power down mode. Or, the DSP56004 can run the ADS7816s at a full 3.2MHz clock rate while on-board software enables the ADS7816s as needed. With additional glue logic, the DSP56004 could be used to run multiple DAC56s or provide $\overline{CS}$ controls for each of the three ADS7816s.

Figure 8 shows a basic data acquisition system. The ADS7816 input range is 0V to 5V, as the reference input is connected directly to the +5V supply. The 5Ω to 10Ω resistor and 1µF to 10µF capacitor filter the microcontroller "noise" on the supply, as well as any high-frequency noise from the supply itself. The exact values should be picked such that the filter provides adequate rejection of the noise.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7816E/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	A16	Samples
ADS7816E/250G4	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	A16	Samples
ADS7816E/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	A16	Samples
ADS7816E/2K5G4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	A16	Samples
ADS7816EB/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	A16	Samples
ADS7816EB/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	A16	Samples
ADS7816EB/2K5G4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	A16	Samples
ADS7816EC/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	A16	Samples
ADS7816EC/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	A16	Samples
ADS7816U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 7816U	Samples
ADS7816U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 7816U	Samples
ADS7816U/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 7816U	Samples
ADS7816UB	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7816U B	Samples
ADS7816UB/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7816U B	Samples
ADS7816UBG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7816U B	Samples
ADS7816UC	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 7816U C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7816UC/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 7816U C	Samples
ADS7816UC/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 7816U C	Samples
ADS7816UG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 7816U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

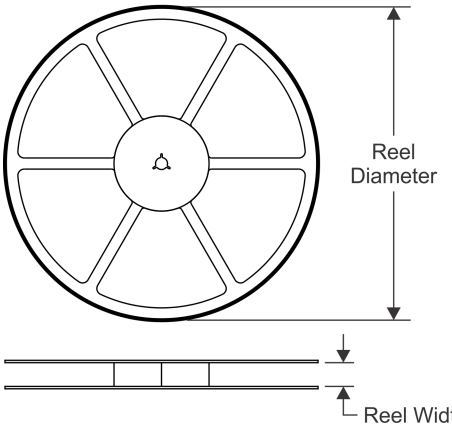
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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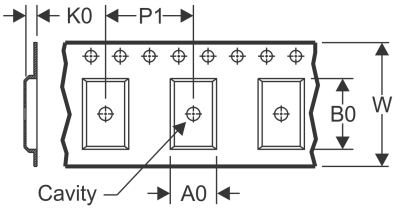
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

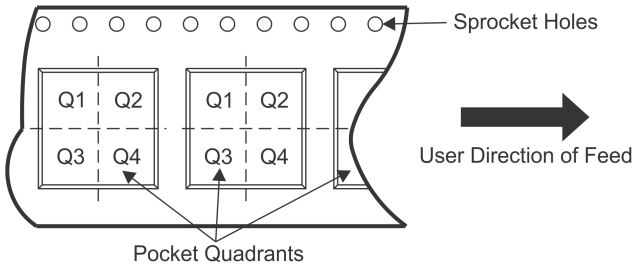


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

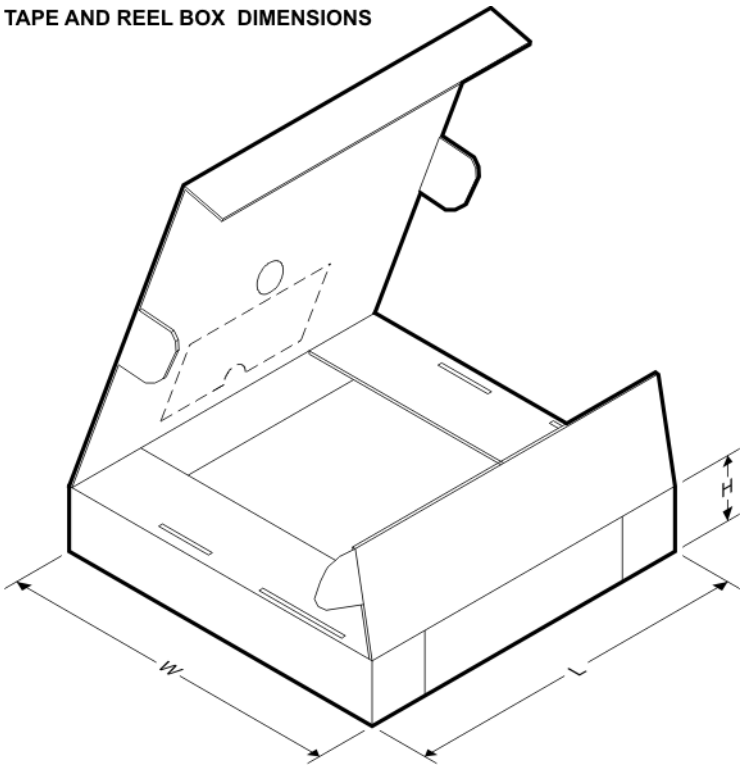
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7816E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7816EB/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7816EB/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7816EC/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7816U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ADS7816UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ADS7816UC/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

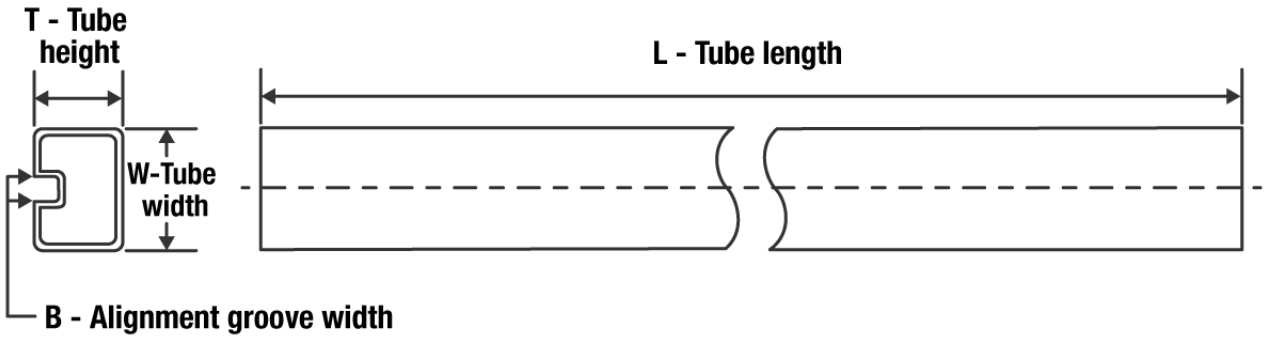
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

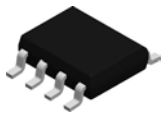
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7816E/2K5	VSSOP	DGK	8	2500	350.0	350.0	43.0
ADS7816EB/250	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS7816EB/2K5	VSSOP	DGK	8	2500	350.0	350.0	43.0
ADS7816EC/2K5	VSSOP	DGK	8	2500	350.0	350.0	43.0
ADS7816U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
ADS7816UB/2K5	SOIC	D	8	2500	367.0	367.0	35.0
ADS7816UC/2K5	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS7816U	D	SOIC	8	75	506.6	8	3940	4.32
ADS7816UB	D	SOIC	8	75	506.6	8	3940	4.32
ADS7816UBG4	D	SOIC	8	75	506.6	8	3940	4.32
ADS7816UC	D	SOIC	8	75	506.6	8	3940	4.32
ADS7816UG4	D	SOIC	8	75	506.6	8	3940	4.32

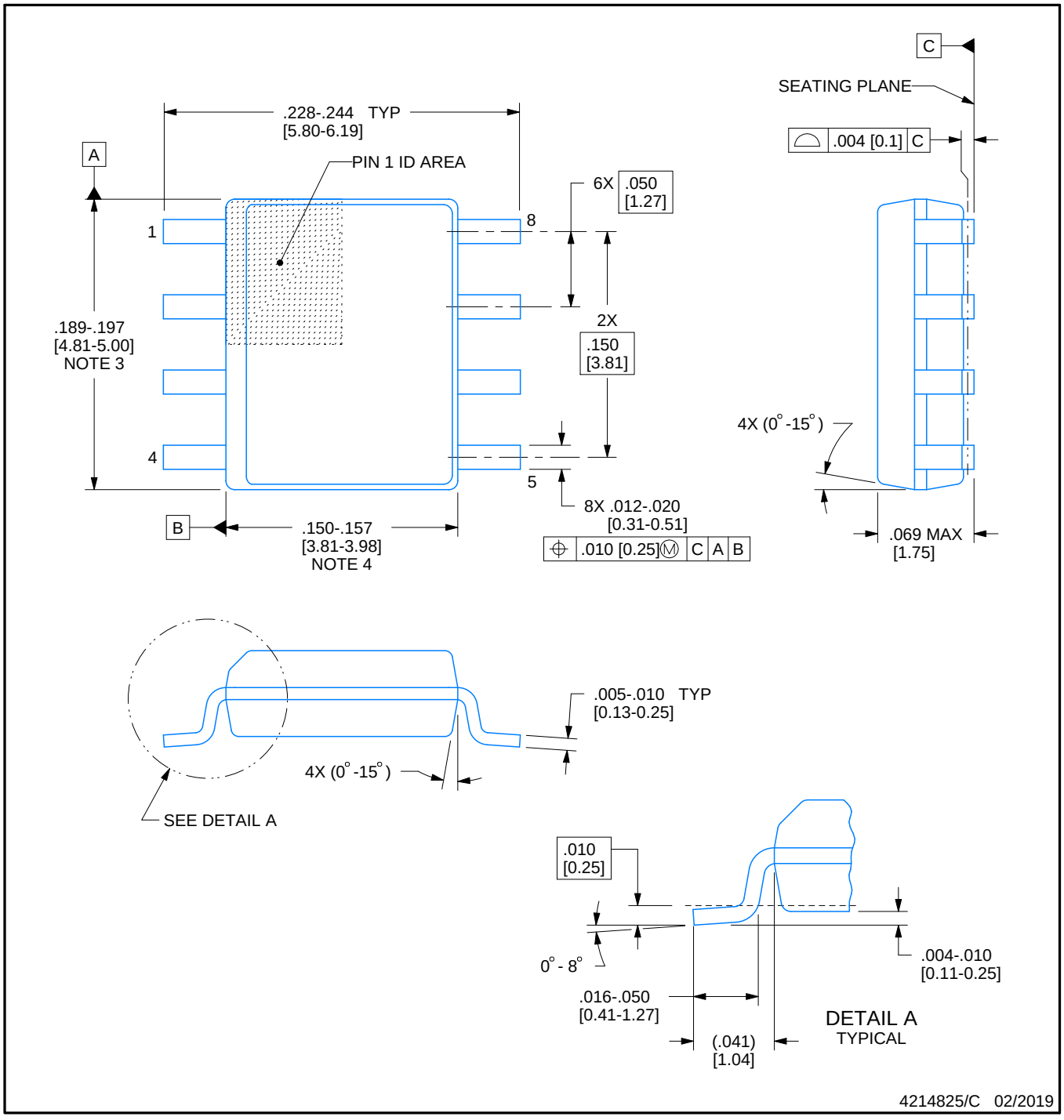


PACKAGE OUTLINE

D0008A

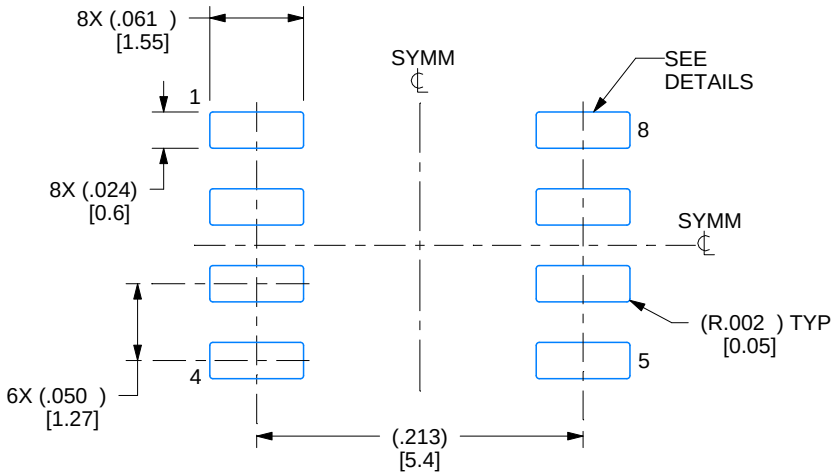
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

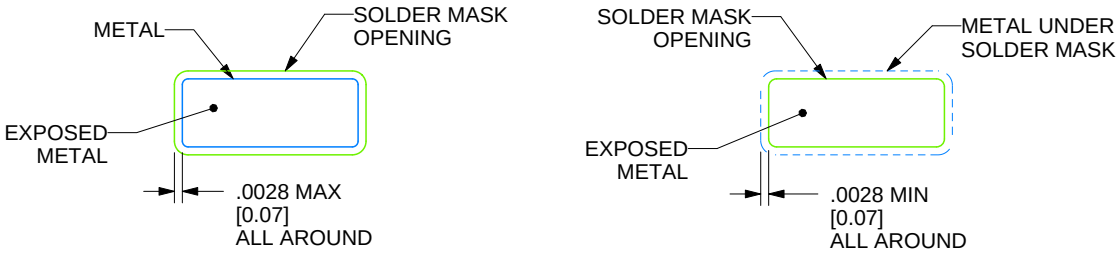


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

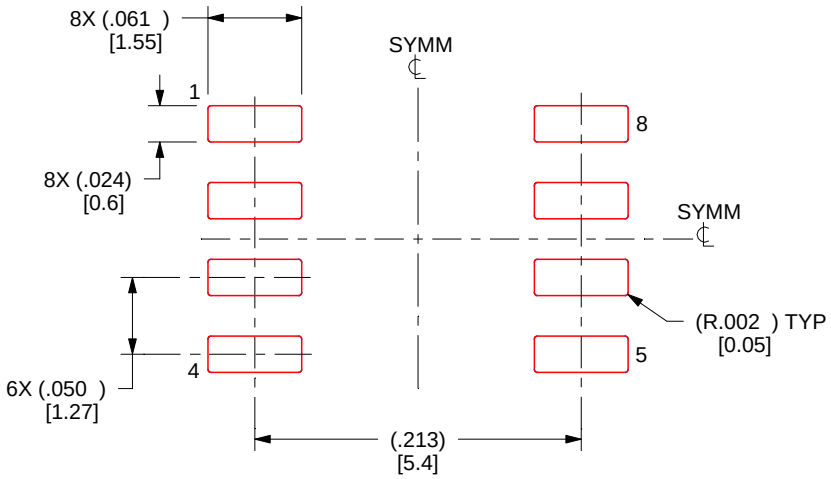
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



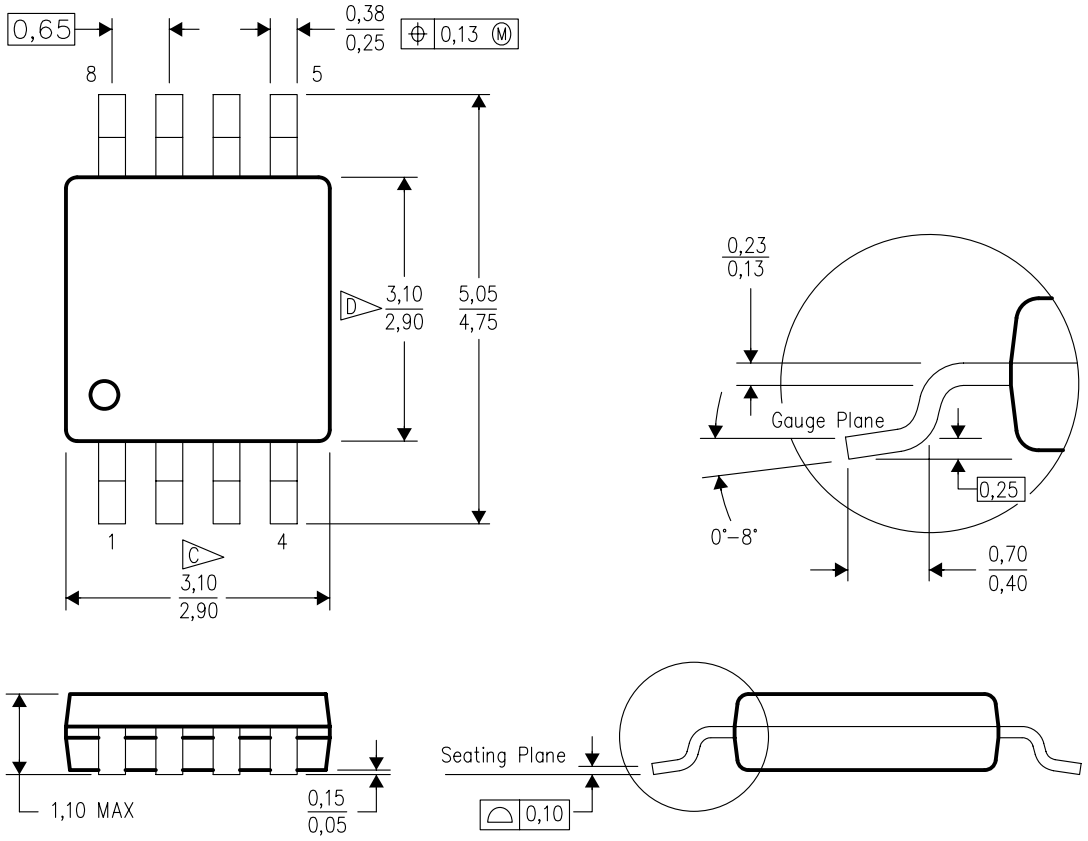
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

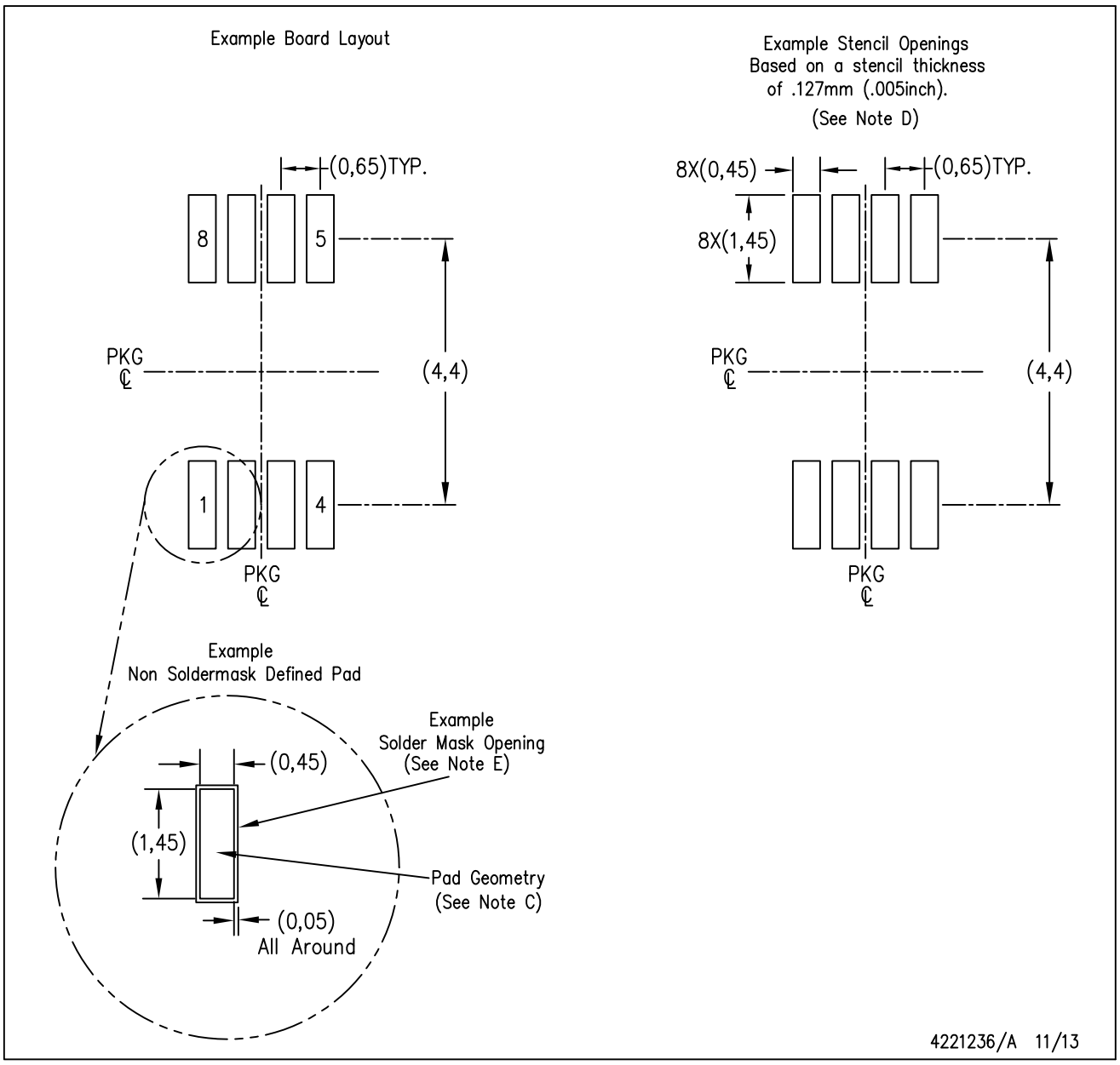
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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