TSC2014 1.2V to 3.6V, 12-Bit, Nanopower, 4-Wire Touch Screen Controller with I²C™ Interface

1 Features

- 4-Wire Touch Screen Interface
- Ratiometric Conversion
- Single 1.2V to 3.6V Supply
- Preprocessing to Reduce Bus Activity
- High-Speed I²C-Compatible Interface
- Internal Detection of Screen Touch
- Register-Based Programmable:
  - 10-Bit or 12-Bit Resolution
  - Sampling Rates
  - System Timing
- On-Chip Temperature Measurement
- Touch Pressure Measurement
- Auto Power-Down Control
- Low Power:
  - 430µW at 1.8V, 50SSPS
  - 320µW at 1.6V, 50SSPS
  - 190µW at 1.2V, 50SSPS
  - 58µW at 1.6V, 8.2kSPS Eq. Rate
  - 37µW at 1.2V, 8.2kSPS Eq. Rate
- Enhanced ESD Protection:
  - ±8kV HBM
  - ±1kV CDM
  - ±25kV Air Gap Discharge
  - ±11kV Contact Discharge
- 1.5 x 2.0 WCSP-12 Package

(1) U.S. Patent No. 6,246,394; other patents pending.

2 Applications

- Cellular Phones
- Portable Instruments
- MP3 Players, Pagers
- Multiscreen Touch Control

3 Description

The TSC2014 is a very low-power touch screen controller designed to work with power-sensitive, handheld applications that are based on advanced low-voltage processors. It works with a supply voltage as low as 1.2V, which can be supplied by a single-cell battery. It contains a complete, ultralow-power, 12-bit, analog-to-digital (A/D) resistive touch screen converter, including drivers and the control logic to measure touch pressure.

In addition to these standard features, the TSC2014 offers preprocessing of the touch screen measurements to reduce bus loading, thus reducing the consumption of host processor resources that can then be redirected to more critical functions.

The TSC2014 supports an I²C serial bus and data transmission protocol in all three defined modes: standard, fast, and high-speed. It offers programmable resolution of 10 or 12 bits to accommodate different screen sizes and performance needs.

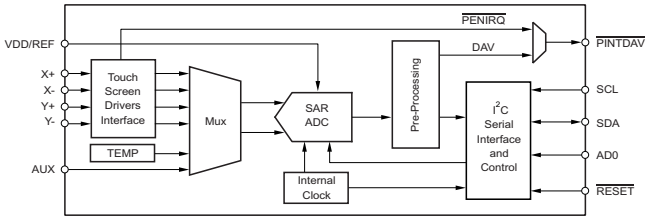
The TSC2014 is available in a miniature, 12-lead, 3 x 4 array, (1.555 ±0.055)mm x (2.055 ±0.055)mm wafer chip-scale package (WCSP) package. The device is characterized for the –40°C to +85°C industrial temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TSC2014	DSBGA (12)	(1.555 ±0.055)mm x (2.055 ±0.055)mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2012) to Revision B	Page
• Added *Device Information* table, *ESD Ratings* table, *Recommended Operating Conditions* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section*Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted the *ORDERING INFORMATION* table	1

Changes from Original (September 2010) to Revision A	Page
• Changed notes for 100kHz Timing Requirements table	7
• Changed notes for 400kHz Timing Requirements table	7
• Changed notes for 1.7MHz Timing Requirements table	8
• Changed Fall Time for SDA Signal from 20ns to 1ns for 1.7MHz Timing Requirements table	8
• Changed notes for 3.4MHz Timing Requirements table	8
• Changed Fall Time for SDA Signal from 10ns to 1ns for 3.4MHz Timing Requirements table	8

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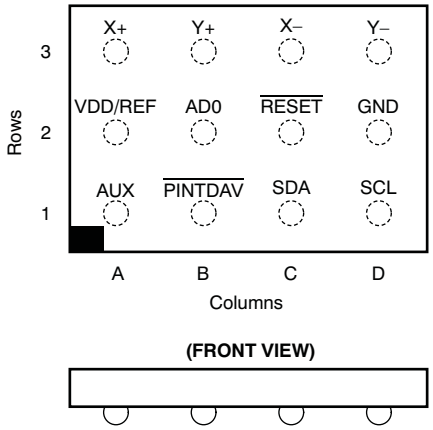
5 Pin Configuration and Functions

YZG Package
WCSP-12
(Top View, Solder Bumps on Bottom Side)



Pin Assignments

WCSP	NAME	I/O	ANALOG/ DIGITAL	DESCRIPTION
A1	AUX	I	A	Auxiliary channel input
A2	VDD/REF			Supply voltage and external reference input
A3	X+	I	A	X+ channel input
B1	$\overline{\text{PINTDAV}}$	O	D	Interrupt output. Data available or $\overline{\text{PENIRQ}}$, depending on setting. Pin polarity is active low.
B2	AD0	I	D	Address input bit 0
B3	Y+	I	A	Y+ channel input
C1	SDA	I/O	D	Serial data I/O
C2	$\overline{\text{RESET}}$	I	D	External hardware-reset input
C3	X–	I	A	X– channel input
D1	SCL	I	D	Serial clock.
D2	GND			Ground
D3	Y–	I	A	Y– channel input

6 Electrical Specifications

6.1 Absolute Maximum Ratings[1]

Over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
Voltage range	Analog input X+, Y+, AUX to GND	–0.4	V_{DD} + 0.1	V
	Analog input X–, Y– to GND	–0.4	V_{DD} + 0.1	V
	VDD/REF pin to GND	–0.	5	V
Digital input voltage to GND		–0.	V_{DD} + 0.3	V
Digital output voltage to GND		–0.	V_{DD} + 0.3	V
Operating free-air temperature range, T_A		–40	85	°C
Storage temperature range, T_{STG}		–65	150	°C
Junction temperature, T_J Max			150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC[1]		TSC2014 YZG (DSBGA) 12 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	115	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	30	°C/W
θ_{JB}	Junction-to-board thermal resistance	82	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	75	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	—	

(1)

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Power Supply, VDD/REF	1.2	3.3	3.6	V
T_A	Operating free-air temperature	–40		85	°C

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6.5 Electrical Characteristics

At T_A = –40°C to +85°C, V_{DD} = +1.2V to +3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TSC2014 MIN	TSC2014 TYP	TSC2014 MAX	UNIT
AUXILIARY ANALOG INPUT							
Input voltage range				0		VDD	V
Input capacitance					12		pF
Input leakage current				–1		+1	µA
Full-scale average input current		VDD = 1.6V, continuous AUX			2		µA
A/D CONVERTER							
Resolution		Programmable: 10 or 12 bits				12	Bits
No missing codes		12-bit resolution		11			Bits
Integral linearity				–3	–0.6 to +0.38	+3	LSB(1)
Differential linearity				–2	–0.46 to +0.49	+4	LSB
Offset error		V_{DD} = 1.6V		–5	0.53	+5	LSB
Gain error		V_{DD} = 1.6V		–3	0.32	+3	LSB
TOUCH SENSORS							
$\overline{PENIRQ}$ 50kΩ pull-up resistor, R_{IRQ}		T_A = +25°C, V_{DD} = 1.6V			50		kΩ
X, Y drivers on-resistance	Y+, X+	T_A = +25°C, V_{DD} = 1.6V			6		Ω
	Y–, X–	T_A = +25°C, V_{DD} = 1.6V			4.5		Ω
X, Y drivers drive current(2)		100ms duration				50	mA
INTERNAL TEMPERATURE SENSOR							
Temperature range				–40		+85	°C
Resolution		Differential method(3)	V_{DD} = 1.6V		0.3		°C/LSB
			V_{DD} = 3V		1.6		°C/LSB
		TEMP1(4)	V_{DD} = 1.6V		0.3		°C/LSB
			V_{DD} = 3V		1.6		°C/LSB
Accuracy		Differential method(3)	V_{DD} = 1.6V		±3		°C/LSB
			V_{DD} = 3V		±2		°C/LSB
		TEMP1(4)	V_{DD} = 1.6V		±3		°C/LSB
			V_{DD} = 3V		±2		°C/LSB
INTERNAL OSCILLATOR							
Clock frequency, f_{OSC}		V_{DD} = 1.2V, T_A = +25°C			3.3		MHz
		V_{DD} = 1.6V		3.3	3.82	4.3	MHz
		V_{DD} = 3.0V, T_A = +25°C			4.1		MHz
Frequency drift		V_{DD} = 1.2V			0.121		%/°C
		V_{DD} = 1.6V			–0.013		%/°C
		V_{DD} = 3.0V			–0.028		%/°C

(1) LSB means Least Significant Bit. With V_{REF} = +2.5V, one LSB is 610µV.
(2) Assured by design, but not tested. Exceeding 50mA source current may result in device degradation.
(3) Difference between TEMP1 and TEMP2 measurement; no calibration necessary.
(4) Temperature drift is –2.1mV/°C, TEMP2 drift is –1.7mV/°C.

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Electrical Characteristics (continued)

At T_A = –40°C to +85°C, V_{DD} = +1.2V to +3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TSC2014 MIN	TSC2014 TYP	TSC2014 MAX	UNIT
DIGITAL INPUT/OUTPUT							
Logic family					CMOS		
Logic level	V_{IH}	1.2V ≤ V_{DD} < 1.6V		0.7 × V_{DD}		V_{DD} + 0.3	V
		1.6V ≤ V_{DD} ≤ 3.6V		0.7 × V_{DD}		V_{DD} + 0.3	V
	V_{IL}	1.2V ≤ V_{DD} < 1.6V		–0.3		0.2 × V_{DD}	V
		1.6V ≤ V_{DD} ≤ 3.6V		–0.3		0.3 × V_{DD}	V
	I_{IL}	SCL and SDA pins		–1		1	µA
	C_{IN}	SCL and SDA pins				10	pF
	V_{OH}	I_{OH} = 2 TTL loads		V_{DD} – 0.2		V_{DD}	V
	V_{OL}	I_{OL} = 2 TTL loads		0		0.2	V
	I_{LEAK}	Floating output		–1		1	µA
	C_{OUT}	Floating output				10	pF
Data format					Straight Binary		
POWER-SUPPLY REQUIREMENTS							
Power-supply voltage							
V_{DD}		Specified performance		1.2		3.6	V
Quiescent supply current (5)		Filter off, M = W = 1, C[3:0] = (1,0,0,0), RM = 1, CL[1:0] = (0,1), cont AUX mode, f_{ADC} = 2MHz, without reading data register	V_{DD} = 1.6V		420	570	µA
		T_A = +25°C, filter on, M = 15, W = 7, PSM = 1, C[3:0] = (0,0,0,0), RM = 1, CL[1:0] = (0,1), BTD[2:0] = (1,0,1), 50SSPS, MAVEX = MAVEY = MAVEZ = 1, f_{ADC} = 2MHz, High-Speed mode, sensor drivers supply included(6)	V_{DD} = 1.2V		156		µA
			V_{DD} = 1.6V		200		µA
			V_{DD} = 3.0V		400		µA
		T_A = +25°C, filter off, M = W = 1, PSM = 1, C[3:0] = (0,0,0,0), RM = 1, CL[1:0] = (0,1), BTD[2:0] = (1,0,1), 50SSPS, MAVEX = MAVEY = MAVEZ = 1, f_{ADC} = 2MHz, High-Speed mode, sensor drivers supply included(6)	V_{DD} = 1.2V		140		µA
			V_{DD} = 1.6V		180		µA
			V_{DD} = 3.0V		370		µA
		T_A = +25°C, filter off, M = W = 1, C[3:0] = (0,1,0,1), RM = 1, CL[1:0] = (0,1), non-cont AUX mode, f_{ADC} = 2MHz, High-Speed mode	V_{DD} = 1.2V, ~27.2kSPS effective rate		150		µA
			V_{DD} = 1.6V, ~28.6kSPS effective rate		200		µA
			V_{DD} = 3.0V, ~29.1kSPS effective rate		390		µA
		T_A = +25°C, filter on, M = 7, W = 3, C[3:0] = (0,1,0,1), RM = 1, CL[1:0] = (0,1), MAVEAUX = 1, non-cont AUX mode, f_{ADC} = 2MHz, High-Speed mode, full speed	V_{DD} = 1.2V, ~10.3kSPS effective rate		272		µA
			V_{DD} = 1.6V, ~11.8kSPS effective rate		365		µA
			V_{DD} = 3.0V, ~12.3kSPS effective rate		683		µA
		T_A = +25°C, filter on, M = 7, W = 3, C[3:0] = (0,1,0,1), RM = 1, CL[1:0] = (0,1), MAVEAUX = 1, non-cont AUX mode, f_{ADC} = 2MHz, High-Speed mode, reduced speed (8.2kSPS equivalent rate)	V_{DD} = 1.2V, ~1.17kSPS effective rate		30.9		µA
			V_{DD} = 1.6V, ~1.17kSPS effective rate		36.2		µA
			V_{DD} = 3.0V, ~1.17kSPS effective rate		64.9		µA
Power-down supply current		T_A = +25°C, Not addressed, SCL = SDA = 1, V_{DD} = 1.6V, $\overline{RESET}$ = 1, $\overline{PINTDAV}$ = 1			0.023	0.8	µA

(5) For detailed information on test condition parameter and bit settings, see the *Digital Interface* section.
(6) Touch sensor modeled by: 2kΩ for X-plane and Y-plane, and 1kΩ for Z (touch resistance).

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6.6 Timing Requirements for Figure 1: I²C Standard Mode (f_{SCL} = 100 kHz)

All specifications typical at –40°C to +85°C, V_{DD} = +1.2V to +3.6V, unless otherwise noted.

TWO-WIRE STANDARD MODE PARAMETERS		TEST CONDITIONS	MIN	MAX	UNIT
Reset low time(1)	$t_{WL(RESET)}$	$V_{DD} \geq 1.6V$	10		µs
		$1.2V \leq V_{DD} < 1.6V$	13		µs
SCL clock frequency	f_{SCL}			100	kHz
Bus free time between a STOP and START condition	t_{BUF}		4.7		µs
Hold time (repeated) START condition	$t_{HD, STA}$		4.0		µs
Low period of SCL clock	t_{LOW}		4.7		µs
High period of the SCL clock	t_{HIGH}		4.0		µs
Setup time for a repeated START condition	$t_{SU, STA}$		4.7		µs
Data hold time	$t_{HD, DAT}$		0	3.45	µs
Data setup time	$t_{SU, DAT}$		250		ns
Rise time of both SDA and SCL signals	t_R	C_b = total bus capacitance		1000	ns
Fall time of both SDA and SCL signals	t_F	C_b = total bus capacitance		300	ns
Setup time for STOP condition	$t_{SU, STO}$		4.0		µs
Capacitive load for each bus line	C_b	C_b = total capacitance of one bus line in pF		400	pF
Pulse width of spike suppressed	t_{SP}		N/A	N/A	ns

(1) Refer to Figure 36.

6.7 Timing Requirements for Figure 1: I²C Fast Mode (f_{SCL} = 400 kHz)

All specifications typical at –40°C to +85°C, V_{DD} = +1.2V to +3.6V, unless otherwise noted.

TWO-WIRE FAST MODE PARAMETERS		TEST CONDITIONS	MIN	MAX	UNIT
Reset low time(1)	$t_{WL(RESET)}$	$V_{DD} \geq 1.6V$	10		µs
		$1.2V \leq V_{DD} < 1.6V$	13		µs
SCL clock frequency	f_{SCL}			400	kHz
Bus free time between a STOP and START condition	t_{BUF}		1.3		µs
Hold time (repeated) START condition	$t_{HD, STA}$		0.6		µs
Low period of SCL clock	t_{LOW}		1.3		µs
High period of the SCL clock	t_{HIGH}		0.6		µs
Setup time for a repeated START condition	$t_{SU, STA}$		0.6		µs
Data hold time	$t_{HD, DAT}$		0	0.9	µs
Data setup time	$t_{SU, DAT}$		100		ns
Rise time of both SDA and SCL signals	t_R	C_b = total bus capacitance	$20 + 0.1 \times C_b$	300	ns
Fall time of both SDA and SCL signals(2)	t_F	C_b = total bus capacitance	$20 + 0.1 \times C_b$	300	ns
Setup time for STOP condition	$t_{SU, STO}$		0.6		µs
Capacitive load for each bus line	C_b	C_b = total capacitance of one bus line in pF		400	pF
Pulse width of spike suppressed	t_{SP}		0	50	ns

(1) Refer to Figure 36.
(2) C_b = the total capacitance of one bus line in pF. If using both Fast mode and Hs-mode devices, faster fall times according to the 3.4MHz High-Speed Mode table are allowed. Note that the TSC2014 is a Hs-mode device and follows the I²C, 3.4MHz, High-Speed Mode table requirements.

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6.8 Timing Requirements for Figure 2: I²C High-Speed Mode (f_{SCL} = 1.7 MHz)

All specifications typical at –40°C to +85°C, V_{DD} = +1.2V to +3.6V, unless otherwise noted.

TWO-WIRE HIGH-SPEED MODE PARAMETERS		TEST CONDITIONS	MIN	MAX	UNIT
Reset low time(1)	$t_{WL(RESET)}$	$V_{DD} \geq 1.6V$	10		µs
		$1.2V \leq V_{DD} < 1.6V$	13		µs
SCL clock frequency	f_{SCL}			1.7	MHz
Hold time (repeated) START condition	$t_{HD, STA}$		160		ns
Low period of SCL clock	t_{LOW}		320		ns
High period of the SCL clock	t_{HIGH}		120		ns
Setup time for a repeated START condition	$t_{SU, STA}$		160		ns
Data hold time	$t_{HD, DAT}$		0	150	ns
Data setup time	$t_{SU, DAT}$		10		ns
Rise time of SCL signal	t_{RCL}	C_b = total bus capacitance(2)	20	80	ns
Rise time of SDA signal	t_{RDA}	C_b = total bus capacitance(2)	20	160	ns
Fall time of SCL signal	t_{FCL}	C_b = total bus capacitance(2)	20	80	ns
Fall time of SDA signal	t_{FDA}	C_b = total bus capacitance(2)	1	160	ns
Rise time of SCL signal after a repeated START condition and after an acknowledge bit	t_{RCL1}	C_b = total bus capacitance(2)	20	160	ns
Setup time for STOP condition	$t_{SU, STO}$		160		ns
Capacitive load for each bus line	C_b	C_b = total capacitance of one bus line in pF		400	pF
Pulse width of spike suppressed	t_{SP}		0	10	ns

(1) Refer to Figure 36.
(2) For capacitive bus loads between 100pF and 400pF, the rise and fall time values must be linearly interpolated.

6.9 Timing Requirements for Figure 2: I²C High-Speed Mode (f_{SCL} = 3.4 MHz)

All specifications typical at –40°C to +85°C, V_{DD} = +1.2V(1) to +3.6V, unless otherwise noted.

TWO-WIRE HIGH-SPEED MODE PARAMETERS		TEST CONDITIONS	MIN	MAX	UNIT
Reset low time(2)	$t_{WL(RESET)}$	$V_{DD} \geq 1.6V$	10		µs
		$1.2V \leq V_{DD} < 1.6V$	13		µs
SCL clock frequency	f_{SCL}			3.4	MHz
Hold time (repeated) START condition	$t_{HD, STA}$		160		ns
Low period of SCL clock	t_{LOW}		160		ns
High period of the SCL clock	t_{HIGH}		60		ns
Setup time for a repeated START condition	$t_{SU, STA}$		160		ns
Data hold time	$t_{HD, DAT}$		0	70	ns
Data setup time	$t_{SU, DAT}$		10		ns
Rise time of SCL signal	t_{RCL}	C_b = total bus capacitance(3)	10	40	ns
Rise time of SDA signal	t_{RDA}	C_b = total bus capacitance(3)	10	80	ns
Fall time of SCL signal	t_{FCL}	C_b = total bus capacitance(3)	10	40	ns
Fall time of SDA signal	t_{FDA}	C_b = total bus capacitance(3)	1	80	ns
Rise time of SCL signal after a repeated START condition and after an acknowledge bit	t_{RCL1}	C_b = total bus capacitance(3)	10	80	ns
Setup time for STOP condition	$t_{SU, STO}$		160		ns
Capacitive load for each bus line	C_b	C_b = total capacitance of one bus line in pF		100	pF
Pulse width of spike suppressed	t_{SP}		0	10	ns

(1) Because of the low supply voltage of 1.2V and the wide temperature range of –40°C to +85°C, the I²C system devices may not reach the maximum specification of I²C High-Speed mode, and f_{SCL} may not reach 3.4MHz.
(2) Refer to Figure 36.
(3) Capacitive load from 10pF to 100pF.

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6.10 Timing Information

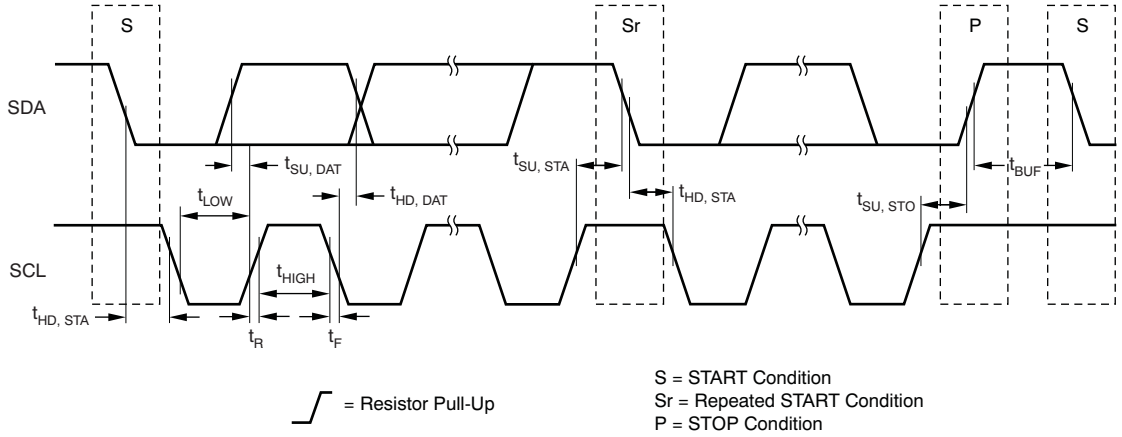
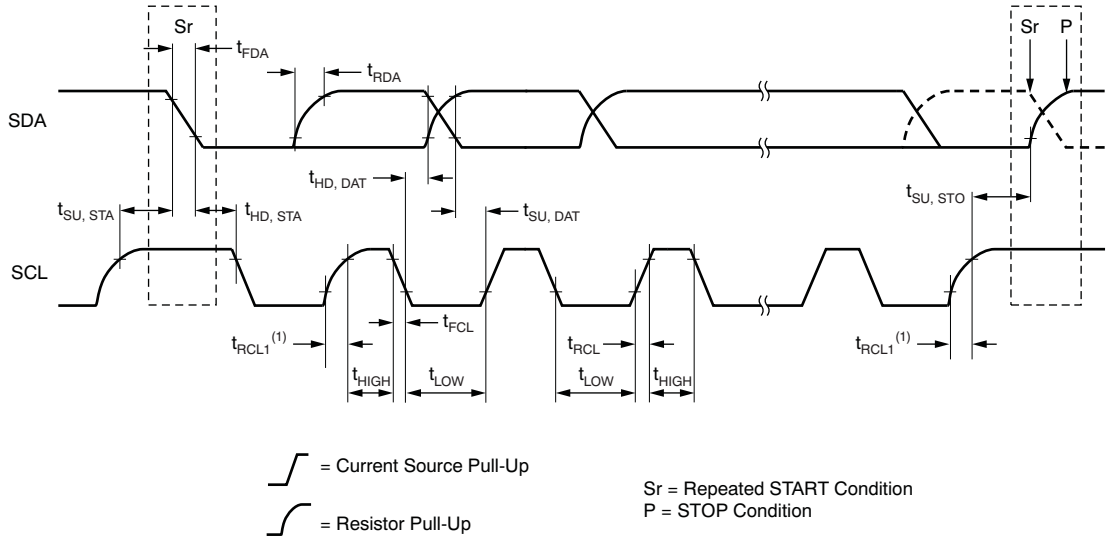


Figure 1. Detailed I/O Timing for Standard and Fast Modes



NOTE: (1) First rising edge of the SCL signal after Sr and after each acknowledge bit.

Figure 2. Detailed I/O Timing for High-Speed Mode

6.11 Typical Characteristics

At T_A = –40°C to +85°C, V_{DD} = +1.2V to +3.6V, f_{ADC} = f_{OSC}/2,High-Speed mode (f_{SCL} = 3.4MHz), 12-bit mode, and non-continuous AUX measurement, unless otherwise noted.

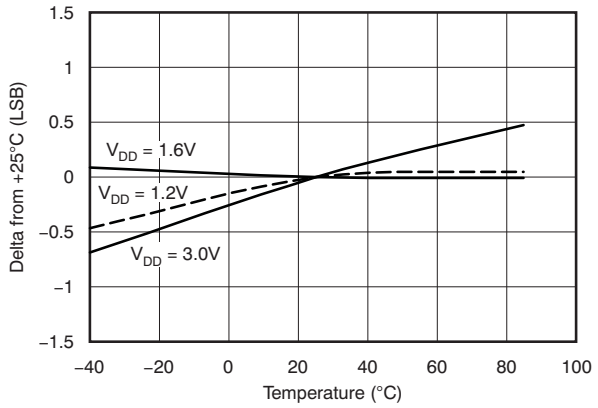


Figure 3. Change in Offset vs Temperature

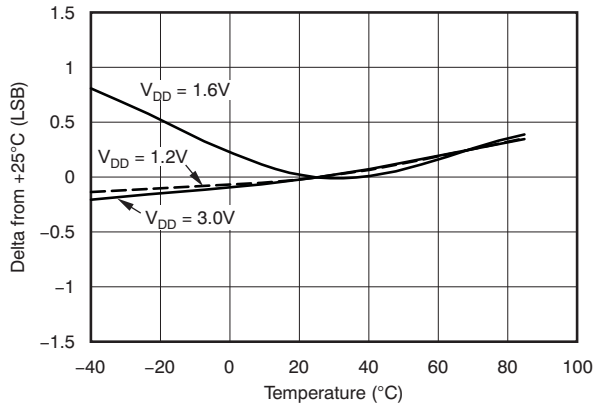


Figure 4. Change in Gain vs Temperature

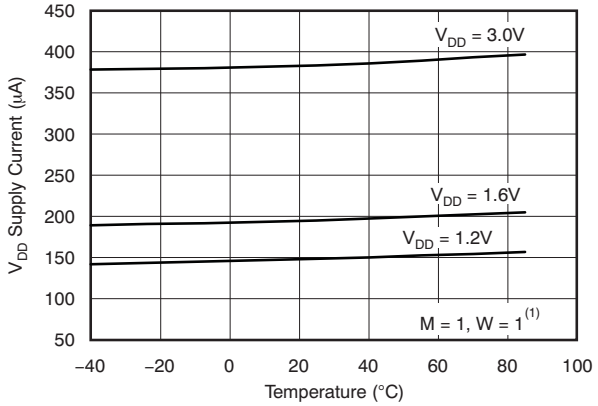


Figure 5. V_{DD} Supply Current vs Temperature

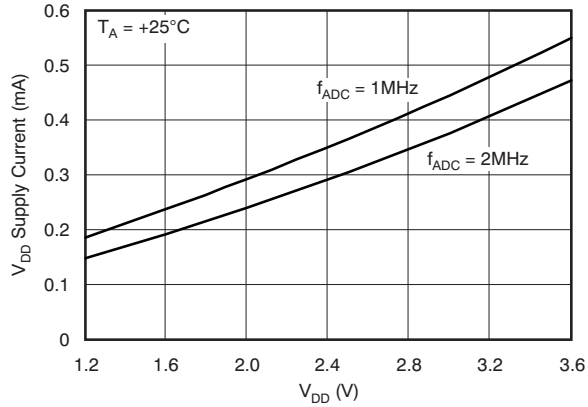


Figure 6. V_{DD} Supply Current vs V_{DD} Supply Voltage

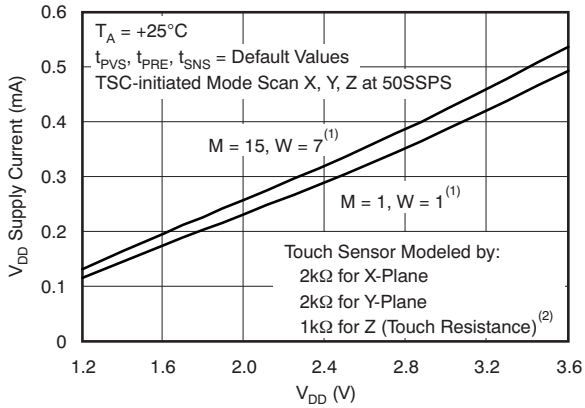


Figure 7. V_{DD} Supply Current vs V_{DD} Supply Voltage

1. See Table 1.
2. See Figure 17.

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Typical Characteristics (continued)

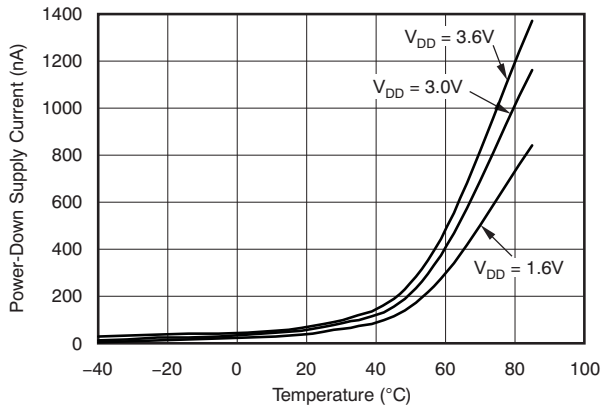

Figure 8. Power-down Supply Current vs Temperature

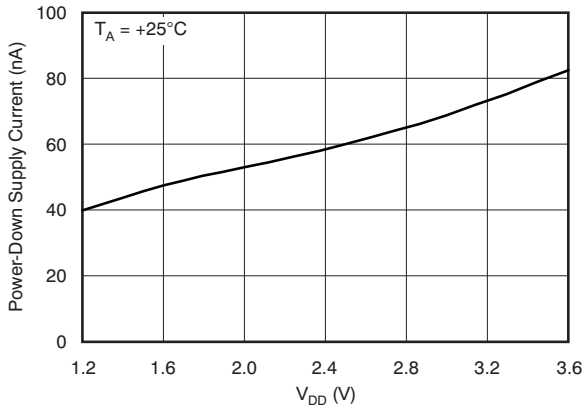

Figure 9. Power-down Supply Current vs V_{DD}

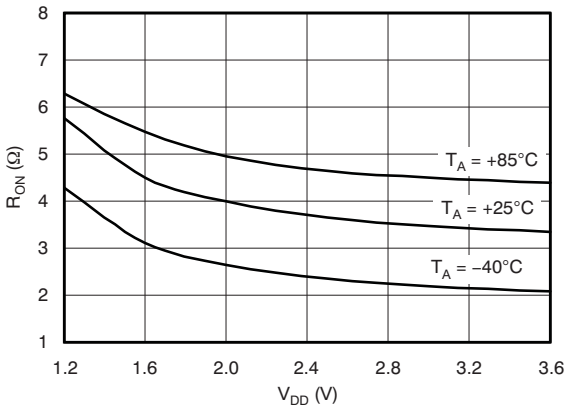

Figure 10. Switch-on Resistance (X_N, Y_N) vs V_{DD} Supply Voltage

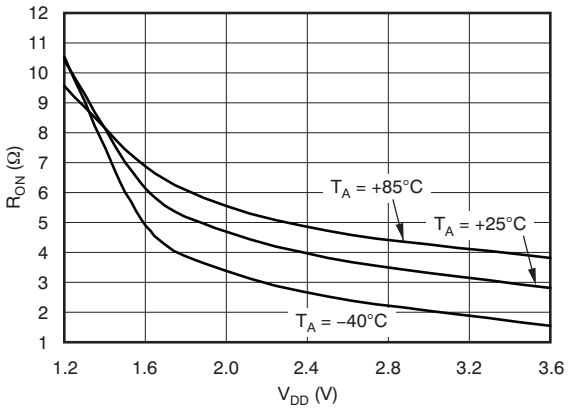

Figure 11. Switch-on Resistance (X_P, Y_P) vs V_{DD} Supply Voltage

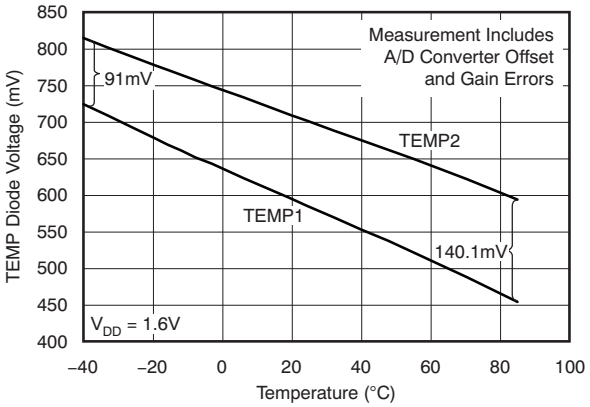

Figure 12. Temp Diode Voltage vs Temperature

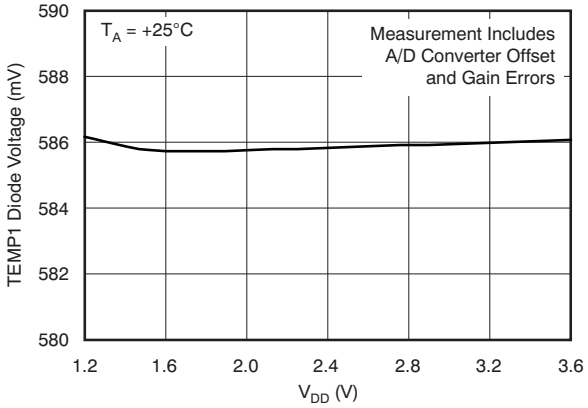

Figure 13. TEMP1 Diode Voltage vs V_{DD} Supply Voltage

Typical Characteristics (continued)

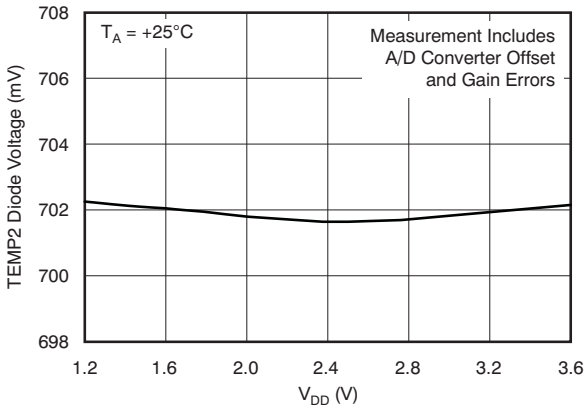

Figure 14. TEMP2 Diode Voltage vs V_{DD} Supply Voltage

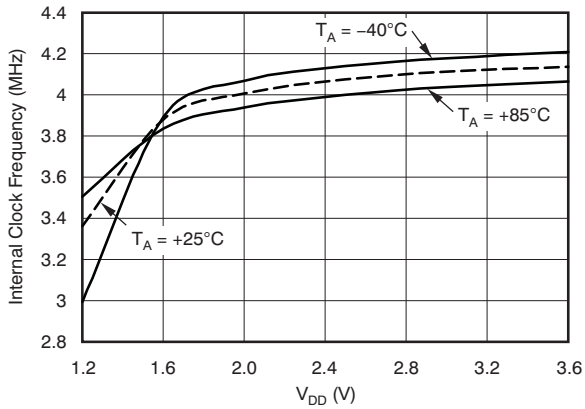

Figure 15. Internal Oscillator Clock Frequency vs V_{DD} Supply Voltage

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7 Detailed Description

7.1 Overview

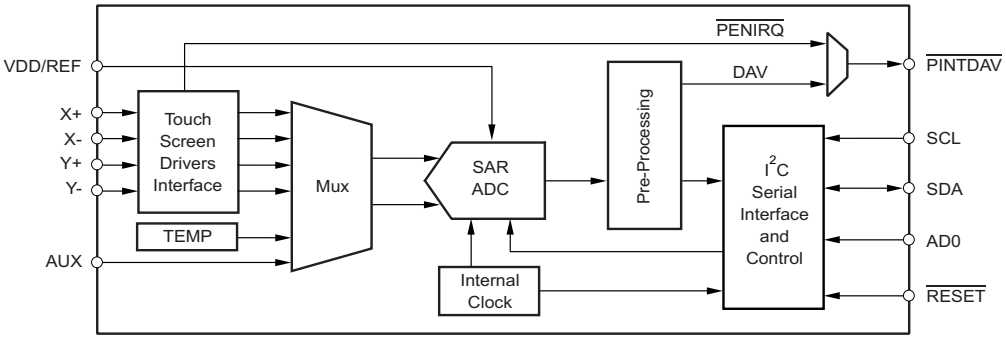
The TSC2014 is an analog interface circuit for a human interface touch screen device. A register-based architecture eases integration with microprocessor-based systems through a standard I^2C bus. All peripheral functions are controlled through the registers and onboard state machines. The TSC2014 features include:

- Very low-power touch screen controller
- Very small onboard footprint
- Relieves host from tedious routine tasks by flexible preprocessing, saving resources for more critical tasks
- Ability to work on very low supply voltage
- Minimal connection interface allows easiest isolation and reduces the number of dedicated I/O pins required
- Miniature, yet complete; requires no external supporting component.
- Enhanced ESD protection

The TSC2014 consists of the following blocks (refer to the block diagram.

- Touch Screen Interface
- Auxiliary Input (AUX)
- Temperature Sensor
- Acquisition Activity Preprocessing
- Internal Conversion Clock
- I^2C Interface

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Touch Screen Operation

A resistive touch screen operates by applying a voltage across a resistor network and measuring the change in resistance at a given point on the matrix where the screen is touched by an input (stylus, pen, or finger). The change in the resistance ratio marks the location on the touch screen.

The TSC2014 supports the resistive 4-wire configurations, as shown in Figure 16. The circuit determines location in two coordinate pair dimensions, although a third dimension can be added for measuring pressure.

Feature Description (continued)

7.3.2 4-Wire Touch Screen Coordinate Pair Measurement

A 4-wire touch screen is typically constructed as shown in Figure 16. It consists of two transparent resistive layers separated by insulating spacers.

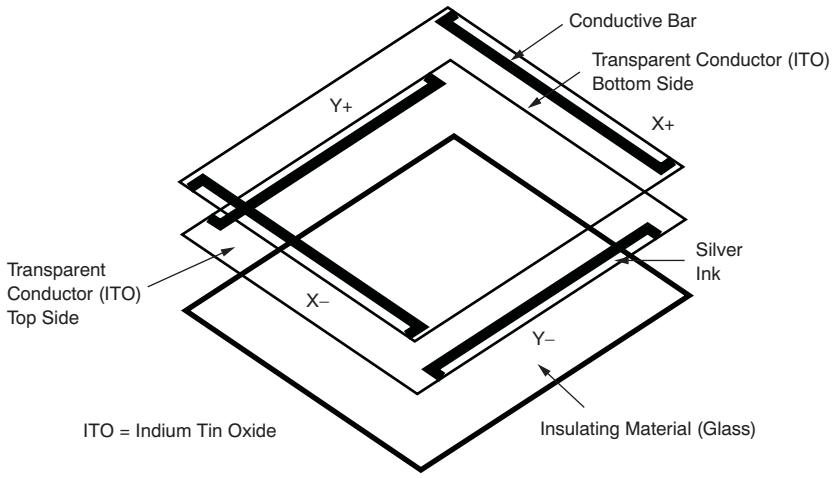

Figure 16. 4-Wire Touch Screen Construction

The 4-wire touch screen panel works by applying a voltage across the vertical or horizontal resistive network. The A/D converter converts the voltage measured at the point where the panel is touched. A measurement of the Y position of the pointing device is made by connecting the X+ input to a data converter chip, turning on the Y+ and Y– drivers, and digitizing the voltage seen at the X+ input. The voltage measured is determined by the voltage divider developed at the point of touch. For this measurement, the horizontal panel resistance in the X+ lead does not affect the conversion because of the high input impedance of the A/D converter.

Voltage is then applied to the other axis, and the A/D converter converts the voltage representing the X position on the screen. This process provides the X and Y coordinates to the associated processor.

Measuring touch pressure (Z) can also be done with the TSC2014. To determine pen or finger touch, the pressure of the *touch* must be determined. Generally, it is not necessary to have very high performance for this test; therefore, 10-bit resolution mode is recommended (however, data sheet calculations are shown using the 12-bit resolution mode). There are several different ways of performing this measurement. The TSC2014 supports two methods. The first method requires knowing the X-plate resistance, the measurement of the X-Position, and two additional cross panel measurements (Z_2 and Z_1) of the touch screen (see Figure 17). Equation 1 calculates the touch resistance:

$$R_{TOUCH} = R_{X-plate} \cdot \frac{X_{Position}}{4096} \left(\frac{Z_2}{Z_1} - 1 \right) \tag{1}$$

The second method requires knowing both the X-plate and Y-plate resistance, measurement of X-Position and Y-Position, and Z_1. Equation 2 also calculates the touch resistance:

$$R_{TOUCH} = \frac{R_{X-plate} \cdot X_{Position}}{4096} \left(\frac{4096}{Z_1} - 1 \right) - R_{Y-plate} \cdot \left(1 - \frac{Y_{POSITION}}{4096} \right) \tag{2}$$

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Feature Description (continued)

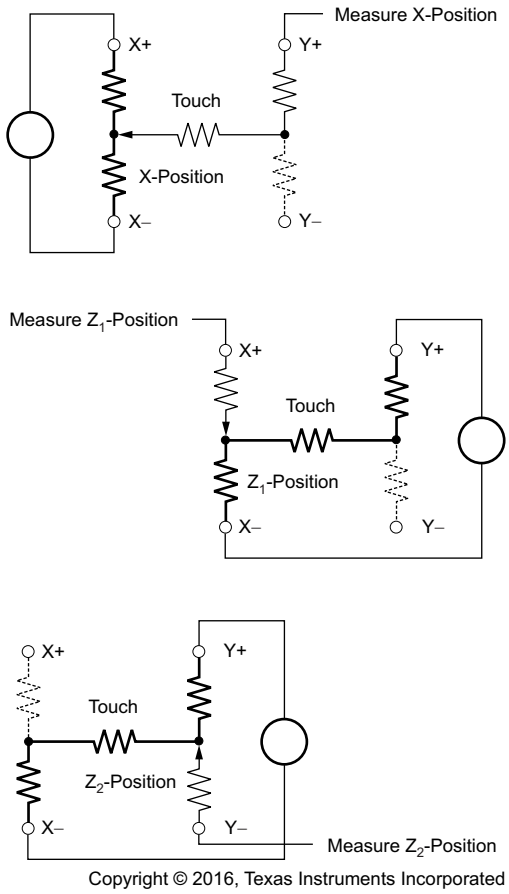

Figure 17. Pressure Measurement

When the touch panel is pressed or touched and the drivers to the panel are turned on, the voltage across the touch panel often overshoots and then slowly settles down (decays) to a stable dc value. This effect is a result of mechanical bouncing caused by vibration of the top layer sheet of the touch panel when the panel is pressed. This settling time must be accounted for, or else the converted value will be in error. Therefore, a delay must be introduced between the time the driver for a particular measurement is turned on, and the time a measurement is made.

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen (for example, noise generated by the LCD panel or back-light circuitry). The value of these capacitors provides a low-pass filter to reduce the noise, but will cause an additional settling time requirement when the panel is touched.

The TSC2014 offers several solutions to this problem. A programmable delay time is available that sets the delay between turning the drivers on and making a conversion. This delay is referred to as the *panel voltage stabilization time*, and is used in some of the TSC2014 modes. In other modes, the TSC2014 can be commanded to turn on the drivers only without performing a conversion. Time can then be allowed before the command is issued to perform a conversion.

The TSC2014 touch screen interface can measure position (X,Y) and pressure (Z). Determination of these coordinates is possible under three different modes of the A/D converter:

- TSMode1 — conversion controlled by the TSC2014 initiated by the TSC;
- TSMode2 — conversion controlled by the TSC2014 initiated by the host responding to the $\overline{\text{PENIRQ}}$ signal; or
- TSMode3 — conversion completely controlled by the host processor.

Feature Description (continued)

7.3.3 Internal Temperature Sensor

In some applications, such as battery recharging, an ambient temperature measurement is required. The temperature measurement technique used in the TSC2014 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage (V_{BE}) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the +25°C value of the V_{BE} voltage and then monitoring the delta of that voltage as the temperature changes.

The TSC2014 offers two modes of temperature measurement. The first mode requires calibration at a known temperature, but only requires a single reading to predict the ambient temperature. The TEMP1 diode, shown in Figure 18, is used during this measurement cycle. This voltage is typically 580mV at +25°C with a 10µA current. The absolute value of this diode voltage can vary by a few millivolts; the temperature coefficient (T_C) of this voltage is very consistent at –2.1mV/°C. During the final test of the end product, the diode voltage is stored at a known room temperature, in system memory, for calibration purposes by the user. The result is an equivalent temperature measurement resolution of 0.3°C/LSB (1LSB = 610µV with V_{REF} = 2.5V).

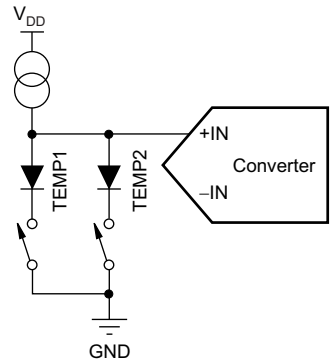

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Figure 18. Functional Block Diagram of Temperature Measurement Mode

The second mode does not require a test temperature calibration, but uses a two-measurement (differential) method to eliminate the need for absolute temperature calibration and for achieving 2°C/LSB accuracy. This mode requires a second conversion of the voltage across the TEMP2 diode with a resistance 91 times larger than the TEMP1 diode. The voltage difference between the first (TEMP1) and second (TEMP2) conversion is represented by:

$$\Delta V = \frac{kT}{q} \cdot \ln(N) \tag{3}$$

Where:

N = the resistance ratio = 91.
k = Boltzmann's constant = 1.3807×10^{-23} J/K (joules/kelvins).
q = the electron charge = 1.6022×10^{-19} C (coulombs).
T = the temperature in kelvins (K).

This method can provide much improved absolute temperature measurement, but a lower resolution of 1.6°C/LSB. The resulting equation to solve for T is:

$$T = \frac{q \cdot \Delta V}{k \cdot \ln(N)} \tag{4}$$

Where:

$\Delta V = V_{BE}$ (TEMP2) – V_{BE}(TEMP1) (in mV).
$\therefore T = 2.573 \cdot \Delta V$ (in K),
or $T = 2.573 \cdot \Delta V - 273$ (in °C).

Temperature 1 and/or temperature 2 measurements have the same timing as Figure 46.

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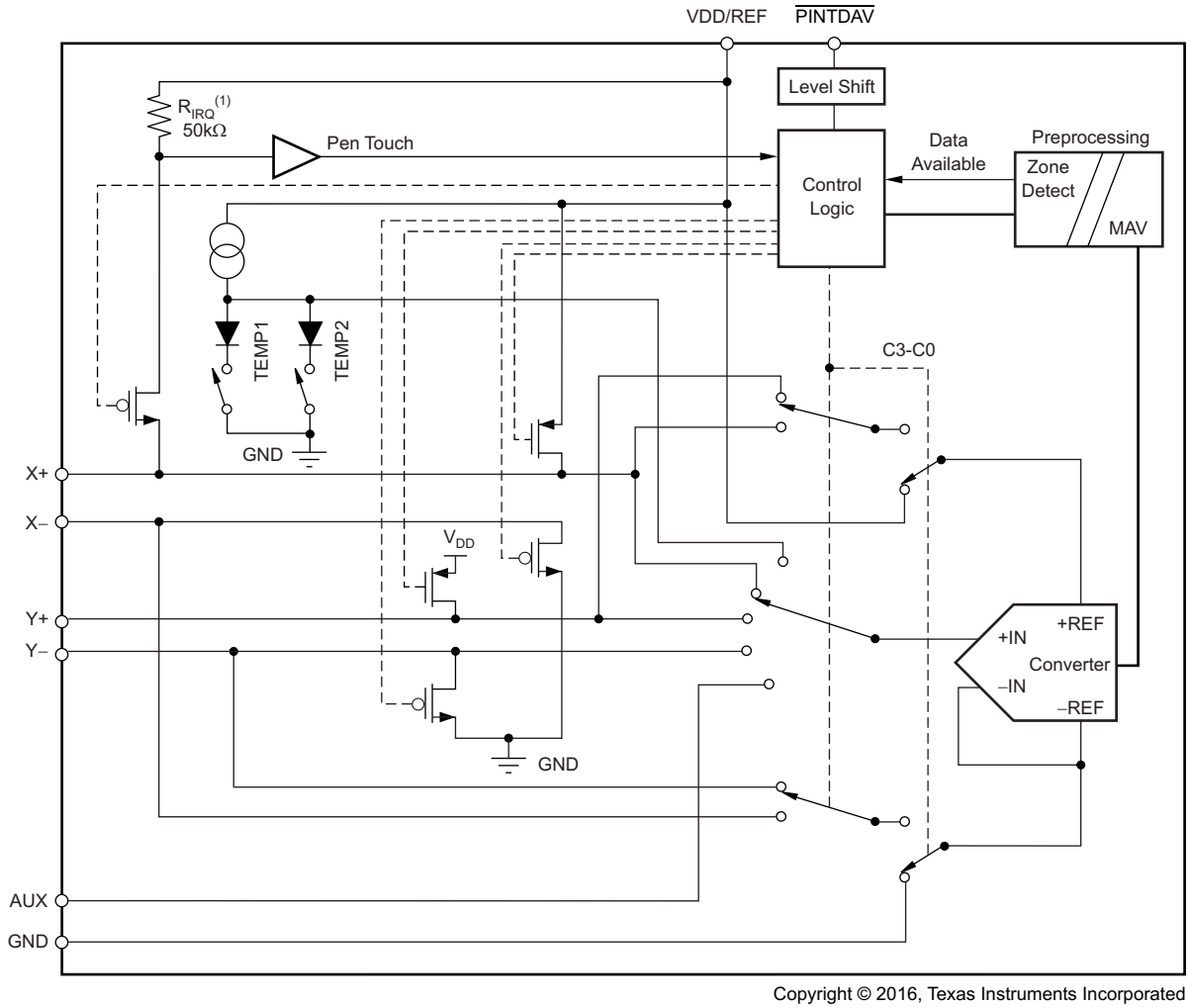
Feature Description (continued)

7.3.4 Analog-to-Digital Converter

Figure 19 shows the analog inputs of the TSC2014. The analog inputs (X, Y, and Z touch panel coordinates, chip temperature and auxiliary inputs) are provided via a multiplexer to the Successive Approximation Register (SAR) Analog-to-Digital (A/D) converter. The A/D architecture is based on capacitive redistribution architecture, which inherently includes a sample-and-hold function.



(1) Untrimmed resistor; see the typical value in the *Electrical Characteristics*

Figure 19. Simplified Diagram of the Analog Input Section

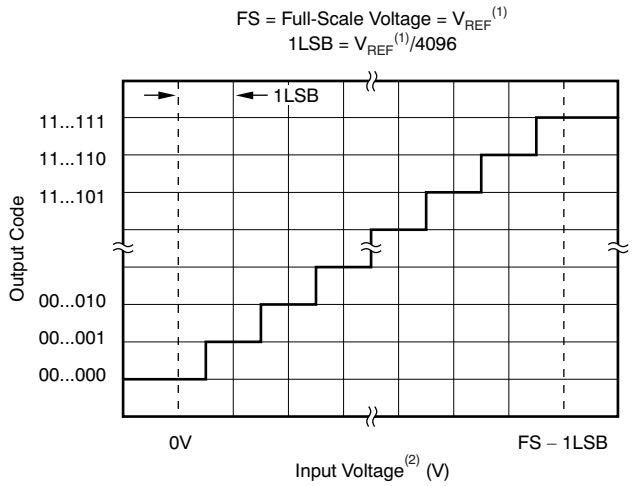
A unique configuration of low on-resistance switches allows an unselected A/D converter input channel to provide power and an accompanying pin to provide ground for driving the touch panel. By maintaining a differential input to the converter and a differential reference input architecture, it is possible to negate errors caused by the driver switch on-resistances.

The A/D converter is controlled by two A/D Converter Control registers. Several modes of operation are possible, depending on the bits set in the control registers. Channel selection, scan operation, preprocessing, resolution, and conversion rate may all be programmed through these registers. These modes are outlined in the sections that follow for each type of analog input. The conversion results are stored in the appropriate result register.

Feature Description (continued)

7.3.4.1 Data Format

The TSC2014 output data are in Straight Binary format as shown in Figure 20. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



(1) Reference voltage at converter: +REF – (–REF). See Figure 19.

(2) Input voltage at converter, after multiplexer: +IN – (–IN). See Figure 19.

Figure 20. Ideal Input Voltages and Output Codes

7.3.4.2 Reference

The TSC2014 uses an external voltage reference that applied to the VREF pin. It is possible to use V_{DD} as the reference voltage because the upper reference voltage range is the same as the supply voltage range.

7.3.4.3 Variable Resolution

The TSC2014 provides either 10-bit or 12-bit resolution for the A/D converter. Lower resolution is often practical for measuring slow changing signals such as touch pressure. Performing the conversions at lower resolution reduces the amount of time it takes for the A/D converter to complete its conversion process, which also lowers power consumption.

7.3.4.4 Conversion Clock and Conversion Time

The TSC2014 contains an internal clock (oscillator) that drives the internal state machines that perform the many functions of the part. This clock is divided down to provide a conversion clock for the A/D converter. The division ratio for this clock is set in the A/D Converter Control register (see Table 14). The ability to change the conversion clock rate allows the user to choose the optimal values for resolution, speed, and power dissipation. If the 4MHz (oscillator) clock is used directly as the A/D converter clock (when CL[1:0] = (0,0)), the A/D converter resolution is limited to 10 bits. Using higher resolutions at this speed does not result in more accurate conversions. 12-bit resolution requires that CL[1:0] is set to (0,1) or (1,0).

Regardless of the conversion clock speed, the internal clock runs nominally at 3.8MHz at a 3V supply (V_{DD}) and slows down to 3.6MHz at a 1.6V supply. The conversion time of the TSC2014 depends on several functions. While the conversion clock speed plays an important role in the time it takes for a conversion to complete, a certain number of internal clock cycles are needed for proper sampling of the signal. Moreover, additional times (such as the panel voltage stabilization time), can add significantly to the time it takes to perform a conversion. Conversion time can vary depending on the mode in which the TSC2014 is used. Throughout this data sheet, internal and conversion clock cycles are used to describe the amount of time that many functions take. These times must be taken into account when considering the total system design.

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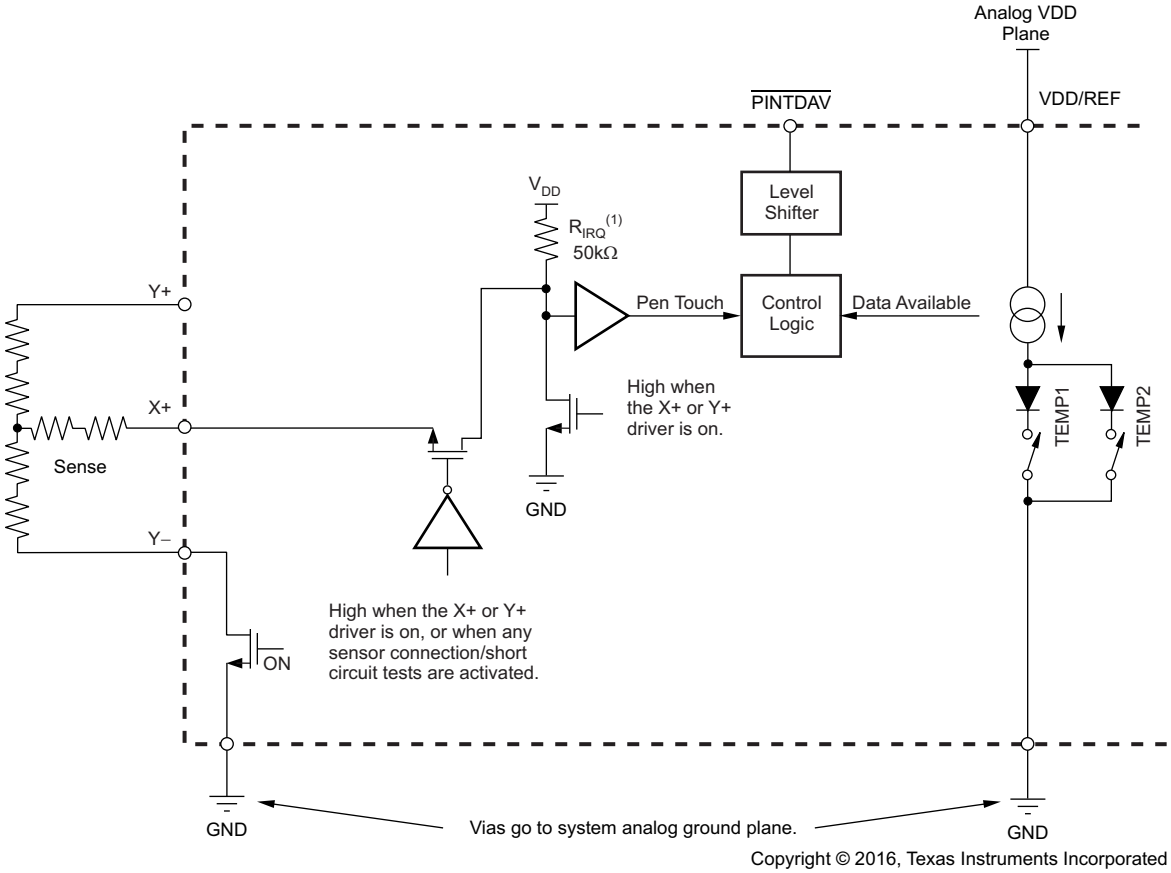
Feature Description (continued)

7.3.4.5 Touch Detect

$\overline{\text{PINTDAV}}$ can be programmed to generate an interrupt to the host. Figure 21 details an example for the Y-position measurement. While in the power-down mode, the Y– driver is on and connected to GND. The internal pen-touch signal depends on whether or not the X+ input is driven low. When the panel is touched, the X+ input is pulled to ground through the touch screen and the internal pen-touch output is set to low because of the detection on the current path through the panel to GND, which initiates an interrupt to the processor. During the measurement cycles for X- and Y-Position, the X+ input is disconnected, which eliminates any leakage current from the pull-up resistor to flow through the touch screen, thus causing no errors.



(1) Untrimmed resistor; see the typical value in the *Electrical Characteristics*

Figure 21. Example of a Pen-Touch Induced Interrupt via the $\overline{\text{PINTDAV}}$ Pin

In modes where the TSC2014 must detect whether or not the screen is still being touched (for example, when doing a pen-touch initiated X, Y, and Z conversion), the TSC2014 must reset the drivers so that the R_{IRQ} resistor is connected again. Because of the high value of this pull-up resistor, any capacitance on the touch screen inputs causes a long delay time, and may prevent the detection from occurring correctly. To prevent this possible delay, the TSC2014 has a circuit that allows any screen capacitance to be *precharged*, so that the pull-up resistor does not have to be the only source for the charging current. The time allowed for this precharge, as well as the time needed to sense if the screen is still touched, can be set in the configuration register.

This configuration underscores the need to use the minimum possible capacitor values on the touch screen inputs. These capacitors may be needed to reduce noise, but too large a value will increase the needed precharge and sense times, as well as the panel voltage stabilization time.

Feature Description (continued)

7.3.4.6 Preprocessing

The TSC2014 offers an array of powerful preprocessing operations that reduce unnecessary traffic on the bus and reduce the host processor loading. This reduction is especially critical for the serial interface, where limited bandwidth is a tradeoff, keeping the connection lines to a minimum.

All data acquisition tasks are looking for specific data that meet certain criteria. Many of these tasks fall into a predefined range, while other tasks may be looking for a value in a noisy environment. If these data are all to be retrieved by host processor for processing, the limited bus bandwidth quickly saturates, along with the host processor processing capability. In any case, the host processor must always be reserved for more critical tasks, not for routine work.

The preprocessing unit consists of two main functions: the combined MAV filter (median value filter and averaging filter), followed by the zone detection.

7.3.4.6.1 Preprocessing—Median Value Filter and Averaging Value Filter

The first preprocessing function, a combined MAV filter, can be operated independently as a median value filter (MVF), an averaging value filter (AVF), and a combined filter (MAVF).

If the acquired signal source is noisy because of the digital switching circuit, it may be necessary to evaluate the data without noise. In this case, the median value filter (MVF) operation helps to discard the noise. The array of *N* converted results is first sorted. The return value is either the middle (median value) of an array of *M* converted results, or the average value of a window size of *W* of converted results:

- N = the total number of converted results used by the MAV filter
- M = the median value filter size programmed
- W = the averaging window size programmed

If M = 1, then N = W. A special case is W = 1, which means the MAVF is bypassed. Otherwise, if W > 1, only averaging is performed on these converted results. In either case, the return value is the averaged value of window size W of converted results. If M > 1 and W = 1, then N = M, meaning only the median value filter is operating. The return value is the middle position converted result from the array of M converted results. If M > 1 and W > 1, then N = M. In this case, W < M. The return value is the averaged value of middle portion W of converted results out of the array of M converted results. Since the value of W is an odd number in this case, the averaging value is calculated with the middle position converted result counted twice (so a total of W + 1 converted results are averaged).

Table 1. Median Value Filter Size Selection

M1	M0	MEDIAN VALUE FILTER M =	POSSIBLE AVERAGING WINDOW SIZE W =
0	0	1	1, 4, 8, 16
0	1	3	1
1	0	7	1, 3
1	1	15	1, 3, 7

Table 2. Averaging Value Filter Size Selection

W1	W0	AVERAGING VALUE FILTER SIZE SELECTION W =	
		M = 1 (Averaging Only)	M > 1
0	0	1	1
0	1	4	3
1	0	8	7
1	1	16	Reserved

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NOTE

The default setting for MAVF is MVF (median value filter with averaging bypassed) for any invalid configuration. For example, if (M1, M0, W1, W0) = (1,0,1,0), the MAVF performs as it was configured for (1,0,0,0), median filter only with filter size = 7 and no averaging. The only exception is M > 1 and (W1, W0) = (1,1). This setting is reserved and should not be used.

Table 3. Combined MAV Filter Setting

M	W	INTERPRETATION	N =	OUTPUT
= 1	= 1	Bypass both MAF and AVF	W	The converted result
= 1	> 1	Bypass MVF only	W	Average of W converted results
> 1	= 1	Bypass AVF only	M	Median of M converted results
> 1	> 1	M > W	M	Average of middle W of M converted results with the median counted twice

The MAV filter is available for all analog inputs including the touch screen inputs, temperature measurements TEMP1 and TEMP2, and the AUX measurement.

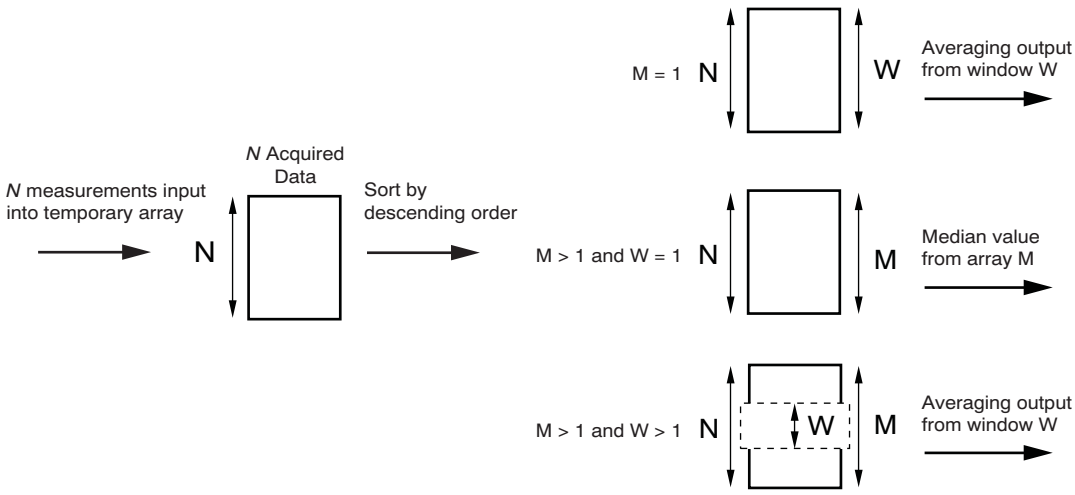

Figure 22. MAV Filter Operation (patent pending)

7.3.4.7 Zone Detection

The Zone Detection unit is capable of screening all processed data from the MAVF and retaining only the data of interest (data that fit the prerequisite). This unit can be programmed to send an alert if a predefined condition set by two threshold value registers is met. Three different zones may be set:

1. Above the upper limit (X ≥ Threshold High)
2. Between the two thresholds (Threshold Low < X < Threshold High)
3. Below the lower limit (X ≤ Threshold Low)

The AUX and temperatures TEMP1 and TEMP2 have separate threshold value registers that can be enabled or disabled. This function is not available to the touch screen inputs. Once the preset condition is met, the $\overline{DAV}$ output to the $\overline{PINTDAV}$ pin is pulled low and the corresponding DAV bit is set.

7.4 Device Functional Modes

7.4.1 I²C Interface

The TSC2014 supports the I²C serial bus and data transmission protocol in all three defined modes: standard, fast, and high-speed. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a *master*. Devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The TSC2014 operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O lines, SDA and SCL.

The following bus protocol has been defined (see Figure 23):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy Both data and clock lines remain HIGH.

Start Data Transfer A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit.

Within the I²C bus specifications, a standard mode (100kHz clock rate), a fast mode (400kHz clock rate), and a high-speed mode (3.4MHz clock rate) are each defined. The TSC2014 works in all three modes.

Acknowledge Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

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Device Functional Modes (continued)

Figure 23 details how data transfer is accomplished on the I^{2}C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
2. **Data transfer from a slave transmitter to a master receiver.** The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer ends with a STOP condition or a repeated START condition. Because a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The TSC2014 may operate in the following two modes:

1. **Slave Receiver Mode**: Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2. **Slave Transmitter Mode**: The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit indicates that the transfer direction is reversed. Serial data are transmitted on SDA by the TSC2014 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

7.4.1.1 I^{2}C Fast or Standard Mode (F/S Mode)

In I^{2}C Fast or Standard (F/S) mode, serial data transfer must meet the timing shown in the Timing Information section.

In the serial transfer format of F/S mode, the master signals the beginning of a transmission to a slave with a START condition (S), which is a high-to-low transition on the SDA input while SCL is high. When the master has finished communicating with the slave, the master issues a STOP condition (P), which is a low-to-high transition on SDA while SCL is high, as shown in Figure 23. The bus is free for another transmission after a stop condition has occurred. Figure 23 shows the complete F/S mode transfer on the I^{2}C, two-wire serial interface. The address byte, control byte, and data byte are transmitted between the START and STOP conditions. The SDA state is only allowed to change while SCL is low, except for the START and STOP conditions. Data are transmitted in 8-bit words. Nine clock cycles are required to transfer the data into or out of the device (8-bit word plus acknowledge bit).

Device Functional Modes (continued)

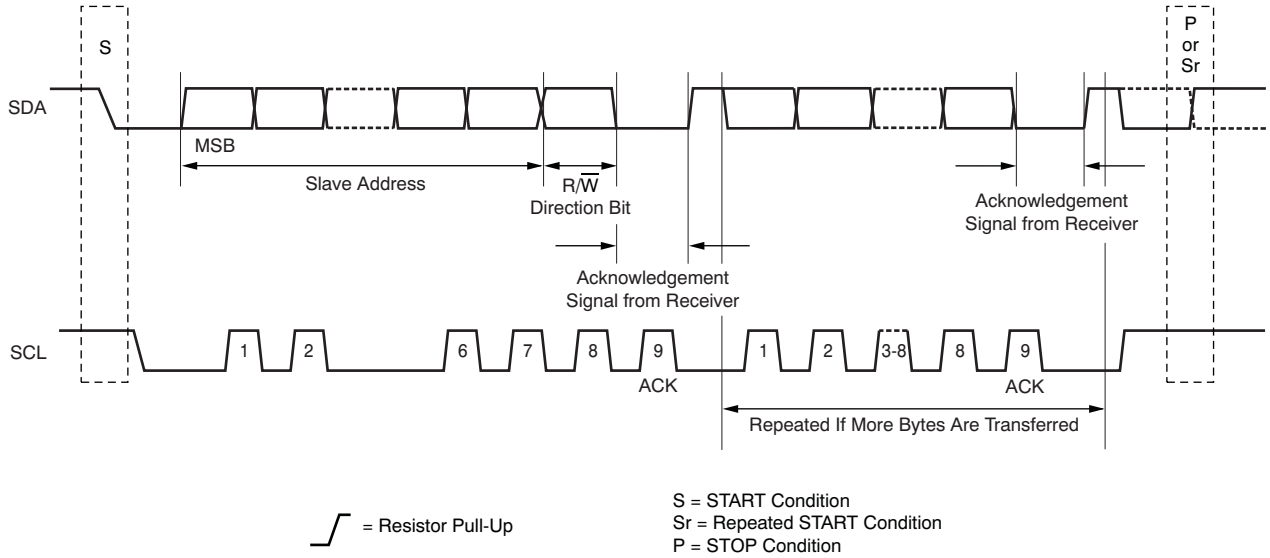

Figure 23. Complete Fast- or Standard-Mode Transfer

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Device Functional Modes (continued)

7.4.1.2 I²C High-Speed Mode (Hs Mode)

Serial data transfer format in High-Speed (Hs) mode meets the Fast or Standard (F/S) mode I²C bus specification. Hs mode can only commence after the following conditions (all of which are in F/S mode) exist:

1. START condition (S)
2. 8-bit master code (00001xxx)
3. not-acknowledge bit (N)

Figure 24 shows this sequence in more detail. Hs-mode master codes are reserved 8-bit codes used only for triggering Hs mode, and are not to be used for slave addressing or any other purpose. The master code indicates to other devices that an Hs-mode transfer is about to begin and the connected devices must meet the Hs mode specification. Because no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge bit (N).

After the not-acknowledge bit (N) and SCL have been pulled up to a HIGH level, the master switches to Hs-mode and enables (at time t_H; shown in Figure 24) the current-source pull-up circuit for SCL. Because other devices can delay the serial transfer before t_H by stretching the LOW period of SCL, the master enables its current-source pull-up circuit when all devices have released SCL, and SCL has reached a HIGH level, thus speeding up the last part of the rise time of the SCL.

The master then sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/$\overline{W}$ bit address, and receives an acknowledge bit (A) from the selected slave. After a repeated START (Sr) condition and after each acknowledge bit (A) or not-acknowledge bit (N), the master disables its current-source pull-up circuit. This disabling enables other devices to delay the serial transfer by stretching the LOW period of SCL. The master re-enables its current-source pull-up circuit again when all devices have released, and SCL reaches a HIGH level, which speeds up the last part of the SCL signal rise time.

Data transfer continues in Hs mode after the next repeated START (Sr), and only switches back to F/S mode after a STOP condition (P). To reduce the overhead of the master code, it is possible that a master links a number of Hs mode transfers, separated by repeated START conditions (Sr).

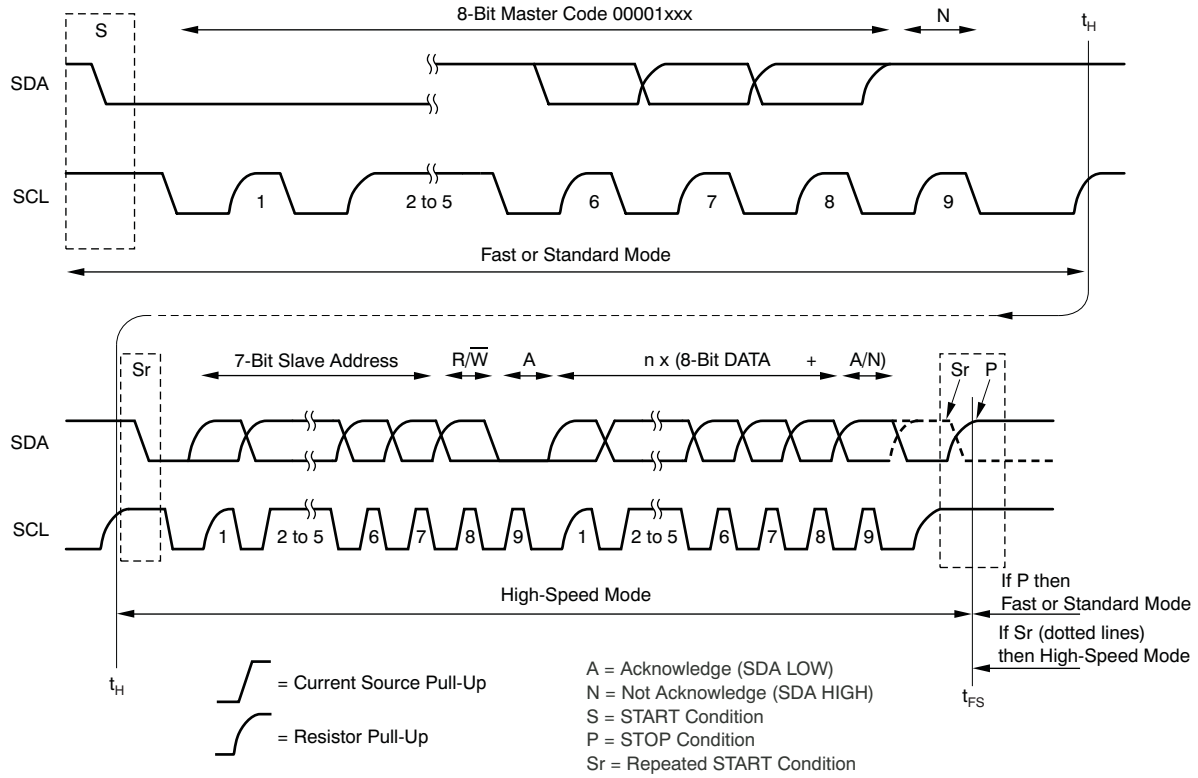

Figure 24. Complete High-Speed Mode Transfer

Device Functional Modes (continued)

7.4.2 Touch Screen Measurements

As noted previously in the discussion of the A/D converter, several operating modes can be used that allow great flexibility for the host processor. This section examines these different modes.

7.4.2.1 Conversion Controlled by TSC2014 Initiated by TSC2014 (TSMode 1)

In TSMode 1, before a pen touch can be detected, the TSC2014 must be programmed with PSM = 1 and one of two scan modes:

1. X-Y-Z Scan (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 0000); or
2. X-Y Scan (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 0001).

See Table 9 for more information on the converter function select bits.

When the touch panel is touched, and the internal pen-touch signal activates, the $\overline{\text{PINTDAV}}$ output is lowered if it is programmed as $\overline{\text{PENIRQ}}$. The TSC2014 then executes the preprogrammed scan function without a host intervention.

At the same time, the TSC2014 starts up its internal clock. It then turns on the Y-drivers, and after a programmed panel voltage stabilization time, powers up the A/D converter and converts the Y coordinate. If preprocessing is selected, several conversions may take place. When data preprocessing is complete, the Y coordinate result is stored in a temporary register.

If the screen is still touched at this time, the X-drivers are enabled, and the process repeats, but measures the X coordinate instead, and stores the result in a temporary register.

If only X and Y coordinates are to be measured, then the conversion process is complete. A set of X and Y coordinates are stored in the X and Y registers. Figure 25 shows a flowchart for this process. The time it takes to go through this process depends upon the selected resolution, internal conversion clock rate, panel voltage stabilization time, precharge and sense times, and whether preprocessing is selected. The time needed to get a complete X and Y coordinate (sample set) reading can be calculated by:

$$t_{COORDINATE} = \frac{OH1}{f_{OSC}} + 2 \cdot \left(t_{PVS} + t_{PRE} + t_{SNS} + \frac{OH_{DLY1}}{f_{OSC}} \right) + 2 \cdot \left(N \cdot \left((B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV} \right) \cdot \left(\frac{1}{f_{OSC}} \right) + \left(\frac{L_{PPRO}}{f_{OSC}} \right) \right) \quad (5)$$

Where:

$t_{COORDINATE}$ = time to complete X/Y coordinate reading.
t_{PVS} = panel voltage stabilization time, as given in Table 15.
t_{PRE} = precharge time, as given in Table 16.
t_{SNS} = sense time, as given in Table 17.
N = number of measurements for MAV filter input, as given in Table 3 as *N*.
(For no MAV: M1-0[1:0] = '00', W1-0[1:0] = '00', N = 1.)
B = number of bits of resolution.
f_{OSC} = TSC onboard OSC clock frequency. See Electrical Characteristics for supply frequency (V_{DD}).
f_{ADC} = A/D converter clock frequency, as given in Table 14.
OH1 = overhead time #1 = 2.5 internal clock cycles.
OH_{DLY1} = total overhead time for t_{PVS}, t_{PRE}, and t_{SNS} = 10 internal clock cycles.
OH_{CONV} = total overhead time for A/D conversion = 3 internal clock cycles.
L_{PPRO} = preprocessor preprocessing time as given in Table 4.

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Device Functional Modes (continued)

Table 4. Preprocessing Delay

M =	W =	L_{PPRO} =	
		FOR B = 12 BIT	FOR B = 10 BIT
1	1, 4, 8, 16	2	2
3, 7	1	28	24
7	3	31	27
15	1	31	29
15	3	34	32
15	7	38	36

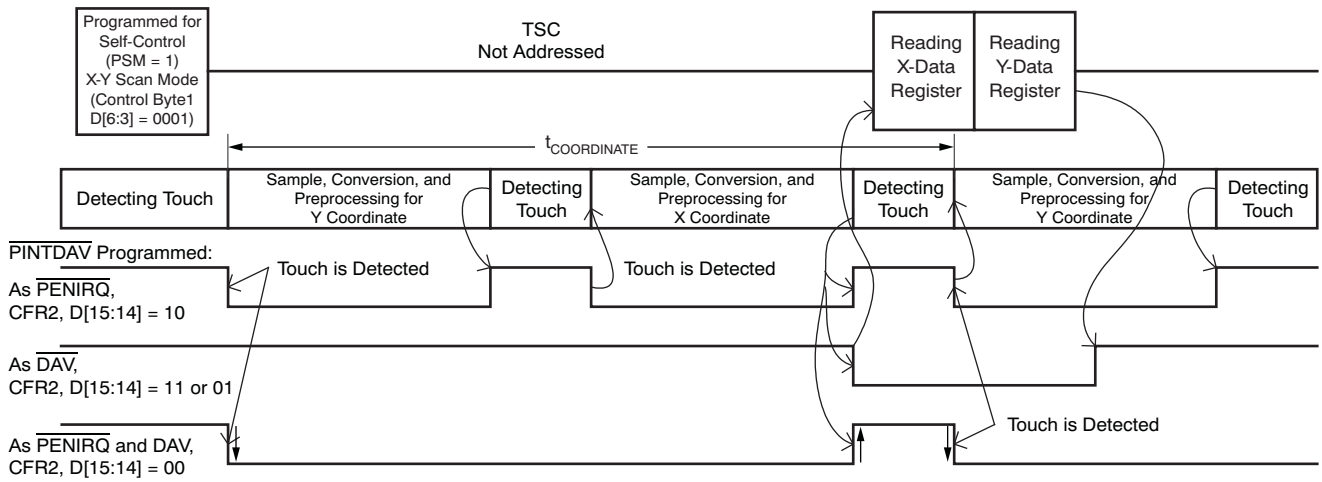

Figure 25. Example of an X and Y Coordinate Touch Screen Scan Using TSMode 1

If the pressure of the touch is also to be measured, the process continues in the same way, but measuring the Z_1 and Z_2 values instead, and storing the results in temporary registers. Once the complete sample set of data (X, Y, Z_1, and Z_2) are available, they are loaded in the X, Y, Z_1, and Z_2 registers. This process is illustrated in Figure 26. As before, this process time depends upon the settings described above. The time for a complete X, Y, Z_1, and Z_2 coordinate reading is given by:

$$t_{COORDINATE} = \frac{OH2}{f_{OSC}} + 3 \cdot \left(t_{PVS} + t_{PRE} + t_{SNS} + \frac{OH_{DLY1}}{f_{OSC}} \right) + 4 \cdot \left(N \cdot \left((B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV} \right) \cdot \left(\frac{1}{f_{OSC}} \right) + \left(\frac{L_{PPRO}}{f_{OSC}} \right) \right) \quad (6)$$

Where:

OH2 = overhead time #2 = 3.5 internal clock cycles.

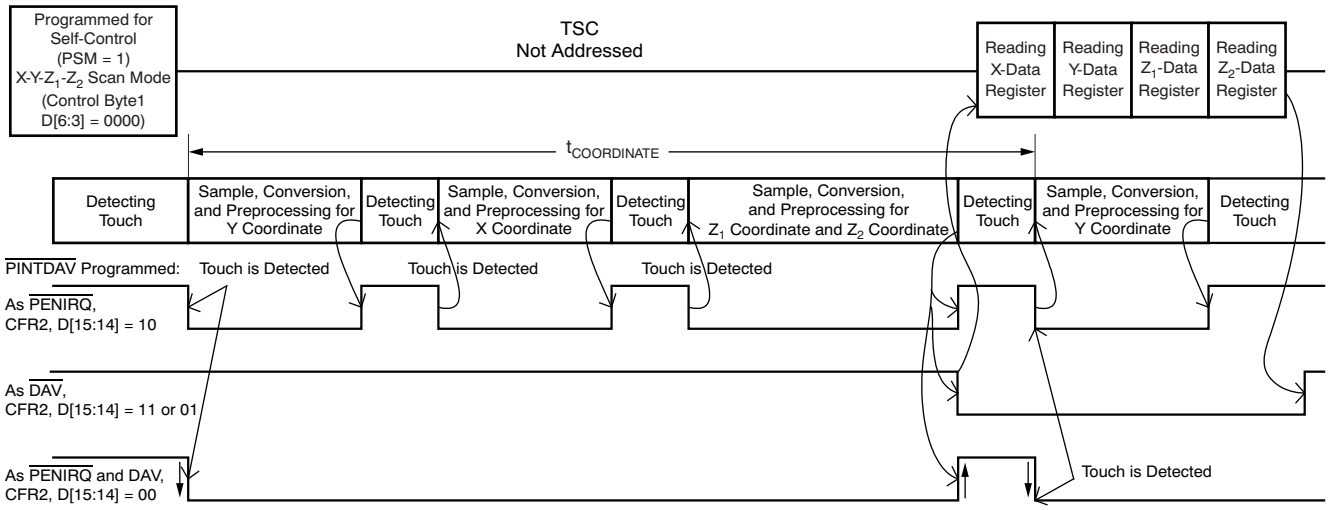

Figure 26. Example of an X, Y, and Z Coordinate Touch Screen Scan Using TSMode 1

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7.4.2.2 Conversion Controlled by TSC2014 Initiated by Host (TSMode 2)

In TSMode 2, the TSC2014 detects when the touch panel is touched and causes the internal Pen-Touch signal to activate, which lowers the $\overline{\text{PINTDAV}}$ output if it is programmed as $\overline{\text{PENIRQ}}$. The host recognizes the interrupt request, and then writes to the A/D Converter Control register to select one of the two touch screen scan functions:

1. X-Y-Z Scan (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 0000); or
2. X-Y Scan (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 0001).

See Table 9 for more information on the converter function select bits.

The conversion process then proceeds as shown in Figure 27; see the previous sections for more details.

The main difference between this mode and the previous mode is that the host, not the TSC2014, decides when the touch screen scan begins.

The time needed to convert both X and Y coordinates under host control (not including the time needed to send the command over the I^{2}C bus) is given by:

$$t_{COORDINATE} = \frac{OH1}{f_{OSC}} + 2 \cdot \left(t_{PVS} + t_{PRE} + t_{SNS} + \frac{OH_{DLY1}}{f_{OSC}} \right) + 2 \cdot \left(N \cdot \left((B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV} \right) \cdot \left(\frac{1}{f_{OSC}} \right) + \left(\frac{L_{PPRO}}{f_{OSC}} \right) \right) \quad (7)$$

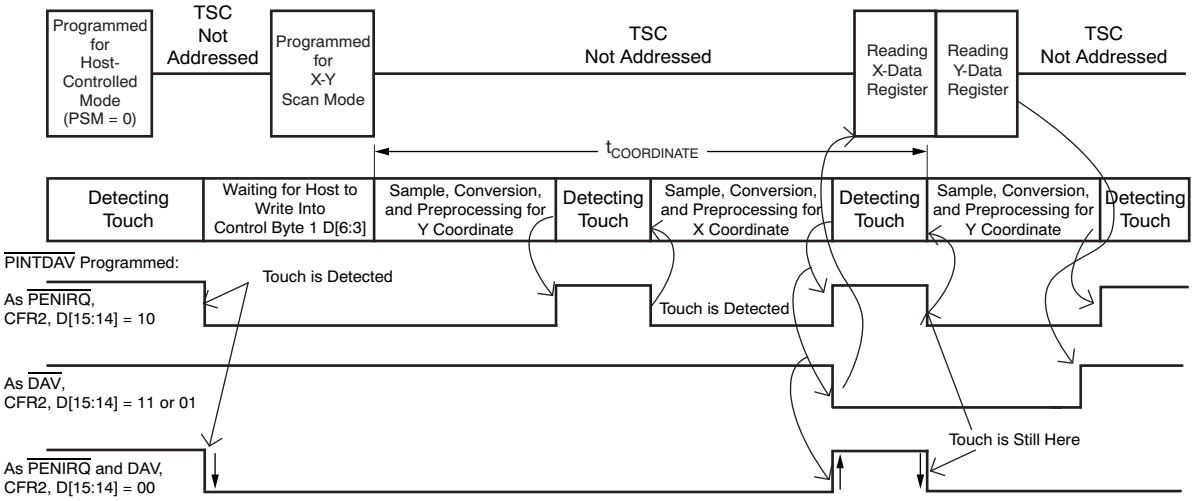


Figure 27. Example of an X and Y Coordinate Touch Screen Scan Using TSMode 2

7.4.2.3 Conversion Controlled by Host (TSMode 3)

In TSMode 3, the TSC2014 detects when the touch panel is touched and causes the internal Pen-Touch signal to be active, which lowers the $\overline{\text{PINTDAV}}$ output if it is programmed as $\overline{\text{PENIRQ}}$. The host recognizes the interrupt request. Instead of starting a sequence in the TSC2014, which then reads each coordinate in turn, the host must now control all aspects of the conversion. Generally, upon receiving the interrupt request, the host turns on the X drivers.

NOTE

If drivers are not turned on, the device detects this condition and turns them on before the scan starts. This situation is why the event of *Turn On Drivers* is shown as optional in Figure 28 and Figure 29.

After waiting for the settling time, the host then addresses the TSC2014 again, this time requesting an X coordinate conversion.

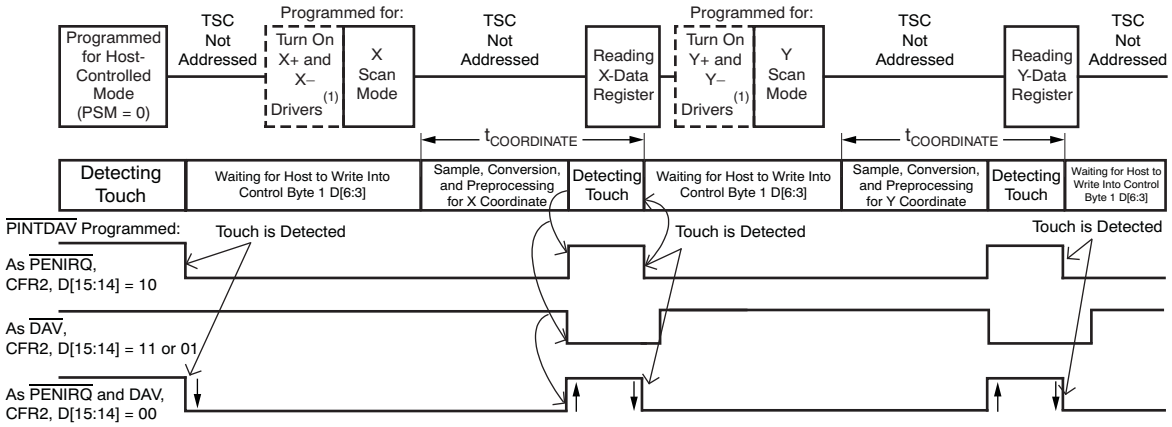
The process is then repeated for the Y and Z coordinates. The processes are outlined in Figure 28 and Table 5. Figure 28 shows two consecutive scans on X and Y. Figure 29 shows a single Z scan.

The time needed to convert any single coordinate X or Y under host control (not including the time needed to send the command over the I^{2}C bus) is given by:

$$t_{COORDINATE} = \frac{OH1}{f_{OSC}} + \left(t_{PRE} + t_{SNS} + \frac{OH_{DLY2}}{f_{OSC}}\right) + N \cdot \left((B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV}\right) \cdot \left(\frac{1}{f_{OSC}}\right) + \left(\frac{L_{PPRO}}{f_{OSC}}\right) \quad (8)$$

Where:

OH_{DLY2} = total overhead time for t_{PRE} and t_{SNS} = 6 internal clock cycles.



NOTE: (1) Optional. If not turned on, it will be turned on by the Scan mode, once detected.

Figure 28. Example of X and Y Coordinate Touch Screen Scan Using TSMode 3

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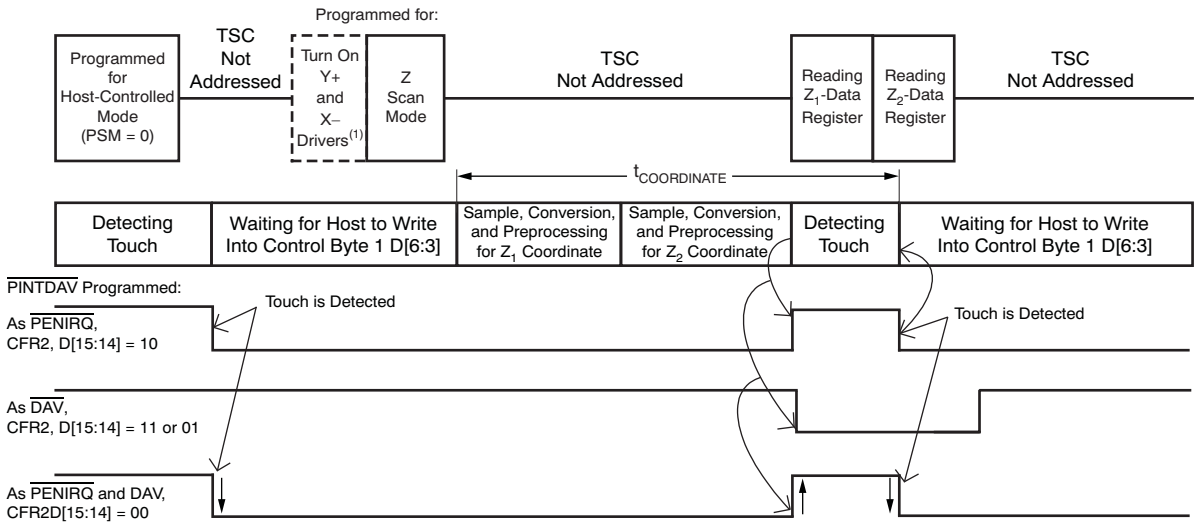
The time needed to convert any Z_1 and Z_2 coordinate under host control (not including the time needed to send the command over the I^2C bus) is given by:

$$t_{COORDINATE} = \frac{OH2}{f_{OSC}} + \left(t_{PRE} + t_{SNS} + \frac{OH_{DLY2}}{f_{OSC}}\right) + N \cdot \left((B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV}\right) \cdot \left(\frac{1}{f_{OSC}}\right) + \left(\frac{L_{PPRO}}{f_{OSC}}\right) \quad (9)$$



NOTE: (1) Optional. If not turned on, it will be turned on by the Scan mode, once detected.

Figure 29. Example of Z_1 and Z_2 Coordinate Touch Screen Scan (without Panel Stabilization Time) Using TSMode 3

If the drivers are not turned on before the touch screen scan mode is programmed, the panel stabilization time should be included. In this case, the time needed to convert any single X or Y under host control (not including the time needed to send the command over the I^2C bus) is given by:

$$t_{COORDINATE} = \frac{OH2}{f_{OSC}} + \left(t_{PVS} + t_{PRE} + t_{SNS} + \frac{OH_{DLY1}}{f_{OSC}}\right) + N \cdot \left((B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV}\right) \cdot \left(\frac{1}{f_{OSC}}\right) + \left(\frac{L_{PPRO}}{f_{OSC}}\right) \quad (10)$$

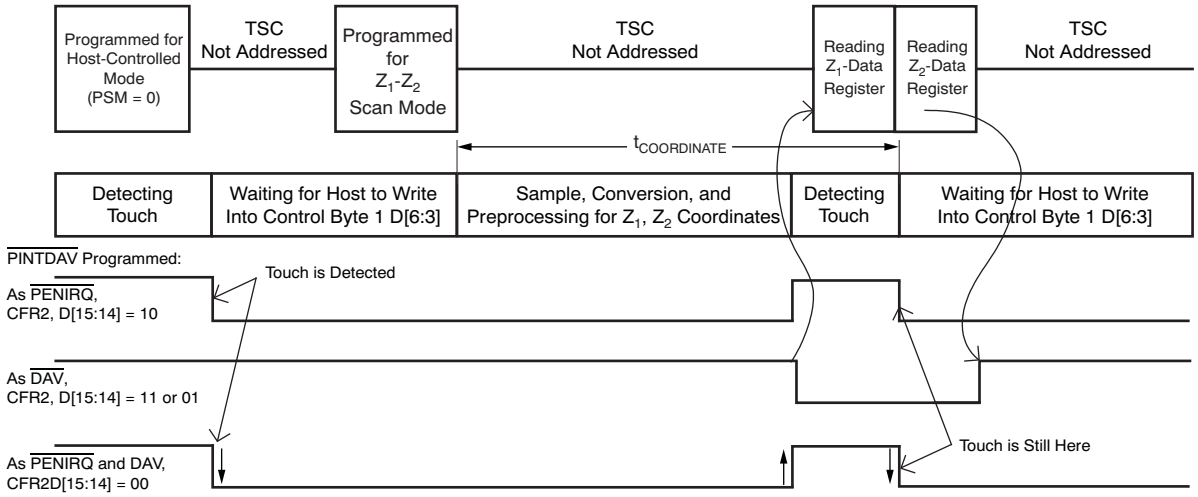


Figure 30. Example of a Z_1 and Z_2 Coordinate Touch Screen Scan (with Panel Stabilization Time) Using TSMode 3

The time needed to convert any single coordinate (either X or Y) under host control (not including the time needed to send the command over the I²C bus) is given by:

$$t_{COORDINATE} = \frac{OH1}{f_{OSC}} + \left(t_{PVS} + t_{PRE} + t_{SNS} + \frac{OH_{DLY1}}{f_{OSC}}\right) + N \cdot \left((B + 2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV}\right) \cdot \left(\frac{1}{f_{OSC}}\right) + \left(\frac{L_{PPRO}}{f_{OSC}}\right) \quad (11)$$

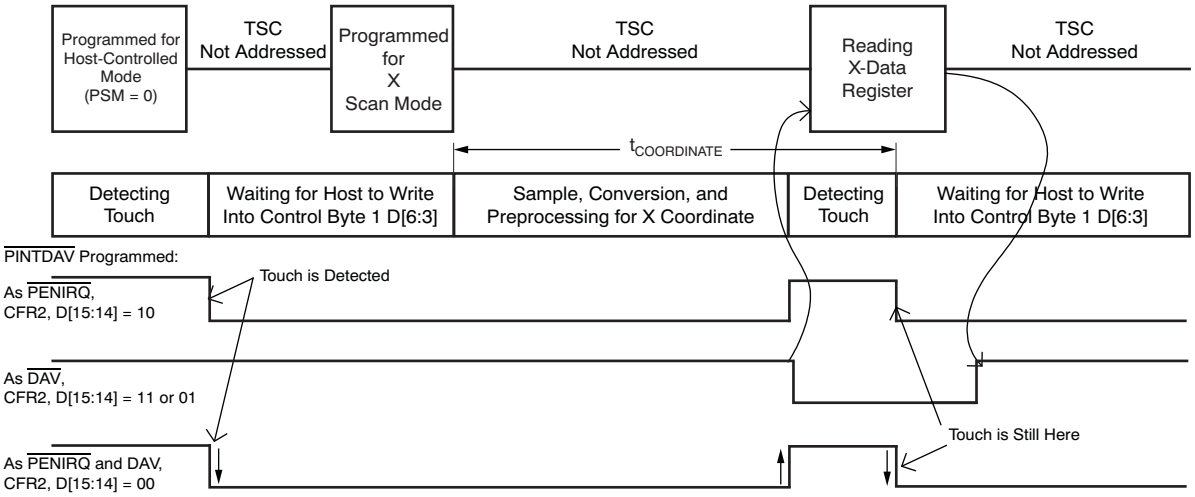


Figure 31. Example of a Single X Coordinate Touch Screen Scan (with Panel Stabilization Time) using TSMode 3

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7.5 Programming

7.5.1 Digital Interface

7.5.1.1 Address Byte

The TSC2014 has a 7-bit slave address word. The first six bits (MSBs) of the slave address are factory-preset to comply with the I^2C standard for A/D converters and are always set at '100100'. The logic state of the address input pin determines the LSB of the device address to activate communication. Therefore, a maximum of two devices with the same preset code can be connected on the same bus at one time.

The AD0 address input is only read during a power-up of the device, and should be connected to supply (VDD/REF) or ground (GND). The slave address is latched into the TSC2014 on the falling edge of SCL after the read/write bit has been received by the slave.

The last bit of the address byte (R/$\overline{W}$) defines the operation to be performed. When set to a '1', a read operation is selected; when set to a '0', a write operation is selected. Following the START condition, the TSC2014 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving the '10010' code, the appropriate device select bits, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

Table 5. I^2C Slave Address Byte

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1	0	0	1	0	0	AD0	R/$\overline{W}$

7.5.1.1.1 Bit D0: R/$\overline{W}$

1: I^2C master read from TSC (I^2C read addressing).

0: I^2C master write to TSC (I^2C write addressing).

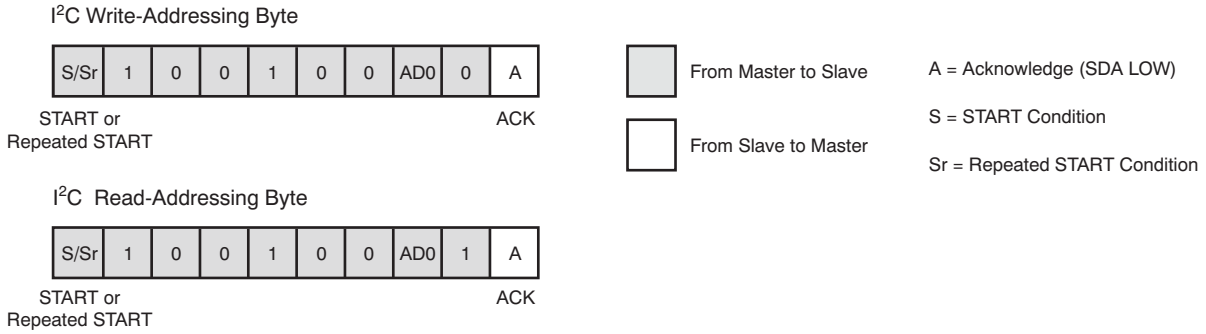
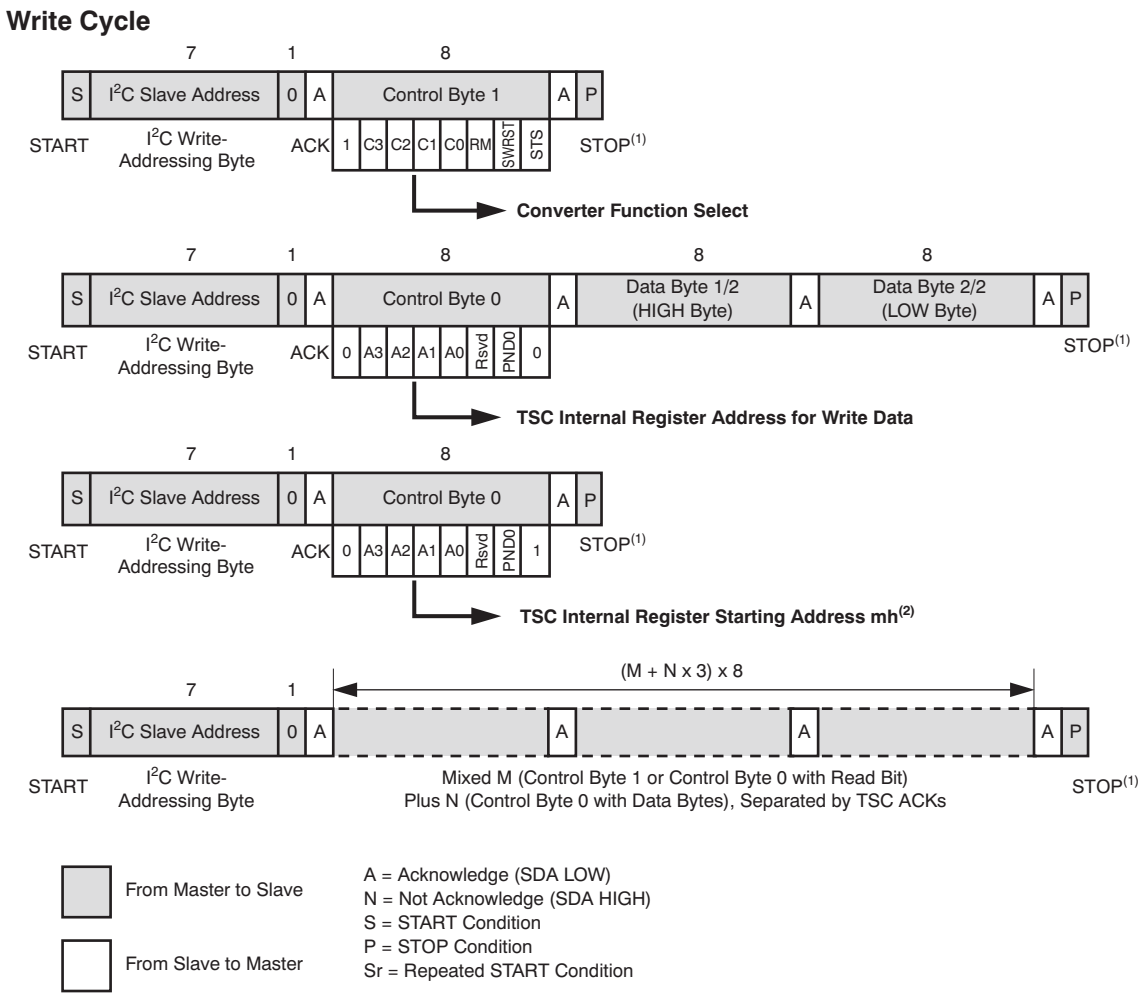


Figure 32. I^2C Bus Addressing (Slave Address Byte Format)

7.5.2 Start A Write Cycle

A write cycle begins when the master issues the slave address to the TSC2014. The slave address consists of seven address bits and a write bit (R/$\overline{W}$ = 0; see Table 5). When the eighth bit has been received and the address matches the AD0 address input pin setting, the TSC2014 issues an acknowledge bit by pulling SDA low for one additional clock cycle (ACK = 0); see Figure 32.

When the master receives the acknowledge bit from the TSC2014, the master writes the input control byte to the slave; see Table 5. After the control byte is received by the slave, the slave issues another acknowledge bit by pulling SDA low for one clock cycle (ACK = 0). The master then ends the write cycle by issuing a STOP or repeated START condition; see Figure 33.



NOTES: (1) In order to start the next sequence, a STOP condition must be followed by a START condition. If no STOP is used, then a Repeated START must be used. Also note that is a STOP condition is issued in High-Speed mode, the mode will revert to the previous mode: Fast or Standard.
(2) mh is a hexadecimal number.

Figure 33. Write Cycle

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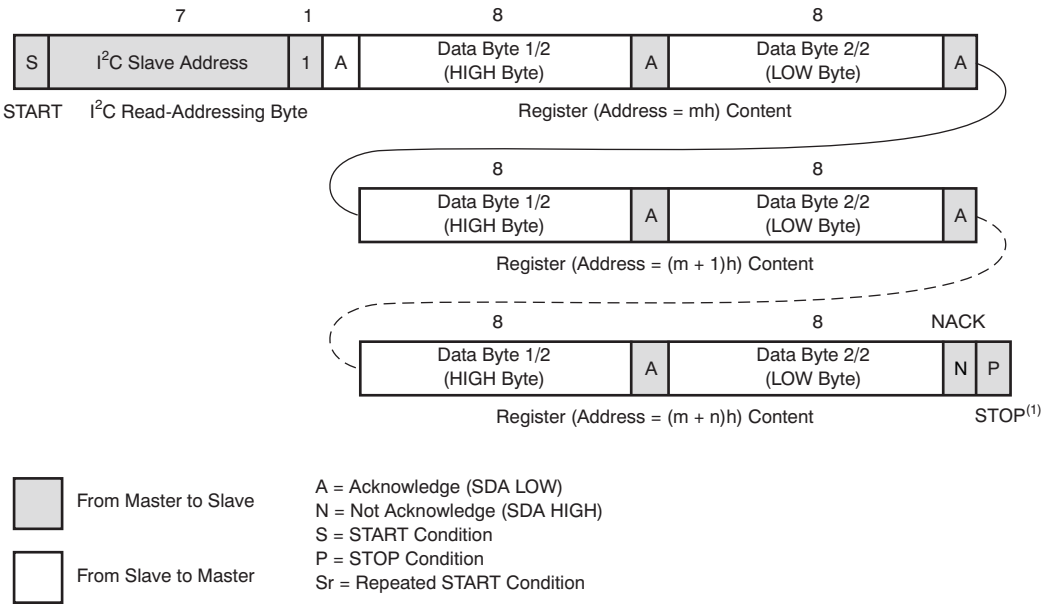
7.5.3 Register Access

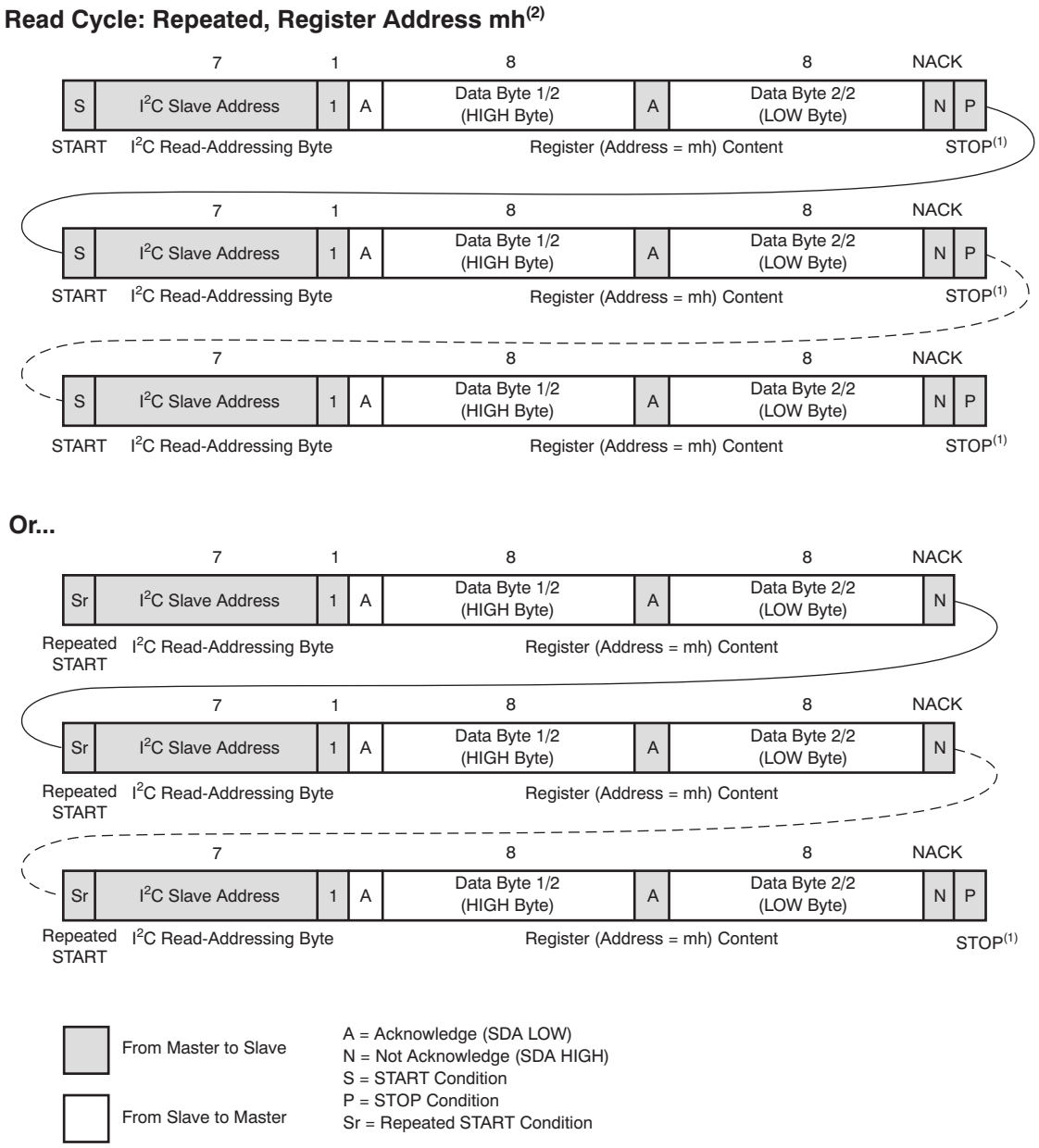
Data access begins with the master issuing a START (or repeated START) condition followed by the 7-bit address and a read bit (R/$\overline{W}$ = 1; see Table 5). When the eighth bit has been received and the address matches, the slave issues an acknowledge by pulling SDA low for one clock cycle (ACK = 0). The first byte of serial data then follows. After the first byte has been sent by the slave, it releases the SDA line for the master to issue an acknowledge (ACK = 0). The slave issues the second byte of serial data upon receiving the acknowledgment from the master (D7-D0), followed by a not-acknowledge bit (ACK = 1) from the master to indicate that the last data byte has been received. The master then issues a STOP condition (P) or repeated START (Sr), which ends the read cycle, as shown in Figure 34 and Figure 35. If the master issues a not-acknowledge (ACK = 1) after receipt of the first data byte, the master must then issue a stop condition (P) to reset the registers. If the master is not ready to receive the second data byte, it should issue the acknowledge (ACK = 0), or the master should stretch the clock. Upon restart of the clock, the second byte of data can be received by the master.

Read Cycle: Sequential, from Register Address mh(2) to (m + n)h(3)



NOTES: (1) In order to start the next sequence, a STOP condition must be followed by a START condition. If no STOP is used, then a Repeated START must be used. Also note that is a STOP condition is issued in High-Speed mode, the mode will revert to the previous mode: Fast or Standard.
(2) mh is a hexadecimal number.
(3) If (m+n)h is greater than Fh, then (m + n)h is modulo 16.

Figure 34. Sequential Read Cycle



NOTES: (1) In order to start the next sequence, a STOP condition must be followed by a START condition. If no STOP is used, then a Repeated START must be used. Also note that is a STOP condition is issued in High-Speed mode, the mode will revert to the previous mode: Fast or Standard.
(2) mh is a hexadecimal number.

Figure 35. Repeated Read Cycle

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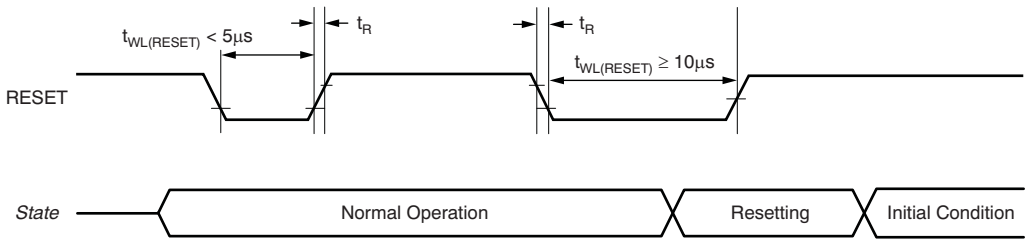
7.5.4 Register Reset

There are three way to reset the TSC2014.

- First: At power-on, a power good signal generates a prolonged reset pulse internally to all registers.
- Second: An external pin, $\overline{\text{RESET}}$, is available to perform a system reset or allow other peripherals (such as a display) to reset the device if the pulse meets the timing requirement (at least 10µs wide). Any $\overline{\text{RESET}}$ pulse less than 5µs will be rejected. To accommodate the timing drift between devices because of process variation, a $\overline{\text{RESET}}$ pulse width between 5µs to 10µs falls into the gray area that is not recognized, and the result is undetermined; this situation should be avoided. Refer to Figure 36 for details. A good reset pulse must be low for at least 10 µs. There is an internal spike filter to reject spikes up to 20ns wide.



NOTE: See *Timing Requirements* for more information.

Figure 36. External Reset Timing

- Third: A software reset can be activated by writing a '1' to CB1.1 (bit 1 of control byte 1). It should be noted this reset is not self-clearing so the user must write a '0' to remove the software reset.

A reset clears all registers and loads default values. A power-on reset and external (hardware) reset take precedence over a software reset. If a software reset is not cleared by the user, it is cleared by either a power-on reset or an external (hardware) reset.

NOTE

It is required to have the host issue a hardware reset to the TSC2014 after the device power is good and stable to ensure all the registers initialized properly.

7.6 Register Maps

7.6.1 R/$\overline{\text{W}}$

Register read and write control. A '1' indicates that the value of the internal register address bits A3-A0 is stored internally as the starting address for a register read (see Figure 33). The content of the addressed register is sent to SDA by using I^2C read addressing (see Figure 34 and Figure 35). A '0' indicates that the data following Control Byte 0 on SDA are written into the internal register addressed by bits A3-A0 (see Figure 33).

Register Maps (continued)

7.6.2 Control Byte 0

Figure 37. Control Byte Format: Start a Conversion and Mode Setting

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
(Control Byte 0)	A3	A2	A1	A0	Reserved (Write '0')	PND0	R/$\overline{W}$

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Control Byte 0 Bit Register Description (D7 = 0)

Bit	Field	Type	Reset	Description
D7	Control Byte ID	R/W	0000h	1: Control Byte 1 (start conversion and channel select and conversion-related configuration). 0: Control Byte 0 (read/write data registers and non-conversion-related controls).
D6	A3	R	0000h	Register Address Bits as detailed in Table 7
D5	A2	R	0000h	
D4	A1	R	0000h	
D3	A0	R	0000h	
D2	RESERVED	R	0000h	A '0' must be set in this bit for normal operation
D1	PND0	R/W	0000h	Power Not Down Control 1: A/D converter biasing circuitry is always on between conversions but is shut down after the converter function stops. 0: A/D converter biasing circuitry is shut down either between conversions or after the converter function stops
D0	R/$\overline{W}$	R/W	0000h	TSC Internal Register Data Flow Control 1: Set the starting address of the TSC internal registers for a register read (see Figure 33) 0: Write to TSC internal registers

Table 7. Internal Register Map

REGISTER ADDRESS				REGISTER CONTENT	READ/WRITE
A3	A2	A1	A0		
0	0	0	0	X measurement result	R
0	0	0	1	Y measurement result	R
0	0	1	0	Z_1 measurement result	R
0	0	1	1	Z_2 measurement result	R
0	1	0	0	AUX measurement result	R
0	1	0	1	Temp1 measurement result	R
0	1	1	0	Temp2 measurement result	R
0	1	1	1	Status	R
1	0	0	0	AUX high threshold	R/W
1	0	0	1	AUX low threshold	R/W
1	0	1	0	Temp high threshold (apply to both TEMP1 and TEMP2)	R/W
1	0	1	1	Temp low threshold (apply to both TEMP1 and TEMP2)	R/W
1	1	0	0	CFR0	R/W
1	1	0	1	CFR1	R/W
1	1	1	0	CFR2	R/W
1	1	1	1	Converter function select status	R

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7.6.3 Control Byte 1

Figure 38. Control Byte Format: Start a Conversion and Mode Setting

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
(Control Byte 1)	C3	C2	C1	C0	RM	SWRST	STS

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. Control Byte 1 Bit Register Description (D7 = 1)

Bit	Field	Type	Reset	Description
D7	Control Byte ID	R/W	0000h	1: Control Byte 1 (start conversion and channel select and conversion-related configuration). 0: Control Byte 0 (read/write data registers and non-conversion-related controls).
D6	C3	R	0000h	Converter function select bits. These bits select the input to be converted, and the converter function to be executed. Table 9 lists the possible converter functions.
D5	C2	R	0000h	
D4	C1	R	0000h	
D3	C0	R	0000h	
D2	RM	R/W	0000h	0: 10 Bit 1: 12 Bit
D1	SWRST	R/W	0000h	Software Reset. This bit is self-clearing. 1: Reset all register values to default
D0	STS	R/W	0000h	Stop bit for all converter functions. This bit is self-clearing.

Table 9. Converter Function Select

C3	C2	C1	C0	FUNCTION
0	0	0	0	Touch screen scan function: X, Y, Z_1, and Z_2 coordinates converted and the results returned to X, Y, Z_1, and Z_2 data registers. Scan continues until either the pen is lifted or a stop bit is sent.
0	0	0	1	Touch screen scan function: X and Y coordinates converted and the results returned to X and Y data registers. Scan continues until either the pen is lifted or a stop bit is sent.
0	0	1	0	Touch screen scan function: X coordinate converted and the results returned to X data register.
0	0	1	1	Touch screen scan function: Y coordinate converted and the results returned to Y data register.
0	1	0	0	Touch screen scan function: Z_1 and Z_2 coordinates converted and the results returned to Z_1 and Z_2 data registers.
0	1	0	1	Auxiliary input converted and the results returned to the AUX data register.
0	1	1	0	A temperature measurement is made and the results returned to the Temperature Measurement 1 data register.
0	1	1	1	A differential temperature measurement is made and the results returned to the Temperature Measurement 2 data register.
1	0	0	0	Auxiliary input is converted ***continuously*** and the results returned to the AUX data register.
1	0	0	1	Touch screen panel connection to X-axis drivers is tested. The test result is output to $\overline{\text{PINTDAV}}$ and shown in STATUS register.
1	0	1	0	Touch screen panel connection to Y-axis drivers is tested. The test result is output to $\overline{\text{PINTDAV}}$ and shown in STATUS register.
1	0	1	1	RESERVED (Note: any condition caused by this command can be cleared by setting the STS bit to 1).
1	1	0	0	Touch screen panel short-circuit (between X and Y plates) is tested through Y-axis. The test result is output to $\overline{\text{PINTDAV}}$ and shown in the STATUS register.
1	1	0	1	X+, X– drivers status
1	1	1	0	Y+, Y– drivers status
1	1	1	1	Y+, X– drivers status

7.6.3.1 Touch Screen Scan Function for XYZ or XY

7.6.3.1.1 C3-C0 = 0000 or 0001

These scan functions can collaborate with the PSM bit that defines the control mode of converter functions. If the PSM bit is set to '1', these scan function select commands are recommended to be issued before a pen touch is detected in order to allow the TSC2014 to initiate and control the scan processes immediately after the screen is touched. If these functions are not issued before a pen touch is detected, the TSC2014 waits for the host to write these functions before starting a scan process. If PSM stays as '1' after a TSC-initiated scan function is complete, the host is not required to write these function select bits again for each of the following pen touches after the detected touch. In the host-controlled converter function mode (PSM = 0), the host must send these functions select bits repeatedly for each scan function after a detected pen touch.

Note that the data registers may be updated while a host reading is in progress. Using the sequential read cycle (see Figure 34) prevents the TSC from updating registers while a host reading is in progress. To ensure that the XYZ or XY coordinates are correctly read, use the sequential read cycle to read the coordinates after the scan.

7.6.3.2 Touch Screen Sensor Connection Tests for X-Axis and Y-Axis

Range of resistances of different touch screen panels can be selected by setting the TBM bits in CFR1; see Table 18. Once the resistance of the sensor panel is selected, two continuity tests are run separately for the X-axis and Y-axis. The unit under test must pass both connection tests to ensure that a proper connection is secured.

7.6.3.2.1 C3-C0 = 1001

$\overline{\text{PINTDAV}}$ = 0 during this connection test. A '1' shown at end of the test indicates the X-axis drivers are well-connected to the sensor; otherwise, X-axis drivers are poorly connected. If drivers fail to connect, then $\overline{\text{PINTDAV}}$ stays low until a stop bit (STS set to '1') is issued.

7.6.3.2.2 C3-C0 = 1010

$\overline{\text{PINTDAV}}$ = 0 during this connection test. A '1' shown at end of the test indicates the Y-axis drivers are well-connected to the sensor; otherwise, Y-axis drivers are poorly connected. If the drivers are fail to connect, then $\overline{\text{PINTDAV}}$ stays low until a stop bit (STS set to '1') is issued.

7.6.3.3 Touch Sensor Short-Circuit Test

If the TBM bits of CFR1 detailed in Table 18 are all set to '1', a short-circuit in the touch sensor can be detected.

7.6.3.3.1 C3-C0 = 1011

Reserved.

7.6.3.3.2 C3-C0 = 1100

$\overline{\text{PINTDAV}}$ = 0 during this short-circuit test. A '1' shown at end of the test indicates there is no short-circuit detected (through Y-axis) between the flex and stable layers. If there is a short-circuit detected, $\overline{\text{PINTDAV}}$ stays low until a stop bit (STS set to '1') is issued.

7.6.3.3.3 RM

Resolution select. If RM = 1, the conversion result resolution is 12-bit; otherwise, the resolution is 10-bit. This bit is the same RM bit shown in CFR0.

7.6.3.3.4 SWRST

Software reset input. All register values are set to default value if a '1' is written to this bit. This bit is automatically set to '0' in order to cancel the software reset and resume normal operation.

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7.6.3.3.5 STS

Stop bit for all converter functions. When writing a '1' to this register, this bit aborts the converter function currently running in the TSC2014. A '0' is automatically written to this register in order to end the stop bit. This bit can only stop converter functions; it does not reset any data, status, or configuration registers. This bit is the same STS bit shown in CFR0, but can only be read through the CFR0 register with different interpretations.

Table 10. STS Bit Operation

OPERATION	VALUE	DESCRIPTION
Write	0	Normal operation
Write	1	Stop converter functions and power down

7.6.4 Communication Protocol

The TSC2014 is controlled entirely by registers. Reading and writing to these registers are accomplished by the use of Control Byte 0, which includes a 4-bit address plus one read/write TSC register control bit. The data registers defined in Table 7 are all 16-bit, right-adjusted.

NOTE

Except for some configuration registers and the Status register that are full 16-bit registers, the rest of the value registers are 12-bit (or 10-bit) data preceded by four (or six) zeros.

7.6.4.1 Configuration Register 0

Figure 39. Configuration Register 0 (Reset Value = 4000h for Read; 0000h for Write)

MSB D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0
PSM	STS	RM	CL1	CL0	PV2	PV1	PV0	PR2	PR1	PR0	SN2	SN1	SN0	DTW	LSM

7.6.4.1.1 PSM

Pen status/control mode. Reading this bit allows the host to determine if the screen is touched. Writing to this bit selects the mode used to control the flow of converter functions that are either initiated and/or controlled by host or under control of the TSC2014 responding to a pen touch. When reading, the PSM bit indicates if the pen is down or not. When writing to this register, this bit determines if the TSC2014 controls the converter functions, or if the converter functions are host-controlled. The default state is the host-controlled converter function mode (0). The other state (1) is the TSC-initiated scan function mode that must only collaborate with C3-C0 = 0000 or 0001 in order to allow the TSC2014 to initiate and control the scan function for XYZ or XY when a pen touch is detected.

Table 11. PSM Bit Operation

OPERATION	VALUE	DESCRIPTION
Read	0	No screen touch detected
Read	1	Screen touch detected
Write	0	Converter functions initiated and/or controlled by host
Write	1	Converter functions initiated and controlled by the TSC2014

7.6.4.1.2 STS

A/D converter status. When reading, this bit indicates if the converter is busy or not busy. Continuous scans or conversions can be stopped by writing a '1' to this bit, immediately aborting the running converter function (even if the pen is still down) and causing the A/D converter to power down. The default state for write is 0 (normal operation), and the default state for read is 1 (converter is not busy). **NOTE:** The same bit can be written through Control Byte 1. This bit is self-clearing.

Table 12. STS Bit Operation

OPERATION	VALUE	DESCRIPTION
Read	0	Converter is busy
Read	1	Converter is not busy
Write	0	Normal operation
Write	1	Stop converter function and power down

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7.6.4.1.3 RM

Resolution control. The A/D converter resolution is specified with this bit. See Table 13 for a description of these bits. This bit is the same whether reading or writing, and defaults to 0. Note that the same bit can be written through Control Byte 1.

Table 13. A/D Converter Resolution Control

RM	FUNCTION
0	10-bit resolution. Power-up and reset default.
1	12-bit resolution

7.6.4.1.4 CL1, CL0

Conversion clock control. These two bits specify the clock rate that the A/D converter uses to perform conversion, as shown in Table 14.

Table 14. A/D Converter Conversion Clock Control

CL1	CL0	FUNCTION
0	0	$f_{ADC} = f_{OSC}/1$. This is referred to as the 4MHz A/D converter clock rate, 10-bit resolution only[(1)].
0	1	$f_{ADC} = f_{OSC}/2$. This is referred to as the 2MHz A/D converter clock rate.
1	0	$f_{ADC} = f_{OSC}/4$. This is referred to as the 1MHz A/D converter clock rate.
1	1	$f_{ADC} = f_{OSC}/4$. This is referred to as the 1MHz A/D converter clock rate.

(1) For V_{DD} = 1.2V at –40°C, a lower A/D converter clock rate should be used to allow enough time for conversion settling.

7.6.4.1.5 PV2-PV0

Panel voltage stabilization time control. These bits specify a delay time from the moment the touch screen drivers are enabled to the time the voltage is sampled and a conversion is started. These bits allow the user to adjust the appropriate settling time for the touch panel and external capacitances. See Table 15 for settings of these bits. The default state is 000, indicating a 0µs stabilization time. These bits are the same whether reading or writing.

Table 15. Panel Voltage Stabilization Time Control

PV2	PV1	PV0	STABILIZATION TIME (t_{PVS})
0	0	0	0µs
0	0	1	100µs
0	1	0	500µs
0	1	1	1ms
1	0	0	5ms
1	0	1	10ms
1	1	0	50ms
1	1	1	100ms

7.6.4.1.6 PR2-PR0

Precharge time selection. These bits set the amount of time allowed for precharging any pin capacitance on the touch screen prior to sensing if a pen touch is happening.

Table 16. Precharge Time Selection

PR2	PR1	PR0	PRECHARGE TIME(t_{PRE})
0	0	0	20µs
0	0	1	84µs
0	1	0	276µs
0	1	1	340µs
1	0	0	1.044ms
1	0	1	1.108ms
1	1	0	1.300ms
1	1	1	1.364ms

7.6.4.1.7 SNS2-SNS0

Sense time selection. These bits set the amount of time the TSC2014 waits to sense whether the screen is touched after converting a coordinate.

Table 17. Sense Time Selection

SNS2	SNS1	SNS0	SENSE TIME (t_{SNS})
0	0	0	32µs
0	0	1	96µs
0	1	0	544µs
0	1	1	608µs
1	0	0	2.080ms
1	0	1	2.144ms
1	1	0	2.592ms
1	1	1	2.656ms

7.6.4.1.8 DTW

Detection of pen touch in wait (patent pending). Writing a '1' to this bit enables the pen touch detection in the background while waiting for the host to issue the converter function in host-initiated/controlled modes. This background detection allows the TSC2014 to pull high at $\overline{\text{PINTDAV}}$ to indicate no pen touch detected while waiting for the host to issue the converter function. If the host polls a high state at $\overline{\text{PINTDAV}}$ before the convert function is sent, the host can abort the issuance of the convert function and stay in the polling $\overline{\text{PINTDAV}}$ mode until the next pen touch is detected.

7.6.4.1.9 LSM

Longer sampling mode. When this bit is set to '1', the extra 500ns of sampling time is added to the normal sampling cycles of each conversion. This additional time is represented as approximately two internal oscillator clock cycles. For V_{DD} = 1.2V at –40°C, the LSM bit should be set to '1' so that the sampled signal has enough time to settle.

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7.6.4.2 Configuration Register 1

Configuration register 1 (CFR1) defines the connection test-bit modes configuration and batch delay selection.

Figure 40. Configuration Register 1 (Reset Value = 0000h)

MSB D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0
Resrvd	Resrvd	Resrvd	Resrvd	TBM3	TBM2	TBM1	TBM0	Resrvd	Resrvd	Resrvd	Resrvd	Resrvd	BTD2	BTD1	BTD0

7.6.4.2.1 TBM3-TBM0

Connection test-bit modes (patent pending). These bits specify the mode of test bits used for the predefined range of the combined X-axis and Y-axis touch screen panel resistance (R_{TS}).

Table 18. Touch Screen Resistance Range and Test-Bit Modes

TEST-BIT MODES				R_{TS} (kΩ)
TBM3	TBM2	TBM1	TBM0	
0	0	0	0	0.17
0	0	0	1	$0.17 < R_{TS} \leq 0.52$
0	0	1	0	$0.52 < R_{TS} \leq 0.86$
0	0	1	1	$0.86 < R_{TS} \leq 1.6$
0	1	0	0	$1.6 < R_{TS} \leq 2.2$
0	1	0	1	$2.2 < R_{TS} \leq 3.6$
0	1	1	0	$3.6 < R_{TS} \leq 5.0$
0	1	1	1	$5.0 < R_{TS} \leq 7.8$
1	0	0	0	$7.8 < R_{TS} \leq 10.5$
1	0	0	1	$10.5 < R_{TS} \leq 16.0$
1	0	1	0	$16.0 < R_{TS} \leq 21.6$
1	0	1	1	$21.6 < R_{TS} \leq 32.6$
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Only for short-circuit panel test

7.6.4.2.2 BTD2-BTD0

Batch Time Delay mode. These are the selection bits that specify the delay before a sample/conversion scan cycle is triggered. When it is set, Batch Time Delay mode uses a set of timers to automatically trigger a sequence of sample-and-conversion events. The mode works for both TSC-initiated scans (XYZ or XY) and host-initiated scans (XYZ or XY).

A TSC-initiated scan (XYZ or XY) can be configured by setting the PSM bit in CFR0 to '1' and C[3:0] in Control Byte 1 to '0000' or '0001'. In the case of a TSC-initiated scan (XYZ or XY), the sequence begins with the TSC responding to a pen touch. After the first processed sample set completes during the batch delay, the scan enters a wait mode until the end of the batch delay is reached. If a pen touch is still detected at that moment, the scan continues to process the next sample set, and the batch delay is resumed. The throughput of the processed sample sets (shown in Table 19 as sample sets per second, or SSPS) is regulated by the selected batch delay during the time of the detected pen touch. A TSC-initiated scan (XYZ or XY) can be configured by setting the PSM bit in CFR0 to '1' and C[3:0] in Control Byte 1 to '0000' or '0001'. Note that the throughput of the processed sample set also depends on the settings of stabilization, precharge, and sense times, and the total number of samples to be processed per coordinates. If the accrual time of these factors exceeds the batch delay time, the accrual time dominates. Batch delay time starts when the pen touch initiates the scan function that converts coordinates.

A host-initiated scan (XYZ or XY) can be configured by setting the PSM bit in CFR0 to '0' and C[3:0] in Control Byte 1 to '0000' or '0001'. For the host-initiated scan (XYZ or XY), the host must set TSC internal register C[3:0] in Control Byte 1 to '0000' or '0001' initially after a pen touch is detected; see *Conversion Controlled by TSC2014 Initiated by Host (TSMode 2)* , in the *Theory of Operation* section. After the scan (XYZ or XY) is engaged, the throughput of the processed sample sets is regulated by the selected batch delay timer, as long as the initial detected touch is not interrupted.

Table 19. Touch Screen Throughput and Batch Selection Bits

BATCH DELAY SELECTION			DELAY TIME (ms)	THROUGHPUT FOR TSC-INITIATED OR HOST-INITIATED SCAN, XYZ OR XY (SSPS)
BTD2	BTD1	BTD0		
0	0	0	0	Normal operation throughput depends on settings.
0	0	1	1	1000
0	1	0	2	500
0	1	1	4	250
1	0	0	10	100
1	0	1	20	50
1	1	0	40	25
1	1	1	100	10

For example, if stabilization time, precharge time, and sense time are selected as 100µs, 84µs, and 96µs, respectively, and the batch delay time is 2ms, then the scan function enters wait mode after the first processed sample set until the 2ms of batch delay time is reached. When the scan function starts to process the second sample set (if the screen is still touched), the batch delay restarts at 2ms (in this example). This procedure remains regulated by 2ms until the pen touch is not detected or the scan function is stopped by a stop bit or any reset form.

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7.6.5 Configuration Register 2

Configuration register 2 (CFR2) defines the preprocessor configuration.

Figure 41. Configuration Register 2 (Reset Value = 0000h)

MSB D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0
PINTS1	PINTS0	M1	M0	W1	W0	TZ1	TZ0	AZ1	AZ0	Resrvd	MAVEX	MAVEY	MAVEZ	MAVEAUX	MAVETEMP

7.6.5.1 PINTS1 (default 0)

This bit controls the output format of the $\overline{\text{PINTDAV}}$ pin. When this bit is set to '0', the output format is shown as the AND-form of internal signals of $\overline{\text{PENIRQ}}$ and DAV). When this bit is set to '1', $\overline{\text{PINTDAV}}$ outputs $\overline{\text{PENIRQ}}$ only.

7.6.5.2 PINTS0 (default 0)

This bit selects what is output on the $\overline{\text{PINTDAV}}$ pin. If this bit set to '0', the output format of $\overline{\text{PINTDAV}}$ depends on the selection made on the PINTS1 bit. If this bit set to '1', the internal signal of $\overline{\text{DAV}}$ is output on $\overline{\text{PINTDAV}}$.

Table 20. PINTSx Selection

PINTS1	PINTS0	$\overline{\text{PINTDAV}}$ PIN OUTPUT =
0	0	AND combination of $\overline{\text{PENIRQ}}$ (active low) and DAV (active high).
0	1	Data available, $\overline{\text{DAV}}$ (active low).
1	0	Interrupt, $\overline{\text{PENIRQ}}$ (active low) generated by pen-touch.
1	1	Data available, $\overline{\text{DAV}}$ (active low).

7.6.5.3 M1, M0, W1, W0 (default 0000)

Preprocessing MAV filter control. Note that when the MAV filter is processing data, the STS bit and the corresponding DAV bits in the status register indicate that the converter is busy until all conversions necessary for the preprocessing are complete. The default state for these bits is 0000, which bypasses the preprocessor. These bits are the same whether reading or writing.

7.6.5.4 TZ1 and TZ0, or AZ1 and AZ0 (default 00)

Zone detection bit definition (for TEMP or AUX measurements). TZ1 and TZ0 are for the TEMP measurement. AZ1 and AZ0 are for the AUX measurement. The action taken in zone detection is to store the processed data in the corresponding data registers and to update the corresponding DAV bits in status register. If the processed data do not meet the selected criteria, these data are ignored and the corresponding DAV bits are not updated. When zone detection is disabled, the processed data are simply stored in the corresponding data registers and the corresponding DAV bits are updated without any comparison of criteria. Note that the converted samples are always processed according to the setting of the MAVE bits for AUX/TEMP before zone detection takes effect. See Table 24 for thresholds.

Table 21. Zone Detection Bit Definition

TZ1/AZ1	TZ0/AZ0	FUNCTION
0	0	Zone detection is disabled.
0	1	When the processed data are below low threshold
1	0	When the processed data are between low and high thresholds
1	1	When the processed data are above high threshold

7.6.5.5 MAVE (default is 00000)

MAV filter function enable bit. When the corresponding bit is set to '1', the MAV filter setup is applied to the corresponding measurement.

7.6.6 Converter Function Select Register

The Converter Function Select (CFN) register reflects the converter function select status.

Figure 42. Converter Function Select Status Register (Reset Value = 0000h)

MSB D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0
CFN15	CFN14	CFN13	CFN12	CFN11	CFN10	CFN9	CFN8	CFN7	CFN6	CFN5	CFN4	CFN3	CFN2	CFN1	CFN0

7.6.6.1 CFN15-CFN13

Touch screen drivers status. These bits represent the current status of the touch screen drivers that are turned on. CFN13 is set to '1' if both X+ and X- drivers are turned on. CFN14 is set to '1' if both Y+ and Y- drivers are turned on. CFN15 is set to '1' if Y+ and X- drivers are turned on. Otherwise, these bits are set to '0'. These bits are reset to 0h whenever the converter function is either complete, stopped by the STS bit, or reset (by a hardware reset from the $\overline{\text{RESET}}$ pin or a software reset from SWRST bit in Control Byte 1).

7.6.6.2 CFN12-CFN0

Converter function select status. These bits represent the converter function currently running, which is set in bits C3-C0 of Control Byte 1. When the CFNx bit shows '1', where x is the decimal value of converter function select bits C3-C0, it indicates that the converter function that is set in bits C3-C0 is running. For example, when CFN2 shows '1', it indicates the converter function set in bits C3-C0 ('0010') is running. The CFNx bits are reset to 0000h whenever the converter function is complete, stopped by STS bit, or reset (by the hardware reset from the $\overline{\text{RESET}}$ pin or the software reset from SWRST bit in Control Byte 1). However, if the TSC-initiated scan function mode is issued (by setting the PSM bit in the CFR0 register to '1'), the CFN0 or CFN1 bit will not be reset when the corresponding converter function is complete because there is no pen touch. This event allows the TSC2014 to immediately initiate the scan process (corresponding to CFN0 or CFN1 set to '1') when the next pen touch is detected.

Figure 43. STATUS Register (Reset Value = 0004h)

MSB D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0
DAV Due X	DAV Due Y	DAV Due Z1	DAV Due Z2	DAV Due AUX	DAV Due TEMP1	DAV Due TEMP2	RESRVD (read '0')	RESET Flag	X CON	Y CON	RESRVD (read '0')	Y SHR	PDST	ID1	ID0

7.6.6.3 DAV Bits

Data available bits. These seven bits mirror the operation of the internal signals of DAV. When any processed data are stored in data registers, the corresponding DAV bit is set to '1'. It stays at '1' until the register(s) updated to the processed data have been read out by the host.

Table 22. DAV Function

DAV	DESCRIPTION
0	No new processed data are available.
1	Processed data are available. This will stay at 1 until the host has read out all updated registers.

7.6.6.4 RESET Flag

See Table 23 for the interpretation of the RESET flag bits.

Table 23. RESET Flag Bits

RESET Flag	DESCRIPTION
0	Device was reset since last status poll (hardware or software reset).
1	Device has not been reset since last status poll.

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7.6.6.5 X CON

This bit is '1' if the X axis of the touch screen panel is properly connected to the X drivers. This bit is the connection test result.

7.6.6.6 Y CON

This bit is '1' if the Y axis of the touch screen panel is properly connected to the Y drivers. This bit is the connection test result.

7.6.6.7 Y SHR

This bit is '1' if there is no short-circuit tested at the Y axis of the touch screen panel. This bit is the short-circuit test result.

7.6.6.8 PDST

Power down status. This bit reflects the setting of the PND0 bit in Control Byte 0. When this bit shows '0', it indicates A/D converter bias circuitry is still powered on after each conversion and before the next sampling; otherwise, it indicates A/D converter bias circuitry is powered down after each conversion and before the next sampling. However, it is powered down between conversion sets. Because this status bit is synchronized with the internal clock, it does not reflect the setting of the PND0 bit until a pen touch is detected or a converter function is running.

7.6.6.9 ID[1:0]

Device ID bits: These bits represent the version ID of TSC2014. This version defaults to '00'.

7.6.7 Data Registers

The data registers of the TSC2014 hold data results from conversions. All of these registers default to 0000h upon reset.

7.6.7.1 X, Y, Z1, Z2, AUX, TEMP1 and TEMP2 Registers

The results of all A/D conversions are placed in the appropriate data registers, as described in Table 7. The data format of the result word (R) of these registers is right-justified, as shown in Figure 44.

The data registers of the TSC2014 hold data results from conversions. All of these registers default to 0000h upon reset.

Figure 44. Internal Register Format

MSB D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0
0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0

The TSC2014 has several 16-bit registers that allow control of the device, as well as providing a location to store results from the TSC2014 until read out by the host microprocessor. Table 24 shows the memory map.

Table 24. Register Content and Reset Values (1)

A3-A0 (HEX)	REGISTER NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	RESET VALUE (HEX)
0	X	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
1	Y	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
2	Z1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
3	Z2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
4	AUX	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
5	Temp1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
6	Temp2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
7	Status	S15	S14	S13	S12	S11	S10	S9	0	S7	S6	S5	Rsvd (2)	S3	S2	S1	S0	0004
8	AUX High	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0FFF
9	AUX Low	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
A	Temp High	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0FFF
B	Temp Low	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
C	CFR0	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	4000
D	CFR1	0	0	0	0	R11	R10	R9	R8	0	0	0	0	0	R2	R1	R0	0000
E	CFR2	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	0	R4	R3	R2	R1	R0	0000
F	Converter Function Select Status	R15	R14	R13	R12	Rsvd (2)	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000

(1) For all combination bits, the pattern marked as *Rsvd* (reserved) must not be used. The default pattern is read back after reset.
(2) This bit is reserved.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Communication with the TSC2014 is done via an I^2C serial interface. The TSC2014 is an I^2C slave device; therefore, data are shifted into or out of the TSC2014 under the control of the host microprocessor, which also provides the serial data clock.

Control of the TSC2014 and its functions is accomplished by writing to different registers in the TSC2014. A simple command protocol (compatible with I^2C) is used to address these registers. This protocol can be an I^2C write-addressing followed by multiple control bytes, or multiple combinations of control/data bytes to be written into different registers (two bytes each). Reading from registers is performed by writing an I^2C read-addressing to the TSC, followed by one or multiple sequential reads from the registers.

The address of the register to be read can be written in TSC Control Byte 0 with the register address and read-bit (as described in the previous paragraph), and serves as a pointer to the register map where the first read starts. This designated register address is static; there is no need to write a register address again unless it is overwritten by a new register address, or if the TSC is reset (by a software reset or by the $\overline{\text{RESET}}$ pin).

The measurement result is placed in the TSC2014 registers and may be read by the host at any time. This preprocessing frees up the host so that resources can be redirected for more critical tasks. Two optional signals are also available from the TSC2014 to indicate that data are available for the host to read. $\overline{\text{PINTDAV}}$ is a programmable interrupt/status output pin. When $\overline{\text{PINTDAV}}$ is programmed as a $\overline{\text{DAV}}$ output, it indicates that an A/D conversion has completed and that data are available. When this pin is programmed as a $\overline{\text{PENIRQ}}$ output, it indicates that a touch has been detected on the touch screen. The status register of the TSC2014 provides an extended status reading including the state of $\overline{\text{DAV}}$ and $\overline{\text{PENIRQ}}$ without the cost of any dedicated pin. Figure 45 shows a typical application of the TSC2014.

8.2 Typical Application

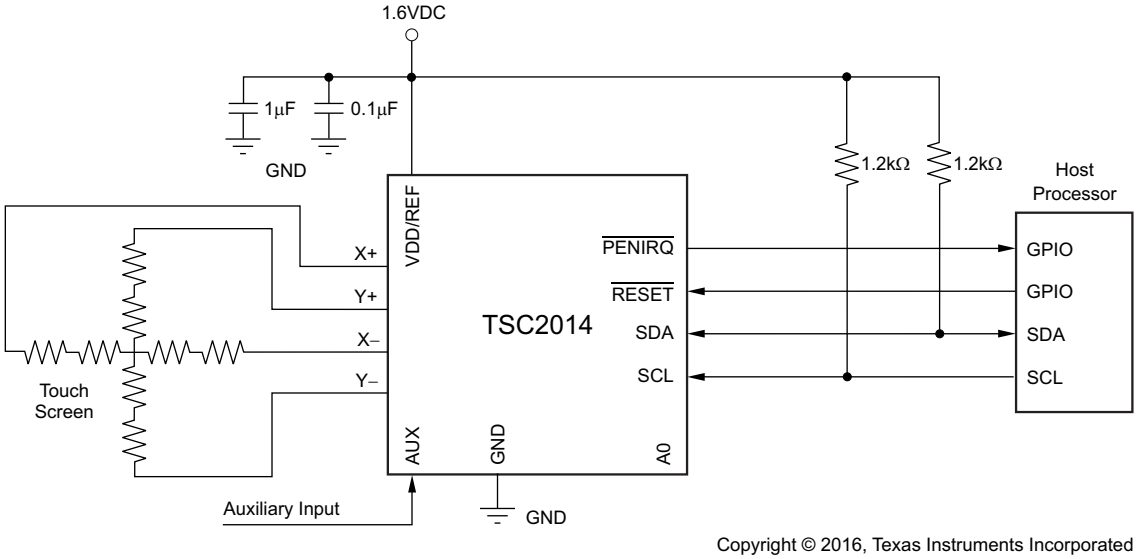

Figure 45. Typical Circuit Configuration

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters shown in Table 25.

Table 25. Design Parameters

PARAMETER	VALUE
Power Supply	1.6 V
Reset	$V_{IH} \geq 1.12$
	$V_{IL} \leq 0.48$
Touch Panel	4 Wire

8.2.2 Detailed Design Procedure

8.2.2.1 Auxiliary and Temperature Measurement

The TSC2014 can measure the voltage from the auxiliary input (AUX) and from the internal temperature sensor. Applications for the AUX can include external temperature sensing, ambient light monitoring for controlling backlighting, or sensing the current drawn from batteries. There are two converter functions that can be used for the measurement of the AUX:

1. Non-continuous AUX measurement shown in Figure 46 (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 0101); or
2. Continuous AUX Measurement shown in Figure 47 (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 1000).

   See Table 9 for more information on the converter function select bits.

There are also two converter functions for the measurement of the internal temperature sensor:

1. TEMP1 measurement (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 0110); or
2. TEMP2 measurement (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 0111).

   See Table 9 for more information on the converter function select bits.

For the detailed calculation of the internal temperature sensor, see the *Internal Temperature Sensor* section. These two converter functions have the same timing as the non-continuous AUX measurement operation as shown in Figure 46; therefore, Equation 12 can also be used for internal temperature sensor measurement. The time needed to make a non-continuous auxiliary measurement or an internal temperature sensor measurement is given by:

$$t_{COORDINATE} = \frac{OH3}{f_{OSC}} + N \cdot \left((B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV} \right) \cdot \left(\frac{1}{f_{OSC}} \right) + \left(\frac{L_{PPRO}}{f_{OSC}} \right) \tag{12}$$

Where:

OH3 = overhead time #3 = 3.5 internal clock cycles.

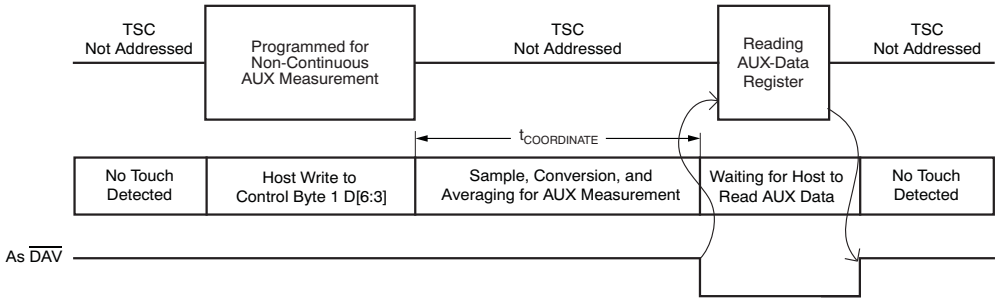

Figure 46. Non-Touch Screen, Non-Continuous AUX Measurement

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The time needed to make continuous auxiliary measurement is given by:

$$t_{COORDINATE} = \frac{OH3}{f_{OSC}} + N \cdot \left((B + 2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV} \right) \cdot \left(\frac{1}{f_{OSC}} \right) + \left(\frac{L_{PPRO}}{f_{OSC}} \right) \quad (13)$$

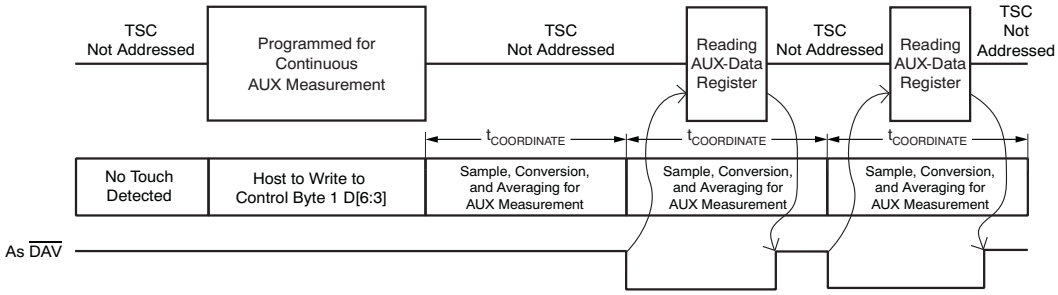

Figure 47. Non-Touch Screen, Continuous AUX Measurement

8.2.3 Application Curves

For application curves, see the figures listed in Table 26.

Table 26. Table of Graphs

DESCRIPTION	FIGURE NUMBER
V_{DD} Supply current vs Temperature	Figure 5
V_{DD} Supply current vs V_{DD}	Figure 6
Power-Down Supply Current vs Temperature	Figure 8
R_{ON} vs V_{DD}	Figure 10

9 Power Supply Recommendations

9.1 Power Supply Decoupling Capacitors

TSC2014 should be clean and well-bypassed. A 0.1-µF ceramic bypass capacitor should be added between (VDD/REF and GND). This capacitor must be placed as close to the device as possible. A 1-µF to 10-µF capacitor may also be needed if the impedance of the connection between VDD/REF and the power supply is high.

10 Layout

10.1 Layout Guidelines

The following layout suggestions should obtain optimum performance from the TSC2014. However, many portable applications have conflicting requirements for power, cost, size, and weight. In general, most portable devices have fairly clean power and grounds because most of the internal components are very low power. This situation would mean less bypassing for the converter power and less concern regarding grounding. Still, each application is unique and the following suggestions should be reviewed carefully.

For optimum performance, care should be taken with the physical layout of the TSC2014 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the SCL input.

With this in mind, power to the TSC2014 should be clean and well-bypassed. A 0.1-µF ceramic bypass capacitor should be added between (VDD/REF and GND). This capacitor must be placed as close to the device as possible. A 1-µF to 10-µF capacitor may also be needed if the impedance of the connection between VDD/REF and the power supply is high.

The A/D converter architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input, which is of particular concern when the reference input is tied to the power supply for auxiliary input and temperature measurements. Any noise and ripple from the supply appears directly in the digital results. While high-frequency noise can be filtered out by the built-in MAV filter, voltage variation as a result of line frequency (50Hz or 60Hz) can be difficult to remove. Some package options have pins labeled as NC (no connection). It is recommended that these NC pins be connected to the ground plane. Avoid any active trace going under the analog pins listed in the *Pin Assignments* table, unless they are shielded by a ground or power plane.

The GND pin should be connected to a clean ground point. In many cases, this point is the analog ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry or battery connection point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Because resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch-screen applications (for example, applications that require a back-lit LCD panel). This electromagnetic inference (EMI) noise can be coupled through the LCD panel to the touch screen and cause flickering of the converted A/D converter data. Several things can be done to reduce this error, such as using a touch screen with a bottom-side metal layer connected to ground, which couples the majority of noise to ground. Another way to filter out this type of noise is by using the TSC2014 built-in MAV filter (see the *Preprocessing* section). Filtering capacitors, from Y+, Y–, X+, and X– to ground, can also help. Note, however, that the use of these capacitors increases screen settling time and requires longer panel voltage stabilization times, and also increases precharge and sense times for the $\overline{\text{PINTDAV}}$ circuitry of the TSC2014. The resistor value varies depending on the touch screen sensor used. The internal 50kΩ pull-up resistor (R_{IRQ}) may be adequate for most of sensors.

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10.2 Layout Example

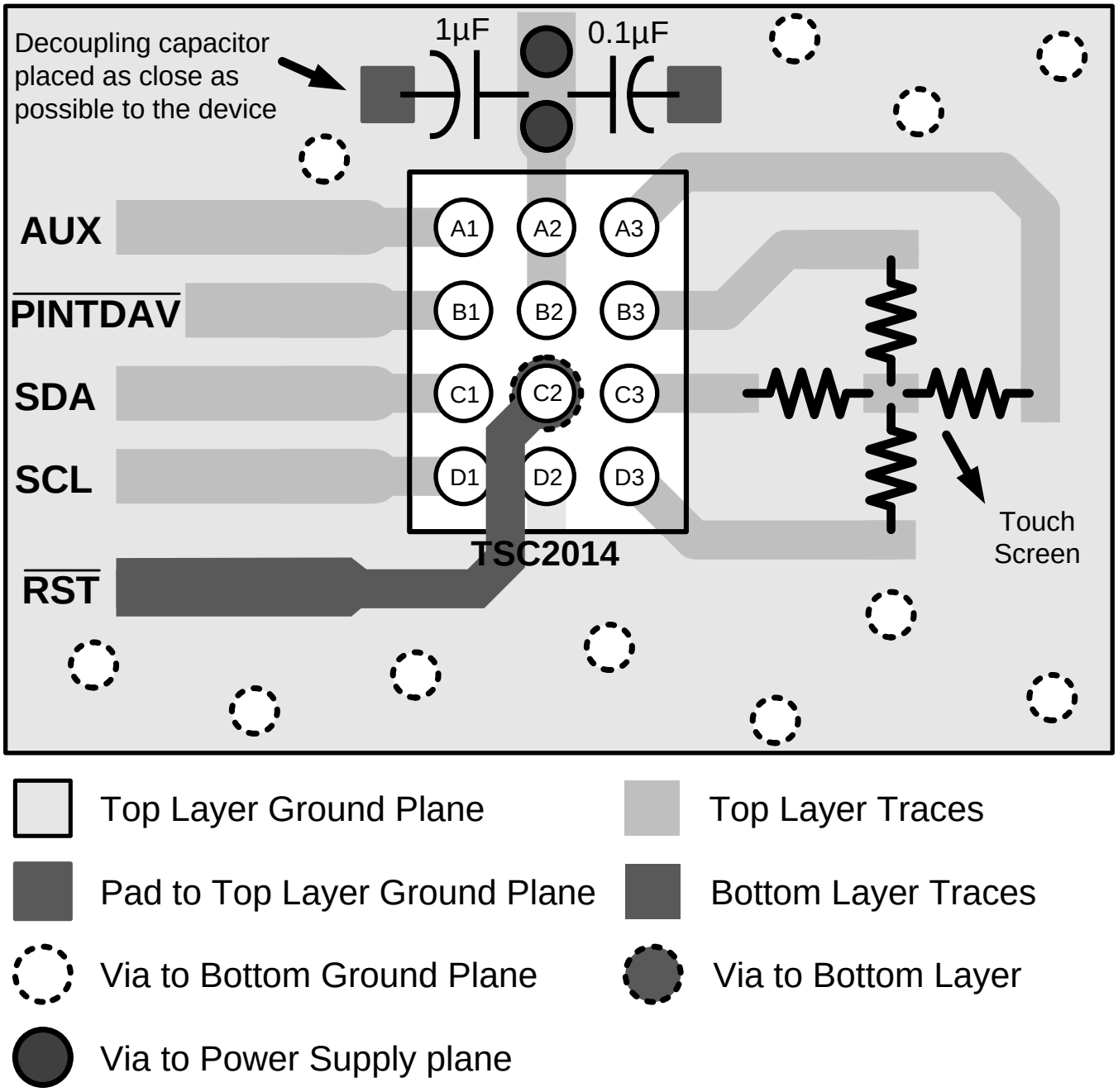

Figure 48. Example Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSC2014IYZGR	ACTIVE	DSBGA	YZG	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TSC2014I	Samples
TSC2014IYZGT	ACTIVE	DSBGA	YZG	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TSC2014I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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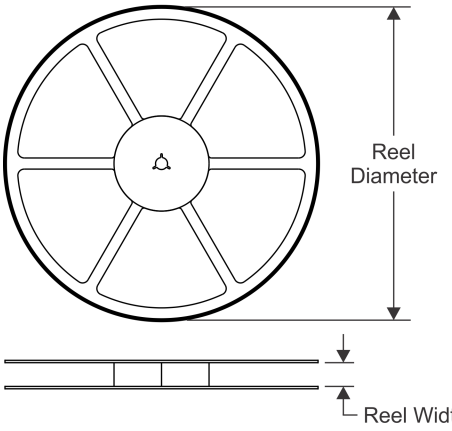
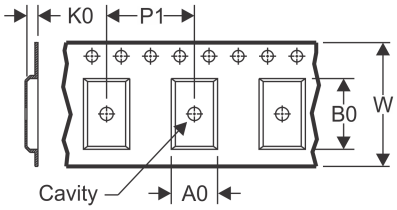
TAPE AND REEL INFORMATION

REEL DIMENSIONS

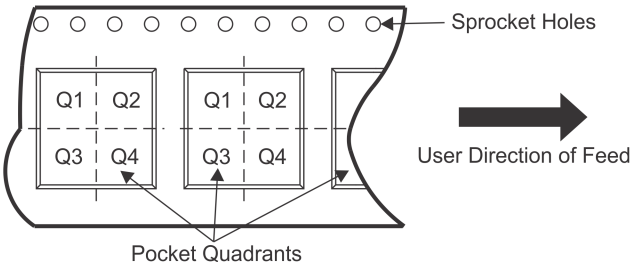


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

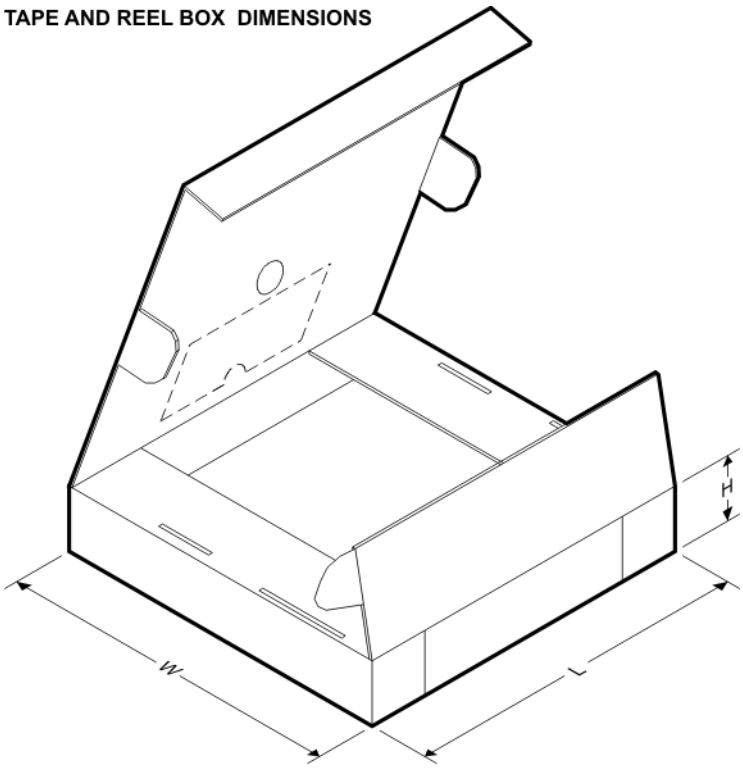
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSC2014IYZGR	DSBGA	YZG	12	3000	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1
TSC2014IYZGT	DSBGA	YZG	12	250	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1

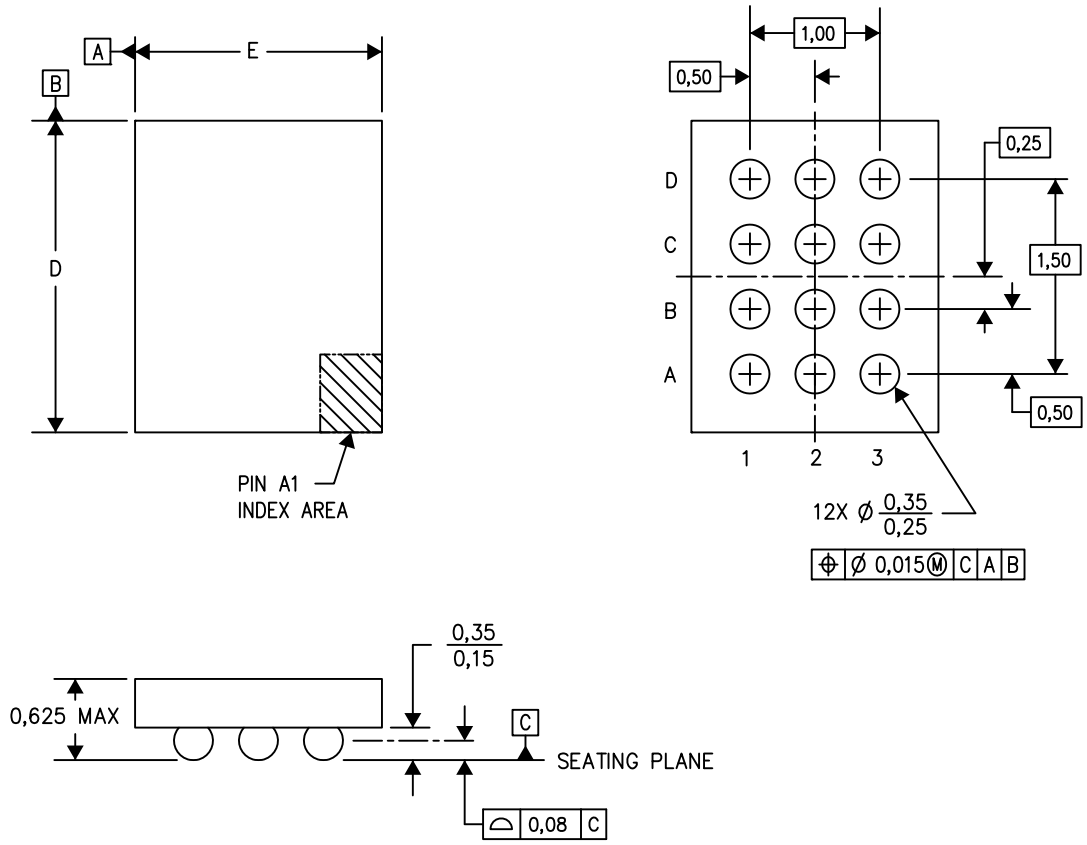
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSC2014IYZGR	DSBGA	YZG	12	3000	182.0	182.0	20.0
TSC2014IYZGT	DSBGA	YZG	12	250	182.0	182.0	20.0

YZG (R–XBGA–N12) DIE–SIZE BALL GRID ARRAY



4205059/E 07/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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