TEXAS INSTRUMENTS

UCC27323, UCC27324, UCC27325
UCC37323, UCC37324, UCC37325

ZHCSIU2J – JUNE 2001 – REVISED SEPTEMBER 2018

UCCx732x 双路 4A 峰值高速低侧电源 MOSFET 驱动器

1 特性

- Bi-CMOS 输出架构
- 可在米勒平坦区提供 ±4A 驱动电流
- 即使在低电源电压下也能实现恒流
- 并联输出以获得更高的驱动电流
- 可提供 MSOP-PowerPAD™封装
- 与电源电压无关的 TTL/CMOS 输入
- 行业标准引脚

2 应用

- 开关电源供电
- 直流/直流转换器
- 光伏逆变器、电机控制、UPS

3 说明

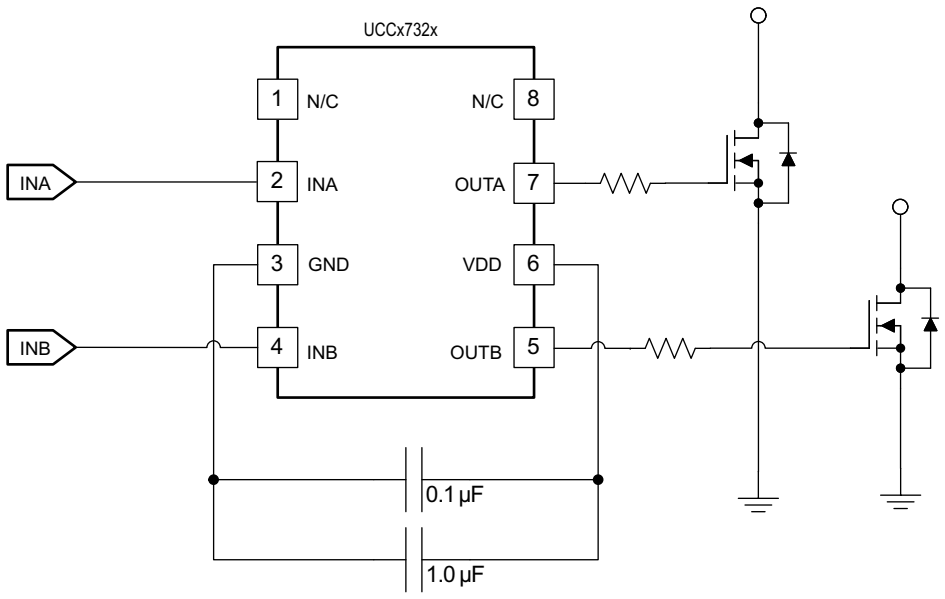
UCC2732x 和 UCC3732x 系列高速双路 MOSFET 驱动器提供 4A 峰值拉电流和 4A 峰值灌电流，以在米勒平坦区域提供最需要的高效 MOSFET 驱动。独特的双极和 MOSFET 混合输出级并联，可在低电源电压下实现高效的拉电流和灌电流。提供了 3 个标准逻辑选项的组合 - 双路反相、双路同相、一路反相和一路同相。输入阈值基于 TTL 和 CMOS，和电源电压无关，并具有能提供极佳防噪性能的宽输入迟滞。UCC2732x 和 UCC3732x 系列提供标准 SOIC-8 (D) 或 PDIP-8 (P) 封装以及热增强型 8 引脚 PowerPAD MSOP 封装 (DGN)，大大降低了热阻以改善长期可靠性。

器件信息(1)

器件	关键规格	封装
UCCx732x	-40C <= 温度 <= 125C 4.5V <= V_{DD} <= 15V 20ns/15ns - 1.8nF 负载时的上升/下降时间 35ns/25ns 上升/下降传播延迟	SOIC (8)：4.90mm × 3.91mm
		MSOP-PowerPAD (8)：3.00mm × 3.00mm
		PDIP (8)：9.81mm × 6.35mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化应用示意图



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本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision I (July 2016) to Revision J **Page**

- Changed NC description from "No connection: must be grounded" to "No Internal Connection" ... 4

Changes from Revision H (May 2013) to Revision I **Page**

- 已添加 *ESD 额定值* 表，*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- Deleted Power Dissipation rows from *Absolute Maximum Ratings* ... 5

Changes from Revision G (March 2010) to Revision H **Page**

- Changed $D_{SCHOTTKY}$ diode direction and voltage of zener diode from 5.5 to 4.5 V in Figure 7 ... 13
- Added three paragraphs after first paragraph of *Operational Waveforms and Circuit Layout* section before Figure 9 ... 16

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5 Device Comparison Table

OUTPUT CONFIGURATION	TEMPERATURE RANGE $T_A = T_J$	PACKAGED DEVICES(1)		
		SOIC-8 (D)	MSOP-8 PowerPAD (DGN)(2)	PDIP-8 (P)
Dual inverting	–40°C to +125°C	UCC27323D	UCC27323DGN	UCC27323P
	0°C to +70°C	UCC37323D	UCC37323DGN	UCC37323P
Dual noninverting	–40°C to +125°C	UCC27324D	UCC27324DGN	UCC27324P
	0°C to +70°C	UCC37324D	UCC37324DGN	UCC37324P
One inverting, one noninverting	–40°C to +125°C	UCC27325D	UCC27325DGN	UCC27325P
	0°C to +70°C	UCC37325D	UCC37325DGN	UCC37325P

(1) D (SOIC-8) and DGN (PowerPAD-MSOP) packages are available taped and reeled. Add R suffix to device type (for example UCC27323DR, UCC27324DGNR) to order quantities of 2,500 devices per reel for D or 1,000 devices per reel for DGN package.
(2) The PowerPAD is not directly connected to any leads of the package. However, the PowerPAD is electrically and thermally connected to the substrate which is the ground of the device.

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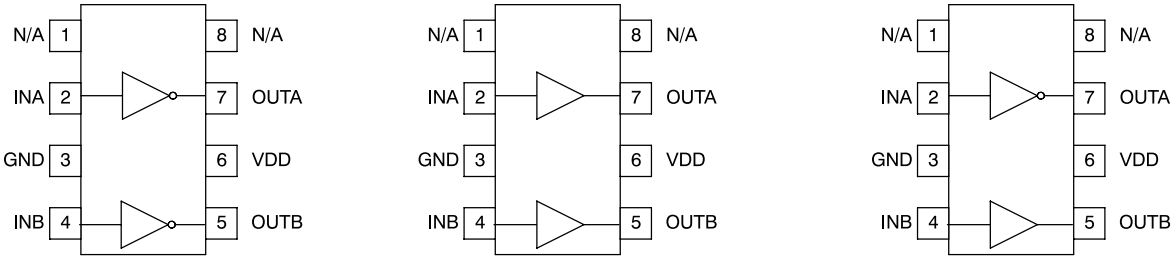
6 Pin Configuration and Functions

D, DGN, or P Package
8-Pin SOIC, MSOP With PowerPAD, or PDIP
Top View



(DUAL INVERTING) **(DUAL NONINVERTING)** **(ONE INVERTING, ONE NONINVERTING)**

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	3	—	**Common ground**: This ground should be connected very closely to the source of the power MOSFET which the driver is driving.
INA	2	I	**Input A**: Input signal of the A driver which has logic compatible threshold and hysteresis. If not used, this input must be tied to either VDD or GND; it must not be left floating.
INB	4	I	**Input B**: Input signal of the A driver which has logic compatible threshold and hysteresis. If not used, this input must be tied to either VDD or GND; it must not be left floating.
N/C	1	—	**No Internal Connection**
N/C	8	—	**No Internal Connection**
OUTA	7	O	**Driver output A**: The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
OUTB	5	O	**Driver output B**: The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
VDD	6	I	**Supply**: Supply voltage and the power input connection for this device.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
	Analog input voltage (INA, INB)		–0.3 to V_{DD} + 0.3 V	not to exceed 16	V
	Output body diode DC current (OUTA, OUTB)			0.2	A
I_{OUT_DC}	Output current (OUTA, OUTB)	DC		0.2	
I_{OUT_PULSED}		Pulsed (0.5 µs)		4.5	
	Output voltage (OUTA, OUTB)			16	V
V_{DD}	Supply voltage		–0.3	16	V
T_J	Junction operating temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage		4.5		15	V
Input voltage		0		15	V
Operating junction temperature	UCC2732x	–40		125	°C
	UCC3732x	0		70	°C

7.4 Thermal Information

THERMAL METRIC(1)		UCCx732x			UNIT
		D (SOIC)	DGN (MSOP With PowerPAD)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.3	56.6	55.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.2	52.8	45.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.3	32.6	32.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.2	1.8	23	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.8	32.3	32.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	5.9	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

V_{DD} = 4.5 to 15 V, $T_A = T_J$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (INA, INB)						
V_{IN_H}	Logic 1 input threshold		2			V
V_{IN_L}	Logic 0 input threshold				1	
	Input current	0 V ← V_{IN} ← V_{DD}	–10		10	µA
OUTPUT (OUTA, OUTB)						
	Output current	V_{DD} = 14 V (1)		4		A
V_{OH}	High-level output voltage	$V_{OH} = V_{DD} – V_{OUT}$, I_{OUT} = –10 mA		300	450	mV
V_{OL}	Low-level output level	I_{OUT} = 10 mA		22	45	
	Output resistance high	T_A = 25°C, I_{OUT} = –10 mA, V_{DD} = 14 V (2)	25	30	35	Ω
		T_A = full range, I_{OUT} = –10 mA, V_{DD} = 14 V (2)	18		42	
	Output resistance low	T_A = 25°C, I_{OUT} = 10 mA, V_{DD} = 14 V (2)	1.9	2.2	2.5	
		T_A = full range, I_{OUT} = 10 mA, V_{DD} = 14 V (2)	1.2		4	
	Latch-up protection		500			mA
OVERALL						
I_{DD}	Static Operating Current	UCCx7323 INA = 0 V, INB = 0 V		300	450	µA
		UCCx7323 INA = 0 V, INB = HIGH		300	450	
		UCCx7323 INA = HIGH, INB = 0 V		300	450	
		UCCx7323 INA = HIGH, INB = HIGH		300	450	
		UCCx7324 INA = 0 V, INB = 0 V		2	50	
		UCCx7324 INA = 0 V, INB = HIGH		300	450	
		UCCx7324 INA = HIGH, INB = 0 V		300	450	
		UCCx7324 INA = HIGH, INB = HIGH		600	750	
		UCCx7325 INA = 0 V, INB = 0 V		150	300	
		UCCx7325 INA = 0 V, INB = HIGH		450	600	
		UCCx7325 INA = HIGH, INB = 0 V		150	300	
		UCCx7325 INA = HIGH, INB = HIGH		450	600	

(1) The pullup and pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The pulsed output current rating is the combined current from the bipolar and MOSFET transistors.
(2) The pullup and pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_R	Rise time (OUTA, OUTB)	C_{LOAD} = 1.8 nF, see Figure 1		20	40	ns
T_F	Fall time (OUTA, OUTB)	C_{LOAD} = 1.8 nF, see Figure 1		15	40	
T_{D1}	Delay, IN rising (IN to OUT)	C_{LOAD} = 1.8 nF, see Figure 1		25	40	
T_{D2}	Delay, IN falling (IN to OUT)	C_{LOAD} = 1.8 nF, see Figure 1		35	35	

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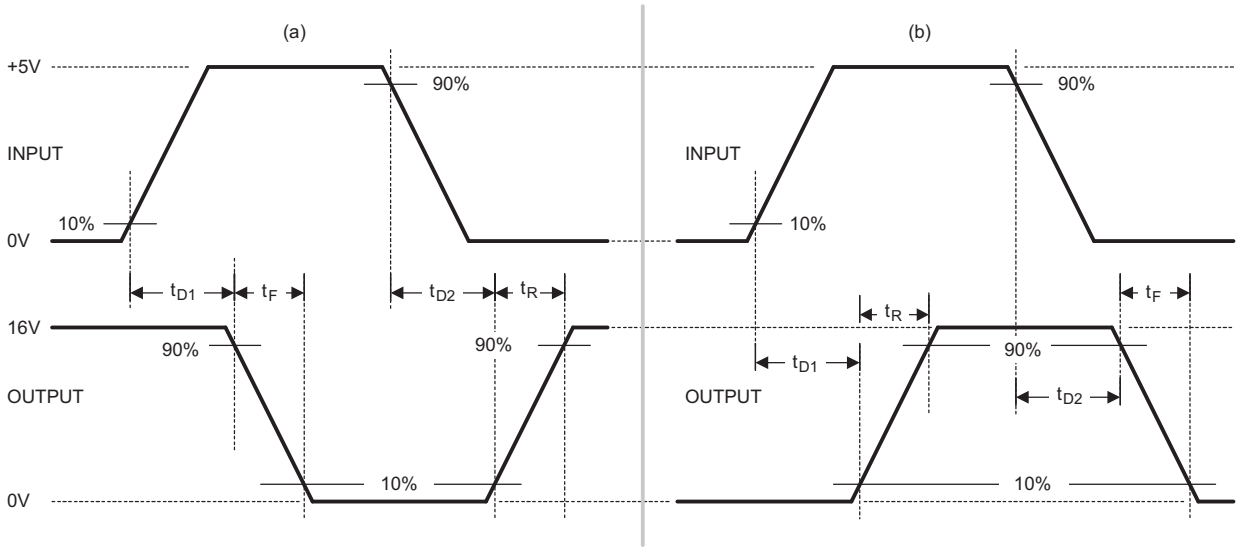

Figure 1. Switching Waveforms for (a) Inverting Driver and (b) Noninverting Driver

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7.7 Typical Characteristics

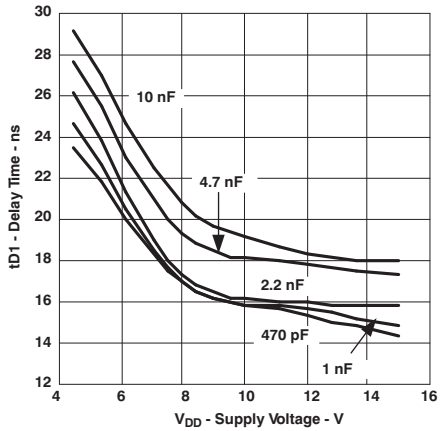

Figure 2. Delay Time (t_{D1}) vs Supply Voltage

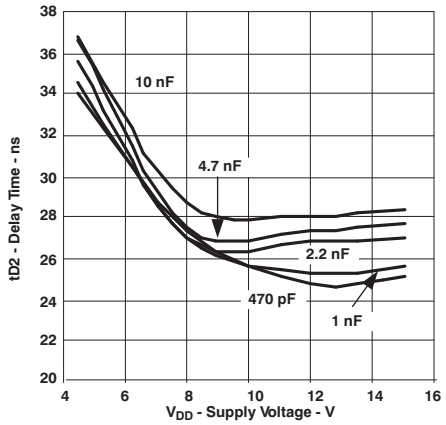

Figure 3. Delay Time (t_{D2}) vs Supply Voltage

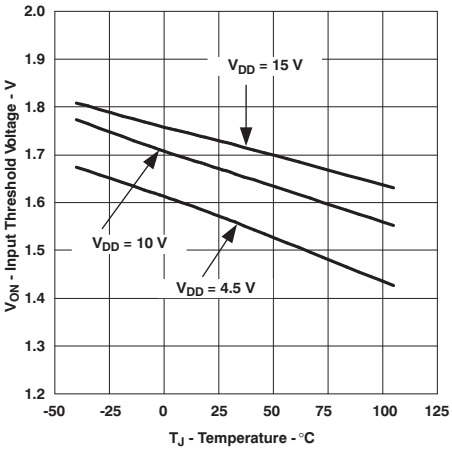

Figure 4. Input Threshold vs Temperature

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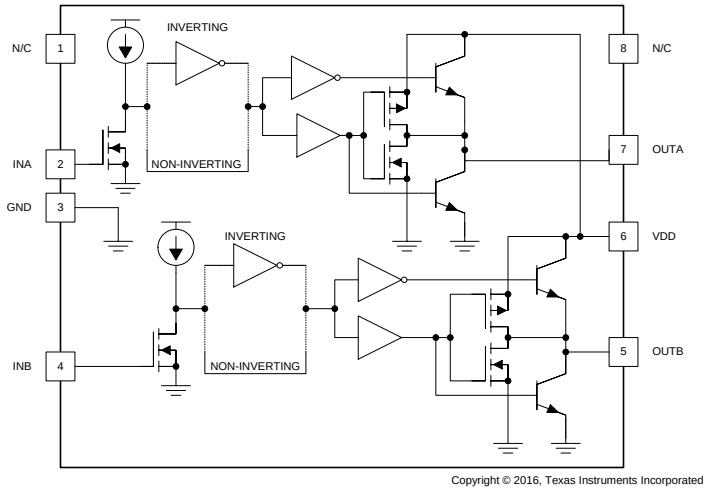
8 Detailed Description

8.1 Overview

The UCC2732x and UCC3732x family of high-speed dual MOSFET drivers can deliver large peak currents into capacitive loads. Three standard logic options are offered – dual-inverting, dual-noninverting and one-inverting and one-noninverting driver. Using a design that inherently minimizes shoot-through current, these drivers deliver 4A of current where it is needed most at the Miller plateau region during the MOSFET switching transition. A unique Bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing and sinking at low supply voltages.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Input Stage

The input thresholds have a 3.3-V logic sensitivity over the full range of V_{DD} voltage; yet it is equally compatible with 0 V to V_{DD} signals.

The inputs of UCC2732x and UCC3732x family of drivers are designed to withstand 500-mA reverse current without either damage to the IC for logic upset. The input stage of each driver must be driven by a signal with a short rise or fall time. This condition is satisfied in typical power-supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The input stages to the drivers function as a digital gate, and are not intended for applications where a slow-changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limited rise or fall times to the power device is desired, an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor may also help remove power dissipation from the device package, as discussed in (see *Thermal Considerations*).

Importantly, input signal of the two channels, INA and INB, which has logic compatible threshold and hysteresis. If not used, INA and INB must be tied to either VDD or GND; it must not be left floating.

8.3.2 Output Stage

Inverting outputs of the UCCx7323 and OUTA of the UCCx7325 are intended to drive external P-channel MOSFETs. Noninverting outputs of the UCCx7324 and OUTB of the UCCx7325 are intended to drive external N-Channel MOSFETs.

Feature Description (continued)

Each output stage is capable of supplying ±4-A peak current pulses and swings to both VDD and GND. The pullup and pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the external MOSFET.

This means that in many cases, external-Schottky-clamp diodes are not required. The UCCx732x family delivers 4 A of gate drive where it is most needed during the MOSFET switching transition – at the Miller plateau region – providing improved efficiency gains. A unique Bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing at low supply voltages.

8.4 Device Functional Modes

With VDD power supply in the range of 4.5 V to 15 V, the output stage is dependent on the states of the HI and LI pins. Table 1 shows the UCCx732x truth table.

Table 1. Input and Output Table

INPUTS (VIN_L, VIN_H)		UCC37323x		UCC37324x		UCC37325x	
INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
L	L	H	H	L	L	H	L
L	H	H	L	L	H	H	H
H	L	L	H	H	L	L	L
H	H	L	L	H	H	L	H

Importantly, if INA and INB are not used, they must be tied to either VDD or GND; it must not be left floating.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

High-frequency power supplies often require high-speed, high-current drivers such as the UCCx732x family. A leading application is the needed to provide a high-power buffer stage between the PWM output of the control IC and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the driver IC is used to drive the power-device gates through a drive transformer. Synchronous rectification supplies are also needed to simultaneously drive multiple devices which presents an extremely large load to the control circuitry.

Driver ICs are used when having the primary PWM regulator IC directly drive the switching devices for one or more reasons is not feasible. The PWMIC does not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases there may be a desire to minimize the effect of high-frequency switching noise by placing the high current driver physically close to the load. Also, newer ICs that target the highest operating frequencies do not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high impedance input to a driver such as the UCCx732x. Finally, the control IC is under thermal stress due to power dissipation, and an external driver helps by moving the heat from the controller to an external package.

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9.2 Typical Application

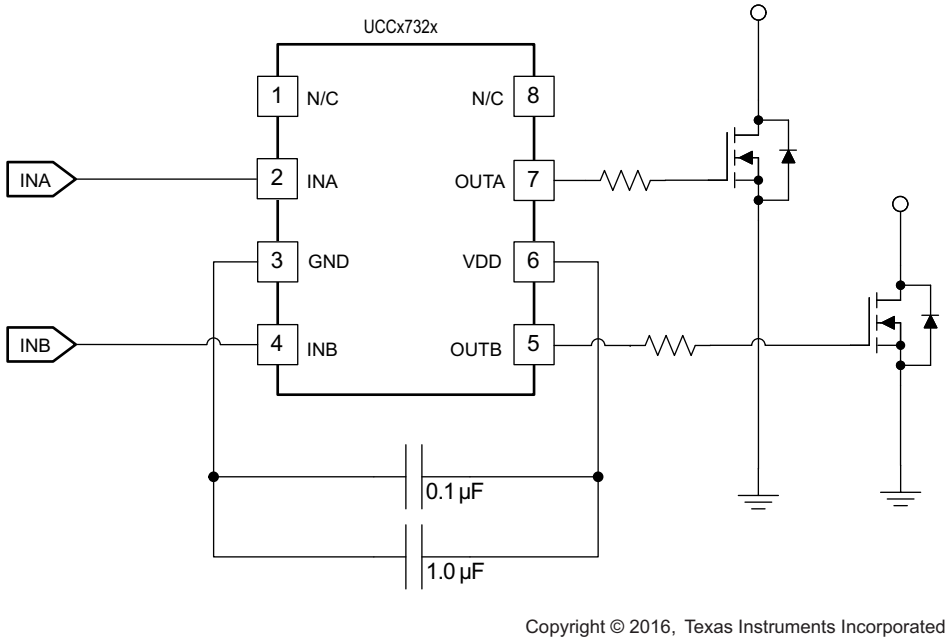

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Figure 5. UCCx732x Driving Two Independent MOSFETs

9.2.1 Design Requirements

To select proper device from UCCx732x family, TI recommends first checking the appropriate logic for the outputs. UCCx7323 has dual inverting outputs; UCCx7324 has dual noninverting outputs; UCCx7325 have inverting channel A and noninverting channel B. Moreover, some design considerations must be evaluated first in order to make the most appropriate selection. Among these considerations are VDD, drive current, and power dissipation.

9.2.2 Detailed Design Procedure

9.2.2.1 Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCCx732x drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver device [1].

Two circuits are used to test the current capabilities of the UCCx732x driver. In each case external circuitry is added to clamp the output near 5 V while the IC is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test there is a transient period where the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient. [1]

The first circuit in Figure 6 is used to verify the current sink capability when the output of the driver is clamped around 5 V, a typical value of gate-source voltage during the Miller plateau region. The UCCx7323 is found to sink 4.5 A at VDD = 15 V and 4.28 A at VDD = 12 V.

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Typical Application (continued)

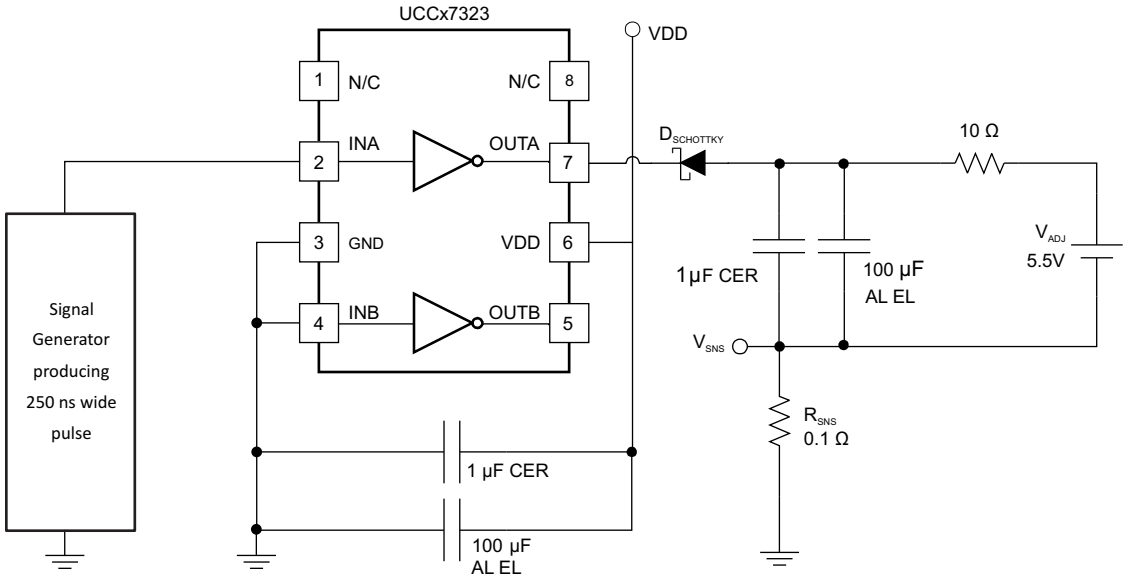

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Figure 6. Current Sink Capability Test

The circuit shown in Figure 7 is used to test the current source capability with the output clamped to around 5 V with a string of Zener diodes. The UCCx7323 is found to source 4.8 A at VDD = 15 V and 3.7 A at VDD = 12 V.

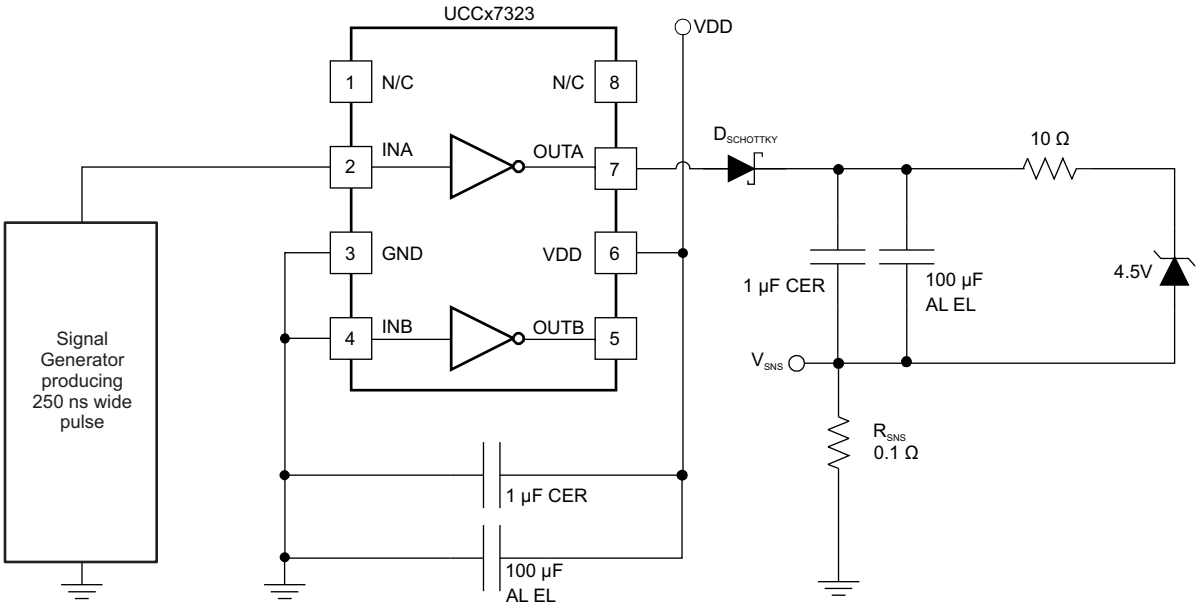

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Figure 7. Current Source Capability Test

Typical Application (continued)

9.2.2.2 Parallel Outputs

The A and B drivers may be combined into a single driver by connecting the INA/INB inputs together as close to the IC as possible, and the OUTA/OUTB outputs ties together if the external gate drive resistor is not used. In some cases where the external gate drive resistor is used, Ti recommends that the resistor can be equally split in OUTA and OUTB respectively to reduce the parasitic inductance induce unbalance between two channels, as show in Figure 8.

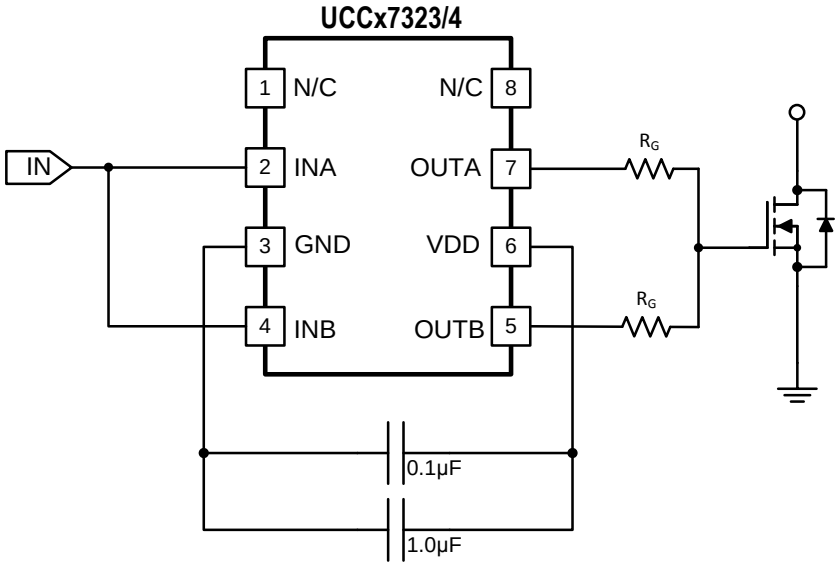

Figure 8. Parallel Operation of UCCx7323 and UCCx7324

Important consideration about paralleling two channels for UCCx7323/4 include: 1) INA and INB should be shorted in PCB layout as close to the device as possible, as well as for OUTA and OUTB, in which condition PCB layout parasitic mismatching between two channels could be minimized. 2) INA/B input slope signal should be fast enough to avoid mismatched V_{IN_H}/V_{IN_L}, t_{d1}/t_{d2} between channel-A and channel-B. TI recommends having input signal slope faster than 20 V/us.

9.2.2.3 VDD

Although quiescent VDD current is very low, total supply current will be higher, depending on OUTA and OUTB current and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated using Equation 1.

$$I_{OUT} = Q_g \times f$$

where f is frequency (1)

For the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-µF ceramic capacitor should be located closest to the VDD to ground connection. In addition, a larger capacitor (such as 1 µF and above) with relatively low ESR should be connected in parallel, to help deliver the high current peaks to the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels in the driver application.

9.2.2.4 Driver Current and Power Requirements

The UCCx732x family of drivers is capable of delivering 4 A of current to a MOSFET gate for a period of tens of nanoseconds. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. A MOSFET is used in this discussion because it is the most common type of switching device used in high-frequency power conversion equipment.

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Typical Application (continued)

Reference [1] and reference [2] discuss the current required to drive a power MOSFET and other capacitive-input switching devices. Reference [2] includes information on the previous generation of bipolar IC gate drivers.

When a driver IC is tested with a discrete, capacitive load, it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 2.

$$E = ½CV^2$$

where

- C is the load capacitor
- V is the bias voltage feeding the driver (2)

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by Equation 3.

$$P = CV^2 \times f$$

where f is the switching frequency (3)

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as Equation 4.

$$P = 10\ nF \times (12\ V)^2 \times (300\ kHz) = 0.432\ W \quad (4)$$

With a 12-V supply, this equates to a current of (see Equation 5):

$$I = P/V = 0.432\ W / 12\ V = 36\ mA \quad (5)$$

The actual current measured from the supply was 0.037 A, and is very close to the predicted value. But, the I_{DD} current that is due to the IC internal consumption should be considered. With no load the IC current draw is 0.0027 A. Under this condition the output rise and fall times are faster than with a load. This could lead to an almost insignificant, yet measurable current due to cross-conduction in the output stages of the driver. However, these small current differences are buried in the high frequency switching spikes, and are beyond the measurement capabilities of a basic lab setup. The measured current with 10-nF load is reasonably close to that expected.

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence $Q_g = C_{eff} \times V$ to provide Equation 6 for power:

$$P = C \times V^2 \times f = V \times Q_g \times f \quad (6)$$

Equation 6 allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage and a specific switching frequency.

9.2.3 Application Curves

Figure 9 shows the circuit performance achievable with a single driver (half of the 8-pin IC) driving a 10-nF load. The input pulse width (not shown) is set to 300 ns to show both transitions in the output waveform. Note the linear rise and fall edges of the switching waveforms which is due to the constant output current characteristic of the driver as opposed to the resistive output impedance of traditional MOSFET-based gate drivers.

Sink and source currents of the driver are dependent upon the VDD value and the output capacitive load. The larger the VDD value, the higher the current capability; also, the larger the capacitive load, the higher the current sink and source capability.

Trace resistance and inductance, including wires and cables for testing, slows down the rise and fall times of the outputs; thus reducing the current capabilities of the driver.

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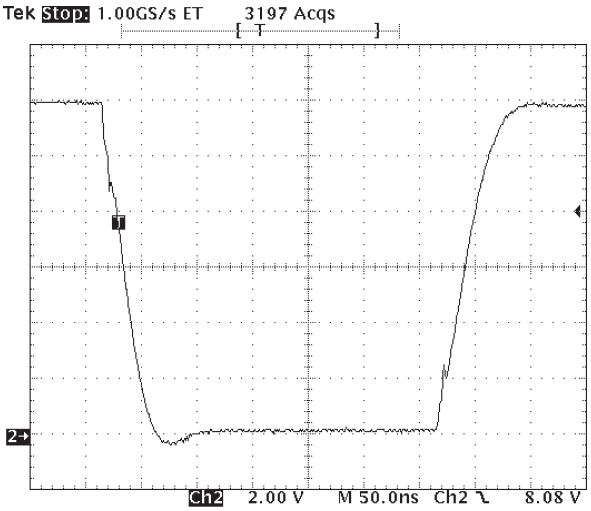
Typical Application (continued)

To achieve higher current results, reduce resistance and inductance on the board as much as possible and increase the capacitive load value in order to swamp out the effect of inductance values.



C_L = 10 nF, C_L = 10 nF, VDD = 12 V

Figure 9. Rising and Falling Time of UCCx732x

10 Power Supply Recommendations

The recommended bias supply voltage range for UCCx732x is from 4.5 V to 15 V. The upper end of this range is driven by the 16 V absolute maximum voltage rating of the VDD. TI recommends keeping proper margin to allow for transient voltage spikes.

A local bypass capacitor must be placed between the VDD and GND pins. And this capacitor must be placed as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. TI recommends using 2 capacitors across VDD and GND: a 100-nF ceramic surface-mount capacitor for high frequency filtering placed very close to VDD and GND pin, and another surface-mount capacitor, 220 nF to
10 µF, for IC bias requirements.

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11 Layout

11.1 Layout Guidelines

Optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1) Low ESR/ESL capacitors must be connected close to the IC between VDD and GND pins to support high peak currents drawn from VDD during the turn-on of the external MOSFETs.

2) Grounding considerations:

The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. The gate driver must be placed as close as possible to the MOSFETs.

Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected to the other circuit nodes such as source of power MOSFET and ground of PWM controller at one, single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.

Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

3) In noisy environments, tying inputs of an unused channel of the UCC2742x device to VDD or GND using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output may be necessary.

4) Separate power traces and signal traces, such as output and input signals.

11.2 Layout Example

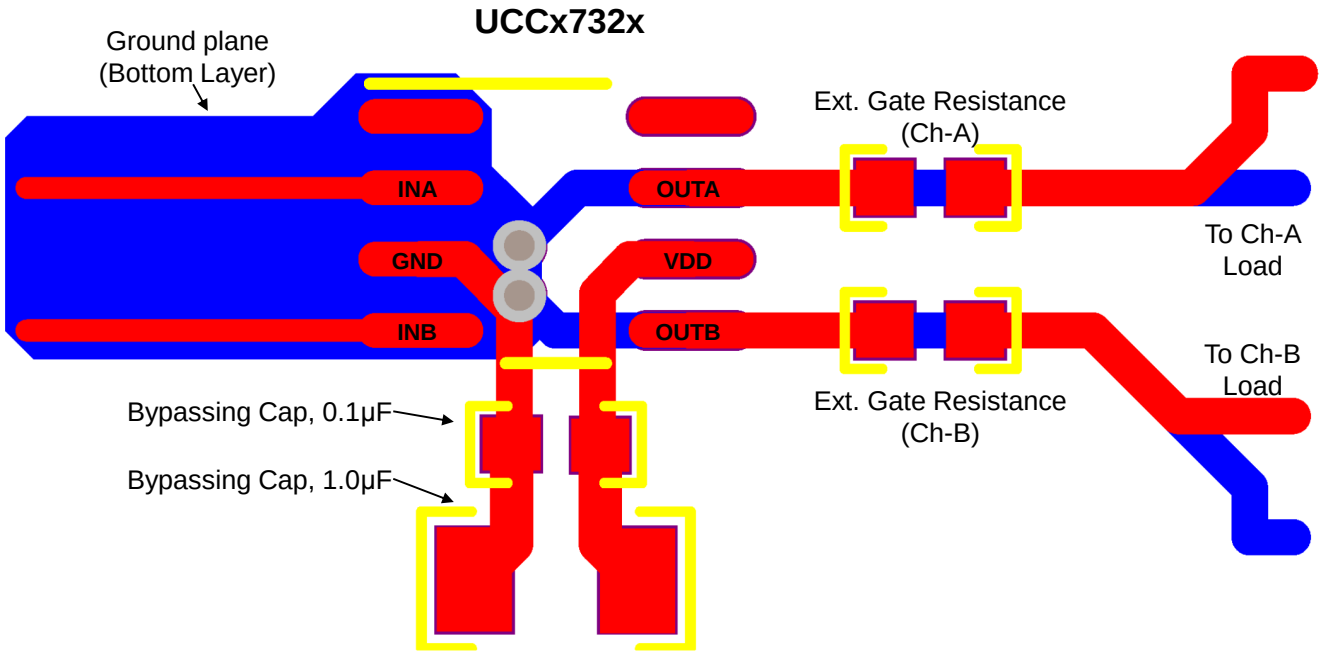

Figure 10. Recommended PCB Layout for UCCx732x

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11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the IC package. In order for a power driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCCx732x family of drivers is available in three different packages to cover a range of application requirements.

The MSOP PowerPAD-8 (DGN) package significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As illustrated in reference [3], the PowerPAD packages offer a lead-frame die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board directly underneath the IC package, reducing the θ_{JC} down to 4.7°C/W. Data is presented in reference [3] to show that the power dissipation can be quadrupled in the PowerPAD configuration when compared to the standard packages. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in reference [4]. This design allows a significant improvement in heat sinking over that which is available in the D or P packages, and is shown to more than double the power capability of the D and P packages.

NOTE

The PowerPAD is not directly connected to any leads of the package. However, the PowerPad is electrically and thermally connected to the substrate which is the ground of the device.

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12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

1. SEM-1400 电源设计研讨会主题 2，*《高速 MOSFET 栅极驱动电路设计和应用指南》* (SLUP133)
2. *《高性能 MOSFET、IGBT 和 MCT 栅极驱动电路的实用注意事项》* (SLUA105)
3. *《PowerPad 热增强型封装》* (SLMA002)
4. *《PowerPAD 速成》*（文献编号：SLMA004）

12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **2.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
UCC27323	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCC27324	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCC27325	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCC37323	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCC37324	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCC37325	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.5 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27323D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27323	Samples
UCC27323DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27323	Samples
UCC27323DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27323	Samples
UCC27323DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27323	Samples
UCC27323DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27323	Samples
UCC27323DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27323	Samples
UCC27323P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	UCC27323P	Samples
UCC27324D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324DGNG4	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324DGNRG4	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	UCC27324P	Samples
UCC27324PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	UCC27324P	Samples
UCC27325D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27325	Samples
UCC27325DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27325	Samples
UCC27325DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27325	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27325DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27325	Samples
UCC27325P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	UCC27325P	Samples
UCC27325PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	UCC27325P	Samples
UCC37323D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	37323	Samples
UCC37323DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37323	Samples
UCC37323DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37323	Samples
UCC37323DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	37323	Samples
UCC37323P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UCC37323P	Samples
UCC37324D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	37324	Samples
UCC37324DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	37324	Samples
UCC37324DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37324	Samples
UCC37324DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37324	Samples
UCC37324DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	37324	Samples
UCC37324P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UCC37324P	Samples
UCC37324PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UCC37324P	Samples
UCC37325D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	37325	Samples
UCC37325DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37325	Samples
UCC37325DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37325	Samples
UCC37325DGNRG4	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37325	Samples
UCC37325DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	37325	Samples
UCC37325P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UCC37325P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC27324 :

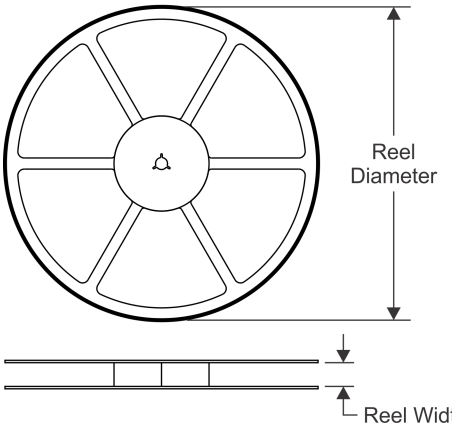
- Automotive : UCC27324-Q1

NOTE: Qualified Version Definitions:

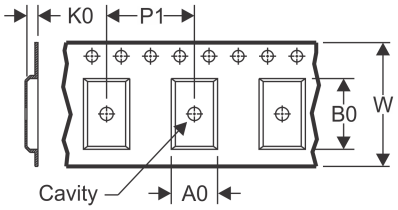
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

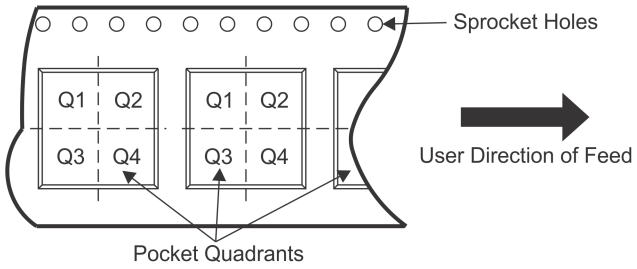


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

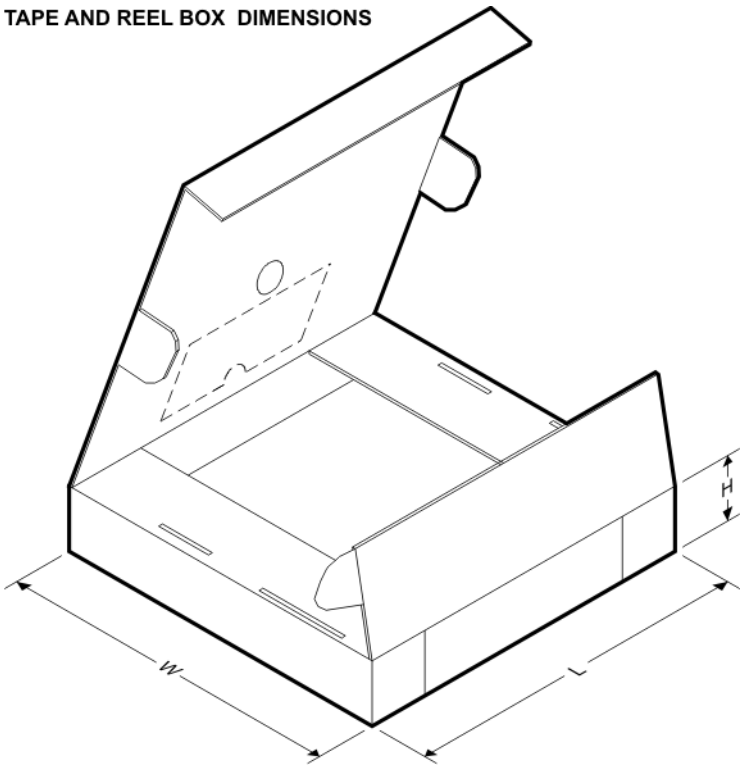
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27323DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27323DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27324DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27324DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27324DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27324DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27325DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27325DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37323DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37323DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37324DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37324DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37325DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37325DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

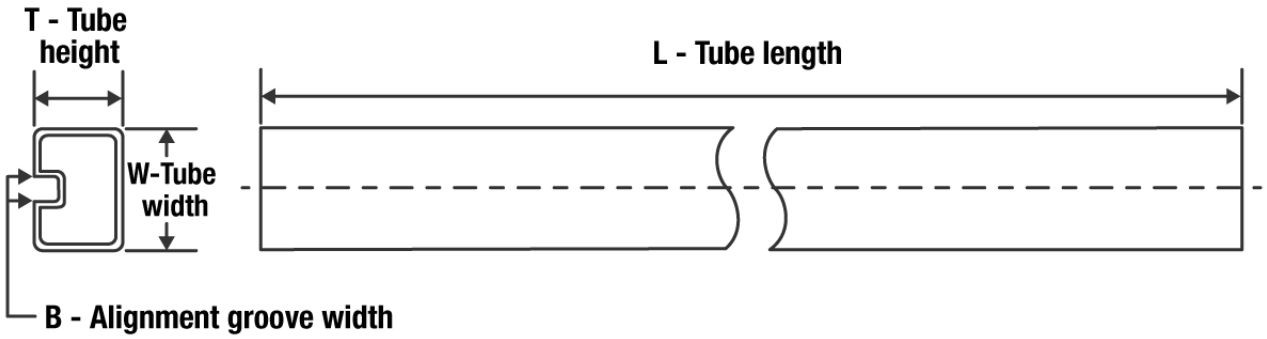
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27323DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC27323DR	SOIC	D	8	2500	340.5	336.1	25.0
UCC27324DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC27324DGNR	HVSSOP	DGN	8	2500	346.0	346.0	29.0
UCC27324DR	SOIC	D	8	2500	853.0	449.0	35.0
UCC27324DR	SOIC	D	8	2500	340.5	336.1	25.0
UCC27325DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC27325DR	SOIC	D	8	2500	340.5	336.1	25.0
UCC37323DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC37323DR	SOIC	D	8	2500	340.5	336.1	25.0
UCC37324DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC37324DR	SOIC	D	8	2500	340.5	336.1	25.0
UCC37325DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC37325DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC27323D	D	SOIC	8	75	507	8	3940	4.32
UCC27323DG4	D	SOIC	8	75	507	8	3940	4.32
UCC27323DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC27323P	P	PDIP	8	50	506	13.97	11230	4.32
UCC27324D	D	SOIC	8	75	507	8	3940	4.32
UCC27324DG4	D	SOIC	8	75	507	8	3940	4.32
UCC27324DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC27324DGNG4	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC27324P	P	PDIP	8	50	506	13.97	11230	4.32
UCC27324PE4	P	PDIP	8	50	506	13.97	11230	4.32
UCC27325D	D	SOIC	8	75	507	8	3940	4.32
UCC27325DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC27325P	P	PDIP	8	50	506	13.97	11230	4.32
UCC27325PE4	P	PDIP	8	50	506	13.97	11230	4.32
UCC37323D	D	SOIC	8	75	507	8	3940	4.32
UCC37323DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC37323P	P	PDIP	8	50	506	13.97	11230	4.32
UCC37324D	D	SOIC	8	75	507	8	3940	4.32
UCC37324DG4	D	SOIC	8	75	507	8	3940	4.32
UCC37324DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC37324P	P	PDIP	8	50	506	13.97	11230	4.32
UCC37324PE4	P	PDIP	8	50	506	13.97	11230	4.32
UCC37325D	D	SOIC	8	75	507	8	3940	4.32
UCC37325DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC37325P	P	PDIP	8	50	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

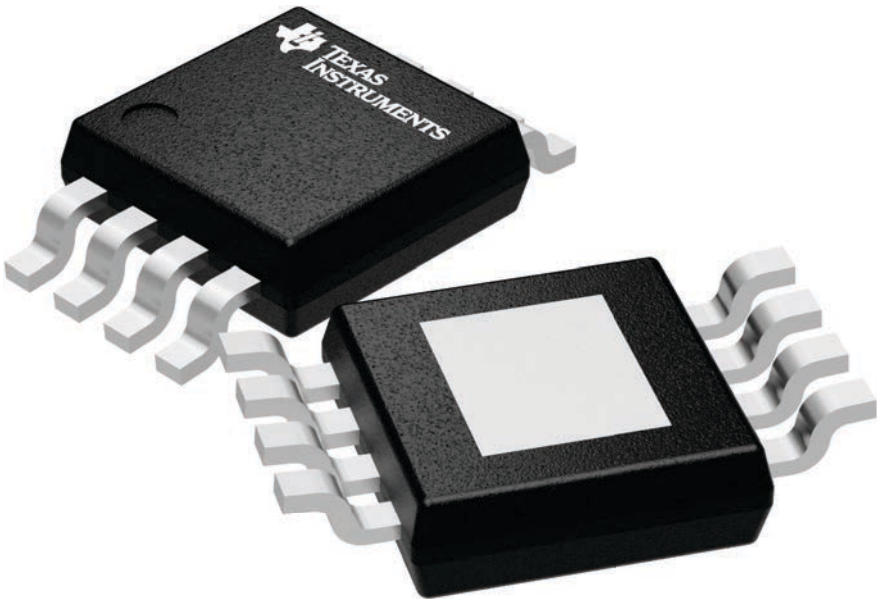
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

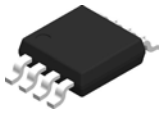
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

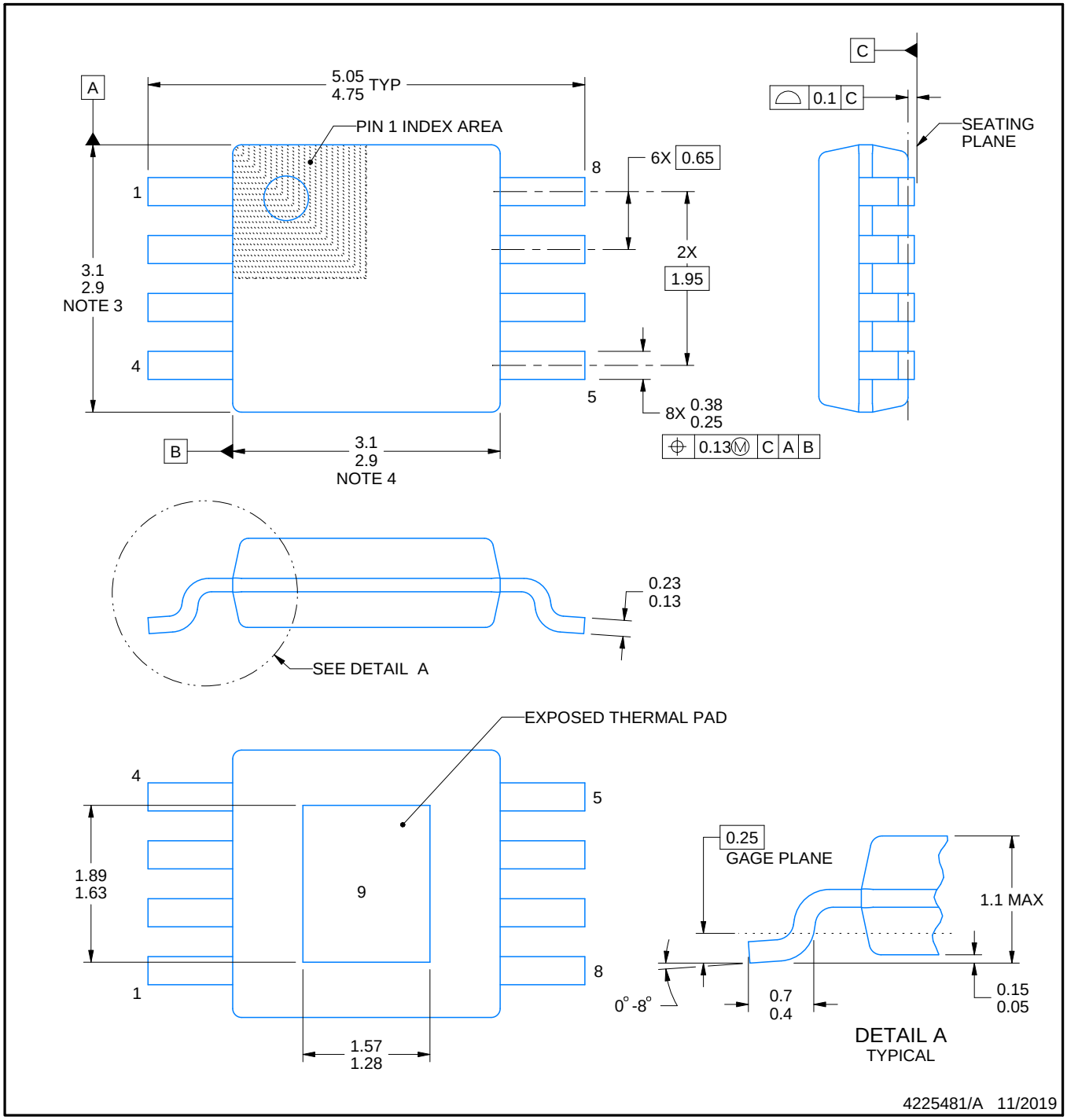
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

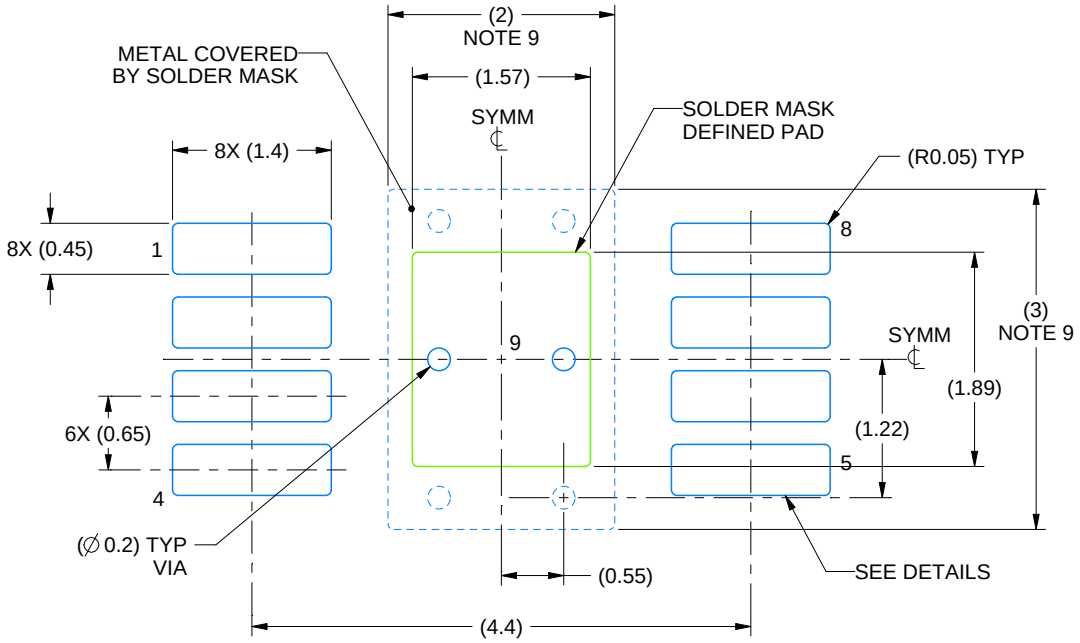
SMALL OUTLINE PACKAGE



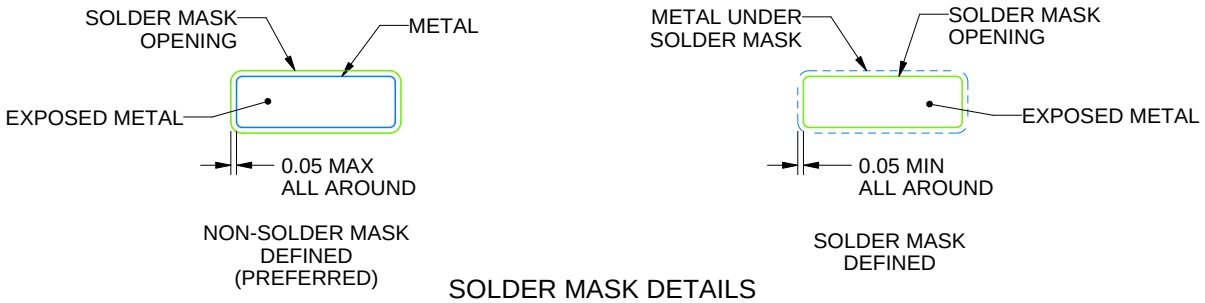
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

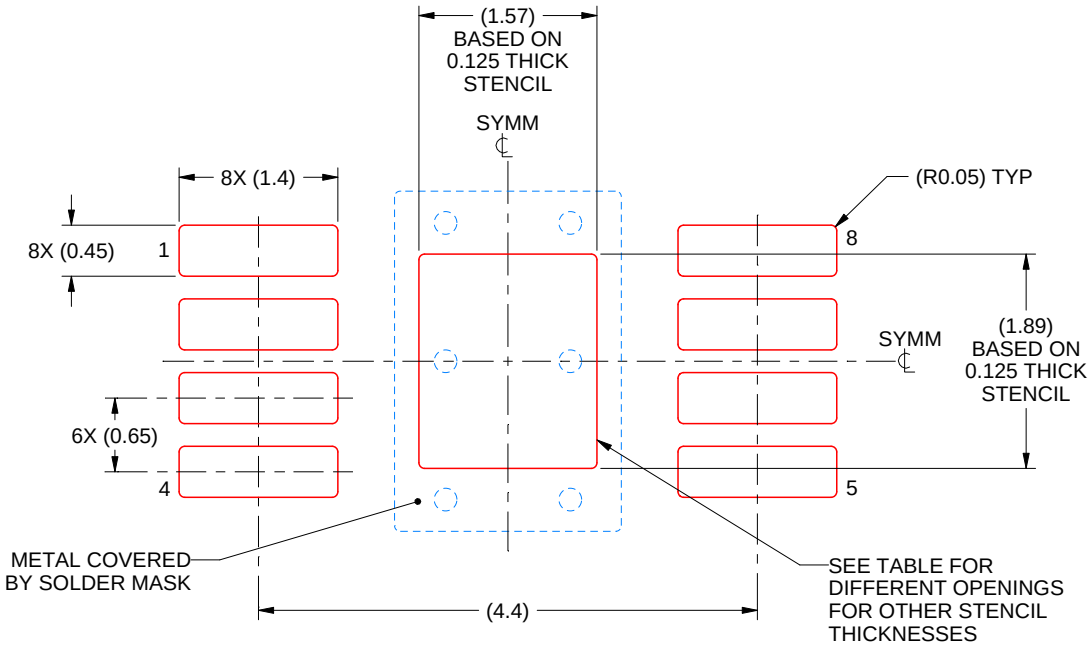


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

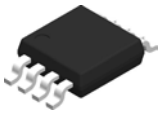
4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

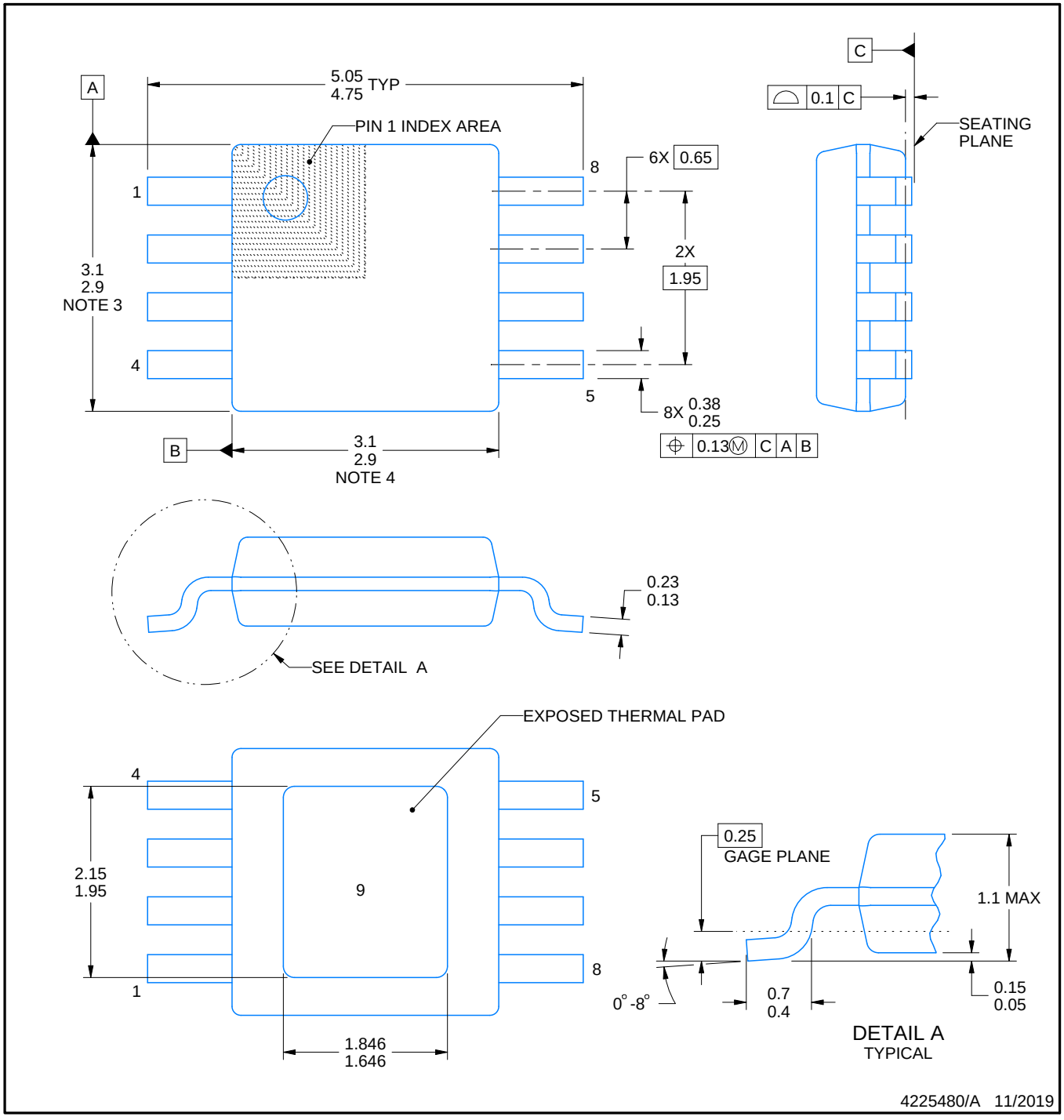
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

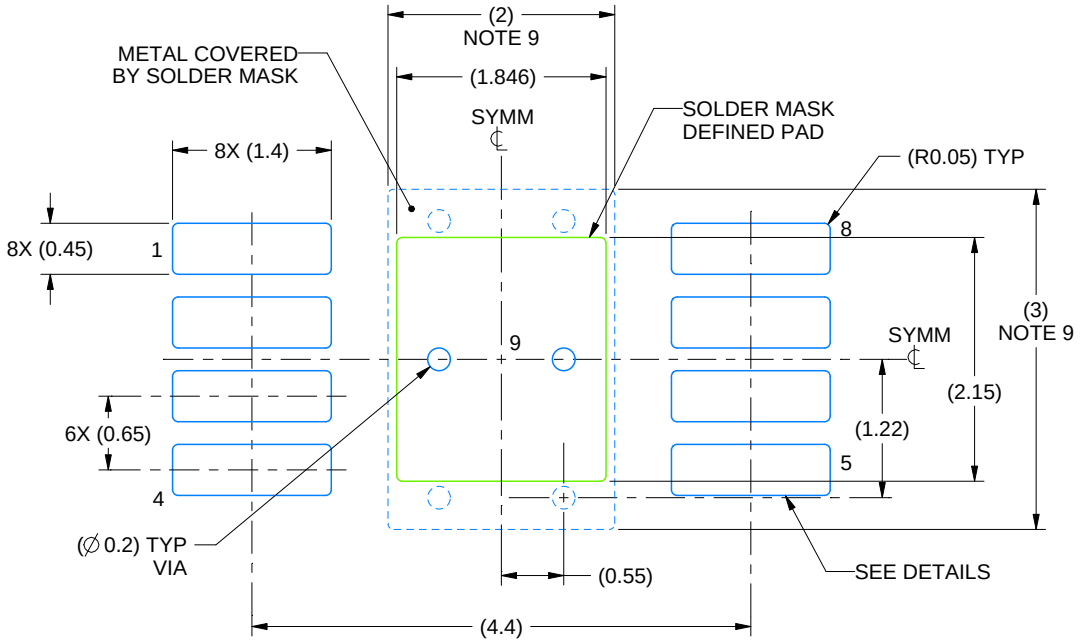
SMALL OUTLINE PACKAGE



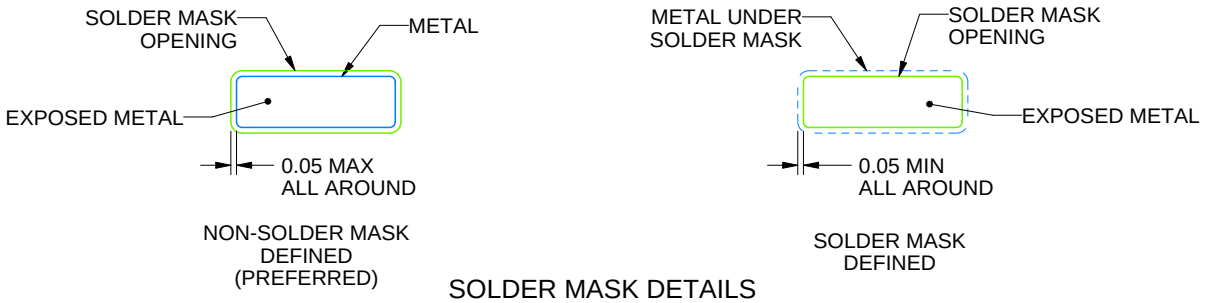
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

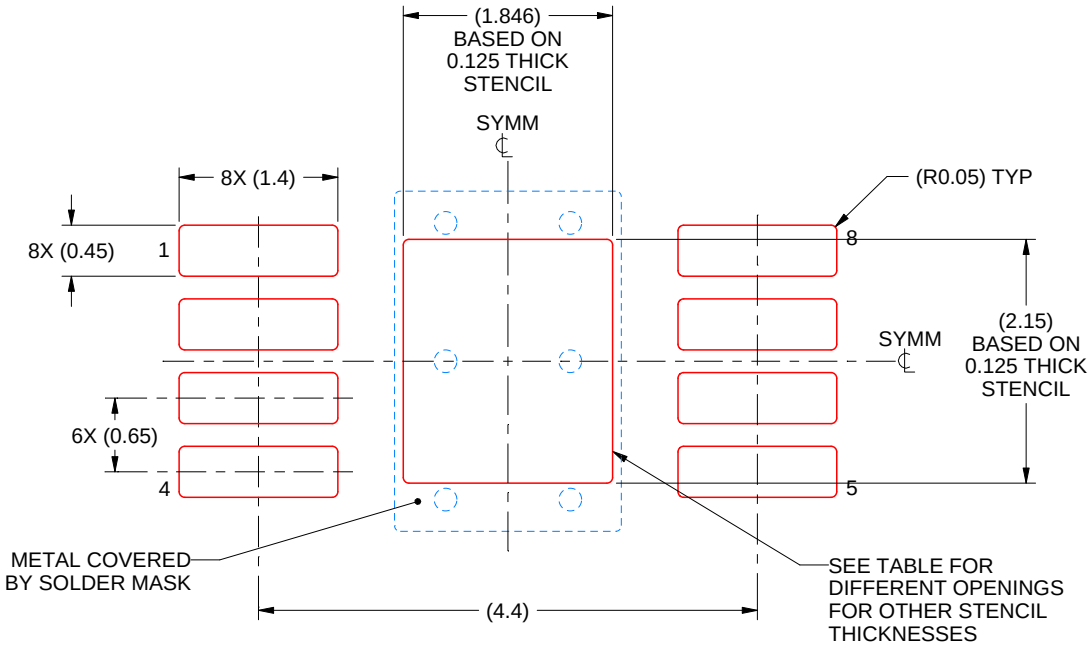


SOLDER MASK DETAILS

4225480/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



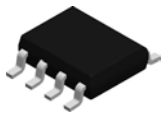
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.06 X 2.40
0.125	1.846 X 2.15 (SHOWN)
0.15	1.69 X 1.96
0.175	1.56 X 1.82

4225480/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

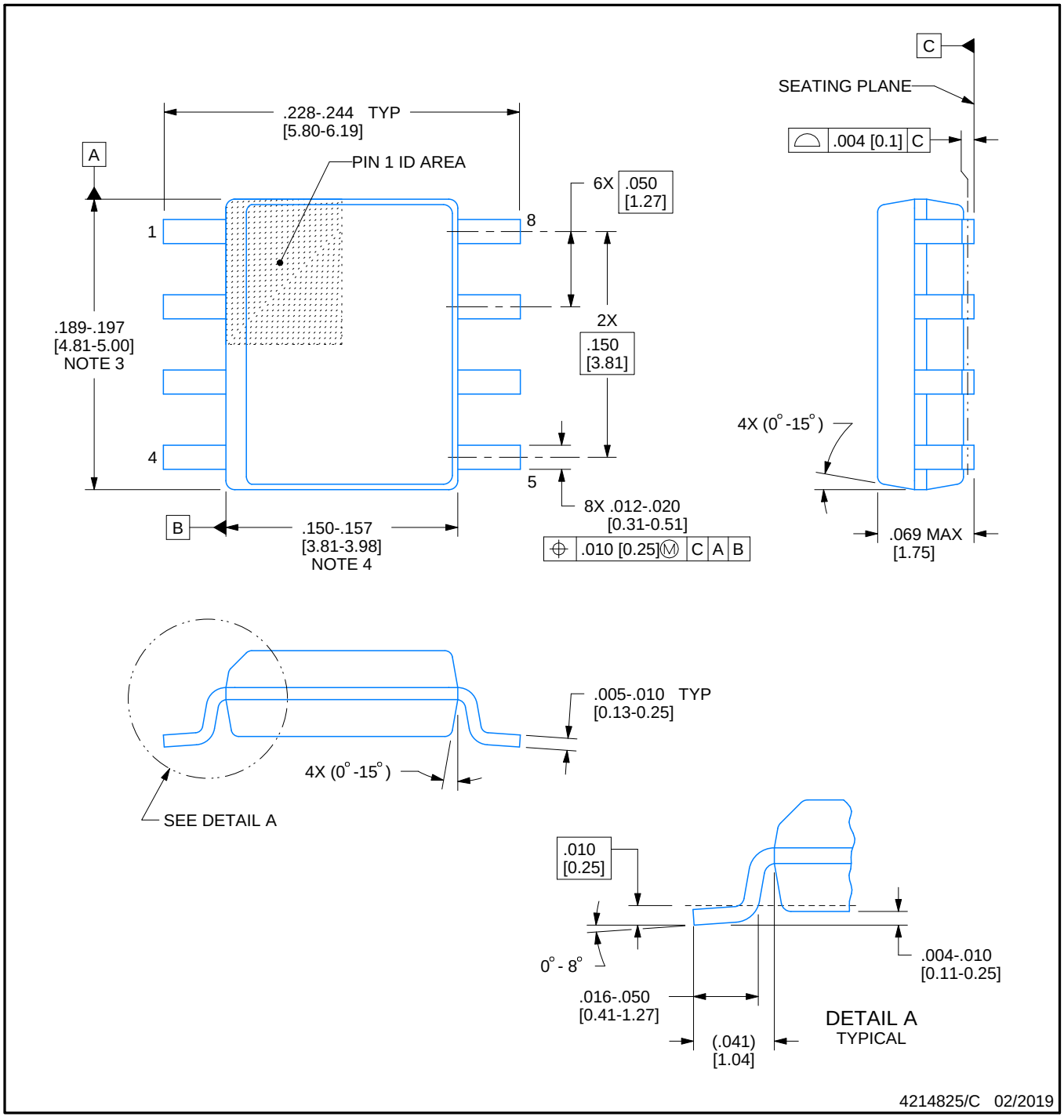


PACKAGE OUTLINE

D0008A

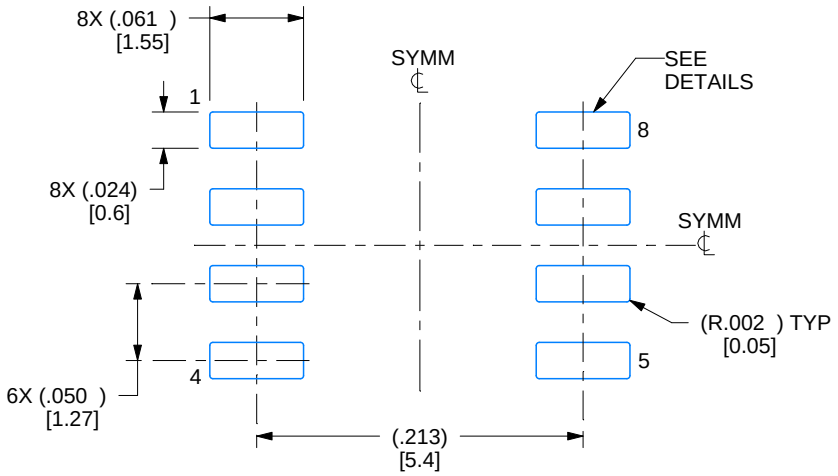
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

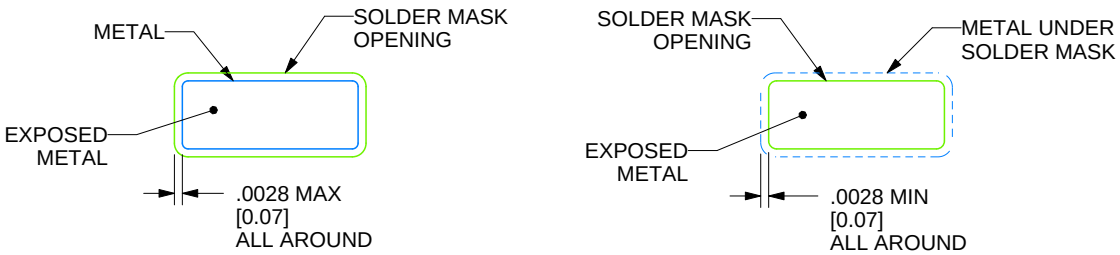


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

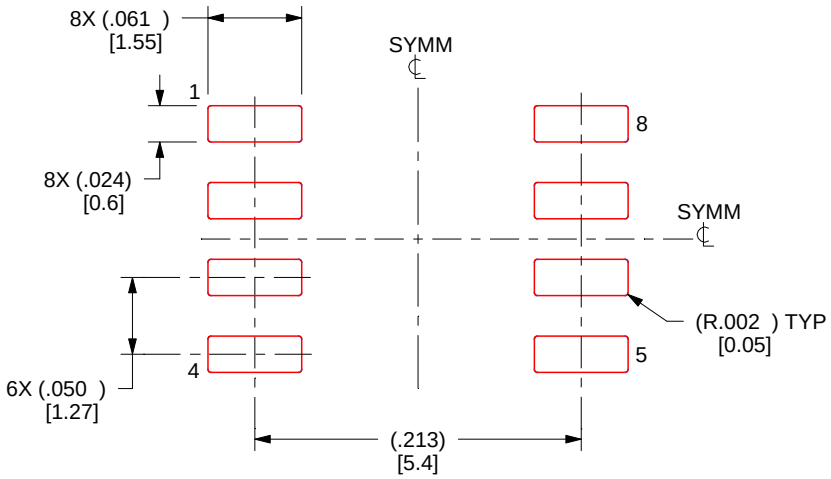
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



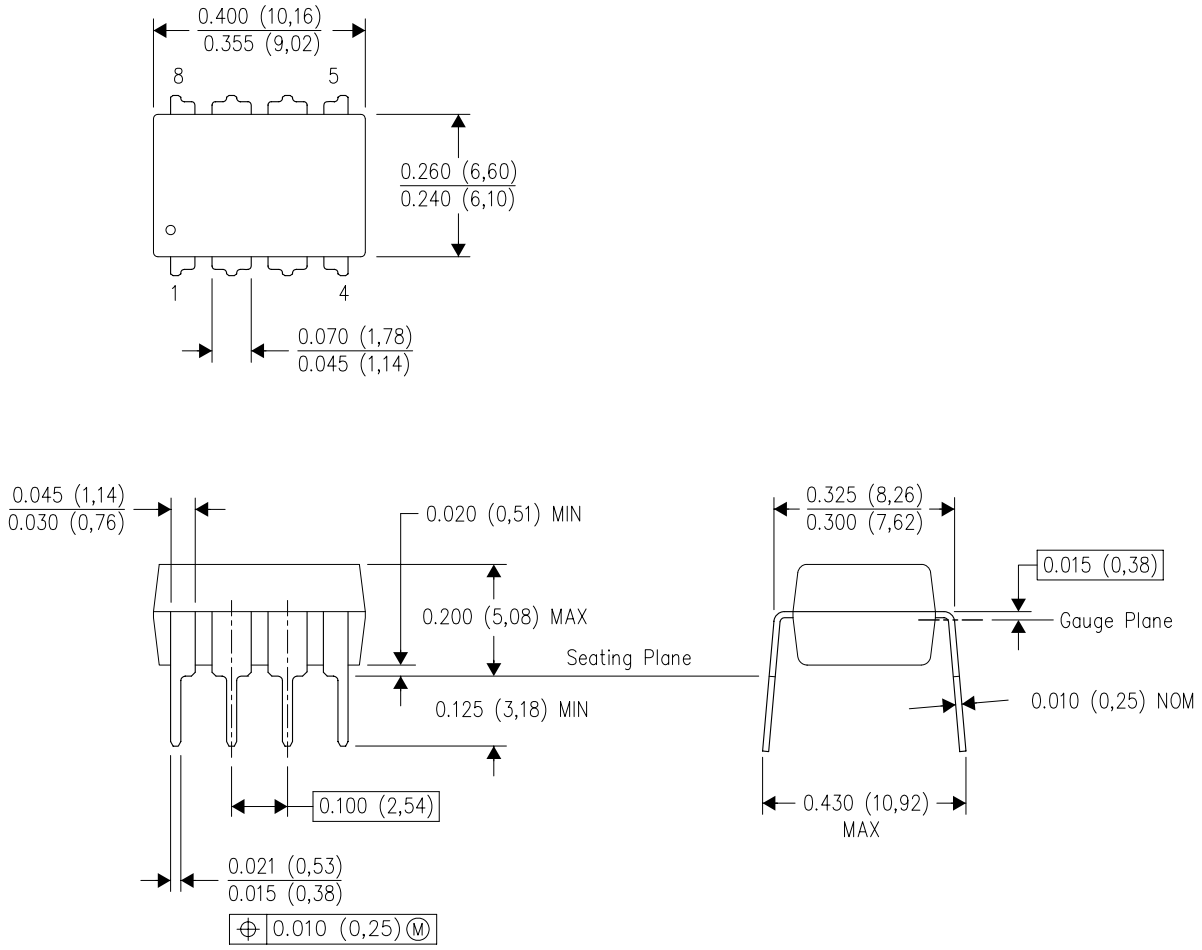
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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