DAC9881 18 位单通道低噪声电压输出数模转换器

1 特性

- 在整个温度范围具有 18 位单调性
- 相对精度：最大 ±2LSB
- 低噪声：24nV/√Hz
- 快速稳定：5µs
- 支持轨至轨运行的片上输出缓冲放大器
- 单电源：2.7V 至 5.5V
- DAC 负载控制
- 可选择的上电复位至零电平或中间电平
- 断电模式
- 单极直接二进制或二进制补码输入模式
- 具有施密特触发输入的快速 SPI：高达 50MHz、1.8V/3V/5V 逻辑电平
- 额定温度范围：-40°C 至 +105°C
- 小型封装：VQFN-24，4mm × 4mm

2 应用

- 半导体测试
- 示波器 (DSO)
- X 射线系统
- 实验室和现场仪表
- 数据采集 (DAQ)

3 说明

DAC9881 是一款 18 位单通道电压输出数模转换器 (DAC)。此器件 具有 18 位单调性、卓越的线性、非常低的噪声和快速稳定时间。片上精度输出放大器可在 2.7V 至 5.5V 的完整电源电压范围内实现轨至轨输出摆幅。

此器件支持标准串行外设接口 (SPI)，这种接口可在高达 50MHz 的输入数据时钟频率下工作。DAC9881 需要外部基准电压来设置 DAC 通道的输出范围。此器件还采用了可编程上电复位电路，确保 DAC 输出可以零电平或中间电平加电并保持，直到写入一个有效代码。

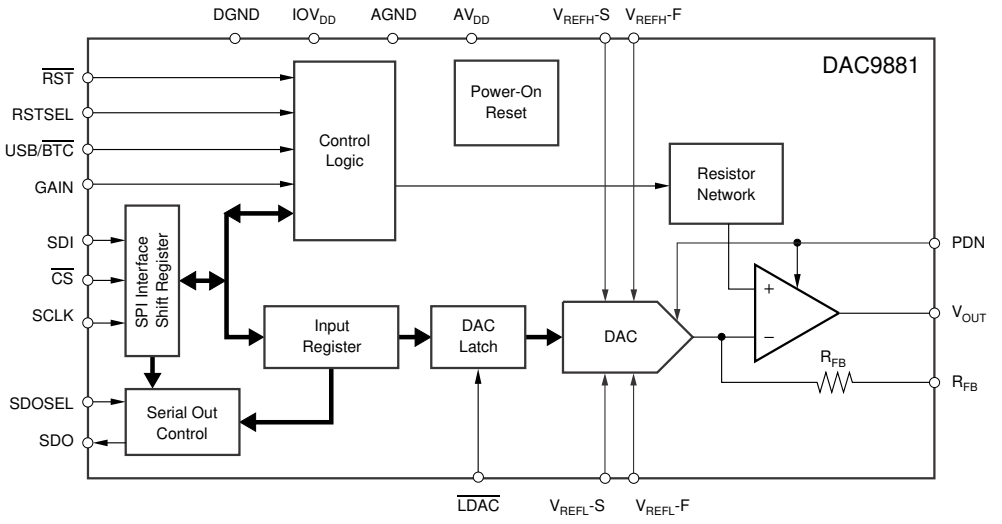
此外，DAC9881 还能够在单极直接二进制或二进制补码模式下运行。DAC9881 可实现低功耗运行。为了进一步节能，可以通过访问 PDN 引脚进入断电模式，从而在 5V 时将电流消耗减少到 25µA。5V 时的功耗为 4mW，在断电模式下降至 125µW。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DAC9881	VQFN (24)	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的封装选项附录。

方框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (March 2016) to Revision C	Page
• Added new text to end of *Hardware Reset* section regarding two's complement mode	30
• Changed Table 3, Reset Values, to show updated content	30

Changes from Revision A (August 2008) to Revision B	Page
• 已添加 *ESD 额定值表*，*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分	1

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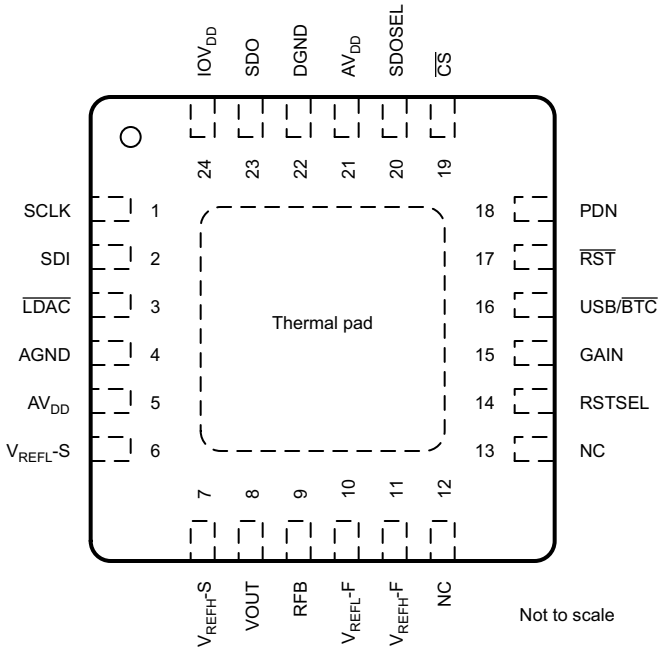
5 Pin Configuration and Functions

RGE Package
24-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SCLK	I	SPI bus serial clock input
2	SDI	I	SPI bus serial data input
3	$\overline{\text{LDAC}}$	I	Load DAC latch control input (active low). When $\overline{\text{LDAC}}$ is low, the DAC latch is transparent, and the contents of the input register are transferred to the DAC latch. The DAC output changes to the corresponding level simultaneously when the DAC latch is updated. It is recommended to connect this pin to IOV_{DD} through a pullup resistor.
4	AGND	I	Analog ground
5	AV_{DD}	I	Analog power supply
6	V_{REFL}-S	I	Reference low input sense
7	V_{REFH}-S	I	Reference high input sense
8	V_{OUT}	O	Output of output buffer
9	R_{FB}	I	Feedback resistor connected to the inverting input of the output buffer
10	V_{REFL}-F	I	Reference low input force
11	V_{REFH}-F	I	Reference high input force
12	NC	—	Do not connect
13	NC	—	Do not connect
14	RSTSEL	I	Selects the value of the output from the V_{OUT} pin after power-on or hardware reset. If RSTSEL = IOV_{DD}, then register data = 20000h. If RSTSEL = DGND, then register data = 00000h.
15	GAIN	I	Buffer gain setting. Gain = 1 when the pin is connected to DGND; Gain = 2 when the pin is connected to IOV_{DD}.
16	USB/$\overline{\text{BTC}}$	I	Input data format selection. Input data are straight binary format when the pin is connected to IOV_{DD}, and in two's complement format when the pin is connected to DGND.
17	$\overline{\text{RST}}$	I	Reset input (active low). Logic low on this pin causes the device to perform a reset.
18	PDN	I	Power-down input (active high). Logic high on this pin forces the device into power-down status. In power-down, the V_{OUT} pin connects to AGND through a 10-kΩ resistor.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
19	$\overline{CS}$	I	SPI bus chip select input (active low). Data bits are not clocked into the serial shift register unless $\overline{CS}$ is low. When $\overline{CS}$ is high, SDO is in a high-impedance state. It is recommended to connect this pin to IOV_{DD} through a pullup resistor.
20	SDOSEL	I	SPI serial data output selection. When SDOSEL is tied to IOV_{DD}, the contents of the existing input register are shifted out from the SDO pin; this is Stand-Alone mode. When SDOSEL is tied to DGND, the contents in the SPI input shift register are shifted out from the SDO pin; this is Daisy-Chain mode for daisy-chained communication.
21	AV_{DD}	I	Analog power supply. Must be connected to pin 5.
22	DGND	I	Digital ground
23	SDO	O	SPI bus serial data output. Refer to the timing diagrams for further detail.
24	IOV_{DD}	I	Interface power. Connect to 1.8 V for 1.8-V logic, 3 V for 3-V logic, and to 5 V for 5-V logic.
Thermal pad		—	The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).[1]

		MIN	MAX	UNIT
	AV_{DD} to AGND	–0.3	6	V
	IOV_{DD} to DGND	–0.3	6	V
	Digital input voltage to DGND	–0.3	IOV_{DD} + 0.3	V
	V_{OUT} to AGND	–0.3	AV_{DD} + 0.3	V
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
AV_{DD}	Analog power supply		2.7		5.5	V
IOV_{DD}	Interface power supply		1.7		AV_{DD}	V
V_{REFH}	Reference high input voltage	AV_{DD} = 5.5 V	1.25	5	AV_{DD}	V
		AV_{DD} = 3 V	1.25	2.5	AV_{DD}	V
V_{REFL}	Reference low input voltage		–0.2	0	0.2	V
T_A	Specified temperature		–40		105	°C

6.4 Thermal Information

THERMAL METRIC[1]		DAC9881 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics: AV_{DD} = 5 V

all specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = 4.75 V to 5.5 V, IOV_{DD} = 1.8 V to 5.5 V, V_{REFH} = 5 V, V_{REFL} = 0 V, and gain = 1X mode (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ACCURACY(1)						
Integral linearity error	Measured by line passing through codes 2048 and 260096	DAC9881S		±2	±3	LSB
		DAC9881SB		±1	±2	LSB
Differential linearity error	Measured by line passing through codes 2048 and 260096	DAC9881S	–1	±0.75	+2	LSB
		DAC9881SB		±0.5	±1	LSB
Monotonicity			18			Bits
Zero-scale error	T_A = 25°C, code = 2048				±16	LSB
	T_{MIN} to T_{MAX}, code = 2048				±32	LSB
Zero-scale drift(2)	Code = 2048			±0.25	±0.8	ppm/°C of FSR
Gain error	T_A = 25°C, measured by line passing through codes 2048 and 260096			±16	±32	LSB
Gain temperature drift(2)	Measured by line passing through codes 2048 and 260096			±0.25	±0.4	ppm/°C
PSRR(2)	V_{OUT} = full-scale, AV_{DD} = 5 V ±10%				32	LSB/V
ANALOG OUTPUT(2)						
Voltage output(3)			0		AV_{DD}	V
Output voltage drift vs time	Device operating for 500 hours at 25°C			0.1		ppm of FSR
	Device operating for 1000 hours at 25°C			0.2		ppm of FSR
Output current(4)				2.5		mA
Maximum load capacitance				200		pF
Short-circuit current				31/–50		mA
REFERENCE INPUT(2)						
V_{REFH} input voltage range	AV_{DD} = 5.5 V		1.25	5	AV_{DD}	V
V_{REFH} input capacitance				5		pF
V_{REFH} input impedance				4.5		kΩ
V_{REFL} input voltage range			–0.2	0	0.2	V
V_{REFL} input capacitance				4.5		pF
V_{REFL} input impedance				5		kΩ
DYNAMIC PERFORMANCE(2)						
Settling time	To ±0.003% FS, R_L = 10 kΩ, C_L = 50 pF, code 04000h to 3C000h			5		µs
Slew rate	From 10% to 90% of 0 V to 5 V			2.5		V/µs
Code change glitch	Code = 1FFFFh to 20000h to 1FFFFh	V_{REFH} = 5 V, gain = 1X mode		37		nV-s
		V_{REFH} = 2.5 V, gain = 1X mode		18		nV-s
		V_{REFH} = 1.25 V, gain = 1X mode		9		nV-s
		V_{REFH} = 2.5 V, gain = 2X mode		21		nV-s
		V_{REFH} = 1.25 V, gain = 2X mode		10		nV-s
Digital feedthrough	$\overline{CS}$ = high, f_{SCLK} = 1 kHz			1		nV-s
Output noise voltage density	f = 1 kHz to 100 kHz, full-scale output	Gain = 1		24	30	nV/√Hz
		Gain = 2		40	48	nV/√Hz
Output noise voltage	f = 0.1 Hz to 10 Hz, full-scale output			2		$µV_{PP}$

(1) DAC output range is 0 V to 5 V. 1 LSB = 19 µV.
(2) Specified by design; not production tested.
(3) The output from the V_{OUT} pin = [(V_{REFH} – V_{REFL}) / 262144] × CODE × Buffer GAIN + V_{REFL}. The maximum range of V_{OUT} is 0 V to AV_{DD}. The full-scale of the output must be less than AV_{DD}; otherwise, output saturation occurs.
(4) See Figure 26, Figure 27, and Figure 28 for details.

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Electrical Characteristics: AV_{DD} = 5 V (continued)

all specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = 4.75 V to 5.5 V, IOV_{DD} = 1.8 V to 5.5 V, V_{REFH} = 5 V, V_{REFL} = 0 V, and gain = 1X mode (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS(2)					
High-level input voltage, V_{IH}	IOV_{DD} = 4.5 V to 5.5 V	3.8		IOV_{DD} + 0.3	V
	IOV_{DD} = 2.7 V to 3.3 V	2.1		IOV_{DD} + 0.3	V
	IOV_{DD} = 1.7 V to 2 V	1.5		IOV_{DD} + 0.3	V
Low-level input voltage, V_{IL}	IOV_{DD} = 4.5 V to 5.5 V	–0.3		0.8	V
	IOV_{DD} = 2.7 V to 3.3 V	–0.3		0.6	V
	IOV_{DD} = 1.7 V to 2 V	–0.3		0.3	V
Digital input current (I_{IN})			±1	±10	µA
Digital input capacitance			5		pF
DIGITAL OUTPUT(2)					
High-level output voltage, V_{OH}	IOV_{DD} = 2.7 V to 5.5 V, I_{OH} = –1 mA	IOV_{DD} – 0.2			V
	IOV_{DD} = 1.7 V to 2 V, I_{OH} = –500 µA	IOV_{DD} – 0.2			V
Low-level output voltage, V_{OL}	IOV_{DD} = 2.7V to 5.5 V, I_{OL} = 1 mA			0.2	V
	IOV_{DD} = 1.7 V to 2 V, I_{OL} = 500 µA			0.2	V
POWER SUPPLY					
AV_{DD}		4.75	5	5.5	V
IOV_{DD}		1.7		AV_{DD}	V
AI_{DD}	V_{IH} = IOV_{DD}, V_{IL} = DGND		0.85	1.5	mA
IOI_{DD}	V_{IH} = IOV_{DD}, V_{IL} = DGND		1	10	µA
AI_{DD} power-down	PDN pin = IOV_{DD}		25	50	µA
Power dissipation	AV_{DD} = 5 V		4.3	7.5	mW

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6.6 Electrical Characteristics: AV_{DD} = 2.7 V

all specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = 2.7 V to 3.3 V, IOV_{DD} = 1.8 V to AV_{DD}, V_{REFH} = 2.5 V, V_{REFL} = 0 V and gain = 1X mode (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ACCURACY(1)						
Integral linearity error	Measured by line passing through codes 2048 and 262143	DAC9881S		±2.5	±3.5	LSB
		DAC9881SB		±2	±3	LSB
Differential linearity error	Measured by line passing through codes 2048 and 262143	DAC9881S		±1	±2	LSB
		DAC9881SB		±0.75	±1.5	LSB
Zero-scale error	T_A = 25°C, code = 2048				±32	LSB
	T_{MIN} to T_{MAX}, code = 2048				±64	LSB
Zero-scale drift(2)	Code = 2048			±0.5	±1.6	ppm/°C of FSR
Gain error	T_A = 25°C, measured by line passing through codes 2048 and 262143			±32	±64	LSB
Gain temperature drift(2)	Measured by line passing through codes 2048 and 262143			±0.5	±0.8	ppm/°C
PSRR(2)	V_{OUT} = full-scale, AV_{DD} = 3 V ±10%				64	LSB/V
ANALOG OUTPUT(2)						
Voltage output(3)			0		AV_{DD}	V
Output voltage drift vs time	Device operating for 500 hours at 25°C			0.2		ppm of FSR
	Device operating for 1000 hours at 25°C			0.4		ppm of FSR
Output current(4)				2.5		mA
Maximum load capacitance				200		pF
Short-circuit current				31/–50		mA
REFERENCE INPUT(2)						
V_{REFH} input voltage range	AV_{DD} = 3 V		1.25	2.5	AV_{DD}	V
V_{REFH} input capacitance				5		pF
V_{REFH} input impedance				4.5		kΩ
V_{REFL} input voltage range			–0.2	0	0.2	V
V_{REFL} input capacitance				4.5		pF
V_{REFL} input impedance				5		kΩ
DYNAMIC PERFORMANCE(2)						
Settling time	To ±0.003% FS, R_L = 10 kΩ, C_L = 50 pF, code 04000h to 3C000h			5		µs
Slew rate	From 10% to 90% of 0 V to 2.5 V			2.5		V/µs
Code change glitch	Code = 1FFFFh to 20000h to 1FFFFh	V_{REFH} = 2.5 V, gain = 1X mode		18		nV-s
		V_{REFH} = 1.25 V, gain = 1X mode		9		nV-s
		V_{REFH} = 1.25 V, gain = 2X mode		10		nV-s
Digital feedthrough	$\overline{CS}$ = high, f_{SCLK} = 1 kHz			1		nV-s
Output noise voltage density	f = 1 kHz to 100 kHz, full-scale output	Gain = 1		24	30	nV/√Hz
		Gain = 2		40	48	nV/√Hz
Output noise voltage	f = 0.1 Hz to 10 Hz, full-scale output			2		$µV_{PP}$

(1) DAC output range is 0 V to 2.5 V. 1 LSB = 9.5 µV.
(2) Specified by design; not production tested.
(3) The output from the V_{OUT} pin = [(V_{REFH} – V_{REFL}) / 262144] × CODE × Buffer GAIN + V_{REFL}. The maximum range of V_{OUT} is 0 V to AV_{DD}. The full-scale of the output must be less than AV_{DD}; otherwise, output saturation occurs.
(4) See Figure 55, Figure 56, and Figure 57 for details.

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Electrical Characteristics: AV_{DD} = 2.7 V (continued)

all specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = 2.7 V to 3.3 V, IOV_{DD} = 1.8 V to AV_{DD}, V_{REFH} = 2.5 V, V_{REFL} = 0 V and gain = 1X mode (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS[(2)]					
High-level input voltage, V_{IH}	IOV_{DD} = 2.7 V to 3.3 V	2.1		IOV_{DD} + 0.3	V
	IOV_{DD} = 1.7 V to 2 V	1.5		IOV_{DD} + 0.3	V
Low-level input voltage, V_{IL}	IOV_{DD} = 2.7 V to 3.3 V	–0.3		0.6	V
	IOV_{DD} = 1.7 V to 2 V	–0.3		0.3	V
Digital input current (I_{IN})			±1	±10	µA
Digital input capacitance			5		pF
DIGITAL OUTPUT[(2)]					
High-level output voltage, V_{OH}	IOV_{DD} = 2.7 V to 3.3 V, I_{OH} = –1 mA	IOV_{DD} – 0.2			V
	IOV_{DD} = 1.7 V to 2 V, I_{OH} = –500 µA	IOV_{DD} – 0.2			V
Low-level output voltage, V_{OL}	IOV_{DD} = 2.7 V to 3.3 V, I_{OL} = 1 mA			0.2	V
	IOV_{DD} = 1.7 to 2 V, I_{OL} = 500 µA			0.2	V
POWER SUPPLY					
AV_{DD}		2.7	3	3.3	V
IOV_{DD}		1.7		AV_{DD}	V
AI_{DD}	$V_{IH} = IOV_{DD}$, V_{IL} = DGND		0.75	1.2	mA
IOI_{DD}	$V_{IH} = IOV_{DD}$, V_{IL} = DGND		1	10	µA
AI_{DD} power-down	PDN pin = IOV_{DD}		25	50	µA
Power dissipation	AV_{DD} = 3 V		2.3	3.6	mW

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6.7 Timing Requirements—Standalone Operation Without SDO

at –40°C to +105°C (unless otherwise noted); see Figure 1 (1)(2)(3)

			MIN	MAX	UNIT
f_{SCLK}	Maximum clock frequency	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$		40	MHz
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$		50	MHz
t_1	Minumum $\overline{CS}$ high time	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	50		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	30		ns
t_2	Delay from $\overline{CS}$ falling edge to SCLK rising edge	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	10		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	8		ns
t_3	Delay from SCLK falling edge to $\overline{CS}$ falling edge	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	0		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	0		ns
t_4	SCLK low time	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	10		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	10		ns
t_5	SCLK high time	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	15		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	10		ns
t_6	SCLK cycle time	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	25		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	20		ns
t_7	Delay from SCLK rising edge to $\overline{CS}$ rising edge	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	10		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	10		ns
t_8	Input data setup time	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	8		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	5		ns
t_9	Input data hold time	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	5		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	5		ns
t_{14}	Delay from $\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	10		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	5		ns
t_{15}	$\overline{LDAC}$ pulse duration	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	15		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	10		ns

(1) All input signals are specified with $t_R = t_F = 2$ns (10% to 90% of IOV_{DD}) and timed from a voltage level of IOV_{DD} / 2.
(2) Specified by design; not production tested.
(3) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.

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6.8 Timing Requirements—Standalone Operation With SDO and Daisy-Chain Mode

at –40°C to +105°C (unless otherwise noted); see Figure 2 and Figure 3[(1)(2)(3)]

			MIN	MAX	UNIT
f_{SCLK}	Maximum clock frequency	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$		20	MHz
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$		25	MHz
t_1	Minumum $\overline{CS}$ high time	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	50		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	30		ns
t_2	Delay from $\overline{CS}$ falling edge to SCLK rising edge	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	10		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	8		ns
t_3	Delay from SCLK falling edge to $\overline{CS}$ falling edge	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	0		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	0		ns
t_4	SCLK low time	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	25		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	20		ns
t_5	SCLK high time	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	25		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	20		ns
t_6	SCLK cycle time	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	50		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	40		ns
t_7	Delay from SCLK rising edge to $\overline{CS}$ rising edge	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	10		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	10		ns
t_8	Input data setup time	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	5		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	5		ns
t_9	Input data hold time	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	5		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	5		ns
t_{10}	Delay from $\overline{CS}$ falling edge to SDO valid	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$		15	ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$		10	ns
t_{11}	Delay from SCLK falling edge to SDO valid	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$		20	ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$		15	ns
t_{12}	SDO data hold from SCLK rising edge	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	t_5		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	t_5		ns
t_{13}	Delay from $\overline{CS}$ rising edge to SDO high-Z	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$		8	ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$		5	ns
t_{14}	Delay from $\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	10		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	5		ns
t_{15}	$\overline{LDAC}$ pulse width	$2.7 \le AV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	15		ns
		$3.6 \le AV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le AV_{DD}$	10		ns

(1) All input signals are specified with $t_R = t_F = 2$ns (10% to 90% of IOV_{DD}) and timed from a voltage level of IOV_{DD} / 2.
(2) Specified by design; not production tested.
(3) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.

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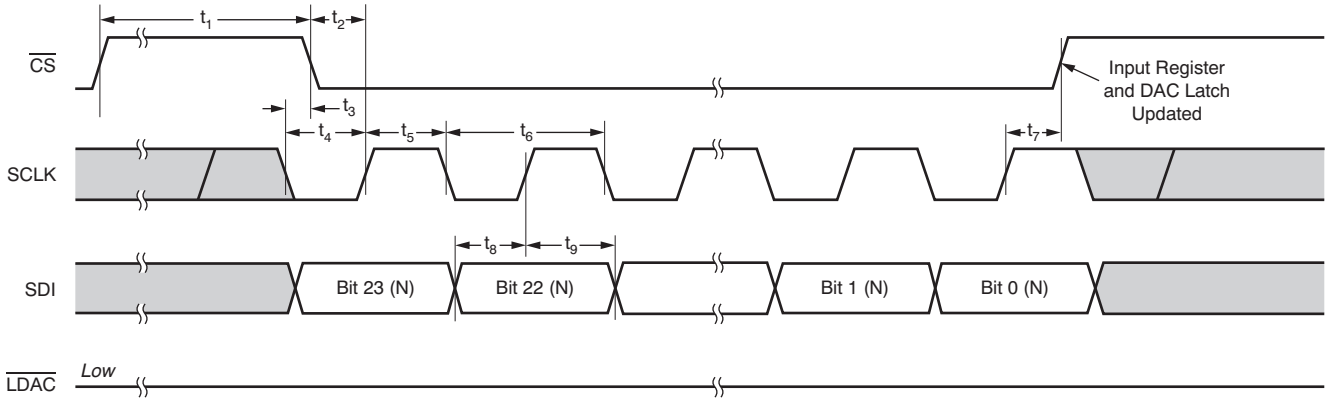
Case 1: Standalone operation without SDO, $\overline{\text{LDAC}}$ tied low.



Case 2: Standalone operation without SDO, $\overline{\text{LDAC}}$ active.

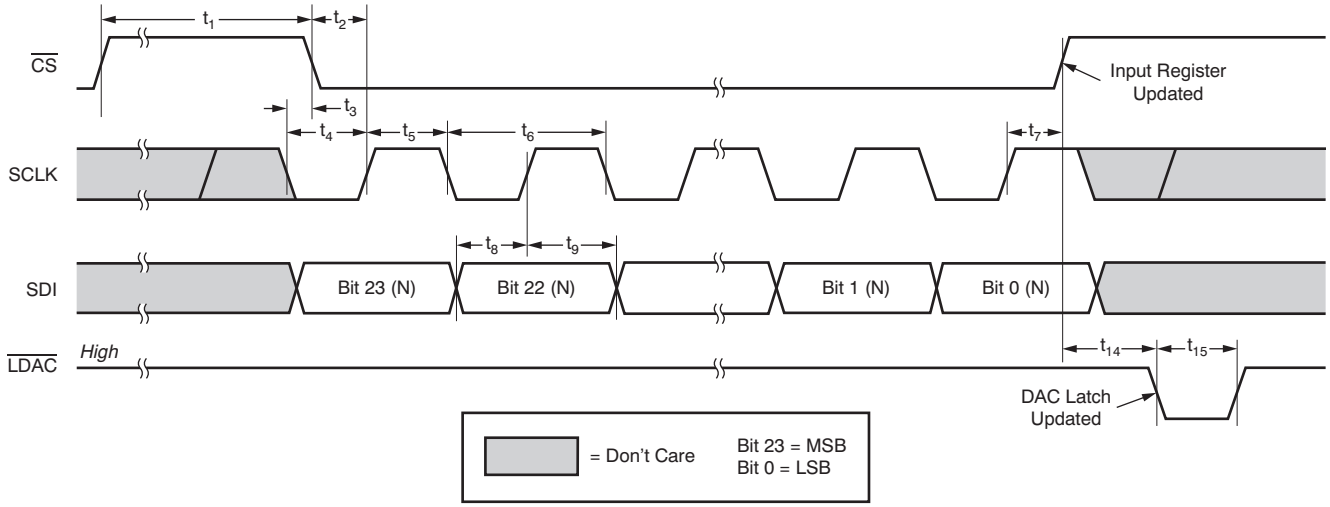


Figure 1. Timing Diagram for Standalone Operation Without SDO

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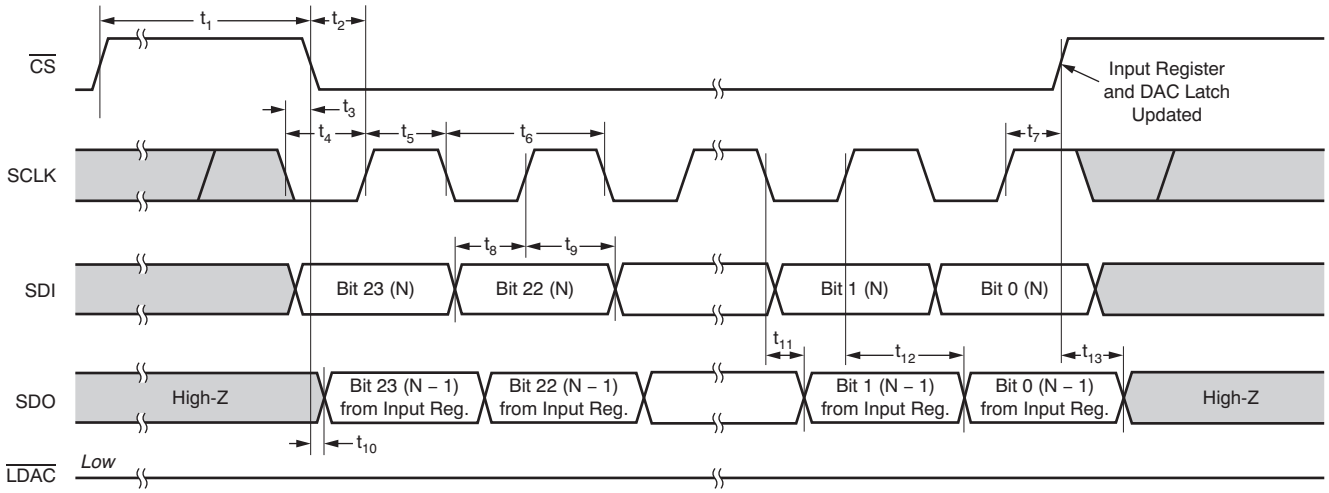
Case 1: Standalone operation with output from SDO, $\overline{\text{LDAC}}$ tied low.



Case 2: Standalone operation with output from SDO, $\overline{\text{LDAC}}$ active.

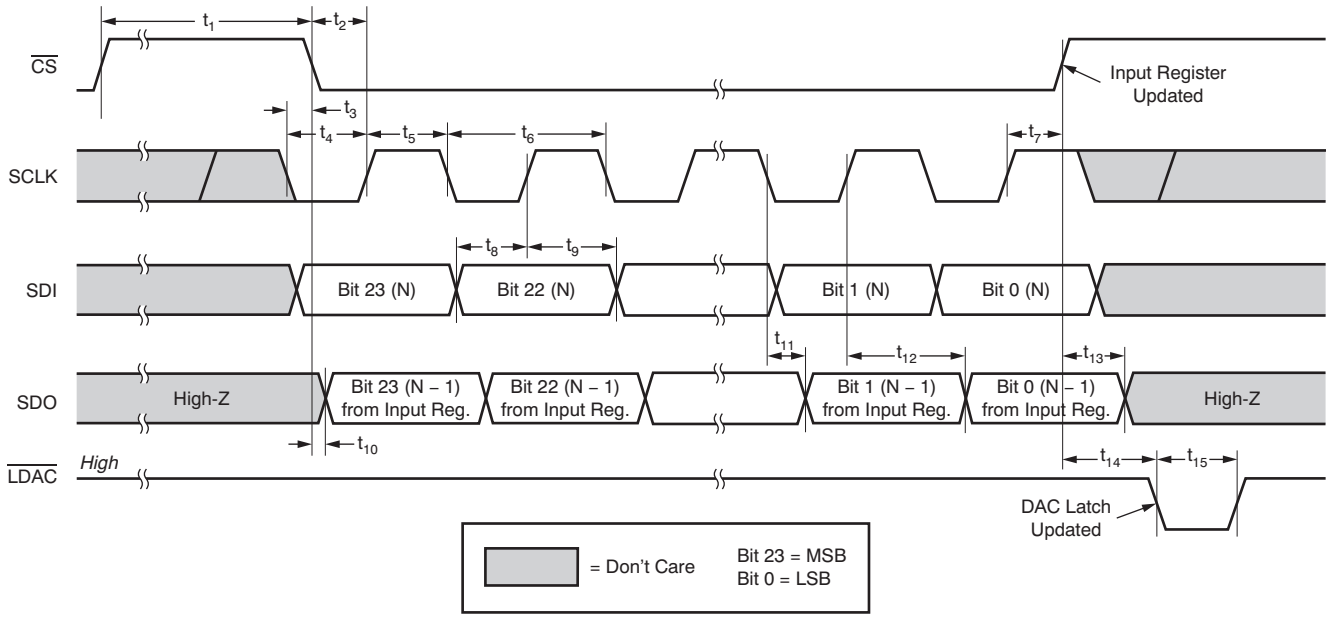
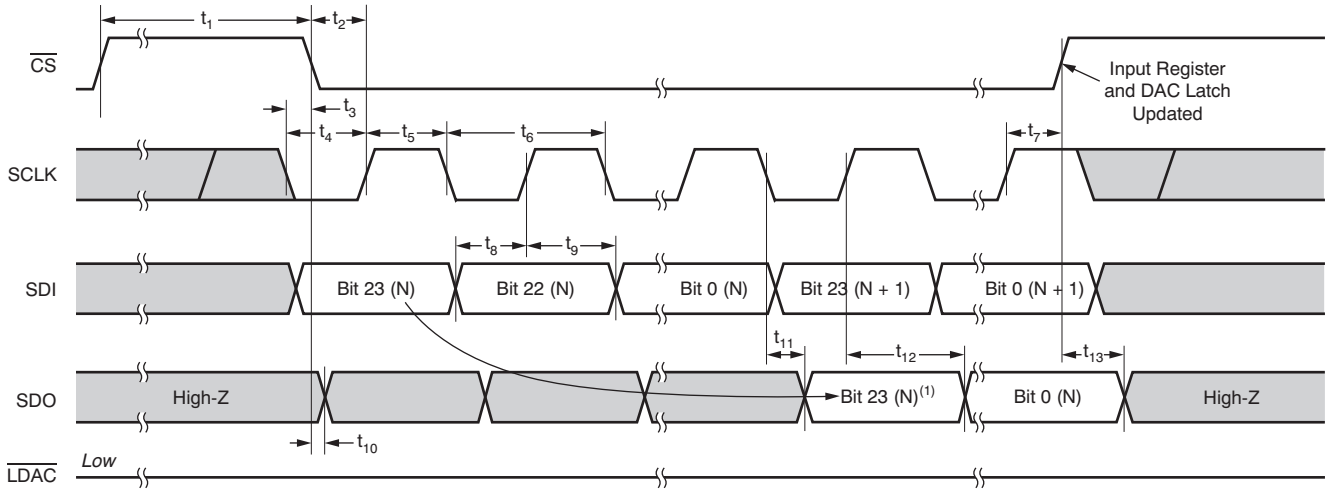
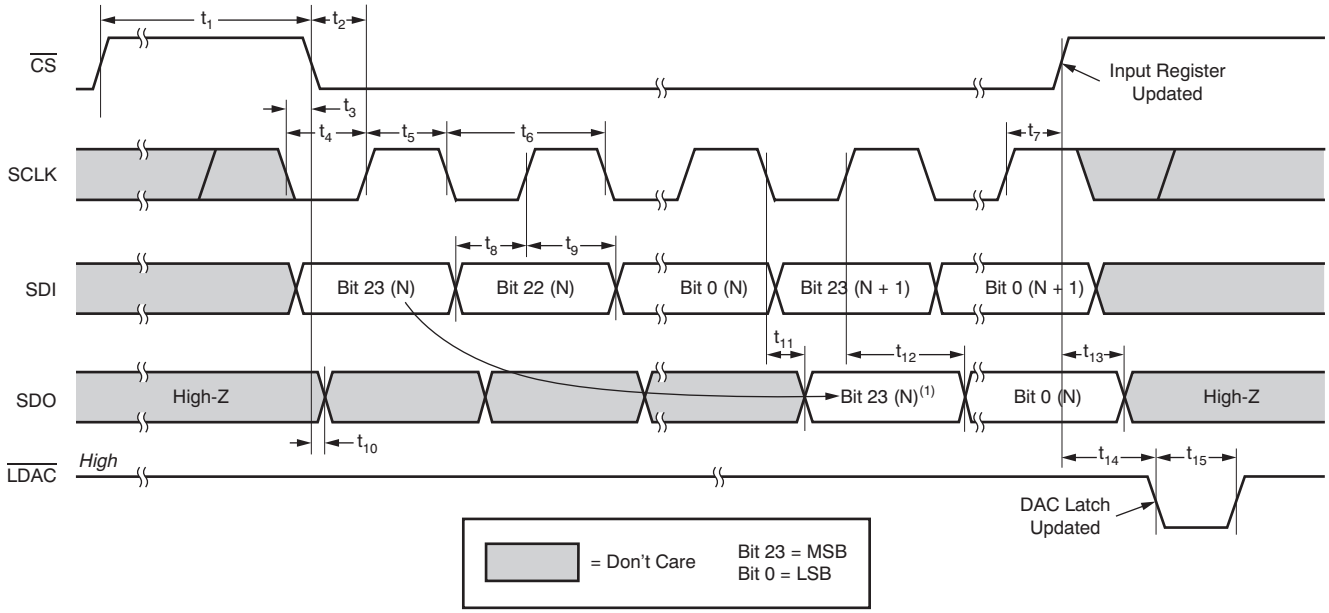


Figure 2. Timing Diagram for Standalone Operation With SDO

Case 1: Daisy Chain, $\overline{\text{LDAC}}$ tied low.



Case 2: Daisy Chain, $\overline{\text{LDAC}}$ active.



NOTE: (1) SDO data delayed from SDI by 24 clock cycles.

Figure 3. Timing Diagram for Daisy-Chain Mode, Two Cascaded Devices

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6.9 Typical Characteristics: AV_{DD} = 5 V

at T_A = 25°C, V_{REFH} = 5 V, V_{REFL} = 0 V, and gain = 1X mode (unless otherwise noted)

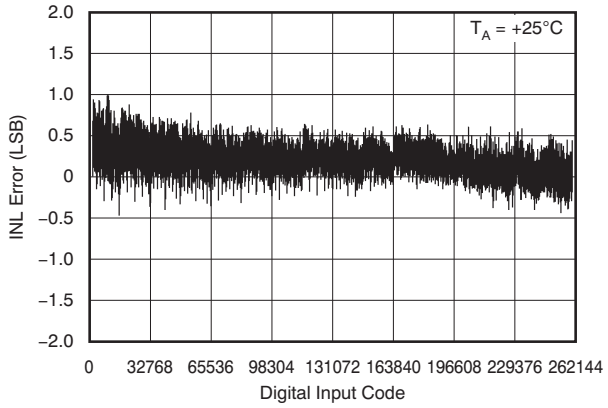


Figure 4. Linearity Error vs Digital Input Code

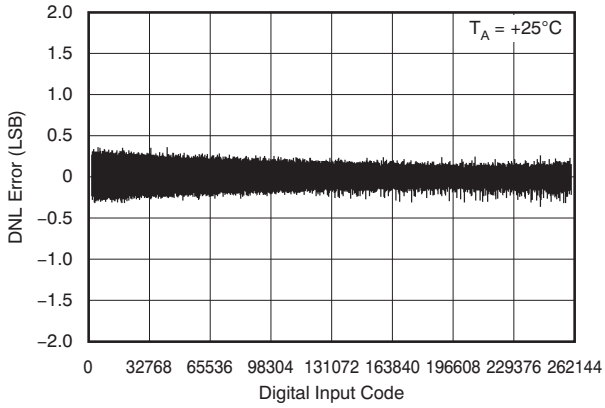


Figure 5. Differential Linearity Error vs Digital Input Code

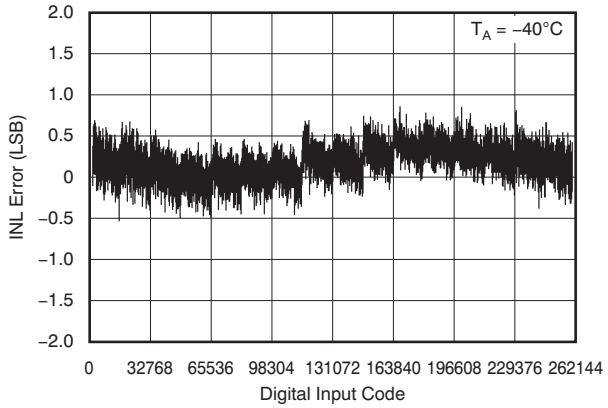


Figure 6. Linearity Error vs Digital Input Code

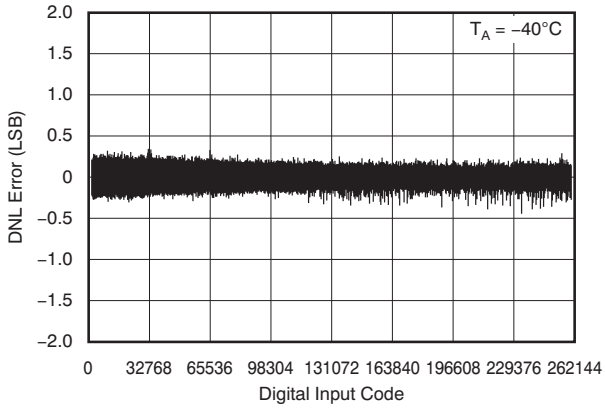


Figure 7. Differential Linearity Error vs Digital Input Code

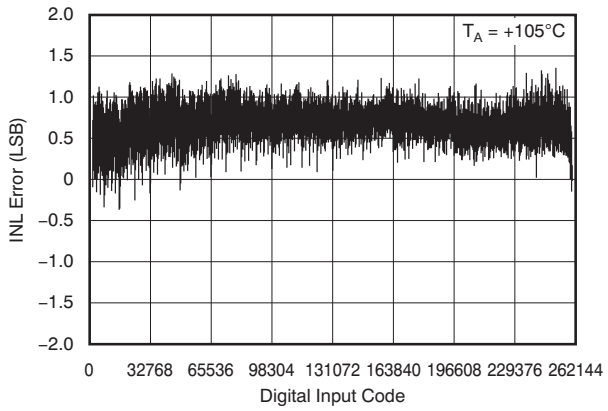


Figure 8. Linearity Error vs Digital Input Code

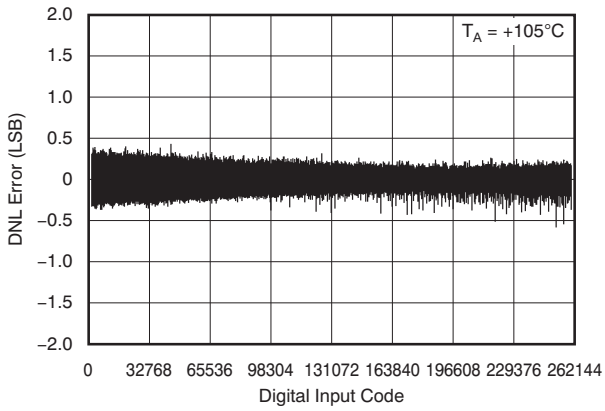


Figure 9. Differential Lineary Error vs Digital Input Code

Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, V_{REFH} = 5 V, V_{REFL} = 0 V, and gain = 1X mode (unless otherwise noted)

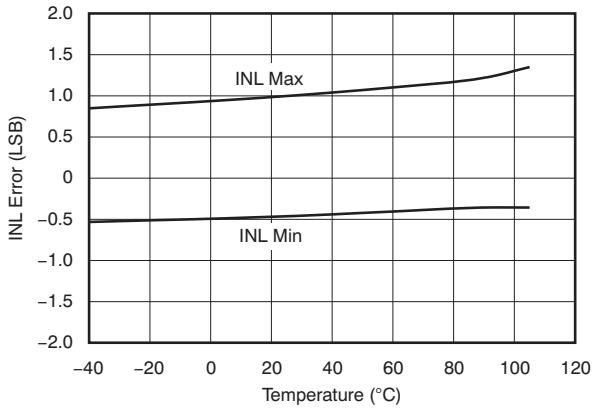


Figure 10. Linearity Error vs Temperature

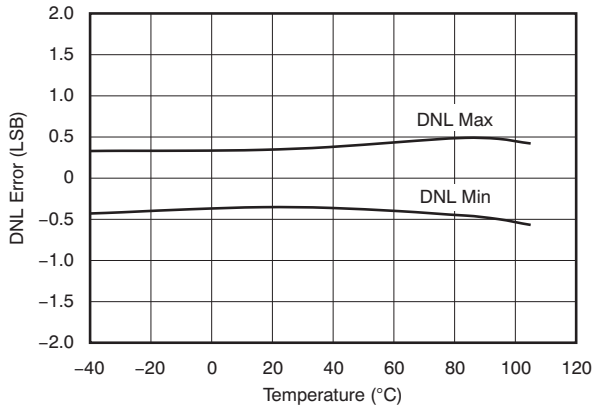
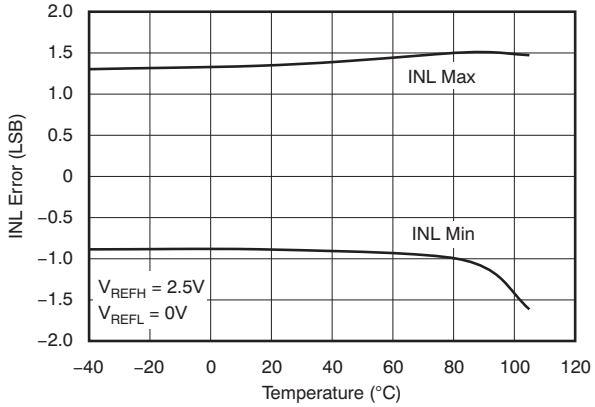
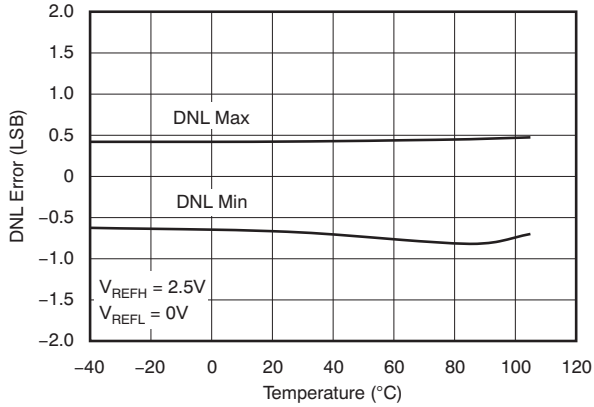


Figure 11. Differential Linearity Error vs Temperature



Gain = 2X mode

Figure 12. Linearity Error vs Temperature



Gain = 2X mode

Figure 13. Differential Linearity Error vs Temperature

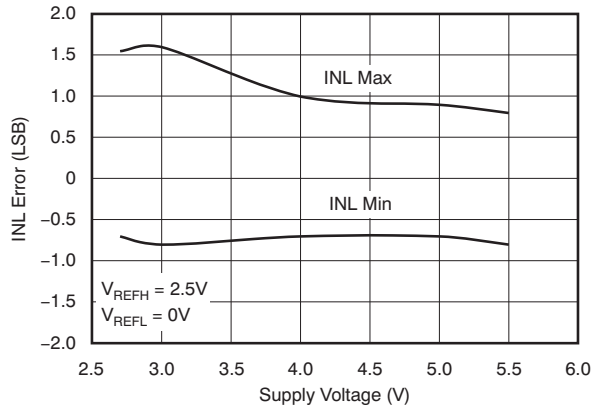


Figure 14. Linearity Error vs Supply Voltage

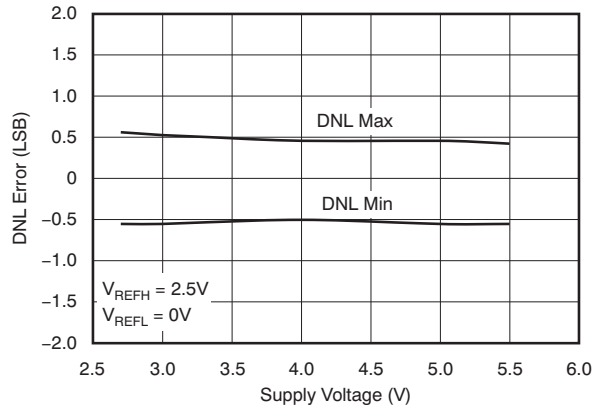


Figure 15. Differential Linearity Error vs Supply Voltage

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Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, V_{REFH} = 5 V, V_{REFL} = 0 V, and gain = 1X mode (unless otherwise noted)

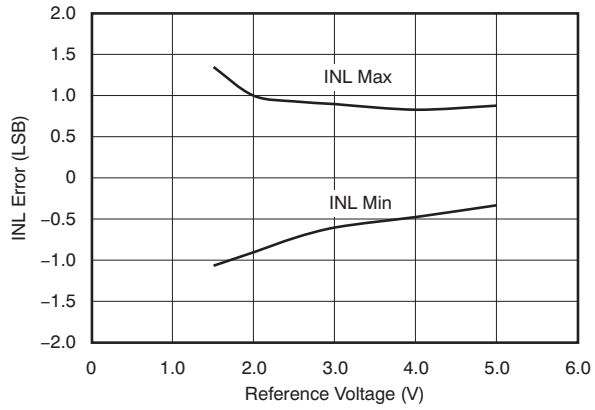


Figure 16. Linearity Error vs Reference Voltage

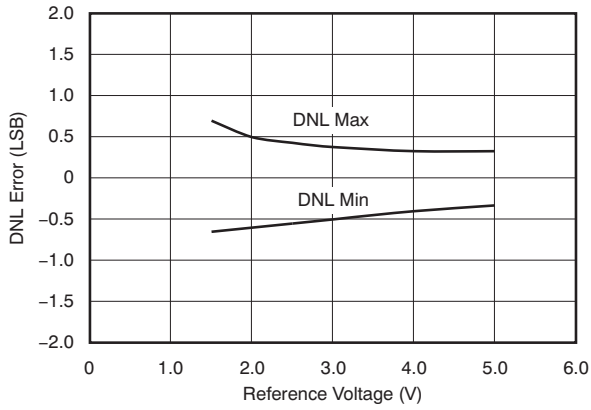


Figure 17. Differential Linearity Error vs Reference Voltage

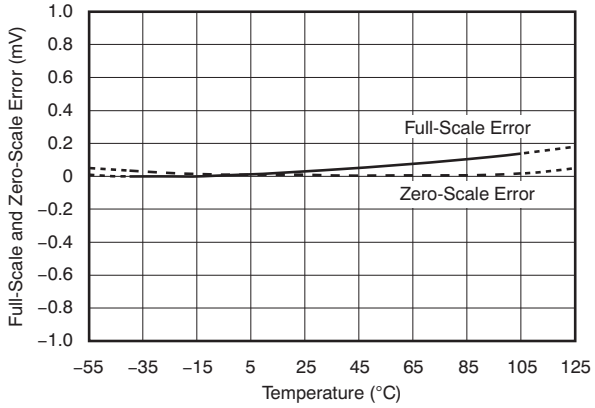
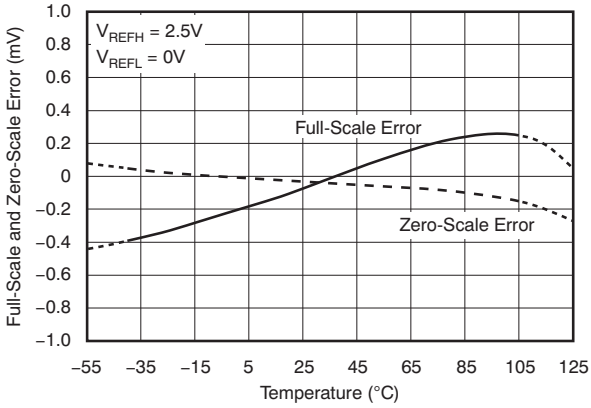


Figure 18. Full-Scale and Zero-Scale Error vs Temperature



Gain = 2X mode

Figure 19. Full-Scale and Zero-Scale Error vs Temperature

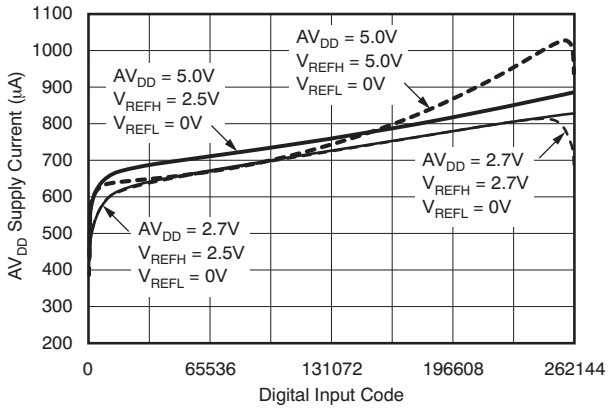
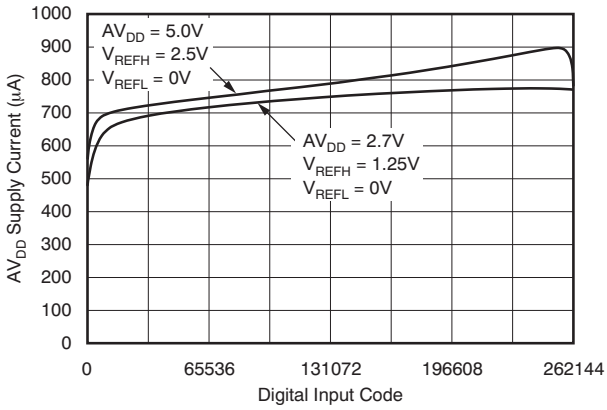


Figure 20. AVDD Supply Current vs Digital Input Code



Gain = 2X mode

Figure 21. AVDD Supply Current vs Digital Input Code

Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, V_{REFH} = 5 V, V_{REFL} = 0 V, and gain = 1X mode (unless otherwise noted)

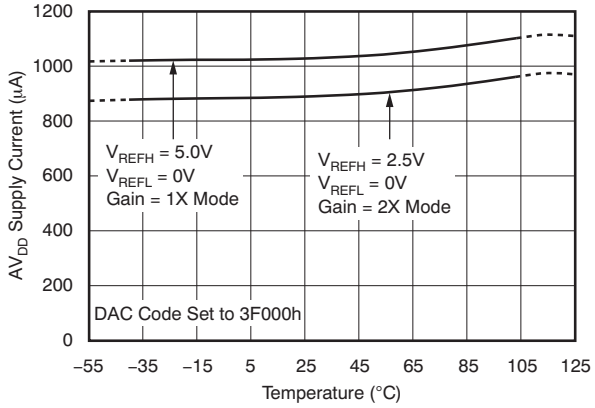


Figure 22. AVDD Supply Current vs Temperature

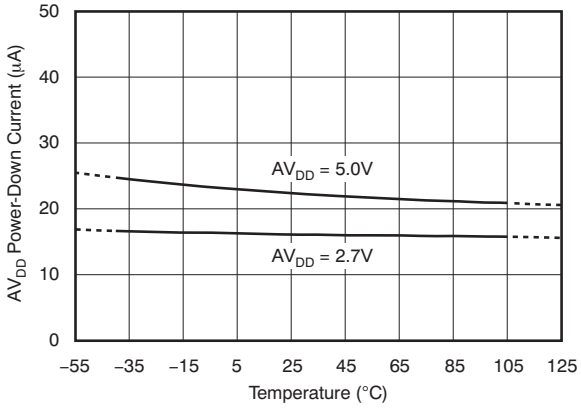


Figure 23. AVDD Power-Down Current vs Temperature

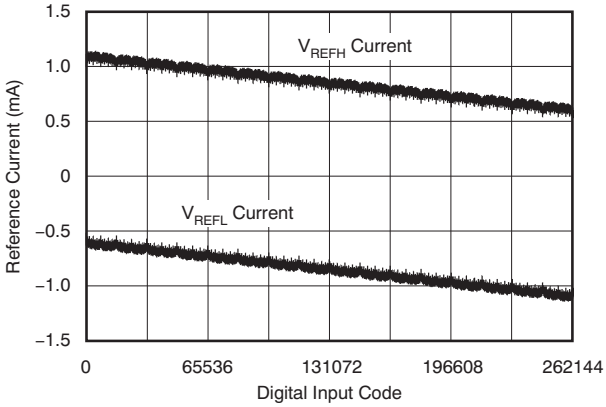


Figure 24. Reference Current vs Digital Input Code

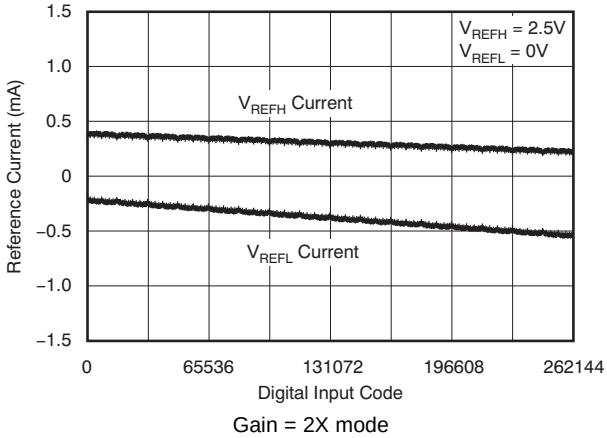


Figure 25. Reference Current vs Digital Input Code

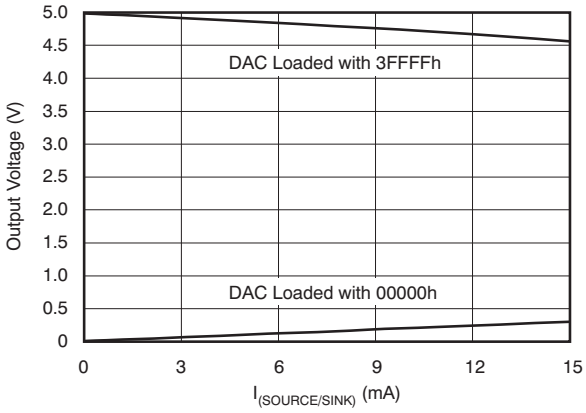


Figure 26. Output Voltage vs Drive Current Capability

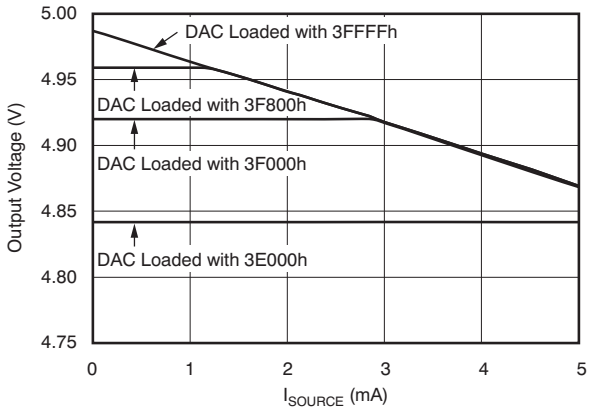


Figure 27. Output Voltage vs Drive Current Capability (Operation Near AV_{DD} Rail)

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Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, V_{REFH} = 5 V, V_{REFL} = 0 V, and gain = 1X mode (unless otherwise noted)

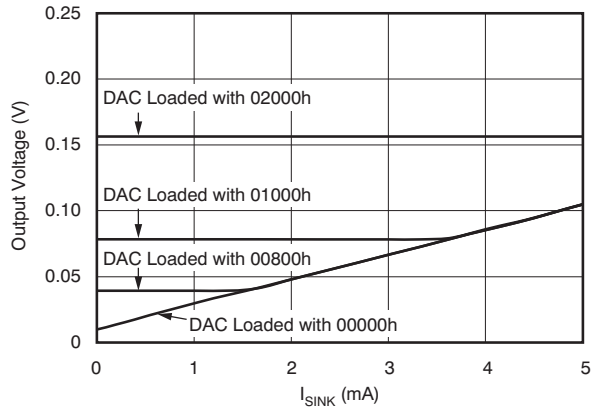


Figure 28. Output Voltage vs Drive Current Capability (Operation Near AGND Rail)

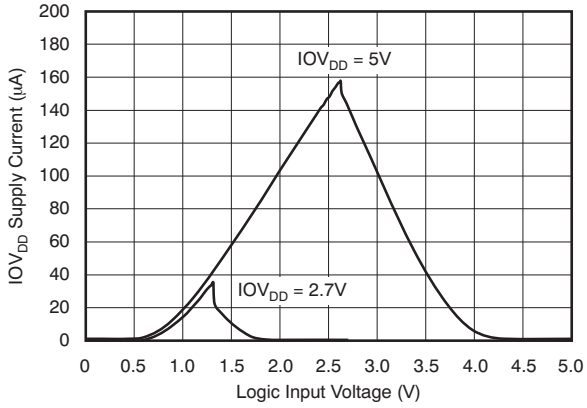


Figure 29. IOVDD Supply Current vs Logic Input Voltage

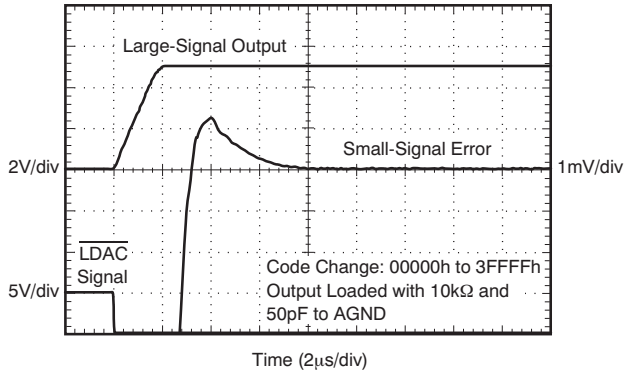


Figure 30. Large-Signal Settling Time

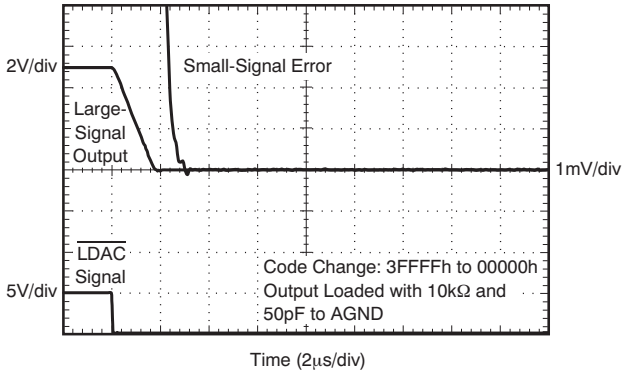


Figure 31. Large-Signal Settling Time

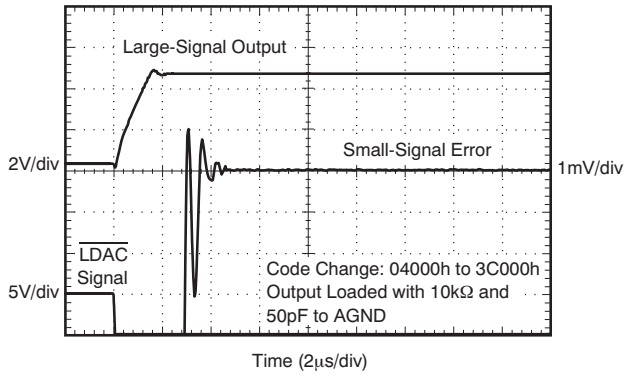


Figure 32. Large-Signal Settling Time

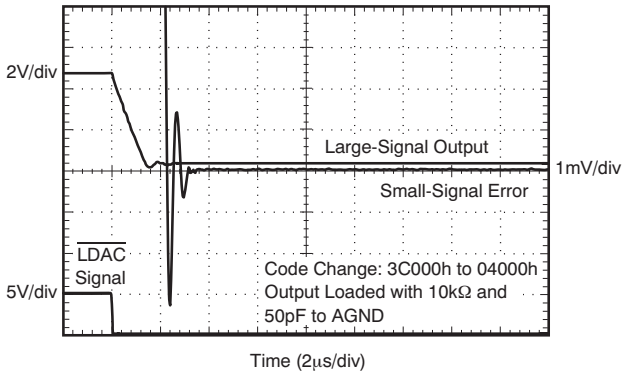
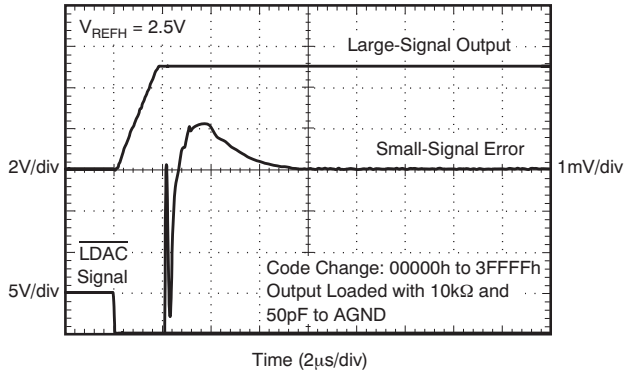


Figure 33. Large-Signal Settling Time

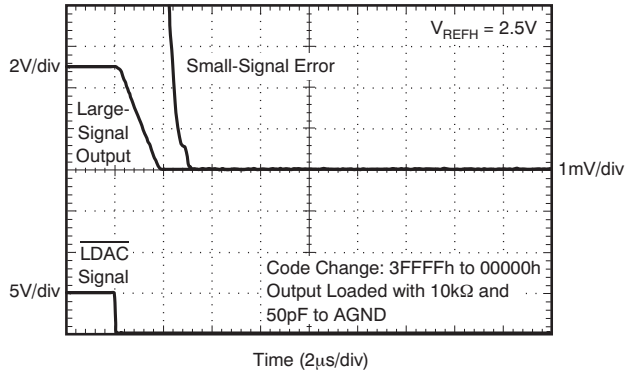
Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, V_{REFH} = 5 V, V_{REFL} = 0 V, and gain = 1X mode (unless otherwise noted)



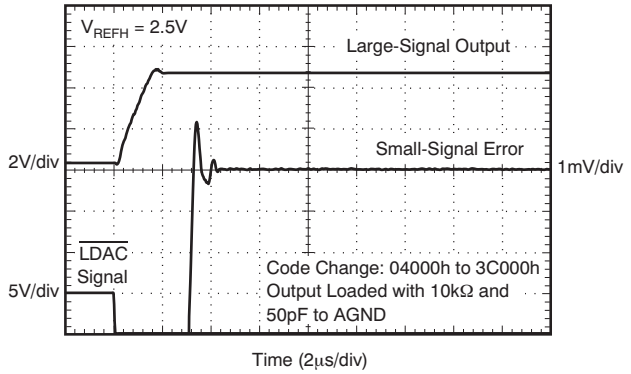
Gain = 2X mode

Figure 34. Large-Signal Settling Time



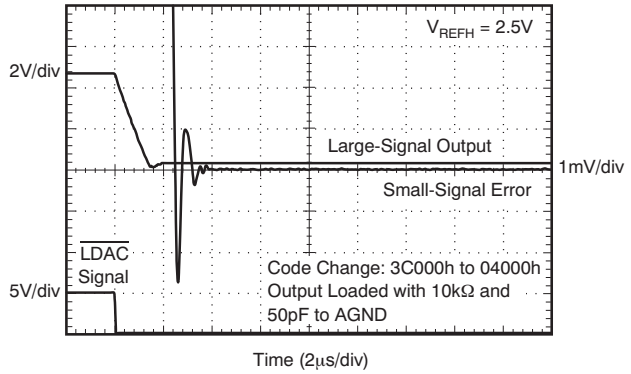
Gain = 2X mode

Figure 35. Large-Signal Settling Time



Gain = 2X mode

Figure 36. Large-Signal Settling Time



Gain = 2X mode

Figure 37. Large-Signal Settling Time

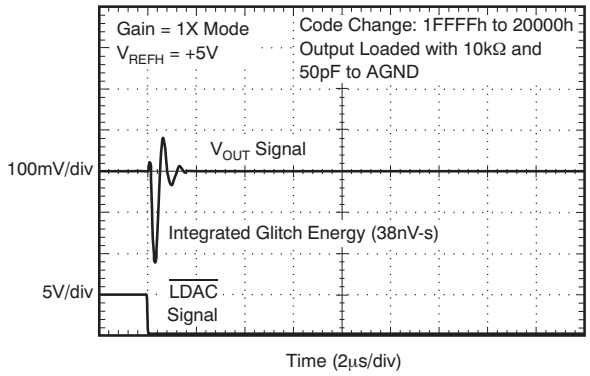


Figure 38. Major Carry Glitch

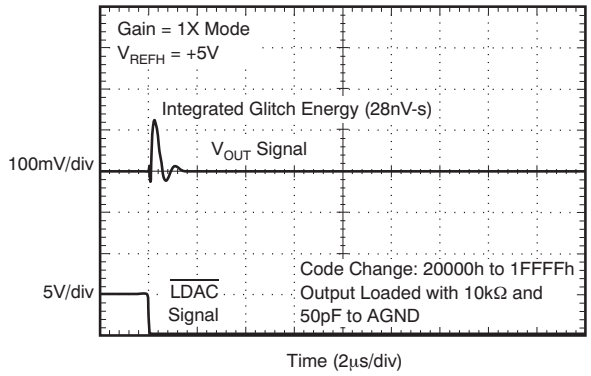


Figure 39. Major Carry Glitch

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Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, V_{REFH} = 5 V, V_{REFL} = 0 V, and gain = 1X mode (unless otherwise noted)

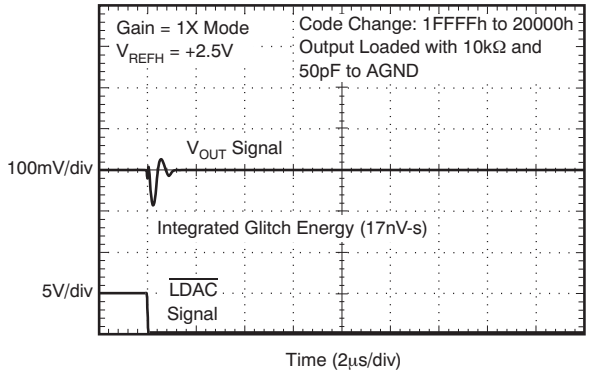

Figure 40. Major Carry Glitch

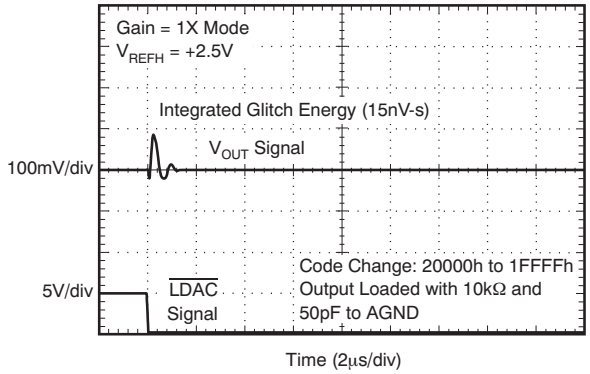

Figure 41. Major Carry Glitch

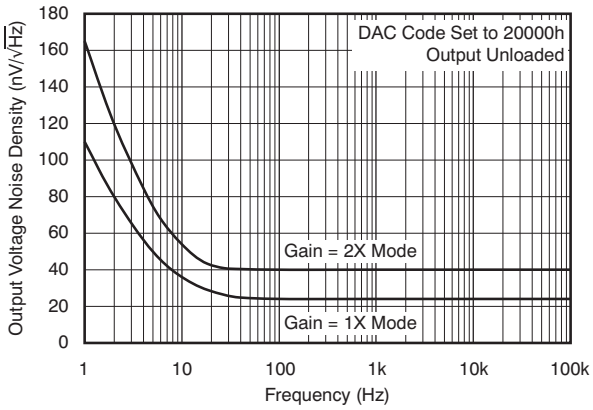

Figure 42. Output Noise Density vs Frequency

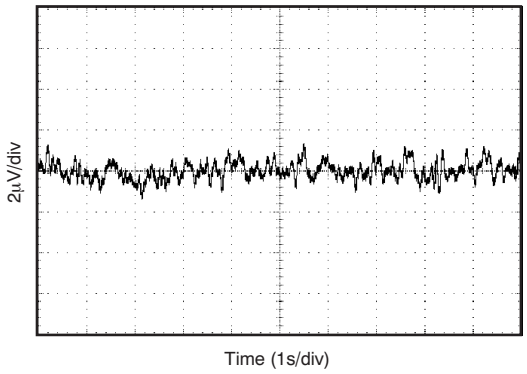

Figure 43. Low-Frequency Output Noise (0.1 Hz to 10 Hz)

6.10 Typical Characteristics: AV_{DD} = 2.7 V

at T_A = 25°C, V_{REFH} = 2.5 V, V_{REFL} = 0 V, and gain = 1X mode (unless otherwise noted)

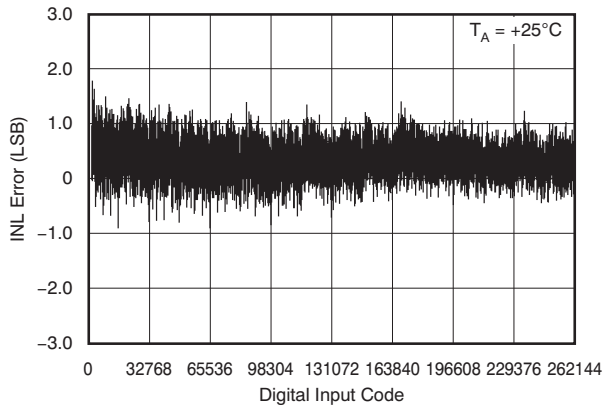

Figure 44. Linearity Error vs Digital Input Code

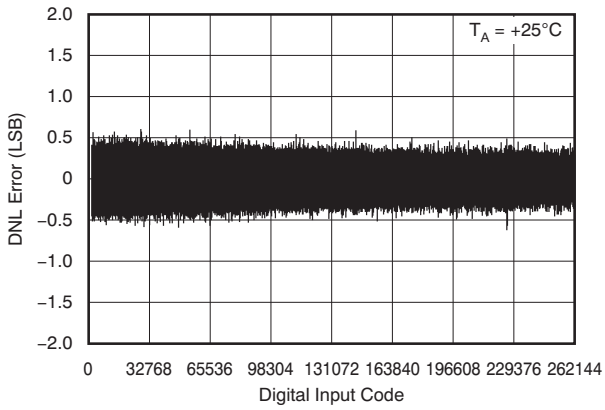

Figure 45. Differential Linearity Error vs Digital Input Code

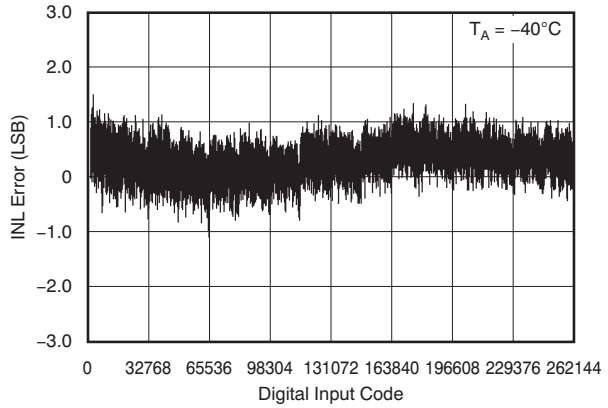

Figure 46. Linearity Error vs Digital Input Code

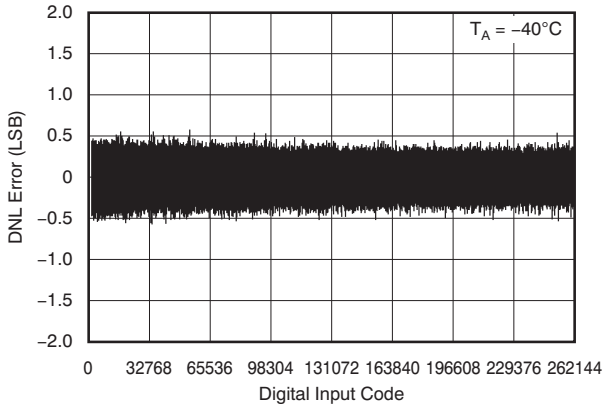

Figure 47. Differential Linearity Error vs Digital Input Code

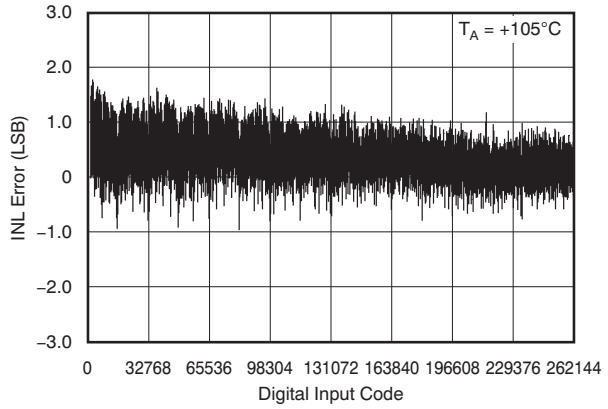

Figure 48. Linearity Error vs Digital Input Code

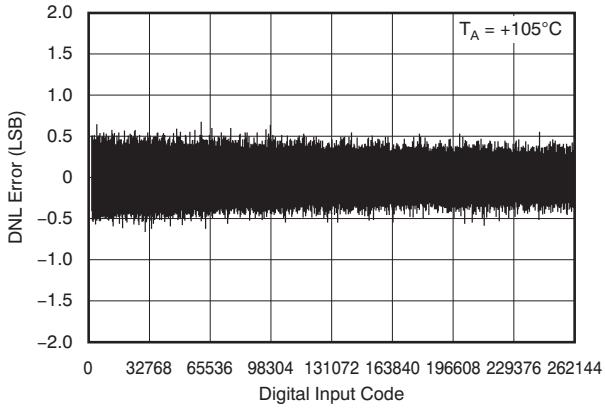

Figure 49. Differential Linearity Error vs Digital Input Code

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Typical Characteristics: AV_{DD} = 2.7 V (continued)

at T_A = 25°C, V_{REFH} = 2.5 V, V_{REFL} = 0 V, and gain = 1X mode (unless otherwise noted)

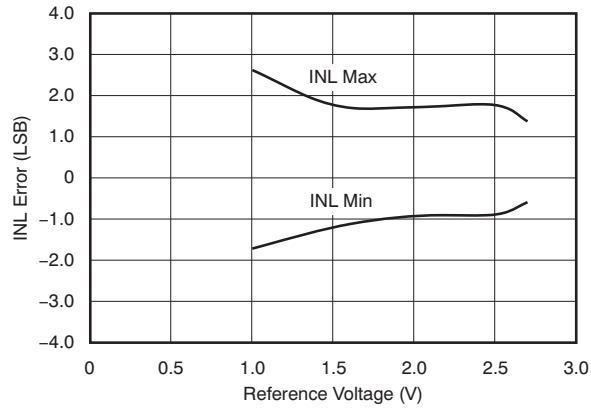


Figure 50. Linearity Error vs Reference Voltage

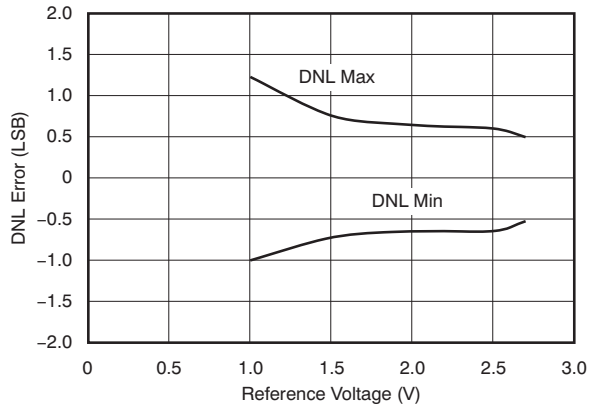


Figure 51. Differential Linearity Error vs Reference Voltage

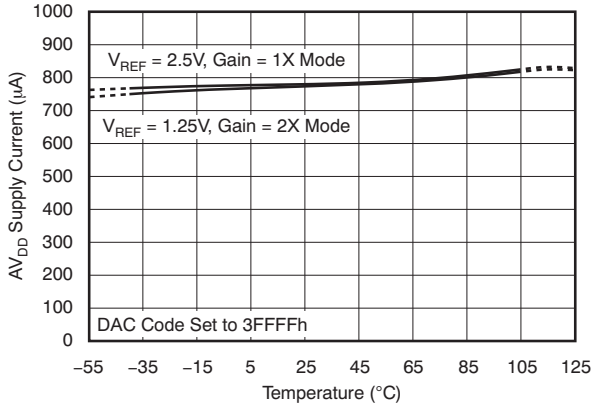


Figure 52. AVDD Supply Current vs Temperature

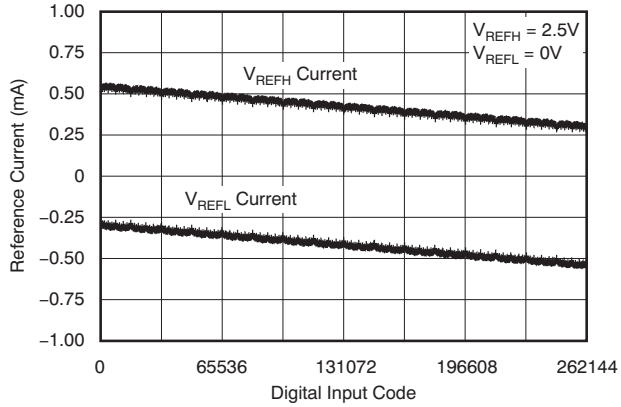
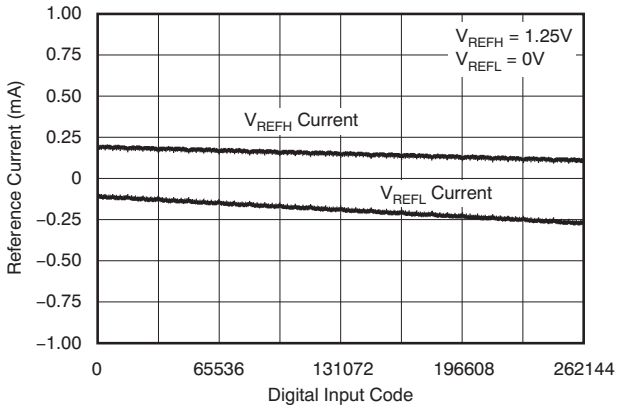


Figure 53. Reference Current vs Digital Input Code



Gain = 2X mode

Figure 54. Reference Current vs Digital Input Code

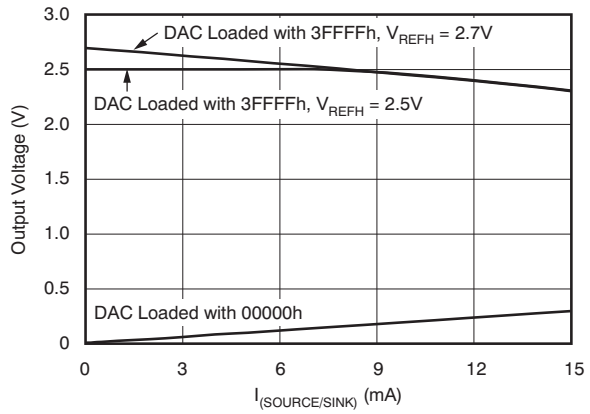


Figure 55. Output Voltage vs Drive Current Capability

Typical Characteristics: AV_{DD} = 2.7 V (continued)

at T_A = 25°C, V_{REFH} = 2.5 V, V_{REFL} = 0 V, and gain = 1X mode (unless otherwise noted)

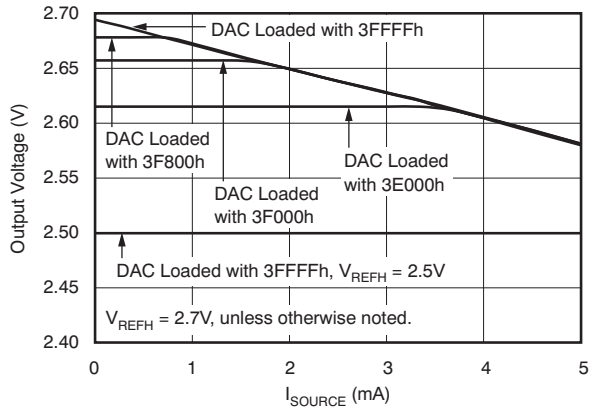


Figure 56. Output Voltage vs Drive Current Capability (Operation Near AV_{DD} Rail)

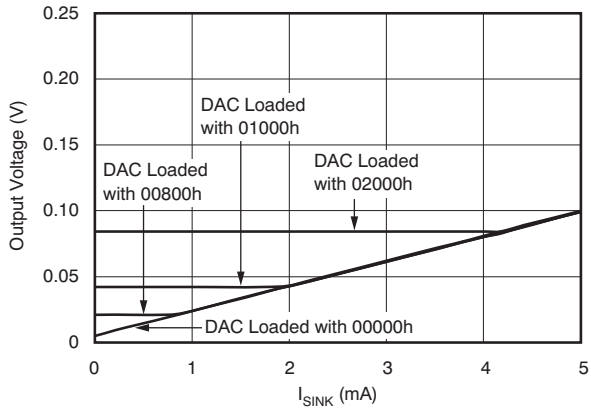


Figure 57. Output Voltage vs Drive Current Capability (Operation Near AGND Rail)

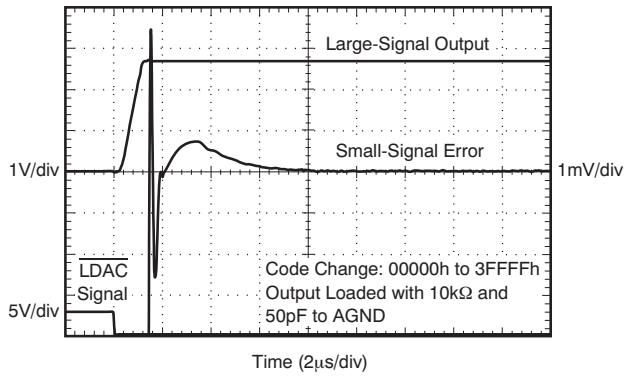


Figure 58. Large-Signal Settling Time

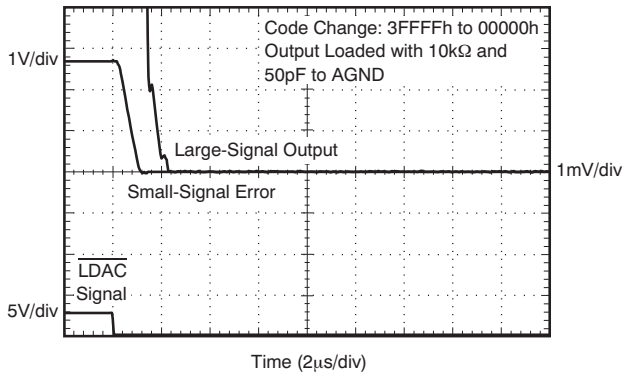


Figure 59. Large-Signal Settling Time

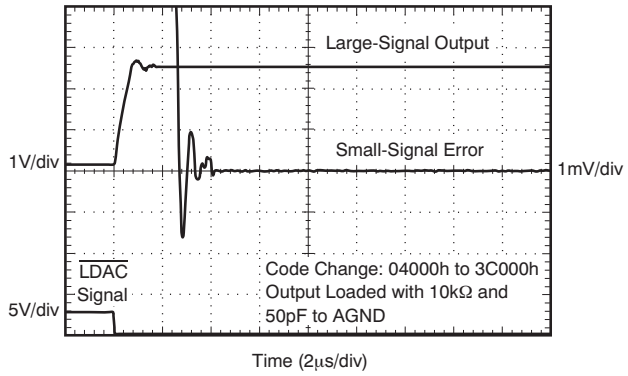


Figure 60. Large-Signal Settling Time

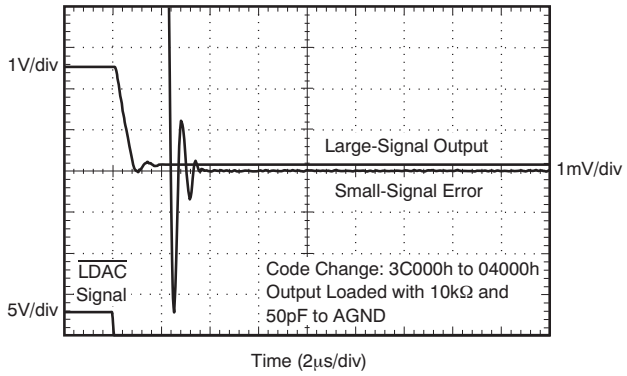


Figure 61. Large-Signal Settling Time

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Typical Characteristics: AV_{DD} = 2.7 V (continued)

at T_A = 25°C, V_{REFH} = 2.5 V, V_{REFL} = 0 V, and gain = 1X mode (unless otherwise noted)

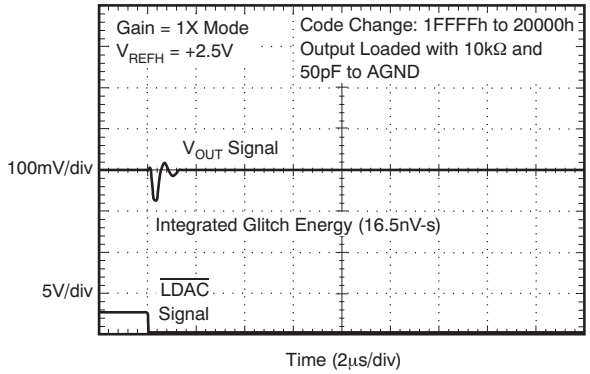

Figure 62. Major Carry Glitch

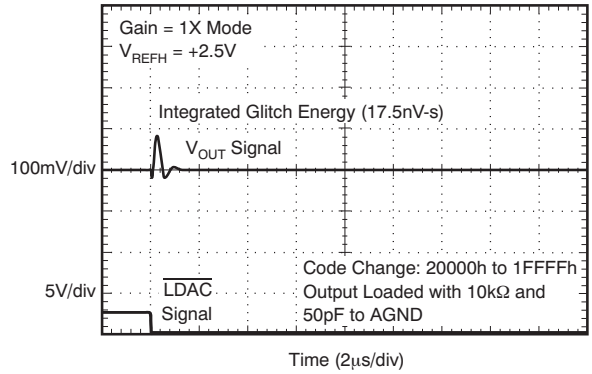

Figure 63. Major Carry Glitch

7 Detailed Description

7.1 Overview

The DAC9881 is a single-channel, 18-bit, serial-input, voltage-output digital-to-analog converter (DAC). The architecture is an R-2R ladder configuration with the four MSBs segmented, followed by an operational amplifier that serves as a buffer, as shown in Figure 64. The on-chip output buffer allows rail-to-rail output swings while providing a low output impedance to drive loads. The DAC9881 operates from a single analog power supply that ranges from 2.7 V to 5.5 V, and typically consumes 850 μA when operating with a 5-V supply. Data are written to the device in a 24-bit word format, using an SPI serial interface. To enable compatibility with 1.8-V, 3-V, or 5-V logic families, an IOV_{DD} supply pin is provided. This pin allows the DAC9881 input and output logic to be powered from the same logic supply used to interface signals to and from the device. Internal voltage translators are included in the DAC9881 to interface digital signals to the device core. See Figure 65 for the basic configuration of the DAC9881.

To provide a known power-up state, the DAC9881 is designed with a power-on reset function. Upon power-up, the DAC9881 is reset to either zero-scale or midscale depending on the state of the RSTSEL pin. A hardware reset can be performed by using the $\overline{RST}$ and RSTSEL pins.

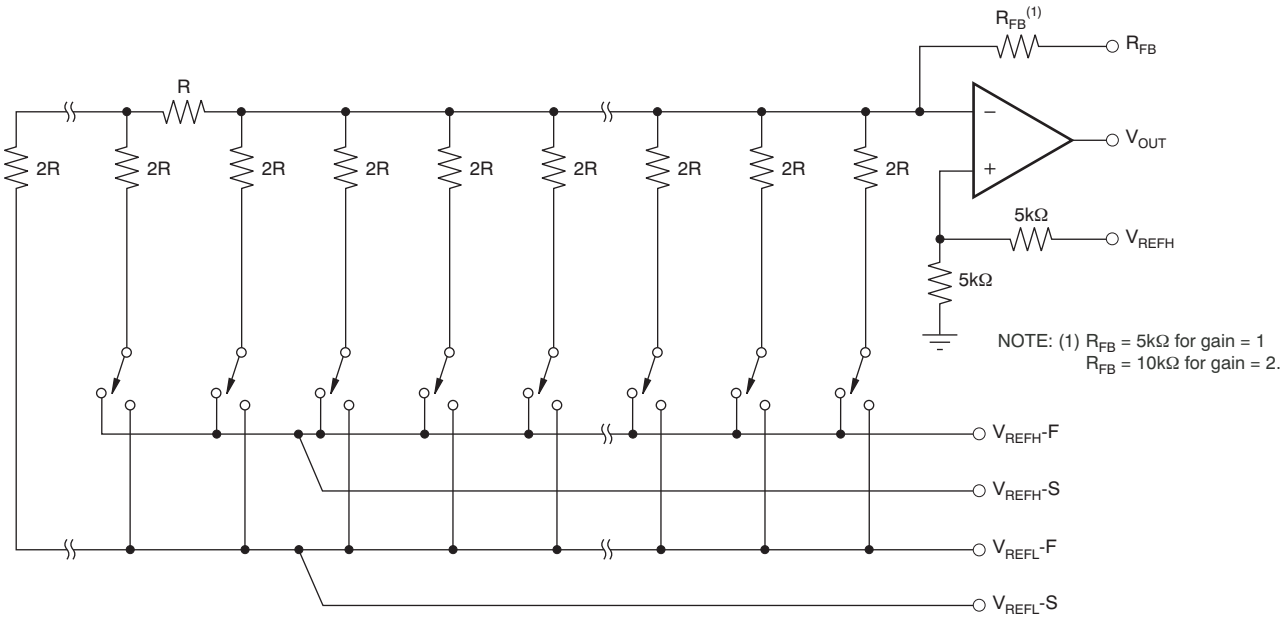

Figure 64. DAC9881 Architecture

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Overview (continued)

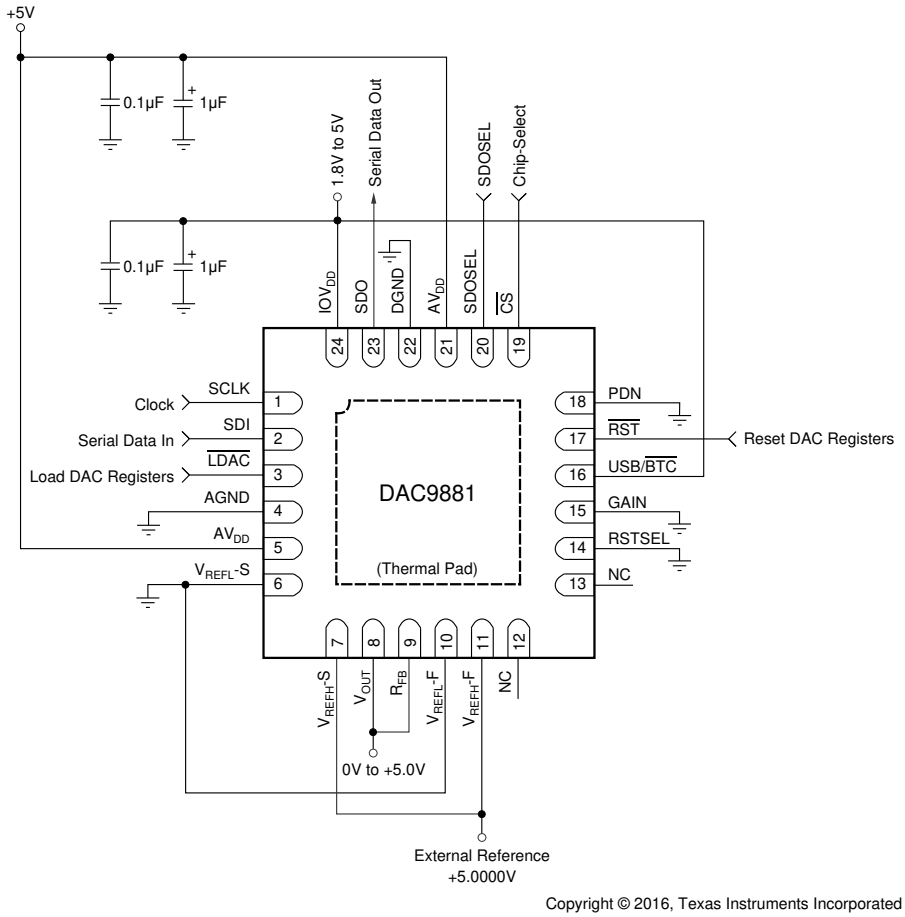
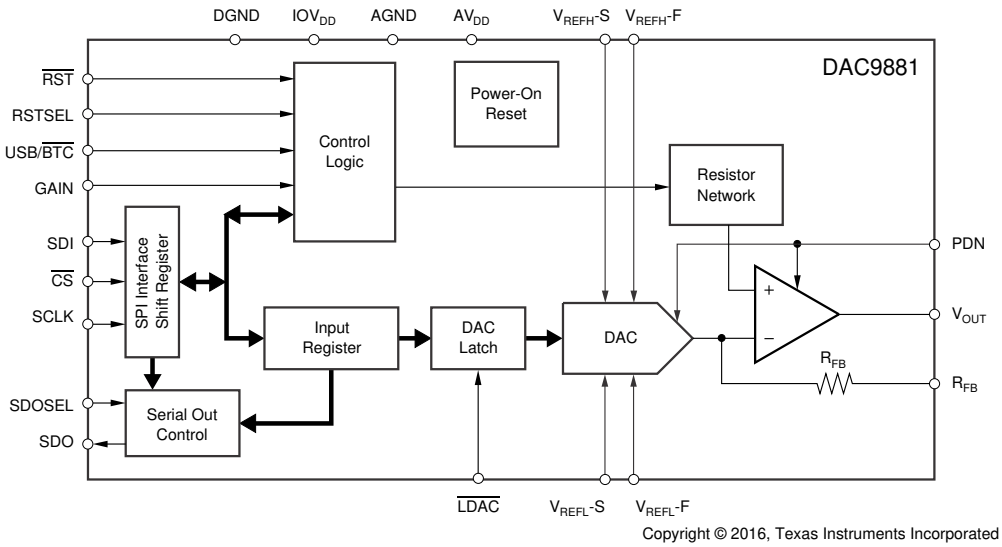


Figure 65. Basic Configuration

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Output

The DAC9881 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in Figure 66), thus ensuring an accurate output voltage. The output buffer V_{OUT} and R_{FB} pins are provided so that the output op amp buffer feedback can be connected at the load. Without a driven load, the DAC9881 output typically swings to within 15 mV of the AGND and AV_{DD} supply rails. Because of the high accuracy of these DACs, system design problems such as grounding and wiring resistance become very important. A 18-bit converter with a 5-V full-scale range has an LSB value of 19 µV. The DAC9881 has a typical feedback resistor current of 0.5 mA; thus, a series wiring resistance of only 100 mΩ (R_{W1}) causes a voltage drop of 50 µV. In terms of a system layout, the resistivity of a typical 1-ounce copper-clad printed circuit board (PCB) is 0.5-mΩ per square. For a 0.5-mA current, a 0.25-mm wide printed-circuit conductor 25-mm long results in a voltage drop of 25 µV.

NOTE

the wiring resistance of R_{W2} is not critical as long as the feedback resistor (R_{FB}) is connected at the driven load.

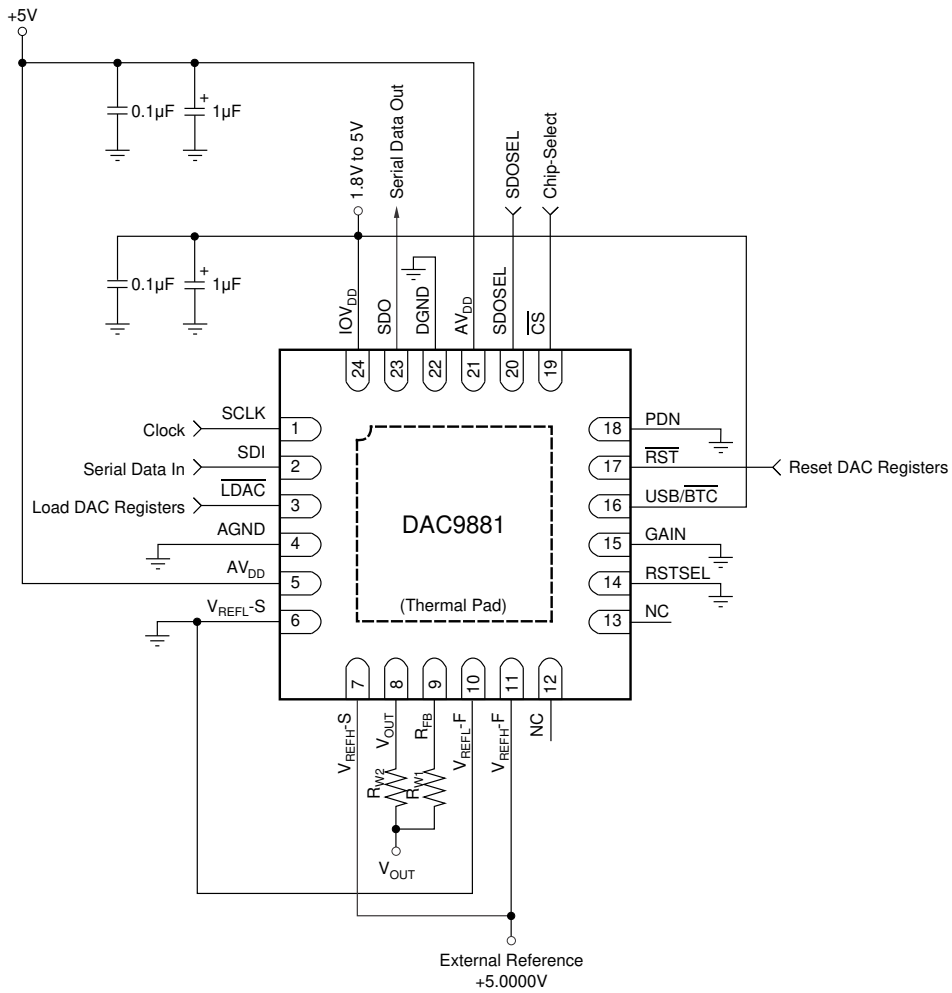


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Figure 66. Analog Output Closed-Loop Configuration (R_{W1} and R_{W2} Represent Wiring Resistance)

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Feature Description (continued)

7.3.2 Reference Inputs

The reference high input, V_{REFH}, can be set to any voltage in the range of 1.25 V to AV_{DD}. The reference low input, V_{REFL}, can be set to any voltage in the range of –0.2 V to +0.2 V (to provide a small offset to the output of the DAC9881, if desired). The current into V_{REFH} and out of V_{REFL} depends on the DAC code, and can vary from approximately 0.5 mA to 1 mA in the gain = 1X mode of operation. The reference high and low inputs appear as variable loads to the external reference circuit. If the external references can source or sink the required current, and if low impedance connections are made to the V_{REFH} and V_{REFL} pins, external reference buffers are not required. Figure 65 shows a simple configuration of the DAC9881 using external references without force and sense reference buffers.

Kelvin sense connections for the reference high and low are included on the DAC9881. When properly used with external reference buffer op amps, these reference Kelvin sense pins make sure that the driven reference high and low voltages remain stable versus varying reference load currents. Figure 67 shows an example of a reference force and sense configuration of the DAC9881 operating from a single analog reference voltage. Both the V_{REFL} and V_{REFH} reference voltages are set to levels of 100 mV from the DAC9881 supply rails, and are derived from a 5-V external reference. Figure 68 illustrates the effect of not using the reference force and sense buffers to drive the DAC9881 V_{REFL} and V_{REFH} pins. Figure 69 shows the improvement when using the reference buffers. A slight degradation in INL and DNL performance is seen without the use of the force and sense buffer configuration.

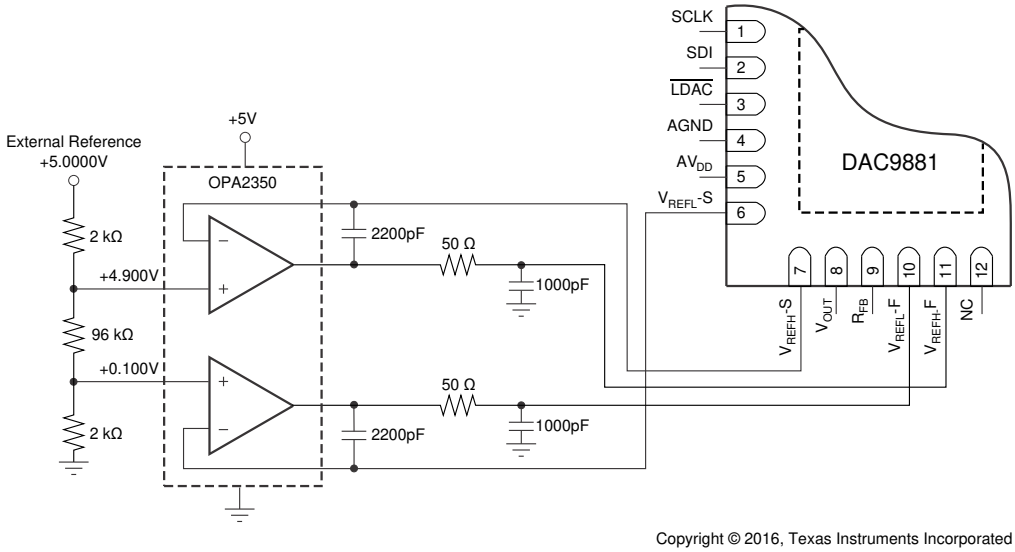

Figure 67. Buffered References (V_{REFH} = +4.900 V and V_{REFL} = 100 mV).

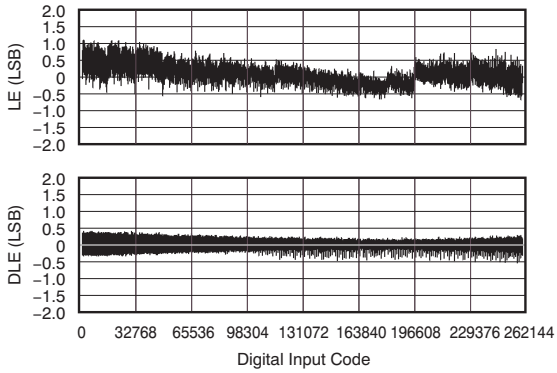

Figure 68. Linearity and Differential Linearity Error for Figure 65 Without Reference Buffers

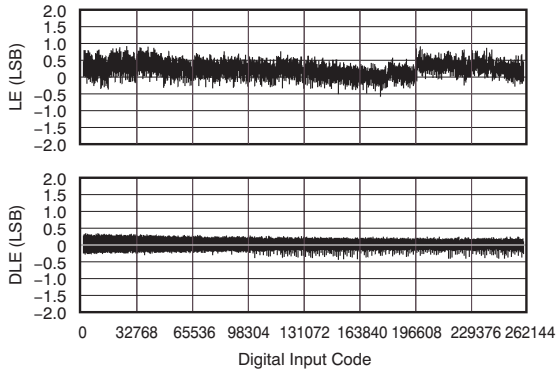

Figure 69. Linearity and Differential Linearity Error for Figure 67 With Reference Buffers

Feature Description (continued)

7.3.3 Output Range

The maximum output range of the DAC9881 is V_{REFL} to (V_{REFH} – V_{REFL}) × G, where *G* is the output buffer gain set by the GAIN pin. When the GAIN pin is connected to DGND, the output buffer gain = 1. When the GAIN pin is connected to IOV_{DD}, the output buffer gain = 2. The output range must not be greater than AV_{DD}; otherwise, output saturation occurs. The DAC9881 output transfer function is given in Equation 1:

$$V_{OUT} = \frac{V_{REFH} - V_{REFL}}{262144} \times \text{CODE} \times \text{Buffer Gain} + V_{REFL}$$

where

- CODE = 0 to 262143. This is the digital code loaded to the DAC
- Buffer Gain = 1 or 2 (set by the GAIN pin)
- V_{REFH} = reference high voltage applied to the device
- V_{REFL} = reference low voltage applied to the device (1)

7.3.4 Input Data Format

The USB/$\overline{BTC}$ pin defines the input data format. When this pin is connected to IOV_{DD}, the input data format is straight binary, as shown in Table 1. When this pin is connected to DGND, the input data format is twos complement, as shown in Table 2.

Table 1. Output vs Straight Binary Code

USB CODE	5-V RANGE	DESCRIPTION
3FFFFh	+4.99998	+Full-scale – 1 LSB
30000h	+3.75000	3/4-scale
20000h	+2.50000	Midscale
10000h	+1.25000	1/4-scale
00000h	0.00000	Zero-scale

Table 2. Output vs Twos Complement Code

$\overline{BTC}$ CODE	5-V RANGE	DESCRIPTION
1FFFFh	+4.99998	+Full-scale – 1 LSB
10000h	+3.75000	3/4-scale
00000h	+2.50000	Midscale
3FFFFh	+2.49998	Midscale – 1LSB
30000h	+1.25000	1/4-scale
20000h	0.00000	Zero-scale

7.3.5 Hardware Reset

When the $\overline{RST}$ pin is low, the device is in hardware reset, and the input register and DAC latch are set to the value defined by the RSTSEL pin. After $\overline{RST}$ goes high, the device is in normal operating mode, and the input register and DAC latch maintain the reset value until new data are written. When USB/$\overline{BTC}$ is connected to DGND, the device is in two's complement mode. In this mode, the $\overline{LDAC}$ pin cannot be kept at logic level 0 or toggled when a hardware reset is issued before writing a valid DAC data.

7.3.6 Power-On Reset

The DAC9881 has a power-on reset feature. After power-on, the value of the input register, the DAC latch, and the output from the V_{OUT} pin are set to the value defined by the RSTSEL pin.

7.3.6.1 Program Reset Value

After a power-on reset or a hardware reset, the output voltage from the V_{OUT} pin and the values of the input register and DAC latch are determined by the status of the RSTSEL pin and the input data format, as shown in Table 3.

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Table 3. Reset Values

$\overline{LDAC}$ PIN	RSTSEL PIN	USB/$\overline{BTC}$ PIN	INPUT FORMAT	V_{OUT}	VALUE OF INPUT REGISTER AND DAC LATCH
DGND or IOV_{DD}	DGND	IOV_{DD}	Straight Binary	0	00000h
DGND or IOV_{DD}	IOV_{DD}	IOV_{DD}	Straight Binary	Midscale	20000h
IOV_{DD}	DGND	DGND	Twos Complement	0	00000h
IOV_{DD}	IOV_{DD}	DGND	Twos Complement	Midscale	20000h

7.3.7 Power Down

The DAC9881 has a hardware power-down feature. When the PDN pin is high, the device is in power-down mode. When the device is in power-down, the V_{OUT} pin is connected to ground through an internal 10kΩ resistor, but the contents of the input register and the DAC latch do not change and SPI communication remains active. When the PDN pin returns low, the device returns to normal operation.

7.3.8 Double-Buffered Interface

The DAC9881 has a double-buffered interface consisting of two register banks: the input register and the DAC latch. The input register is connected directly to the input shift register and the digital code is transferred to the input register upon completion of a valid write sequence. The DAC latch contains the digital code used by the resistor R-2R ladder. The contents of the DAC latch defines the output from the DAC.

Access to the DAC latch is controlled by the $\overline{LDAC}$ pin. When $\overline{LDAC}$ is high, the DAC latch is latched and the input register can change state without affecting the contents of the DAC latch. When $\overline{LDAC}$ is low, however, the DAC latch becomes transparent and the contents of the input register is transferred to the DAC register.

7.3.8.1 Load DAC Pin ($\overline{LDAC}$)

$\overline{LDAC}$ transfers data from the input register to the DAC latch (and, therefore, updates the DAC output). The contents of the DAC latch (and the output from DAC) can be changed in two ways, depending on the status of $\overline{LDAC}$.

7.3.8.1.1 Synchronous Mode

When $\overline{LDAC}$ is tied low, the DAC latch updates as soon as new data are transferred into the input register after the rising edge of $\overline{CS}$.

7.3.8.1.2 Asynchronous Mode

When $\overline{LDAC}$ is high, the DAC latch is latched. The DAC latch (and DAC output) is not updated at the same time that the input register is written to. When $\overline{LDAC}$ goes low, the DAC latch updates with the contents of the input register.

7.3.9 1.8-V to 5-V Logic Interface

All digital input and output pins are compatible with any logic supply voltage between 1.8 V and 5 V. Connect the interface logic supply voltage to the IOV_{DD} pin. Although timing is specified down to 2.7 V (see the *timing diagrams*), IOV_{DD} can operate as low as 1.8 V, but with degraded timing and temperature performance. For the lowest power consumption, logic V_{IH} levels should be as close as possible to IOV_{DD}, and logic V_{IL} levels should be as close as possible to GND.

7.3.10 Power-Supply Sequence

For the device to work properly, IOVDD must not come up before AV_{DD}, and the reference voltage must come up after the AV_{DD} supply. Additionally, because the DAC input shift register is not reset during a power-on reset or hardware reset, the $\overline{CS}$ pin must not be unintentionally asserted during power-up of the device. To avoid improper power-up, it is recommended that the $\overline{CS}$ and $\overline{LDAC}$ pins be connected to IOV_{DD} through pullup resistors. To make sure that the electrostatic discharge (ESD) protection circuitry of this device is not activated, all other digital pins must be held at ground potential until IOV_{DD} is applied.

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7.4 Device Functional Modes

7.4.1 Serial Interface

The DAC9881 is controlled by a versatile three-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with SPI, QSPI™, MICROWIRE, and DSP interface standards.

7.4.1.1 Input Shift Register

Data are loaded into the device as a 24-bit word under the control of the serial clock input, SCLK. The timing diagrams for this operation are shown in *timing diagrams* section.

The $\overline{CS}$ input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can be transferred into the device only while $\overline{CS}$ is low. When $\overline{CS}$ is high, the SCLK and SDI signals are blocked out, and SDO is in high-Z status. To start the serial data transfer, $\overline{CS}$ should be taken low, observing the minimum delay from $\overline{CS}$ falling edge to SCLK rising edge, t_2. After $\overline{CS}$ goes low, serial input data from SDI are clocked into the device input shift register on the rising edges of SCLK for 24 or more clock pulses. If a frame contains less than 24 bits of data, the frame is invalid. Invalid input data are not written into the input register and DAC, although the input register and DAC will continue to hold data from the preceding valid data cycle. If more than 24 bits of data are transmitted in one frame, the last 24 bits are written into the shift register and DAC. $\overline{CS}$ may be taken high after the rising edge of the 24th SCLK pulse, observing the minimum SCLK rising edge to $\overline{CS}$ rising edge time, t_7. The contents of the shift register are transferred into the input register on the rising edge of $\overline{CS}$. When data have been transferred into the input register of the DAC, the corresponding DAC register and DAC output can be updated by taking the $\overline{LDAC}$ pin low. Table 4 shows the input shift register data word format. D17 is the MSB of the 18-bit DAC data.

Table 4. Input Shift Register Data Word Format

BIT	B23	B22	B21	B20	B19	B18	B17 (MSB)	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
DATA	X(1)	X	X	X	X	X	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

(1) X = don't care.

7.4.1.1.1 Stand-Alone Mode

When the SDOSEL pin is tied to IOV_{DD}, the interface is in Stand-Alone mode. This mode provides serial readback for diagnostic purposes. The new input data (24 bits) are clocked into the device shift register and the existing data in the input register (24 bits) are shifted out from the SDO pin. If more than 24 SCLKs are clocked when $\overline{CS}$ is low, the contents of the input register are shifted out from the SDO pin, followed by zeroes; the last 24 bits of input data remain in the shift register. If less than 24 SCLKs are clocked while $\overline{CS}$ is low, the data from the SDO pin are part of the data in the input register and must be ignored. Refer to Figure 2 for further details.

7.4.1.1.2 Daisy-Chain Mode

When the SDOSEL pin is tied to GND, the interface is in Daisy-Chain mode. For systems that contain several DACs, the SDO pin may be used to daisy-chain several devices together.

In Daisy-Chain mode, SCLK is continuously applied to the input shift register while $\overline{CS}$ is low. If more than 24 clock pulses are applied, the data ripple out of the shift register and appear on the SDO line. These data are clocked out on the falling edge of SCLK and are valid on the rising edge. By connecting this line to the SDI input on the next DAC in the chain, a multi-DAC interface is constructed. 24 clock pulses are required for each DAC in the chain. Therefore, the total number of clock cycles must be equal to (24 x *N*), where *N* is the total number of devices in the chain. When the serial transfer to all devices is complete, $\overline{CS}$ should be taken high. This action prevents any further data from being clocked into the input shift register. The contents in the shift registers are transferred into the relevant input registers on the rising edge of the $\overline{CS}$ signal.

A continuous SCLK source may be used if $\overline{CS}$ can be held low for the correct number of clock cycles. Alternatively, a burst clock containing the exact number of clock cycles can be used and $\overline{CS}$ can be taken high some time later. When the transfer to all input registers is complete, a common $\overline{LDAC}$ signal updates all DAC registers, and all analog outputs update simultaneously.

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8 Application and Implementation

NOTE

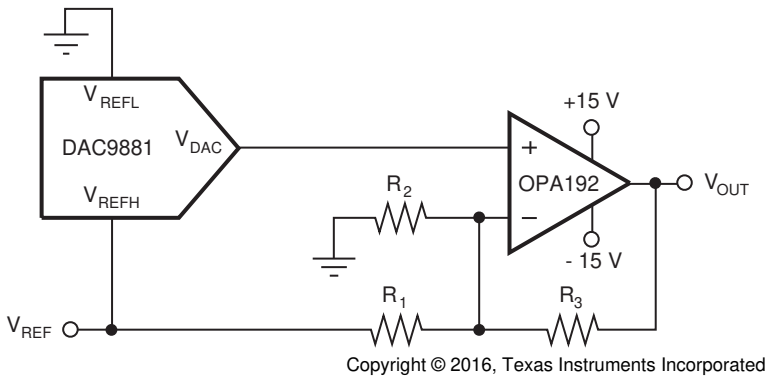
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The excellent linearity as well as low-noise and fast settling time makes the DAC9881 a strong performer in applications such as automatic test equipment, precision instrumentation and data acquisition systems. Additionally, the energy saving feature of the device, through the PDN pin, significantly reduces power dissipation -- this mode reduces current consumption, as low as 25 µA with a 5-V supply.

8.1.1 Bipolar Operation Using the DAC9881

The DAC9881 is designed for single-supply operation; however, a bipolar output is also possible using the circuit shown in Figure 70. This circuit gives a bipolar output voltage of VOUT. When GAIN = 1, VOUT can be calculated using Equation 2:



Some pins are omitted for clarity.

Figure 70. Bipolar Output Range

$$V_{OUT}(CODE) = \left[\left(V_{REF} \times \frac{CODE}{2^{18}}\right)\left(1 + \frac{R_3}{R_2} + \frac{R_3}{R_1}\right) - \left(V_{REF} \times \frac{R_3}{R_1}\right)\right]$$

where

- V_{OUT}(CODE) = output voltage vs code
- CODE = 0 to 262143. This is the digital code loaded to the DAC
- V_{REF} = reference voltage applied to the DAC9881 (2)

As an example, a ±8-V output span can be achieved by using values of 5 V, 6.25 kΩ, 16.67 kΩ, and 10 kΩ for Vref, R1, R2, and R3 respectively.

8.2 Typical Application

8.2.1 DAC9881 Sample-and-Hold Circuit

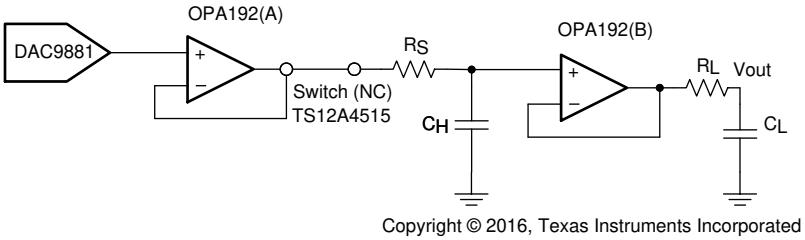


Figure 71. DAC9881 Sample-and-Hold Circuit

8.2.1.1 Design Requirements

The inherent architecture of the DAC9881, which consists of an R-2R architecture, enables great performance in regards to noise and accuracy, but at a cost of large glitch area. Glitch area, also known as glitch impulse area, is defined as the area associated with the overshoot or undershoot created by a code transition, and is generally quantified in Volt-seconds. Different code-to-code transitions produce different levels of glitch impulses. DACs with R-2R architectures produce large glitches during major-carry transitions.

There are two methods that can be used to reduce this glitch area:

1. Add an external RC Filter to the output of the DAC.
   – The low-pass filter helps attenuate high-frequency glitches that would normally propagate to the DAC output. Best practice is to use a small resistor value, as large resistance develops a large potential drop and reduces the voltage seen at the load. Capacitor values can be determined from the desired cutoff frequency of the low-pass filter, as well as settling time.
2. Another technique is to employ a Sample and Hold (S&H) circuit following the DAC output.
   – In its simplest form, the sample and hold circuit can be constructed from the following components: a capacitive element, output buffer, and switch. A schematic of the simplified S&H is shown in Figure 72.

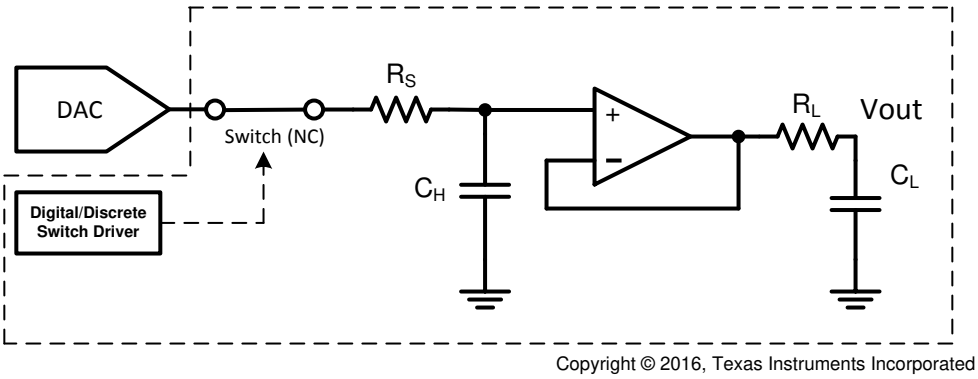


Figure 72. Simplified Sample and Hold Circuit

8.2.1.2 Detailed Design Procedure

The Sample/Track and Hold modes of operation correspond to the state of the switch, which connects the DAC output to the hold capacitor C_H. In sample mode – also referred to as track mode -- the switch is closed, allowing the capacitor to charge or discharge to the sampled DAC output voltage. The operational amplifier is configured as a buffer, which tracks and relays the voltage seen across C_H to the output of the circuit. In hold mode, the switch opens, disconnecting C_H from the DAC output. The DAC is updated while the circuit is in hold mode, preventing any DAC major carry glitches from propagating to the S&H output. The capacitor retains the previous sampled voltage, and this value is buffered to the output of the circuit. In real circuits, switch leakage and operational amplifier input bias current must be considered as it will impact circuit performance. The switch is generally controlled by an external discrete or digital driver.

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Typical Application (continued)

After the DAC glitch relays, the switch closes and re-enters sample or track mode.

More information related to this circuit can be found in *Sample and Hold Glitch Reduction for Precision Outputs Design Guide* (TIDU022).

8.2.1.3 Application Curves

Glitch reduction and total unadjusted error (TUE) plots of the solution presented in *Sample and Hold Glitch Reduction for Precision Outputs Design Guide* (TIDU022) is shown in the following plots. The glitch area is reduced from 35.11 nVs to 2.01 nVs.

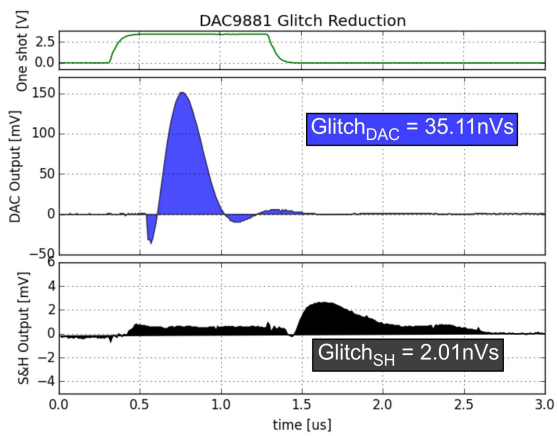
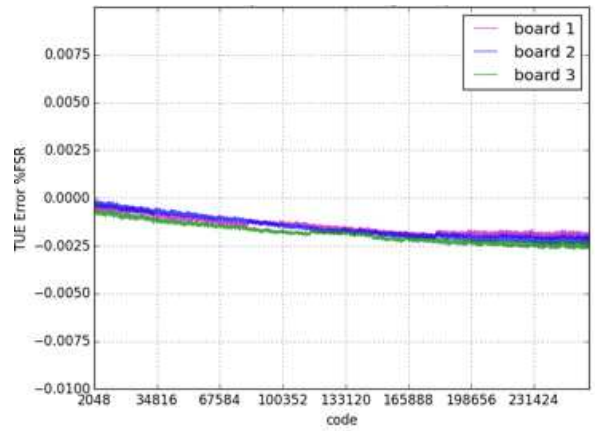


Figure 73. DAC9881 Sample-and-Hold TUE Error %FSR



C_H = 8.2 nF R_S = 14.7 Ω

Figure 74. Measured Glitch Area (20000h-1FFFFh) (Top) Digital Signal One-Shot Pulse; (Middle) DAC Output Glitch; (Bottom) S-H Output Glitch

8.3 System Example

Figure 75 displays a typical serial interface that may be used when connecting the DAC9881's SPI serial interface to a (master) microcontroller. The setup for the interface is as follows: The microcontroller's output SPI CLK drives the SCLK pin of the DAC9881, while the DAC9881 SDI pin is driven by the MOSI pin of the microcontroller. The $\overline{CS}$ pin of the DAC9881 can be asserted from a general program input/output pin of the microcontroller. When data are to be transmitted to the DAC9881, the $\overline{CS}$ pint is taken low. The data from the microcontroller is then transmitted to the DAC9881, totaling 24 bits latched into the DAC9881 device through the negative edge of SCLK. $\overline{CS}$ is then brought high after the completed write. The DAC9881 requires its data with the MSB as the first bit received.

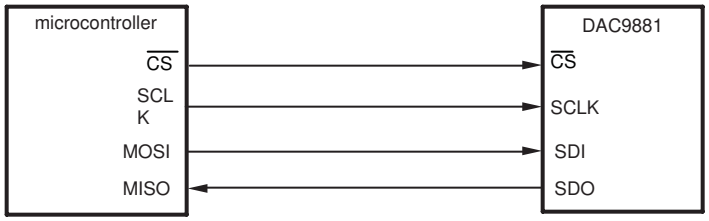


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Figure 75. Simplified Sample-and-Hold Circuit

9 Power Supply Recommendations

The DAC9881 operates within the specified supply voltage range of 2.7 V to 5.5 V. The power applied to AVDD should be well regulated and low noise. Switching power supplies and DC/DC converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. To further minimize noise from the power supply, a strong recommendation is to include a 1-µF to 10-µF capacitor and 0.1-µF bypass capacitor. The current consumption on the AVDD pin, the short-circuit current limit, and the load current for the device is listed in *Electrical Characteristics*. The power supply must meet the aforementioned current requirements.

10 Layout

10.1 Layout Guidelines

A precision analog component requires careful layout, the list below provides some insight into good layout practices.

- All Power Supply pins should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1 µF to 0.22 µF ceramic with a X7R or NP0 dielectric.
- Power supplies and VrefH/L bypass capacitors should be placed close to terminals to minimize inductance and optimize performance.
- A high-quality ceramic type NP0 or X7R is recommended for optimal performance across temperature, and a very low dissipation factor.
- The digital and analog sections should have proper placement with respect to the digital pins and analog pins of the DAC9881 device. The separation of analog and digital blocks allows for better design and practice because of less coupling into neighboring blocks, and less interaction between analog and digital return currents.

10.2 Layout Example

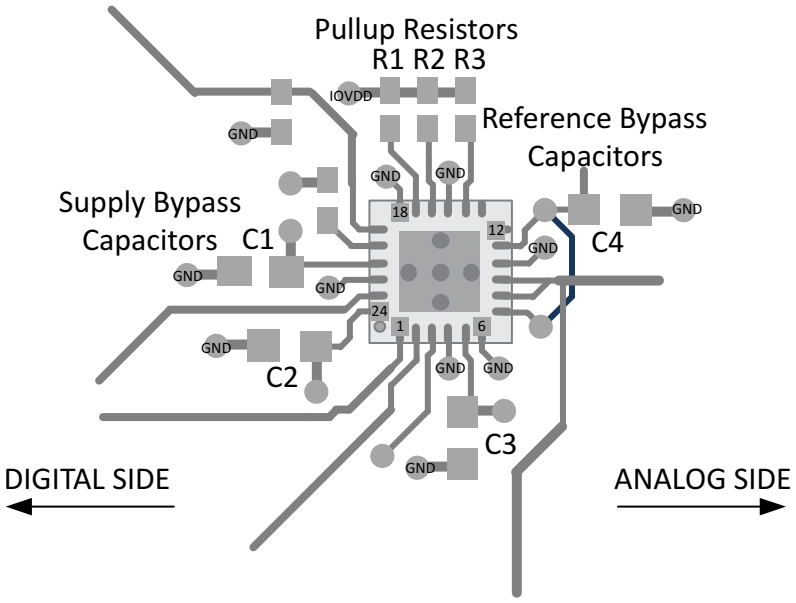

Figure 76. DAC9881 Basic Layout Example

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11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- *《DAC9881 评估模块用户指南》*
- *《通过采样和减少干扰实现高精度输出》*设计指南

11.2 接收文档更新通知

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11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC9881SBRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 105	DAC 9881 B	Samples
DAC9881SBRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 105	DAC 9881 B	Samples
DAC9881SRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 105	DAC 9881	Samples
DAC9881SRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 105	DAC 9881	Samples
DAC9881SRGETG4	ACTIVE	VQFN	RGE	24	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 105	DAC 9881	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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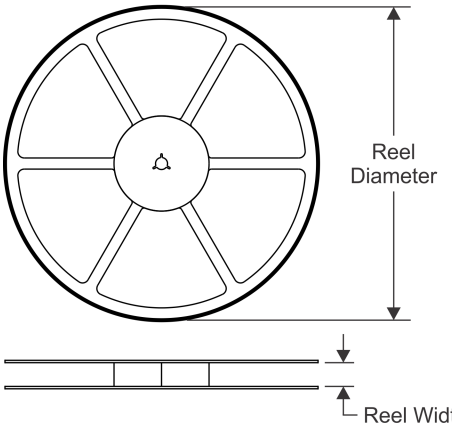
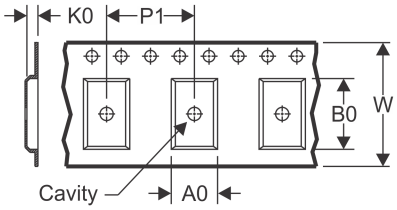
TAPE AND REEL INFORMATION

REEL DIMENSIONS

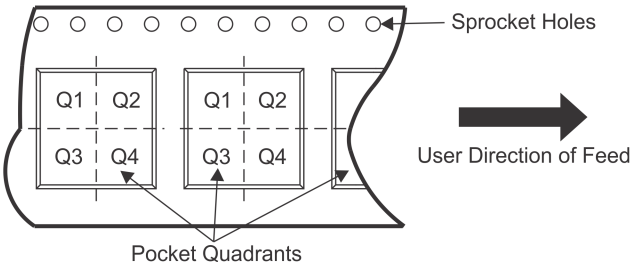


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

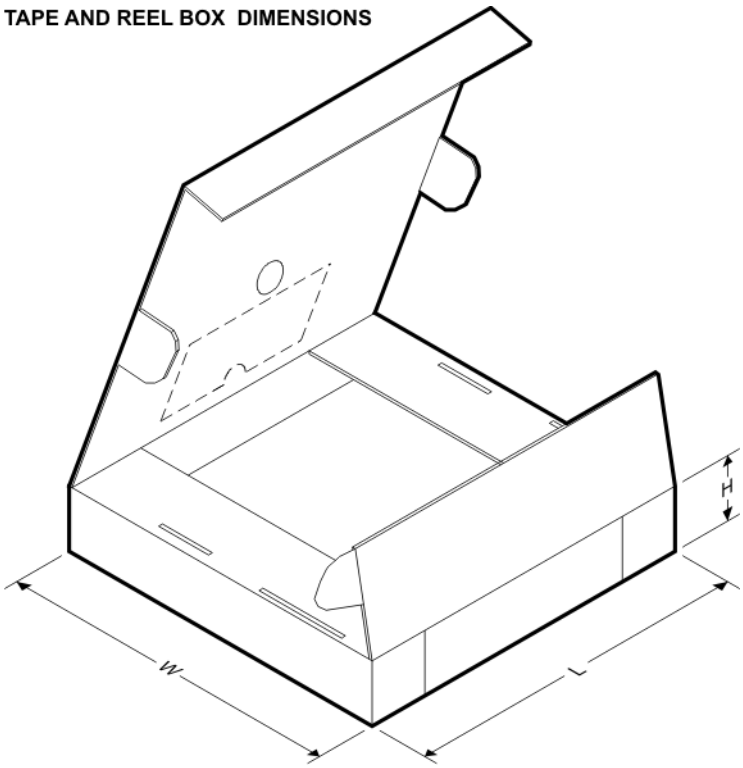
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC9881SBRGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
DAC9881SRGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

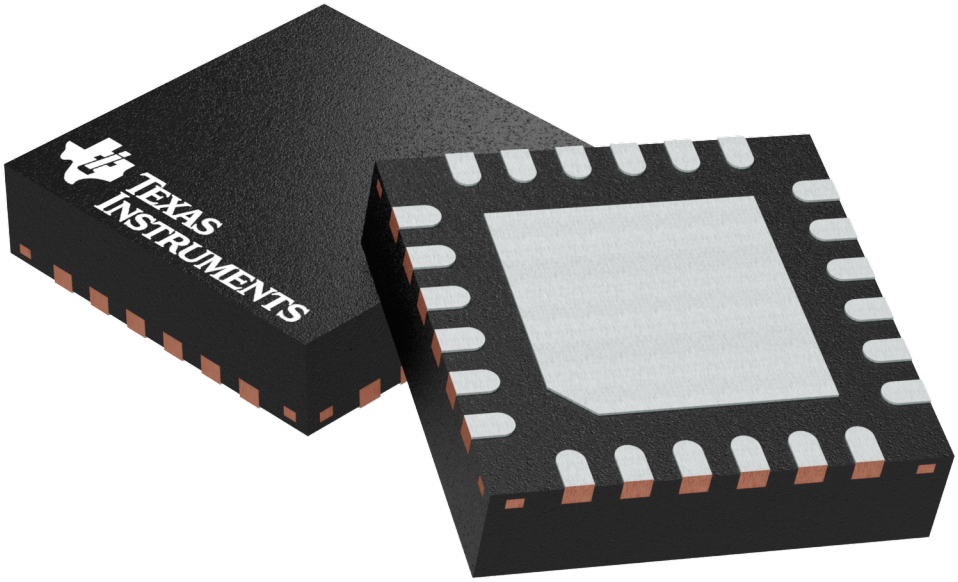


*All dimensions are nominal

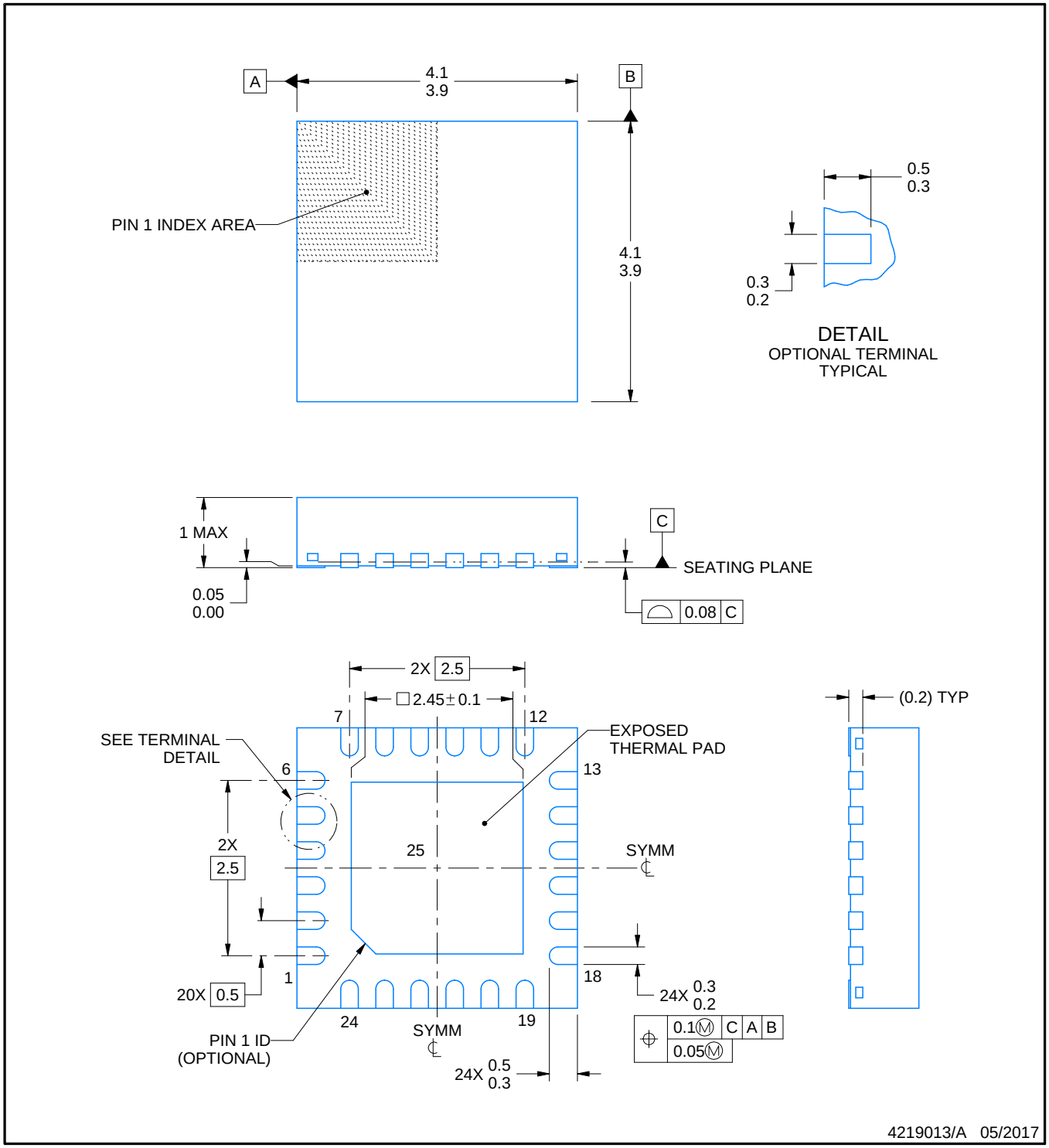
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC9881SBRGER	VQFN	RGE	24	3000	350.0	350.0	43.0
DAC9881SRGER	VQFN	RGE	24	3000	350.0	350.0	43.0

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

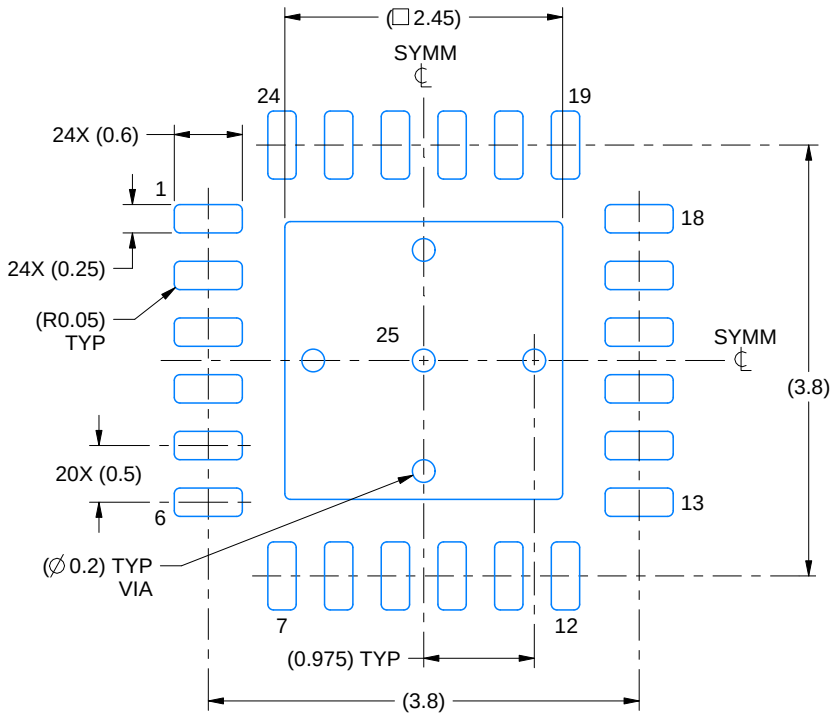


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

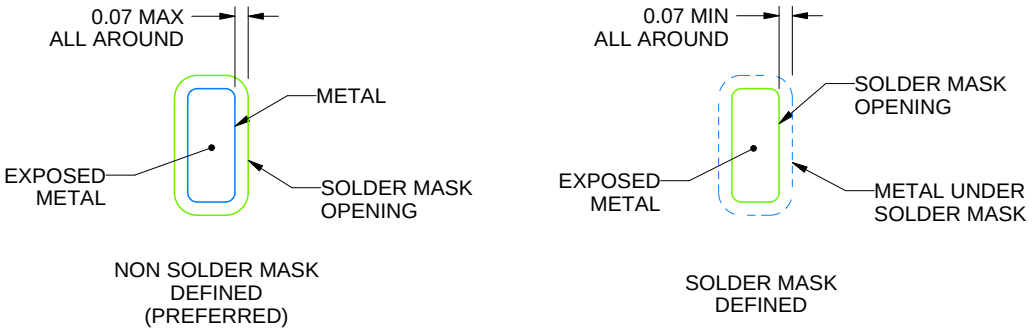


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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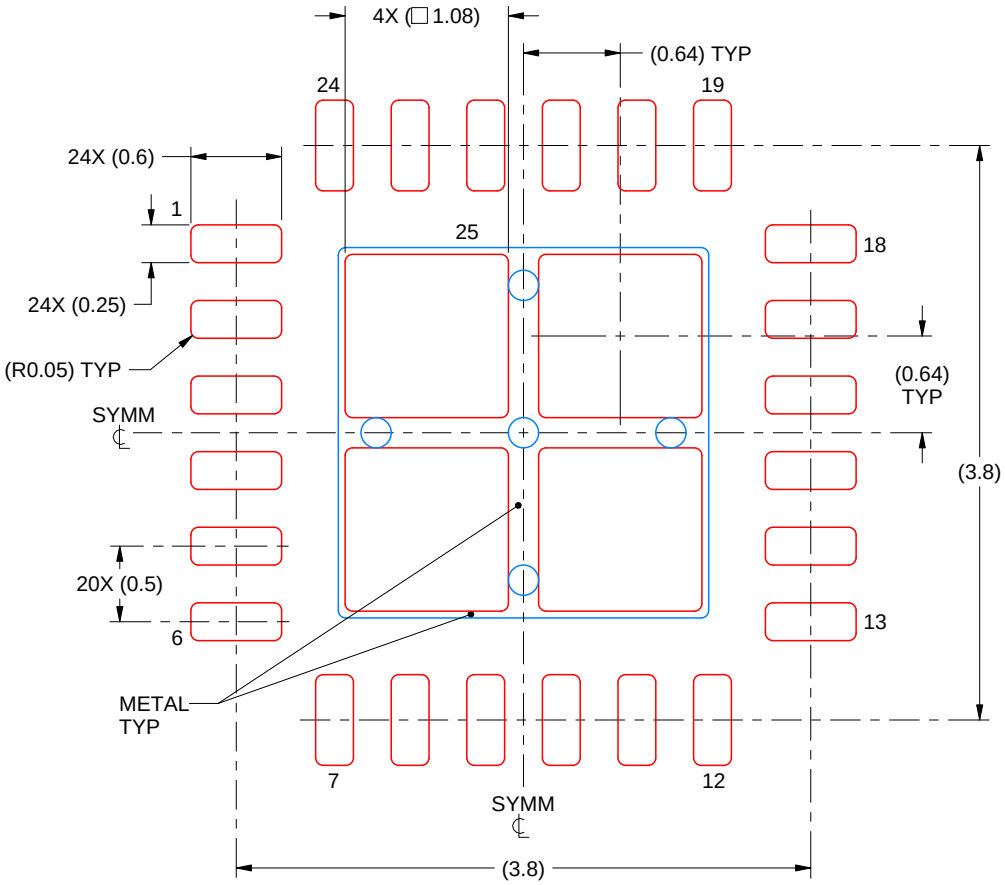
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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