- **Internal Look-Ahead Circuitry for Fast Counting**
- **Carry Output for N-Bit Cascading**
- **Fully Synchronous Operation for Counting**

D, DB, OR N PACKAGE
(TOP VIEW)

```
         _____
$\overline{CLR}$  [ 1    16 ] V_CC
 CLK  [ 2    15 ] RCO
   A  [ 3    14 ] Q_A
   B  [ 4    13 ] Q_B
   C  [ 5    12 ] Q_C
   D  [ 6    11 ] Q_D
 ENP  [ 7    10 ] ENT
 GND  [ 8     9 ] $\overline{LOAD}$
```

description

This synchronous, presettable, 4-bit binary counter has internal carry look-ahead circuitry for use in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. However, counting spikes can occur on the ripple-carry (RCO) output. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of CLK.

This counter is fully programmable. That is, it can be preset to any number between 0 and 15. Because presetting is synchronous, a low logic level at the load ($\overline{LOAD}$) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of ENP and ENT.

The clear function is asynchronous, and a low logic level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs to low, regardless of the levels of CLK, $\overline{LOAD}$, ENP, and ENT.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications, without additional gating. This function is implemented by the ENP and ENT inputs and an RCO output. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. RCO, thus enabled, produces a high-logic-level pulse while the count is 15 (HHHH). The high-logic-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

The SN74F161A features a fully independent clock circuit. Changes at ENP, ENT, or $\overline{LOAD}$ that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the setup and hold times.
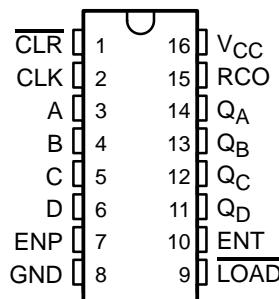
ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74F161AN	SN74F161AN
	SOIC – D	Tube	SN74F161AD	F161A
		Tape and reel	SN74F161ADR	
	SSOP – DB	Tape and reel	SN74F161ADBR	F161A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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TEXAS INSTRUMENTS

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state diagram

```
0  →  1  →  2  →  3  →  4
↑                       ↓
15                      5
↑                       ↓
14                      6
↑                       ↓
13                      7
↑                       ↓
12 ←  11 ← 10 ←  9  ←  8
```
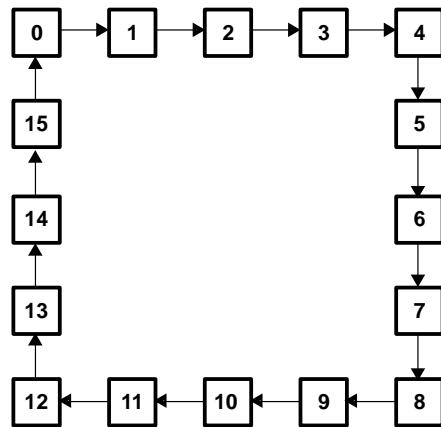
logic diagram (positive logic)
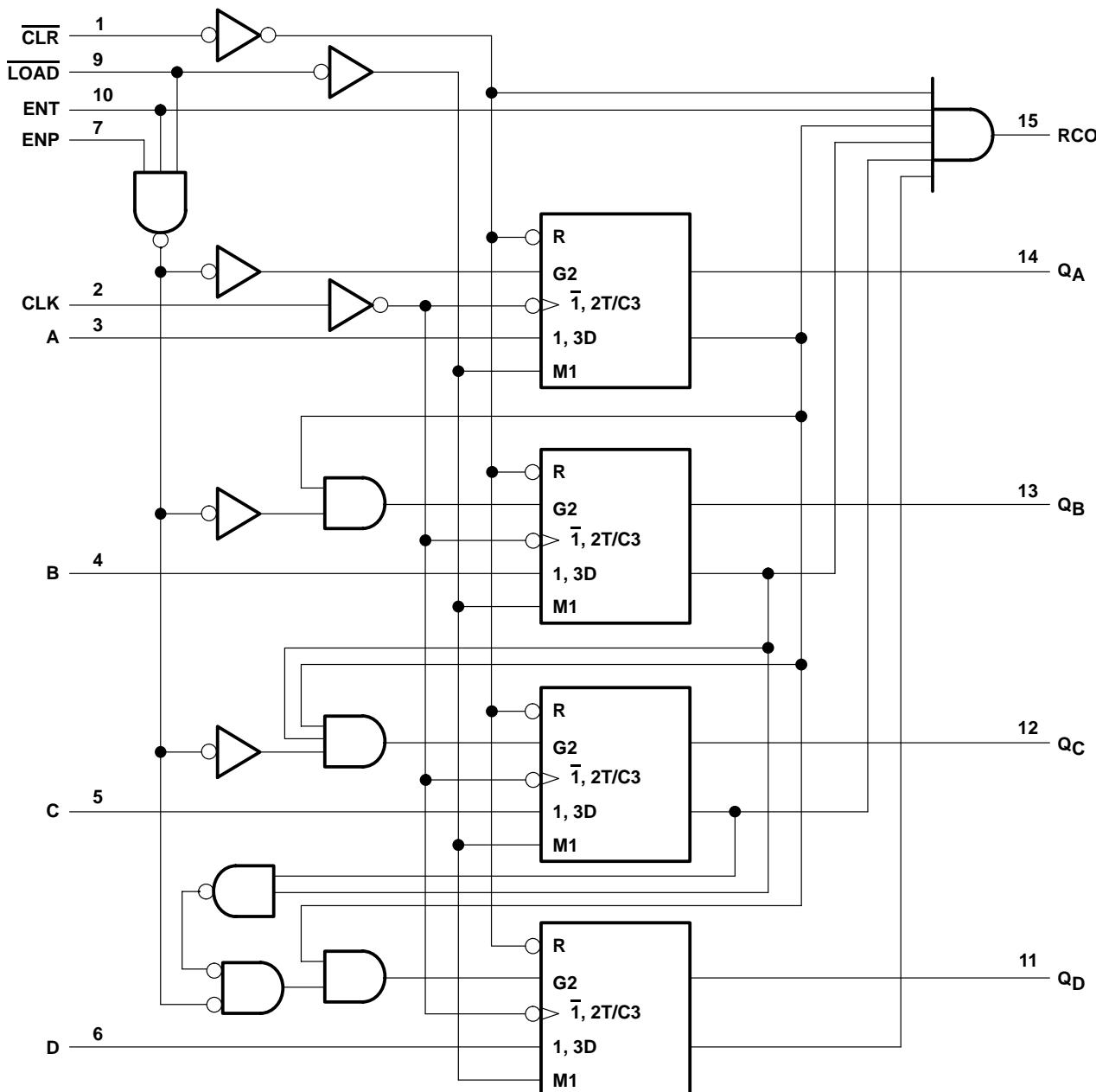
logic symbol, each flip-flop
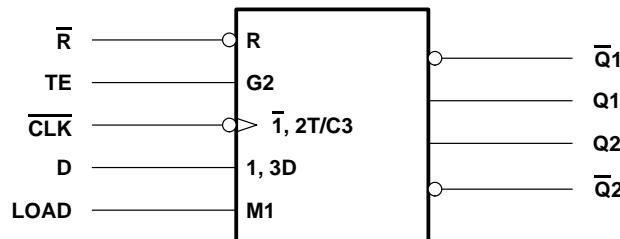
logic diagram, each flip-flop (positive logic)
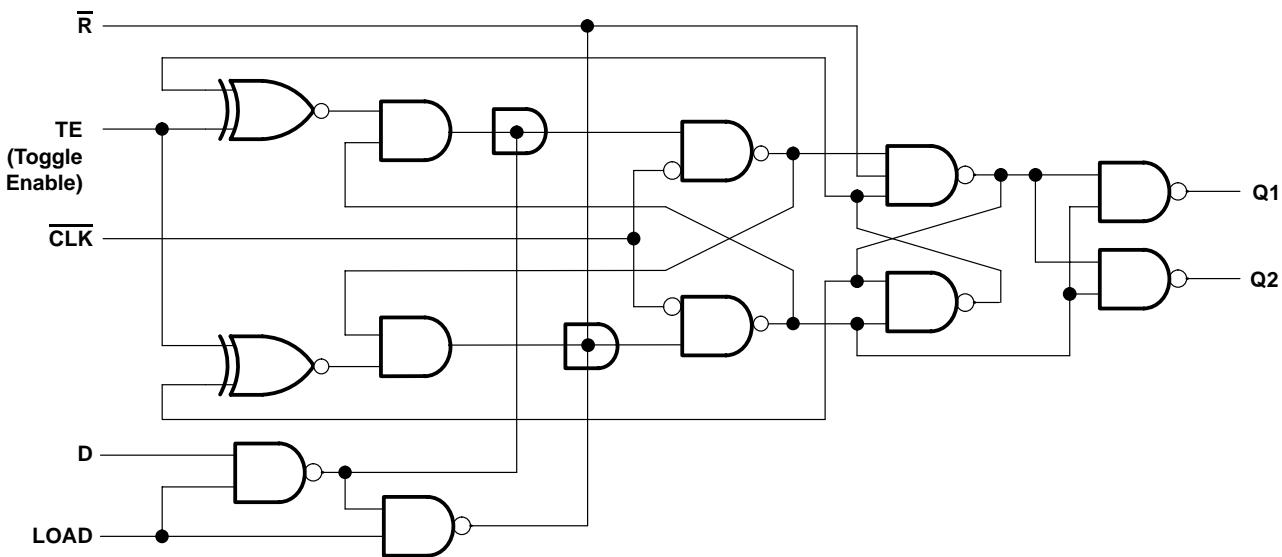
typical clear, preset, count, and inhibit sequences

The following timing sequence is illustrated below:

1. Clear outputs to zero

2. Preset to binary 12

3. Count to 13, 14, 15, 0, 1, and 2

4. Inhibit
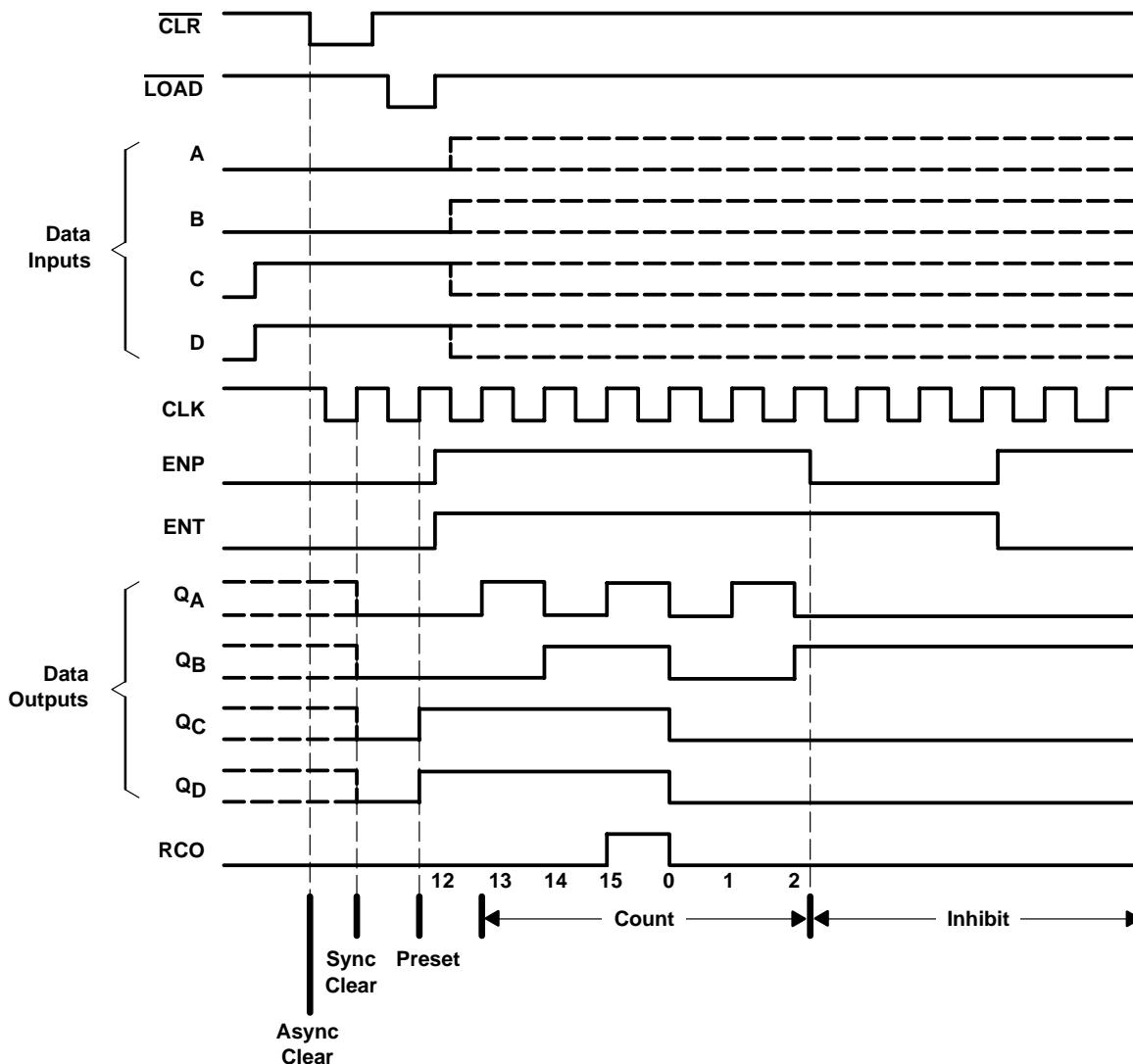
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −1.2 V to 7 V
Input current range .... −30 mA to 5 mA
Voltage range applied to any output in the high state .... −0.5 V to V_{CC}
Current into any output in the low state .... 40 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 73°C/W
DB package .... 82°C/W
N package .... 67°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[‡]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −1 mA	2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	ENP, CLK, A, B, C, D	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6	mA
	ENT, $\overline{LOAD}$					−1.2	
	CLR					−0.6	
I_{OS}[§]		V_{CC} = 5.5 V,	V_O = 0	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V			37	55	mA

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
f_{clock}	Clock frequency			0	100	0	90	MHz
t_w	Pulse duration	CLK high or low (loading)		5		5		ns
		CLK (counting)	High	4		4		
			Low	6		7		
		$\overline{CLR}$ low		5		5		
t_{su}	Setup time	Data before CLK↑	High or low	5		5		ns
		$\overline{LOAD}$ before CLK↑	High	11		11.5		
			Low	8.5		9.5		
		ENP and ENT before CLK↑	High	11		11.5		
			Low	5		5		
t_h	Hold time	Data after CLK↑	High or low	2		2		ns
		LOAD after CLK↑	High	2		2		
			Low	0		0		
		ENP and ENT after CLK↑	High or low	0		0		
t_{su}	Inactive-state setup time, $\overline{CLR}$ high before CLK↑†			6		6		ns

† Inactive-state setup time also is referred to as recovery time.

switching characteristics (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 PF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V TO 5.5 V, C_L = 50 PF, R_L = 500 Ω, T_A = MIN TO MAX‡		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			100	120		90		MHz
t_{PLH}	CLK ($\overline{LOAD}$ high)	Any Q	2.7	5.1	7.5	2.7	8.5	ns
t_{PHL}			2.7	7.1	10	2.7	11	
t_{PLH}	CLK ($\overline{LOAD}$ low)	Any Q	3.2	5.6	8.5	3.2	9.5	ns
t_{PHL}			3.2	5.6	8.5	3.2	9.5	
t_{PLH}	CLK	RCO	4.2	9.6	14	4.2	15	ns
t_{PHL}			4.2	9.6	14	4.2	15	
t_{PLH}	ENT	RCO	1.7	4.1	7.5	1.7	8.5	ns
t_{PHL}			1.7	4.1	7.5	1.7	8.5	
t_{PHL}	CLR	Any Q	4.7	8.6	12	4.7	13	ns
		RCO	3.7	7.6	10.5	3.7	11.5	

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 4:   Load circuits and waveforms are shown in Figure 1.

TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
Open Collector	7 V

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
  B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
    Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, duty cycle = 50%.
  D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS
INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74F161AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F161A	Samples
SN74F161ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F161A	Samples
SN74F161AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74F161AN	Samples
SN74F161ANE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74F161AN	Samples
SN74F161ANSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F161A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
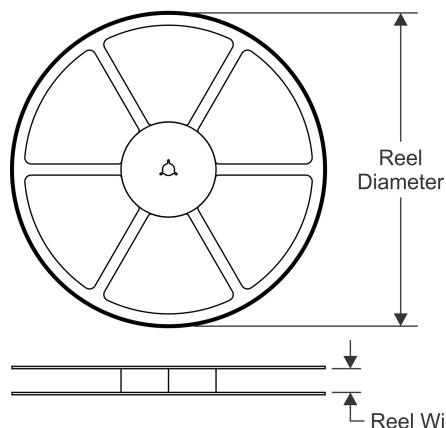
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
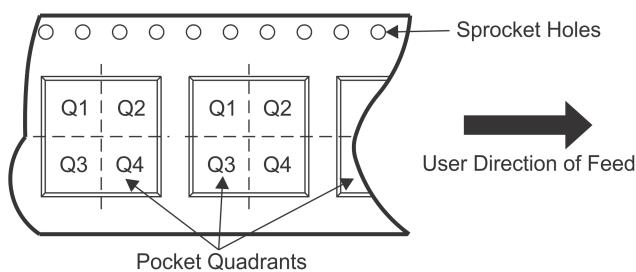
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F161ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74F161ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F161ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74F161ANSR	SO	NS	16	2000	853.0	449.0	35.0

PACKAGE MATERIALS INFORMATION

TUBE
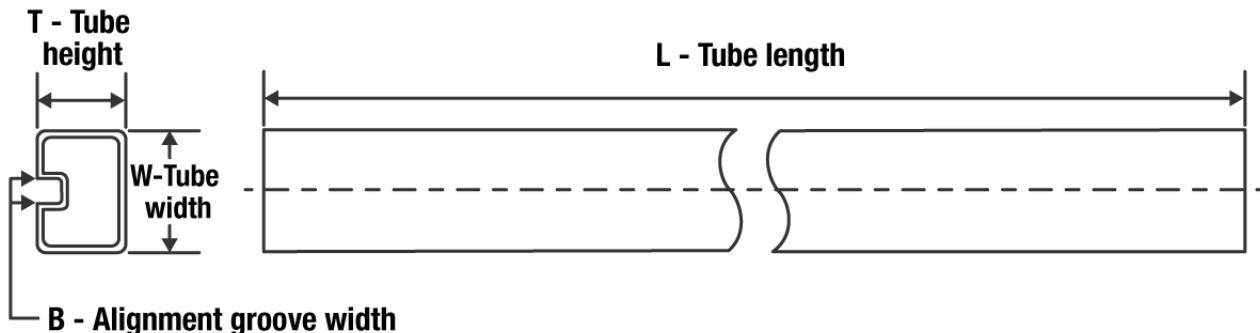
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74F161AD	D	SOIC	16	40	507	8	3940	4.32
SN74F161AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74F161AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74F161ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74F161ANE4	N	PDIP	16	25	506	13.97	11230	4.32

C

SEATING PLANE

0.1 C

8.2
7.4 TYP

A

PIN 1 ID
AREA

14X 1.27

1

16

10.4
10.0
NOTE 3

2X
8.89

8

9

16X 0.51
0.35

B

5.4
5.2
NOTE 4

⌖ 0.25Ⓜ C A B

2.00 MAX

SEE DETAIL A

0.15 TYP

0.25

GAGE PLANE

0.3
0.1

0° - 10°

1.05
0.55

(1.25)

DETAIL A
TYPICAL

4220735/A   12/2021
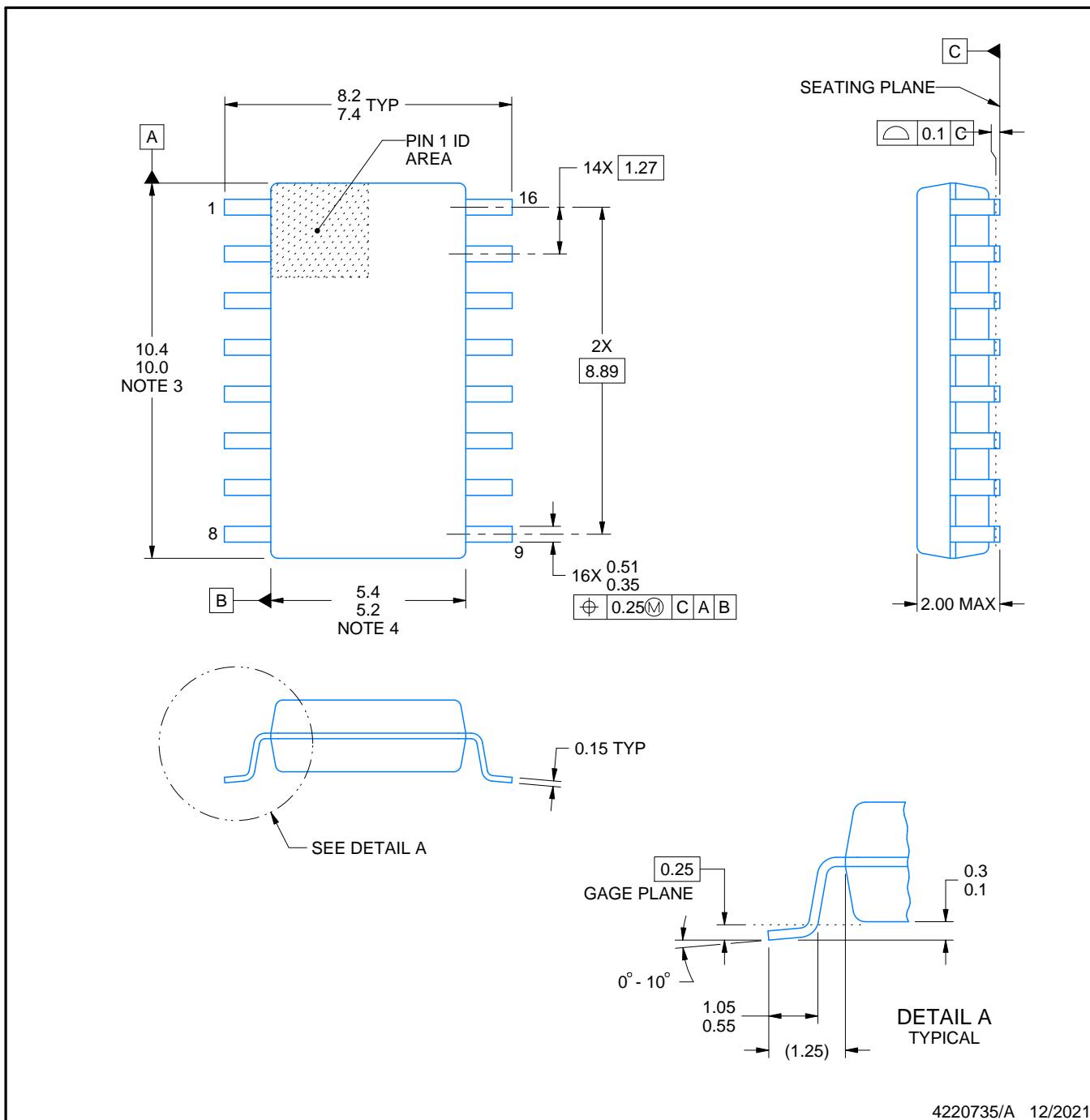
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

16X (1.85)

SYMM

SEE DETAILS

1

16

16X (0.6)

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)
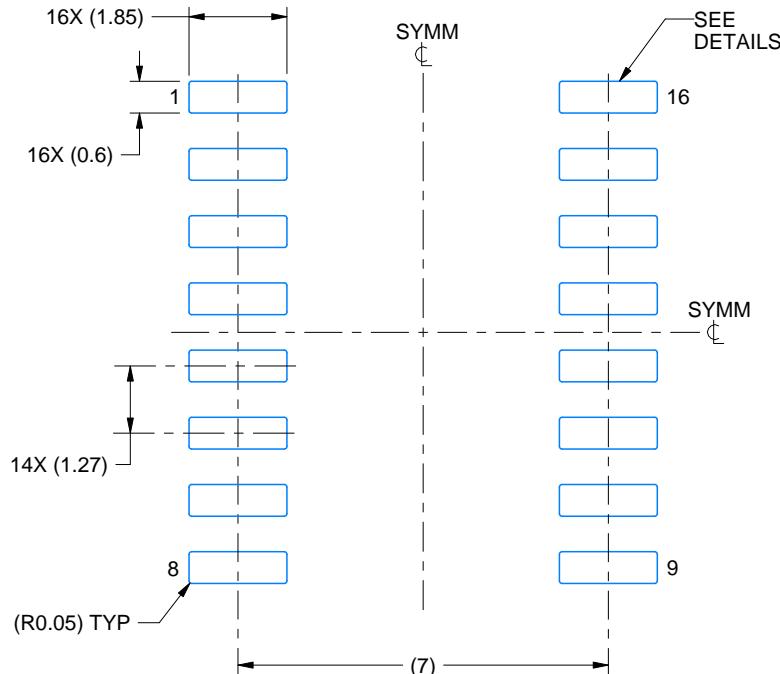
LAND PATTERN EXAMPLE
SCALE:7X

METAL

SOLDER MASK OPENING

SOLDER MASK OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
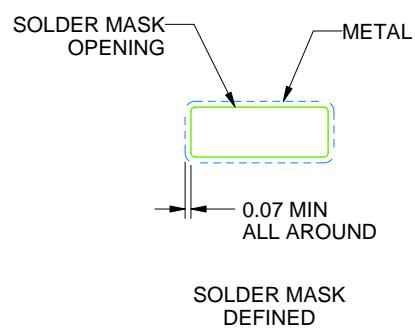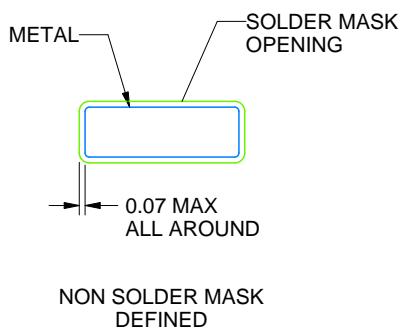
SOLDER MASK DETAILS

4220735/A   12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.85)

SYMM

1

16X (0.6)

16

14X (1.27)

SYMM

8

9

(R0.05) TYP

(7)
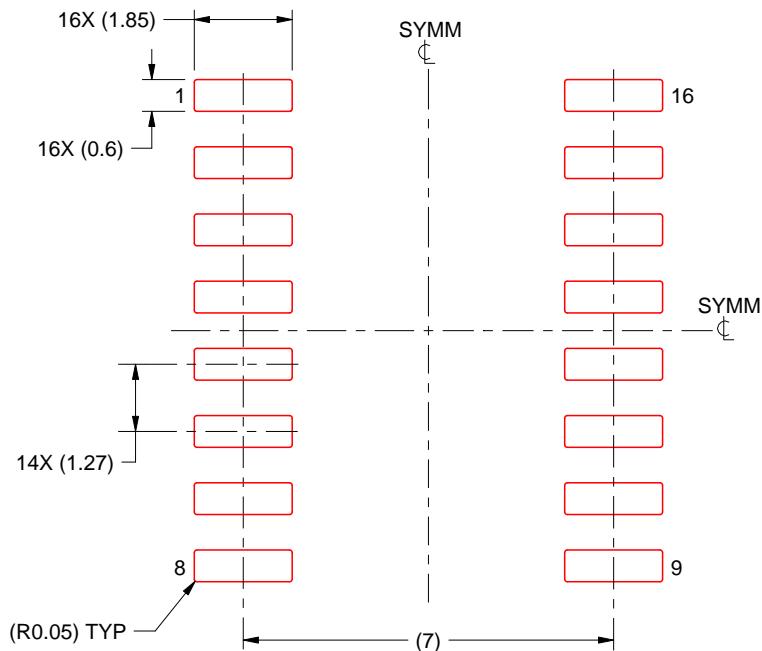
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A   12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE
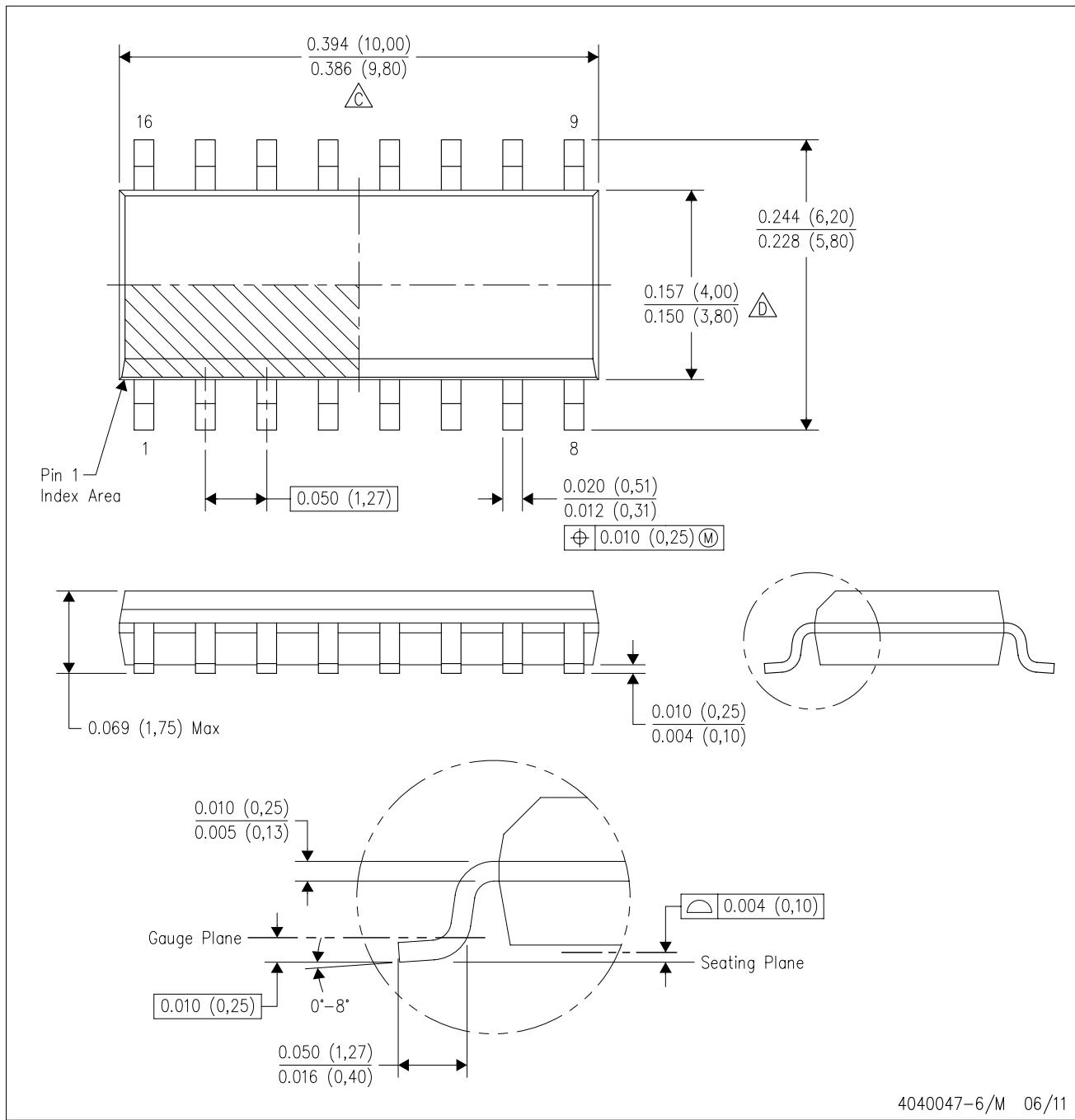
0.394 (10,00)
0.386 (9,80)
/C\

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   /D\

1   8

Pin 1
Index Area

0.050 (1,27)   0.020 (0,51)
                          0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

△ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
      /C\ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
          not exceed 0.006 (0,15) each side.
      /D\ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E. Reference JEDEC MS−012 variation AC.

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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

14x1,27

16x0,55

16x1,50

14x1,27

5,40

5.40
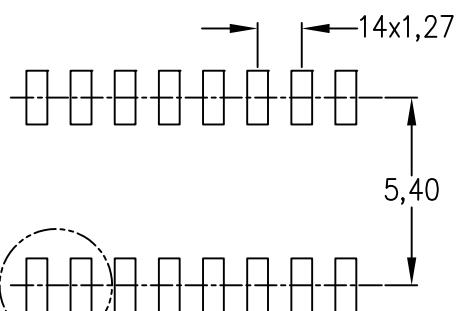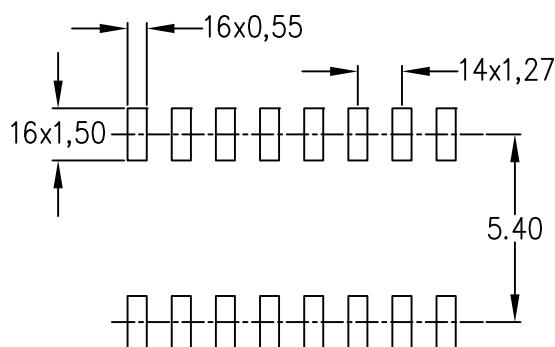
Example
Non Soldermask Defined Pad
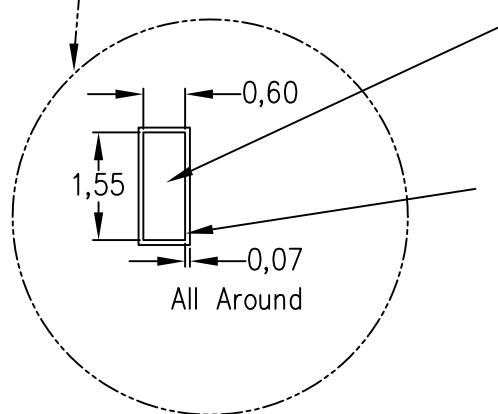
Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−4/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

	PINS **	14	16	20	24
DIM					
A MAX		10,50	10,50	12,90	15,30
A MIN		9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE
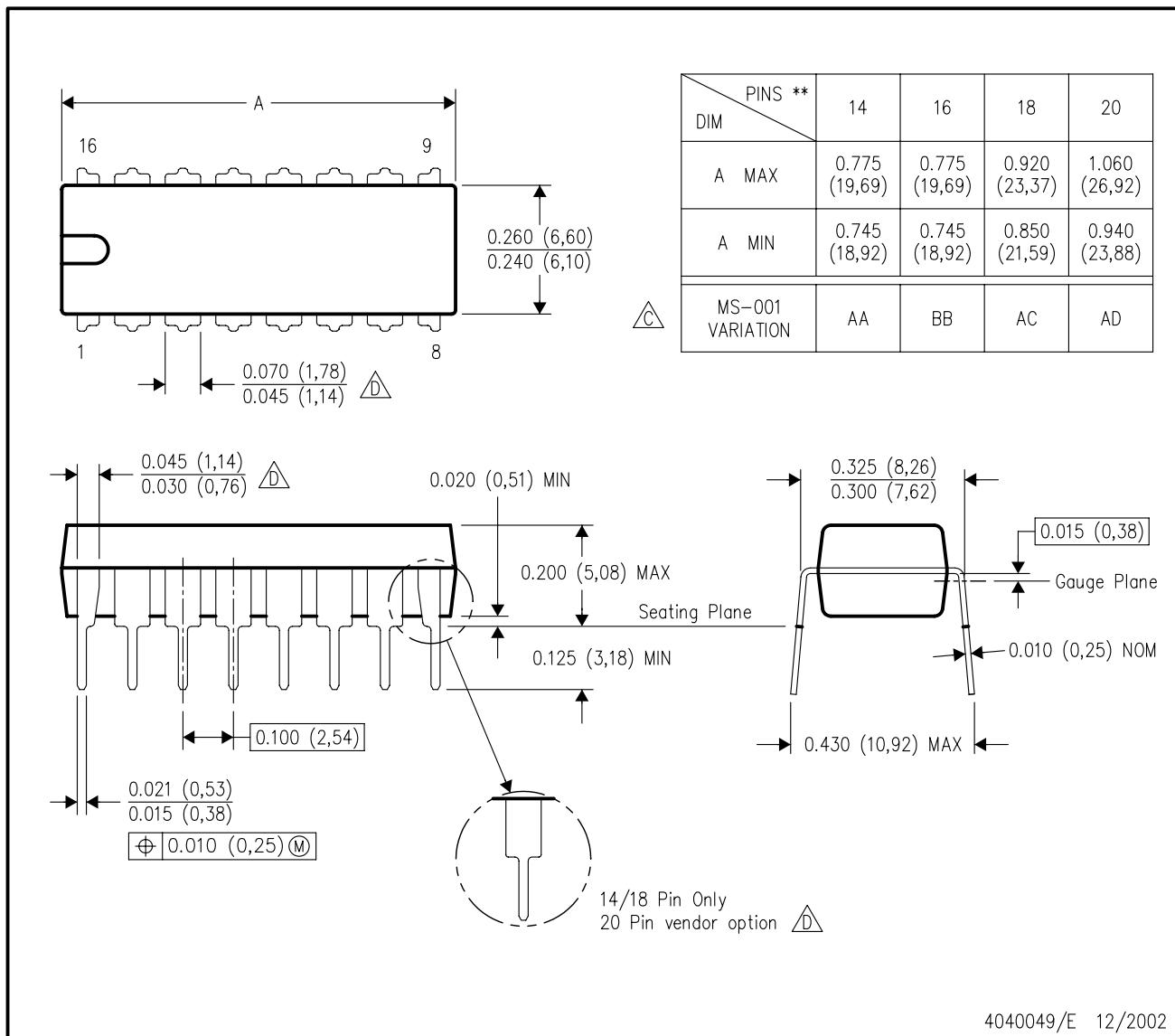
16 PINS SHOWN

	PINS **	14	16	18	20
DIM					
A MAX		0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN		0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION		AA	BB	AC	AD

A

16   9

0.260 (6,60) / 0.240 (6,10)

1   8

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

0.200 (5,08) MAX

Gauge Plane

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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