DS91M047 125 MHz Quad M-LVDS Line Driver

Check for Samples: DS91M047

FEATURES

- **DC - 125 MHz / 250 Mbps Low Jitter, Low Skew, Low Power Operation**
- **Conforms to TIA/EIA-899 M-LVDS Standard**
- **Controlled Transition Times (2 ns typ) Minimize Reflections**
- **8 kV ESD on M-LVDS Pins Protects Adjoining Components**
- **Flow-Through Pinout Simplifies PCB Layout**
- **Industrial Operating Temperature Range (−40°C to +85°C)**
- **Available in a Space Saving SOIC-16 Package**

APPLICATIONS

- **Multidrop / Multipoint Clock and Data Distribution**
- **High-Speed, Low Power, Short-Reach Alternative to TIA/EIA-485/422**
- **Clock Distribution in AdvancedTCA (ATCA) and MicroTCA (µTCA, uTCA) Backplanes**

DESCRIPTION

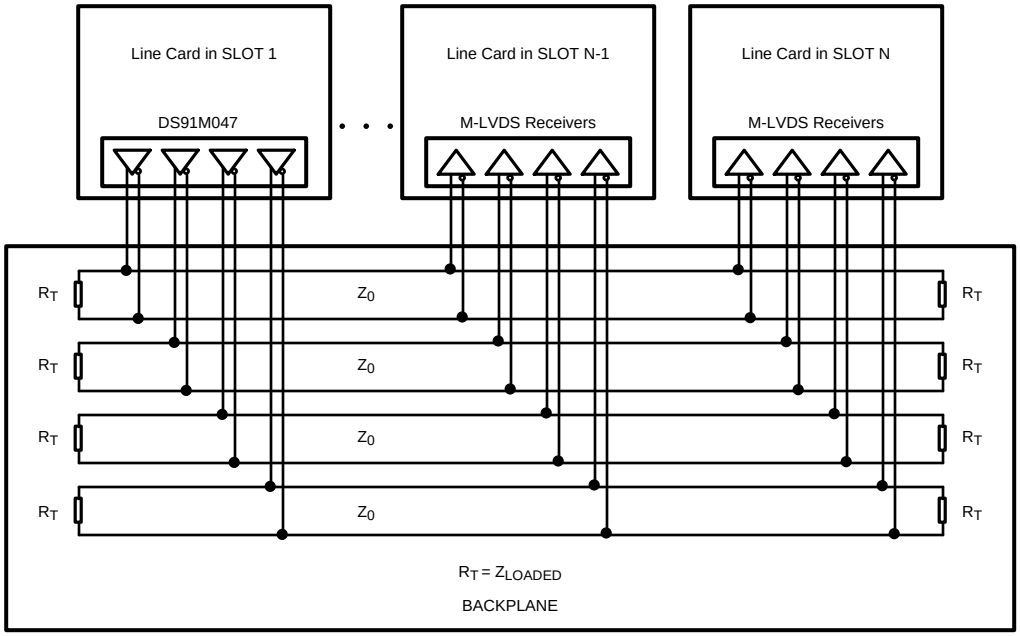
The DS91M047 is a high-speed quad M-LVDS line driver designed for driving clock or data signals to up to four multipoint networks.

M-LVDS (Multipoint LVDS) is a new family of bus interface devices based on LVDS technology specifically designed for multipoint and multidrop cable and backplane applications. It differs from standard LVDS in providing increased drive current to handle double terminations that are required in multi-point applications. Controlled transition times minimize reflections that are common in multipoint configurations due to unterminated stubs.

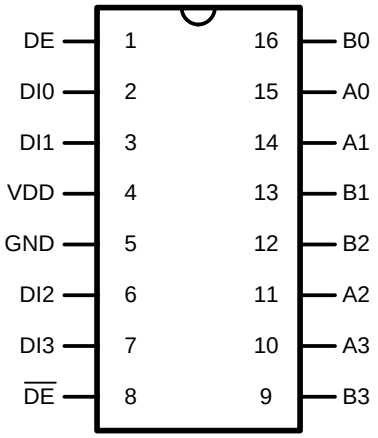
The DS91M047 accepts LVTTL/LVCMOS input levels and translates them to M-LVDS signal levels with transition times of greater than 1 ns. The device provides the DE and $\overline{DE}$ inputs that are ANDed together and control the TRI-STATE outputs. The DE and $\overline{DE}$ inputs are common to all four drivers.

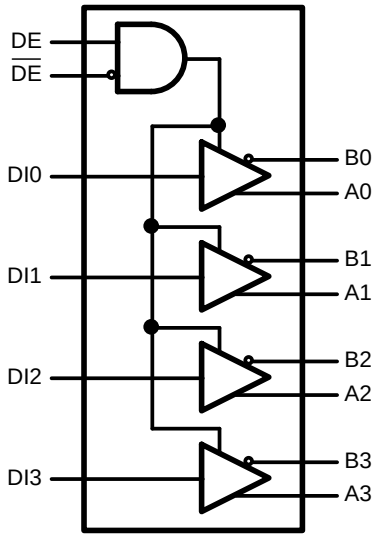
The DS91M047 has a flow-through pinout for easy PCB layout. The DS91M047 provides a new alternative for high speed multipoint interface applications. It is packaged in a space saving SOIC-16 package.

TYPICAL APPLICATION



Connection Diagrams





PIN DESCRIPTIONS

Pin No.	Name	Description
2, 3, 6, 7	DI	Driver input pin, LVCMOS compatible.
10, 11, 14, 15	A	Non-inverting driver output pin, M-LVDS levels.
9, 12, 13, 16	B	Inverting driver output pin, M-LVDS levels.
1	DE	Driver enable pin: When DE is low, the driver is disabled. When DE is high and $\overline{DE}$ is low or open, the driver is enabled. If both DE and $\overline{DE}$ are open circuit, then the driver is disabled.
8	$\overline{DE}$	Driver enable pin: When $\overline{DE}$ is high, the driver is disabled. When $\overline{DE}$ is low or open and DE is high, the driver is enabled. If both DE and $\overline{DE}$ are open circuit, then the driver is disabled.
4	V_{DD}	Power supply pin, +3.3V ± 0.3V
5	GND	Ground pin

TRUTH TABLE

Enables		Input	Outputs	
DE	$\overline{DE}$	DI	A	B
H	L	L	L	H
		H	H	L
All other combinations of ENABLE inputs		X	Z	Z

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Power Supply Voltage		−0.3V to +4V
LVCMOS Input Voltage		−0.3V to (V_{DD} + 0.3V)
M-LVDS Output Voltage		−1.9V to +5.5V
M-LVDS Output Short Circuit Current Duration		Continuous
Junction Temperature		+140°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature Range	Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation @ +25°C	D Package	2.21W
	Derate D Package	19.2 mW/°C above +25°C
Package Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	θ_{JA}	+52°C/W
	θ_{JC}	+19°C/W
ESD Susceptibility	HBM	≥8 kV
	MM	≥250V
	CDM	≥1250V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

	Min	Typ	Max	Units
Supply Voltage (VDD)	+3.0	+3.3	+3.6	V
Voltage at Any Bus Terminal (Separate or Common-Mode)	−1.4		+3.8	V
High Level Input Voltage (V_{IH})	2.0		V_{DD}	V
Low Level Input Voltage (V_{IL})	0		0.8	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

DC ELECTRICAL CHARACTERISTICS[1][2][3][4]

Over supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS DC Specifications						
V_{IH}	High-Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low-Level Input Voltage		GND		0.8	V
I_{IH}	High-Level Input Current	V_{IH} = 3.6V	-15	±1	15	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0V	-15	±1	15	µA
V_{CL}	Input Clamp Voltage	I_{IN} = -18 mA	-1.5			V
M-LVDS DC Specifications						
$\|V_{AB}\|$	Differential Output Voltage Magnitude	R_L = 50Ω, C_L = 5 pF See Figure 1 and Figure 3	480		650	mV
ΔV_{AB}	Change in Differential Output Voltage Magnitude Between Logic States		−50		50	mV
$V_{OS(SS)}$	Steady-State Common-Mode Output Voltage	R_L = 50Ω See Figure 1 and Figure 2	0.30	1.6	2.10	V
$\|\Delta V_{OS(SS)}\|$	Change in Steady-State Common-Mode Output Voltage Between Logic States		0		50	mV
$V_{A(OC)}$	Maximum Steady-State Open-Circuit Output Voltage	See Figure 4	0		2.4	V
$V_{B(OC)}$	Maximum Steady-State Open-Circuit Output Voltage		0		2.4	V
$V_{P(H)}$	Voltage Overshoot, Low-to-High Level Output[5]	R_L = 50Ω, C_L = 5 pF C_D = 0.5 pF, see Figure 6 and Figure 7			$1.2V_{SS}$	V
$V_{P(L)}$	Voltage Overshoot, High-to-Low Level Output[5]		$-0.2V_{SS}$			V
I_{OS}	Output Short-Circuit Current[6]	See Figure 5	-43		43	mA
I_A	Driver High-Impedance Output Current	V_A = 3.8V, V_B = 1.2V	0		32	µA
		V_A = 0V or 2.4V, V_B = 1.2V	−20		20	µA
		V_A = −1.4V, V_B = 1.2V	−32		0	µA
I_B	Driver High-Impedance Output Current	V_A = 3.8V, V_B = 1.2V	0		32	µA
		V_A = 0V or 2.4V, V_B = 1.2V	−20		20	µA
		V_A = −1.4V, V_B = 1.2V	−32		0	µA
I_{AB}	Driver High-Impedance Output Differential Curent (I_A − I_B)	V_A = V_B, −1.4V ≤ V ≤ 3.8V	−4		4	µA
$I_{A(OFF)}$	Driver High-Impedance Output Power-Off Current	V_A = 3.8V, V_B = 1.2V DE = 0V 0V ≤ V_{DD} ≤ 1.5V	0		32	µA
		V_A = 0V or 2.4V, V_B = 1.2V DE = 0V 0V ≤ V_{DD} ≤ 1.5V	−20		20	µA
		V_A = −1.4V, V_B = 1.2V DE = 0V 0V ≤ V_{DD} ≤ 1.5V	−32		0	µA
$I_{B(OFF)}$	Driver High-Impedance Output Power-Off Current	V_A = 3.8V, V_B = 1.2V DE = 0V 0V ≤ V_{DD} ≤ 1.5V	0		32	µA
		V_A = 0V or 2.4V, V_B = 1.2V DE = 0V 0V ≤ V_{DD} ≤ 1.5V	−20		20	µA
		V_A = −1.4V, V_B = 1.2V DE = 0V 0V ≤ V_{DD} ≤ 1.5V	−32		0	µA

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
(3) Typical values represent most likely parametric norms for V_{DD} = +3.3V and T_A = +25°C, and at the Recommended Operating Conditions at the time of product characterization and are not ensured.
(4) C_L includes fixture capacitance and C_D includes probe capacitance.
(5) Specification is specified by characterization and is not tested in production.
(6) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

DC ELECTRICAL CHARACTERISTICS[1][2][3][4] (continued)

Over supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{AB(OFF)}$	Driver High-Impedance Output Power-Off Current ($I_{A(OFF)}$ − $I_{B(OFF)}$)	$V_A = V_B$, −1.4V ≤ V ≤ 3.8V DE = 0V 0V ≤ V_{DD} ≤ 1.5V	−4		4	µA
C_A	Driver Output Capacitance	V_{DD} = 0V		7.8		pF
C_B	Driver Output Capacitance			7.8		pF
C_{AB}	Driver Output Differential Capacitance			3		pF
$C_{A/B}$	Driver Output Capacitance Balance (C_A/C_B)			1		
I_{CC}	Power Supply Current	R_L = 50Ω (All Outputs) DI = V_{DD} or GND (All Inputs) DE = V_{DD}, $\overline{DE}$ = GND f = 125 MHz		65	75	mA
I_{CCZ}	TRI-STATE Power Supply Current	R_L = 50Ω (All Outputs) DI = V_{DD} or GND (All Inputs) DE = GND, $\overline{DE}$ = V_{DD}		19	24	mA

SWITCHING CHARACTERISTICS[1][2][3]

Over supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Differential Propagation Delay High to Low	R_L = 50Ω C_L = 5 pF, C_D = 0.5 pF See Figure 6 and Figure 7	1.5	3.1	5.0	ns
t_{PLH}	Differential Propagation Delay Low to High		1.5	3.1	5.0	ns
t_{SKD1}	Differential Pulse Skew $\lvert t_{PHL} - t_{PLH} \rvert$[4][5]		0	70	140	ps
t_{SKD2}	Channel-to-Channel Skew[4][6]		0	70	200	ps
t_{SKD3}	Differential Part-to-Part Skew[4][7] (Constant T_A and V_{DD})		0	0.8	1.5	ns
t_{SKD4}	Differential Part-to-Part Skew[8]		0		3.5	ns
t_{TLH}	Rise Time[4]		1.1	2.0	3.0	ns
t_{THL}	Fall Time[4]		1.1	2.0	3.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 50Ω C_L = 5 pF, C_D = 0.5 pF See Figure 8 and Figure 9		7	12.5	ns
t_{PLZ}	Disable Time Low to Z			7	12.5	ns
t_{PZH}	Enable Time Z to High			7	12.5	ns
t_{PZL}	Enable Time Z to Low			7	12.5	ns
f_{MAX}	Maximum Operating Frequency	See[4]	125			MHz

(1) The Electrical Characteristics list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms for V_{DD} = +3.3V and T_A = +25°C, and at the Recommended Operating Conditions at the time of product characterization and are not ensured.
(3) C_L includes fixture capacitance and C_D includes probe capacitance.
(4) Specification is specified by characterization and is not tested in production.
(5) t_{SKD1}, $\lvert t_{PLHD} - t_{PHLD} \rvert$, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(6) t_{SKD2}, Channel-to-Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels.
(7) t_{SKD3}, Part-to-Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.
(8) t_{SKD4}, Part-to-Part Skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.

PARAMETER MEASUREMENT INFORMATION

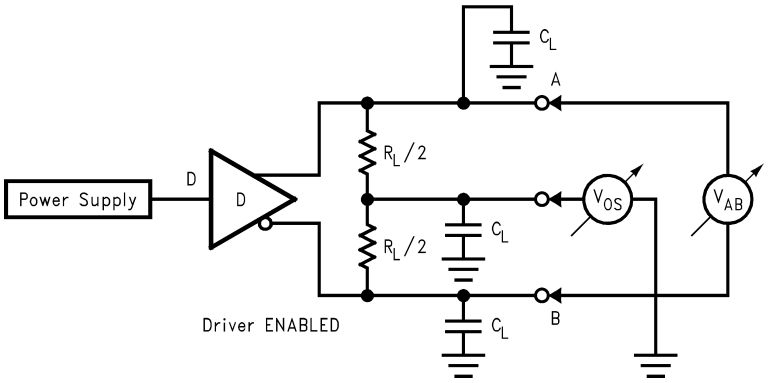


Figure 1. Differential Driver Test Circuit

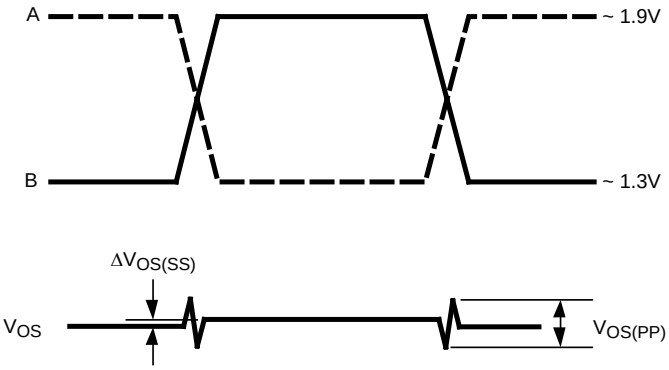


Figure 2. Differential Driver Waveforms

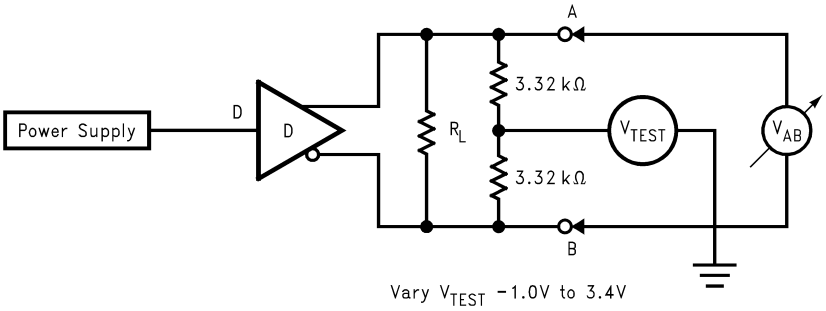


Figure 3. Differential Driver Full Load Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

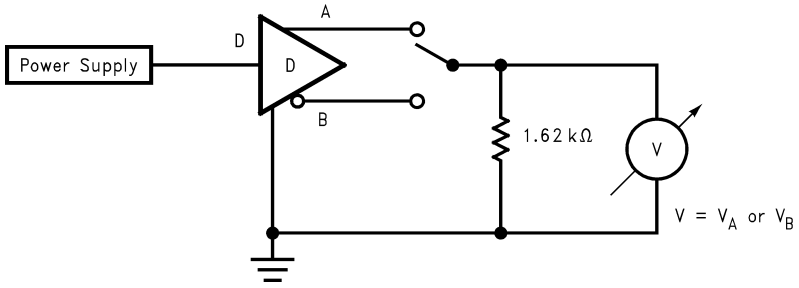


Figure 4. Differential Driver DC Open Test Circuit

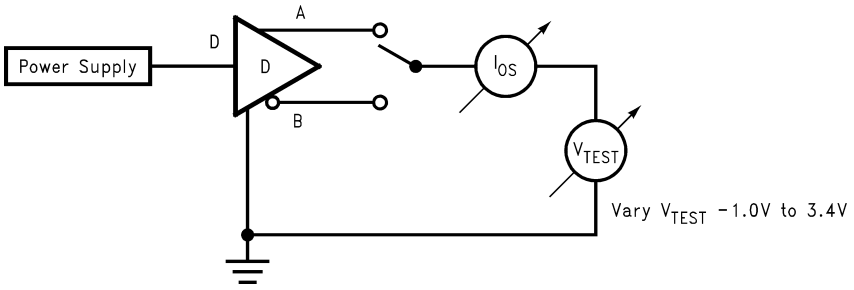


Figure 5. Differential Driver Short-Circuit Test Circuit

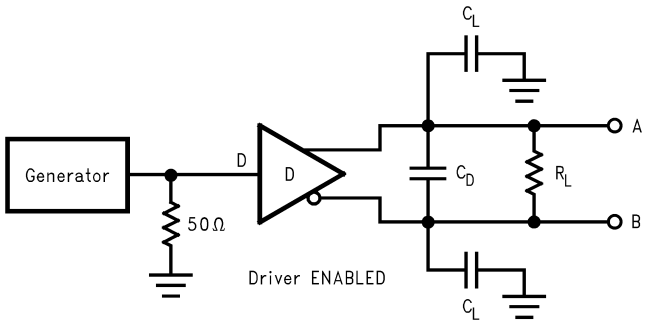


Figure 6. Driver Propagation Delay and Transition Time Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

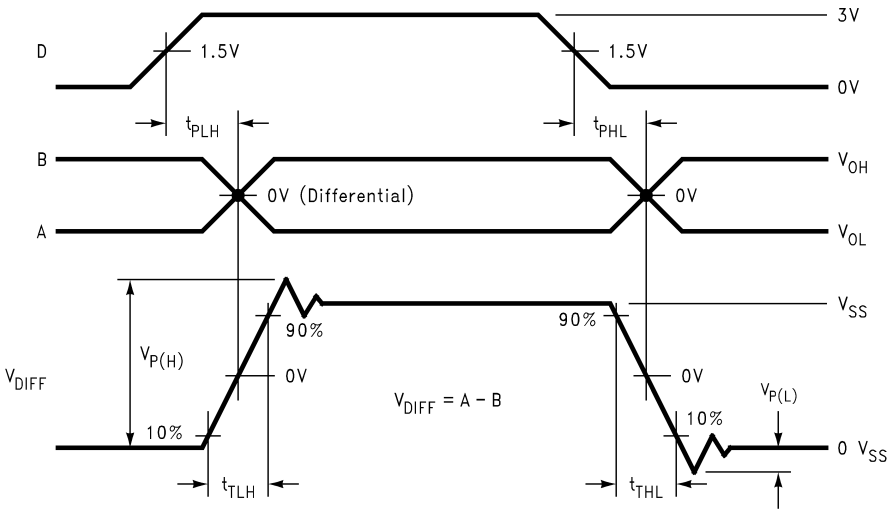


Figure 7. Driver Propagation Delay and Transition Time Waveforms

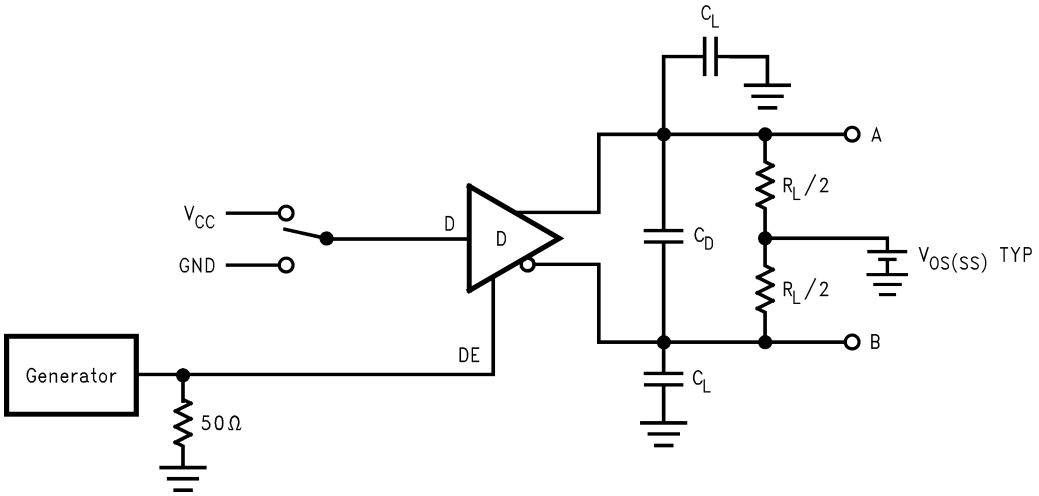


Figure 8. Driver TRI-STATE Delay Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

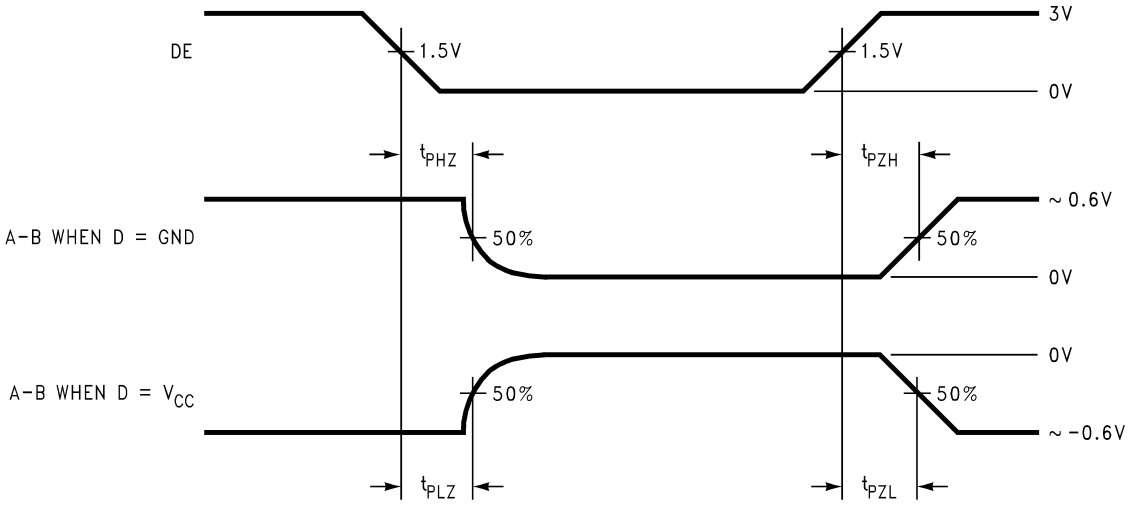


Figure 9. Driver TRI-STATE Delay Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS

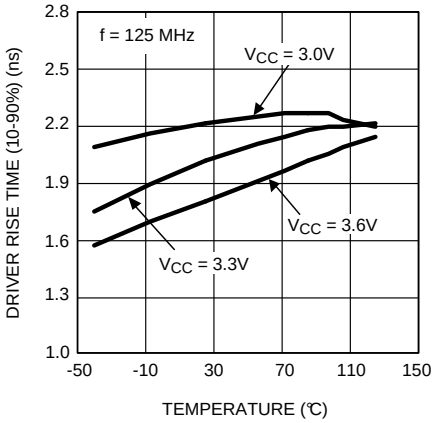


Figure 10. Driver Rise Time as a Function of Temperature

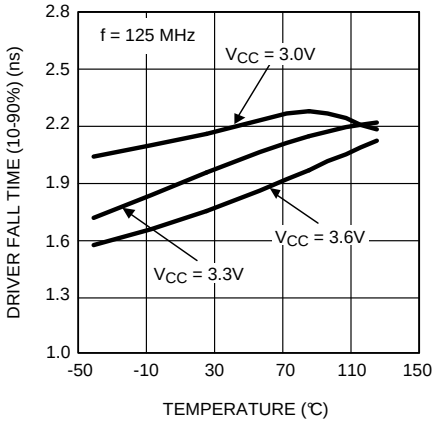


Figure 11. Driver Fall Time as a Function of Temperature

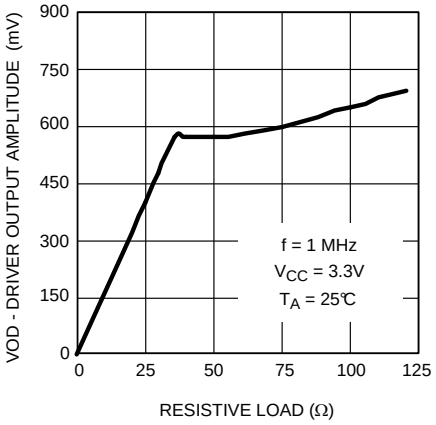


Figure 12. Driver Output Signal Amplitude as a Function of Resistive Load

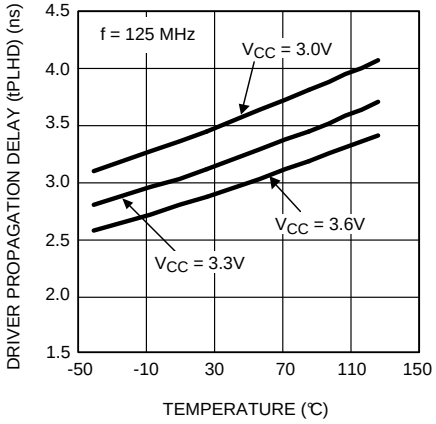


Figure 13. Driver Propagation Delay (tPLHD) as a Function of Temperature

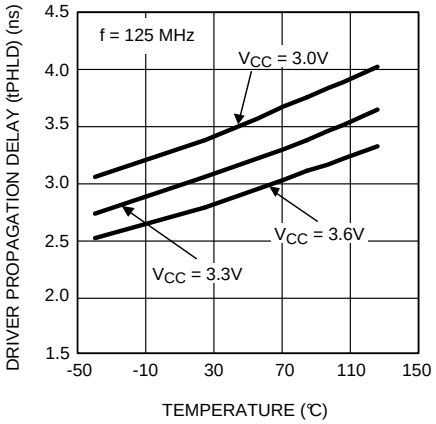


Figure 14. Driver Propagation Delay (tPHLD) as a Function of Temperature

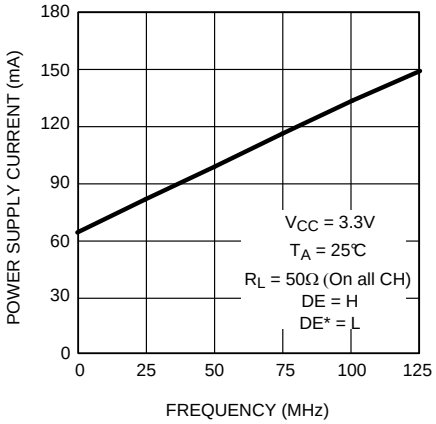


Figure 15. Driver Power Supply Current as a Function of Frequency

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS91M047TMA/NOPB	ACTIVE	SOIC	D	16	48	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DS91M047 TMA	Samples
DS91M047TMAX/NOPB	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DS91M047 TMA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

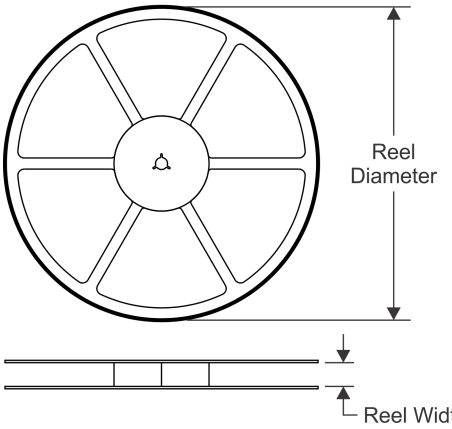
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

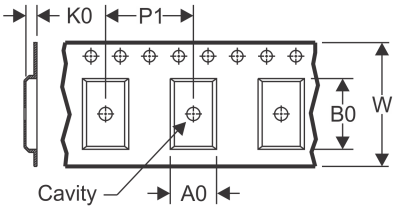
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

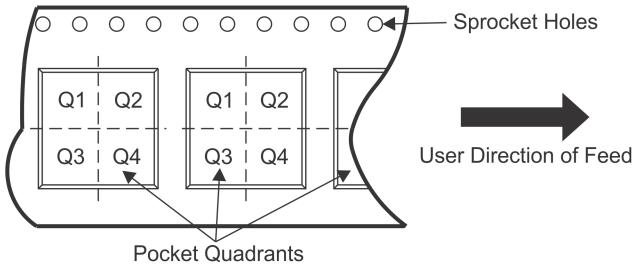


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

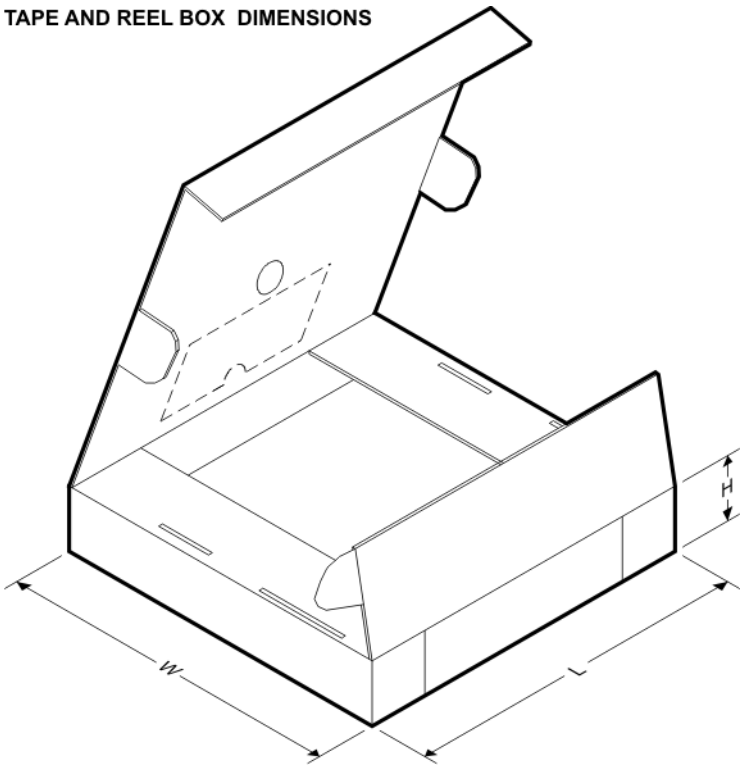
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS91M047TMAX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

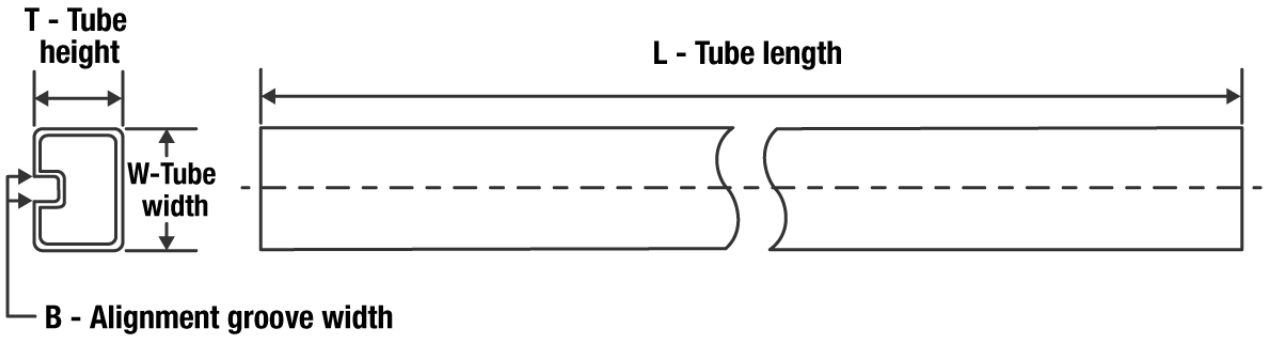
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS91M047TMAX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

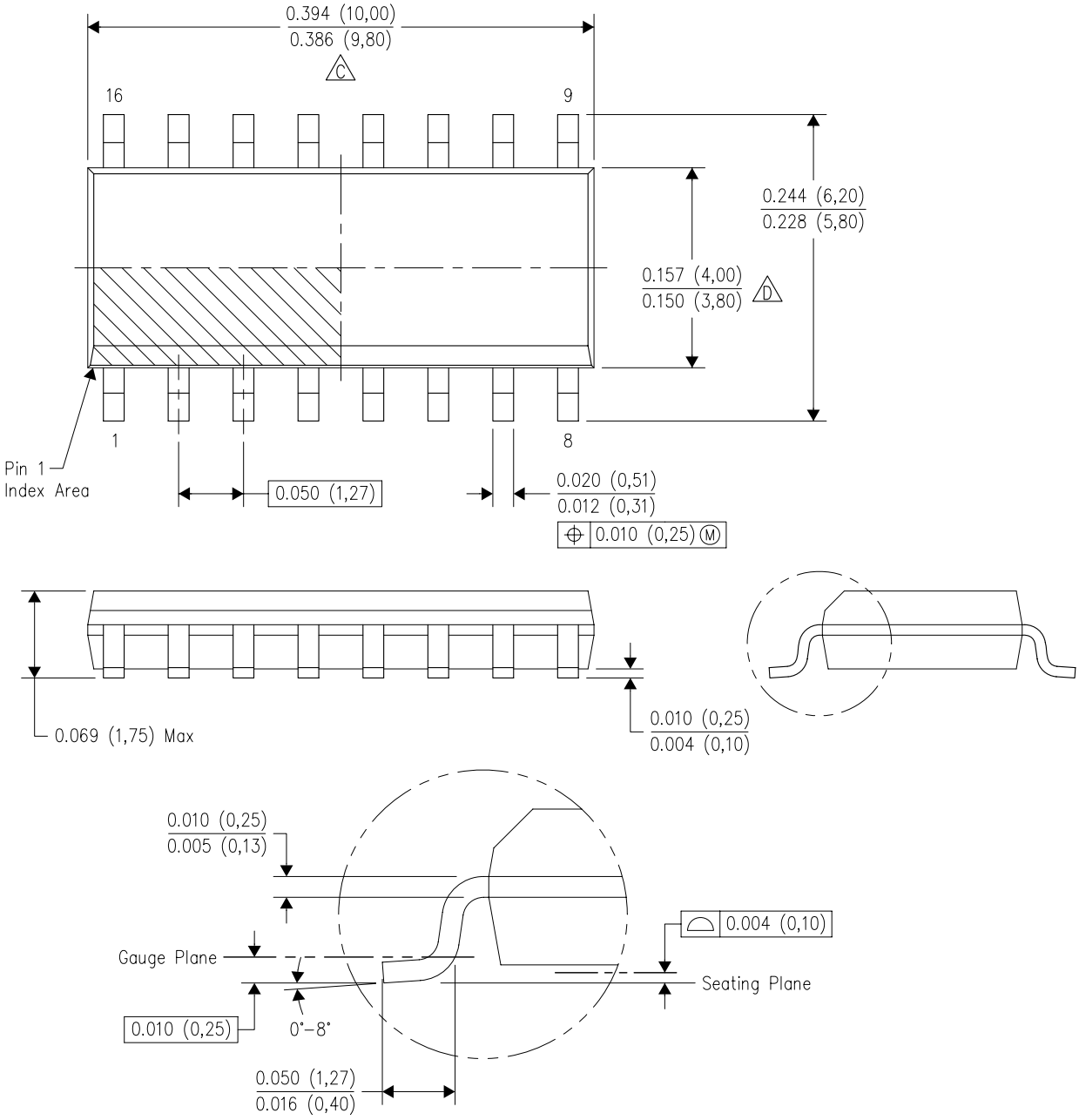
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS91M047TMA/NOPB	D	SOIC	16	48	495	8	4064	3.05

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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