INTEGRATED PHOTO FLASH CHARGER AND IGBT DRIVER

FEATURES

- **Wide Input Voltage**
  - **VBAT = 1.4 V to 12 V**
  - **VCC = 2.7 V to 5.5 V**
- **Integrated 50-V Power Switch With Lower R_{ON}**
- **Programmable Peak Current at Primary Side From 0.5 A to 2 A**
- **Optimized Switch ON/OFF Control for Fast Charging**
- **Charge Complete Detection at Primary Side With High Accuracy**
- **Integrated Insulated Gate Bipolar Transfer (IGBT) Driver**
- **3-mm × 3-mm, 16-Pin QFN Package**
- **Protection**
  - **Overcurrent Protection (OCP)**
  - **Thermal Shutdown (TSD)**

APPLICATIONS

- **Digital Still Cameras**
- **Optical Film Cameras**
- **Digital Video Camcorders**
- **Cell Phones**

DESCRIPTION/ORDERING INFORMATION

The TPS65563A offers a complete solution for a charging photo flash capacitor and flashing xenon tube with an insulated gate bipolar transfer (IGBT) driver. This device has an integrated voltage reference, power switch (SW), comparators for peak current detection/power SW turnon detection/charge complete detection, an IGBT driver, and control logics for charging applications/driving IGBT applications.

Compared with discrete solutions, this device reduces the component count, shrinks the total solution size, and erases the difficulty of design for xenon-tube applications.

Additional advantages are a fast charging time and high efficiency since this device has an optimized pulse width modulation (PWM) control algorithm for photo flash charging. In addition, this device has high accuracy for peak current detection and for charge completion detection. The distribution of charging time is smaller.

Other provisions of the device include sensing the output voltage at the primary side, programmable peak current at the primary side, protection features (thermal shutdown and overcurrent), an output pin for charge completion detection, and input pins for charge enable, flash acceptable, and flash on.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–35°C to 85°C	QFN	TPS65563ARGTT	CHS
		TPS65563ARGTR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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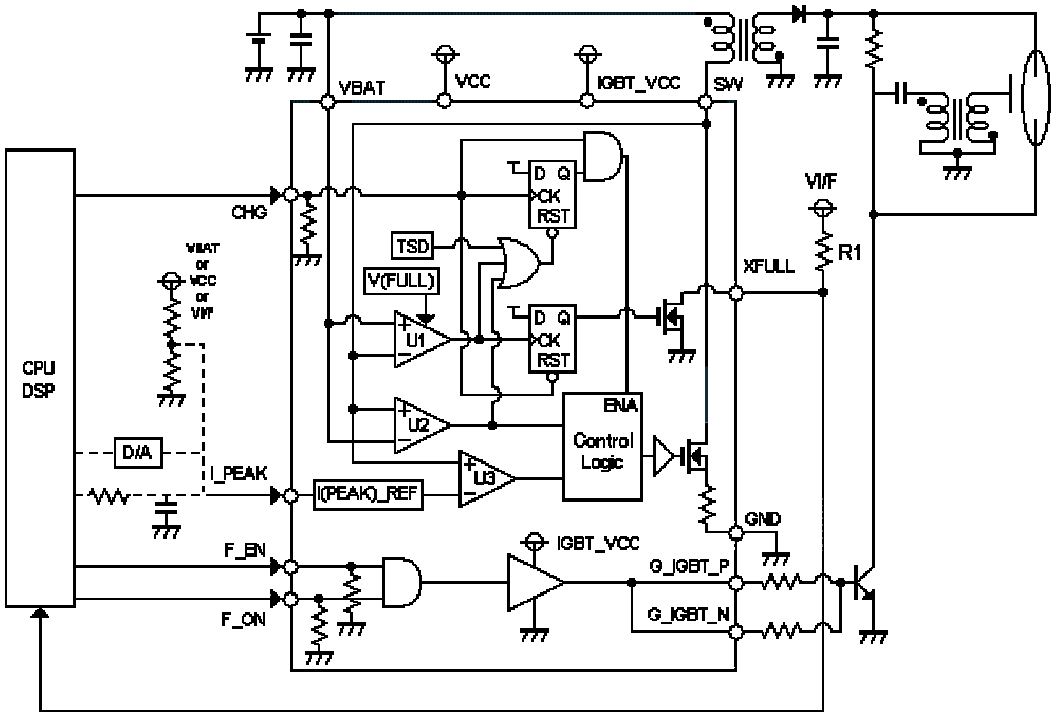


Figure 1. Application Circuit

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

				UNIT
	Supply voltage range	VCC, IGBT_VCC	–0.6 to 6	V
		VBAT	–0.6 to 13	
V_o	Output voltage range of XFULL		–0.6 to 6	V
V_{SW}	Switch terminal voltage range		–0.6 to 50	V
I_{SW}	Switch current between SW and GND		3	A
V_I	Input voltage range	CHG, I_PEAK, F_ON, F_EN	–0.3 to V_{CC}	V
T_{stg}	Storage temperature range		–40 to 150	°C
T_J	Maximum junction temperature		125	°C
ESD rating	Human Body Model (HBM) JES22-A114		1.5	kV

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
	Supply voltage	VCC, IGBT_VCC	2.7	5.5	V
		VBAT	1.4	12	
V_{SW}	Switch terminal voltage		–0.3	45	V
I_{SW}	Switch current between SW and GND			2.3	A
V_{IH}	High-level digital input voltage at CHG, F_ON, and F_EN		2.0		V
V_{IL}	Low-level digital input voltage at CHG, F_ON, and F_EN			0.6	V
	Operating free-air temperature		–35	85	°C

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$(1)	POWER RATINGS T_A < 25°C	POWER RATINGS RATE T_A = 85°C
QFN	47.4°C/W	2.11 W	0.844 W

(1) The thermal resistance, $R_{\theta JA}$, is based on a soldered PowerPAD™ package on a 2S2P JEDEC board using thermal vias.

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ELECTRICAL CHARACTERISTICS

T_A = 25°C, VBAT = 4.2 V, VCC = 3 V, IGBT_VCC = 3 V, V_{SW} = 4.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current from VBAT	CHG = VCC, F_ON = GND, F_EN = GND, XFULL = Hi-Z		140	200	µA
I_{CC2}	Supply current from VCC	CHG = VCC, F_ON = GND, F_EN = GND, XFULL = Hi-Z		2	3	mA
I_{CC3}	Supply current from IGBT_VCC	CHG = GND, F_ON = VCC, F_EN = VCC		14	20	µA
I_{CC4}	Supply current from VCC, IGBT_VCC, and VBAT	CHG = GND, F_ON = GND, F_EN = GND			1	µA
I_{LKG1_SW}	Leakage current of SW	V_{SW} = 4.2 V			2	µA
I_{LKG2_SW}	Leakage current of SW	V_{SW} = 45 V			500	µA
I_{sink}	Sink current at I_PEAK	VCC = V_{I_PEAK} = 3 V			0.1	µA
I_{PEAK1}	Lower point of I_{SW}	V_{I_PEAK} = 0.1V	0.42	0.62	0.82	A
I_{PEAK2}	Middle point of I_{SW}	V_{I_PEAK} = 0.65 V	1.1	1.3	1.5	A
I_{PEAK3}	Upper point of I_{SW}	V_{I_PEAK} = 1.5 V	1.8	2	2.2	A
R_{ON_XFULL}	ON resistance between XFULL and GND	I_{X_FULL} = 1 mA		1.5	3	kΩ
R_{ON_SW}	ON resistance between SW and GND	I_{SW} = 1 A, VCC = 3 V		0.4	0.7	Ω
$R_{G_IGBT_N}$	G_IGBT_N ON resistance	$I_{G_IGBT_N}$ = 100 mA	3	5	7.5	Ω
$R_{G_IGBT_P}$	G_IGBT_P ON resistance	$I_{G_IGBT_P}$ = 100 mA	3	5	7.5	Ω
R_{INPD}	Pulldown resistance of CHG, F_ON, and F_EN	V_{CHG}, V_{F_ON}, V_{F_EN} = 3 V		100		kΩ
T_{SD} (1)	Thermal shutdown detection temperature		140	150	160	°C
V_{FULL}	Charge completion detection voltage at SW		VBAT+28.6	VBAT+29	VBAT+29.4	V
V_{ZERO}	Zero current detection at SW		VBAT+10m	VBAT+25m	VBAT+40m	V
V_{OCP}	Overcurrent protection trigger voltage at SW		VBAT–150m	VBAT–100m	VBAT–50m	V

(1) Specified by design

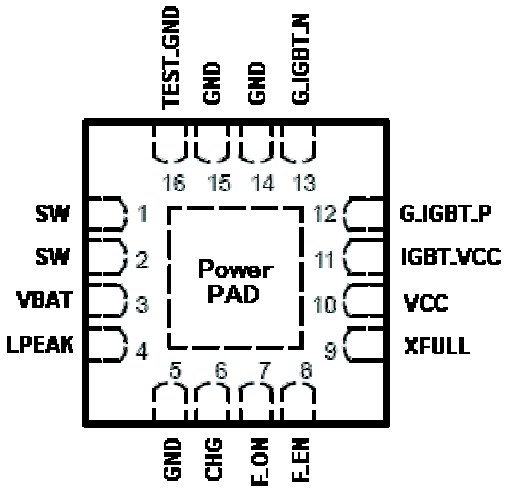
SWITCHING CHARACTERISTICS

T_A = 25°C, VBAT = 4.2 V, VCC and IGBT_VCC = 3 V, V_{SW} = 4.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD} (1)	Propagation delay	G_IGBT turns high/low after F_ON/F_EN turns high/low		25		ns
		SW OFF after I_{SW} exceeds the threshold defined by I_PEAK		75		
		XFULL turns low after V_{SW} exceeds V_{FULL}		200		
		SW ON after CHG turns high		50	150	µs

(1) Specified by design

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TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
1, 2	SW	O	Primary-side power MOSFET switch. Connect SW to the switched side of the transformer.
3	VBAT	I	Battery voltage monitor input for detecting OFF timing of power MOSFET. Connect VBAT to an input voltage from battery. The arrowable range is from 1.4 V to 12 V. Bypass VBAT to GND with a 10-µF ceramic capacitor as close to the IC as possible.
4	I_PEAK	I	Primary-side peak current control input. The voltage at I_PEAK sets the peak current into SW. See the *Programming Peak Current* section for details on selecting V_{I_PEAK}.
6	CHG	I	Charge enable/disable input. Drive CHG high to start charging the output capacitor. Drive CHG low to terminate charging.
7	F_ON	I	Flash enable/disable. High level is xenon flash on with F_EN being high. Low level is xenon flash off even if F_EN is high.
8	F_EN	I	Flash acceptable. High level is acceptable to xenon flash on with F_ON pin. Low level forces disable of xenon flash on even if F_ON is high.
9	XFULL	O	Charge completion indicator. XFULL is an open-drain output that pulls low once the output is fully charged. XFULL is high impedance during charging and all fault conditions. The recovery condition from low to high is to turn low at the CHG pin only.
10	VCC	I	Power supply. VCC is the gate drive supply and IC supply. The allowable range is from 2.7 V to 5.5 V. Bypass VCC to GND with a 1-µF ceramic capacitor as close to the IC as possible.
11	IGBT_VCC	O	Power supply for IGBT driver block
12	G_IGBT_P	O	IGBT gate driver output for turning on G_IGBT swings from GND to IGBT_VCC to drive external IGBT devices. The external resistor is needed. The value depends on the characteristics of IGBT.
13	G_IGBT_N	O	IGBT gate driver output for turning off G_IGBT swings from IGBT_VCC to GND to drive external IGBT devices. The external resistor is needed. The value depends on the characteristics of IGBT.
5, 14, 15	GND	–	Ground for power and IC internal circuits. Connect to the ground plane.
16	TEST_GND	–	Used by TI, should be connected to GND and ground plane

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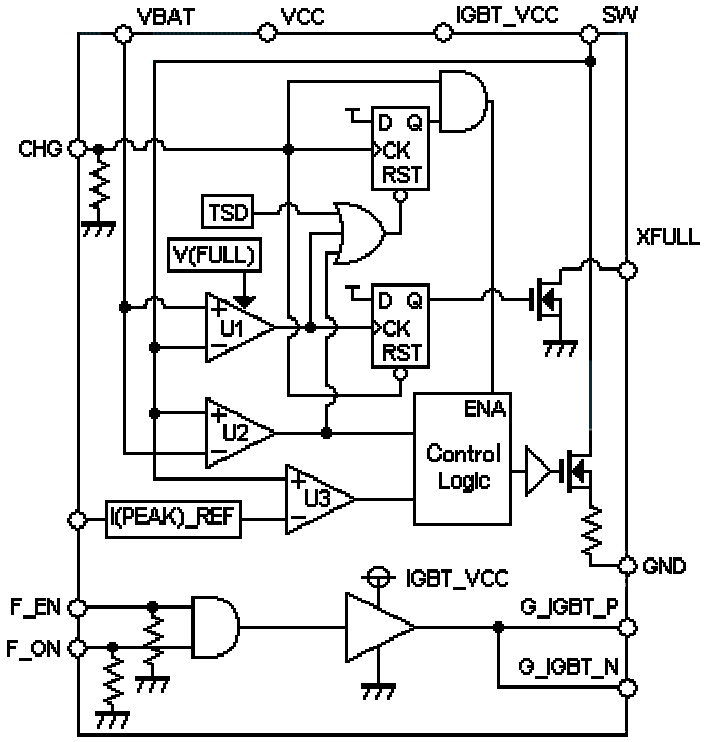


Figure 2. Block Diagram

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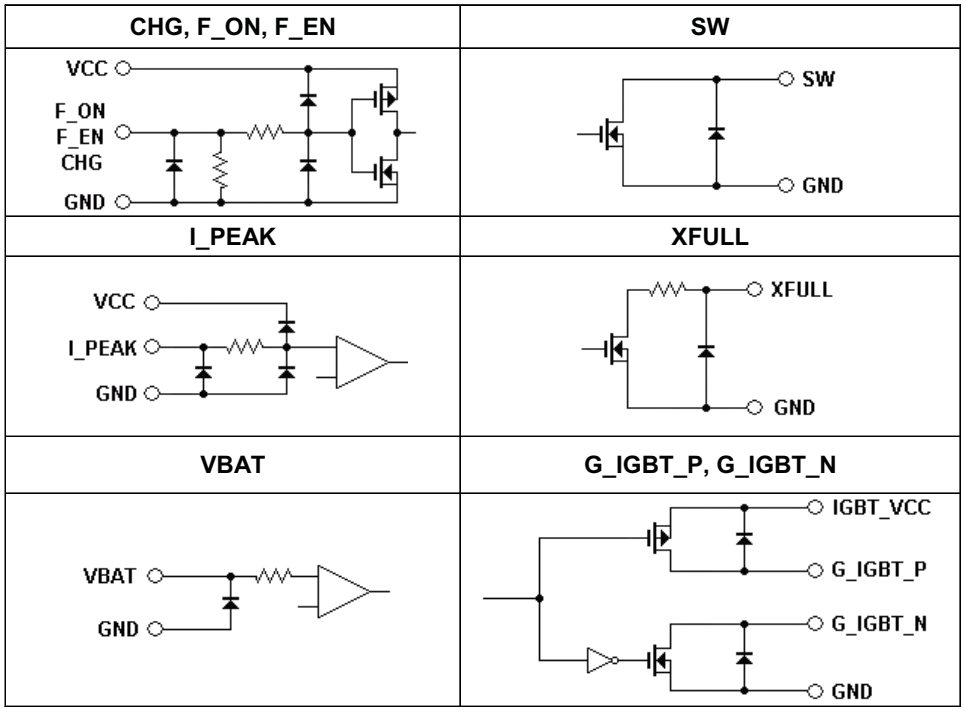


Figure 3. I/O Equivalent Circuits

PRINCIPLES OF OPERATION

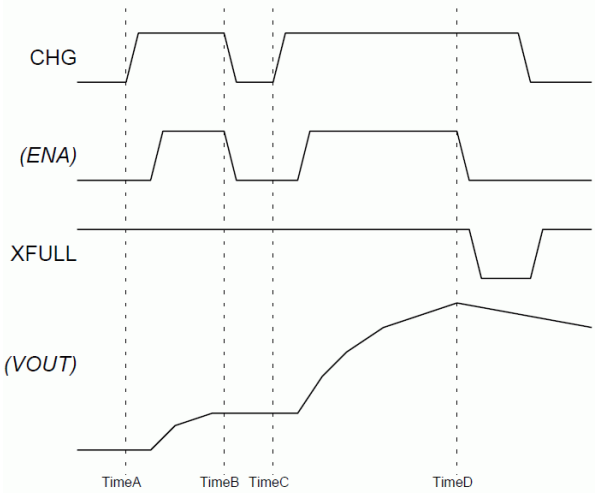


Figure 4. Charging Sequence Chart

Start/Stop Charging

The TPS65563A has an enable/disable pin for charging (CHG). The only way to start charging is to input a high-level signal into CHG (see A and C in Figure 2). This high level is latched by internal D-FF shown in Figure 2. The internal enable (ENA) signal goes up with some delay, which is specified as SW ON after CHG↑ in Switching Characteristics. This is to avoid incorrect operation with a pulsed noise at CHG.

To stop charging, there are three trigger events:

- Forced stop by inputting a low level at CHG (see B in Figure 4)
- Automatic stop by detecting a full charge. VOUT reaches the target value (see D in Figure 4).
- Protected stop by detecting an overcurrent protection (OCP) on the SW pin

When the host inputs the high-level signal into CHG, the voltage of VCC and VBAT must meet the recommended range; VBAT is from 1.4 V to 12 V, VCC is from 2.7 V to 5.5 V. It is acceptable to start recharging after a forced stop controlled by CHG (see C in Figure 4).

Charging Status Indication

When the charging operation is complete, the TPS65563A drives the charge completion indicator pin, XFULL, to a low level. A controller can detect the status of the device as a logic signal when it is connected through a pullup resistor (R1) (see Figure 1). The only way to reset the indication at XFULL is to input a low level into CHG (see Figure 4).

The XFULL output enables the controller to find the device-protected situation. If overcurrent protection (OCP) occurs, XFULL never goes to a low level when CHG is at a high level. Therefore, the controller detects OCP by measuring the time from turning CHG to a high level to turning XFULL to a low level. If the duration is longer than the maximum designed charge time, OCP occurs.

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Charging Control

Figure 5 shows a timing diagram at beginning/ending. The TPS65563A provides three comparators to control the charging operation. U1 is the V_{FULL} comparator to detect the charge completion, U2 is the V_{ZERO} comparator to detect the turn-on time of the power SW, and U3 is the I_{PEAK} comparator to detect the turn-off time of the power SW.

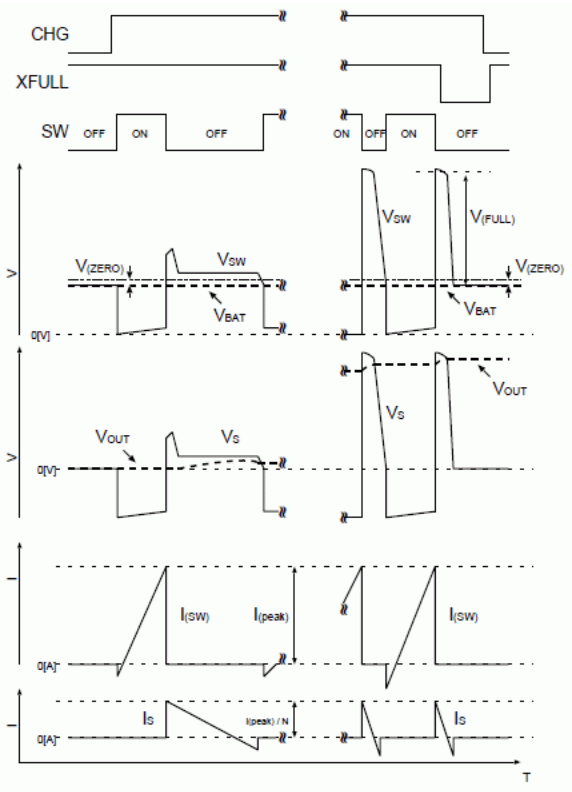


Figure 5. Beginning/Ending Timing

While the power SW is ON, the I_{PEAK} comparator (U3) monitors current flow through the power SW from SW to GND. When the current at SW (I_{SW}) exceeds the threshold defined by the voltage of the I_PEAK pin (I_{PEAK}), the power SW turns OFF.

After the power SW turns OFF, the spike voltage occurs immediately because of leakage inductance at the primary side. It might cause the power SW to break. To avoid this, the leakage inductance should be reduced as much as possible.

When the power SW is OFF, the magnetic energy in the transformer starts discharging from the primary side to the secondary side. During this discharge, the V_{ZERO} comparator (U2) monitors the kickback voltage at the primary side to compare it with the VBAT voltage. The kickback voltage increases rapidly until the diode placed at secondary side turns ON. The diode turns ON when the voltage of secondary side of the transformer reaches more than the voltage of the output capacitor. After the diode turns ON, the kickback voltage is almost stable until the magnetic energy at the primary side discharges completely.

After the discharge stops, the small amount of energy left in the transformer is released via parasitic paths, and the kickback voltage reaches almost zero voltage. During this period, U2 makes the power SW turn ON when (V_{SW} – VBAT) drops from V_{ZERO}.

The V_{FULL} comparator (U1) also monitors the kickback voltage. When V_{SW} – VBAT exceeds V_{FULL}, the TPS65563A stops the charging operation. After detection, XFULL goes to low level to indicate charge completion. After charge completion, the TPS65563A immediately goes into disable mode with the internal ENA automatically turning to a low level. The purpose is to save the consumption power.

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In Figure 5, ON time is almost the same period in every switch cycle. But the current at SW always starts from negative value because of the Trr of the diode. Because of this, ON time depends on Trr. ON time is calculated by Equation 1.

$$T_{ON(n)} = L_p \frac{I_{PEAK}}{VBAT} + Trr(n) \quad (1)$$

Where:

$T_{ON(n)}$ = ON time at n cycle switching

Lp = Inductance of primary side

I_{PEAK} = Peak current at primary side

VBAT = Battery voltage

Trr(n) = Reverse recovery time at n cycle switching

OFF time is dependant on output voltage. As the output voltage gets higher, OFF time gets shorter (see Equation 2).

$$T_{OFF(n)} = N \times L \frac{I_{PEAK}}{V_{OUT(n)}} \quad (2)$$

Where:

$T_{OFF(n)}$ = OFF time at n cycle switching

N = Turn ratio of transformer

$V_{OUT(n)}$ = Output voltage at n cycle switching

Programming Peak Current

The TPS65563A provides a method to program the peak primary current with a voltage applied to the I_PEAK pin. Figure 6 shows how to program I_{PEAK}.

Figure 6 shows the relationship between I_PEAK pin voltage and a peak current at the primary side. This function has the analog slope controlled by I_PEAK. The maximum voltage to control peak current at the primary side is around 1.2 V and it is acceptable to input the voltage up to VCC.

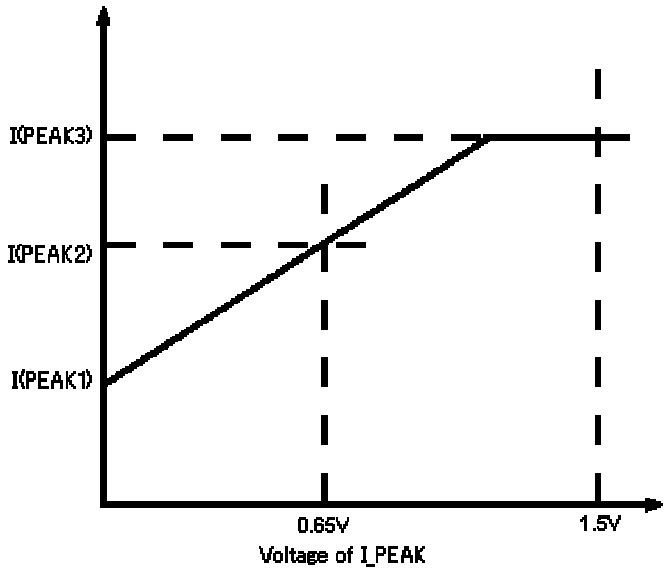


Figure 6. I_PEAK Pin Voltage vs Peak Current at Primary Side

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Typical usages of this function are:

- Setting the peak charging currents based on the battery voltage. The easiest way is to connect a resistive divider with battery voltage. This saves battery life.
- Reducing peak current at the primary side when the system powers a zoom-lens motor. This avoids inadvertent shutdowns due to a large current from the battery.

In Figure 1, three optional connections to I_PEAK are shown:

1. Use the controller to input PWM signal with RC filter.
2. Use a digital-to-analog converter (DAC).
3. Use a resistive divider to input a fixed value into I_PEAK.

Methods 1 and 2 make it possible to delicately control peak current at the primary side. For example, set higher current during initial charging, but set lower current just before complete charging. This effectively saves the battery life.

IGBT Driver Control

The TPS65563A integrates an IGBT driver for flashing the xenon tube. After charge completion, the xenon tube allows turnon with the IGBT driver. If the earlier flashing is needed before charge completion, the confirmation of the lowest allowable flashing voltage to apply to the xenon tube is required.

G_IGBT should be connected to the gate of IGBT as close as possible to avoid the misoperation of flashing or breaking the gate of IGBT. The output voltage of G_IGBT voltage depends on IGBT_VCC. The rise time and fall time of G_IGBT are almost the same because the TPS65563A does not include a pullup/pulldown resistor for the IGBT driver. The rise time and fall time should be met with the value specified in the data sheet of the IGBT to avoid breaking the IGBT.

The IGBT drive has two logic inputs, one is flash acceptable (F_EN) and the other is flash enable (F_ON). To turn on the xenon tube, high-level signal should be inputted into both F_EN and F_ON. It is acceptable to connect both F_EN and F_ON if simple control is preferred.

Protection

The TPS65563A provides two protection mechanisms; thermal shutdown and overcurrent protection.

Thermal Shutdown (TSD)

Once the TPS65563A die temperature reaches a specific temperature, the operation is immediately latched off. To recover the operation, the TPS65563A die temperature should be lower than a specific temperature and forced to a low level at CHG if protection is needed.

Overcurrent Protection (OCP)

The TPS65563A has OCP at the SW pin. The TPS65563A is latched off if the SW pin is dropped to compare VBAT pin voltage during the switch ON time. The threshold is specified in Overcurrent Protection Trigger Voltage at SW in Electrical Characteristics. To recover the operation, the CHG level is forced to a low level after protection occurs and peak current is less than threshold.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65563ARGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-35 to 85	CHS	Samples
TPS65563ARGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-35 to 85	CHS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

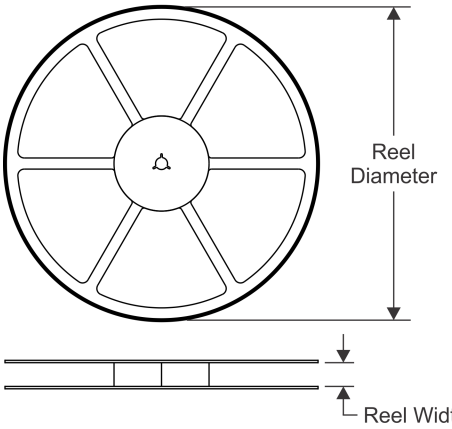
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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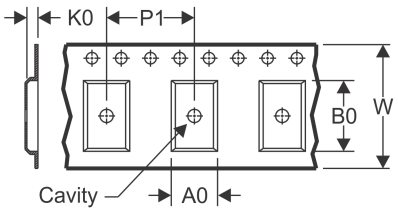
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

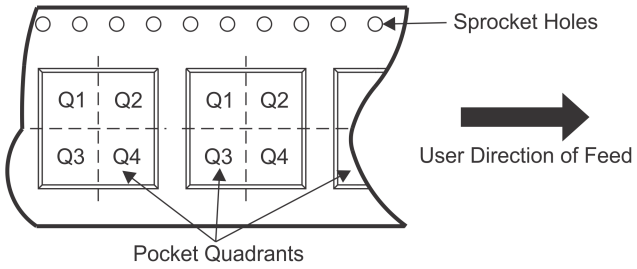


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

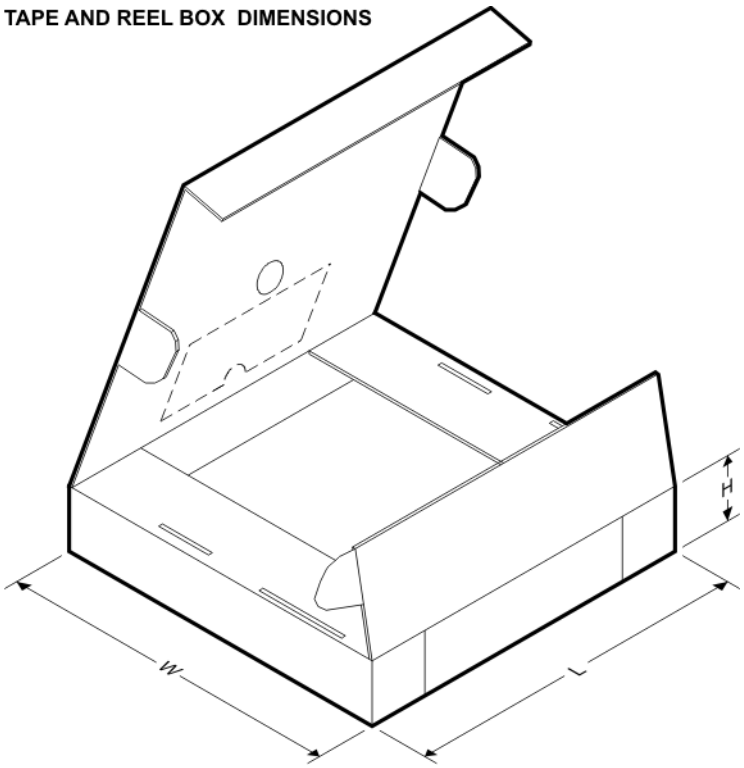
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65563ARGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65563ARGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

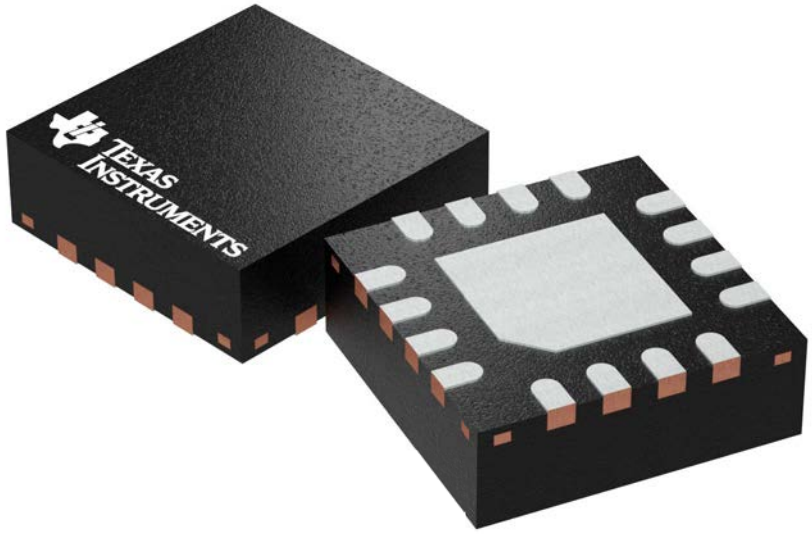


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65563ARGTR	VQFN	RGT	16	3000	853.0	449.0	35.0
TPS65563ARGTT	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



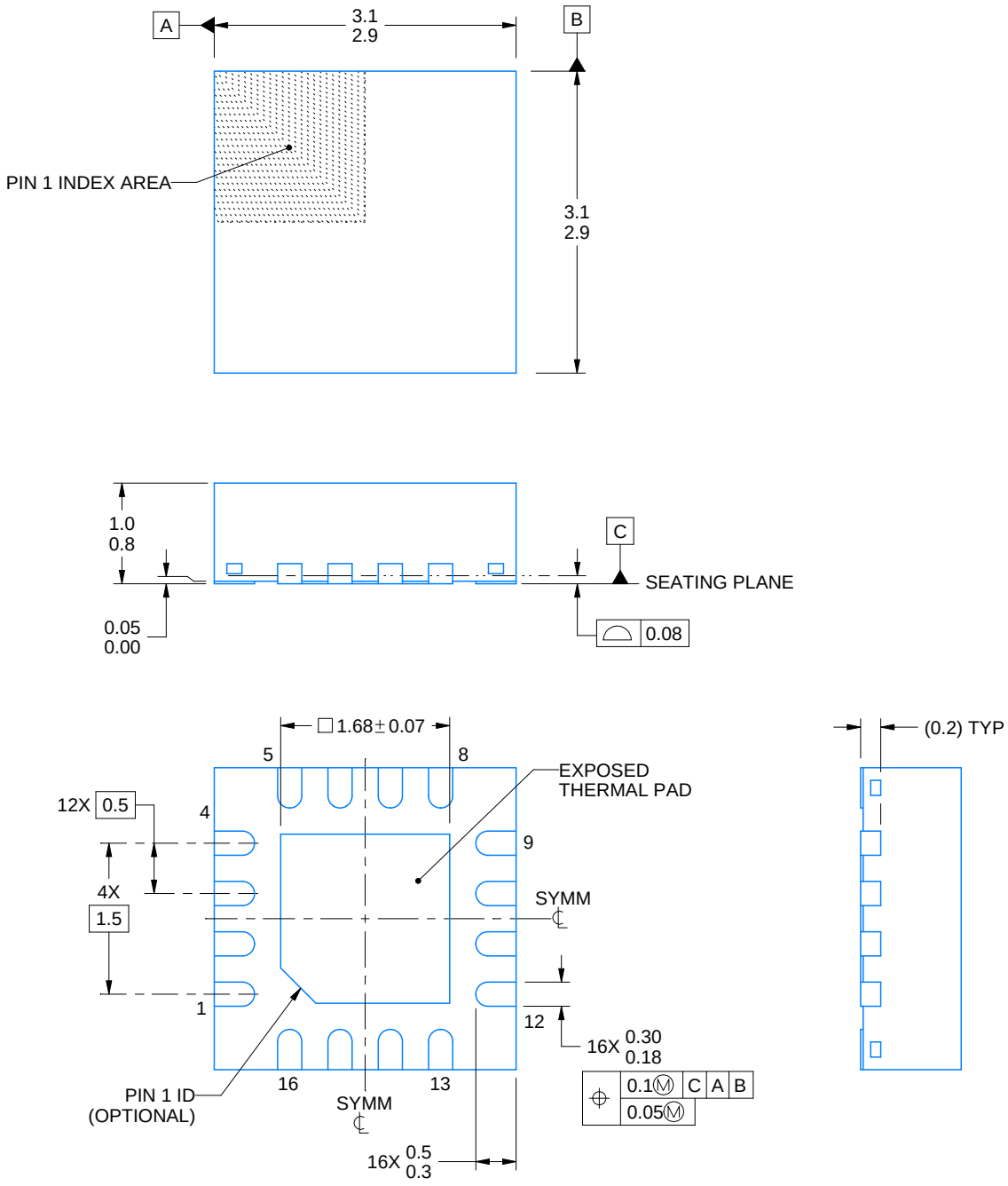
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016C

PACKAGE OUTLINE

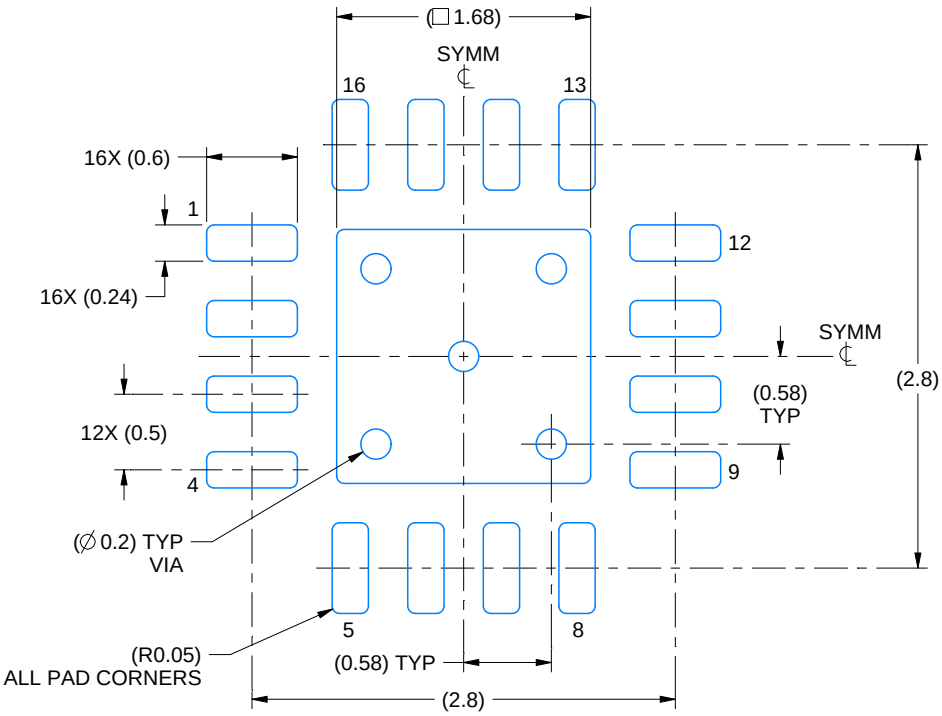
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

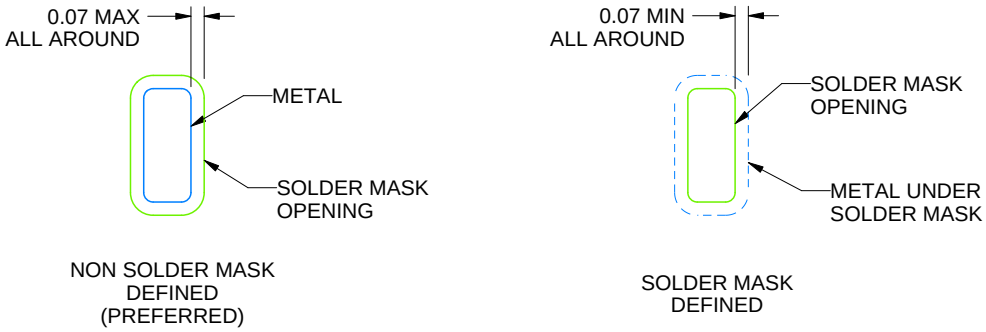


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

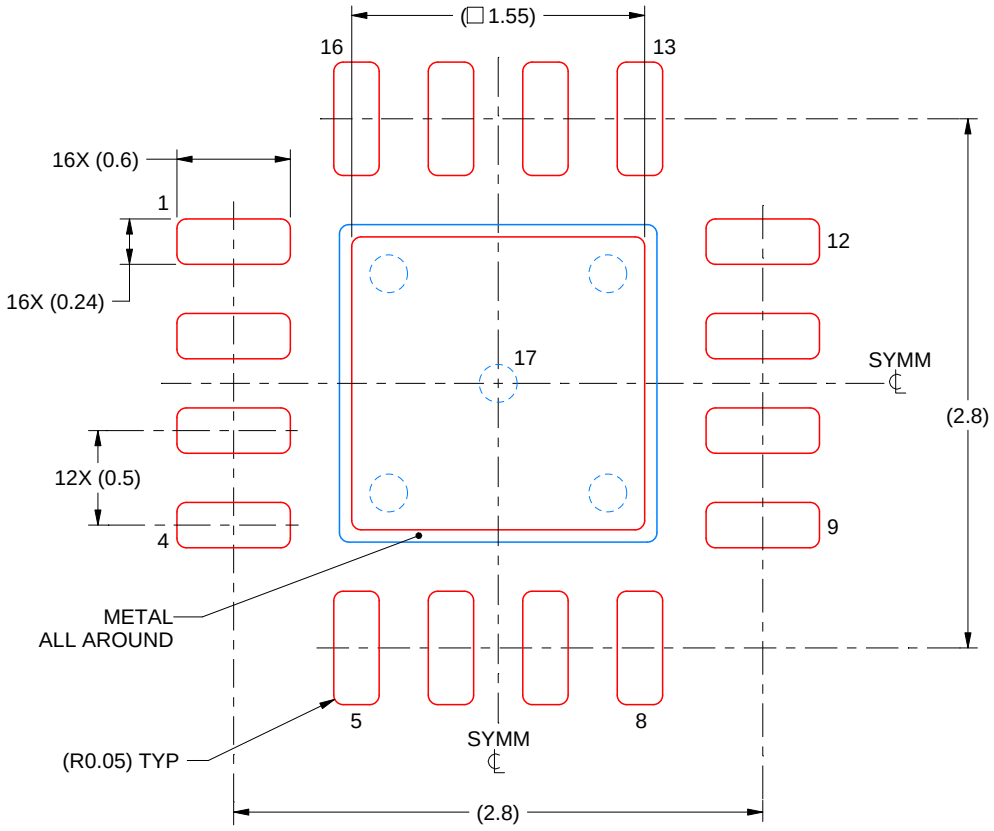


SOLDER MASK DETAILS

4222419/C 04/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/C 04/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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