

适用于隔离式电源的 UCD3138128 和 UCD3138A64 高度集成数字控制器

1 特性

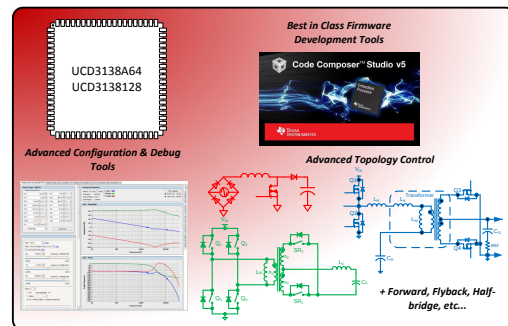
- UCD3138 系列的 64kB 和 128kB 程序闪存衍生器件
 - 2-32kB 或 4-32kB 编程闪存存储器组
 - 支持从组 1 执行，同时对其它组进行编程
 - 在不关闭电源的情况下，能够更新固件
 - 与 UCD3138 (+1 SPI, +1 I2C) 相对的额外通信端口
 - 基于引导闪存的双存储器映像支持“高速”固件更新
- 可对多达 3 个独立式反馈环路的数字控制
 - 专用的基于 PID 的硬件
 - 2 极 / 2 零可配置、非线性控制
- 高达 16MSPS 误差 A/D 转换器 (EADC)
 - 可配置分辨率 (最小值: 1mV/LSB)
 - 高达 8 倍过采样和自适应采样定位
 - 基于硬件的取平均值操作 (高达 8x)
 - 14 位高效参考数模转换器 (DAC)
- 高达 8 个高分辨率数字脉宽调制 (DPWM) 输出
 - 脉宽分辨率为 250ps
 - 4ns 频率和相位分辨率
 - 可调相移和死区
 - 逐周期占空比匹配
 - 高达 2MHz 开关频率
- 可配置后缘/前缘/三角调制
- 实时时钟 (RTC) 支持
- 可配置的反馈控制
 - 电压、平均电流和峰值电流模式控制
 - 恒定电流、恒定功率
- 可配置 FM，相移调制和脉宽调制 (PWM)
- 快速，自动和平滑模式开关
 - 频率调制和 PWM
 - 相移调制和 PWM
- 高效和轻负载管理
 - 突发模式 & 理想的二极管仿真
 - 同步整流器软启动/关闭
 - 低集成电路 (IC) 待机功率
- 初级侧电压感应
- 电流共享 (平均 & 主/从)
- 特有丰富的故障保护选项

- 7 个模拟 / 4 个数字比较器，
- 逐周期电流限制
- 可编程消隐时间和故障计数
- 外部故障输入
- 多个 UCD3138x 器件间的 DPWM 波形同步
- 15 通道, 12 位, 267ksps 通用 ADC
- 内部温度传感器
- 完全可编程高性能 31.25MHz, 32 位 ARM7TDMI-S 处理器
 - 64kB 程序闪存 (2-32kB 组)
 - 具有纠错码 (ECC) 的 2kB 数据闪存
 - 8kB 数据 RAM
 - 4kB 引导 ROM 支持固件引导加载
- 通信外设,
 - 2 个 I²C/PMBus 接口
 - 2 个 UART, 1 个 SPI
- 具有可选输入引脚的定时器捕捉
- 80 引脚四方扁平 (QFP) 封装
- 工作温度范围: -40°C 至 125°C

2 应用范围

- 电源和电信整流器
- 功率因数校正
- 独立的 DC-DC 模块
- 具有峰值电流模式控制、逻辑链路控制 (LLC)、硬开关全桥拓扑 (HSFB)、前馈等功能的移相全桥

典型应用与工具



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3 修订历史记录

Changes from Revision A (June 2014) to Revision B	Page
• Changed Device Grounding and Layout Guidelines.	71

Changes from Original (June 2014) to Revision A	Page
• 添加了器件 UCD313128	1
• 将特性从“64kB 程序闪存衍生器件”更改为“64kB 和 128kB 编程闪存衍生器件...”	1
• 已将特性从：2-32kB 编程闪存存储器组更改为：2-32kB 或 4-32kB 编程闪存存储器组	1
• 已添加特性：“基于引导闪存的双存储器...”	1
• 已将特性从：4kB 数据 RAM 更改为：8kB 数据 RAM	1
• 已将特性从：“8kB 引导 ROM 支持...”更改为：“4kB 引导 ROM 支持...”	1
• 在整个文档中将 UCD3138A64 更改为 UCD3138x	4
• 更改了“产品系列比较”表	5
• Changed title From: POWER ON RESET AND BROWN OUT (V33D pin, See Figure 3) To: POWER ON RESET AND BROWN OUT (V33A pin, See Figure 3)	12
• Changed title From: POWER ON RESET AND BROWN OUT (V33A pin, See Figure 3) To: POWER ON RESET AND BROWN OUT (V33A pin, See Figure 3)	14
• Changed From: V33D To: V33A in the definitions list following Figure 3	16
• Changed paragraph 2 of the Memory section From: 2048x32-bit Boot ROM To: 1024x32-bit Boot ROM	19
• Changed text in the Memory section description From: The availability of 64 kB of program Flash memory in 2-32 kB banks, enables the designers to implement dual images To: The availability of 64 kB or 128 kB of program Flash memory in 2-32 kB or 4-32 kB banks, enables the designers to implement multiple images	19
• Added a 2 new paragraphs to the end of the Memory section description.	19
• Changed the Memory Map (After Reset Operation) to include Program Flash 2 and Program Flash 3	55
• Changed the Memory Map (Normal Operation) to include Program Flash 2 and Program Flash 3	55

• Added Figure 36	57
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4 说明

UCD3138 系列是一款德州仪器 (TI) 数字电源控制器，此控制器在一个单芯片解决方案内提供高集成度和出色性能。相对于德州仪器 (TI) 的 UCD3138x 数字电源控制器，UCD3138x 中的 UCD3138A64 可提供 64kB 程序闪存存储器（UCD3138128 可提供 128KB 程序闪存存储器），以及 SPI 和另一个 I²C 端口等其他通信选件。利用多个 32kB 组内的程序闪存存储器，设计人员能够在器件中实施固件的双镜像（例如，一个主镜像 + 一个备用镜像），并能够选择使用适当算法从任一组中执行。它还为处理器创造了独一无二的机会来载入一个新程序并随后执行该程序，而不会中断电力输送。该特性使得最终用户能够现场为电源添加新特性，同时消除了载入新程序所需的任何停机时间。

UCD3138 系列灵活的特性使得此器件适用于广泛的电源转换优化。此外，器件内的多种外设已经过专门优化，用于提升 AC/DC 和隔离式 DC/DC 应用性能并减少信息技术 (IT) 和网络基础设施空间内的解决方案组件数量。

UCD3138 系列是完全可编程解决方案，此方案可以使用户对相关应用实现完全控制，同时还能够区分他们的解决方案。与此同时，德州仪器 (TI) 致力于通过提供一流的开发工具来简化用户的开发工作，其中包括应用固件，Code Composer Studio™ 软件开发环境和德州仪器 (TI) 的整合电源开发 GUI，这使得用户能够配置和监控关键系统参数。

控制器内核上是数字电源外设 (DPP)。每个 DPP 执行一个高速数字控制环路，此环路由一个专用误差模数转换器 (EADC)，一个基于 PID 的 2 极 - 2 零数字补偿器和脉宽分辨率为 250ps 的 DPWM 输出组成。此器件还包含一个 12 位，267ksps 通用 ADC，此 ADC 具有多达 15 个通道、定时器、中断控制、PMBus，I²C，SPI 以及 UART 通信端口。此器件基于一个执行实时监控、配置外设且管理通信的 32 位 ARM7TDMI-S 精简指令集计算机 (RISC) 微控制器。ARM 微控制器从可编程闪存存储器以及片载 RAM 和 ROM 里执行它的程序。

除了 DPP，特定电源管理外设已被添加以便在全部运行范围内启用高效、针对增加的功率密度的高集成度、可靠性、和最低总体系统成本以及支持最广泛控制体系和拓扑数量的高灵活性。此类外设包括：轻负载突发模式、同步整流、LLC 和移相全桥模式开关、输入电压前馈、覆铜线迹电流感应、理想的二极管仿真、恒定电流恒定功率控制、同步整流软导通和关断、峰值电流模式控制、磁通量均衡、次级侧输入电压感应、高分辨率电流共享、具有预偏置的硬件可配置软启动以及几个其他功能。已经针对电压模式和峰值电流模式受控相移全桥、单双相位功率因数校正 (PFC)、无桥 PFC、硬开关全桥和半桥、有源钳位正向转换器、双开关正向转换器、以及 LLC 半桥和全桥进行了拓扑支持优化。

器件信息 (1)

产品型号	封装	封装尺寸（标称值）
UCD3138128	TQFP (80)	12.00mm x 12.00mm
UCD3138A64		

(1) 如需详细订购信息，请查看本数据表结尾的[机械、封装和可订购信息](#)部分。

5 产品系列比较

特性	UCD3138 RHA/RMH	UCD3138064 RMH	UCD3138 RGC	UCD3138064 RGC	UCD3138064 RGZ	UCD3138128 PFC	UCD3138A64 PFC
提供的封装	40 引脚 QFN (6mm x 6mm)	40 引脚 QFN (6mm x 6mm)	64 引脚 QFN (9mm x 9mm)	64 引脚 QFN (9mm x 9mm)	48 引脚 QFN (7mm x 7mm)	80 引脚 QFP (14mm x 14mm) (含引线)	80 引脚 QFP (14mm x 14mm) (含引线)
ARM7TDMI-S 内核处理器	31.25MHz	31.25MHz	31.25MHz	31.25MHz	31.25MHz	31.25MHz	31.25MHz
高分辨率数字脉宽调制 (DPWM) 输出 (250ps 分辨率)	8	8	8	8	8	8	8
高速独立反馈环路数量 (# 经调节的输出 电压)	3	3	3	3	3	3	3
12 位, 256kps, 通用 ADC 通道	7	7	14	14	9	15	15
ADC 输出上的数字比较器	4	4	4	4	4	4	4
闪存存储器 (程序)	32kB	64kB	32kB	64kB	64kB	128kB	64kB
32kB 闪存存储器组中存储器的数量	1	2	1	2	2	4	仅提供 1 组 64kB 闪存
闪存存储器 (数据)	2kB	2kB	2kB	2kB	2kB	2kB	2kB
RAM	4kB	4kB	4kB	4kB	4kB	8kB	8kB
可编程故障输出	1 + 2 ⁽¹⁾	1 + 2 ⁽¹⁾	4	2 + 2 ⁽¹⁾	1 + 2 ⁽¹⁾	4	4
具有逐周期电流限制的高速模拟比较器	6	6	7	7	6	7	7
UART (SCI)	1 ⁽¹⁾	1 ⁽¹⁾	2	2	2	2	2
PMBus/I ² C	1	1	1	1	1	1	1
其它 I ² C	0	0	0	1 ⁽¹⁾	1 ⁽¹⁾	1	1
SPI	0	0	0	1 ⁽¹⁾	1 ⁽¹⁾	1	1
定时器	4 (16 位) 和 1 (24 位)	4 (16 位) 和 1 (24 位)	4 (16 位) 和 1 (24 位)	4 (16 位) 和 1 (24 位)	4 (16 位) 和 1 (24 位)	4 (16 位) 和 2 (24 位)	4 (16 位) 和 2 (24 位)
定时器 PWM 输出	1 ⁽¹⁾	1 ⁽¹⁾	2	2	1 ⁽¹⁾	4	4
定时器捕捉输入	2 ⁽¹⁾	2 ⁽¹⁾	1 + 3 ⁽¹⁾	1 + 3 ⁽¹⁾	2 ⁽¹⁾	2 + 2 ⁽¹⁾	2 + 2 ⁽¹⁾
数字通用输入输出 (GPIO) 总数	18	18	30	30	24	43	43
外部中断	0	0	1	1	0	1	1
外部石英钟支持	否	否	否	否	否	是 (引脚 #61、 62)	是 (引脚 #61、 62)
峰值电流模式控制	只适用于 EADC2	所有 EADC 通道	只适用于 EADC	所有 EADC 通道	所有 EADC 通道	所有 EADC 通道	所有 EADC 通道

(1) 代表一个可通过固件编程的备用引脚输出。

UCD3138128, UCD3138A64

ZHCSCX7B – JUNE 2014 – REVISED FEBRUARY 2017

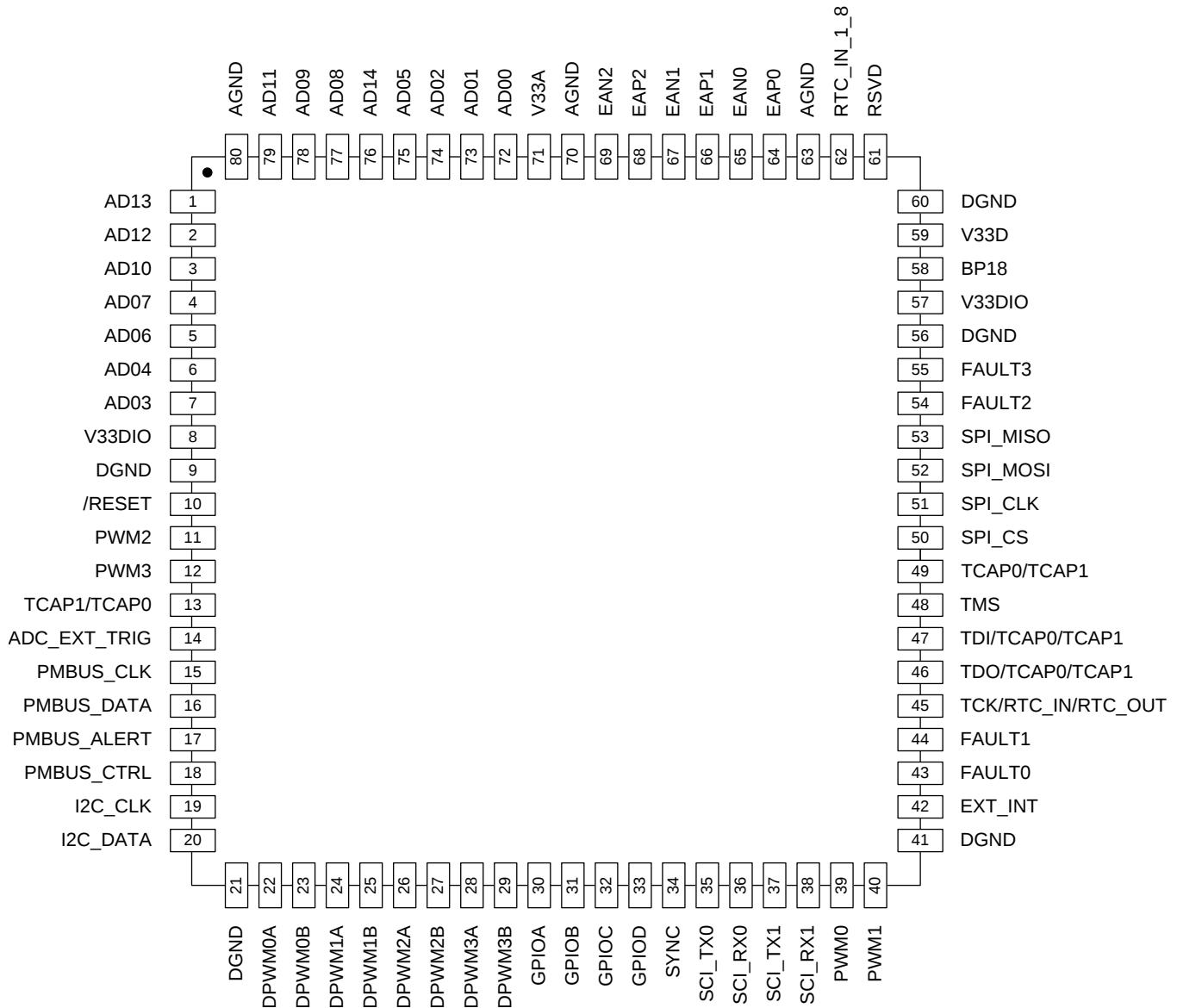
www.ti.com.cn

6 Product Feature Overview

FEATURE	UCD3138x 80 PIN
ARM7TDMI-S Core Processor	31.25 MHz
High Resolution DPWM Outputs (250ps Resolution)	8
Number of High Speed Independent Feedback Loops (# Regulated Output Voltages)	3
12-bit, 267ksps, General Purpose ADC Channels	15
Digital Comparators at ADC Outputs	4
Flash Memory (Program) (UCD3138A64)	64 kB
Flash Memory (Program) (UCD3138128)	128 kB
Flash Memory (Data)	2 kB
Flash Security	√
RAM	8 kB
DPWM Switching Frequency	up to 2 MHz
Programmable Fault Inputs	4
High Speed Analog Comparators with Cycle-by-Cycle Current Limiting	7
UART (SCI)	2
PMBus	1
I ² C	1
SPI	1
Timers	4 (16 bit) and 2 (24 bit)
Timer PWM Outputs	4
Timer Capture Inputs	2
Watchdog	√
On Chip Oscillator	√
Power-On Reset and Brown-Out Detector	√
Sync IN and Sync OUT Functions	√
Total GPIO (includes all pins with multiplexed functions such as, DPWM, Fault Inputs, SCI, etc.)	43
External Interrupts	1

7 Pin Configuration and Functions

**12mm × 12mm TQFP
80 Pins
Bottom View**



Additional pin functionality is specified in the following table.

Pin Functions

PIN	NAME	PRIMARY ASSIGNMENT	ALTERNATE ASSIGNMENT		CONFIGURABLE AS A GPIO?
			NO. 1	NO. 2	
1	AD13	12-bit ADC, Ch 13, comparator E; I-share	DAC output		
2	AD12	12-bit ADC, Ch 12			
3	AD10	12-bit ADC, Ch 10			
4	AD07	12-bit ADC, Ch 7, Connected to comparator F and reference to comparator G	DAC output		
5	AD06	12-bit ADC, Ch 6, Connected to comparator F	DAC output		
6	AD04	12-bit ADC, Ch 4, Connected to comparator D	DAC output		
7	AD03	12-bit ADC, Ch 3, Connected to comparator B and C			
8	V33DIO	Digital I/O 3.3V core supply			

Pin Functions (continued)

PIN	NAME	PRIMARY ASSIGNMENT	ALTERNATE ASSIGNMENT		CONFIGURABLE AS A GPIO?
			NO. 1	NO. 2	
9	DGND	Digital ground			
10	RESET	Device Reset Input, active low			
11	PWM2	General purpose PWM 2			Yes
12	PWM3	General purpose PWM 3			Yes
13	TCAP1	Timer Capture Input	TCAP0		Yes
14	ADC_EXT_TRIG	ADC conversion external trigger input			Yes
15	PMBUS_CLK	PMBUS Clock (Open Drain)			Yes
16	PMBUS_DATA	PMBus data (Open Drain)			Yes
17	PMBUS_ALERT	PMBus Alert (Open Drain)			Yes
18	PMBUS_CTRL	PMBus Control (Open Drain)			Yes
19	I2C_CLK	I2C Clock			Yes
20	I2C_DATA	I2C Data			Yes
21	DGND	Digital ground			
22	DPWM0A	DPWM 0A output			Yes
23	DPWM0B	DPWM 0B output			Yes
24	DPWM1A	DPWM 1A output			Yes
25	DPWM1B	DPWM 1B output			Yes
26	DPWM2A	DPWM 2A output			Yes
27	DPWM2B	DPWM 2B output			Yes
28	DPWM3A	DPWM 3A output			Yes
29	DPWM3B	DPWM 3B output			Yes
30	GPIOA	General Purpose I/O Pin			Yes
31	GPIOB	General Purpose I/O Pin			Yes
32	GPIOC	General Purpose I/O Pin			Yes
33	GIPOD	General Purpose I/O Pin			Yes
34	SYNC	DPWM Synchronize pin			Yes
35	SCI_TX0	SCI TX 0			Yes
36	SCI_RX0	SCI RX 0			Yes
37	SCI_TX1	SCI TX 1			Yes
38	SCI_RX1	SCI RX 1			Yes
39	PWM0	General purpose PWM 0			Yes
40	PWM1	General purpose PWM 1			Yes
41	DGND	Digital ground			
42	EXT_INT	External Interrupt			Yes
43	FAULT0	External fault input 0			Yes
44	FAULT1	External fault input 1			Yes
45	TCK ⁽¹⁾	JTAG TCK (for manufacturer test only)	RTC_IN	RTC_OUT	Yes
46	TDO ⁽¹⁾	JTAG TDO (for manufacturer test only)	TCAP0	TCAP1	Yes
47	TDI ⁽¹⁾	JTAG TDI (for manufacturer test only)	TCAP0	TCAP1	Yes
48	TMS ⁽¹⁾	JTAG TMS (for manufacturer test only)			Yes
49	TCAP0	Timer Capture Input	TCAP1		Yes
50	SPI_CS	SPI Chip Select			Yes
51	SPI_CLK	SPI Clock			Yes
52	SPI_MOSI	SPI Master Output Slave Input			Yes
53	SPI_MISO	SPI Master Input Slave Output			Yes
54	FAULT2	External fault input 2			Yes
55	FAULT3	External fault input 3			Yes
56	DGND	Digital ground			
57	V33DIO	Digital I/O 3.3V core supply			
58	BP18	1.8V Bypass (For internal use only, do not load)			
59	V33D	Digital 3.3V core supply			
60	DGND	Digital ground			
61	RSVD	Internal use only. Tie to BP18.			
62	RTC_IN_1_8	RTC external clock input			

(1) Fusion Digital Power based debug tools are recommended instead of JTAG.

Pin Functions (continued)

PIN	NAME	PRIMARY ASSIGNMENT	ALTERNATE ASSIGNMENT		CONFIGURABLE AS A GPIO?
			NO. 1	NO. 2	
63	AGND	Analog ground			
64	EAP0	Channel #0, differential analog voltage, positive input			
65	EAN0	Channel #0, differential analog voltage, negative input			
66	EAP1	Channel #1, differential analog voltage, positive input			
67	EAN1	Channel #1, differential analog voltage, negative input			
68	EAP2	Channel #2, differential analog voltage, positive input			
69	EAN2	Channel #2, differential analog voltage, negative input			
70	AGND	Analog ground			
71	V33A	Analog 3.3V supply			
72	AD00	12-bit ADC, Ch 0, Connected to current source			
73	AD01	12-bit ADC, Ch 1, Connected to current source			
74	AD02	12-bit ADC, Ch 2, Connected to comparator A, I-share			
75	AD05	12-bit ADC, Ch 5			
76	AD14	12-bit ADC, Ch 14			
77	AD08	12-bit ADC, Ch 8			
78	AD09	12-bit ADC, Ch 9			
79	AD11	12-bit ADC, Ch 11			
80	AGND	Analog ground			

8 Specifications

8.1 Absolute Maximum Ratings ⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
V33D	V33D to DGND	–0.3	3.8	V
V33DIO	V33DIO to DGND	–0.3	3.8	V
V33A	V33A to AGND	–0.3	3.8	V
BP18	BP18 to DGND	–0.3	2.5	V
DGND – AGND	Ground difference		0.3	V
RTC_IN_1_8/RSVD		–0.3	3.0	V
All Pins, excluding AGND ⁽²⁾	Voltage applied to any pin	–0.3	3.8	V
T _{OPT}	Junction Temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Referenced to DGND

8.2 Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature range		−55	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	−2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	−500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V33D	Digital power	3.0	3.3	3.6	V
V33DIO	Digital I/O power	3.0	3.3	3.6	V
V33A	Analog power	3.0	3.3	3.6	V
BP18	1.8 V digital power	1.6	1.8	2.0	V
T _J	Junction temperature	-40	-	125	°C

8.4 Thermal Information

THERMAL METRIC ⁽¹⁾		80-PIN QFN	UNIT
R _{θJA}	Junction-to-ambient thermal resistance	47.8	°C/W
R _{θJctop}	Junction-to-case (top) thermal resistance	7.8	
R _{θJB}	Junction-to-board thermal resistance	24.4	
Ψ _{JT}	Junction-to-top characterization parameter	0.2	
Ψ _{JB}	Junction-to-board characterization parameter	24.0	
R _{θJcbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

8.5 Electrical Characteristics

V33A = V33D = V33DIO = 3.3V; 1μF from BP18 to DGND, T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT					
I33A ⁽¹⁾	Measured on V33A. The device is powered up but all ADC12 and EADC sampling is disabled		6.3		mA
I33DIO ⁽¹⁾	All GPIO and communication pins are open		0.35		mA
I33D ⁽¹⁾	ROM program execution		69		mA
I33	The device is in ROM mode with all DPWMs enabled and switching at 2 MHz. The DPWMs are all unloaded.		93	100	mA
ERROR ADC INPUTS EAP, EAN					
EAP – AGND		-0.15		1.998	V
EAP – EAN		-0.256		1.848	V
Typical error range	AFE = 0	-256		248	mV
EAP – EAN Error voltage digital resolution	AFE = 3	0.8	1	1.20	mV
	AFE = 2	1.7	2	2.30	mV
	AFE = 1	3.55	4	4.45	mV
	AFE = 0	6.90	8	9.10	mV
R _{EA}	Input impedance (See Figure 9)	AGND reference	0.5		MΩ
I _{OFFSET}	Input offset current (See Figure 9)	-5		5	μA
EADC Offset	Input voltage = 0 V at AFE = 0	-16		16	mV
	Input voltage = 0 V at AFE = 1	-10		10	mV
	Input voltage = 0 V at AFE = 2	-6		-6	mV
	Input voltage = 0 V at AFE = 3	-4		4	mV
Sample Rate				15.62 5	MHz
Analog Front End Amplifier Bandwidth			100		MHz

(1) Characterized by design and not production tested.

Electrical Characteristics (continued)

V33A = V33D = V33DIO = 3.3V; 1μF from BP18 to DGND, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
A ₀	Gain	See Figure 10		1		V/V
	Minimum output voltage				21	mV
EADC DAC						
	DAC range		0		1.6	V
	VREF DAC reference resolution	10 bit, No dithering enabled		1.56		mV
	VREF DAC reference resolution	With 4 bit dithering enabled		97.6		μV
	INL		–1.5		1.5	LSB
	DNL		–1.0		2.1	LSB
	DAC reference voltage		1.58		1.61	V
ADC12						
I _{BIAS}	Bias current for PMBus address pins		9.5		10.5	μA
	Measurement range for voltage monitoring		0		2.5	V
	Internal ADC reference voltage	–40°C to 125°C	2.475	2.500	2.53	V
	Change in Internal ADC reference from 25°C reference voltage ⁽¹⁾	–40°C to 25°C		–0.7		mV
		25°C to 125°C		–6		
	ADC12 INL integral nonlinearity ⁽¹⁾	ADC_SAMPLING_SEL = 6 for all ADC12 data, 25 °C to 125 °C		–7.5/+2.9		LSB
	ADC12 DNL differential nonlinearity ⁽¹⁾			–0.7/+3.2		LSB
	ADC Zero Scale Error		–7	±5	7	mV
	ADC Full Scale Error		–35	±20	35	mV
	Input bias	2.5 V applied to pin			200	nA
	Input leakage resistance ⁽¹⁾	ADC_SAMPLING_SEL= 6 or 0		1		MΩ
	Input Capacitance ⁽¹⁾			10		pF
DIGITAL INPUTS/OUTPUTS⁽²⁾⁽³⁾						
V _{OL}	Low-level output voltage ⁽⁴⁾	I _{OH} = 4 mA, V33DIO = 3 V			DGND + 0.25	V
V _{OH}	High-level output voltage ⁽⁴⁾	I _{OH} = –4 mA, V33DIO = 3 V	V33DIO – 0.6			V
V _{IH}	High-level input voltage	V33DIO = 3 V	2.1			V
V _{IL}	Low-level input voltage	V33DIO = 3 V			1.1	V
I _{OH}	Output sinking current				4	mA
I _{OL}	Output sourcing current		–4			mA
SYSTEM PERFORMANCE						
	Processor master clock (MCLK)			31.25		MHz
t _{Delay}	Digital filter delay ⁽⁵⁾	(1 clock = 32ns)			6	MCLKs
f _(PCLK)	Internal oscillator frequency		240	250	260	MHz
I _{SHARE}	Current share current source (See Figure 28)		238		259	μA
R _{SHARE}	Current share resistor (See Figure 28)		9.7		10.3	kΩ
POWER ON RESET AND BROWN OUT (V33A pin, See Figure 3)						
V _{GH}	Voltage good High			2.7		V
V _{GL}	Voltage good Low			2.5		V
V _{res}	Voltage at which IReset signal is valid ⁽¹⁾			0.8		V

(2) DPWM outputs are low after reset. Other GPIO pins are configured as inputs after reset.

(3) On the 40 pin package V33DIO is connected to V33D internally.

(4) The maximum total current, I_{OHmax} and I_{OLmax} for all outputs combined, should not exceed 12 mA to hold the maximum voltage drop specified. Maximum sink current per pin = –6 mA at V_{OL}; maximum source current per pin = 6 mA at V_{OH}.

(5) Time from close of error ADC sample window to time when digitally calculated control effort (duty cycle) is available. This delay, which has no variation associated with it, must be accounted for when calculating the system dynamic response.

Electrical Characteristics (continued)

V33A = V33D = V33DIO = 3.3V; 1μF from BP18 to DGND, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Brownout	Internal signal warning of brownout conditions		2.9		V
TEMPERATURE SENSOR⁽¹⁾					
V _{TEMP}	Voltage range of sensor	1.46		2.44	V
Voltage resolution	Volts/°C		6.3		mV/°C
Temperature resolution	Degree C per bit		0.0969		°C/LSB
Accuracy ⁽¹⁾⁽⁶⁾	–40°C to 125°C	–10	±5	10	°C
Temperature range	–40°C to 125°C	–40		125	°C
I _{TEMP}	Current draw of sensor when active		30		μA
V _{AMB} Ambient temperature	Trimmed 25°C reading		1.87		V
ANALOG COMPARATOR					
DAC Reference DAC Range		0		2.5	V
Reference Voltage		2.478	2.5	2.513	V
Bits			7		bits
INL ⁽¹⁾		–0.42		0.21	LSB
DNL ⁽¹⁾		0.06		0.12	LSB
Offset		–5.5		19.5	mV
Reference DAC buffered output load ⁽⁷⁾		0.5		1	mA
Buffer offset (–0.5 mA)				8.3	mV
Buffer offset (1.0 mA)				17	mV
RTC INTERFACE					
f _{RTC} RTC external input frequency			10		MHz

(6) Ambient temperature offset value from the TEMPSENCTRL register should be used to meet accuracy.

(7) Available from reference DACs for comparators D, E, F and G.

8.6 Timing Characteristics

V33A = V33D = V33DIO = 3.3V; 1μF from BP18 to DGND, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
EADC DAC					
t Settling Time	From 10% to 90%		250		ns
ADC12					
ADC single sample conversion time ⁽¹⁾	ADC_SAMPLING_SEL = 6 or 0		3.9		μs
SYSTEM PERFORMANCE					
TWD Watchdog time out resolution	Total time is: TWD x (WDCTRL.PERIOD+1)	10.5	13.3	17	ms
Time to disable DPWM output based on active FAULT pin signal	High level on FAULT pin		66		ns
Flash Read			1		MCLKs
t _{Delay} Digital filter delay ⁽²⁾	(1 clock = 32ns)			6	MCLKs
Retention period of flash content (data retention and program)	T _J = 25°C	100			years
Program time to erase one page or block in data flash or program flash			20		ms
Program time to write one word in program flash			50		μs

(1) Characterized by design and not production tested.

(2) Time from close of error ADC sample window to time when digitally calculated control effort (duty cycle) is available. This delay, which has no variation associated with it, must be accounted for when calculating the system dynamic response.

Timing Characteristics (continued)

V33A = V33D = V33DIO = 3.3V; 1μF from BP18 to DGND, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Program time to write one word in data flash			40		μs
Sync-in/sync-out pulse width	Sync pin		256		ns
POWER ON RESET AND BROWN OUT (V33A pin, See Figure 3)					
t _{POR}	Time delay after Power is good or RESET* relinquished		1		ms
t _{EXC1}	The time it takes from the device to exit a reset state and begin executing the boot flash. ⁽¹⁾	I _{RESET} goes from a low state to a high state. This is approximately equivalent to toggling the external reset pin from low to high state.	0.5		ms
t _{EXC2}	The time it takes from the device to exit a reset state and begin executing program flash bank 0 (32 kB). ⁽¹⁾	I _{RESET} goes from a low state to a high state. This is approximately equivalent to toggling the external reset pin from low to high state.	3		ms
t _{EXCT}	The time it takes from the device to exit a reset state and begin executing the total program flash (64 kB). ⁽¹⁾	I _{RESET} goes from a low state to a high state. This is approximately equivalent to toggling the external reset pin from low to high state.	6		ms
TEMPERATURE SENSOR⁽¹⁾					
t _{ON}	Turn on time / settling time of sensor		100		μs
ANALOG COMPARATOR					
Bits			7		bits
INL ⁽¹⁾		–0.42		0.21	LSB
DNL ⁽¹⁾		0.06		0.12	LSB
Time to disable DPWM output based on 0 V to 2.5 V step input on the analog comparator. ⁽¹⁾			90	150	ns

8.7 PMBUS/SMBUS/IC Timing²

The timing characteristics and timing diagram for the communications interface that supports I²C, SMBus, and PMBus in Slave or Master mode are shown in the [Timing Requirements](#), [Figure 1](#), and [Figure 2](#). The numbers in the [Timing Requirements](#) are for 400 kHz operating frequency. However, the device supports two speeds, standard (100 kHz) and fast (400 kHz).

8.8 Timing Requirements

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Typical values at T _A = 25°C and VCC = 3.3 V (unless otherwise noted)					
f _{SMB}	SMBus/PMBus operating frequency	Slave mode, SMBC 50% duty cycle	100	400	kHz
f _{I2C}	I ² C operating frequency	Slave mode, SCL 50% duty cycle	100	400	kHz
t _(BUF)	Bus free time between start and stop ⁽¹⁾		1.3		μs
t _(HD:STA)	Hold time after (repeated) start ⁽¹⁾		0.6		μs
t _(SU:STA)	Repeated start setup time ⁽¹⁾		0.6		μs
t _(SU:STO)	Stop setup time ⁽¹⁾		0.6		μs
t _(HD:DAT)	Data hold time	Receive mode	0		ns
t _(SU:DAT)	Data setup time		100		ns
t _(TIMEOUT)	Error signal/detect ⁽²⁾			35	ms
t _(LOW)	Clock low period		1.3		μs

(1) Fast mode, 400 kHz

(2) The device times out when any clock low exceeds t_(TIMEOUT).

Timing Requirements (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(HIGH)}$	Clock high period ⁽³⁾			35	ms
$t_{(LOW:SEXT)}$	Cumulative clock low slave extend time ⁽⁴⁾			25	ms
t_f	Clock/data fall time	Rise time $t_r = (V_{ILmax} - 0.15)$ to $(V_{IHmin} + 0.15)$		$20 + 0.1 C_b^{(5)}$	300 ns
t_r	Clock/data rise time	Fall time $t_f = 0.9 VDD$ to $(V_{ILmax} - 0.15)$		$20 + 0.1 C_b^{(5)}$	300 ns
C_b	Total capacitance of one bus line			400	pF

(3) $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for $t > 50$ ms causes reset of any transaction that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0] = 0).

(4) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.

(5) C_b (pF)

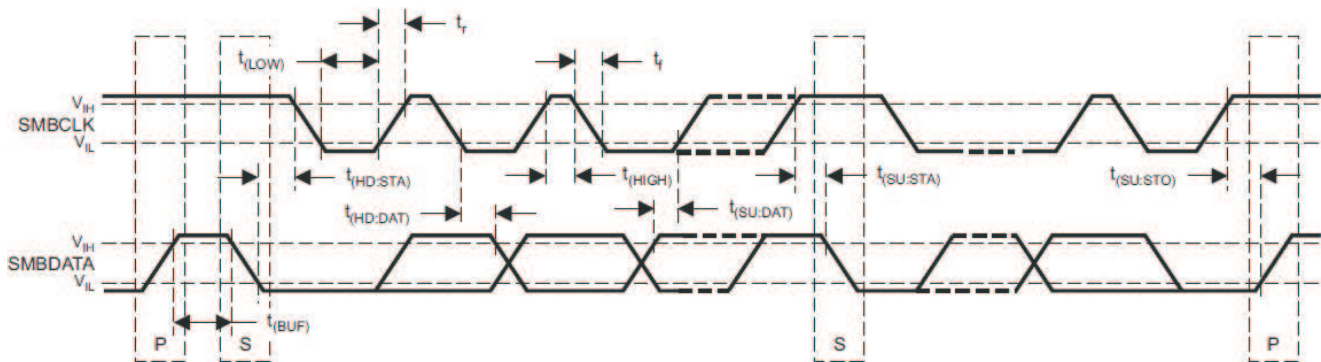


Figure 1. IC/SMBUS/PMBUS Timing Diagram²

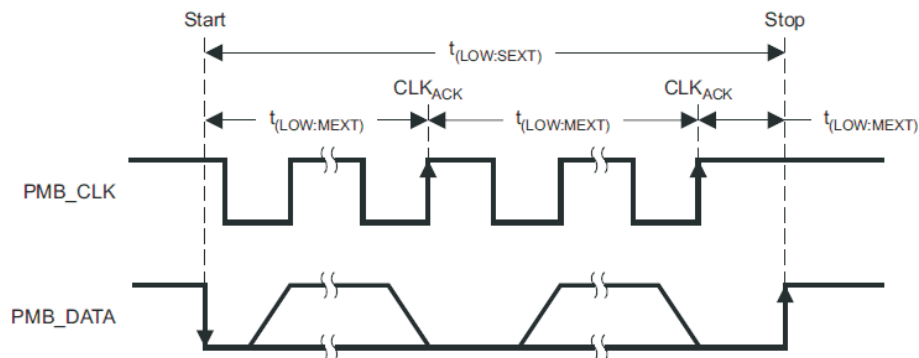


Figure 2. Bus Timing In Extended Mode

8.9 Power On Reset (POR) / Brown Out Detect (BOD)

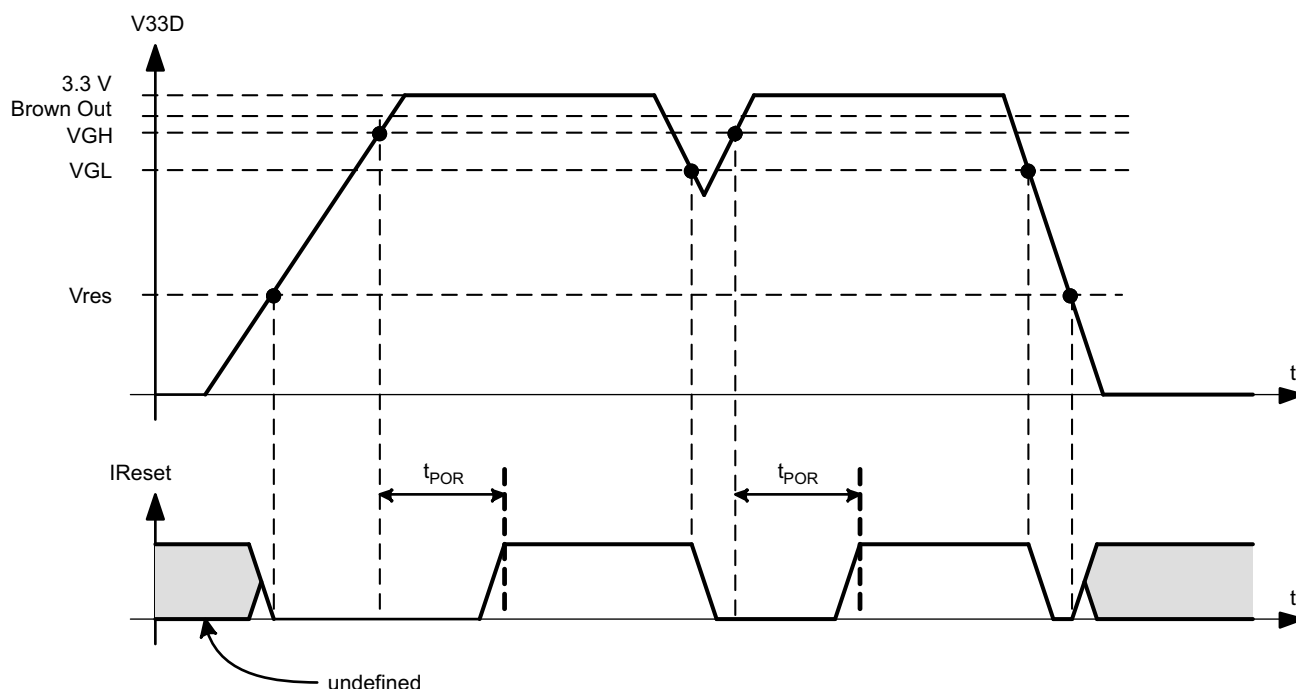
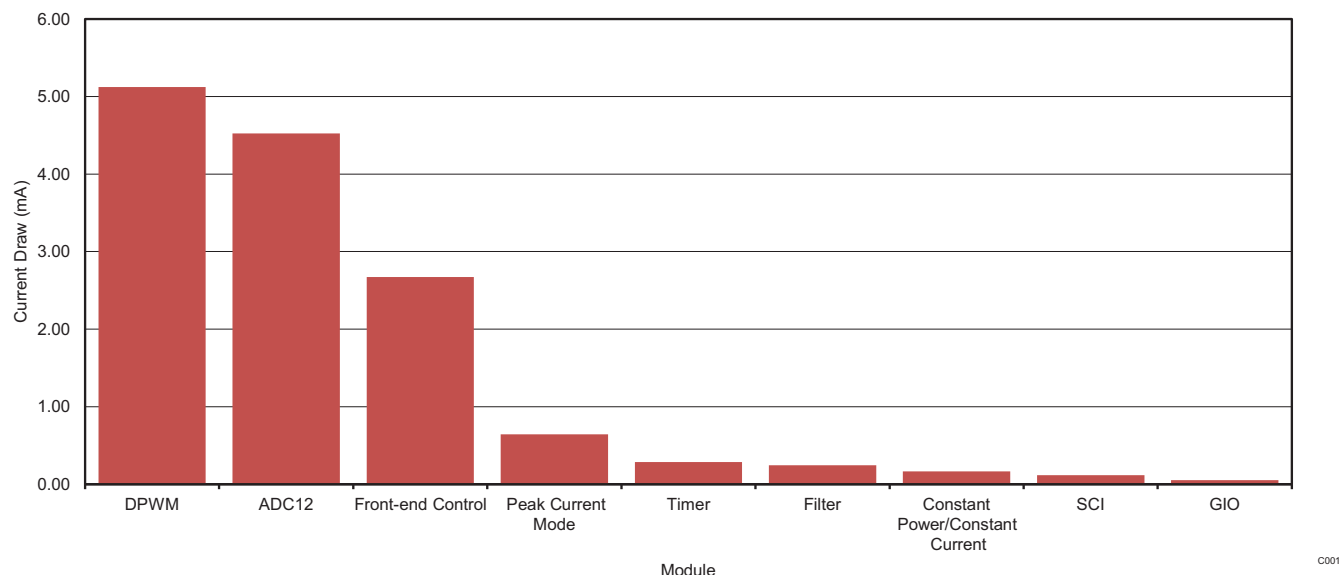


Figure 3. Power On Reset (POR) / Brown Out Reset (BOR)

- VGH – This is the V33A threshold where the internal power is declared good. The UCD3138x comes out of reset when above this threshold.
- VGL – This is the V33A threshold where the internal power is declared bad. The device goes into reset when below this threshold.
- V_{res} – This is the V33A threshold where the internal reset signal is no longer valid. Below this threshold the device is in an indeterminate state.
- I_{Reset} – This is the internal reset signal. When low, the device is held in reset. This is equivalent to holding the reset pin on the IC low.
- t_{POR} – The time delay from when VGH is exceeded to when the device comes out of reset.
- Brown Out – This is the V33A voltage threshold at which the device sets the brown out status bit. In addition an interrupt can be triggered if enabled.

8.10 Typical Clock Gating Power Savings



The CLKGATECTRL register provides control bits that can enable or disable the clock to several peripherals such as, PCM, CPCC, digital filters, front ends, DPWMs, UARTs, ADC-12 and more.

By default, all these controls are enabled. If a specific peripheral is not used the clock gate can be disabled in order to block the propagation of the clock signal to that peripheral and therefore reduce the overall current consumption of the device. The power savings chart displays the power savings per module. For example there are 4 DPWM modules, therefore, if all 4 are disabled a total of ~20 mA can be saved.

8.11 Typical Characteristics

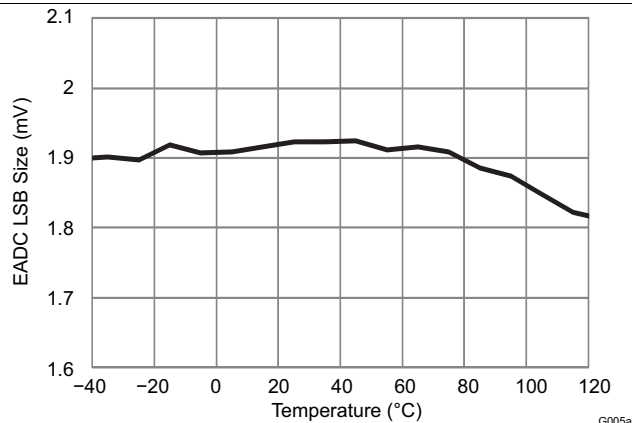


Figure 4. EADC LSB Size With 4x Gain (mV) vs. Temperature

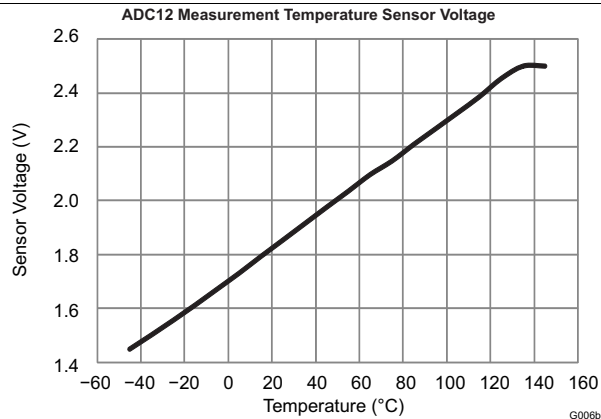


Figure 5. ADC12 Measurement Temperature Sensor Voltage vs. Temperature

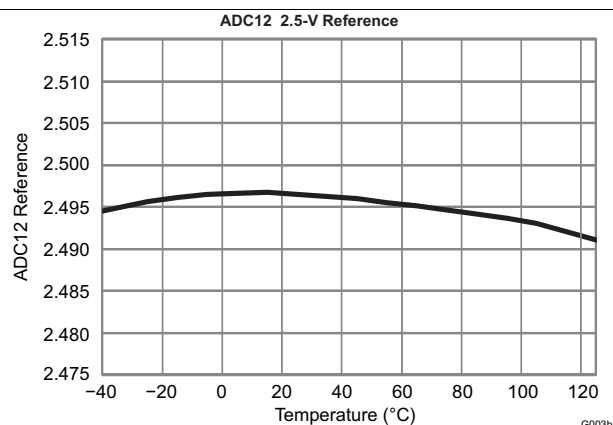


Figure 6. ADC12 2.5-V Reference vs. Temperature

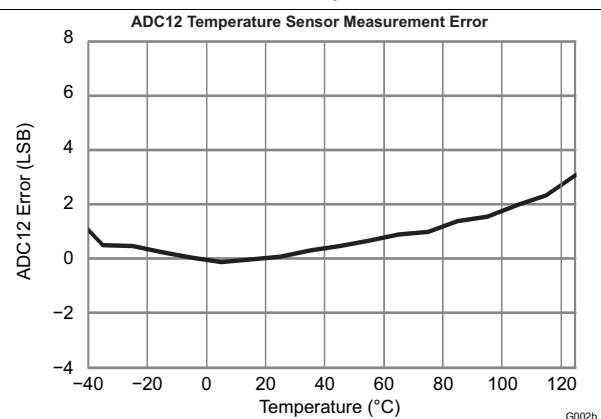


Figure 7. ADC12 Temperature Sensor Measurement Error vs. Temperature

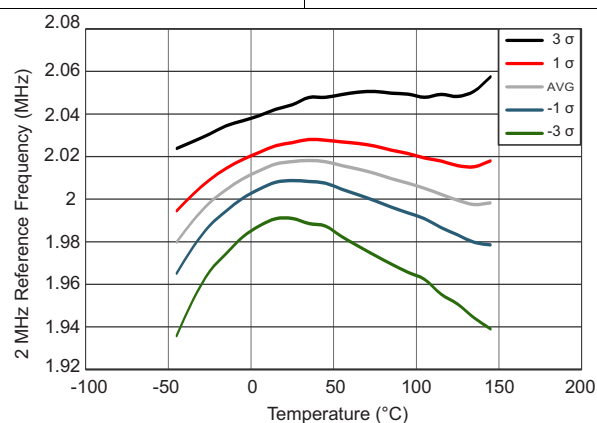


Figure 8. Oscillator Frequency (2MHz Reference, Divided Down From 250MHz) vs. Temperature

9 Detailed Description

9.1 Overview

9.1.1 ARM Processor

The ARM7TDMI-S processor is a synthesizable member of the ARM family of general purpose 32-bit microprocessors. The ARM architecture is based on RISC (Reduced Instruction Set Computer) principles where two instruction sets are available. The 32-bit ARM instruction set and the 16-bit Thumb instruction set. The Thumb instructions allow for higher code density equivalent to a 16-bit microprocessor, with the performance of the 32-bit microprocessor.

The three-staged pipelined ARM processor has fetch, decode and execute stage architecture. Major blocks in the ARM processor include a 32-bit ALU, 32 x 8 multiplier, and a barrel shifter.

9.1.2 Memory

The UCD3138x (ARM7TDMI-S) is a Von-Neumann architecture, where a single bus provides access to all of the memory modules. All of the memory module addresses are sequentially aligned along the same address range. This applies to program flash, data flash, ROM and all other peripherals.

Within the UCD3138 family architecture, there is a 1024x32-bit Boot ROM that contains the initial firmware startup routines for PMBUS communication and non-volatile (FLASH) memory download. This boot ROM is executed after power-up-reset checks if there is a valid FLASH program written. If a valid program is present, the ROM code branches to the main FLASH-program execution. If there is no valid program, the device waits for a program download through the PMBus.

The UCD3138 family also supports customization of the boot program by allowing an alternative boot routine to be executed from program FLASH. This feature enables assignment of a unique address to each device; therefore, enabling firmware reprogramming even when several devices are connected on the same communication bus.

There are three separate flash memory areas present inside the device. There are 2-32 kB program flash blocks and 1-2 kB data flash area. The 32 kB program areas are organized as 8 k x 32 bit memory blocks and are intended to be for the firmware programs. The blocks are configured with page erase capability for erasing blocks as small as 1 kB per page, or with a mass erase for erasing the entire 32 kB array. The flash endurance is specified at 1000 erase/write cycles and the data retention is good for 100 years. The 2 kB data flash array is organized as a 512 x 32 bit memory (32 byte page size). The data flash is intended for firmware data value storage and data logging. Thus, the Data flash is specified as a high endurance memory of 20 k cycles with embedded error correction code (ECC).

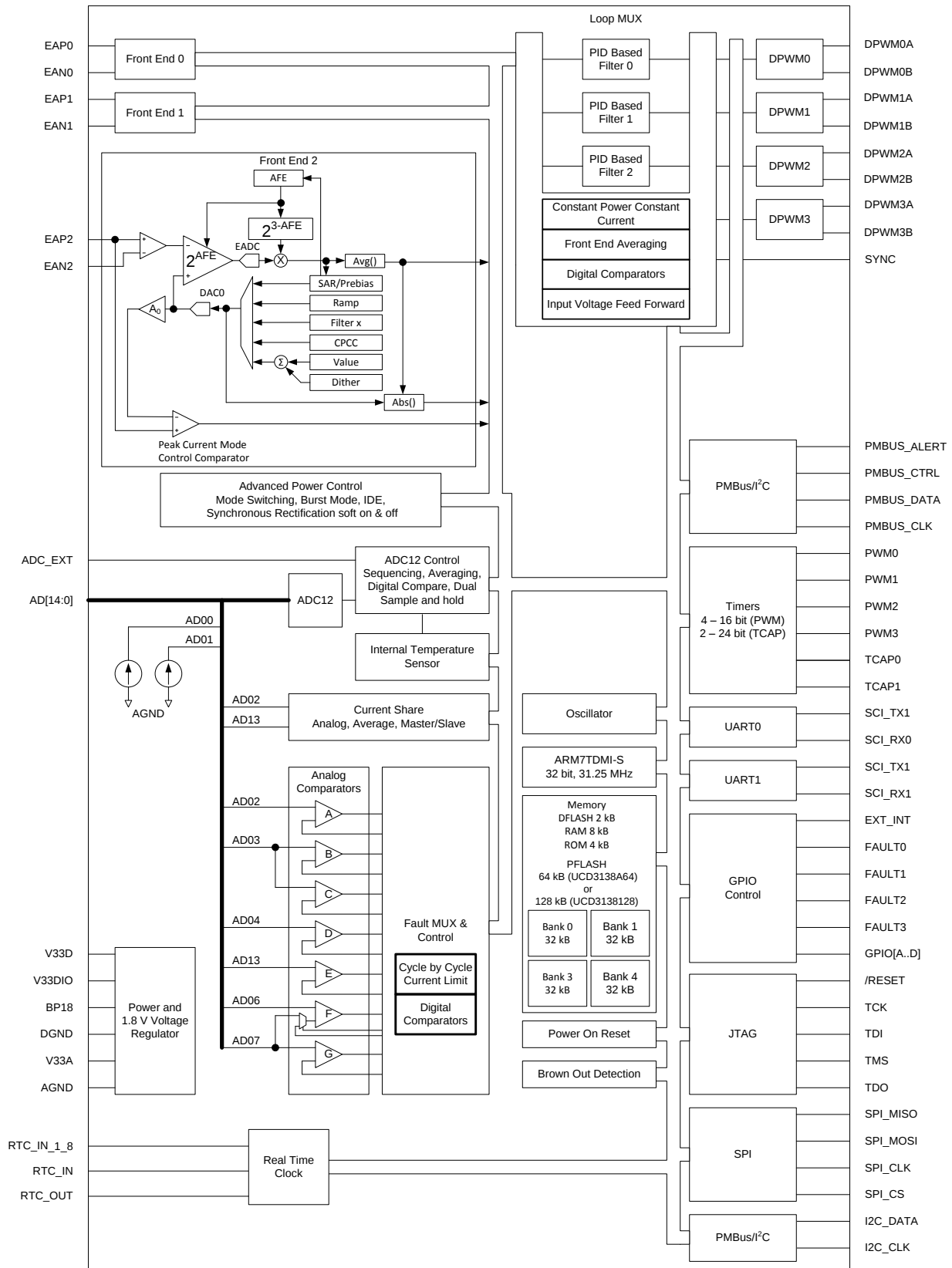
For run time data storage and scratchpad memory, a 8 kB RAM is available. The RAM is organized as a 2 k x 32 bit array.

The availability of 64 kB or 128 kB of program Flash memory in 2-32 kB or 4-32 kB banks, respectively enables the designers to implement multiple images of firmware (e.g. one main image + one back-up image) in the device and the flexibility to execute from either of the banks using appropriate algorithms. It also creates the unique opportunity for the processor to load a new program and subsequently execute that program without interrupting power delivery. This feature allows the end user to add new features to the power supply while eliminating any down-time required to load the new program.

The UCD3138128 adds two additional 32 kB program flash blocks. On the UCD3138128, the boot ROM supports a dual image configuration where each image contains 64 kB. If the first 64kB has an invalid program, the boot ROM will check for a valid program in the second 64kB and jump there. The boot ROM also supports a configuration with a single program occupying the entire 128 kB.

For the UCD3138128, on the fly updates are supported through boot ROM while UCD3138A64 on the fly updates are supported through boot flash. Detailed procedures can be found in [SLUUB54](#)

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 System Module

The System Module contains the interface logic and configuration registers to control and configure all the memory, peripherals and interrupt mechanisms. The blocks inside the system module are the address decoder, memory management controller, system management unit, central interrupt unit, and clock control unit.

9.3.1.1 Address Decoder (DEC)

The Address Decoder generates the memory selects for the FLASH, ROM and RAM arrays. The memory map addresses are selectable through configurable register settings. These memory selects can be configured from 1 kB to 16 MB. Power on reset uses the default addresses in the memory map for ROM execution, which is then configured by the ROM code to the application setup. During access to the DEC registers, a wait state is asserted to the CPU. DEC registers are only writable in the ARM privilege mode for user mode protection.

9.3.1.2 Memory Management Controller (MMC)

The MMC manages the interface to the peripherals by controlling the interface bus for extending the read and write accesses to each peripheral. The unit generates eight peripheral select lines with 1 kB of address space decoding.

9.3.1.3 System Management (SYS)

The SYS unit contains the software access protection by configuring user privilege levels to memory or peripherals modules. It contains the ability to generate fault or reset conditions on decoding of illegal address or access conditions. A clock control setup for the processor clock (MCLK) speed, is also available.

9.3.1.4 Central Interrupt Module (CIM)

The CIM accepts 32 interrupt requests for meeting firmware timing requirements. The ARM processor supports two interrupt levels: FIQ and IRQ. FIQ is the highest priority interrupt. The CIM provides hardware expansion of interrupts by use of FIQ/IRQ vector registers for providing the offset index in a vector table. This numerical index value indicates the highest precedence channel with a pending interrupt and is used to locate the interrupt vector address from the interrupt vector table. Interrupt channel 0 has the lowest precedence and interrupt channel 31 has the highest precedence. To remove the interrupt request, the firmware should clear the request as the first action in the interrupt service routine. The request channels are maskable, allowing individual channels to be selectively disabled or enabled.

Table 1. Interrupt Priority Table

NAME	MODULE COMPONENT OR REGISTER	DESCRIPTION	PRIORITY
BRN_OUT_INT	Brownout	Brownout interrupt	0 (Lowest)
EXT_INT	External Interrupts	Interrupt on external input pin	1
WDRST_INT	Watchdog Control	Interrupt from watchdog exceeded (reset)	2
WDWAKE_INT	Watchdog Control	Wake-up interrupt when watchdog equals half of set watch time	3
SCI_ERR_INT	UART or SCI Control	UART or SCI error Interrupt. Frame, parity or overrun	4
SCI_RX_0_INT	UART or SCI Control	UART0 RX buffer has a byte	5
SCI_TX_0_INT	UART or SCI Control	UART0 TX buffer empty	6
SCI_RX_1_INT	UART or SCI Control	UART1 RX buffer has a byte	7
SCI_TX_1_INT	UART or SCI Control	UART1 TX buffer empty	8
PMBUS_INT		PMBus related interrupt	9
DIG_COMP_SPI_I2C_INT	12-bit ADC Control, SPI, I ² C	Digital comparator, SPI and I ² C interrupt	10
FE0_INT	Front End 0	"Prebias complete", "Ramp Delay Complete", "Ramp Complete", "Load Step Detected", "Over-Voltage Detected", "EADC saturated"	11

Feature Description (continued)

Table 1. Interrupt Priority Table (continued)

NAME	MODULE COMPONENT OR REGISTER	DESCRIPTION	PRIORITY
FE1_INT	Front End 1	"Prebias complete", "Ramp Delay Complete", "Ramp Complete", "Load Step Detected", "Over-Voltage Detected", "EADC saturated"	12
FE2_INT	Front End 2	"Prebias complete", "Ramp Delay Complete", "Ramp Complete", "Load Step Detected", "Over-Voltage Detected", "EADC saturated"	13
PWM3_INT	16-bit Timer PWM 3	16-bit Timer PWM3 counter overflow or compare interrupt	14
PWM2_INT	16-bit Timer PWM 2	16-bit Timer PWM2 counter Overflow or compare interrupt	15
PWM1_INT	16-bit Timer PWM 1	16-bit Timer PWM1 counter overflow or compare interrupt	16
PWM0_INT	16-bit timer PWM 0	16-bit Timer PWM0 counter overflow or compare interrupt	17
OVF24_INT	24-bit Timer Control	24-bit Timer counter overflow interrupt	18
CAPTURE_1_INT	24-bit Timer Control	24-bit Timer capture 1 interrupt	19
Reserved for future use			20
CAPTURE_0_INT	24-bit Timer Control	24-bit Timer capture 0 interrupt	21
COMP_0_INT	24-bit Timer Control	24-bit Timer compare 0 interrupt	22
CPCC_RTC_INT	Constant Power Constant Current or Real Time Clock Output	Mode switched in CPCC module Flag needs to be read for details. RTC timer output generates an interrupt.	23
ADC_CONV_INT	12-bit ADC Control	ADC end of conversion interrupt	24
FAULT_INT	Fault Mux Interrupt	Analog comparator interrupts, Over-Voltage detection, Under-Voltage detection, LLM load step detection	25
DPWM3	DPWM3	Same as DPWM1	26
DPWM2	DPWM2	Same as DPWM1	27
DPWM1	DPWM1	1) Every (1-256) switching cycles 2) Fault Detection 3) Mode switching	28
DPWM0	DPWM0	Same as DPWM1	29
EXT_FAULT_INT	External Faults	Fault pin interrupt	30
SYS_SSI_INT	System Software	System software interrupt	31 (highest)

9.3.2 Peripherals

9.3.2.1 Digital Power Peripherals

At the core of the UCD3138x controller are 3 Digital Power Peripherals (DPP). Each DPP can be configured to drive from one to eight DPWM outputs. Each DPP consists of:

- Differential input error ADC (EADC) with sophisticated controls
- Hardware accelerated digital 2-pole/2-zero PID based filter
- Digital PWM module with support for a variety of topologies

These can be connected in many different combinations, with multiple filters and DPWMs. They are capable of supporting functions like input voltage feed forward, current mode control, and constant current/constant power, etc.. The simplest configuration is shown in the following figure:



9.3.2.1.1 Front End

Figure 9 shows the block diagram of the front end module. It consists of a differential amplifier, an adjustable gain error amplifier, a high speed flash analog to digital converter (EADC), digital averaging filters and a precision high resolution set point DAC reference. The programmable gain amplifier in concert with the EADC and the adjustable digital gain on the EADC output work together to provide 9 bits of range with 6 bits of resolution on the EADC output. The output of the Front End module is a 9 bit sign extended result with a gain of 1 LSB / mV. Depending on the value of AFE selected, the resolution of this output could be either 1, 2, 4 or 8 LSBs. In addition Front End 0 has the ability to automatically select the AFE value such that the minimum resolution is maintained that still allows the voltage to fit within the range of the measurement. The EADC control logic receives the sample request from the DPWM module for initiating an EADC conversion. EADC control circuitry captures the EADC-9-bit-code and strobes the filter for processing of the representative error. The set point DAC has 10 bits with an additional 4 bits of dithering resulting in an effective resolution of 14 bits. This DAC can be driven from a variety of sources to facilitate things like soft start, nested loops, etc. Some additional features include the ability to change the polarity of the error measurement and an absolute value mode which automatically adds the DAC value to the error.

It is possible to operate the controller in a peak current mode control configuration. In this mode topologies like the phase shifted full bridge converter can be controlled to maintain transformer flux balance. The internal DAC can be ramped at a synchronously controlled slew rate to achieve a programmable slope compensation. This eliminates the sub-harmonic oscillation as well as improves input voltage feed-forward performance. A0 is a unity gain buffer used to isolate the peak current mode comparator. The offset of this buffer is specified in the [Electrical Characteristics](#) table.

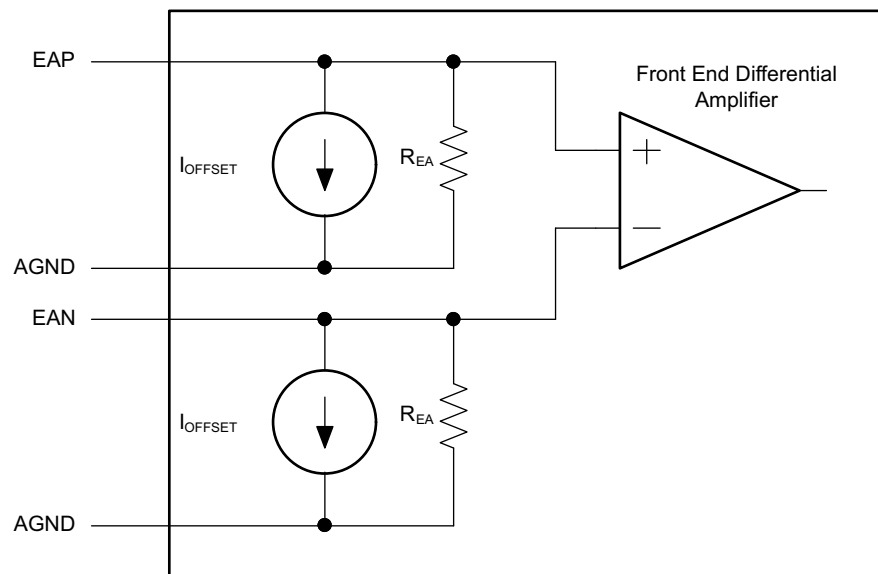


Figure 9. Input Stage Of EADC Module

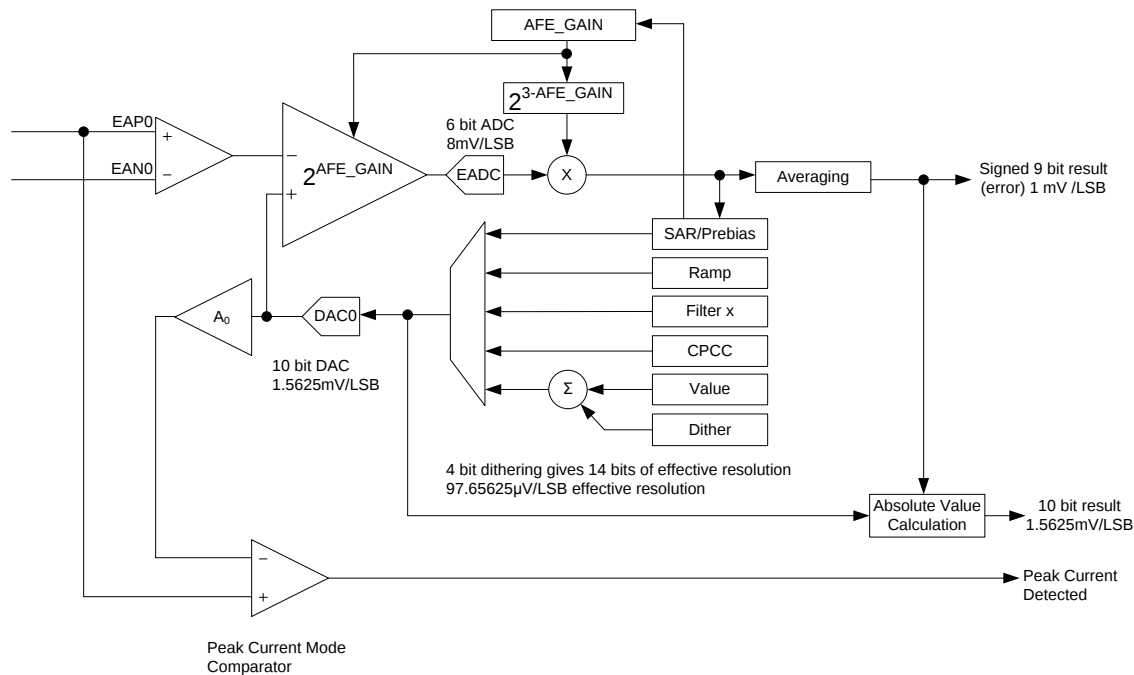


Figure 10. Front End Module

9.3.2.1.2 DPWM Module

The DPWM module represents one complete DPWM channel with 2 independent outputs, A and B. Multiple DPWM modules within the UCD3138x system can be configured to support all key power topologies. DPWM modules can be used as independent DPWM outputs, each controlling one power supply output voltage rail. It can also be used as a synchronized DPWM—with user selectable phase shift between the DPWM channels to control power supply outputs with multiphase or interleaved DPWM configurations.

The output of the filter feeds the high resolution DPWM module. The DPWM module produces the pulse width modulated outputs for the power stage switches. The filter calculates the necessary duty ratio as a 24-bit number in Q23 fixed point format (23 bit integer with 1 sign bit). This represents a value within the range 0.0 to 1.0. This duty ratio value is used to generate the corresponding DPWM output ON time. The resolution of the DPWM ON time is 250 psec.

Each DPWM module can be synchronized to another module or to an external synchronization signal. An input SYNC signal causes a DPWM ramp timer to reset. The SYNC signal outputs—from each of the four DPWM modules—occur when the ramp timer crosses a programmed threshold. This allows the phase of the DPWM outputs for multiple power stages to be tightly controlled.

The DPWM logic takes the output of the filter and converts it into the correct DPWM output for several power supply topologies. It provides for programmable dead times and cycle adjustments for current balancing between phases. It controls the triggering of the EADC. It can synchronize to other DPWMs or to external sources. It can provide synchronization information to other DPWMs or to external recipients. In addition, it interfaces to several fault handling circuits. Some of the control for these fault handling circuits is in the DPWM registers. Fault handling is covered in the Fault Mux section.

Each DPWM module supports the following features:

- Dedicated 14 bit time-base with period and frequency control
- Shadow period register for end of period updates.
- Quad-event control registers (A and B, rising and falling) (Events 1-4)
 - Used for on/off DPWM duty ratio updates.
- Phase control relative to other DPWM modules
- Sample trigger placement for output voltage sensing at any point during the DPWM cycle.
- Support for 2 independent edge placement DPWM outputs (same frequency or period setting)

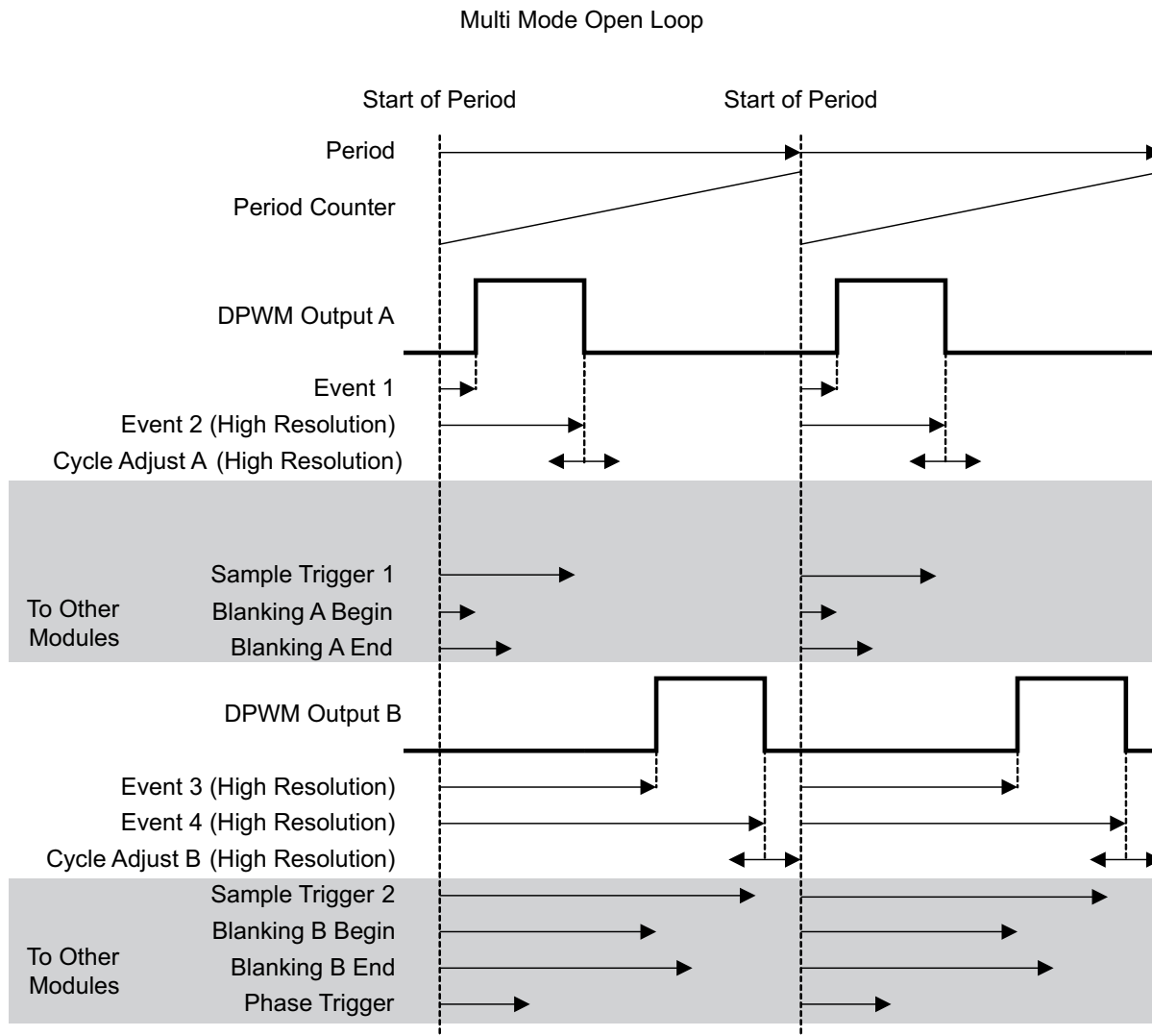
- Dead-time between DPWM A and B outputs
- High Resolution PWM capability – 250 ps
- Pulse cycle adjustment of up to $\pm 8.192 \mu\text{s}$ ($32768 \times 250 \text{ ps}$)
- Active high/ active low output polarity selection
- Provides events to trigger both CPU interrupts and start of ADC12 conversions.

9.3.2.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*—This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*—count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*—low resolution switching period count. (count of PCLK cycles)
4. *Event 1*—count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*—DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*—DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*—DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*—Constant offset for Event 2 and Event 4 adjustments.

Basic comparisons between the programmed registers and the DPWM counter can create the desired edge placements in the DPWM. High resolution edge capability is available on Events 2, 3 and 4.



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
 DPWM A Falling Edge = Event 2 + Cycle Adjust A
 DPWM B Rising Edge = Event 3
 DPWM B Falling Edge = Event 4 + Cycle Adjust B
 Phase Trigger = Phase Trigger Register value

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin,
 Blanking B End

The drawing above is for multi-mode, open loop. Open loop means that the DPWM is controlled entirely by its own registers, not by the filter output. In other words, the power supply control loop is not closed.

The Sample Trigger signals are used to trigger the Front End to sample input signals. The Blanking signals are used to blank fault measurements during noisy events, such as FET turn on and turn off. Additional DPWM modes are described below.

9.3.2.1.4 High Resolution DPWM

Unlike conventional PWM controllers where the frequency of the clock dictates the maximum resolution of PWM edges, the UCD3138x DPWM can generate waveforms with resolutions as small as 250 ps. This is 16 times the resolution of the clock driving the DPWM module.

This is achieved by providing the DPWM mechanism with 16 phase shifted clock signals of 250 MHz each.

9.3.2.1.5 Over Sampling

The DPWM module has the capability to trigger an over sampling event by initiating the EADC to sample the error voltage. The default “00” configuration has the DPWM trigger the EADC once based on the sample trigger register value. The over sampling register has the ability to trigger the sampling 2, 4 or 8 times per PWM period. Thus the time the over sample happens is at the divide by 2, 4, or 8 time set in the sampling register. The “01” setting triggers 2X over sampling, the “10” setting triggers 4X over sampling, and the “11” triggers over sampling at 8X.

9.3.2.1.6 DPWM Interrupt Generation

The DPWM has the capability to generate a CPU interrupt based on the PWM frequency programmed in the period register. The interrupt can be scaled by a divider ratio of up to 255 for developing a slower interrupt service execution loop. This interrupt can be fed to the ADC circuitry for providing an ADC12 trigger for sequence synchronization. [Table 2](#) outlines the divide ratios that can be programmed.

9.3.2.1.7 DPWM Interrupt Scaling/Range

Table 2. DPWM Interrupt Divide Ratio

INTERRUPT DIVIDE SETTING	INTERRUPT DIVIDE COUNT	INTERRUPT DIVIDE COUNT (HEX)	SWITCHING PERIOD FRAMES (assume 1MHz loop)	NUMBER OF 32 MHZ PROCESSOR CYCLES
1	0	00	1	32
2	1	01	2	64
3	3	03	4	128
4	7	07	8	256
5	15	0F	16	512
6	31	1F	32	1024
7	47	2F	48	1536
8	63	3F	64	2048
9	79	4F	80	2560
10	95	5F	96	3072
11	127	7F	128	4096
12	159	9F	160	5120
13	191	BF	192	6144
14	223	DF	224	7168
15	255	FF	256	8192

9.3.3 Automatic Mode Switching

Automatic Mode switching enables the DPWM module to switch between modes automatically, with no firmware intervention. This is useful to increase efficiency and power range. The following paragraphs describe phase-shifted full bridge and LLC examples.

9.3.3.1 Phase Shifted Full Bridge Example

In phase shifted full bridge topologies, efficiency can be increased by using pulse width modulation, rather than phase shift, at light load. This is shown below:

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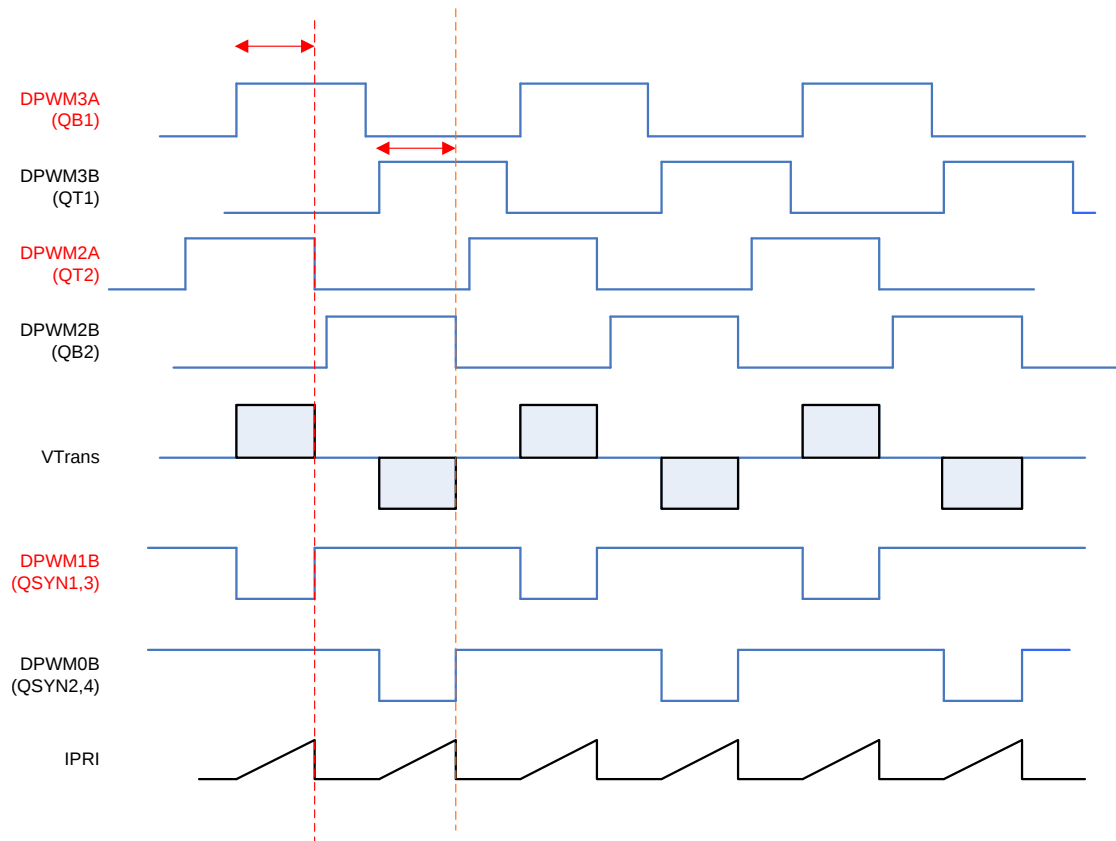


Figure 11. Phase-Shifted Full Bridge Waveforms

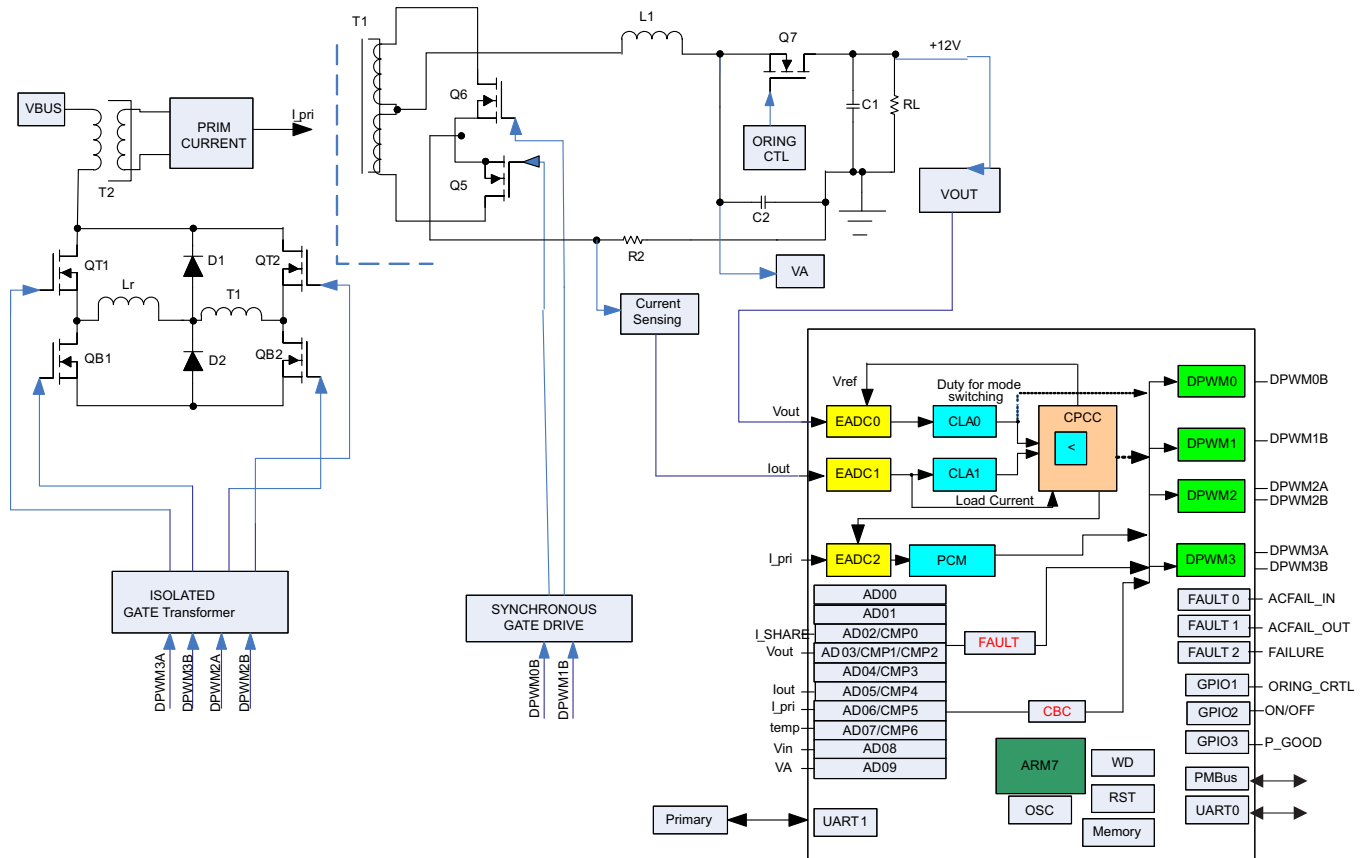


Figure 12. Secondary-Referenced Phase-Shifted Full Bridge Control With Synchronous Rectification

9.3.3.2 LLC Example

In LLC, three modes are used. At the highest frequency, a pulse width modulated mode (Multi Mode) is used. As the frequency decreases, resonant mode is used. As the frequency gets still lower, the synchronous MOSFET drive changes so that the on-time is fixed and does not increase. In addition, the LLC control supports cycle-by-cycle current limiting. This protection function operates by a comparator monitoring the maximum current during the DPWMA conduction time. Any time this current exceeds the programmable comparator reference the pulse is immediately terminated. Due to classic instability issues associated with half-bridge topologies it is also possible to force DPWMB to match the truncated pulse width of DPWMA. Here are the waveforms for the LLC:

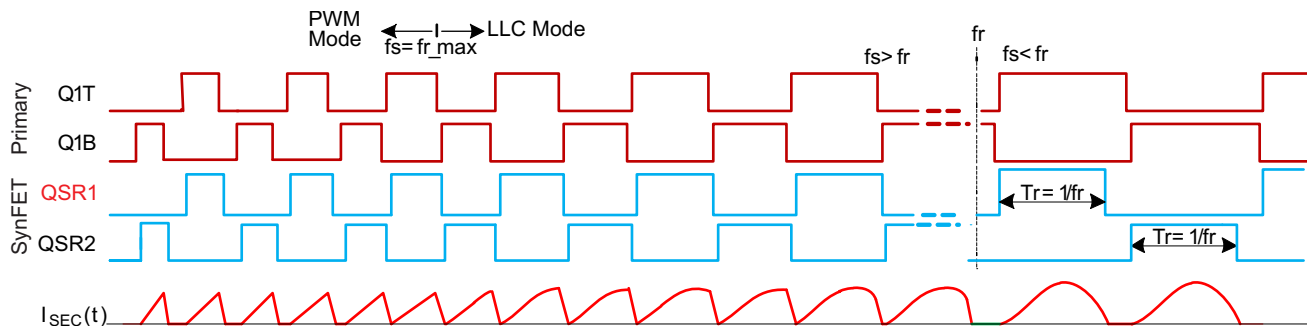


Figure 13. LLC Waveforms

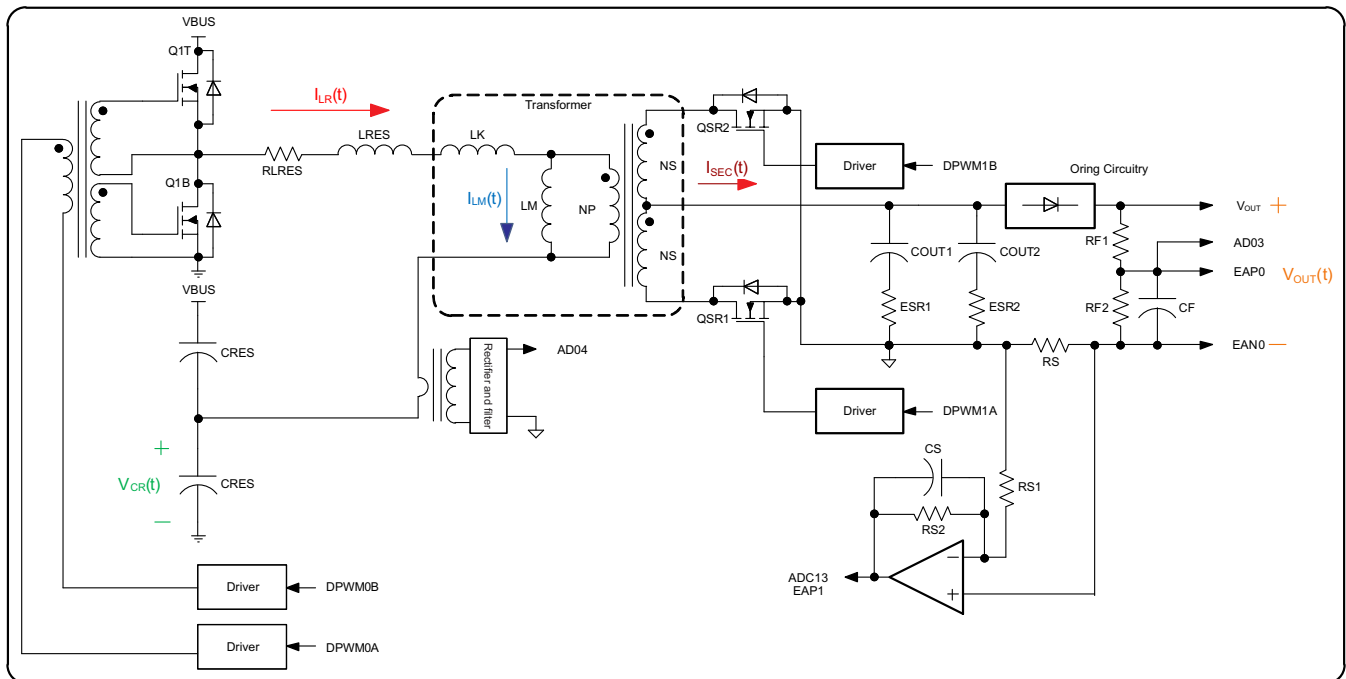


Figure 14. Secondary-Referenced Half-Bridge Resonant LLC Control With Synchronous Rectification

9.3.3.3 Mechanism For Automatic Mode Switching

The UCD3138x allows the customer to enable up to two distinct levels of automatic mode switching. These different modes are used to enhance light load operation, short circuit operation and soft start. Many of the configuration parameters for the DPWM are in DPWM Control Register 1. For automatic mode switching, some of these parameters are duplicated in the Auto Config Mid and Auto Config High registers.

If automatic mode switching is enabled, the filter duty signal is used to select which of these three registers is used. There are 4 registers which are used to select the points at which the mode switching takes place. They are used as shown below.

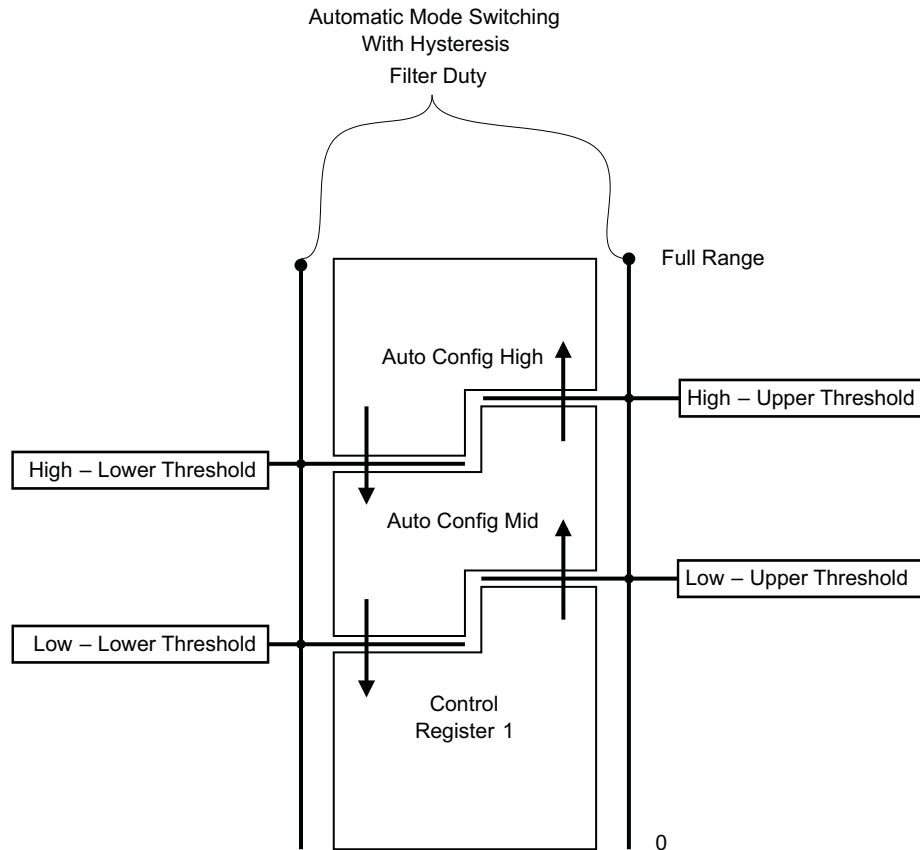


Figure 15. Automatic Mode Switching

As shown, the registers are used in pairs for hysteresis. The transition from Control Register 1 to Auto Config Mid only takes place when the Filter Duty goes above the Low Upper threshold. It does not go back to Auto Config Mid until the Low Lower Threshold is passed. This prevents oscillation between modes if the filter duty is close to a mode switching point.

9.3.4 DPWMC, Edge Generation, Intramux

The UCD3138x has hardware for generating complex waveforms beyond the simple DPWMA and DPWMB waveforms already discussed – DPWMC, the Edge Generation Module, and the IntraMux.

DPWMC is a signal inside the DPWM logic. It goes high at the Blanking A begin time, and low at the Blanking A end time.

The Edge Gen module takes DPWMA and DPWMB from its own DPWM module, and the next one, and uses them to generate edges for two outputs. For DPWM3, the DPWM0 is considered to be the next DPWM. Each edge (rising and falling for DPWMA and DPWMB) has 8 options which can cause it.

The options are:

0 = DPWM(n) A Rising edge

- 1 = DPWM(n) A Falling edge
- 2 = DPWM(n) B Rising edge
- 3 = DPWM(n) B Falling edge
- 4 = DPWM(n+1) A Rising edge
- 5 = DPWM(n+1) A Falling edge
- 6 = DPWM(n+1) B Rising edge
- 7 = DPWM(n+1) B Falling edge

Where “n” is the numerical index of the DPWM module of interest. For example n=1 refers to DPWM1.

The Edge Gen is controlled by the DPWMEDGEGEN register. It also has an enable/disable bit.

The IntraMux is controlled by the Auto Config registers. Intra Mux is short for intra multiplexer. The IntraMux takes signals from multiple DPWMs and from the Edge Gen and combines them logically to generate DPWMA and DPWMB signals. This is useful for topologies like phase-shifted full bridge, especially when they are controlled with automatic mode switching. Of course, it can all be disabled, and DPWMA and DPWMB will be driven as described in the sections above. If the Intra Mux is enabled, high resolution must be disabled, and DPWM edge resolution goes down to 4 ns.

Here is a drawing of the Edge Gen/Intra Mux:

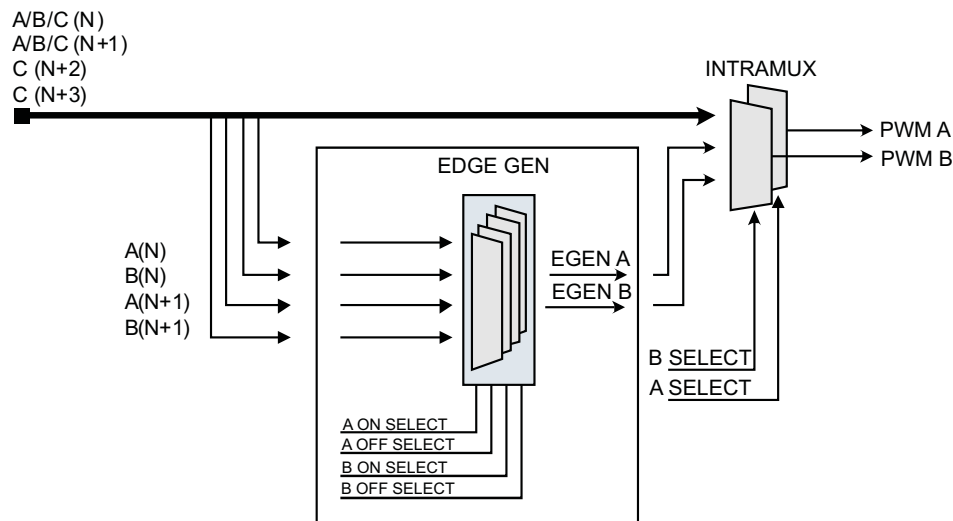


Figure 16. Edge Generation / IntraMux

Here is a list of the IntraMux modes for DPWMA:

- 0 = DPWMA(n) pass through (default)
- 1 = Edge-gen output, DPWMA(n)
- 2 = DPWNC(n)
- 3 = DPWMB(n) (Crossover)
- 4 = DPWMA(n+1)
- 5 = DPWMB(n+1)
- 6 = DPWMC(n+1)
- 7 = DPWMC(n+2)
- 8 = DPWMC(n+3)

and for DPWMB:

- 0 = DPWMB(n) pass through (default)
- 1 = Edge-gen output, DPWMB(n)
- 2 = DPWNC(n)
- 3 = DPWMA(n) (Crossover)
- 4 = DPWMA(n+1)
- 5 = DPWMB(n+1)

6 = DPWMC(n+1)

7 = DPWMC(n+2)

8 = DPWMC(n+3)

The DPWM number wraps around just like the Edge Gen unit. For DPWM3 the following definitions apply:

DPWM(n)	DPWM3
DPWM(n+1)	DPWM0
DPWM(n+2)	DPWM1
DPWM(n+3)	DPWM2

9.3.5 Filter

The UCD3138x filter is a PID filter with many enhancements for power supply control. Some of its features include:

- Traditional PID Architecture
- Programmable non-linear limits for automated modification of filter coefficients based on received EADC error
- Multiple coefficient sets fully configurable by firmware
- Full 24-bit precision throughout filter calculations
- Programmable clamps on integrator branch and filter output
- Ability to load values into internal filter registers while system is running
- Ability to stall calculations on any of the individual filter branches
- Ability to turn off calculations on any of the individual filter branches
- Duty cycle, resonant period, or phase shift generation based on filter output.
- Flux balancing
- Voltage feed forward

Here is the first section of the Filter :

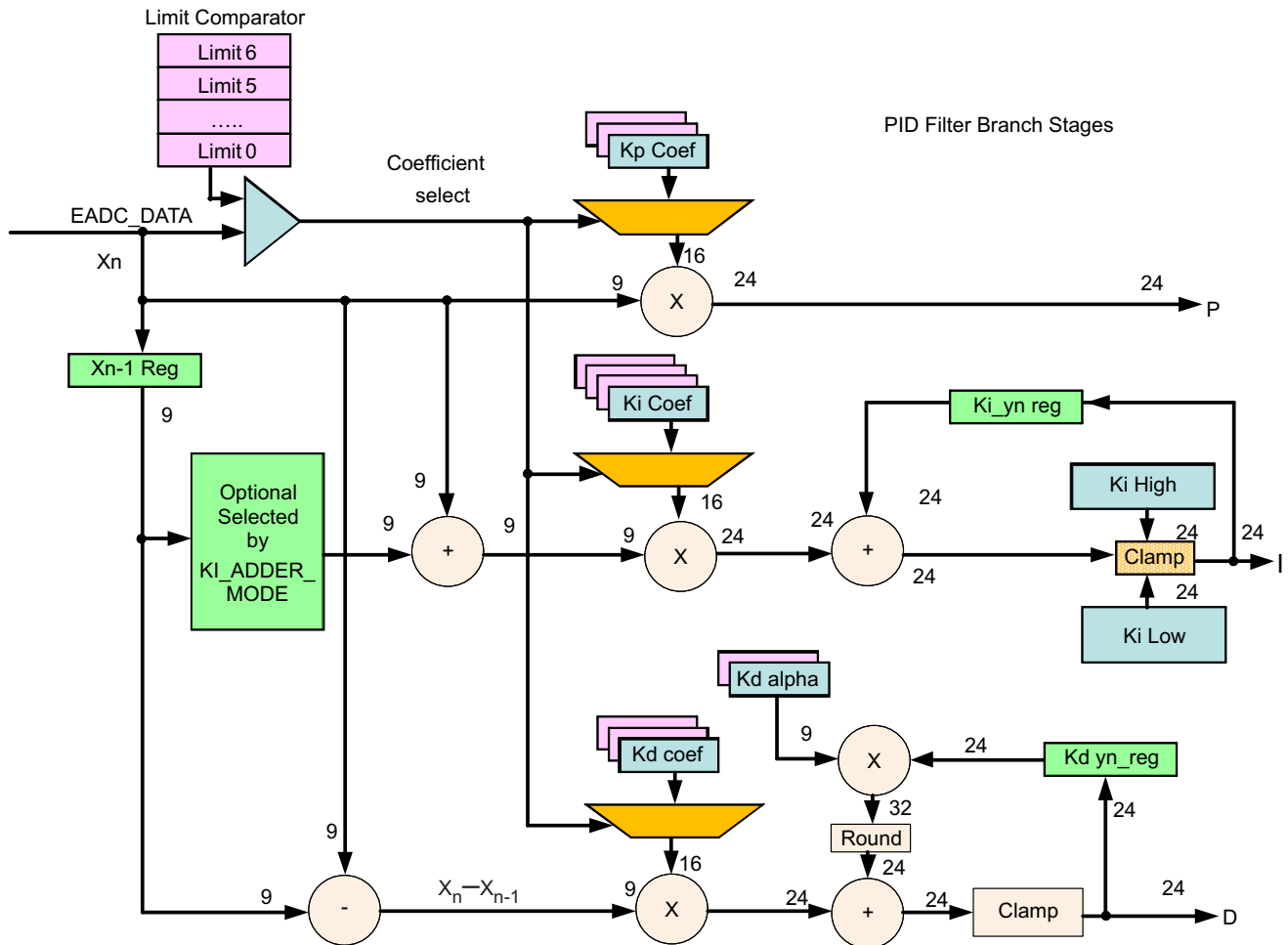


Figure 17. First Section of the Filter

The filter input, X_n , generally comes from a front end. Then there are three branches, P, I, and D. Note that the D branch also has a pole, K_d Alpha. Clamps are provided both on the I branch and on the D alpha pole.

The filter also supports a nonlinear mode, where up to 7 different sets of coefficients can be selected depending on the magnitude of the error input X_n . This can be used to increase the filter gain for higher errors to improve transient response.

Here is the output section of the filter (S0.23 means that there is 1 sign bit, 0 integer bits and 23 fractional bits):

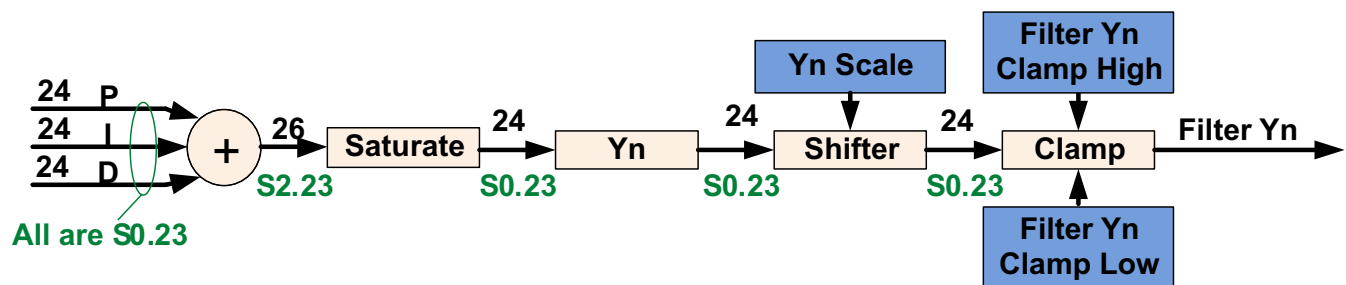


Figure 18. Output Section of the Filter

This section combines the P, I, and D sections, and provides for saturation, scaling, and clamping.

There is a final section for the filter, which permits its output to be matched to the DPWM:

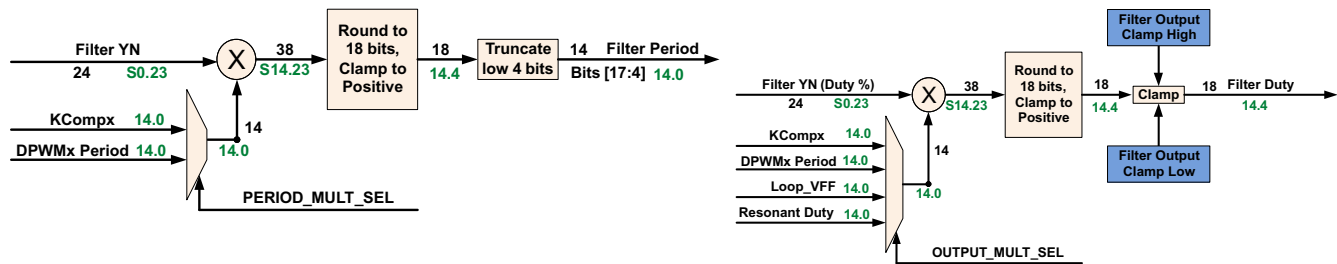


Figure 19. Final Section for the Filter

This permits the filter output to be multiplied by a variety of correction factors to match the DPWM Period, to provide for Voltage Feed Forward, or for other purposes. After this, there is another clamp. For resonant mode, the filter can be used to generate both period and duty cycle.

9.3.5.1 Loop Multiplexer

The Loop Mux controls interconnections between the filters, front ends, and DPWMs. Any filter, front end, and DPWM can be combined in a variety of configurations.

It also controls the following connections:

- DPWM to Front End
- Front End DAC control from Filters or Constant Current/Constant Power Module
- Filter Special Coefficients and Feed Forward
- DPWM synchronization
- Filter to DPWM

The following control modules are configured in the Loop Mux:

- Constant Power/Constant Current
- Cycle Adjustment (Current and flux balancing)
- Global Period
- Light Load (Burst Mode)
- Analog Peak Current Mode

9.3.5.2 Fault Multiplexer

In order to allow a flexible way of mapping several fault triggering sources to all the DPWMs channels, the UCD3138x provides an extensive array of multiplexers that are united under the name Fault Mux module.

The Fault Mux Module supports the following types of mapping between all the sources of fault and all the different fault response mechanisms inside each DPWM module.

- Many fault sources may be mapped to a single fault response mechanism. For instance an analog comparator in charge of over voltage protection, a digital comparator in charge of over current protection and an external digital fault pin can be all mapped to a Fault-A signal connected to a single FAULT MODULE and shut down DPWM1-A.
- A single fault source can be mapped to many fault response mechanisms inside many DPWM modules. For instance an analog comparator in charge of over current protection can be mapped to DPWM-0 through DPWM-3 by way of several fault modules.
- Many fault sources can be mapped to many fault modules inside many DPWM modules.

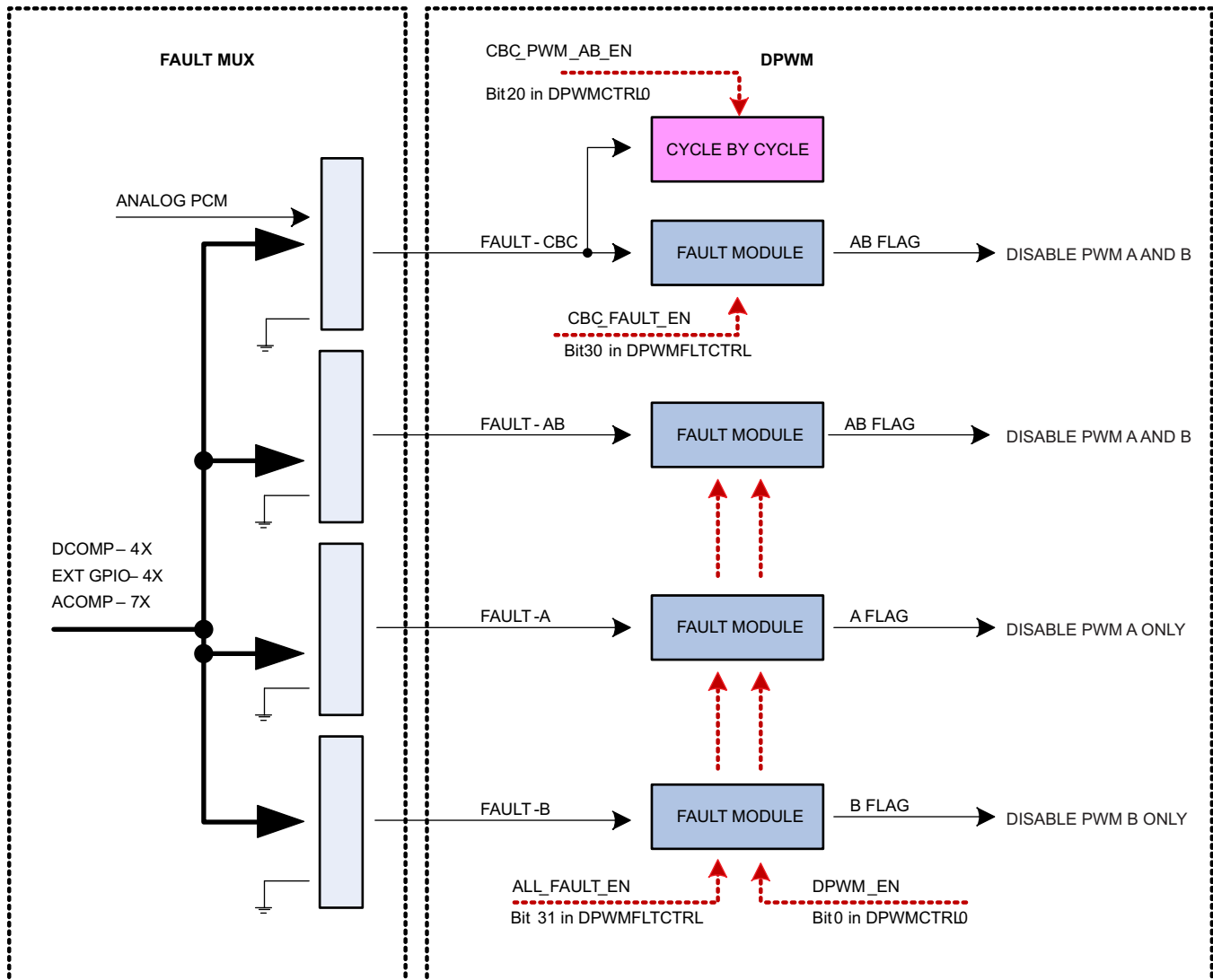


Figure 20. Fault Mux Module

The Fault Mux Module provides a multitude of fault protection functions within the UCD3138x high-speed loop (Front End Control, Filter, DPWM and Loop Mux modules). The Fault Mux Module allows highly configurable fault generation based on digital comparators, high-speed analog comparators and external fault pins. Each of the fault inputs to the DPWM modules can be configured to one or any combination of the fault events provided in the Fault Mux Module.

Each one of the DPWM engines has four fault modules. The modules are called CBC fault module, AB fault module, A fault module and B fault module.

The internal circuitry in all the four fault modules is identical, and the difference between the modules is limited to the way the modules are attached to the DPWMs.

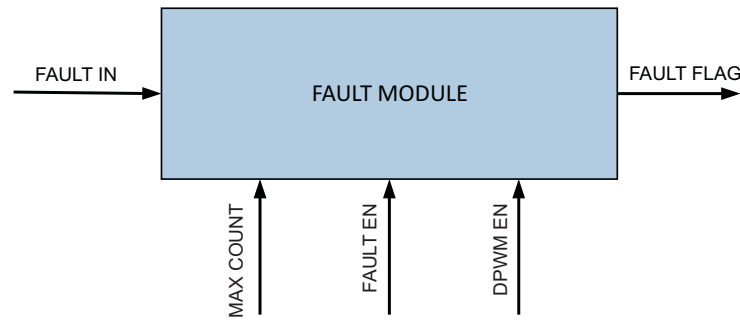


Figure 21. Fault Module

All fault modules provide immediate fault detection but only once per DPWM switching cycle. Each one of the fault modules own a separate max_count and the fault flag will be set only if sequential cycle-by-cycle fault count exceeds max_count.

Once the fault flag is set, DPWMs need to be disabled by DPWM_EN going low in order to clear the fault flags. Please note, all four Fault Modules share the same DPWM_EN control, all fault flags (output of Fault Modules) will be cleared simultaneously.

All four Fault Modules share the same global FAULT_EN as well. Therefore a specific Fault Module cannot be enabled/ disabled separately.

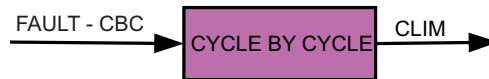


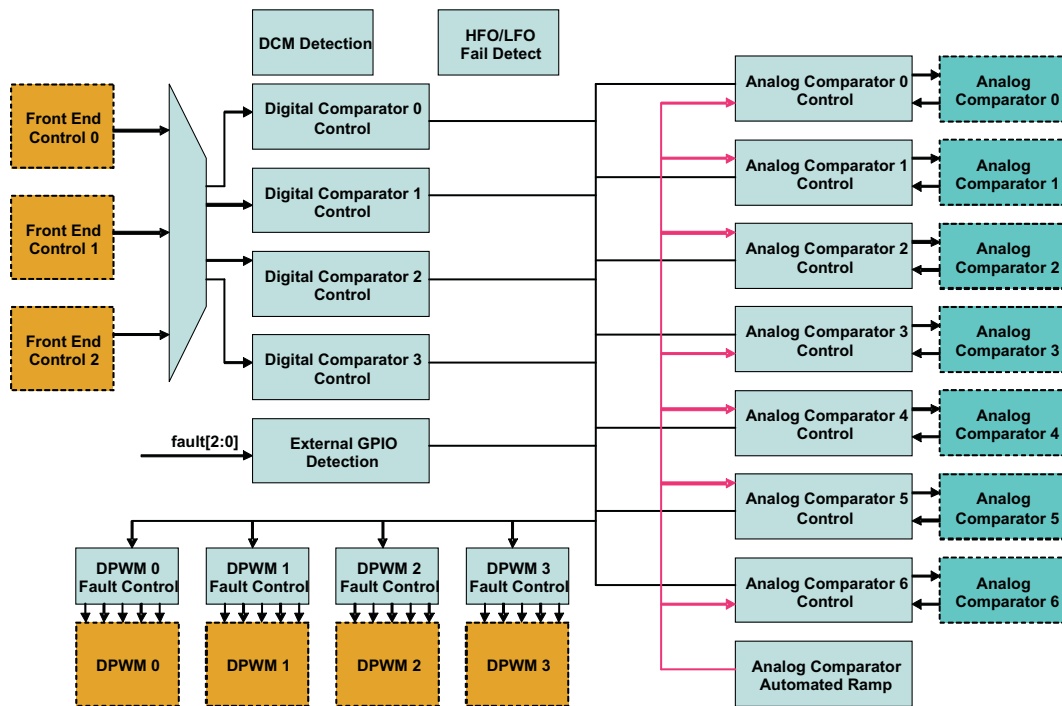
Figure 22. Cycle-By-Cycle Block

Unlike Fault Modules, only one Cycle by Cycle block is available in each DPWM module.

The Cycle by Cycle block works in conjunction with CBC Fault Module and enables DPWM reaction to signals arriving from the Analog Peak current mode (PCM) module.

The Fault Mux Module supports the following basic functions:

- 4 digital comparators with programmable thresholds and fault generation
- Configuration for 7 high speed analog comparators with programmable thresholds and fault generation
- External GPIO detection control with programmable fault generation
- Configurable DPWM fault generation for DPWM Current Limit Fault, DPWM Over-Voltage Detection Fault, DPWM A External Fault, DPWM B External Fault and DPWM IDE Flag
- Clock Failure Detection for High and Low Frequency Oscillator blocks
- Discontinuous Conduction Mode Detection


Figure 23. Fault Mux Block Diagram

9.3.6 Communication Ports

9.3.6.1 SCI (UART) Serial Communication Interface

A maximum of two independent Serial Communication Interface (SCI) or Universal Asynchronous Receiver/Transmitter (UART) interfaces are included within the device for asynchronous start-stop serial data communication (see the pin out sections for details). Each interface has a 24 bit pre-scaler for supporting programmable baud rates, a programmable data word and stop bit options. Half or full duplex operation is configurable through register bits. A loop back feature can also be setup for firmware verification. Both SCI-TX and SCI-RX pin sets can be used as GPIO pins when the peripheral is not being used.

9.3.6.2 PMBus/I²C

The UCD3138x has two independent interfaces which both support PMBus and I²C in master and slave modes. Only one of the interfaces has control of the address pin current sources as well as support for the optional Control and Alert lines described in the PMBus specification. Other than these differences, the interfaces are identical.

The PMBus/I²C interface is designed to minimize the processor overhead required for interface. It can automatically detect and acknowledge addresses. It handles start and stop conditions automatically, and can clock stretch until the processor has time to poll the PMBus status. It will automatically receive and send up to 4 bytes at a time. It can automatically verify and generate a PEC. This means that a write byte command can be received by the processor with only one function call. There is no need for any interrupts at all with this PMBus/I²C interface. If it is polled every few milliseconds, it will work perfectly.

The interface also supports automatic ACK of two independent addresses. If both PMBus/I²C interfaces are used at the same time a total of 4 independent addresses can be automatically detected.

Example: PMBus Address Decode via ADC12 Reading

The user can allocate 2 pins of the 12-bit ADC input channels, AD_00 and AD_01, for PMBus address decoding. At power-up the device applies I_{BIAS} to each address detect pin and the voltage on that pin is captured by the internal 12-bit ADC.

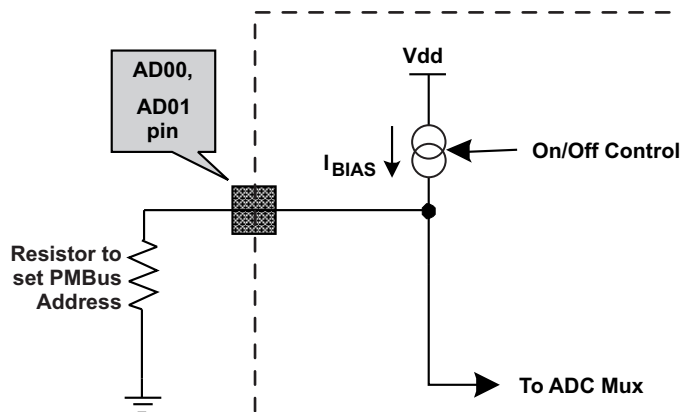


Figure 24. PMBUS Address Detection Method

PMBus/I²C address 0x7E is a reserved address and should not be used in a system using the UCD3138x. This address is used for manufacturing test.

9.3.6.3 SPI

The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the UCD3138x and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters. The SPI allows serial communication with other SPI devices through a 3-pin or 4-pin mode interface. The SPI typically is configured as a master for communicating to external EEPROM.

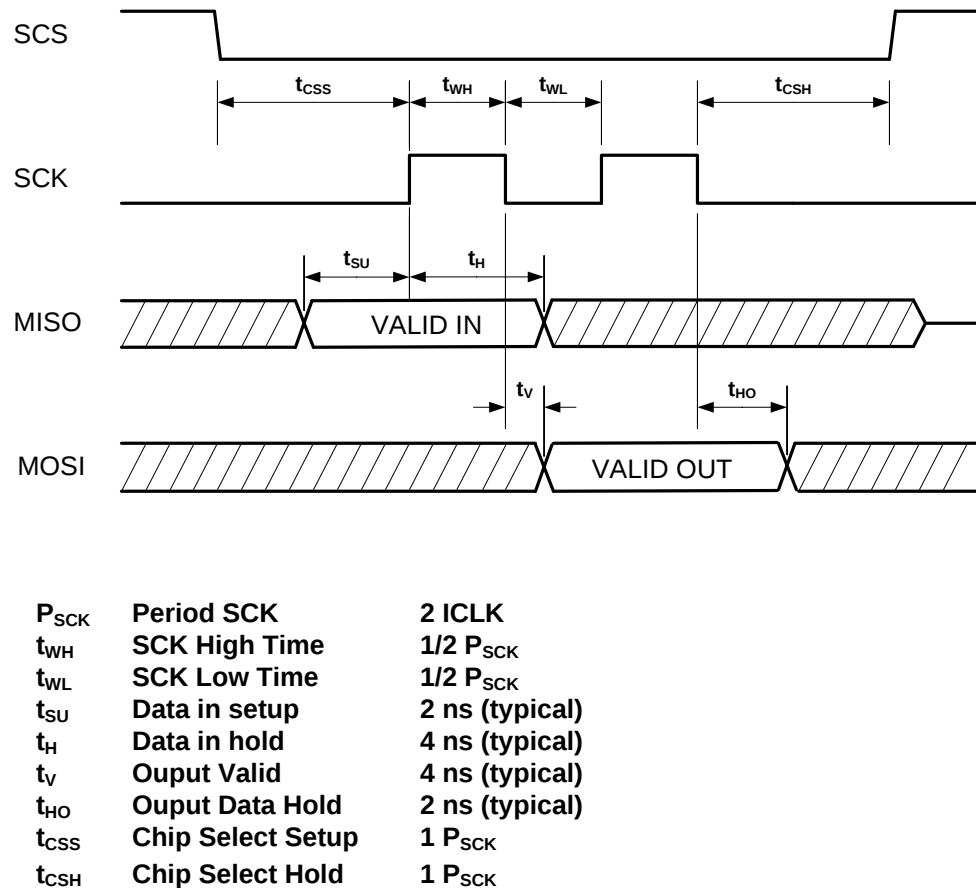


Figure 25. SPI Timing Diagram

9.3.7 Real Time Clock

The UCD3138x has an internal real time clock (RTC) function that can track time in seconds, minutes, hours and days. This function requires an external precision 10 MHz clock.

- Firmware writable time/day register which tracks the total number of days.
 - The day counter will be able to count 4 years worth of days.
 - Years and months and leap year calculation must be calculated in firmware.
- Firmware programmable frequency correction of ± 200 ppm in 0.8 ppm steps
- The RTC function can provide interrupts to the IRQ or FIQ at 1, 10, 30, and 60 second intervals.
- The clock from the RTC driver can be driven to an external pin through an internal multiplexor
- The clock for the RTC function can come from an external clock through a dedicated GPIO pin.

9.3.8 Timers

External to the Digital Power Peripherals there are 3 different types of timers in UCD3138x. They are the 24-bit timer, 16-bit timer and the watchdog timer

9.3.8.1 24-Bit Timer

There is one 24 bit timer which runs off the Interface Clock. It can be used to measure the time between two events, and to generate interrupts after a specific interval. Its clock can be divided down by an 8-bit pre-scalar to provide longer intervals. The timer has two compare registers (Data Registers). Both can be used to generate an interrupt after a time interval. Additionally, the timer has a shadow register (Data Buffer register) which can be used to store CPU updates of the compare events while still using the timer. The selected shadow register update mode happens after the compare event matches.

The two capture pins TCAP0 and TCAP1 are inputs for recording a capture event. A capture event can be set either to rising, falling, or both edges of the capture pin signal. Upon this event, the counter value is stored in the corresponding capture data register. Five Interrupts from the 24 bit timer can be set, which are the counter rollover event (overflow), capture events 0 and 1, and the two comparison match events. Each interrupt can be disabled or enabled.

9.3.8.2 16-Bit PWM Timers

There are four 16 bit counter PWM timers which run off the Interface Clock and can further be divided down by a 8-bit pre-scaler to generate slower PWM time periods. Each timer has two compare registers (Data Registers) for generating the PWM set/unset events. Additionally, each timer has a shadow register (Data Buffer register) which can be used to store CPU updates of compare events while still using the timer. The selected shadow register update mode happens after the compare event matches.

The counter reset can be configured to happen on a counter roll over, a compare equal event, or by a software controlled register. Interrupts from the PWM timer can be set due to the counter rollover event (overflow) or by the two comparison match events. Each comparison match and the overflow interrupts can be disabled or enabled.

Upon an event comparison, the PWM pin can be configured to set, clear, toggle or have no action at the output. The value of PWM pin output can be read for status or simply configured as General Purpose I/O for reading the value of the input at the pin.

9.3.8.3 Watchdog Timer

A watchdog timer is provided on the device for ensuring proper firmware loop execution. The timer is clocked off of a separate low speed oscillator source. If the timer is allowed to expire, a reset condition is issued to the ARM processor. The watchdog is reset by a simple CPU write bit to the watchdog key register by the firmware routine. On device power-up the watchdog is disabled. Yet after it is enabled, the watchdog cannot be disabled by firmware. Only a device reset can put this bit back to the default disabled state. A half timer flag is also provided for status monitoring of the watchdog.

9.3.9 General Purpose ADC12

The ADC12 is a 12 bit, high speed analog to digital converter, equipped with the following options:

- Typical conversion speed of 267 ksp/s
- Conversions can consist from 1 to 16 ADC channel conversions in any desired sequence
- Post conversion averaging capability, ranging from 4X, 8X, 16X or 32X samples
- Configurable triggering for ADC conversions from the following sources: firmware, DPWM rising edge, ADC_EXT_TRIG pin or Analog Comparator results
- Interrupt capability to embedded processor at completion of ADC conversion
- Six digital comparators on the first 6 channels of the conversion sequence using either raw ADC data or averaged ADC data
- Two 10 μ A current sources for excitation of PMBus addressing resistors
- Dual sample and hold for accurate power measurement
- Internal temperature sensor for temperature protection and monitoring

The control module ([ADC12 Control Block Diagram](#)) contains the control and conversion logic for auto-sequencing a series of conversions. The sequencing is fully configurable for any combination of 16 possible ADC channels through an analog multiplexer embedded in the ADC12 block. Once converted, the selected channel value is stored in the result register associated with the sequence number. Input channels can be sampled in any desired order or programmed to repeat conversions on the same channel multiple times during a conversion sequence. Selected channel conversions are also stored in the result registers in order of conversion, where the result 0 register is the first conversion of a 16-channel sequence and result 15 register is the last conversion of a 16-channel sequence. The number of channels converted in a sequence can vary from 1 to 16.

Unlike EADC0 through EADC2, which are primarily designed for closing high speed compensation loops, the ADC12 is not usually used for loop compensation purposes. The EADC converters have a substantially faster conversion rate, thus making them more attractive for closed loop control. The ADC12 features make it best suited for monitoring and detection of currents, voltages, temperatures and faults. Please see the [Typical Characteristics plots](#) for the temperature variation associated with this function.

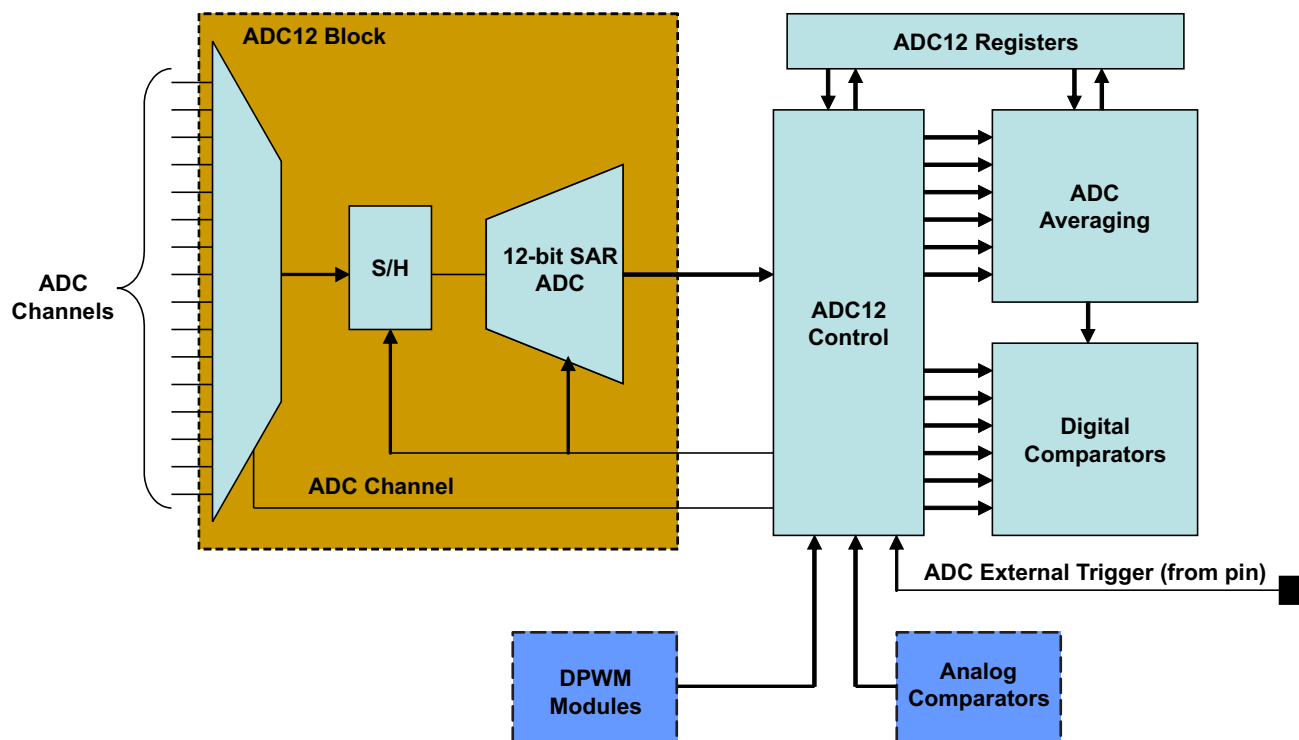


Figure 26. ADC12 Control Block Diagram

9.3.10 Miscellaneous Analog

The Miscellaneous Analog Control (MAC) Registers are a catch-all of registers that control and monitor a wide variety of functions. These functions include device supervisory features such as Brown-Out and power saving configuration, general purpose input/output configuration and interfacing, internal temperature sensor control and current sharing control.

The MAC module also provides trim signals to the oscillator and AFE blocks. These controls are usually used at the time of trimming at manufacturing; therefore this document will not cover these trim controls.

9.3.11 Brownout

Brownout function is used to determine if the device supply voltage is lower than a threshold voltage, a condition that may be considered unsafe for proper operation of the device.

The brownout threshold is higher than the reset threshold voltage; therefore, when the supply voltage is lower than brownout threshold, it still does not necessarily trigger a device reset.

The brownout interrupt flag can be polled or alternatively can trigger an interrupt to service such case by an interrupt service routine. Please see the [Power On Reset \(POR\) / Brown Out Reset \(BOR\)](#) section.

9.3.12 Global I/O

Up to 32 pins in UCD3138x can be configured in the Global I/O register to serve as a general purpose input or output pins (GPIO). This includes all digital input or output pins except for the RESET pin.

The pins that cannot be configured as GPIO pins are the supply pins, ground pins, ADC-12 analog input pins, EADC analog input pins and the RESET pin. Additional digital pins not listed in this register can be configured through their local configuration registers.

There are two ways to configure and use the digital pins as GPIO pins:

1. Through the centralized Global I/O control registers.
2. Through the distributed control registers in the specific peripheral that shares it pins with the standard GPIO functionality.

The Global I/O registers offer full control of:

1. Configuring each pin as a GPIO.
2. Setting each pin as input or output.
3. Reading the pin's logic state, if it is configured as an input pin.
4. Setting the logic state of the pin, if it is configured as an output pin.
5. Connecting pin/pins to high rail through internal push/pull drivers or external pull up resistors.

The Global I/O registers include Global I/O EN register, Global I/O OE Register, Global I/O Open Drain Control Register, Global I/O Value Register and Global I/O Read Register.

The following is showing the format of Global I/O EN Register (GLBIOEN) as an example:

BIT NUMBER	31:0
Bit Name	GLOBAL_IO_EN
Access	R/W
Default	0000_0000_0000_0000_0000_0000_0000_0000

Bits 29-0: GLOBAL_IO_EN – This register enables the global control of digital I/O pins

0 = Control of IO is done by the functional block assigned to the IO (Default)

1 = Control of IO is done by Global IO registers.

BIT	PIN_NAME	PIN NUMBER
		UCD3138x
31	PWM2	11
30	PWM3	12
29	FAULT3	55
28	ADC_EXT_TRIG	14
27	TCK	45
26	TDO	46
25	TMS	48
24	TDI	47
23	SCI_TX1	37
22	SCI_TX0	35
21	SCI_RX1	38
20	SCI_RX0	36
19	TCAP0	49
18	PWM1	40
17	PWM0	39
16	TCAP1	13
15	I2C_DATA	20
14	PMBUS_CTRL	18
13	PMBUS_ALERT	17
12	EXT_INT	42
11	FAULT2	54
10	FAULT1	44
9	FAULT0	43
8	SYNC	34
7	DPWM3B	29
6	DPWM3A	28
5	DPWM2B	27
4	DPWM2A	26
3	DPWM1B	25
2	DPWM1A	24
1	DPWM0B	23
0	DPWM0A	22

9.3.13 Temperature Sensor Control

Temperature sensor control register provides internal temperature sensor enabling and trimming capabilities. The internal temperature sensor is disabled by default.

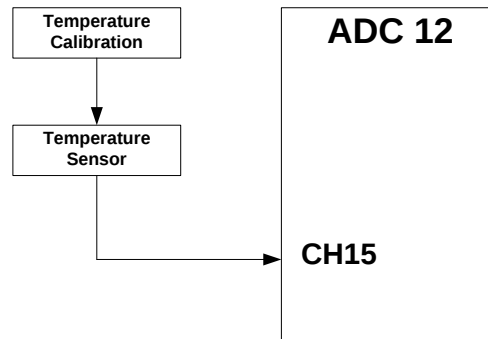


Figure 27. Internal Temp Sensor

Temperature sensor is calibrated at room temperature (25 °C) via a calibration register value.

The temperature sensor is measured using ADC12 (via Ch15). The temperature is then calculated using a mathematical formula involving the calibration register (this effectively adds a delta to the ADC measurement).

The temperature sensor can be enabled or disabled.

9.3.14 I/O Mux Control

I/O Mux Control register may be used in order to choose a single specific functionality that is desired to be assigned to a physical device pin for your application. See the UCD3138x programmer's manual for details on the available configurations.

9.3.15 Current Sharing Control

UCD3138x provides three separate modes of current sharing operation.

- Analog bus current sharing
- PWM bus current sharing
- Master/Slave current sharing
- AD02 has a special ESD protection mechanism that prevents the pin from pulling down the current-share bus if power is missing from the UCD3138x

The simplified current sharing circuitry is shown in the drawing below. The digital pulse connected to SW3 transforms SW3 into a pulse-width-modulated current source. Details on the frequency and resolution of this feature are in the digital power fusion peripherals manual.

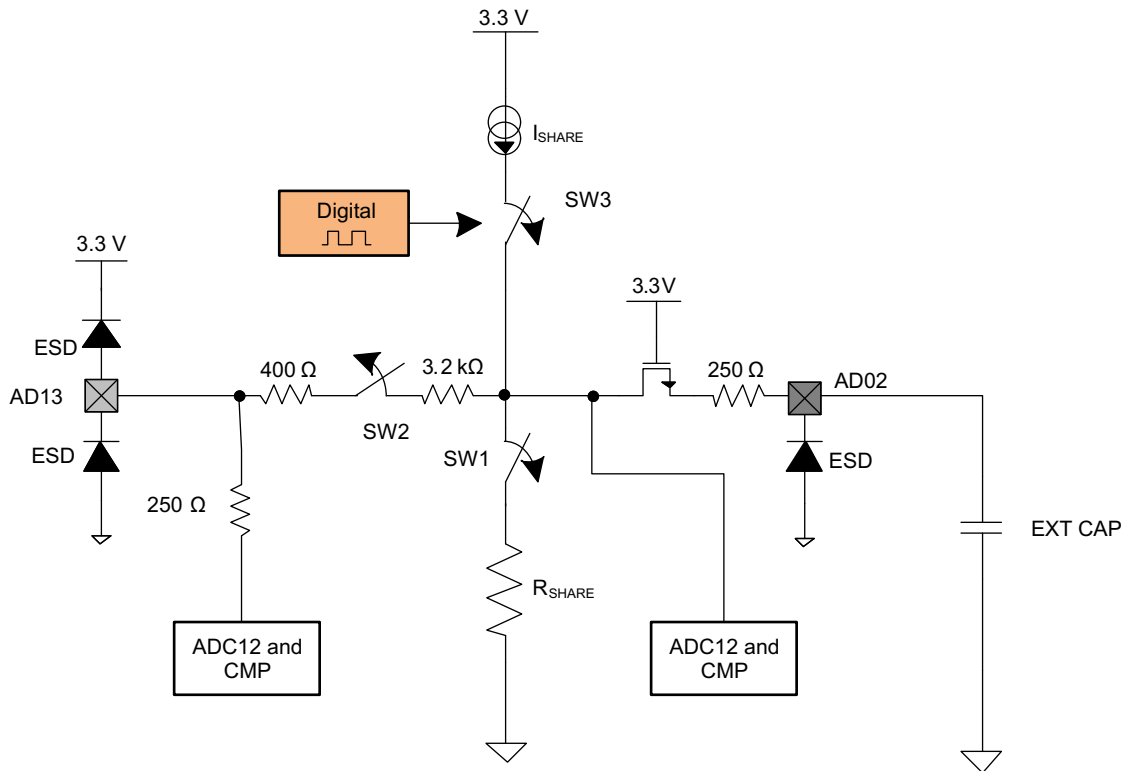


Figure 28. Simplified Current Sharing Circuitry

CURRENT SHARING MODE	FOR TEST ONLY, ALWAYS KEEP 00	CS_MODE	EN_SW1	EN_SW2	DPWM
Off or Slave Mode (3-state)	00	00 (default)	0	0	0
PWM Bus	00	01	1	0	ACTIVE
Off or Slave Mode (3-state)	00	10	0	0	0
Analog Bus or Master	00	11	0	1	0

The period and the duty of 8-bit PWM current source and the state of the SW1 and SW2 switches can be controlled through the current sharing control register (CSCTRL).

9.3.16 Temperature Reference

The temperature reference register (TEMPREF) provides the ADC12 count when ADC12 measures the internal temperature sensor (channel 15) during the factory trim and calibration.

This information can be used by different periodic temperature compensation routines implemented in the firmware. But it should not be overwritten by firmware, otherwise this factory written value will be lost until the device is reset.

9.4 Device Functional Modes

9.4.1 DPWM Modes Of Operation

The DPWM is a complex logic system which is highly configurable to support several different power supply topologies. The discussion below will focus primarily on waveforms, timing and register settings, rather than on logic design.

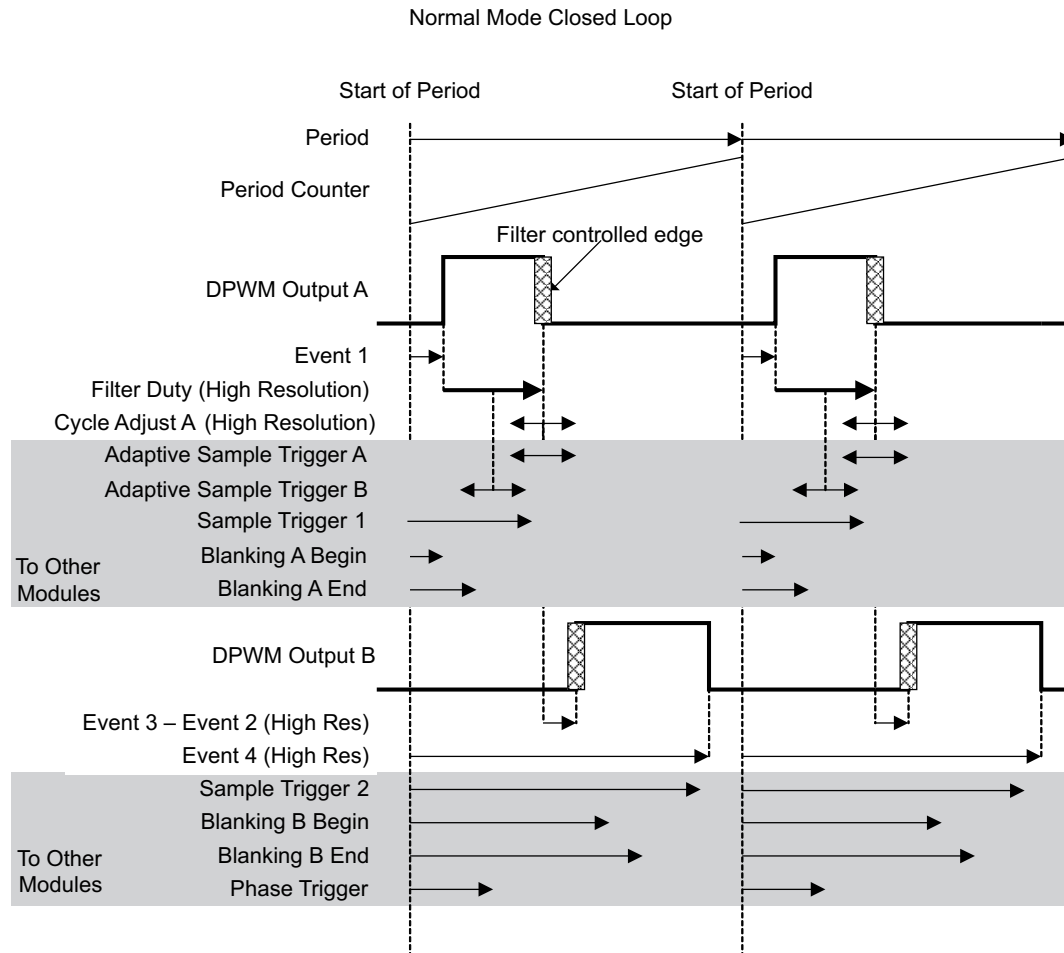
The DPWM is centered on a period counter, which counts up from 0 to PRD, and then is reset and starts over again.

The DPWM logic causes transitions in many digital signals when the period counter hits the target value for that signal.

9.4.1.1 Normal Mode

In Normal mode, the Filter output determines the pulse width on DPWM A. DPWM B fits into the rest of the switching period, with a dead time separating it from the DPWM A on-time. It is useful for buck topologies, among others. Here is a drawing of the Normal Mode waveforms:

Device Functional Modes (continued)



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
 DPWM A Falling Edge = Event 1 + Filter Duty + Cycle Adjust A
 Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register or
 Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
 DPWM B Rising Edge = Event 1 + Filter Duty + Cycle Adjust A + (Event 3 – Event 2)
 DPWM B Falling Edge = Event 4
 Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

Figure 29. Normal Mode - Closed Loop

Cycle adjust A can be used to adjust pulse widths on individual phases of a multi-phase system. This can be used for functions like current balancing. The Adaptive Sample Triggers can be used to sample in the middle of the on-time (for an average output), or at the end of the on-time (to minimize phase delay) The Adaptive Sample Register provides an offset from the center of the on-time. This can compensate for external delays, such as MOSFET and gate driver turn on times.

Blanking A-Begin and Blanking A-End can be used to blank out noise from the MOSFET turn on at the beginning of the period (DPWMA rising edge). Blanking B could be used at the turn off time of DPWMB. The other edges are dynamic, so blanking is more difficult.

Device Functional Modes (continued)

Cycle Adjust B has no effect in Normal Mode.

9.4.1.2 Phase Shifting

In most modes, it is possible to synchronize multiple DPWM modules using the phase shift signal. The phase shift signal has two possible sources. It can come from the Phase Trigger Register. This provides a fixed value, which is useful for an application like interleaved PFC.

The phase shift value can also come from the filter output. In this case, the changes in the filter output causes changes in the phase relationship of two DPWM modules. This is useful for phase shifted full bridge topologies.

The following figure shows the mechanism of phase shift:

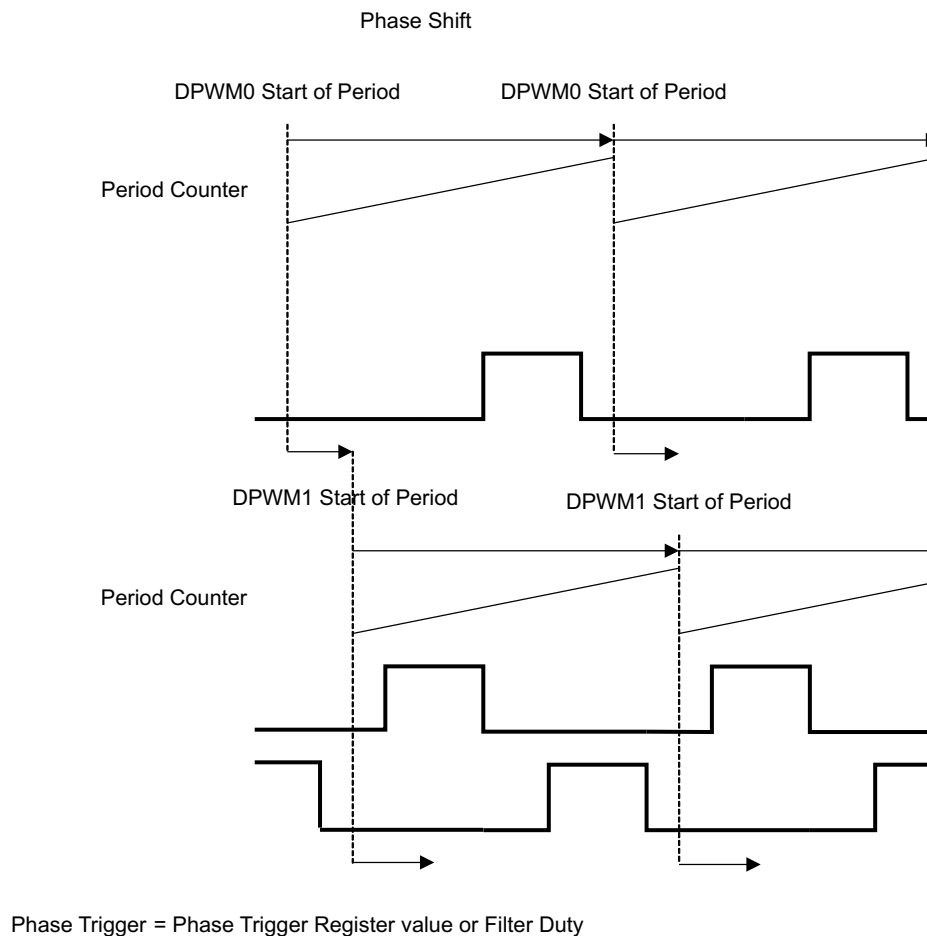


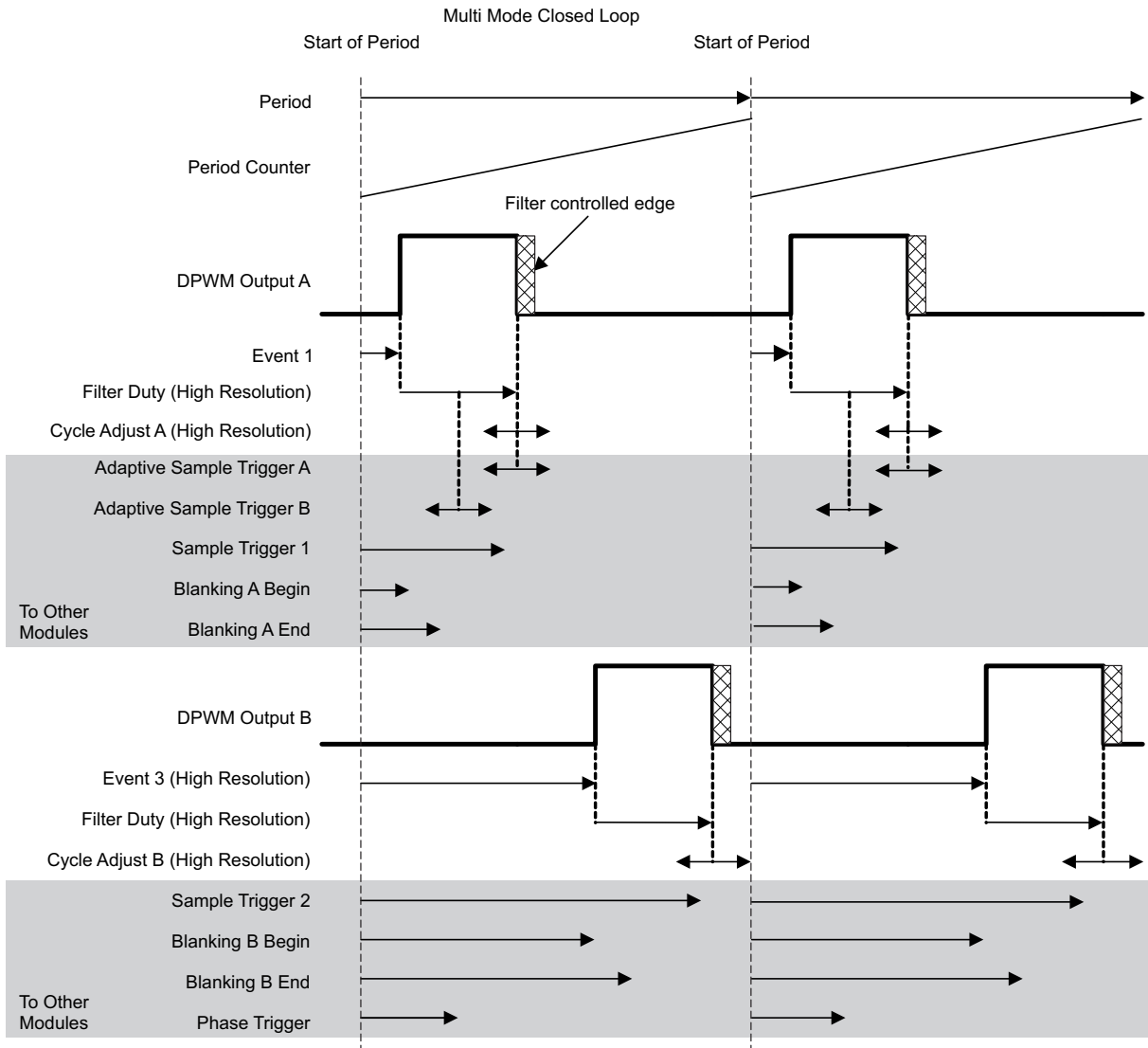
Figure 30. Phase Shifting

Device Functional Modes (continued)

9.4.1.3 DPWM Multiple Output Mode

Multi mode is used for systems where each phase has only one driver signal. It enables each DPWM peripheral to drive two phases with the same pulse width, but with a time offset between the phases, and with different cycle adjusts for each phase.

The Multi-Mode diagram is shown in [Figure 31](#).



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
 DPWM A Falling Edge = Event 1 + Filter Duty + Cycle Adjust A
 Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register or
 Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
 DPWM B Rising Edge = Event 3
 DPWM B Falling Edge = Event 3 + Filter Duty + Cycle Adjust B
 Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

Figure 31. DPWM Multi-Mode Close Loop

Device Functional Modes (continued)

Event 2 and Event 4 are not relevant in Multi mode.

DPWMB can cross over the period boundary safely, and still have the proper pulse width, so full 100% pulse width operation is possible. DPWMA cannot cross over the period boundary.

Since the rising edge on DPWM B is also fixed, Blanking B-Begin and Blanking B-End can be used for blanking this rising edge.

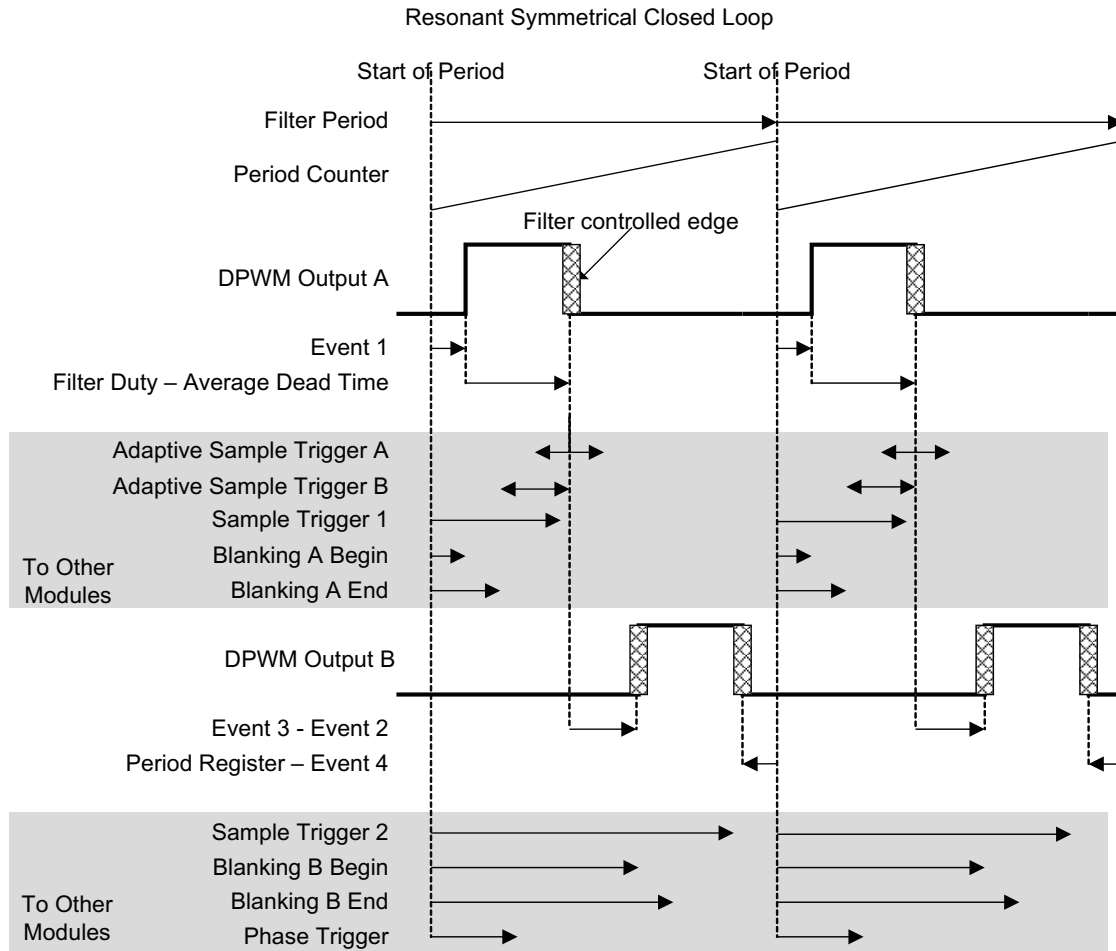
And, of course, Cycle Adjust B is usable on DPWM B.

9.4.1.4 DPWM Resonant Mode

This mode provides a symmetrical waveform where DPWMA and DPWMB have the same pulse width. As the switching frequency changes, the dead times between the pulses remain the same.

The equations for this mode are designed for a smooth transition from PWM mode to resonant mode, as described in the [LLC Example](#) section. Here is a diagram of this mode:

Device Functional Modes (continued)



Events which change with DPWM mode:

Dead Time 1 = Event 3 – Event 2

Dead Time 2 = Event 1 + Period Register – Event 4

Average Dead Time = (Dead Time 1 + Dead Time 2)/2

DPWM A Rising Edge = Event 1

DPWM A Falling Edge = Event 1 + Filter Duty – Average Dead Time

Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register

Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register

DPWM B Rising Edge = Event 1 + Filter Duty – Average Dead Time + (Event 3 – Event 2)

DPWM B Falling Edge = Filter Period – (Period Register – Event 4)

Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

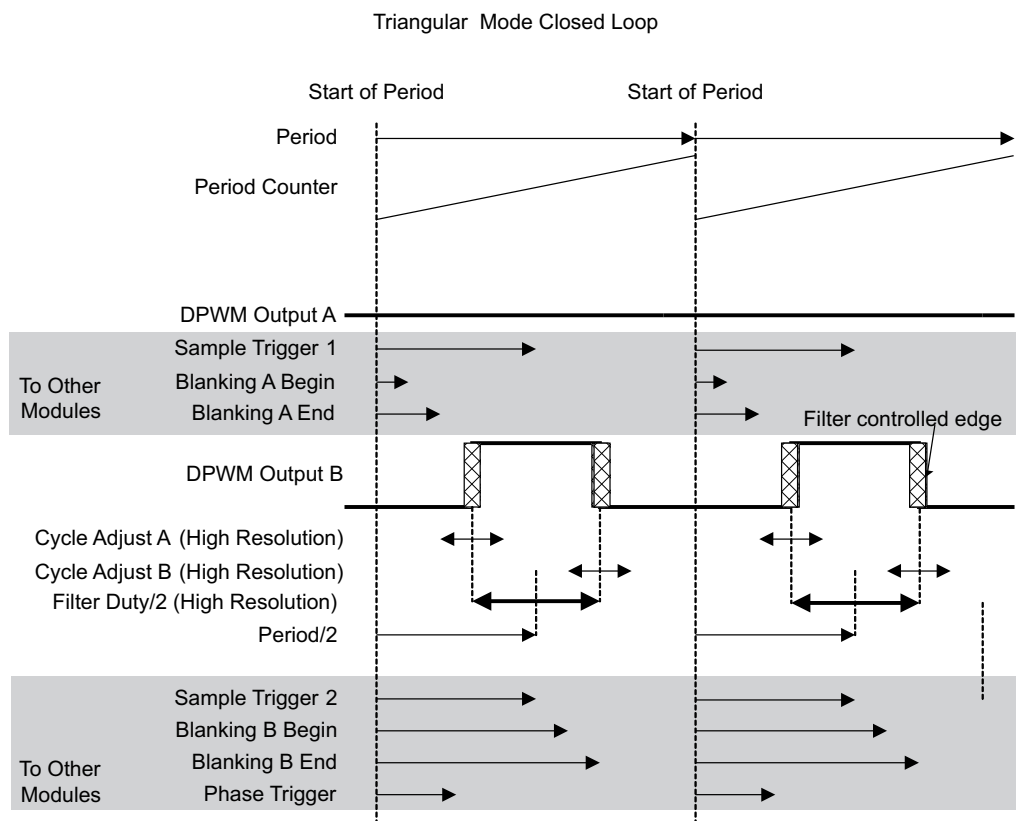
Figure 32. DPWM Resonant Symmetrical Mode

Device Functional Modes (continued)

The Filter has two outputs, Filter Duty and Filter Period. In this case, the Filter is configured so that the Filter Period is twice the Filter Duty. So if there were no dead times, each DPWM pin would be on for half of the period. For dead time handling, the average of the two dead times is subtracted from the Filter Duty for both DPWM pins. Therefore, both pins will have the same on-time, and the dead times will be fixed regardless of the period. The only edge which is fixed relative to the start of the period is the rising edge of DPWM A. This is the only edge for which the blanking signals can be used easily.

9.4.2 Triangular Mode

Triangular mode provides a stable phase shift in interleaved PFC and similar topologies. In this case, the PWM pulse is centered in the middle of the period, rather than starting at one end or the other. In Triangular Mode, only DPWM-B is available. Here is a diagram for Triangular Mode:



Events which change with DPWM mode:

DPWM A Rising Edge = None
 DPWM A Falling Edge = None
 Adaptive Sample Trigger = None
 DPWM B Rising Edge = $\text{Period}/2 - \text{Filter Duty}/2 + \text{Cycle Adjust A}$
 DPWM B Falling Edge = $\text{Period}/2 + \text{Filter Duty}/2 + \text{Cycle Adjust B}$
 Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

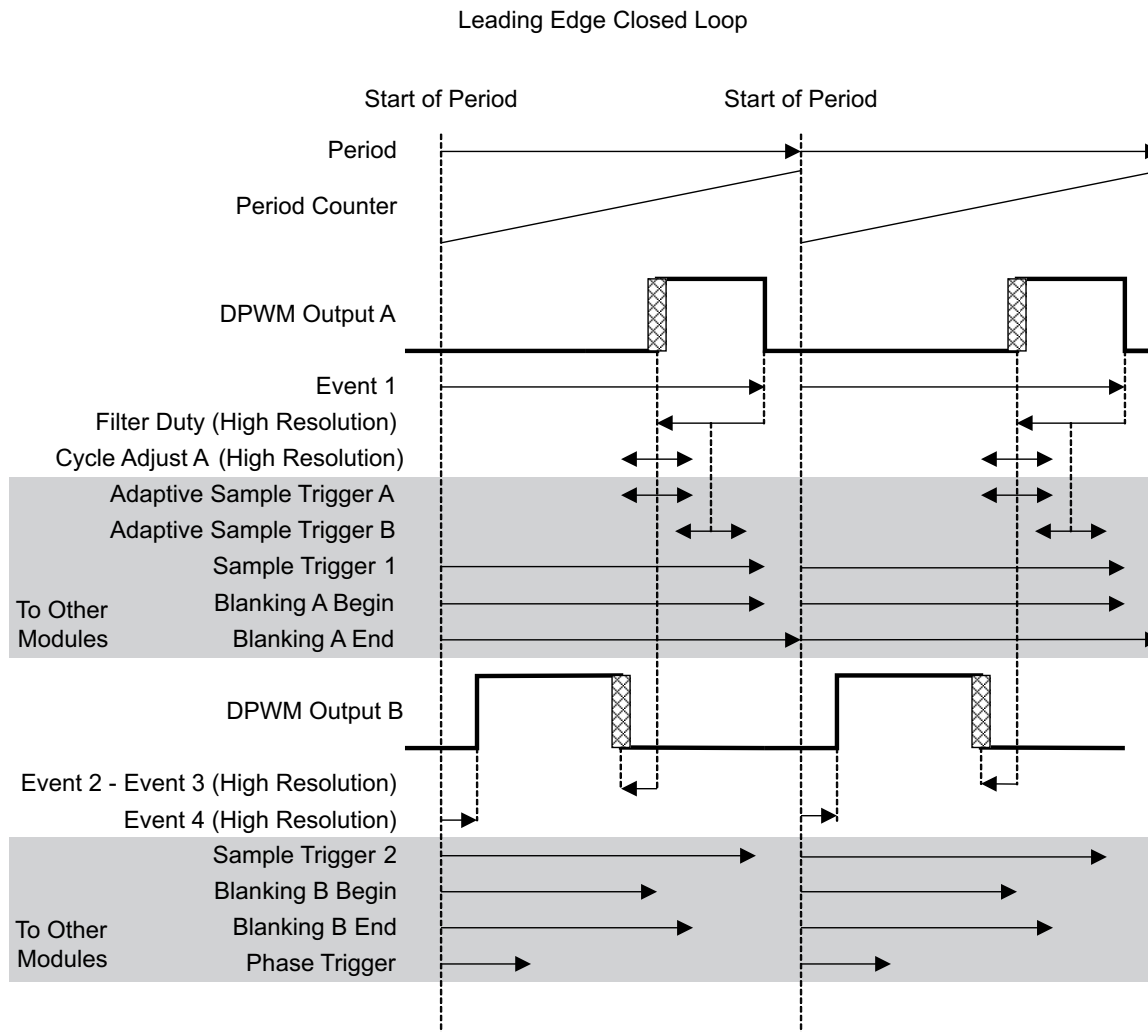
Figure 33. Triangular Mode

Device Functional Modes (continued)

All edges are dynamic in triangular mode, so fixed blanking is not that useful. The adaptive sample trigger is not needed. It is very easy to put a fixed sample trigger exactly in the center of the FET on-time, because the center of the on-time does not move in this mode.

9.4.3 Leading Edge Mode

Leading edge mode is similar to Normal mode, reversed in time. The DPWM A falling edge is fixed, and the rising edge moves to the left, or backwards in time, as the filter output increases. The DPWM B falling edge stays ahead of the DPWMA rising edge by a fixed dead time. Here is a diagram of the Leading Edge Mode:

Device Functional Modes (continued)


Events which change with DPWM mode:

DPWM A Falling Edge = Event 1

DPWM A Rising Edge = Event 1 - Filter Duty + Cycle Adjust A

Adaptive Sample Trigger A = Event 1 - Filter Duty + Adaptive Sample Register or

Adaptive Sample Trigger B = Event 1 - Filter Duty/2 + Adaptive Sample Register

DPWM B Rising Edge = Event 4

DPWM B Falling Edge = Event 1 - Filter Duty + Cycle Adjust A -(Event 2 – Event 3)

Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

Figure 34. Leading Edge Mode

As in the Normal mode, the two edges in the middle of the period are dynamic, so the fixed blanking intervals are mainly useful for the edges at the beginning and end of the period.

9.5 Register Maps

9.5.1 CPU Memory Map And Interrupts

When the device comes out of power-on-reset, the data memories are mapped to the processor as follows:

9.5.1.1 Memory Map (After Reset Operation)

ADDRESS	SIZE (BYTES)	MODULE
0x0000_0000 – 0x0003_FFFF In 32 repeated blocks of 8 k each	32 X 8 k	Boot ROM
0x0004_0000 – 0x0004_7FFF	32 k	Program Flash 0
0x0004_8000 – 0x0004_FFFF	32 k	Program Flash 1
0x0005_0000_0x0005_7FFF	32 k	Program Flash 2
0x0005_0000_0x0005_7FFF	32 k	Program Flash 3
0x0006_9800 – 0x0006_9FFF	2 k	Data Flash
0x0006_A000 – 0x0006_BFFF	8 k	Data RAM

9.5.1.2 Memory Map (Normal Operation)

Just before the boot ROM program gives control to flash program, the ROM configures the memory as follows:

ADDRESS	SIZE (BYTES)	MODULE
0x0002_0000 – 0x0002_1FFF	8 k	Boot ROM
0x0000_0000 – 0x00000_07FFF	32 k	Program Flash 0 (or 1)
0x0000_8000 – 0x08000_0FFFF	32 k	Program Flash 1 (or 0)
0x0000_8000 - 0x10000_17FFF	32 k	Program Flash 2 (or 0 for UCD3138128 only)
0x0000_8000 - 0x18000_1FFFF	32 k	Program Flash 3 (or 1 for UCD3138128 only)
0x0006_9800 – 0x0006_9FFF	2 k	Data Flash
0x0006_A000 – 0x0006_BFFF	8 k	Data RAM

9.5.1.3 Memory Map (System And Peripherals Blocks)

ADDRESS	SIZE	MODULE
0x0012_0000 - 0x0012_00FF	256	Loop Mux
0x0013_0000 - 0x0013_00FF	256	Fault Mux
0x0014_0000 - 0x0014_00FF	256	ADC
0x0015_0000 - 0x0015_00FF	256	DPWM 3
0x0016_0000 - 0x0016_00FF	256	Filter 2
0x0017_0000 - 0x0017_00FF	256	DPWM 2
0x0018_0000 - 0x0018_00FF	256	Front End/Ramp Interface 2
0x0019_0000 - 0x0019_00FF	256	Filter 1
0x001A_0000 - 0x001A_00FF	256	DPWM 1
0x001B_0000 – 0x001B_00FF	256	Front End/Ramp Interface 1
0x001C_0000 - 0x001C_00FF	256	Filter 0
0x001D_0000 - 0x001D_00FF	256	DPWM 0
0x001E_0000 - 0x001E_00FF	256	Front End/Ramp Interface 0
0xFFFF7_E400 - 0xFFFF7_34FF	256	RTC
0xFFFF7_EC00 - 0xFFFF7_ECFF	256	UART 0
0xFFFF7_ED00 - 0xFFFF7_EDFF	256	UART 1
0xFFFF7_F000 - 0xFFFF7_F0FF	256	Miscellaneous Analog Control
0xFFFF7_F600 - 0xFFFF7_F6FF	256	PMBus/I ² C Interface (1)
0xFFFF7_F700 - 0xFFFF7_F7FF	256	PMBus/I ² C Interface (2)

ADDRESS	SIZE	MODULE
0xFFFF7_FA00 - 0xFFFF7_FAFF	256	GIO
0xFFFF7_FD00 - 0xFFFF7_FDFE	256	Timer
0xFFFFF_FD00 - 0xFFFFF_FDFE	256	MMC
0xFFFFF_FE00 - 0xFFFFF_FEFF	256	DEC
0xFFFFF_FF20 - 0xFFFFF_FF37	23	CIM
0xFFFFF_FFD0 - 0xFFFFF_FFEC	28	SYS

The registers and bit definitions inside the System and Peripheral blocks are detailed in the programmer's manuals.

9.5.2 Boot ROM

The device incorporates a 8 kB boot ROM. This boot ROM includes support for:

- Program download through the PMBus
- Device initialization
- Examining and modifying registers and memory
- Verifying and executing program flash automatically
- Jumping to a customer defined boot program
- Checksum evaluation to support using the program flash as a single 64 kB block or as 2-32 kB blocks.

The Boot ROM is entered automatically on device reset. It initializes the device and then performs checksums on the program flash. If the first 2 kB of program FLASH 0 has a valid checksum, the program branches to location 0 in Program FLASH 0. This permits the use of a custom boot program. If the first checksum fails, it performs some additional checksum calculations to determine where the valid program is located. This permits full automated program memory checking, when there is no need for a custom boot program. The complete decision tree is located in [Figure 35](#). Additionally, the part can support two separate programs in block 0 and block 1 through a custom boot-flash routine.

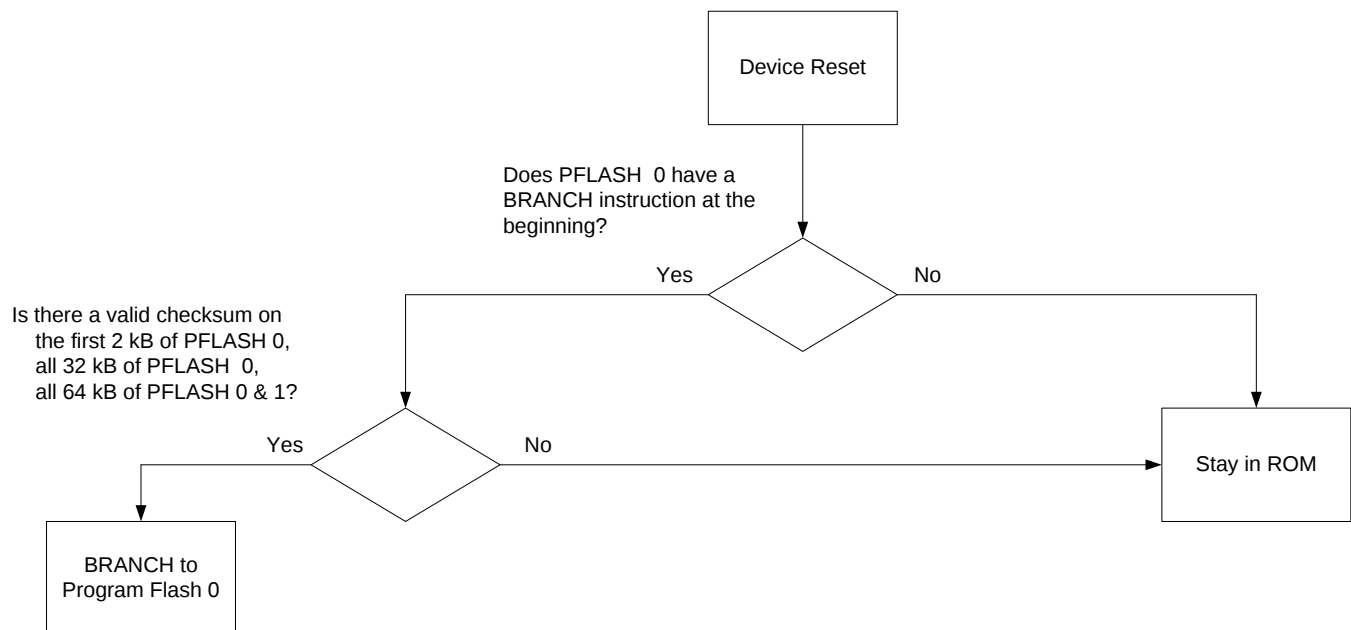


Figure 35. Check Sum Evaluation Flowchart, 64 kB

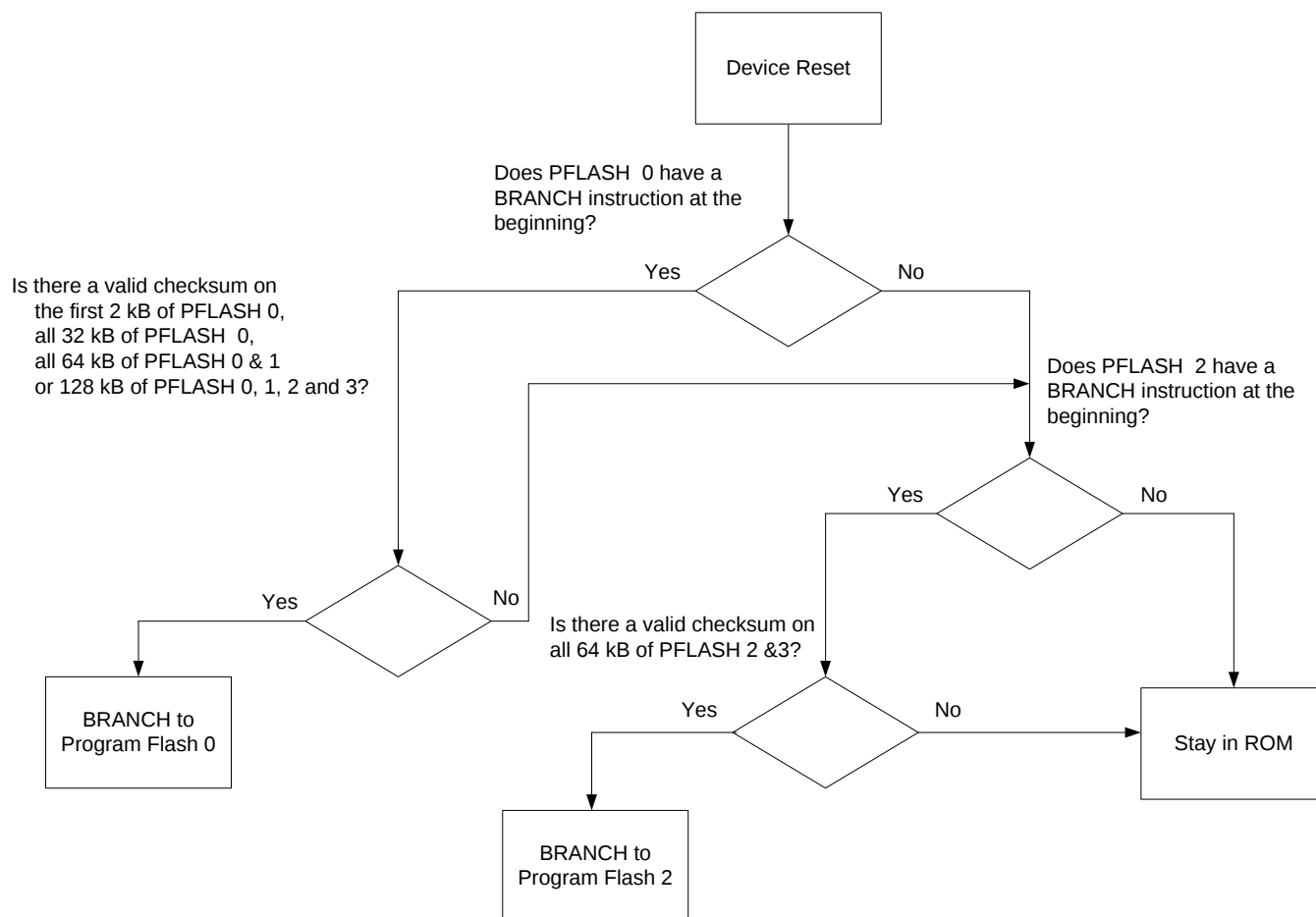


Figure 36. Check Sum Evaluation Flowchart, 128 kB

If none of the checksums are valid, the Boot ROM stays in control, and accepts commands via the PMBus interface. These functions can be used to read and write to all memory locations in the device. Typically they are at address 11 and are used to download a program to Program Flash, and to command its execution.

9.5.3 Customer Boot Program

As described above, it is possible to generate a user boot program using 2 kB or more of the Program Flash. This can support things which the Boot ROM does not support, including:

- Program download via UART – useful especially for applications where the UCD3138A64 or UCD3138128 is isolated from the host (e.g., PFC)
- Encrypted download – useful for code security in field updates.
- PMBus download at different addresses
- Different command formats

9.5.4 Flash Management

The device offers a variety of features providing for easy prototyping and easy flash programming. At the same time, high levels of security are possible for production code, even with field updates. Standard firmware will be provided for storing multiple copies of system parameters in data flash. This minimizes the risk of losing information if data-flash programming is interrupted.

9.6 Synchronous Rectifier MOSFET Ramp And IDE Calculation

The device has built in logic for optimizing the performance of the synchronous rectifier MOSFETs. This comes in two forms:

- Synchronous Rectifier MOSFET ramp for softly turning on and off the MOSFETs
- Ideal Diode Emulation (IDE) calculation

When starting up a power supply, it is not uncommon for there to already be a voltage present on the output – this is called pre-bias. It can be very difficult to calculate the ideal synchronous rectifier MOSFET on-time for this case. If it is not calculated correctly, it may pull down the pre-bias voltage, causing the power supply to sink current. To avoid this, the synchronous rectifier MOSFETs are not turned on until after the power supply has ramped up to the nominal output voltage. The synchronous rectifier MOSFETs are then turned on slowly in order to avoid an output voltage glitch. The synchronous rectifier MOSFET ramp logic can be used to turn them on at a rate well below the bandwidth of the filter.

In discontinuous mode, the ideal on-time for the synchronous rectifier MOSFETs is a function of V_{in} , V_{out} , and the primary side duty cycle (D). The IDE logic in the UCD3138x takes V_{in} and V_{out} data from the firmware and combines it with D data from the filter hardware. It uses this information to calculate the ideal on-time for the synchronous rectifier MOSFETs.

10 Applications and Implementation

10.1 Application Information

The UCD3138x has an extensive set of fully-programmable, high-performance peripherals that make it suitable for a wide range of power supply applications. In order to make the part easier to use, TI has prepared an extensive set of materials to demonstrate the features of the device for several key applications. In each case the following items are available:

1. Full featured EVM hardware that demonstrates classic power supply functionality.
2. An EVM user guide that contains schematics, bill-of-materials, layout guidance and test data showcasing the performance and features of the device and the hardware.
3. A firmware programmers manual that provides a step-by-step walk through of the code.

Table 3. Application Information

APPLICATION	EVM DESCRIPTION
Phase shifted full bridge	This EVM demonstrates a PSFB DC-DC power converter with digital control using the UCD3138x device. Control is implemented by using PCMC with slope compensation. This simplifies the hardware design by eliminating the need for a series blocking capacitors and providing the inherent input voltage feed-forward that comes from PCMC. The controller is located on a daughter card and requires firmware in order to operate. This firmware, along with the entire source code, is made available through TI. A free, custom function GUI is available to help the user experiment with the different hardware and software enabled features. The EVM accepts a DC input from 350 VDC to 400 VDC, and outputs a nominal 12 VDC with full load output power of 360 W, or full output current of 30 A.
LLC resonant converter	This EVM demonstrates an LLC resonant half-bridge DC-DC power converter with digital control using the UCD3138x device. The controller is located on a daughter card and requires firmware in order to operate. This firmware, along with the entire source code, is made available through TI. A free, custom function GUI is available to help the user experiment with the different hardware and software enabled features. The EVM accepts a DC input from 350 VDC to 400 VDC, and outputs a nominal 12 VDC with full load output power of 340 W, or full output current of 29 A.

10.2 Typical Application

This section summarizes the PSFB EVM DC-DC power converter.

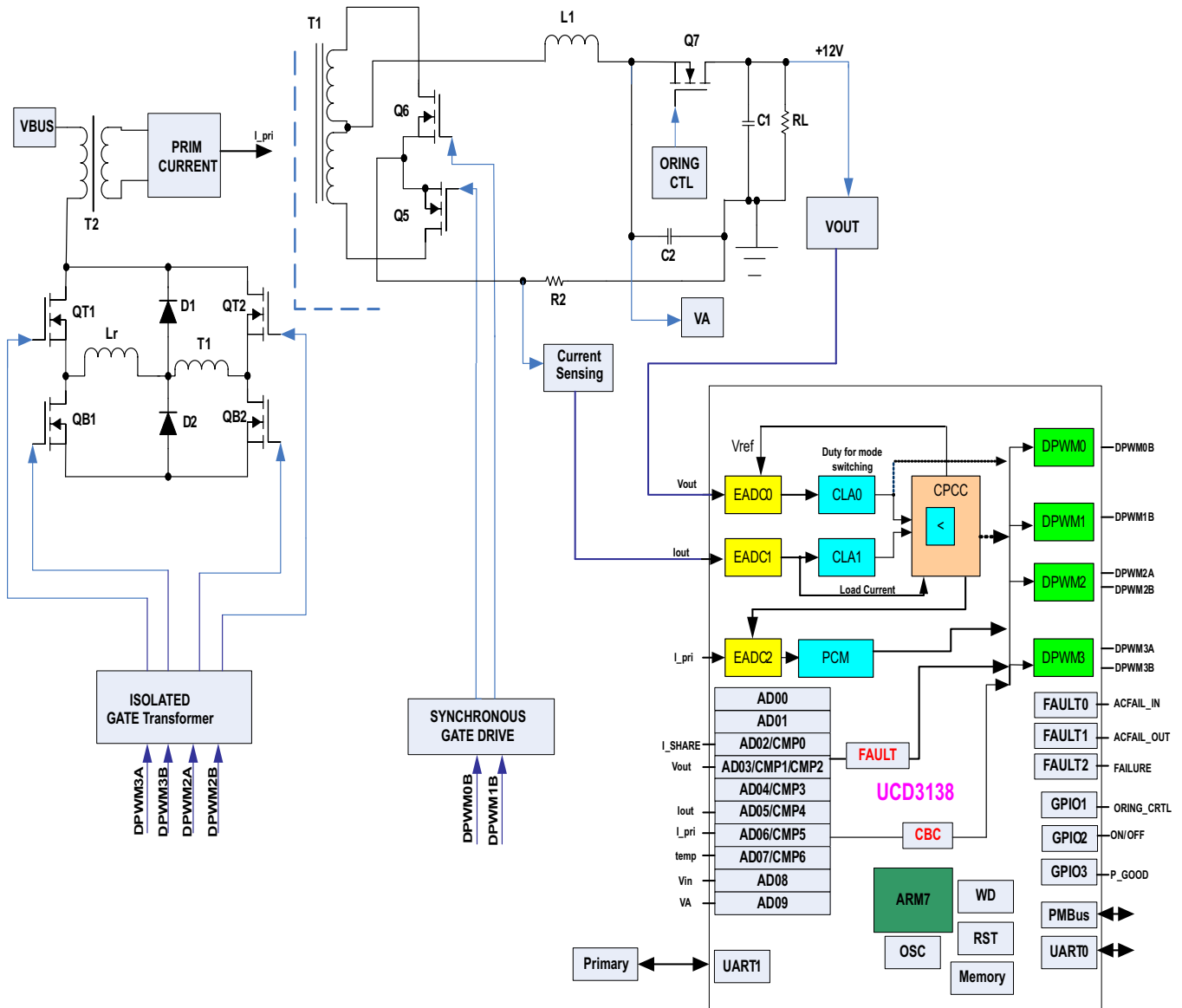


Figure 37. Phase-Shifted Full-Bridge

Typical Application (continued)

10.2.1 Design Requirements

Table 4. Input Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ALL SPECIFICATIONS at $V_{in}=400V$ and $25^{\circ}C$ AMBIENT UNLESS OTHERWISE NOTED.						
V_{in}	Input voltage range	Normal Operating	350	385	420	V
V_{inmax}	Max input voltage	Continuous			420	V
I_{in}	Input current	$V_{in}=350V$, Full Load		1.15		A
I_{stby}	Input no load current	Output current is 0A		30		mA
V_{on}	Under voltage lockout	V_{in} Decreasing (input voltage is detected on secondary side)		340		V
V_{hys}		V_{in} Increasing		360		V

Table 5. Output Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ALL SPECIFICATIONS at $V_{in}=400V$ and $25^{\circ}C$ AMBIENT UNLESS OTHERWISE NOTED.						
V_O	Output voltage setpoint	No load on outputs		12		V
Reg_{line}	Line regulation	All outputs; $360 \leq V_{in} \leq 420$; $I_O = I_{Omax}$			0.5	%
Reg_{load}	Load regulation	All outputs; $0 \leq I_O \leq I_{Omax}$; $V_{in} = 400V$			1	%
V_n	Ripple and noise ⁽¹⁾	5Hz to 20 MHz		100		mVpp
I_O	Output current		0		30	A
η	Efficiency at phase-shift mode	$V_O = 12V$, $I_O = 15A$		93%		
η	Efficiency at PWM ZVS mode	$V_O = 12V$, $I_O = 15A$		93%		
η	Efficiency at hard switching mode	$V_O = 12V$, $I_O = 15A$		90%		
V_{adj}	Output adjust range		11.4		12.6	V
V_{tr}	Transient response overshoot/undershoot	50% Load Step at 1A μ S, min load at 2A		± 0.36		V
$t_{settling}$	Transient response settling time			100		μ S
t_{start}	Output rise time	10% to 90% of V_{out}		50		mS
	Overshoot	At Startup			2	%
f_s	Switching frequency	Over V_{in} and I_O ranges		150		kHz
I_{share}	Current sharing accuracy	50% - full load		± 5		%
ϕ	Loop phase margin	10% - Full load		45		degree
G	Loop gain margin	10% - Full load		10		dB

(1) Ripple and noise are measured with 10 μ F Tantalum capacitor and 0.1 μ F ceramic capacitor across output.

10.2.2 Detailed Design Procedure

10.2.2.1 PCMC (Peak Current Mode Control) PSFB (Phase Shifted Full Bridge) Hardware Configuration Overview

The hardware configuration of the UCD3138x PCMC PSFB converter contains two critical elements that are highlighted in the subsequent sections.

- DPWM initialization - This section will highlight the key register settings and considerations necessary for the UCD3138x to generate the correct MOSFET waveforms for this topology. This maintains the proper phase relationship between the MOSFETs and synchronous rectifiers as well as the proper set up required to function correctly with PCMC.
- PCMC initialization - This section will discuss the register settings and hardware considerations necessary to modulate the DPWM pins with PCMC and internal slope compensation.

10.2.2.2 DPWM Initialization for PSFB

The UCD3138x DPWM peripheral provides flexibility for a wide range of topologies. The PSFB configuration utilizes the Intra-Mux and Edge Generation Modules of the DPWM. For a diagram showing these modules, see the UCD3138x Digital Power Peripherals Manual.

Here is a schematic of the power stage of the PSFB:

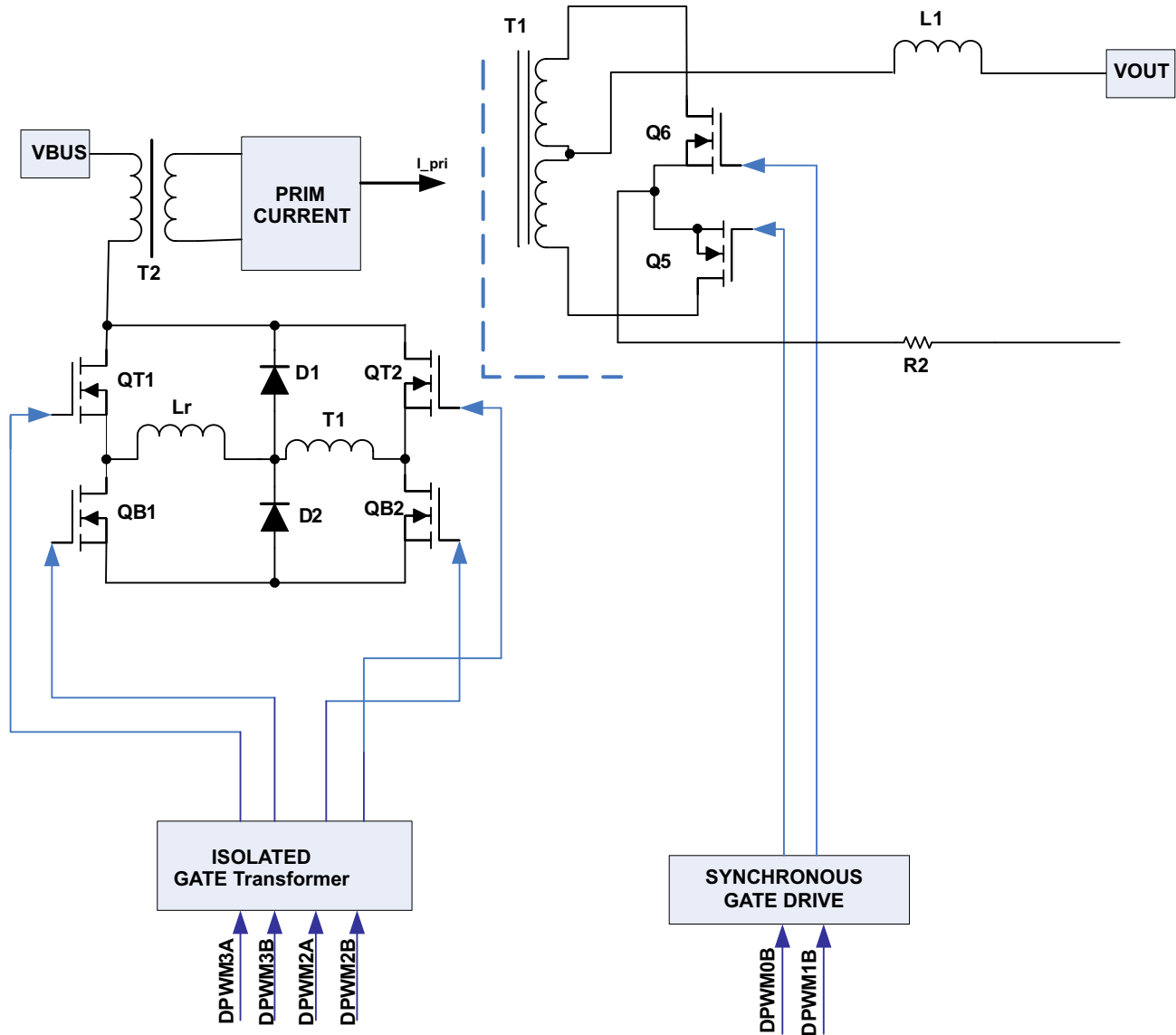
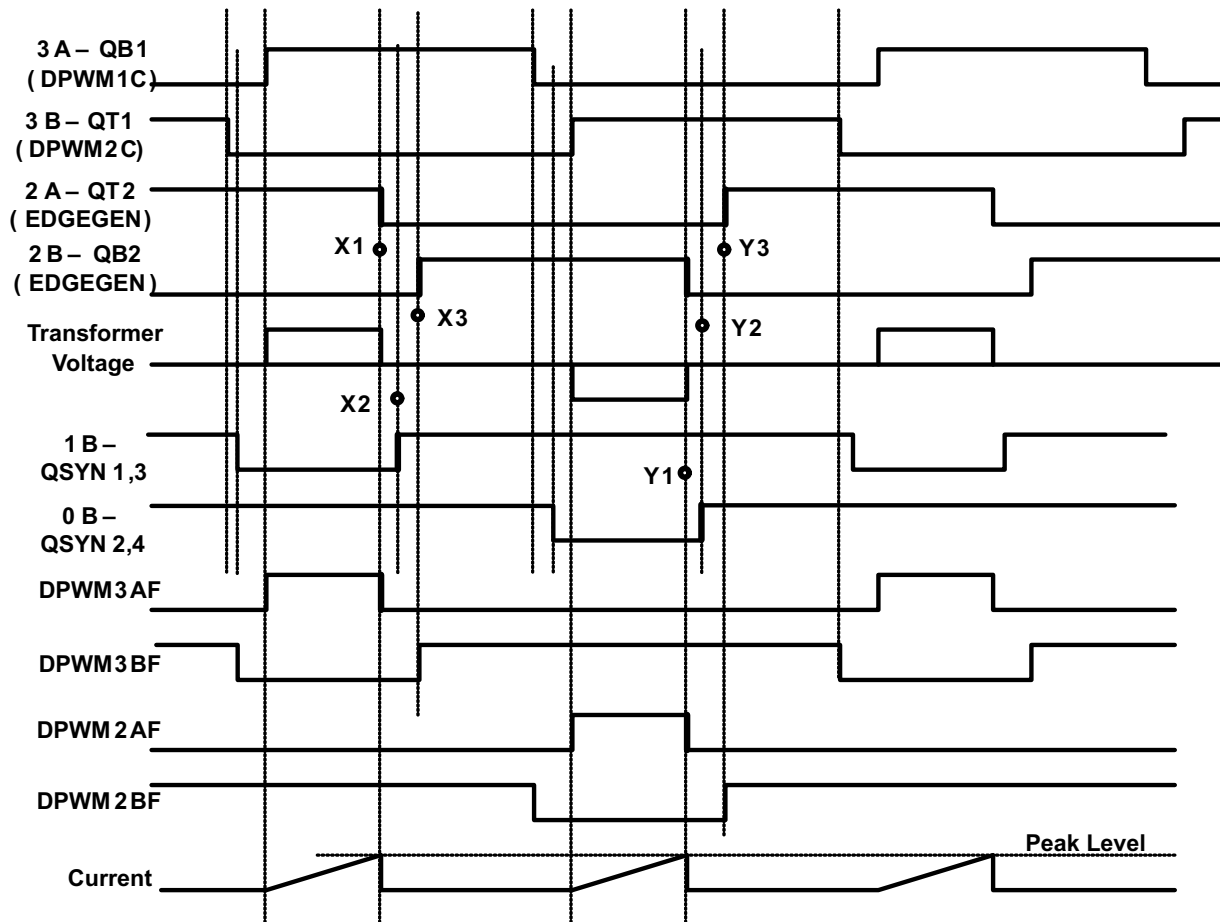


Figure 38. Schematic – PSFB Power Stage

Here is an overview of the key PSFB signals:



X1, X2, X3 and Y1, Y2, Y3 are sets of moving edges
All other edges are fixed .

Figure 39. Key PSFB Signals

10.2.2.3 DPWM Synchronization

DPWM1 is synchronized to DPWM0, DPWM2 is synchronized to DPWM1, and DPWM3 is synchronized to DPWM2, $\frac{1}{2}$ period out of phase using these commands:

```
Dpwm1Regs.DPWMCTRL0.bit.MSYNC_SLAVE_EN = 1; //configured to slave
Dpwm2Regs.DPWMCTRL0.bit.MSYNC_SLAVE_EN = 1; // configured to slave
Dpwm3Regs.DPWMCTRL0.bit.MSYNC_SLAVE_EN = 1; // configured to slave
```

```
Dpwm0Regs.DPWMPHASETRIG.all = PWM_SLAVESYNC;
Dpwm1Regs.DPWMPHASETRIG.all = PWM_SLAVESYNC;
Dpwm2Regs.DPWMPHASETRIG.all = PWM_SLAVESYNC;
```

```
LoopMuxRegs.DPWMMUX.bit.DPWM1_SYNC_SEL = 0; // Slave to dpwm-0
LoopMuxRegs.DPWMMUX.bit.DPWM2_SYNC_SEL = 1; // Slave to dpwm-1
LoopMuxRegs.DPWMMUX.bit.DPWM3_SYNC_SEL = 2; // Slave to dpwm-2
```

If the event registers on the DPWMs are the same, the two pairs of signals will be symmetrical. All code examples are taken from the PSFB EVM code, unless otherwise stated.

10.2.2.4 Fixed Signals to Bridge

The two top signals in the above drawing have fixed timing. The DPWM1CF and DPWM2CF signals are used for these pins. DPWMCxF refers to the signal coming out of the fault module of DPWMx, as shown in [Figure 40](#).

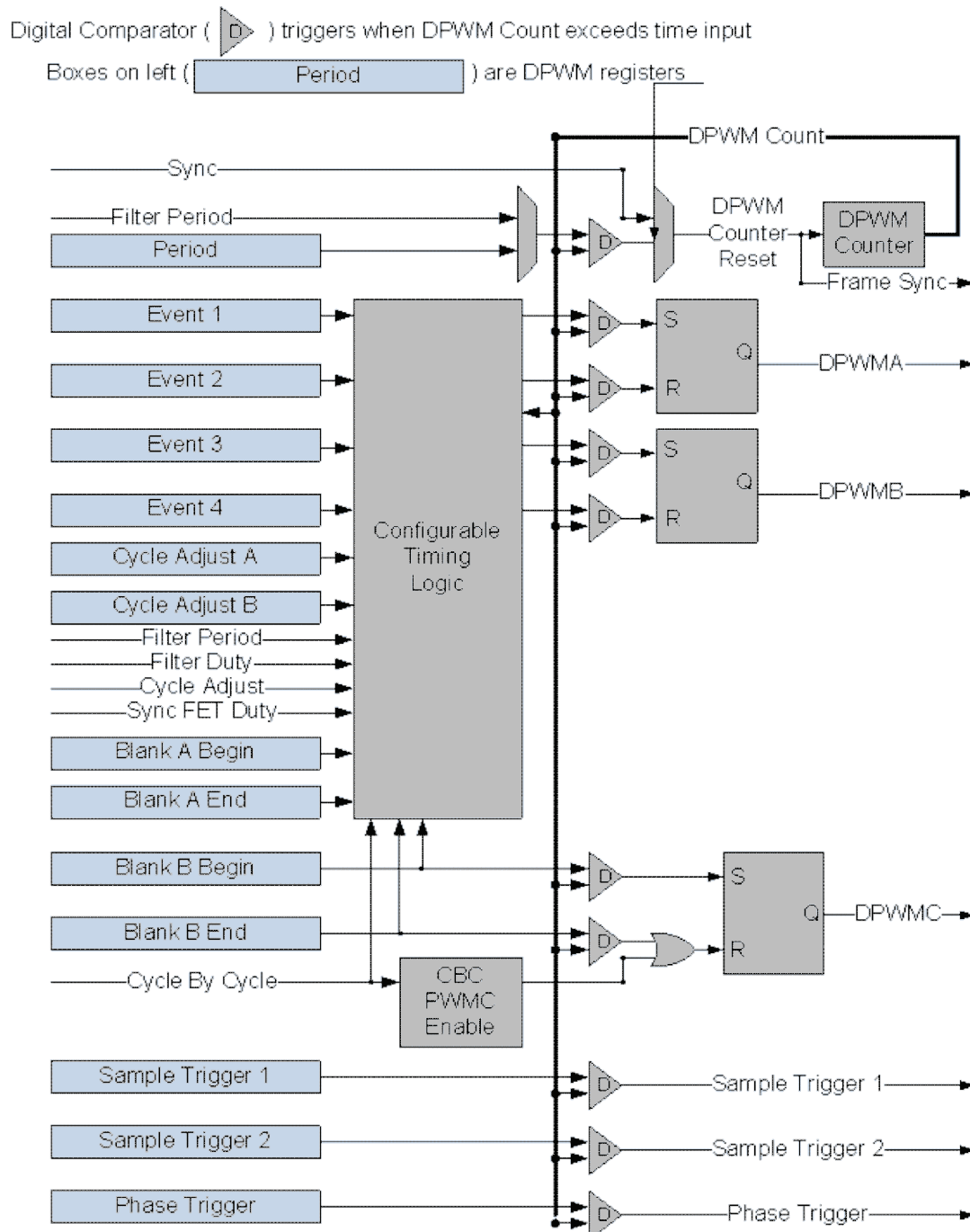


Figure 40. Fixed Signals to Bridge

These signals are actually routed to pins DPWM3A and 3B using the Intra Mux with these statements:

```
Dpwm3Regs.DPWMCTRL0.bit.PWM_A_INTRA_MUX = 7; // Send DPWM1C  
Dpwm3Regs.DPWMCTRL0.bit.PWM_B_INTRA_MUX = 8; // Send DPWM2C
```

Since these signals are really being used as events in the timer, the #defines are called EV5 and EV6. Here are the statements which initialize them:

```
// Setup waveform for DPWM-C (re-using blanking B regs)
Dpwm2Regs.DPWMBLKBEG.all = PWM2_EV5 + (4 *16);
Dpwm2Regs.DPWMBLKBEND.all = PWM2_EV6;
```

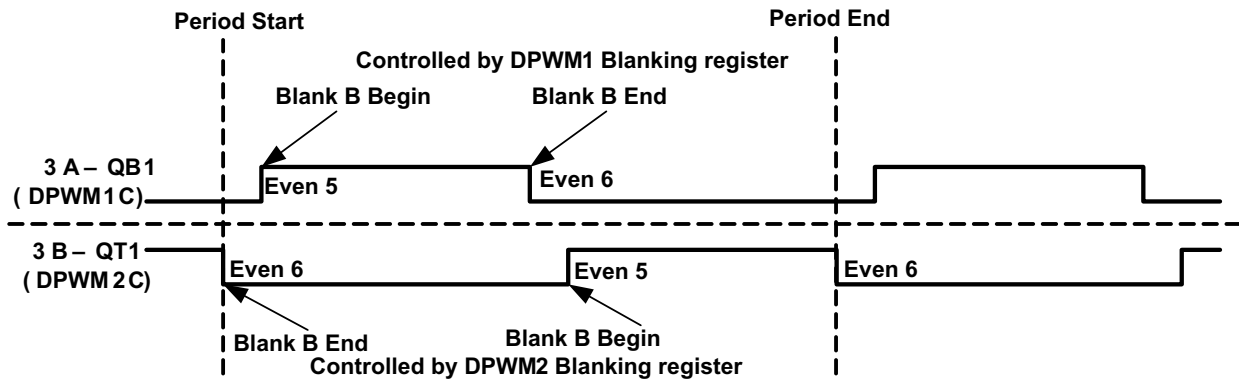


Figure 41. Blank B Timing Information

The statements for DPWM1 are the same. Remember that DPWMC reuses the Blank B registers for timing information.

10.2.2.5 Dynamic Signals to Bridge

DPWM0 and 1 are set at normal mode. PCMC triggering signal (fault) chops DPWM0A and 1A cycle by cycle. The corresponding DPWM0B and 1B are used for synchronous rectifier MOSFET control. The same PCMC triggering signal is applied to DPWM2 and DPWM3. Both of these are set to normal mode as well. DPWM2 and 3 are chopped and their edges are used to generate the next two dynamic signals to the bridge. They are generated using the Edge Generator Module in DPWM2. The Edge Generator sources are DPWM2 and DPWM3. The edges used are:

- DPWM2A turned on by a rising edge on DPWM2BF
- DPWM2A turned off by a falling edge on DPWM3AF
- DPWM2B turned on by a rising edge on DPWM3BF
- DPWM2B turned off by a falling edge on DPWM2AF

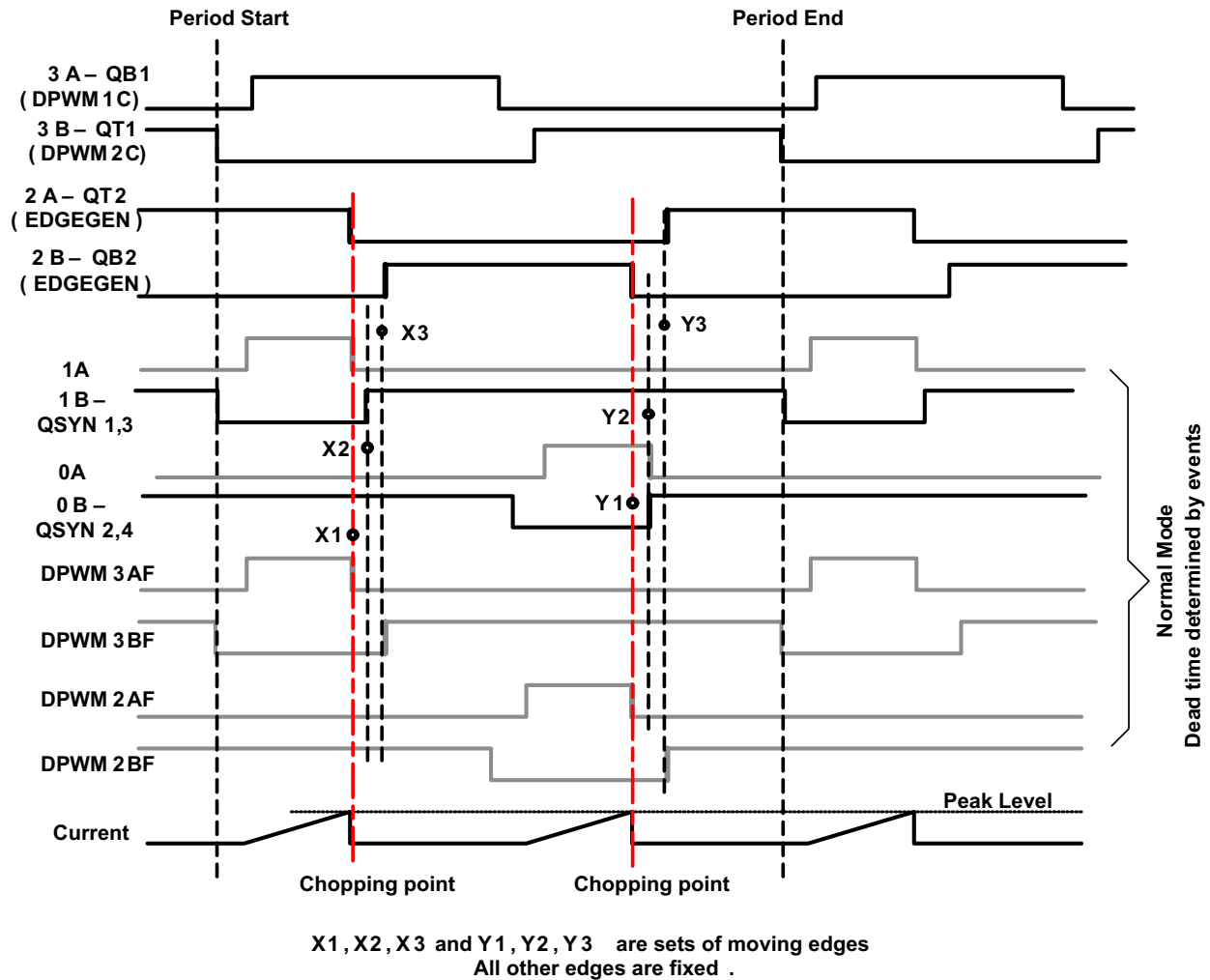


Figure 42. Dynamic Signals to Bridge

The Edge Generator is configured with these statements:

```
Dpwm2Regs.DPWMEDGEGEN.bit.A_ON_EDGE = 2;
Dpwm2Regs.DPWMEDGEGEN.bit.A_OFF_EDGE = 5;
Dpwm2Regs.DPWMEDGEGEN.bit.B_ON_EDGE = 6;
Dpwm2Regs.DPWMEDGEGEN.bit.B_OFF_EDGE = 1;
```

```
Dpwm2Regs.DPWMCTRL0.bit.PWM_A_INTRA_MUX = 1; // EDGE GEN-A out the A output
Dpwm2Regs.DPWMCTRL0.bit.PWM_B_INTRA_MUX = 1; // EDGE GEN-B out the B output
```

```
Dpwm2Regs.DPWMEDGEGEN.bit.EDGE_EN = 1;
```

The EDGE_EN bits are set for all 4 DPWMs. This is done to ensure that all signals have the same timing delay through the DPWM.

The final 6 gate signals are shown in [Figure 43](#).

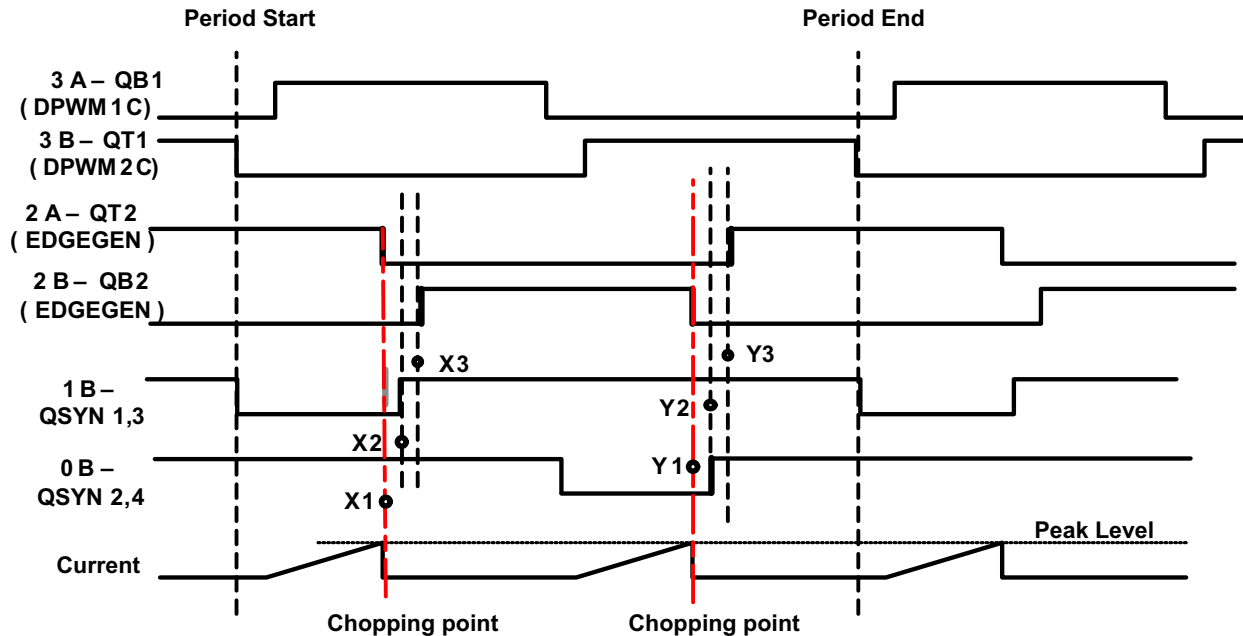


Figure 43. Final 6 Gate Signals

Note how the falling edge of DPWM2AF aligns with the X1 edge, and how the rising edge of DPWM2BF aligns with the X3 edge. The falling edges on DPWM2AF and DPWM3AF are caused by the peak detection logic. This is fed through the Cycle By Cycle logic. The Cycle By Cycle logic also has a special feature to control the rising edges of DPWM2BF (X1 and X3) and DPWM3BF (Y1 and Y3). It uses the value of Event3 – Event2 to control the time between the edges. The same feature is used with DPWM0 and DPWM1 to control the X2 and Y2 signals. Using the other 2 DPWMs permits these signals to have a different dead time.

The same setup can be used for voltage mode control. In this case, the Filter output sets the timing of the falling edge on DPWMxAF.

All DPWMs are configured in Normal mode, with CBC enabled. If external slope compensation is used, DPWM1A and DPWM1B are used to reset the external compensator at the beginning of each half cycle. If no PCMC event occurs, the values of Events 2 and 3 determine the locations of the edges, just as in open loop mode.

10.2.3 System Initialization for PCM

PCM (Peak Current Mode) is a specialized configuration for the UCD3138x which involves several peripherals. This section describes how it works across the peripherals.

10.2.3.1 Use of Front Ends and Filters in PSFB

All three front ends are used in PSFB. The same signals are used in the same places for both PCMC and voltage mode. The same hardware can be used for both control modes, with the mode determined by which firmware is loaded into the device. FE0 and FE1 are used with their associated filters, but Filter 2 is not used at all.

- FE0 – Vout – voltage loop
- FE1 – Iout – current loop
- FE2 – I_{pri} – PCM

In PCMC mode, FE2 is used for PCMC, and the voltage loop is normally used to provide the start point for the compensation ramp. If the CPCC firmware detects a need for constant current mode, it switches to the current loop for the start point.

10.2.3.2 Peak Current Detection

Peak current detection involves all the major modules of the DPPs, the Front End, Filter, Loop Mux, Fault Mux and the DPWMs. A drawing of the major elements is shown in Figure 44.

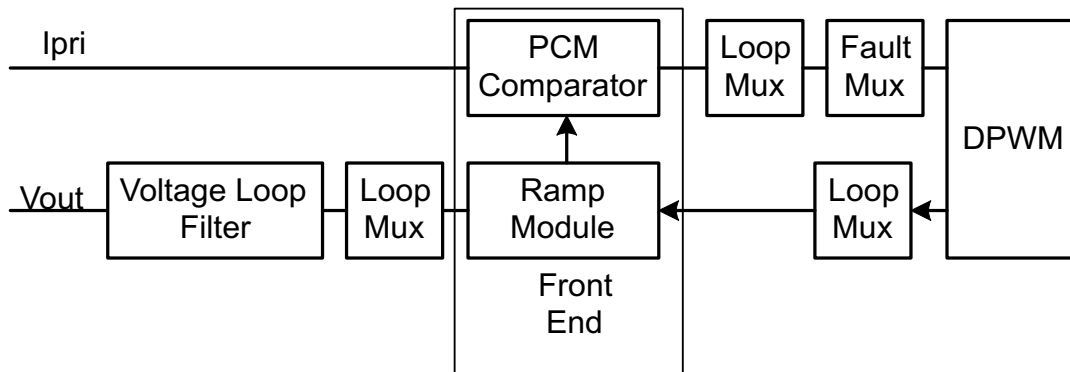


Figure 44. Peak Current Detection Function

All signals without arrows flow from left to right. The voltage loop is used to select a peak current level. This level is fed to the Ramp module to generate a compensation ramp. The compensation ramp is compared to the primary current by the PCMC comparator in the Front End. When the ramp value is greater than the primary current, the APCMC signal is sent to the DPWM, causing the events described in the previous sections.

The DPWM frame start and output pin signals can be used to trigger the Ramp Module. In this case, unlike in the case of other ramp module functions, each DPWM frame triggers the start of the ramp. The ramp steps every 32 ns.

The Filter is configured normally, there is no real difference for PCMC. The PCM_FILTER_SEL bits in the LoopMux.PCMCTRL register are used to select which filter is connected to the ramp module:

```
LoopMuxRegs.PCMCTRL.bit.PCM_FILTER_SEL = 0; //select filter0
```

With Firmware Constant Power/Constant current, Filter 1 and Front End 1 are used as a current control loop, with the EADC DAC set to high current. If the voltage loop value becomes higher than the current loop value, then Filter 1 is used to control the PCM ramp start value:

```
LoopMuxRegs.PCMCTRL.bit.PCM_FILTER_SEL = 1;  
//select filter1 for slope compensation source
```

In the ramp module, there are 2 bitfields in the RAMPCTRL register which must be configured. The PCM_START_SEL must be set to a 1 to enable the Filter to be used as a ramp start source. The RAMP_EN bit must be set, of course.

The DAC_STEP register sets the slope of the compensation ramp. The DAC value is in volts, of course, so it is necessary to calculate the slope after the current to voltage conversion. Here is the formula for converting from millivolts per microsecond to DACSTEP.

m = compensation slope in millivolts per microsecond

$$ACSTEP = 335.5 \times M$$

In C, this can be written:

```
#define COMPENSATION_SLOPE 150 //compensation slope in millivolts per microsecond  
#define DACSTEP_COMP_VALUE ((int) (COMPENSATION_SLOPE*335.5) )  
//value in DACSTEP for desired compensation slope  
  
FeCtrl0Regs.DACSTEP.all = DACSTEP_COMP_VALUE;
```

It may also be necessary to set a ramp ending value in the RAMPDACEND register.

In addition, it is necessary to set the D2S_COMP_EN bit in the EADCCTRL register. This is for enabling the differential to single ended comparator function. The front end diagram leaves it out for simplicity, but the connection between the DAC and the EADC amplifier is actually differential. The PCMC comparator, however, is single ended. So a conversion is necessary as shown in Figure 45.

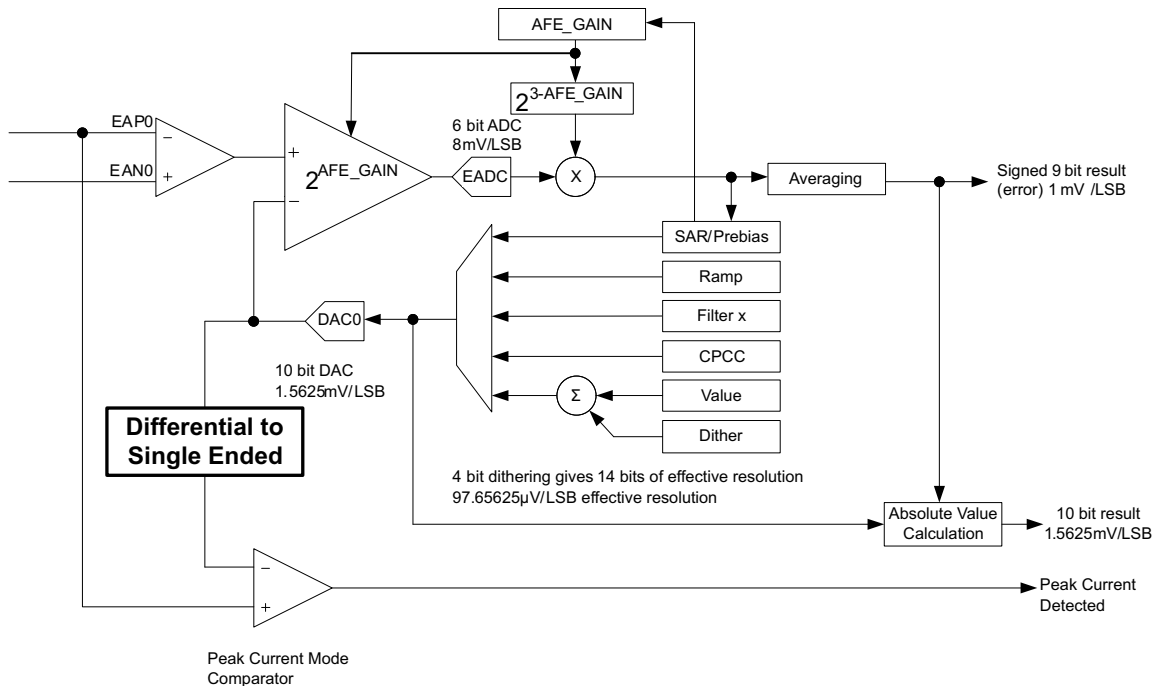


Figure 45. Differential to Single-Ended Comparator Function

The EADC_MODE bit in EADCCTRL should be set to a 5 for peak current mode.

The peak current detection signal next goes to the Loop Mux. The Fault Mux has only 1 APCM input, but there are 3 front ends. So the PCM_FE_SEL bits in APCMCTRL must be used to select which front end is used:

LoopMuxRegs.APCMCTRL.bit.PCM_FE_SEL = 2; // use FE2 for PCM */

The PCM_EN bit must also be set.

LoopMuxRegs.APCMCTRL.bit.PCM_EN = 1; // Enable PCM

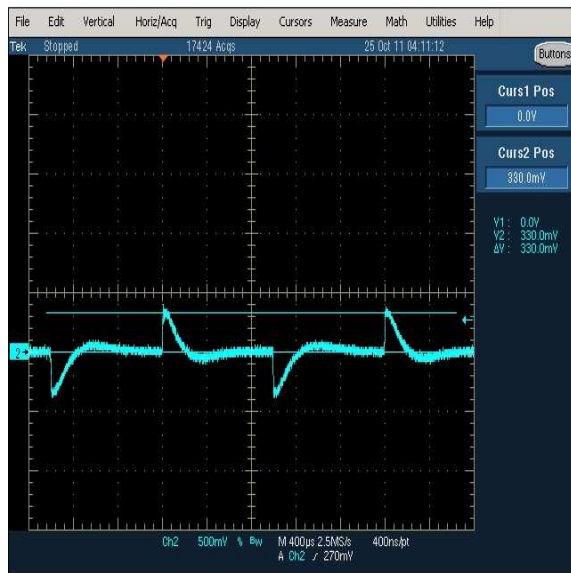
Next the Fault Mux is used to enable the APCM bit to the CLIM/CBC signal to the DPWM. There are 4 DPWMxCLIM registers, one for each DPWM. The ANALOG_PCM_EN bit must be set in each one to connect the PCM detection signal to the CLIM/CBC signal on each DPWM. For the latest configuration information on all of these bits, consult the appropriate EVM firmware. To avoid errors, it is best to configure your hardware design using the same DPWMs, filters, and front ends for the same functions as the EVM.

DPWM timing is used to trigger the start of the ramp. This is selected by the FECTRLxMUX registers in the Loop Mux. DPWMx_FRAME_SYNC_EN bits, when set, cause the ramp to be triggered at the start of the DPWM period.

10.2.3.3 Peak Current Mode (PCM)

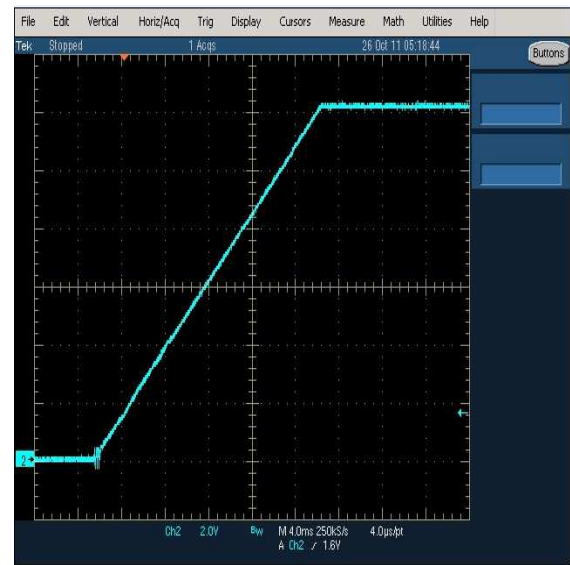
There is one peak current mode control module in the device however any front end can be configured to use this module.

10.2.4 Application Curves



1A-16A-1A Vin =385V

Figure 46. Load Transient



30A Load syncFETs off

Figure 47. V_{OUT} Soft Start

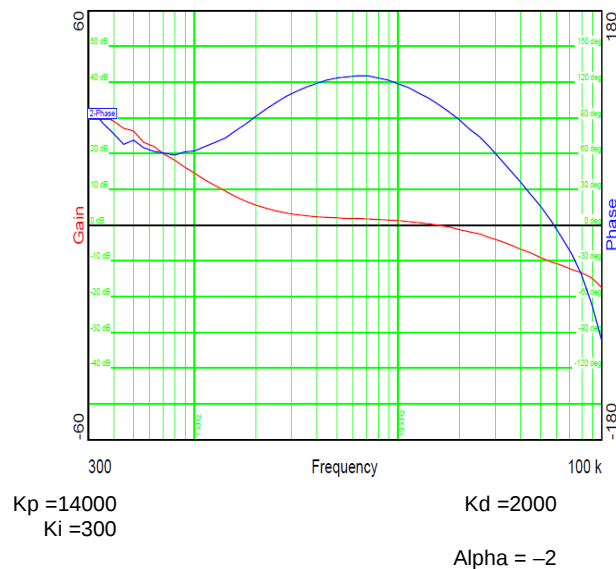


Figure 48. Bode Plot

11 Power Supply Recommendations

- Both 3.3 VD and 3.3 VA should have a local 4.7 μ F capacitor placed as close as possible to the device pins
- BP18 should have a 1 μ F capacitor.

12 Layout

12.1 Device Grounding and Layout Guidelines

- Single ground is recommended: SGND. A multilayer such as 4 layers board is recommended so that one solid SGND is dedicated for return current path, referred to the layout example.
- Apply multiple different capacitors for different frequency range on decoupling circuits. Each capacitor has different ESL, Capacitance and ESR, and they have different frequency response.
- Avoid long traces close to radiation components, and place them into an internal layer, and it is preferred to have grounding shield.
- Analog circuits and digital circuits should have separate return to ground; although with a single plane, still try to avoid mixing analog current and digital current.
- Do not use a ferrite bead or larger than 3- Ω resistor to connect between V33A and V33D.
- Both 3.3VD and 3.3VA should have local decoupling capacitors close to the device power pins, add vias to connect decoupling caps directly to SGND.
- Avoid negative current/negative voltage on all pins, so Schottky clamping diodes may be needed to limit the voltage; avoid more than 3.8 V or less than –0.3 V voltage spikes on all pins; add Schottky diodes on the pins which could have voltage spikes during surge test; be aware that a Schottky has relatively higher leakage current, which can affect the voltage sensing at high temperature.
- If V33 slew rate is less than 2.5 V/ms the RESET pin should have a 2.21-k Ω resistor between the reset pin and V33D and a 2.2- μ F capacitor from RESET to ground. For more details please refer to the [UCD3138 Family - Practical Design Guideline](#). This capacitor must be located close to the device RESET pin.
- RSVD (Pin 61) should be connected to BP18 through 1-k Ω resistor.
- Configure unused GPIO pins to be inputs or connect them to the ground (DGND or SGND); when an external pull-up resistor is used for GPIO, the pull-up resistor needs to be 1 k Ω or higher.
- For more details please refer to the [UCD3138 Family - Practical Design Guideline](#).

12.2 Layout Examples

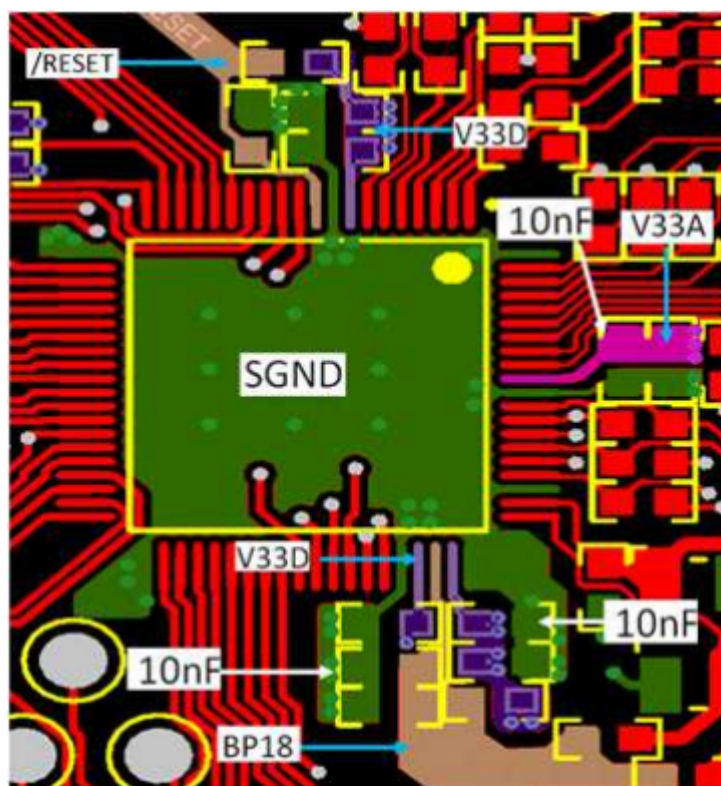


Figure 49. Layout Example

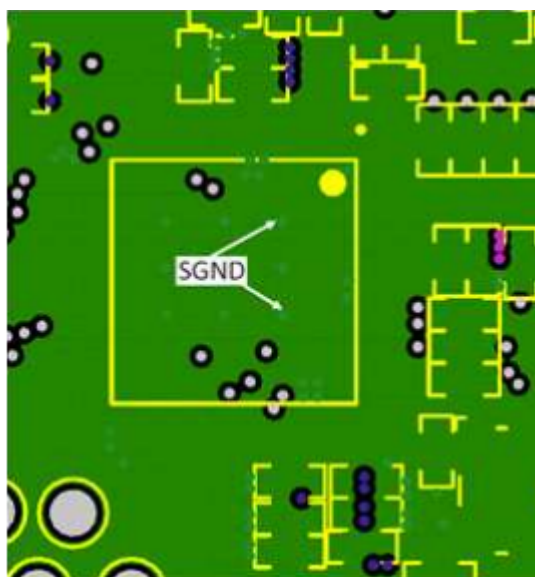


Figure 50. Layout Example

13 器件和文档支持

13.1 器件支持

13.1.1 开发支持

UCD3138x 应用固件在德州仪器 (TI) Code Composer Studio (CCS) 集成开发环境中开发。

特定电源拓扑的器件编程、实时调试以及主要器件参数的监视/配置工作都可通过德州仪器 (TI) 的 FUSION_DIGITAL_POWER_DESIGNER 图形用户界面进行 (http://www.ti.com/tool/fusion_digital_power_designer)。FUSION_DIGITAL_POWER_DESIGNER 软件应用采用 PMBus 协议通过串行总线与器件通信，所使用的接口适配器为德州仪器 (TI) 评估模块 (EVM) USB-TO-GPIO (<http://www.ti.com/tool/usb-to-gpio>)。FUSION_DIGITAL_POWER_DESIGNER GUI 的器件 GUI 模块中的“内存调试器”工具可提供基于 PMBUS 的实时调试功能，这是替代基于 JTAG 的传统方法的有效选择。

该软件应用还可用于器件编程，所使用的工具是针对生产环境进行优化的 FUSION_MFR_GUI (http://www.ti.com/tool/fusion_mfr_gui)。FUSION_MFR_GUI 工具支持多个板载器件，并具有内置记录和报告功能。

13.2 文档支持

13.2.1 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 6. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
UCD3138A64	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCD3138128	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.2.2 相关文档

在参考文档方面，以下编程手册可提供关于 UCD3138x 数字控制器应用和使用方法的详细信息：

- UCD3138064 或 UCD3138128 编程手册
- UCD3138 数字电源外设编程手册 本手册中介绍的关键主题包括：
 - 数字脉宽调制器 (DPWM)
 - 工作模式（正常/多相/相移/谐振等）
 - 自动模式切换
 - 数字脉宽调制控制器 (DPWMC)，边沿生成和内部多路复用
 - 前端
 - 模拟前端
 - ADC 或 EADC 误差
 - 前端 DAC
 - 斜坡模块
 - 逐次逼近寄存器模块
 - 滤波器
 - 滤波器数学函数
 - 环路复用
 - 模拟峰值电流模式
 - 恒定功率/恒定电流 (CPCC)
 - 自动周期调整
 - 故障复用
 - 模拟比较器
 - 数字比较器
 - 故障引脚功能

- DPWM 故障动作
- 理想二极管仿真 (IDE)，断续传导模式 (DCM) 检测
- 振荡器故障检测
- UCD3138A64 或 UCD3138128 中上述全部外设的寄存器映射

3. UCD3138 监视和通信编程手册

本手册中介绍的关键主题包括：

- ADC12
 - 控制、转换、定序和取平均值
 - 数字比较器
 - 温度传感器
 - PMBUS 寻址
 - 双路采样与保持
- 其它模拟控制（电流分流、欠压、时钟门控）
- PMBUS 接口
- 通用输入输出 (GPIO)
- 定时器模块
- PMBus
- UCD3138A64 中上述全部外设的寄存器映射

4. UCD3138 ARM 和数字系统编程手册

本手册中介绍的关键主题包括：

- 引导 ROM 和引导闪存
 - BootROM 函数
 - 存储器读/写功能
 - 校验和函数
 - 闪存函数
 - 避免程序闪存锁定
- ARM7 构架
 - 工作模式
 - 硬件/软件中断
 - 指令集
 - 两种内部工作状态（Thumb 16 位模式/ARM 32 位模式）
- 存储器与系统模块
 - 地址解码器、DEC（存储器映射）
 - 存储器控制器 (MMC)
 - 中央中断模块
- UCD3138A64 或 UCD3138128 中上述全部外设的寄存器映射

5. 适用于 UCD31XX 隔离式电源的 FUSION_DIGITAL_POWER_DESIGNER 应用 – 用户指南

13.2.2.1 参考文档

1. UCD3138064 编程手册（文献编号：SLUUAD8）
2. UCD3138 数字电源外设编程手册（文献编号：SLUU995）
3. UCD3138 监视与通信编程手册（文献编号：SLUU996）
4. UCD3138 ARM 和数字系统编程手册（文献编号：SLUU994）
5. 《隔离电源应用 FUSION_DIGITAL_POWER_DESIGNER》（文献编号：SLUA676）
6. Code Composer Studio 开发工具 v3.3 – 入门指南（文献编号：SPRU509H）
7. ARM7TDMI-S 技术参考手册
8. 系统管理总线 (SMBus) 技术规范
9. PMBus™ 电源系统管理协议规范
10. UCD3138128 编程手册（文献编号：SLUUB54）

除上述工具和文档外，如需获取有关评估模块、参考应用固件和应用手册/设计提示的最新信息，请访问 <http://www.ti.com/product/UCD3138A64>。

13.3 商标

PMBus is a trademark of SMIF, Inc.

All other trademarks are the property of their respective owners.

13.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.5 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCD3138128PFC	ACTIVE	TQFP	PFC	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD3138128	Samples
UCD3138128PFCR	ACTIVE	TQFP	PFC	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD3138128	Samples
UCD3138A64PFC	ACTIVE	TQFP	PFC	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD3138A64	Samples
UCD3138A64PFCR	ACTIVE	TQFP	PFC	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD3138A64	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

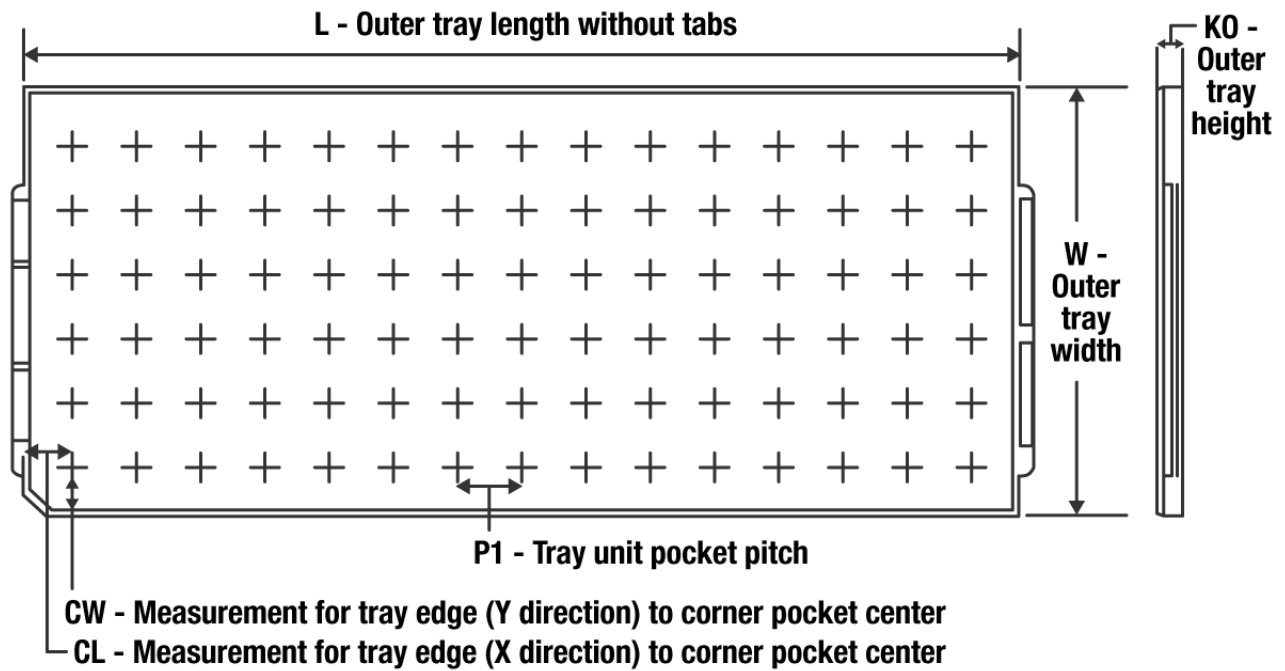
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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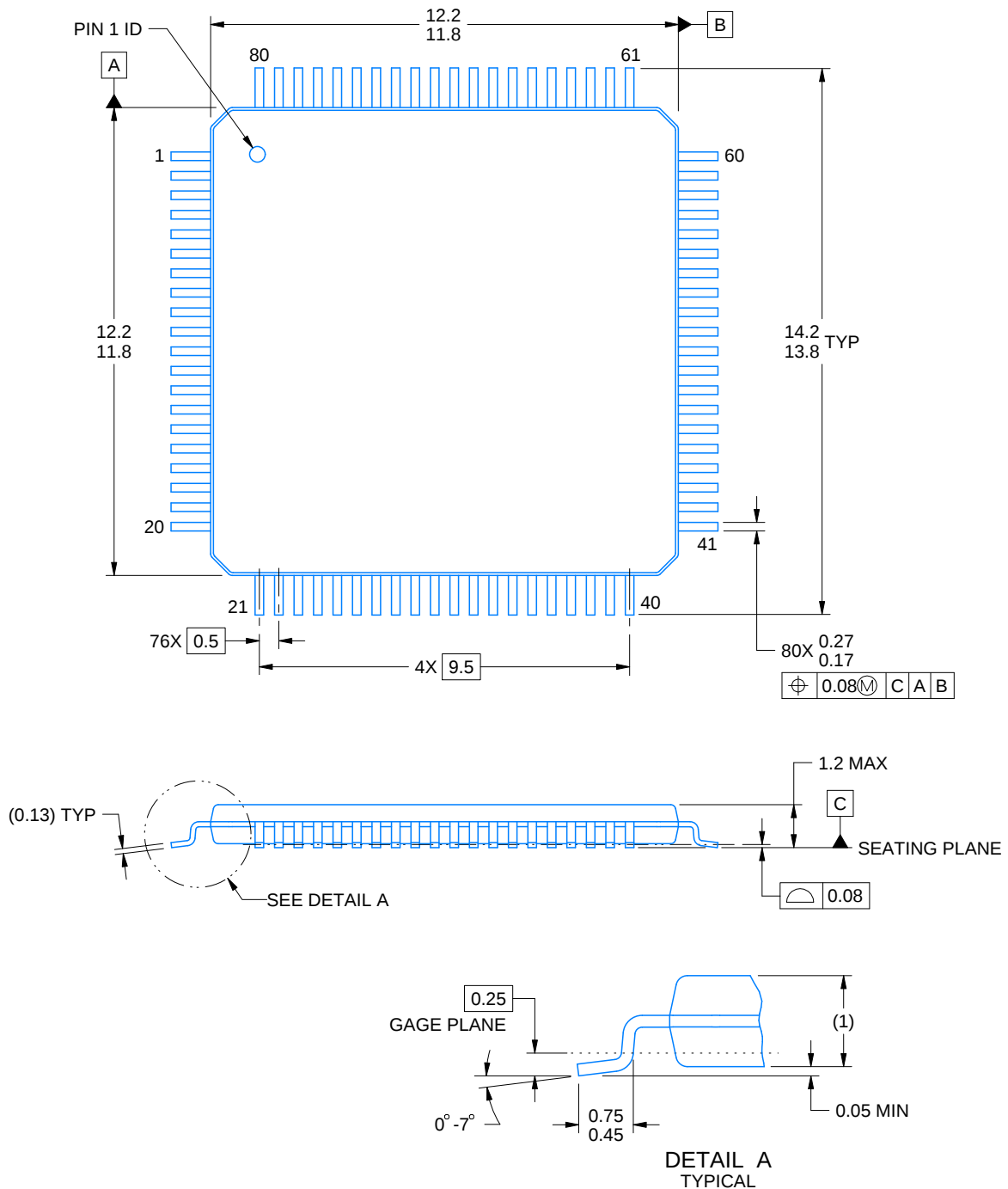
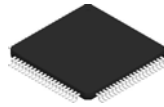
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
UCD3138128PFC	PFC	TQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
UCD3138A64PFC	PFC	TQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3



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NOTES:

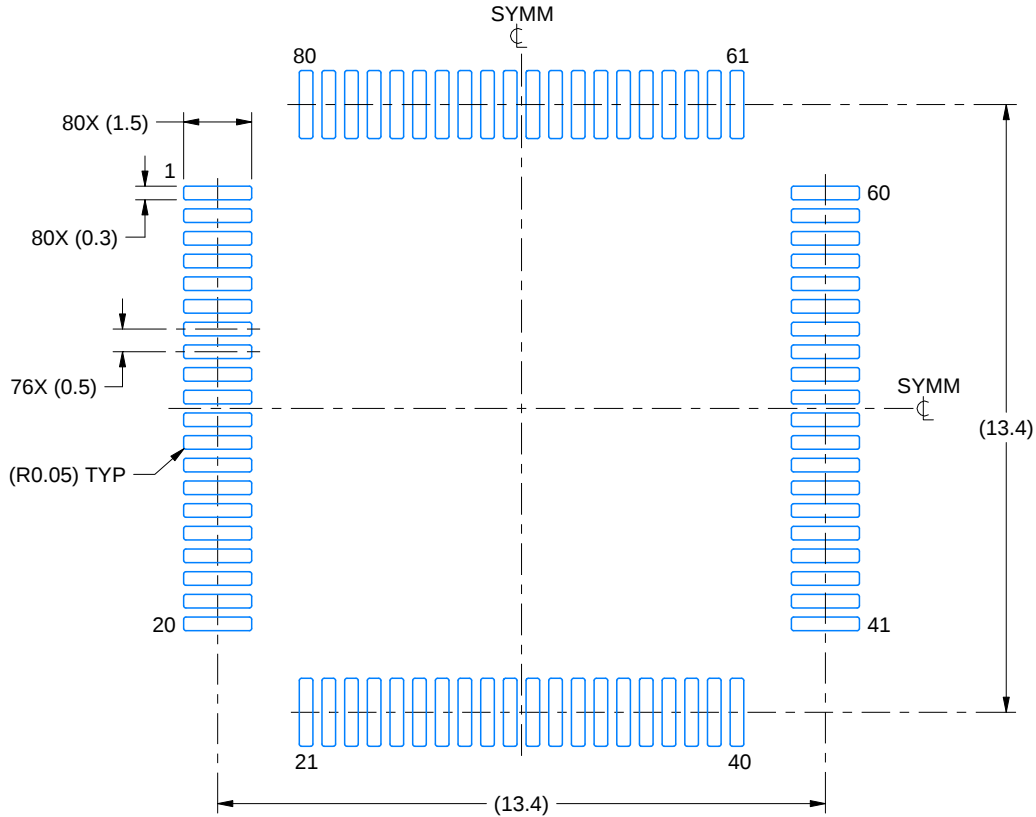
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

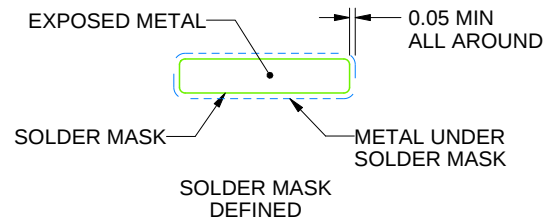
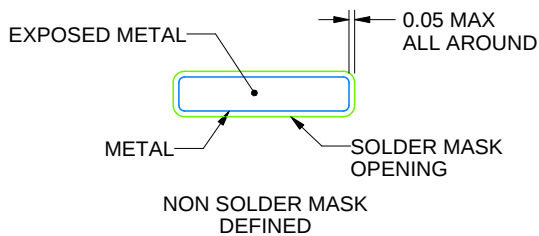
PFC0080A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

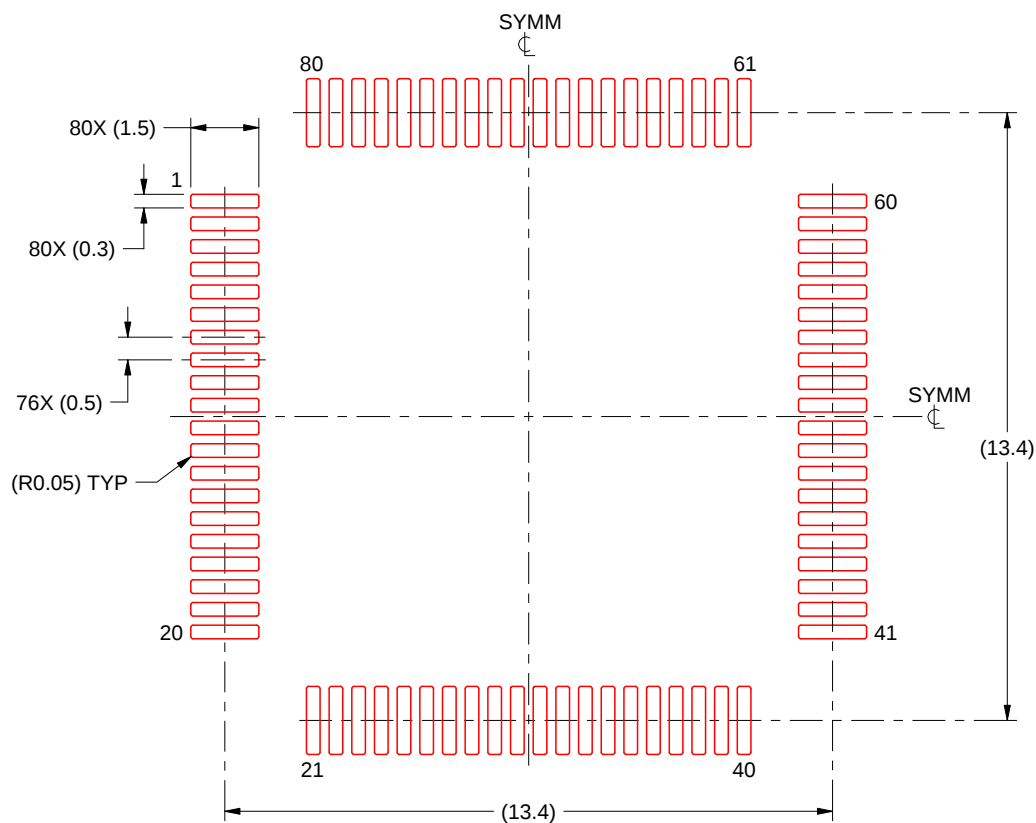
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PFC0080A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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