LP38852-ADJ 1.5-A Fast-Response High-Accuracy Adjustable LDO Linear Regulator With Enable and Soft-Start

1 Features

- Input V_{IN} Range 0.93 V to 5.5 V
- Adjustable V_{OUT} Range 0.8 V to 1.8 V
- Wide V_{BIAS} Supply Operating Range 3 V to 5.5 V
- Dropout Voltage of 130 mV (Typical) at 1.5-A Load Current
- Precision Output Voltage Across All Line and Load Conditions:
  - ±1.5% V_{ADJ} for T_J = 25°C
  - ±2% V_{ADJ} for 0°C ≤ T_J ≤ +125°C
  - ±3% V_{ADJ} for –40°C ≤ T_J ≤ +125°C
- Overtemperature and Overcurrent Protection
- Stable with 10-µF Ceramic Capacitors
- Available in 7-pin TO-220, 7-Pin DDPAK/TO-263, and 8-Pin SO PowerPAD™ Packages
- −40°C to +125°C Operating Junction Temperature Range

2 Applications

- ASIC Power Supplies In:
  - Desktops, Notebooks, and Graphics Cards, Servers
  - Gaming Set Top Boxes, Printers and Copiers
- Server Core and I/O Supplies
- DSP and FPGA Power Supplies
- SMPS Post-Regulator

3 Description

The LP38852-ADJ is a high-current, fast-response regulator which can maintain output voltage regulation with extremely low input-to-output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: V_{BIAS} provides voltage to drive the gate of the N-MOS power transistor, while V_{IN} is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultralow V_{IN} voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of this device makes it suitable for use in powering DSP, microcontroller core voltages, and switch-mode power supply post-regulators.

Dropout Voltage: 130 mV (typical) at 1.5-A load current.

Low Ground Pin Current: 10 mA (typical) at 1.5-A load current.

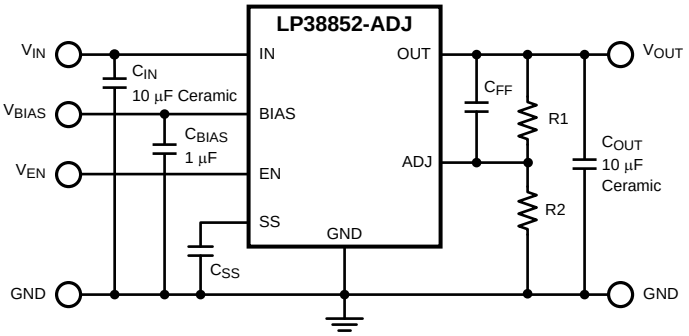
Soft Start: Programmable soft-start time.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP38852-ADJ	DDPAK/TO-263 (7)	10.10 mm × 8.89 mm
	TO-220 (7)	14.986 × 10.16 mm
	SO PowerPAD (8)	4.89 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2013) to Revision F **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and *Thermal Information* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Deleted Lead temperature from Abs Max table; it is in POA ... 4
- Updated thermal information ... 5
- Deleted out-of-date heatsinking subsections ... 17

Changes from Revision D (April 2013) to Revision E **Page**

- Changed layout of National Data Sheet to TI format ... 19

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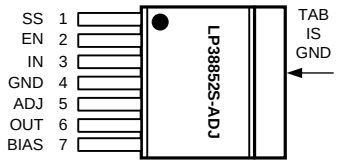
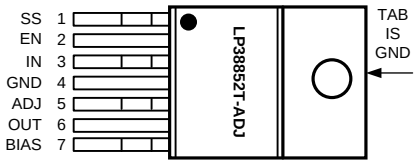
5 Pin Configuration and Functions

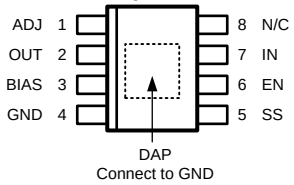
KTW Package
7-Pin DDPAK/TO-263
Top View



NDZ Package
7-Pin TO-220
Top View



DDA Package
8-Pin SO PowerPAD
Top View



Pin Functions

PIN				TYPE	DESCRIPTION
NAME	DDPAK/TO-263	TO-220	SO PowerPAD		
ADJ	5	5	1	O	The feedback connection to set the output voltage
BIAS	7	7	3	I	The supply for the internal control and reference circuitry.
EN	2	2	6	I	Device enable, High = On, Low = Off.
GND	4	4	4	GND	Ground
IN	3	3	7	I	The unregulated voltage input
N/C	-	-	8	—	No internal connection
OUT	6	6	2	O	The regulated output voltage
SS	1	1	5	O	Soft-start capacitor connection. Used to control the rise time of V_{OUT} at turnon.
TAB	TAB	TAB	—	—	The KTW and NDZ TAB is a thermal and electrical connection that is physically attached to the backside of the die, and used as a thermal heat-sink connection.
DAP	—	—	DAP	—	The SO PowerPAD DAP is a thermal connection only that is physically attached to the backside of the die, and used as a thermal heat-sink connection.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
V_{IN} supply voltage (survival)	−0.3	6	V
V_{BIAS} supply voltage (survival)	−0.3	6	V
V_{SS} soft-start voltage (survival)	−0.3	6	V
V_{OUT} voltage (survival)	−0.3	6	V
I_{OUT} current (survival)	Internally Limited		
Junction temperature	−40	150	°C
Power dissipation(3)	Internally Limited		
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/ Distributors for availability and specifications.
(3) Device power dissipation must be de-rated based on device power dissipation (P_D), ambient temperature (T_A), and package junction to ambient thermal resistance ($R_{\theta JA}$). Additional heat-sinking may be required to ensure that the device junction temperature (T_J) does not exceed the maximum operating rating. See the *Application and Implementation* section for details.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN} supply voltage (survival)				(V_{OUT} + V_{DO}) to V_{BIAS}	V
V_{BIAS} supply voltage (survival)(1)	0.8 V ≤ V_{OUT} ≤ 1.2 V	3		5.5	V
	1.2 V < V_{OUT} ≤ 1.8 V	4.5		5.5	V
V_{EN} voltage		0		V_{BIAS}	V
I_{OUT}		0		3	mA
Junction temperature(2)		−40		125	°C

(1) V_{IN} cannot exceed either V_{BIAS} or 4.5 V, whichever value is lower.
(2) Device power dissipation must be de-rated based on device power dissipation (P_D), ambient temperature (T_A), and package junction-to-ambient thermal resistance ($R_{\theta JA}$). Additional heat sinking may be required to ensure that the device junction temperature (T_J) does not exceed the maximum operating rating. See the *Application and Implementation* section for details.

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6.4 Thermal Information

THERMAL METRIC[1]		LP38852-ADJ			UNIT
		KTW (DDPAK/TO-263)	NDZ (TO-220)	DDA (SO PowerPAD)	
		7 PINS	7 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.3	34.0	48.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.6	36.4	54.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.3	25.0	29.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	6.3	9.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.0	23.6	29.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified: V_{OUT} = 0.8 V, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, V_{EN} = V_{BIAS}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = open; typical (TYP) limits are for T_J = 25°C only, and minimum (MIN) and maximum (MAX) limits apply over the junction temperature (T_J) range of –40°C to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ADJ}	V_{ADJ} accuracy	$V_{OUT(NOM)}$+1 V ≤ V_{IN} ≤ V_{BIAS} ≤ 4.5 V[1] 3 V ≤ V_{BIAS} ≤ 5.5 V, 10 mA ≤ I_{OUT} ≤ 1.5 A T_J = 25°C	492.5	500.	507.5	mV
		$V_{OUT(NOM)}$+1 V ≤ V_{IN} ≤ V_{BIAS} ≤ 4.5 V[1] 3 V ≤ V_{BIAS} ≤ 5.5 V, 10 mA ≤ I_{OUT} ≤ 1.5 A	485		515	
		$V_{OUT(NOM)}$+1 V ≤ V_{IN} ≤ V_{BIAS} ≤ 4.5 V[1] 3 V ≤ V_{BIAS} ≤ 5.5 V, 10 mA ≤ I_{OUT} ≤ 1.5 A, 0°C ≤ T_J ≤ +125°C	490	500.	510	
V_{OUT}	V_{OUT} range	3 V ≤ V_{BIAS} ≤ 5.5 V	0.8		1.2	V
		4.5 V ≤ V_{BIAS} ≤ 5.5 V	0.8		1.8	
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation, V_{IN}[2]	$V_{OUT(NOM)}$+1 V ≤ V_{IN} ≤ V_{BIAS}		0.04		%/V
$\Delta V_{OUT}/\Delta V_{BIAS}$	Line regulation, V_{BIAS}[2]	3 V ≤ V_{BIAS} ≤ 5.5 V		0.1		%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Output voltage load regulation[3]	10 mA ≤ I_{OUT} ≤ 1.5 A		0.2		%/A
V_{DO}	Dropout voltage[4]	I_{OUT} = 1.5 A, T_J = 25°C		130	165	mV
		I_{OUT} = 1.5 A			180	
$I_{GND(IN)}$	Quiescent current drawn from V_{IN} supply	V_{OUT} = 0.8 V, V_{BIAS} = 3 V 10 mA ≤ I_{OUT} ≤ 1.5 A T_J = 25°C		7	8.5	mA
		V_{OUT} = 0.8 V, V_{BIAS} = 3 V 10 mA ≤ I_{OUT} ≤ 1.5 A			9	
		V_{EN} ≤ 0.5 V, T_J = 25°C		1	100	µA
		V_{EN} ≤ 0.5 V			300	
$I_{GND(BIAS)}$	Quiescent current drawn from V_{BIAS} supply	10 mA ≤ I_{OUT} ≤ 1.5 A, T_J = 25°C		3	3.8	mA
		10 mA ≤ I_{OUT} ≤ 1.5 A			4.5	
		V_{EN} ≤ 0.5 V, T_J = 25°C		100	170	µA
		V_{EN} ≤ 0.5 V			200	

(1) V_{IN} cannot exceed either V_{BIAS} or 4.5 V, whichever value is lower.
(2) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
(3) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.
(4) Dropout voltage is defined as the input to output voltage differential (V_{IN} – V_{OUT}) where the input voltage is low enough to cause the output voltage to drop 2% from the nominal value.

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Electrical Characteristics (continued)

Unless otherwise specified: V_{OUT} = 0.8 V, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, V_{EN} = V_{BIAS}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = open; typical (TYP) limits are for T_J = 25°C only, and minimum (MIN) and maximum (MAX) limits apply over the junction temperature (T_J) range of –40°C to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO	Undervoltage lockout threshold	V_{BIAS} rising until device is functional T_J = 25°C	2.2	2.45	2.7	V
		V_{BIAS} rising until device is functional	2		2.9	
$UVLO_{(HYS)}$	Undervoltage lockout hysteresis	V_{BIAS} falling from UVLO threshold until device is non-functional T_J = 25°C	60	150	300	mV
		V_{BIAS} falling from UVLO threshold until device is non-functional	50		350	
I_{SC}	Output short-circuit current	V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, V_{OUT} = 0 V		4.5		A
SOFT-START						
r_{SS}	Soft-start internal resistance		11	13.5	16	kΩ
t_{SS}	Soft-start time t_{SS} = C_{SS} × r_{SS} × 5	C_{SS} = 10 nF		675		µs
ENABLE						
I_{EN}	ENABLE pin current	V_{EN} = V_{BIAS}		0.01		µA
		V_{EN} = 0 V, V_{BIAS} = 5.5 V, T_J = 25°C	–19	–30	–40	
		V_{EN} = 0 V, V_{BIAS} = 5.5 V	–13		–51	
$V_{EN(ON)}$	Enable voltage threshold	V_{EN} rising until output = ON, T_J = 25°C	1	1.25	1.5	V
		V_{EN} rising until output = ON	0.9		1.55	
$V_{EN(HYS)}$	Enable voltage hysteresis	V_{EN} falling from $V_{EN(ON)}$ until Output = OFF T_J = 25°C	50	100	150	mV
		V_{EN} falling from $V_{EN(ON)}$ until Output = OFF	30		200	
AC PARAMETERS						
PSRR (V_{IN})	Ripple rejection for V_{IN} input voltage	V_{IN} = $V_{OUT(NOM)}$ + 1 V, f = 120 Hz		80		dB
		V_{IN} = $V_{OUT(NOM)}$ + 1 V, f = 1 kHz		65		
PSRR (V_{BIAS})	Ripple rejection for V_{BIAS} voltage	V_{BIAS} = $V_{OUT(NOM)}$ + 3 V, f= 120 Hz		58		dB
		V_{BIAS} = $V_{OUT(NOM)}$ + 3 V, f = 1 kHz		58		
e_n	Output noise density	f = 120 Hz		1		µV/√Hz
	Output noise voltage	BW = 10 Hz − 100 kHz		150		$µV_{RMS}$
		BW = 300 Hz − 300 kHz		90		
THERMAL PARAMETERS						
T_{SD}	Thermal shutdown junction temperature			160		°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis			10		°C

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{OFF}	Turnoff delay time, R_{LOAD} x C_{OUT} << t_{OFF}		20		µs
t_{ON}	Turnon delay time, R_{LOAD} x C_{OUT} << t_{ON}		15		µs

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6.7 Typical Characteristics

Refer to the *Typical Application Circuit*. Unless otherwise specified: T_J = 25°C, R1 = 1.4 kΩ, R2 = 1 kΩ, C_{FF}= 0.01 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, I_{OUT} = 10 mA, C_{IN} = 10-µF ceramic, C_{OUT} = 10-µF ceramic, C_{BIAS} = 1-µF Ceramic, C_{SS} = open.

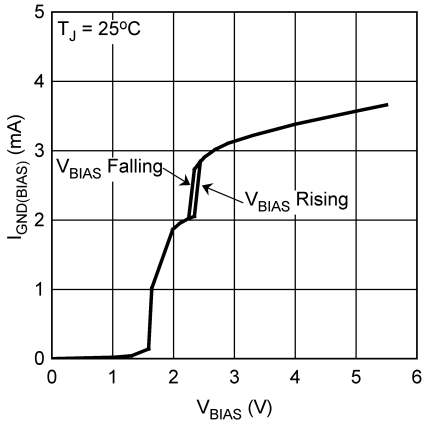

Figure 1. V_{BIAS} Ground Pin Current ($I_{GND(BIAS)}$) vs V_{BIAS}

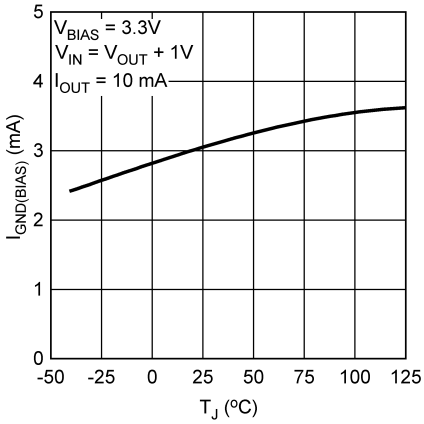

Figure 2. V_{BIAS} Ground Pin Current ($I_{GND(BIAS)}$) vs Temperature

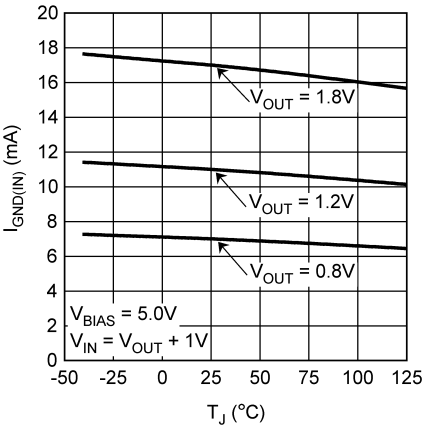

Figure 3. V_{IN} Ground Pin Current vs Temperature

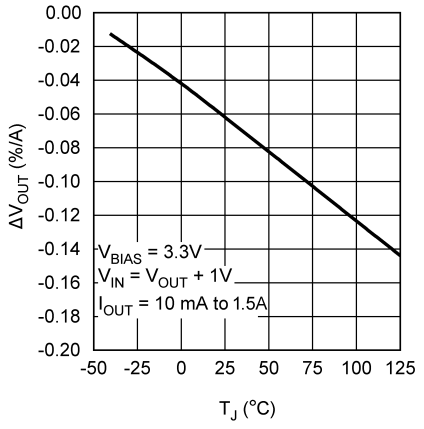

Figure 4. Load Regulation vs Temperature

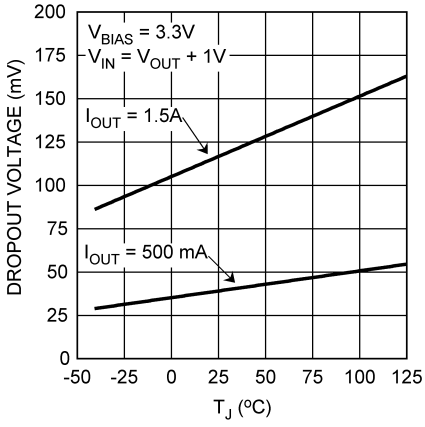

Figure 5. Dropout Voltage (V_{DO}) vs Temperature

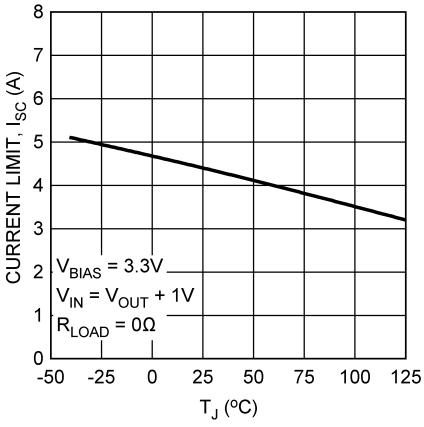

Figure 6. Output Current Limit (I_{SC}) vs Temperature

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Typical Characteristics (continued)

Refer to the *Typical Application Circuit*. Unless otherwise specified: T_J = 25°C, R1 = 1.4 kΩ, R2 = 1 kΩ, C_{FF}= 0.01 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, I_{OUT} = 10 mA, C_{IN} = 10-µF ceramic, C_{OUT} = 10-µF ceramic, C_{BIAS} = 1-µF Ceramic, C_{SS} = open.

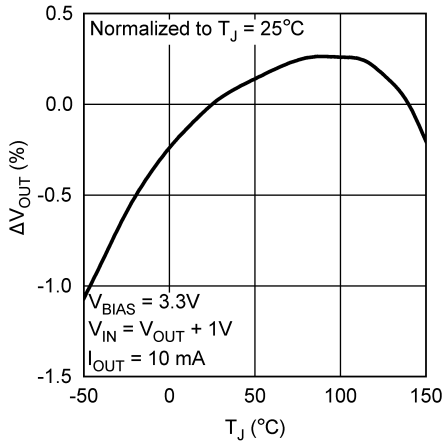

Figure 7. V_{OUT} vs Temperature

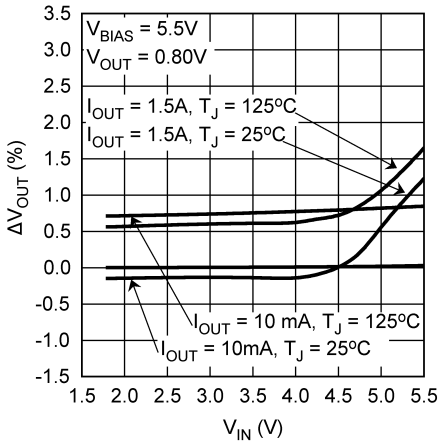

Figure 8. V_{OUT} vs V_{IN}

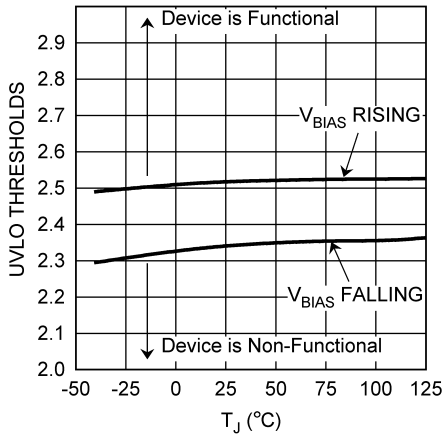

Figure 9. UVLO Thresholds vs Temperature

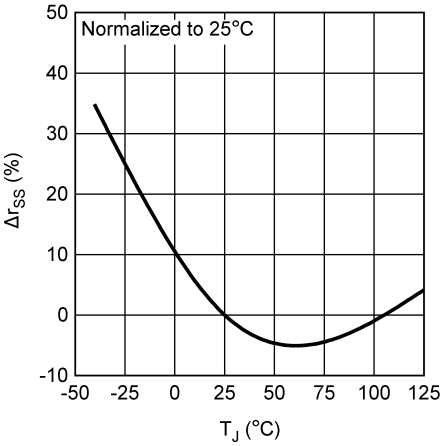

Figure 10. Soft-Start R_{SS} Variation vs Temperature

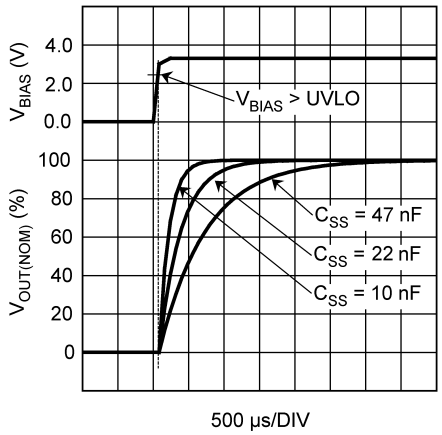

Figure 11. V_{OUT} vs C_{SS}

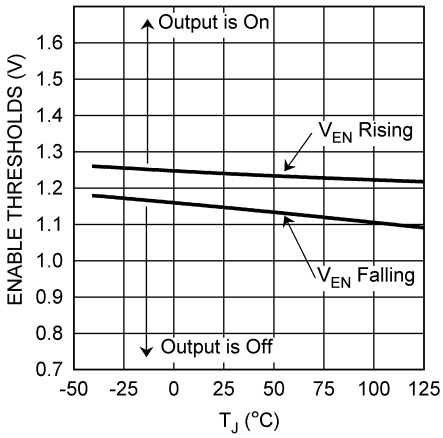

Figure 12. Enable Thresholds (V_{EN}) vs Temperature

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Typical Characteristics (continued)

Refer to the *Typical Application Circuit*. Unless otherwise specified: T_J = 25°C, R1 = 1.4 kΩ, R2 = 1 kΩ, C_{FF}= 0.01 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, I_{OUT} = 10 mA, C_{IN} = 10-µF ceramic, C_{OUT} = 10-µF ceramic, C_{BIAS} = 1-µF Ceramic, C_{SS} = open.

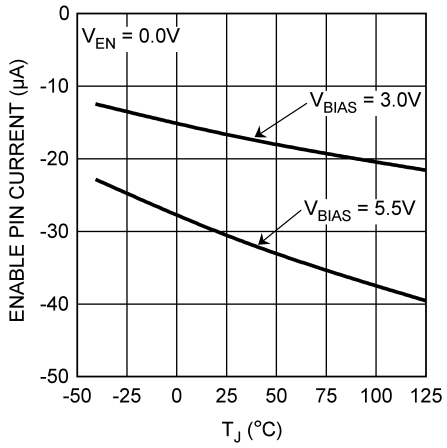

Figure 13. Enable Pulldown Current (I_{EN}) vs Temperature

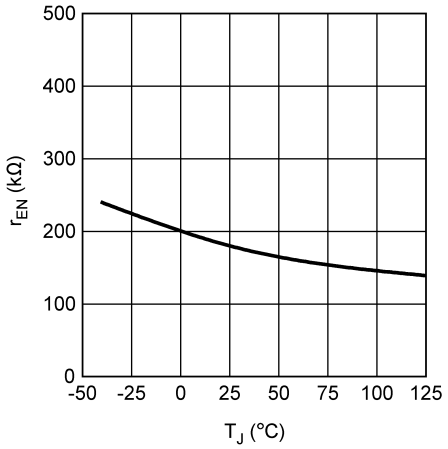

Figure 14. Enable Pullup Resistor (R_{EN}) vs Temperature

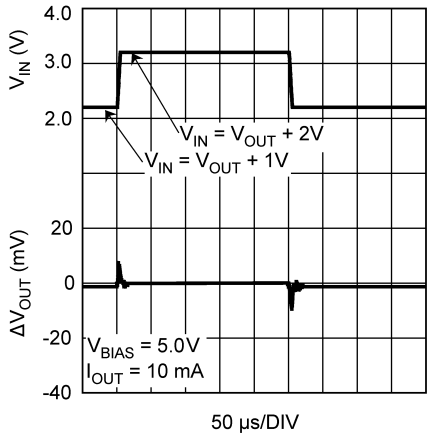

Figure 15. V_{IN} Line Transient Response

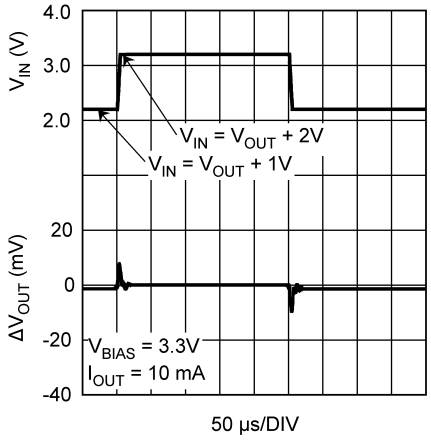

Figure 16. V_{IN} Line Transient Response

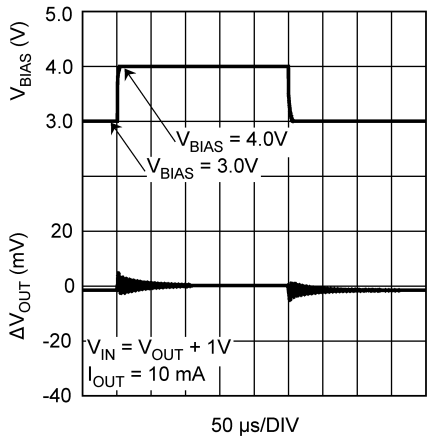

Figure 17. V_{BIAS} Line Transient Response

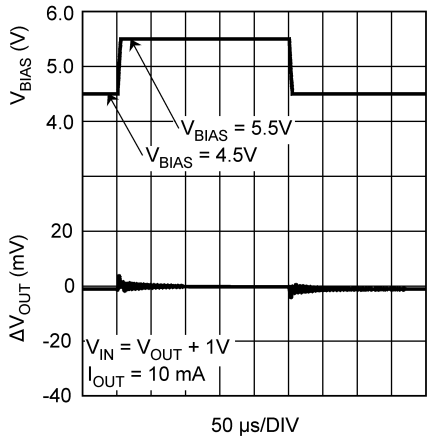

Figure 18. V_{BIAS} Line Transient Response

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Typical Characteristics (continued)

Refer to the *Typical Application Circuit*. Unless otherwise specified: T_J = 25°C, R1 = 1.4 kΩ, R2 = 1 kΩ, C_{FF}= 0.01 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, I_{OUT} = 10 mA, C_{IN} = 10-µF ceramic, C_{OUT} = 10-µF ceramic, C_{BIAS} = 1-µF Ceramic, C_{SS} = open.

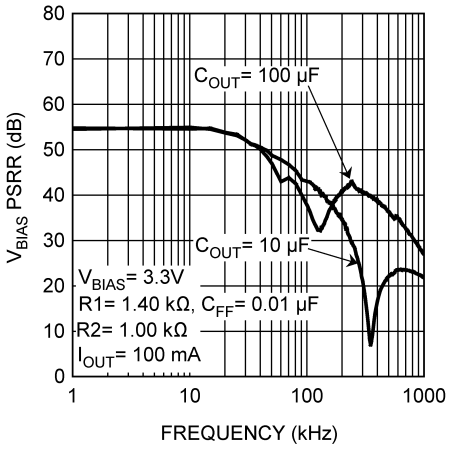

Figure 19. V_{BIAS} PSRR

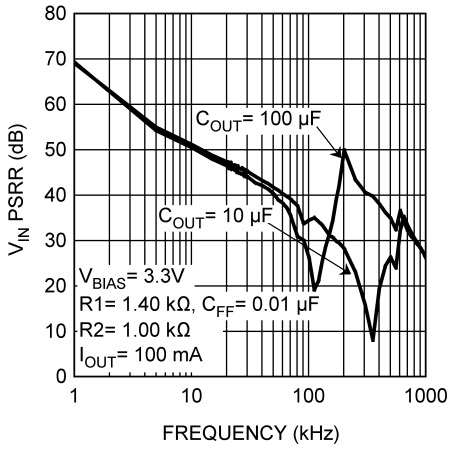

Figure 20. V_{IN} PSRR

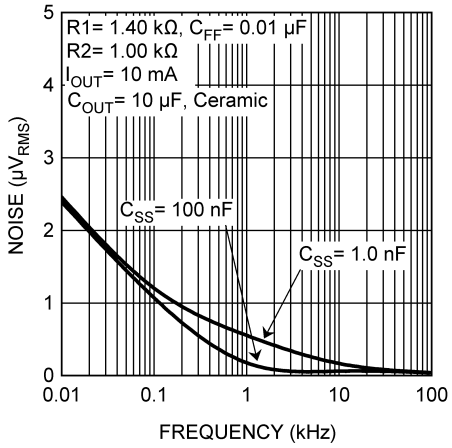

Figure 21. Output Noise

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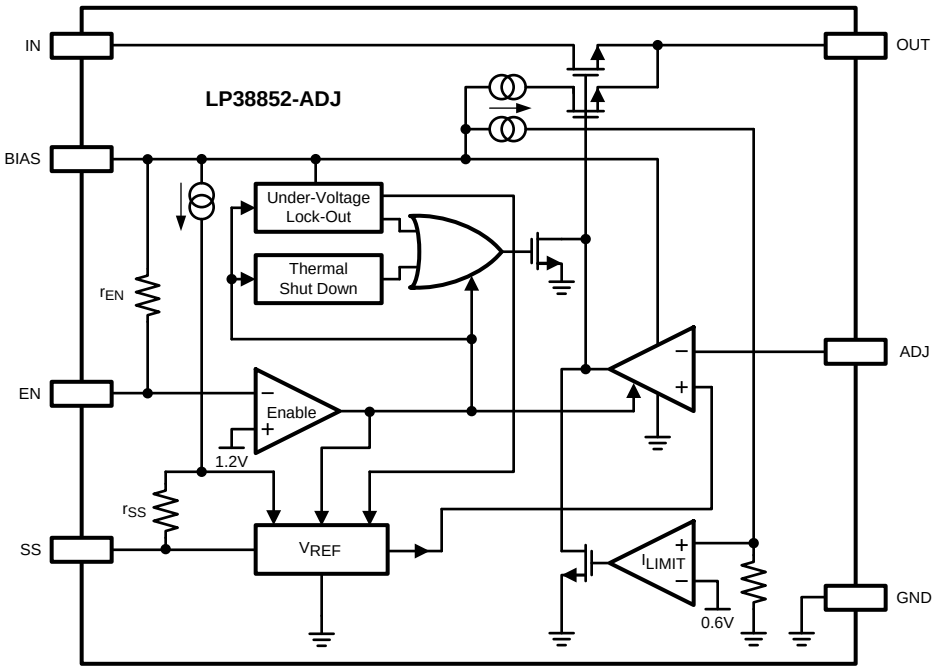
7 Detailed Description

7.1 Overview

The LP38852-ADJ is a high-current, low-dropout, fast-response linear regulator capable of sourcing 1.5-A load with only 130-mV dropout. This device operates from two input voltages: V_{BIAS} provides voltage to internal circuit, while V_{IN} is the input voltage supplying power to load. The use of an external bias rail allows the part to operate from ultra-low V_{IN} voltages. The fast transient response of this device makes it suitable for powering DSP, microcontroller cores, and post-regulators.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The bias voltage is monitored by a circuit which prevents the device from functioning when the bias voltage is below the UVLO threshold of approximately 2.45 V.

As the bias voltage rises above the UVLO threshold the device control circuitry becomes active. There is approximately 150 mV of hysteresis built into the UVLO threshold to provide noise immunity.

When the bias voltage is between the UVLO threshold and the minimum operating rating value of 3 V the device is functional, but the operating parameters are not within the specified limits.

7.3.2 Supply Sequencing

There is no requirement for the order that V_{IN} or V_{BIAS} are applied or removed.

One practical limitation is that the soft-start circuit starts charging soft-start timing capacitor (C_{SS}) when both V_{BIAS} rises above the UVLO threshold and the EN pin is above the $V_{EN(ON)}$ threshold. If the application of V_{IN} is delayed beyond this point the benefits of soft start is compromised.

In any case, the output voltage cannot be ensured until both V_{IN} and V_{BIAS} are within the range of specified operating values.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the OUT pin must be diode clamped to ground. A Schottky diode is recommended for this diode clamp.

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Feature Description (continued)

7.3.3 Reverse Voltage

A reverse voltage condition exists when the voltage at the OUT pin is higher than the voltage at the IN pin. Typically this happens when V_{IN} is abruptly taken low, and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed.

The NMOS pass element, by design, contains no body diode. This means that, as long as the gate of the pass element is not driven, there is no reverse current flow through the pass element during a reverse voltage event. The gate of the pass element is not driven when V_{BIAS} is below the UVLO threshold, or when the EN pin is held low.

When V_{BIAS} is above the UVLO threshold, and the EN pin is above the $V_{EN(ON)}$ threshold, the control circuitry is active and attempts to regulate the output voltage. Because the input voltage is less than the output voltage the control circuit drives the gate of the pass element to the full V_{BIAS} potential when the output voltage begins to fall. In this condition, reverse current flows from the OUT pin to the IN pin , limited only by the $R_{DS(ON)}$ of the pass element and the output-to-input voltage differential. Discharging an output capacitor up 1000 µF in this manner does not damage the device as the current rapidly decays. However, continuous reverse current must be avoided.

7.3.4 Soft-Start

The LP38852-ADJ incorporates a soft-start function that reduces the start-up current surge into the output capacitor (C_{OUT}) by allowing V_{OUT} to rise slowly to the final value. This is accomplished by controlling V_{REF} at the SS pin. C_{SS} is internally held to ground until both V_{BIAS} rises above the UVLO threshold and the EN pin is higher than the $V_{EN(ON)}$ threshold.

V_{REF} rises at an RC rate defined by the internal resistance of the SS pin (r_{SS}) and the external capacitor connected to the SS pin. This allows the output voltage to rise in a controlled manner until steady-state regulation is achieved. Typically, five time constants are recommended to assure that the output voltage is sufficiently close to the final steady-state value. During the soft-start time the output current can rise to the built-in current limit.

$$\text{Soft-Start Time} = C_{SS} \times r_{SS} \times 5 \quad (1)$$

Because the V_{OUT} rise is exponential, not linear, the in-rush current peaks during the first time constant (τ), and V_{OUT} requires four additional time constants (4τ) to reach the final value (5τ) .

After achieving normal operation, if either V_{BIAS} falls below the ULVO threshold, or the EN pin falls below the $V_{EN(OFF)}$ threshold, the device output is disabled, and the C_{SS} discharge circuit becomes active. The C_{SS} discharge circuit remains active until V_{BIAS} falls to 500 mV (typical). When V_{BIAS} falls below 500 mV (typical), the C_{SS} discharge circuit ceases to function due to a lack of sufficient biasing to the control circuitry.

Because V_{REF} appears on the SS pin, any leakage through C_{SS} causes V_{REF} to fall, thus affecting V_{OUT}. A leakage of 50 nA (about 10 MΩ) through C_{SS} causes V_{OUT} to be approximately 0.1% lower than nominal, while a leakage of 500 nA (about 1 MΩ) causes V_{OUT} to be approximately 1% lower than nominal. Typical ceramic capacitors have a factor of 10× difference in leakage between 25°C and 85°C, so the maximum ambient temperature must be included in the capacitor selection process.

Typical C_{SS} values are in the range of 1 nF to 100 nF, providing typical soft-start times in the range of 70 µs to 7 ms (5τ). Values less than 1 nF may be used, but the soft-start effect is minimal. Values larger than 100 nF provide soft start but may not be fully discharged if V_{BIAS} falls from the UVLVO threshold to less than 500 mV in less than 100 µs.

Figure 22 shows the relationship between the C_{OUT} value and a typical C_{SS} value.

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Feature Description (continued)

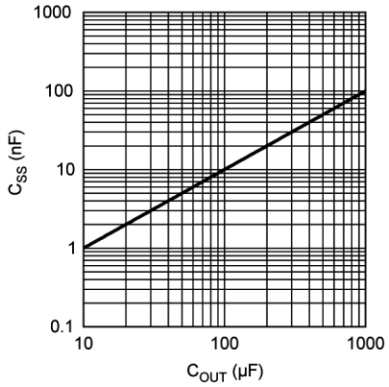

Figure 22. Typical C_{SS} vs C_{OUT} Values

The C_{SS} capacitor must be connected to a clean ground path back to the device ground pin. No components, other than C_{SS}, should be connected to the SS pin, as there could be adverse effects to V_{OUT}.

If the soft-start function is not needed the SS pin must be left open, although some minimal capacitance value is always recommended.

7.3.5 Setting The Output Voltage

The output voltage is set using the external resistive divider R1 and R2. (Refer to the Figure 23.) The output voltage is given by Equation 2:

$$V_{OUT} = V_{ADJ} \times \left(1 + \left(\frac{R1}{R2}\right)\right) \quad (2)$$

The resistors used for R1 and R2 must be high quality, tight tolerance, and with matching temperature coefficients. It is important to remember that, although the value of V_{ADJ} is specified, the use of low quality resistors for R1 and R2 can easily produce a V_{OUT} value that is unacceptable.

It is recommended that the values selected for R1 and R2 are such that the parallel value is less than 10 kΩ. This is to prevent internal parasitic capacitances on the ADJ pin from interfering with the F_Z pole set by R1 and C_{FF}.

$$((R1 \times R2) / (R1 + R2)) \leq 10\ k\Omega \quad (3)$$

Table 1 lists some suggested, best fit, standard ±1% resistor values for R1 and R2, and a standard ±10% capacitor values for C_{FF}, for a range of V_{OUT} values. Other values of R1, R2, and C_{FF} are available that give similar results.

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Table 1. Suggested Resistor Values

V_{OUT}	R1	R2	C_{FF}	F_Z
0.8 V	1.07 kΩ	1.78 kΩ	12 nF	12.4 kHz
0.9 V	1.50 kΩ	1.87 kΩ	8.2 nF	12.9 kHz
1 V	1.00 kΩ	1.00 kΩ	12 nF	13.3 kHz
1.1 V	1.65 kΩ	1.37 kΩ	8.2 nF	11.8 kHz
1.2 V	1.40 kΩ	1.00 kΩ	10 nF	11.4 kHz
1.3 V	1.15 kΩ	715 Ω	12 nF	11.5 kHz
1.4 V	1.07 kΩ	590 Ω	12 nF	12.4 kHz
1.5 V	2.00 kΩ	1.00 kΩ	6.8 nF	11.7 kHz
1.6 V	1.65 kΩ	750 Ω	8.2 nF	11.8 kHz
1.7 V	2.55 kΩ	1.07 kΩ	5.6 nF	11.1 kHz
1.8 V	2.94 kΩ	1.13 kΩ	4.7 nF	11.5 kHz

Please refer to the TI Application Note AN-1378 *Method for Calculating Output Voltage Tolerances in Adjustable Regulators* (SNVA112) for additional information on how resistor tolerances affect the calculated V_{OUT} value.

7.3.6 Enable (EN)

The EN pin provides a mechanism to enable, or disable, the regulator output stage. The EN pin has an internal pullup to V_{BIAS} through a 180-kΩ (typical) resistor. The EN pin can be left open or connected V_{BIAS} if the enable function is not needed.

7.4 Device Functional Modes

7.4.1 Input Voltage

The input voltage (V_{IN}) is the high-current external voltage rail that is regulated down to a lower voltage, which is applied to the load. The input voltage must be at least V_{OUT} + V_{DO} and no higher than whatever value is used for V_{BIAS}.

For applications where V_{BIAS} is higher than 4.5 V, V_{IN} must be no greater than 4.5 V, otherwise output voltage accuracy may be affected.

7.4.2 Bias Voltage

The bias voltage (V_{BIAS}) is a low-current external voltage rail required to bias the control circuitry and provide gate drive for the N-FET pass transistor. When V_{OUT} is set to 1.2 V, or less, V_{BIAS} may be anywhere in the operating range of 3 V to 5.5 V. If V_{OUT} is set higher than 1.2 V , V_{BIAS} must be between 4.5 V and 5.5 V to ensure proper operation of the device.

7.4.3 Enable (EN) Operation

If the EN pin is actively driven, pulling the EN pin above the V_{EN} threshold of 1.25 V (typical) turns on the regulator output; pulling the EN pin below the V_{EN} threshold turns off the regulator output. There is approximately 100 mV of hysteresis built into the enable threshold provide noise immunity.

If the enable function is not needed the EN pin must be left open, or connected directly to V_{BIAS}. If the EN pin is left open, stray capacitance on this pin must be minimized; otherwise, the output turnon is delayed while the stray capacitance is charged through the internal resistance (r_{EN}).

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The typical applications of the LP38852-ADJ include DSP supply, microcontroller supplies, and post regulators.

8.2 Typical Application

Figure 23 shows the typical application circuit for LP38852-ADJ.

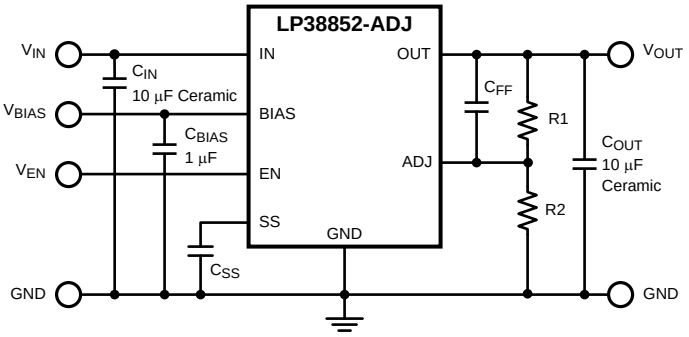

Figure 23. LP38852-ADJ Typical Application

8.2.1 Design Requirements

For typical linear regulator applications, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.3 V
Adjustable output voltage	0.8 V to 1.8 V
Output current	1.5 A

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

To assure regulator stability, input and output capacitors are required as shown in the Figure 23.

8.2.2.1.1 Input Capacitor

The input capacitor must be at least 10 µF, but can be increased without limit. Its purpose is to provide a low source impedance for the regulator input. A ceramic capacitor, X5R or X7R, is recommended.

Tantalum capacitors may also be used at the input pin. There is no specific equivalent series resistance (ESR) limitation on the input capacitor (the lower, the better).

Aluminum electrolytic capacitors can be used, but are not recommended as their ESR increases very quickly at cold temperatures. They are not recommended for any application where the ambient temperature falls below 0°C.

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8.2.2.1.2 Output Capacitor

A minimum output capacitance of 10 µF, ceramic, is required for stability. The amount of output capacitance can be increased without limit. The output capacitor must be located less than 1 cm from the output pin of the device and returned to the device ground pin with a clean analog ground.

Only high-quality ceramic types such as X5R or X7R are recommended, as the Z5U and Y5F types do not provide sufficient capacitance over temperature.

Tantalum capacitors also provide stable operation across the entire operating temperature range. However, the effects of ESR may provide variations in the output voltage during fast load transients. Using the minimum recommended 10-µF ceramic capacitor at the output allows unlimited capacitance, tantalum or aluminum, to be added in parallel.

8.2.2.1.3 Bias Capacitor

The capacitor on the bias pin must be at least 1 µF and can be any good-quality capacitor (ceramic is recommended).

8.2.2.1.4 Setting the Output Voltage

According to Table 1, R1 is set to 1.07 kΩ, and R2 is set to 1.78 kΩ.

8.2.2.1.5 Feed Forward Capacitor, C_{FF}

When using a ceramic capacitor for C_{OUT}, the typical ESR value is too small to provide any meaningful positive phase compensation, F_Z, to offset the internal negative phase shifts in the gain loop (see Figure 23).

$$F_Z = (1 / (2 \times \pi \times C_{OUT} \times ESR)) \quad (4)$$

A capacitor placed across the gain resistor R1 provides additional phase margin to improve load transient response of the device. This capacitor, C_{FF}, in parallel with R1, forms a zero in the loop response given by the formula:

$$F_Z = (1 / (2 \times \pi \times C_{FF} \times R1)) \quad (5)$$

For optimum load transient response select C_{FF} so the zero frequency, F_Z, falls between 10 kHz and 15 kHz.

$$(C_{FF} = (1 / (2 \times \pi \times R1 \times F_Z)) \quad (6)$$

The phase lead provided by C_{FF} diminishes as the DC gain approaches unity, or V_{OUT} approaches V_{ADJ}. This is because C_{FF} also forms a pole with a frequency of:

$$F_P = (1 / (2 \times \pi \times C_{FF} \times (R1 \parallel R2))) \quad (7)$$

NOTE

It is important that at higher output voltages, where R1 is much larger than R2, the pole and zero are far apart in frequency. At lower output voltages the frequency of the pole and the zero move closer together. The phase lead provided from C_{FF} diminishes quickly as the output voltage is reduced and has no effect when $V_{OUT} = V_{ADJ}$. For this reason, relying on this compensation technique alone is adequate only for higher output voltages. For the LP38852-ADJ, the practical minimum V_{OUT} is 0.8 V when a ceramic capacitor is used for C_{OUT}.

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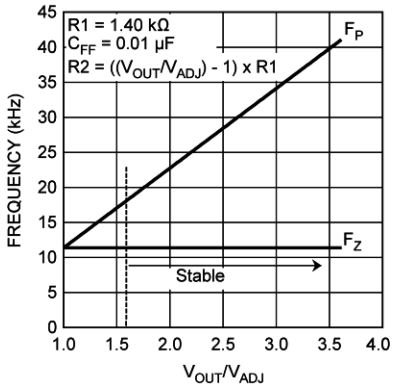

Figure 24. F_{ZERO} and F_{POLE} vs Gain

8.2.2.2 Power Dissipation and Heat Sinking

Additional copper area for heat sinking may be required depending on the maximum device dissipation (P_D) and the maximum anticipated ambient temperature (T_A) for the device. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

The total power dissipation of the device is the sum of three different points of dissipation in the device.

The first part is the power that is dissipated in the NMOS pass element, and can be determined with Equation 8:

$$P_{D(PASS)} = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (8)$$

The second part is the power that is dissipated in the bias and control circuitry and can be determined with Equation 9:

$$P_{D(BIAS)} = V_{BIAS} \times I_{GND(BIAS)}$$

where

- $I_{GND(BIAS)}$ is the portion of the operating ground current of the device that is related to V_{BIAS}. (9)

The third part is the power that is dissipated in portions of the output stage circuitry and can be determined with Equation 10:

$$P_{D(IN)} = V_{IN} \times I_{GND(IN)}$$

where

- $I_{GND(IN)}$ is the portion of the operating ground current of the device that is related to V_{IN}. (10)

The total power dissipation is then:

$$P_D = P_{D(PASS)} + P_{D(BIAS)} + P_{D(IN)} \quad (11)$$

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum anticipated ambient temperature (T_A) for the application, and the maximum allowable operating junction temperature ($T_{J(MAX)}$) .

$$\Delta T_J = T_{J(MAX)} – T_{A(MAX)} \quad (12)$$

The maximum allowable value for junction-to-ambient thermal resistance, $R_{\theta JA}$, can be calculated using Equation 13:

$$R_{\theta JA} \leq \Delta T_J / P_D \quad (13)$$

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8.2.3 Application Curves

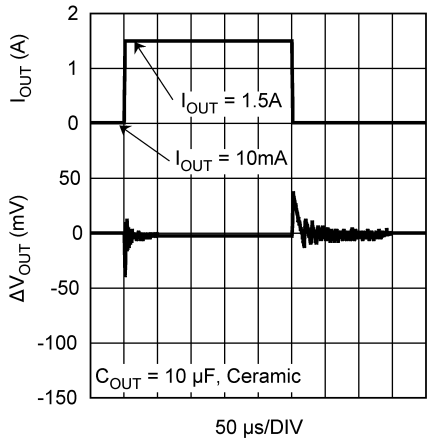

Figure 25. Load Transient Response

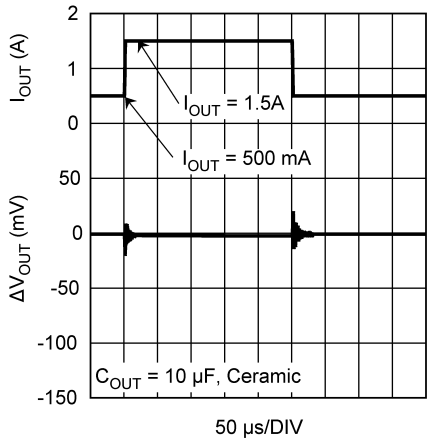

Figure 26. Load Transient Response

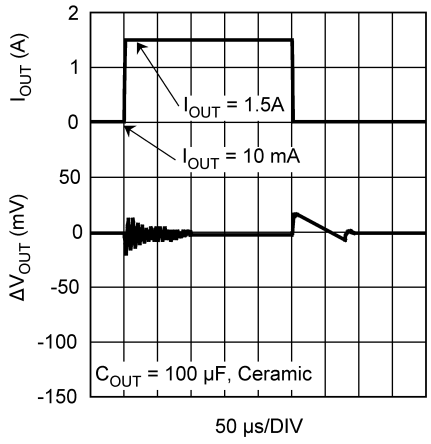

Figure 27. Load Transient Response

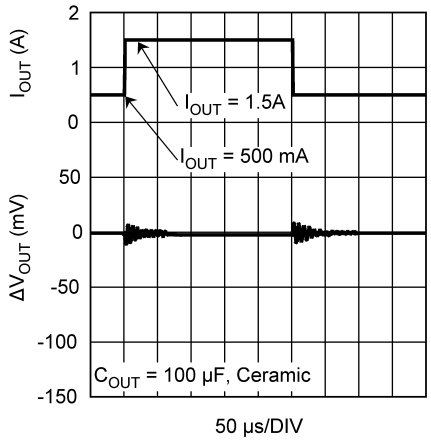

Figure 28. Load Transient Response

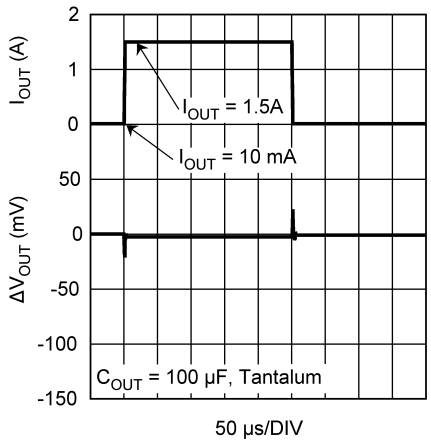

Figure 29. Load Transient Response

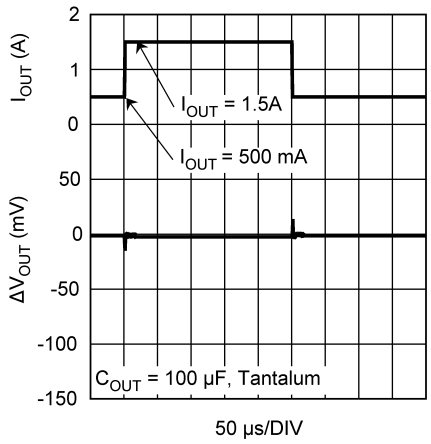

Figure 30. Load Transient Response

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9 Power Supply Recommendations

The LP38852-ADJ device is designed to operate from an input voltage supply range between 3 V and 5.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. An input capacitor of at least 10 µF is required.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near to the respective LDO pin connections as practical. Place ground return connections to the input and output capacitor, and to the LDO ground pin, as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitic, and thereby reduces load current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and it behaves similarly to a thermal plane to spread heat from the LDO device when connected to the SO PowerPAD. In most application, this ground plane is necessary to meet thermal requirements.

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10.2 Layout Examples

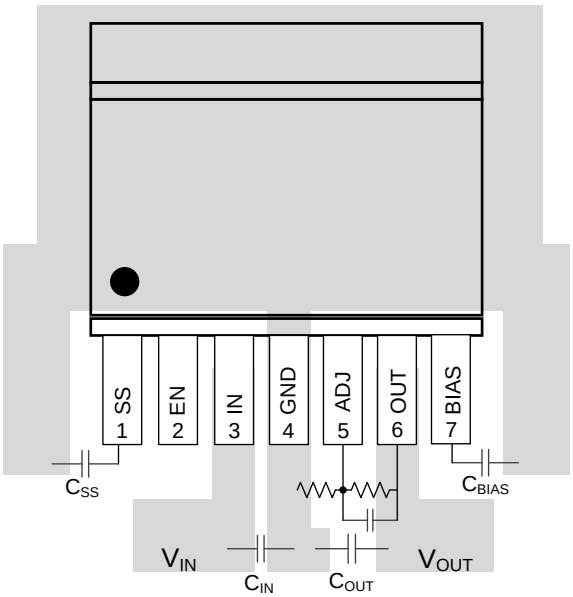

Figure 31. LP38852 DDPAK/TO-263 and TO-220 Layout Example

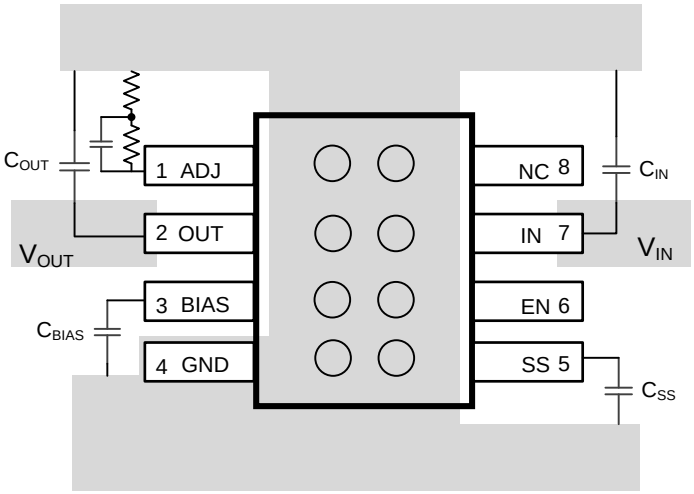

Figure 32. LP38852 SO PowerPAD Layout Example

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For additional information, see the following:

TI Application Note AN-1378 *Method for Calculating Output Voltage Tolerances in Adjustable Regulators* (SNVA112)

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

SO PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38852MR-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L38852 MRADJ	Samples
LP38852MRX-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L38852 MRADJ	Samples
LP38852S-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTW	7	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP38852S -ADJ	Samples
LP38852SX-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTW	7	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP38852S -ADJ	Samples
LP38852T-ADJ/NOPB	ACTIVE	TO-220	NDZ	7	45	RoHS & Green	SN	Level-1-NA-UNLIM	-40 to 125	LP38852T -ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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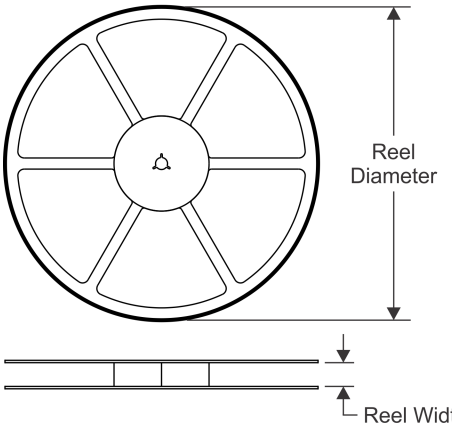
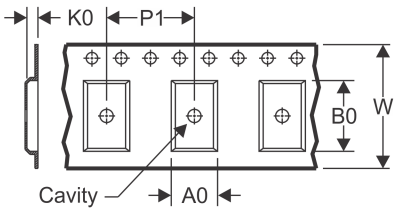
TAPE AND REEL INFORMATION

REEL DIMENSIONS

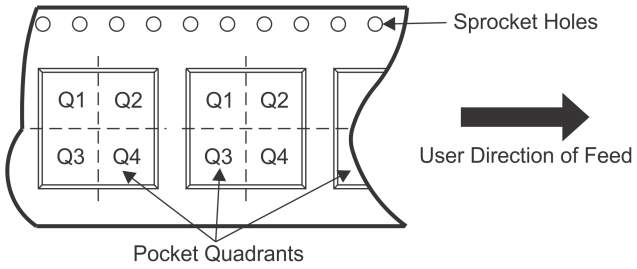


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

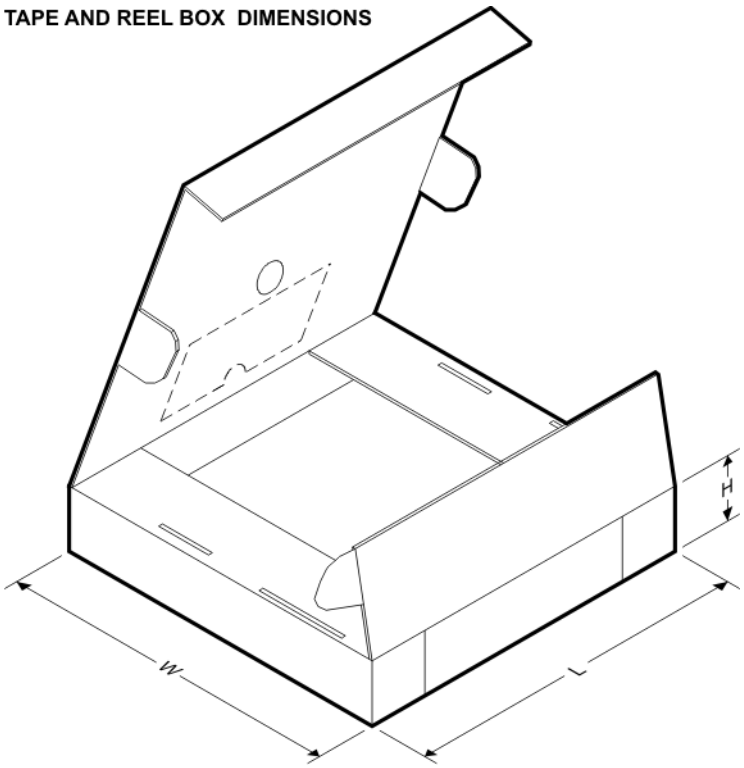
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38852MRX-ADJ/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP38852SX-ADJ/NOPB	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

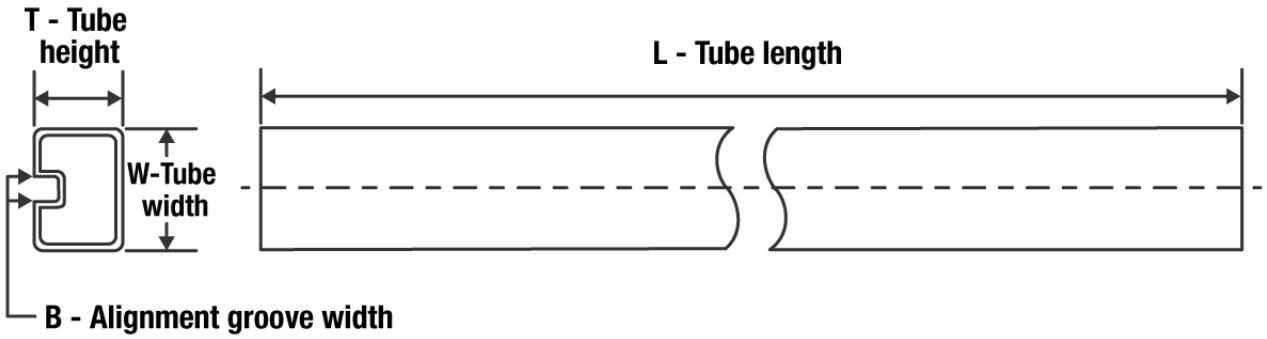
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38852MRX-ADJ/NOPB	SO PowerPAD	DDA	8	2500	853.0	449.0	35.0
LP38852SX-ADJ/NOPB	DDPAK/TO-263	KTW	7	500	367.0	367.0	45.0

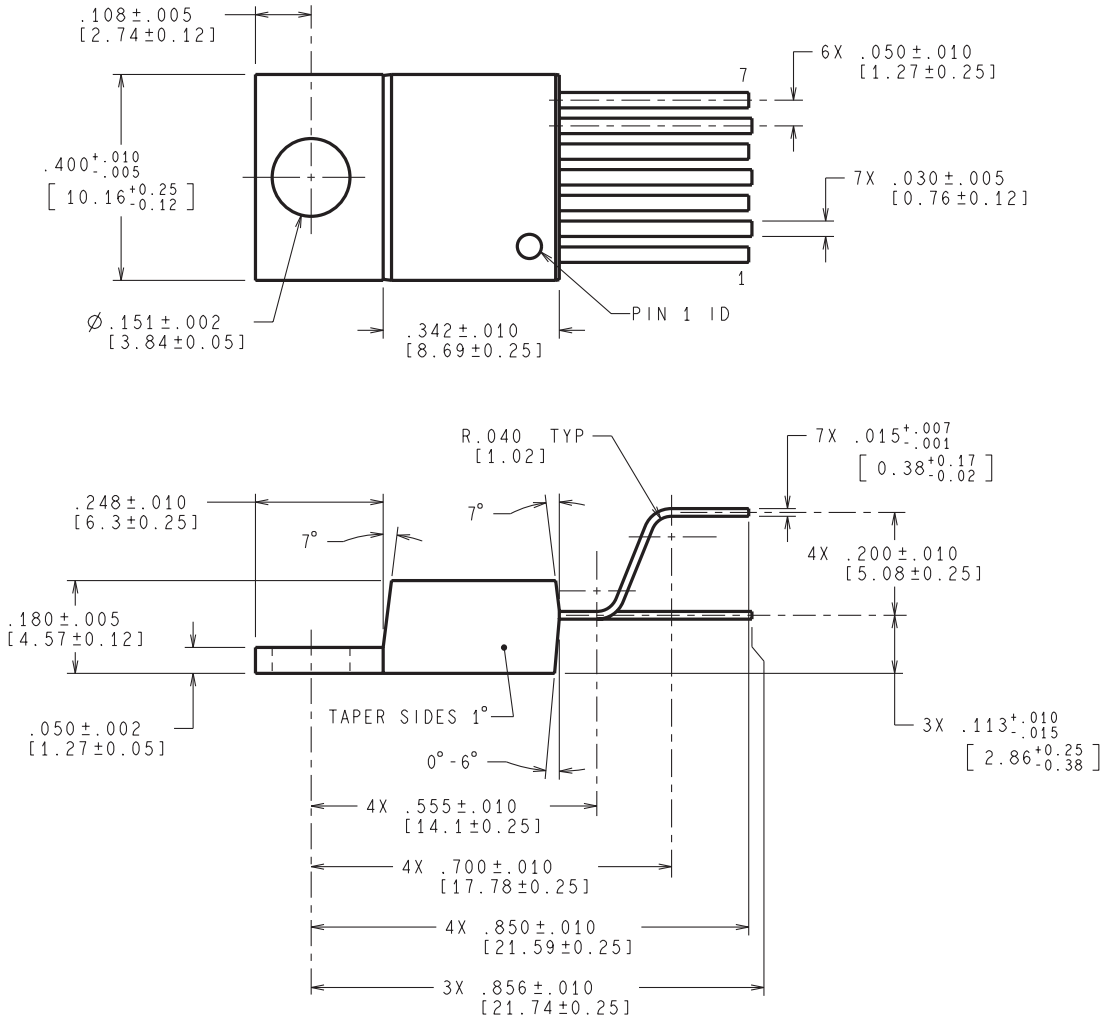
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP38852MR-ADJ/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LP38852MR-ADJ/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LP38852S-ADJ/NOPB	KTW	TO-263	7	45	502	25	8204.2	9.19
LP38852T-ADJ/NOPB	NDZ	TO-220	7	45	502	30	30048.2	10.74

NDZ0007B



CONTROLING DIMENSIONS IS INCH
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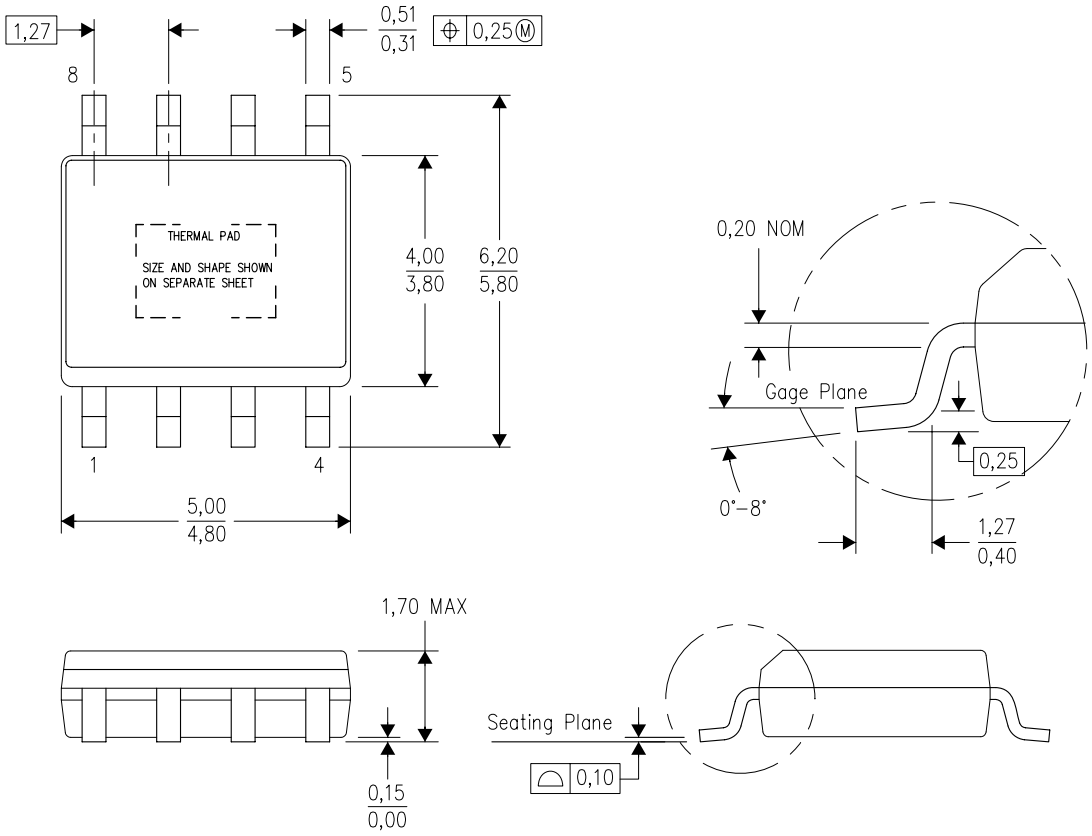
TA07B (Rev E)

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

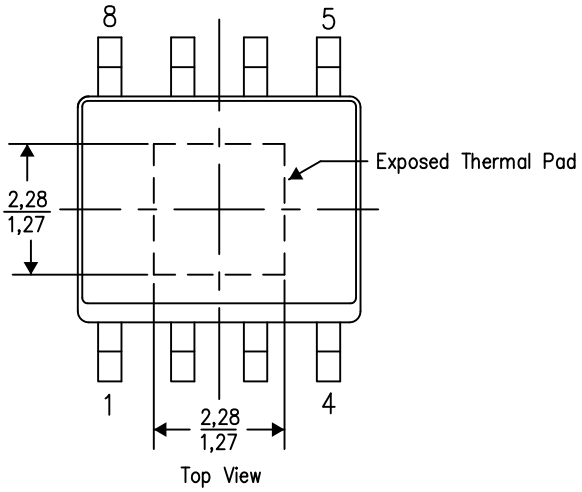
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



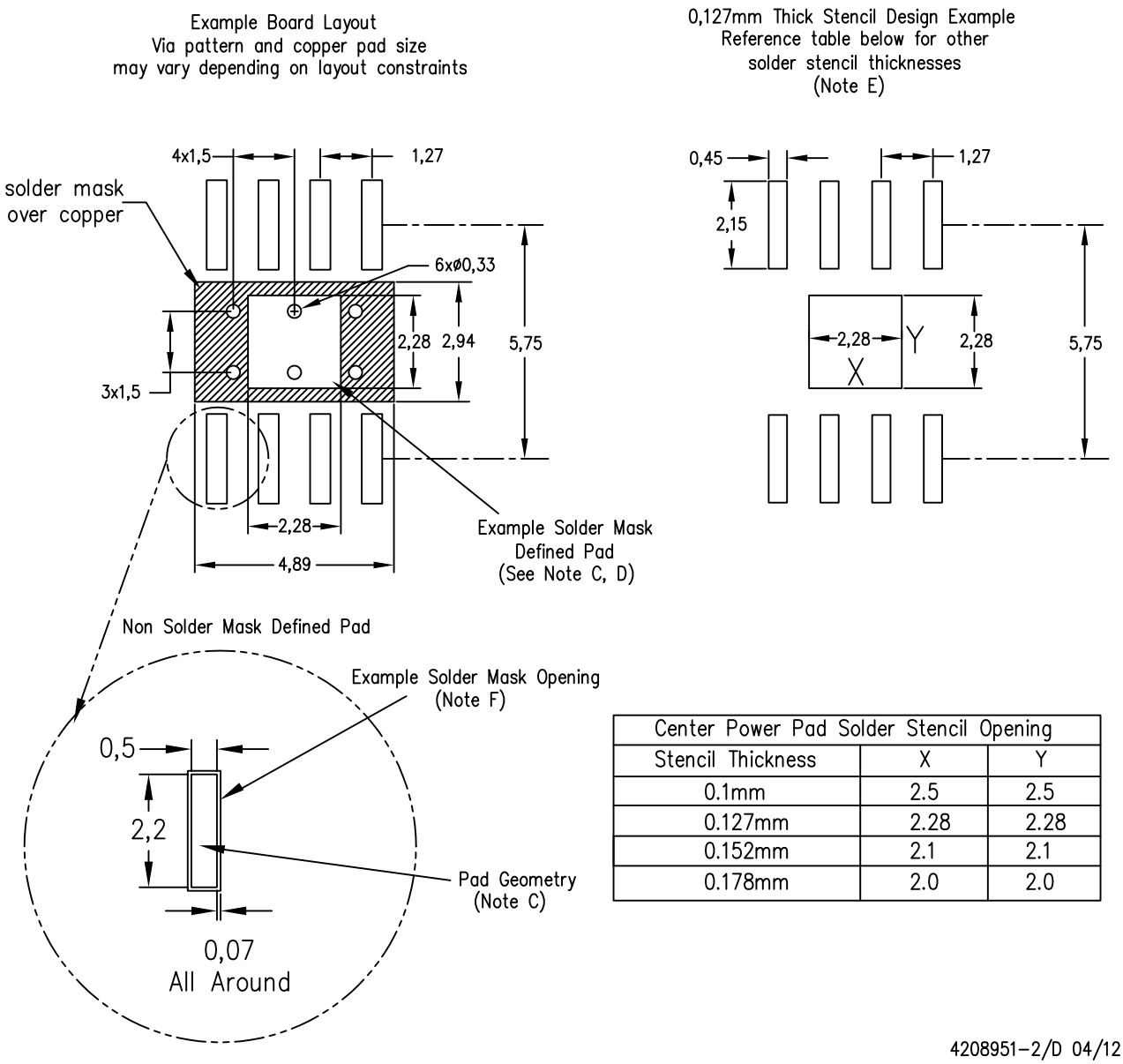
Exposed Thermal Pad Dimensions

4206322–2/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.5
0.127mm	2.28	2.28
0.152mm	2.1	2.1
0.178mm	2.0	2.0

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

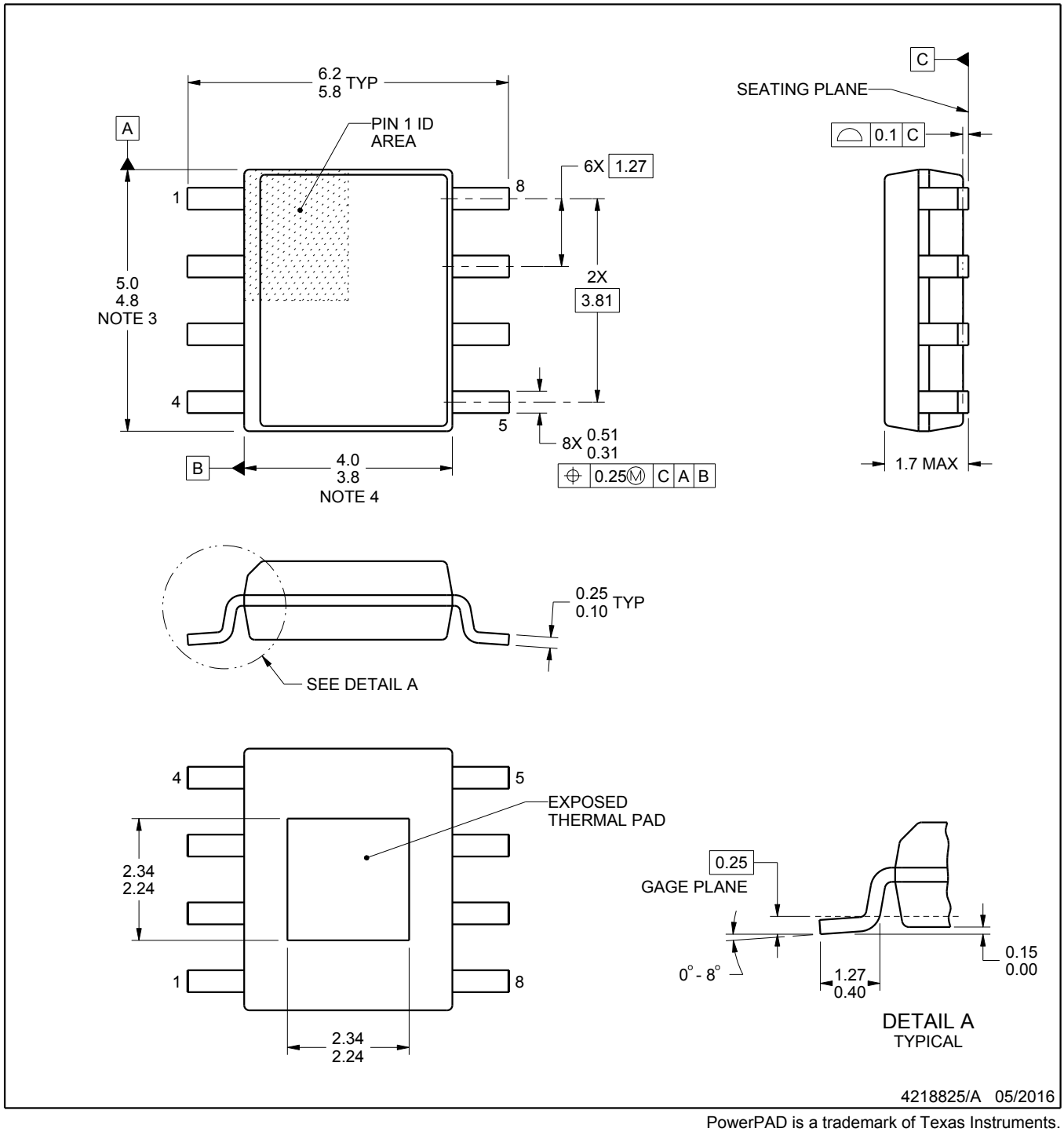
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DDA0008A

PowerPAD™ SOIC - 1.7 mm max height

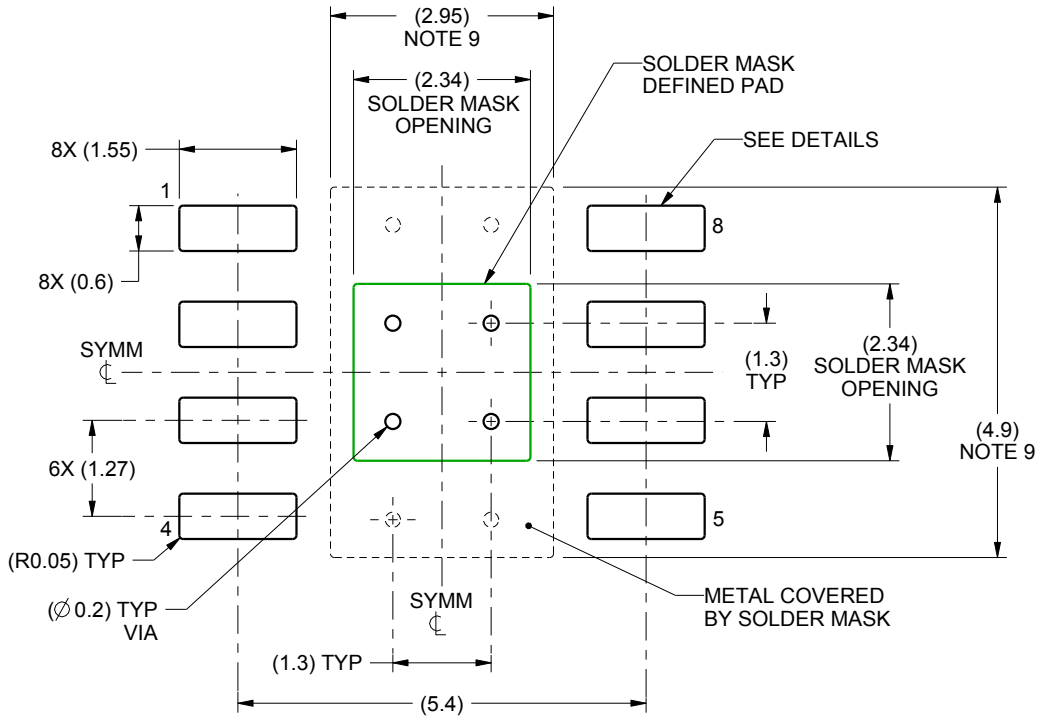
PLASTIC SMALL OUTLINE



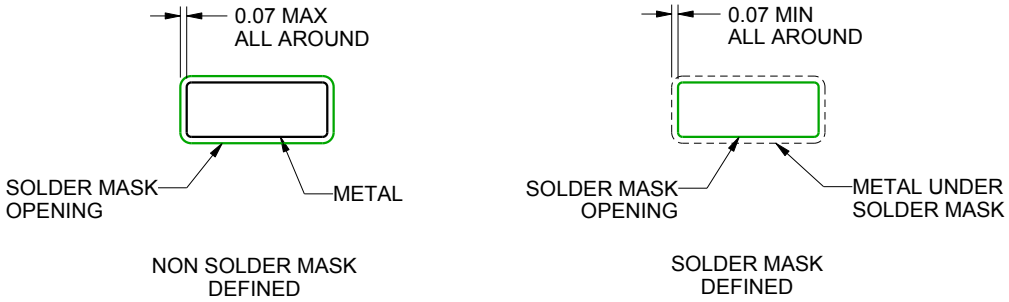
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X

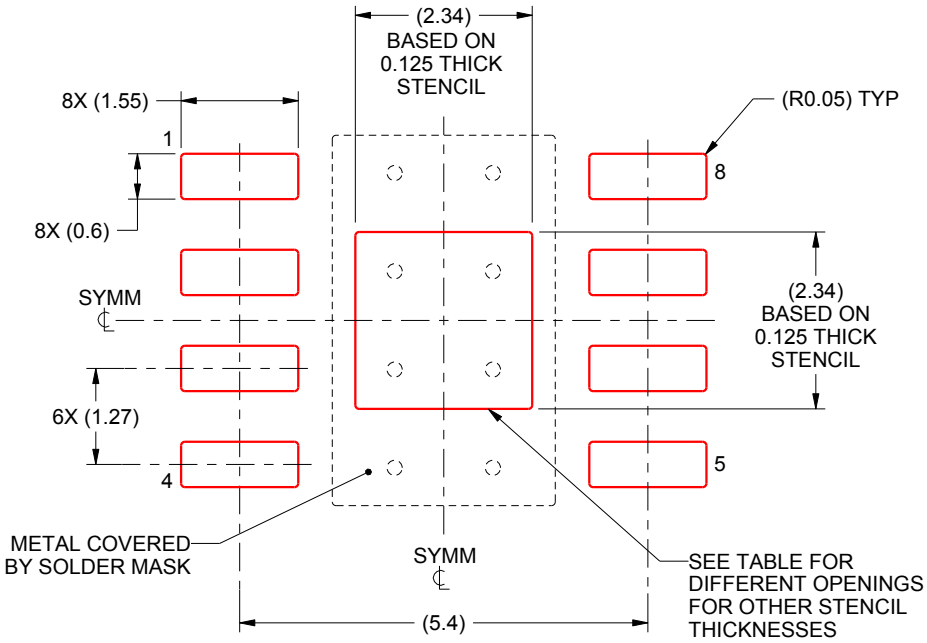


SOLDER MASK DETAILS

4218825/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

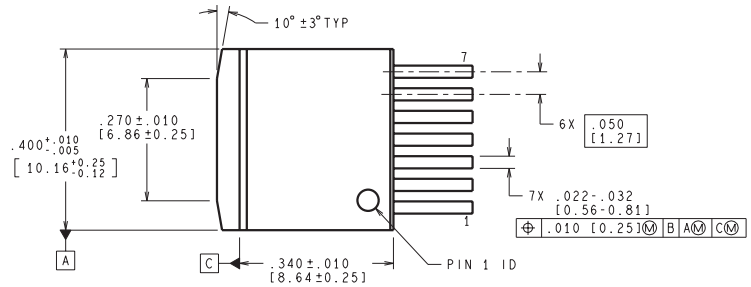
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 2.62
0.125	2.34 X 2.34 (SHOWN)
0.150	2.14 X 2.14
0.175	1.98 X 1.98

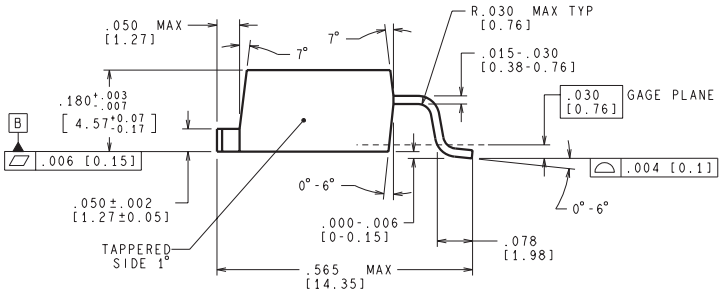
4218825/A 05/2016

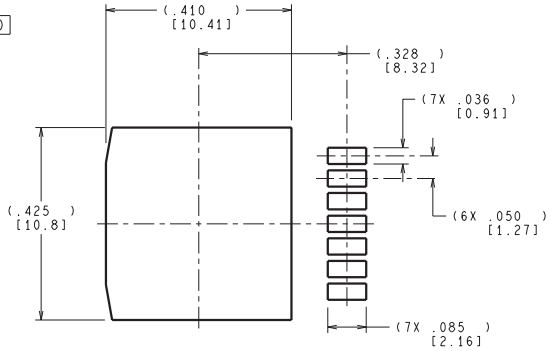
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

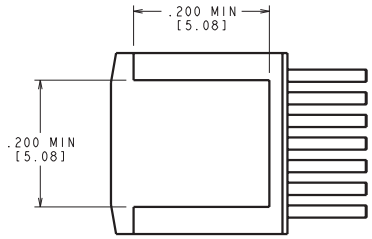
KTW0007B







LAND PATTERN RECOMMENDATION



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TS7B (Rev E)

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