TEXAS INSTRUMENTS

TPS61000, TPS61001, TPS61002, TPS61003
TPS61004, TPS61005, TPS61006, TPS61007

SLVS279D – MARCH 2000 – REVISED AUGUST 2015

TPS6100x Single- and Dual-Cell Boost Converter With Start-up Into Full Load

1 Features

- Start-Up Into a Full Load With Supply Voltages as Low as 0.9 V Over Full Temperature Range
- Minimum 100-mA Output Current From 0.8-V Supply Voltage, 250 mA From 1.8 V
- High Power Conversion Efficiency, up to 90%
- Power-Save Mode for Improved Efficiency at Low Output Currents
- Device Quiescent Current Less Than 50 µA
- Added System Security With Integrated Low-Battery Comparator
- Low-EMI Converter (Integrated Antiringing Switch Across Inductor)
- Micro-Size 10-Pin MSOP Package
- Evaluation Modules Available (TPS6100xEVM–156)

2 Applications

- Single- and Dual-Cell Battery Operated Products
- MP3-Players and Wireless Headsets
- Pagers and Cordless Phones
- Portable Medical Diagnostic Equipment
- Remote Controls

3 Description

The TPS6100x devices are boost converters intended for systems that are typically operated from a single- or dual-cell nickel-cadmium (NiCd), nickel-metal hydride (NiMH), or alkaline battery. The converter output voltage can be adjusted from 1.5 V to a maximum of 3.3 V and provides a minimum output current of 100 mA from a single battery cell and 250 mA from two battery cells. The converter starts up into a full load with a supply voltage of 0.9 V and stays in operation with supply voltages as low as 0.8 V.

The converter is based on a fixed-frequency, current-mode pulse-width-modulation (PWM) controller that goes into power-save mode at low load currents. The current through the switch is limited to a maximum of 1100 mA, depending on the output voltage. The current sense is integrated to further minimize external component count. The converter can be disabled to minimize battery drain when the system is put into standby.

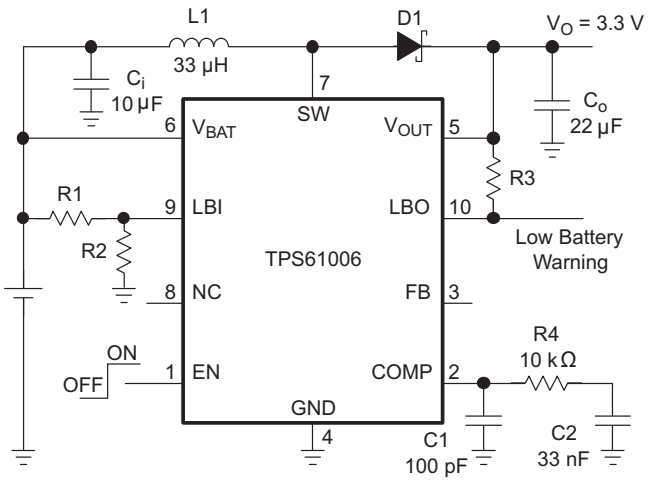
A low-EMI mode is implemented to reduce interference and radiated electromagnetic energy that is caused by the ringing of the inductor when the inductor discharge-current decreases to zero. The device is packaged in the space-saving 10-pin MSOP package.

Device Information(1)

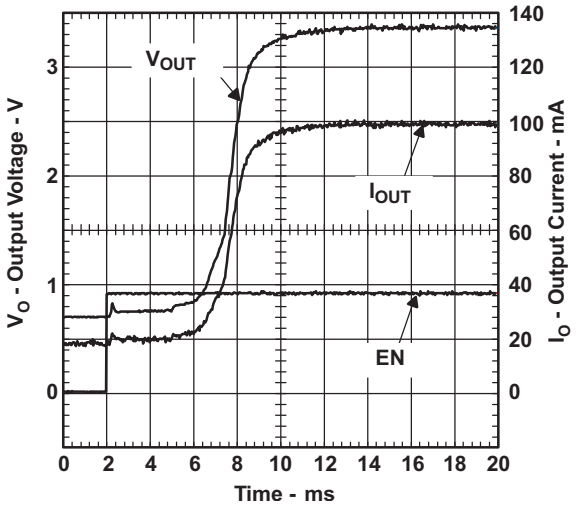
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6100x	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit for Fixed Output Voltage Options



TPS61006 Start-Up Timing Into 33-Ω Load



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2003) to Revision D **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Replaced the *Dissipation Ratings* table with the *Thermal Information* table ... 4

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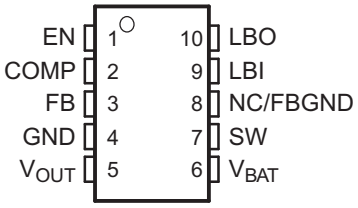
5 Available Options

T_A	PACKAGE	OUTPUT VOLTAGE (V)	PART NUMBER(1)	MARKING DGS PACKAGE
–40°C to 85°C	10-Pin MSOP DGS	Adj. from 1.5 V to 3.3 V	TPS61000DGS	ADA
		1.5	TPS61001DGS	ADB
		1.8	TPS61002DGS	ADC
		2.5	TPS61003DGS	ADD
		2.8	TPS61004DGS	ADE
		3.0	TPS61005DGS	ADF
		3.3	TPS61006DGS	ADG
		Adj. from 1.5 V to 3.3 V	TPS61007DGS	AD

(1) The DGS package is available taped and reeled. Add R suffix to device type (e.g. TPS61000DGSR) to order quantities of 2500 devices per reel.

6 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



TPS61007 only

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	2	—	Compensation of error amplifier. Connect R-C-C network to set frequency response of control loop. See the Application section for more details.
EN	1	I	Chip-enable input. The converter is switched on if EN is set high, and is switched off when EN is connected to ground (shutdown mode).
FB	3	I	Feedback input for adjustable output voltage (TPS61000 only). The output voltage is programmed depending on the values of resistors R1 and R2. For the fixed output voltage versions (TPS61000, TPS61002, TPS61003, TPS61004, TPS61005, TPS61006), leave the FB pin unconnected.
NC/FBGND	8	—	Not connected (TPS61000, TPS61002, TPS61003, TPS61004, TPS61005, TPS61006). A ground pin for the feedback resistor divider for the TPS61007 only.
GND	4	—	Ground
LBI	9	I	Low-battery detector input. A low-battery signal is generated at the LBO pin when the voltage on LBI drops below the threshold of 500 mV. Connect LBI to GND or V_{BAT} if the low-battery detector function is not used. Do not leave this pin floating.
LBO	10	O	Open-drain low-battery detector output. This pin is pulled low if the voltage on LBI drops below the threshold of 500 mV. A pullup resistor should be connected between LBO and V_{OUT}.
SW	7	I	Switch input pin. The node between inductor and anode of the rectifier diode is connected to this pin.
V_{BAT}	6	I	Supply pin
V_{OUT}	5	O	Output voltage. For the fixed output voltage versions, the integrated resistive divider is connected to this pin.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage (V_{BAT}, V_{OUT}, COMP, FB, LBO, EN, LBI)	–0.3	3.6	V
	Input voltage (SW)	–0.3	V_{OUT} + 0.7	V
	Peak current into SW		1300	mA
	Continuous total power dissipation	See *Thermal Information*		
T_A	Operating free-air temperature	–40	85	°C
T_J	Maximum junction temperature		150	°C
	Lead temperature		260	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{BAT}	Supply voltage		0.8		V_O	V
V_O	Output current	V_{BAT} = 0.8 V		100		mA
		V_{BAT} = 0.8 V		250		
	Inductor		10		33	µH
	Input capacitor			10		µF
	Output capacitor			22		µF
T_J	Operating junction temperature		–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6100x DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	80.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	79.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

over recommended operating free-air temperature range, V_{BAT} = 1.2 V, EN = V_{BAT} (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage for start up		R_L = 33 Ω		0.9			V
			R_L = 3 kΩ,	T_A = 25°C	0.8			
	Input voltage once started		I_O = 100 mA		0.8			
V_O	Programmable output voltage	TPS61000, TPS61007	I_O = 100 mA		1.5		3.3	V
V_O	Output voltage	TPS61001	1.2 V,	I_O = 1 mA	1.44	1.5	1.55	V
			0.8 V < V_I < V_O,	I_O = 100 mA	1.45	1.5	1.55	
		TPS61002	1.2 V,	I_O = 1 mA	1,72	1.8	1.86	V
			0.8 V < V_I < V_O,	I_O = 100 mA	1.74	1.8	1.86	
		TPS61003	1.2 V,	I_O = 1 mA	2.40	2.5	2.58	V
			0.8 V < V_I < V_O,	I_O = 100 mA	2.42	2.5	2.58	
			1.6 V < V_I < V_O,	I_O = 200 mA	2.42	2.5	2.58	
		TPS61004	1.2 V,	I_O = 1 mA	2.68	2.8	2.89	V
			0.8 V < V_I < V_O,	I_O = 100 mA	2.72	2.8	2.89	
			1.6 V < V_I < V_O,	I_O = 200 mA	2.72	2.8	2.89	
		TPS61005	1.2 V,	I_O = 1 mA	2.88	3.0	3.1	V
			0.8 V < V_I < V_O,	I_O = 100 mA	2.9	3.0	3.1	
			1.6 V < V_I < V_O,	I_O = 200 mA	2.9	3.0	3.1	
		TPS61006	1.2 V,	I_O = 1 mA	3.16	3.3	3.4	V
			0.8 V < V_I < V_O,	I_O = 100 mA	3.2	3.3	3.4	
			1.6 V < V_I < V_O,	I_O = 200 mA	3.2	3.3	3.4	
I_O	Maximum continuous output current		V_I = 0.8 V		100			mA
			V_I = 1.8 V		250			
I_{ILIM}	Switch current limit	TPS61001	0.8 V < V_I < V_O			0.5		A
		TPS61002				0.65		
		TPS61003				0.9		
		TPS61004				0.95		
		TPS61005				1		
		TPS61006				1.1		
V_{FB}	Feedback voltage	TPS61000, TPS61007			468	500	515	mV
f	Oscillator frequency				360	500	840	kHz
D_{MAX}	Maximum duty cycle					85%		
$r_{DS(on)}$	Switch-on resistance		V_O = 3.3 V			0.18	0.27	Ω
	Line regulation (1)		V_I = 0.8 V to 1.25 V,	I_O = 50 mA		0.3		%/V
	Load regulation fixed output voltage versions (1)		V_I = 1.2 V,	I_O = 10 mA to 90 mA		0.25%		
I_Q	Quiescent current drawn from power source ower (current into V_{BAT} and into V_{OUT})		I_O = 0 mA, V_{EN} = V_I, V_O = 3.4 V	V_{BAT}			44	µA
				V_{OUT}			6	
I_{SD}	Shutdown current from power source (current into V_{BAT} and into V_{OUT})		V_{EN} = 0 V			0.2	5	µA
V_{IL}	EN low-level input voltage						0.2x V_{BAT}	V
V_{IH}	EN high-level input voltage				0.8 × V_{BAT}			V

(1) Line and load regulation is measured as a percentage deviation from the nominal value (i.e., as percentage deviation from the nominal output voltage). For line regulation, x %/V stands for ±x% change of the nominal output voltage per 1-V change on the input/supply voltage. For load regulation, y% stands for ±y% change of the nominal output voltage per the specified current change.

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Electrical Characteristics (continued)

over recommended operating free-air temperature range, V_{BAT} = 1.2 V, EN = V_{BAT} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	EN input current	EN = GND or V_{BAT}		0.1	1	µA
V_{IL}	LBI low-level input voltage threshold	V_{LBI} voltage decreasing	470	500	530	mV
	LBI input hysteresis			10		
I_I	LBI input current			0.01	0.1	µA
V_{OL}	LBO low-level output voltage	V_{LBI} = 0 V, V_O = 3.3 V, I_{OL} = 50 µA		0.04	0.2	V
	LBO output leakage current	V_{LBI} = 650 mV, V_{LBO} = 3.3 V		0.01	1	µA
I_{FB}	FB input bias current (TPS61000, TPS61007 only)	V_{FB} = 500 mV		0.01	0.1	µA

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7.6 Typical Characteristics

Table 1. Table of Graphs

TITLE			
η	Efficiency	vs Output Current	Figure 1, Figure 2
		vs Inductor Type	Figure 3
		vs Input Voltage	Figure 4
I_O	Maximum Output Current	vs Input Voltage	Figure 5
V_O	Output Voltage	vs Output Current	Figure 6
V_O	TPS61007 Output Voltage	vs Output Current	Figure 7
I_Q	No-Load Supply Current	vs Input Voltage	Figure 8
I_{SD}	Shutdown Current	vs Input Voltage	Figure 9
V_I	Minimum Start-Up Input Voltage	vs Load Current	Figure 10
I_{LIM}	Switch Current Limit	vs Output Voltage	Figure 11

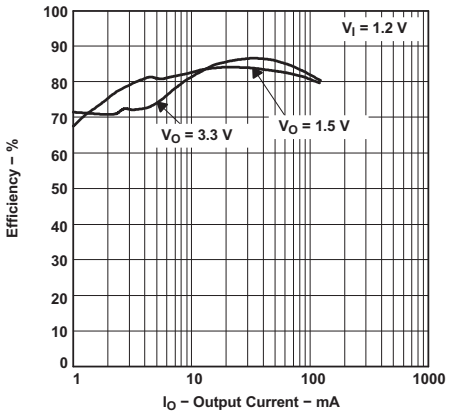


Figure 1. Efficiency vs Output Currency

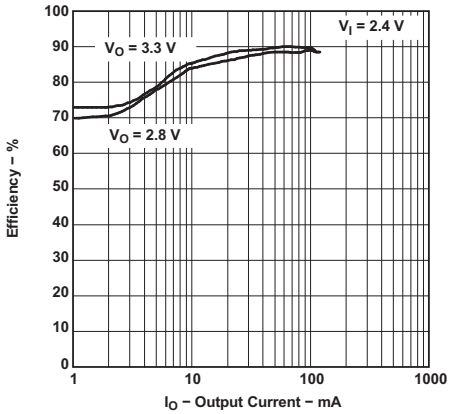


Figure 2. Efficiency vs Output Currency

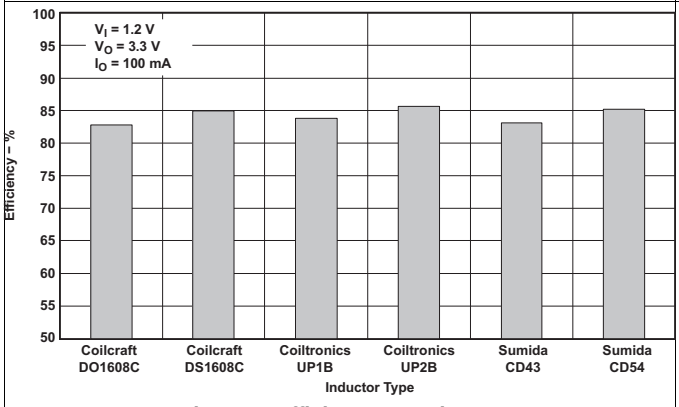


Figure 3. Efficiency vs Inductor Type

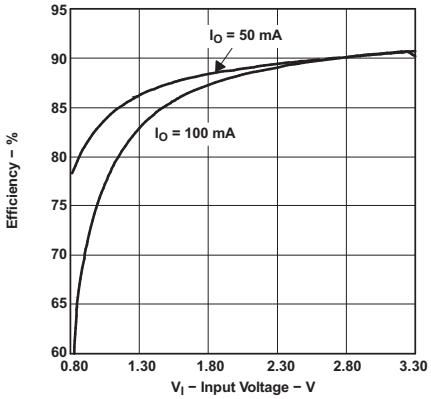


Figure 4. Efficiency vs Input Voltage

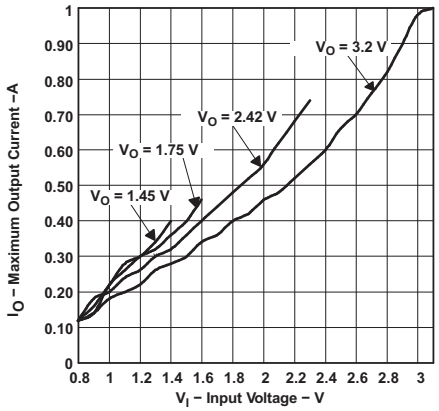


Figure 5. Maximum Output Current vs Input Voltage

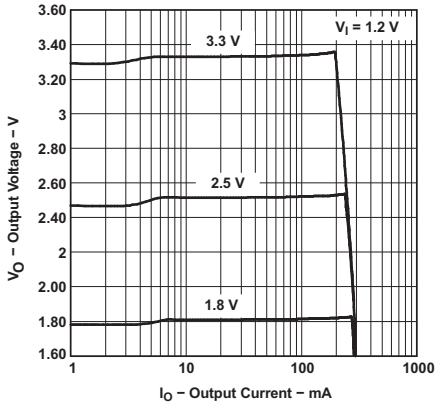


Figure 6. TPS61002/3/6 Output Voltage vs Output Current

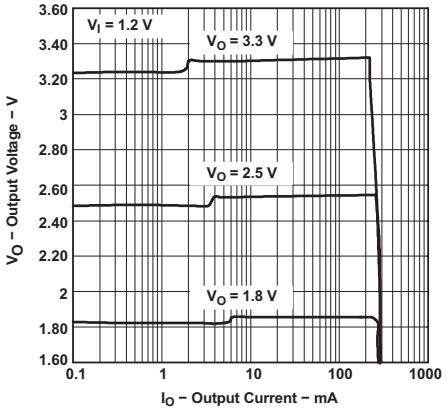


Figure 7. TPS61007 Output Voltage vs Output Current

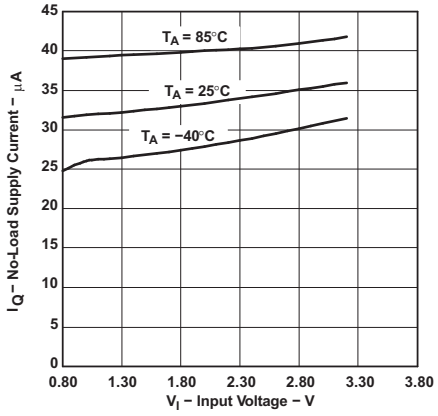


Figure 8. No-Load Supply Current vs Input Voltage

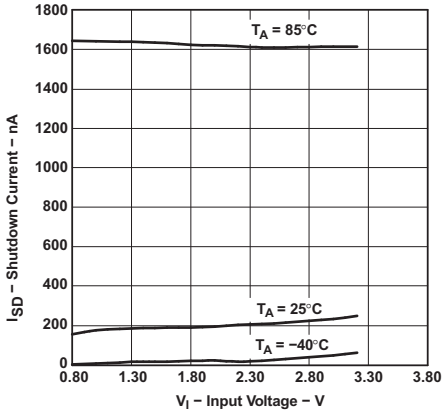


Figure 9. Shutdown Current vs Input Voltage

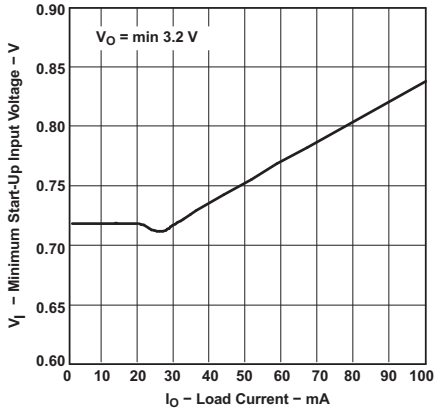


Figure 10. Minimum Start-up Input Voltage vs Load Current

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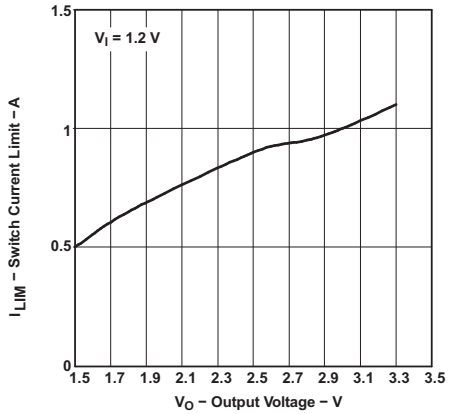
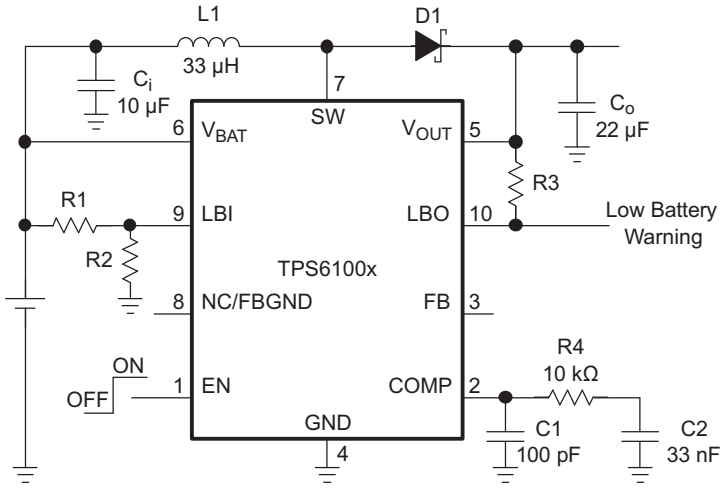


Figure 11. TPS61000, TPS61007 Switch Current Limit vs Output Voltage

8 Parameter Measurement Information



List of Components:
IC1: Only fixed output versions (unless otherwise noted)
L1: Coilcraft DO3308P−333
D1: Motorola Schottky Diode MBRM120LT3
C_I: Ceramic
C_O: Ceramic

Figure 12. Circuit Used for Typical Characteristics Measurements

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9 Detailed Description

9.1 Overview

The TPS6100x Non-synchronous step-up converter typically operates at a 500-kHz frequency pulse width modulation (PWM) at moderate to heavy load currents. The converter enters Power Save mode at low load currents to maintain a high efficiency over a wide load. Additionally, the device integrates a circuit which removes the ringing that typically appears on the SW-node when the converter enters the discontinuous current mode.

9.2 Functional Block Diagrams

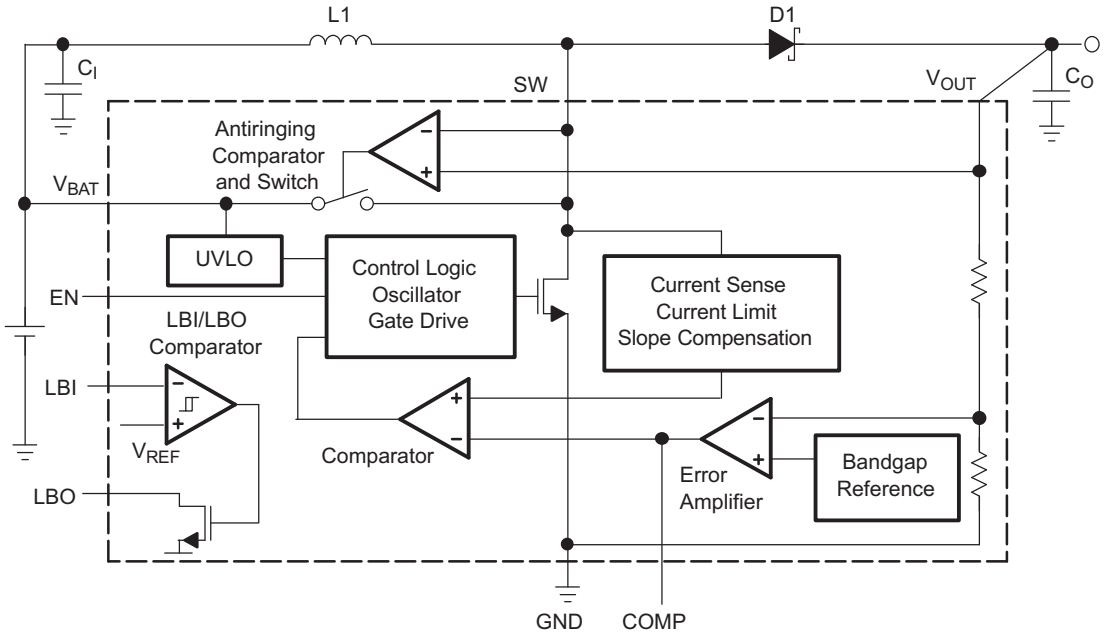


Figure 13. Fixed Output-Voltage Option

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Functional Block Diagrams (continued)

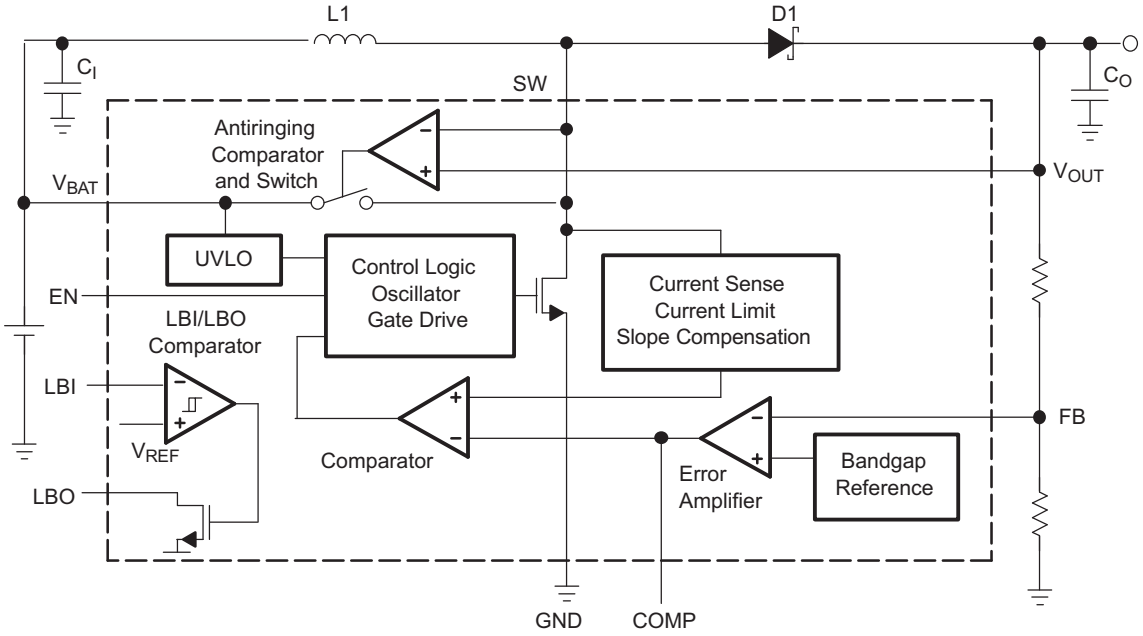


Figure 14. Adjustable Output-Voltage Option (TPS61000 Only)

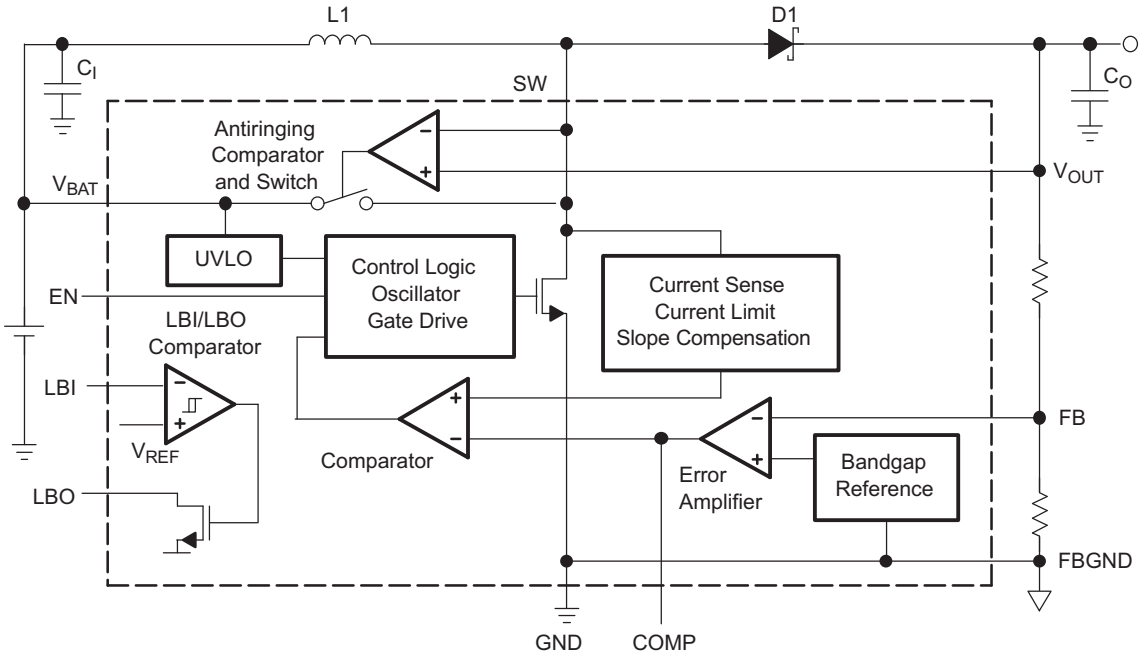


Figure 15. Adjustable Output-Voltage Option (TPS61007 Only)

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9.3 Feature Description

9.3.1 Controller Circuit

The device is based on a current-mode control topology using a constant-frequency pulse-width modulator to regulate the output voltage. It runs at an oscillator frequency of 500 kHz. The current sense is implemented by measuring the voltage across the switch. The controller also limits the current through the power switch on a pulse-by-pulse basis. Care must be taken that the inductor saturation current is higher than the current limit of the TPS6100x. This prevents the inductor from going into saturation and therefore protects both device and inductor. The current limit should not become active during normal operating conditions.

The TPS6100x is designed for high efficiency over a wide output current range. Even at light loads the efficiency stays high because the controller enters a power-save mode, minimizing switching losses of the converter. In this mode, the controller only switches if the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses, and again goes into the power-save mode once the output voltage exceeds the threshold voltage. The controller enters the power-save mode when the output current drops to levels that force the discontinuous current mode. It calculates a minimum duty cycle based on input and output voltage and uses the calculation for the transition out of the power-save mode into continuous current mode.

The control loop must be externally compensated with an R/C/C network connected to the COMP pin. See the application section for more details on the design of the compensation network.

9.3.2 Device Enable

The device is put into operation when EN is set high. During start-up of the converter the input current from the battery is limited until the voltage on COMP reaches its operating point. The device is put into a shutdown mode when EN is set to GND. In this mode, the regulator stops switching and all internal control circuitry including the low-battery comparator is switched off. The output voltage drops to one diode drop below the input voltage in shutdown.

9.3.3 Undervoltage Lockout

An undervoltage lockout function prevents the device start-up if the supply voltage on V_{BAT} is lower than approximately 0.7 V. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on V_{BAT} drops below approximately 0.7 V.

If the EN pin is hardwired to V_{BAT} and if the voltage at V_{BAT} drops temporarily below the UVLO threshold voltage, the device switches off and does not start up again automatically, even if the supply voltage rises above 0.9 V. The device starts up again only after a signal change from low to high on EN or if the battery voltage is completely removed.

9.3.4 Low-Battery Detector Circuit (LBI and LBO)

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO pin is high impedance. The LBO pin goes active low when the voltage on the LBI pin decreases below the set threshold voltage of 500 mV ±15 mV, which is equal to the internal reference voltage. The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 10 mV. See the application section for more details about the programming of the LBI threshold.

If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to V_{BAT}) and the LBO pin can be left unconnected. Do not let the LBI pin float.

9.3.5 Low-EMI Switch

The device integrates a circuit which removes the ringing that typically appears on the SW-node when the converter enters the discontinuous current mode. In this case, the current through the inductor ramps to zero and the Schottky diode stops conducting. Due to remaining energy that is stored in parasitic components of the diode, inductor, and switch, a ringing on the SW pin is induced. The integrated antiringing switch clamps this voltage internally to V_{BAT} and therefore dampens this ringing.

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Feature Description (continued)

The antiringing switch is turned on by a comparator that monitors the voltage between SW and V_{OUT}. This voltage indicates when the diode is reverse biased. The ringing on the SW-node is damped to a large degree, reducing the electromagnetic interference generated by the switching regulator to a great extent.

9.3.6 Adjustable Output Voltage (TPS61000 and TPS61007 Only)

The accuracy of the internal voltage reference, the controller topology, and the accuracy of the external resistor divider determine the accuracy of the adjustable output voltage versions. The reference voltage has an accuracy of ±4% over line, load, and temperature. The controller switches between fixed frequency and pulse-skip mode, depending on load current. This adds an offset to the output voltage that is equivalent to 1% of V_O. Using 1% accurate resistors for the feedback divider, a total accuracy of ±6% can be achieved over the complete temperature and output current range. The TPS61007 is an improved adjustable output voltage version. Ground shift in the feedback loop was eliminated by adding a separate ground pin for the feedback resistor divider (FBGND).

9.4 Device Functional Modes

9.4.1 Power Save Mode

The TPS6100x enters a power-save mode, minimizing switching losses of the converter. In this mode, the controller only switches if the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses, and again goes into the power-save mode once the output voltage exceeds the threshold voltage.

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS6100x boost converter family is intended for systems that are powered by a single-cell NiCd or NiMH battery with a typical terminal voltage between 0.9 V to 1.6 V. It can also be used in systems that are powered by two-cell NiCd or NiMH batteries with a typical stack voltage between 1.8 V and 3.2 V. Additionally, singleor dual-cell, primary and secondary alkaline battery cells can be the power source in systems where the TPS6100x is used.

10.1.1 Schematic of TPS6100x Evaluation Modules (TPS6100XEVM156)

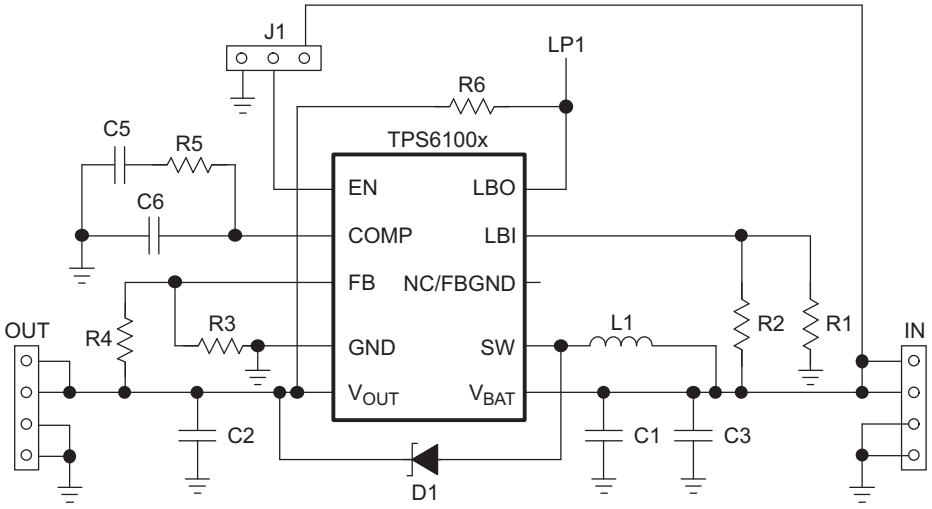


Figure 16. Schematic of TPS6100x Evaluation Modules

Evaluation modules are available for device types TPS61000, TPS61002, TPS61003, and TPS61006.

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10.2 Typical Application

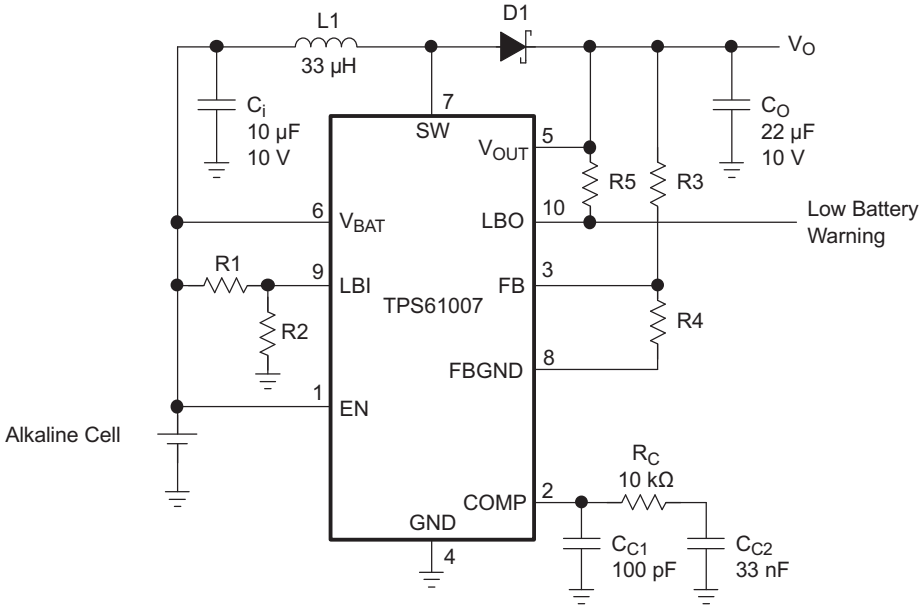


Figure 17. Typical Application Circuit for Adjustable Output Voltage Option

10.2.1 Design Requirements

See Table 2 for design parameters.

Table 2. TPS6100x Output Design Parameters

DESIGN PARAMETERS	VALUES
Input voltage range	1.8 V to 3.3 V
Output voltage	3.3 V
Output voltage ripple	±3% VOUT

10.2.2 Detailed Design Procedure

10.2.2.1 Programming the TPS61000 and TPS61007 Adjustable Output Voltage Devices

The output voltage of the TPS61000 and TPS61007 can be adjusted with an external resistor divider. The typical value of the voltage on the FB pin is 500 mV in fixed-frequency operation and 485 mV in the power-save operation mode. The maximum allowed value for the output voltage is 3.3 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA, and the voltage across R4 is typically 500 mV. Based on those two values, the recommended value for R4 is in the range of 500 kΩ in order to set the divider current at 1 µA. From that, the value of resistor R3, depending on the needed output voltage V_{OUT}, can be calculated using the following equation:

$$R3 = R4 \times \left(\frac{V_O}{V_{FB}} - 1 \right) = 500\ k\Omega \times \left(\frac{V_O}{500\ mV} - 1 \right) \quad (1)$$

If, as an example, an output voltage of 2.5 V is needed, a 2-MΩ resistor should be chosen for R3.

The TPS61007 is an improved version of the TPS61000 adjustable output voltage device. The FBGND pin is internally connected to GND.

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10.2.2.2 Programming the Low Battery Comparator Threshold Voltage

The current through the resistive divider should be about 100 times greater than the current into the LBI pin. The typical current into the LBI pin is 0.01 µA. The voltage across R2 is equal to the reference voltage that is generated on-chip, which has a value of 500 mV ±15 mV. The recommended value for R2 is therefore in the range of 500 kΩ. From that, the value of resistor R1, depending on the desired minimum battery voltage ($V_{BAT)}$, can be calculated using the following equation:

$$R1 = R2 \times \left(\frac{V_{TRIP}}{V_{REF}} - 1 \right) = 500\ k\Omega \times \left(\frac{V_{BAT}}{0.5\ V} - 1 \right) \quad (2)$$

For example, if the low-battery detection circuit should flag an error condition on the LBO output pin at a battery voltage of 1 V, a resistor in the range of 500 kΩ should be chosen for R1.

The output of the low battery comparator is a simple open-drain output that goes active low if the battery voltage drops below the programmed threshold voltage on LBI. The output requires a pullup resistor with a recommended value of 1MΩ, and should only be pulled up to the V_{OUT}. If not used, the LBO pin can be left floating.

10.2.2.3 Inductor Selection

The output filter of inductive switching regulators is a low pass filter of second order. It consists of an inductor and a capacitor, often referred to as storage inductor and output capacitor.

To select an inductor, keep the possible peak inductor current below the current limit threshold of the power switch in your chosen configuration. For example, the current limit threshold of the TPS61006's switch is 1100 mA at an output voltage of 3.3 V. The highest peak current through the inductor and the switch depends on the output load, the input (V_{BAT}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using the following equation:

$$I_L = I_{OUT} \times \frac{V_{OUT}}{V_{BAT} \times 0.8} \quad (3)$$

For example, for an output current of 100 mA at 3.3 V, at least 515-mA current flows through the inductor at a minimum input voltage of 0.8 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor as well as output voltage ripple and EMI. But in the same way, the regulation time at load change rises. In addition, a larger inductor increases the total system cost.

With those parameters it is possible to calculate the value for the inductor:

$$L = \frac{V_{BAT} \times (V_{OUT} - V_{BAT})}{\Delta I_L \times f \times V_{OUT}} \quad (4)$$

where

- f is the switching frequency
- ΔI_L is the ripple current in the inductor, that is 20% x I_L

In this example, the desired inductor has the value of 12 µH. With this calculated value and the calculated currents, it is possible to chose a suitable inductor. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in equation 3. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

The following inductors from different suppliers were tested. All work with the TPS6100x converter within their specified parameters:

Table 3. Recommended Inductors

VENDOR	PART NUMBER
Coilcraft	DO1608P Series
	DS1608P Series
	DO3308 Series

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Table 3. Recommended Inductors (continued)

VENDOR	PART NUMBER
Coiltronics	UP1B Series
	UP2B Series
Murata	LQH3N Series
Sumida	CD43 Series
	CD54 Series
	CDR74B Series
TDK	NLC453232T Series

10.2.2.4 Capacitor Selection

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero.

$$C_{min} = \frac{I_{OUT} \times (V_{OUT} - V_{BAT})}{f \times \Delta V \times V_{OUT}}$$

where

- f is the switching frequency
- ΔV is the maximum allowed ripple. (5)

With a chosen ripple voltage of 15 mV, a minimum capacitance of 10 µF is needed. The total ripple will be larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using the following equation:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (6)$$

An additional ripple of 30 mV is the result of using a tantalum capacitor with a low ESR of 300 mΩ. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 45 mV. It is possible to improve the design by enlarging the capacitor or using smaller capacitors in parallel to reduce the ESR or by using better capacitors with lower ESR, like ceramics. For example, a 10-µF ceramic capacitor with an ESR of 50 mΩ is used on the evaluation module (EVM). Tradeoffs have to be made between performance and costs of the converter circuit.

A 10-µF input capacitor is recommended to improve transient behavior of the regulator. A ceramic capacitor or a tantalum capacitor with a 100-nF ceramic capacitor in parallel placed close to the IC is recommended.

10.2.2.5 Rectifier Selection

The rectifier diode has a major impact on the overall converter efficiency. Standard diodes are not suitable for low-voltage switched mode power supplies. A Schottky diode with low forward voltage and fast reverse recovery should be used as a rectifier to minimize overall losses of the dc-dc converter. The maximum current rating of the diode must be high enough for the application. The maximum diode current is equal to the maximum current in the inductor that was calculated in equation 3. The maximum reverse voltage is the output voltage. The chosen diode should therefore have a reverse voltage rating higher than the output voltage.

Table 4. Recommended Diodes

VENDOR	PART NUMBER
Motorola Surface Mount	MBRM120LT3
	MBR0520LT1
Motorola Axial Lead	1N1517
	RB520S-30
ROHM	RB160L–40

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The typical forward voltage of those diodes is in the range of 0.35 to 0.45 V assuming a peak diode current of 600 mA.

10.2.2.6 Compensation of the Control Loop

An R/C/C network must be connected to the COMP pin in order to stabilize the control loop of the converter. Both the pole generated by the inductor L1 and the zero caused by the ESR and capacitance of the output capacitor must be compensated. The network shown in Figure 18 satisfies these requirements.

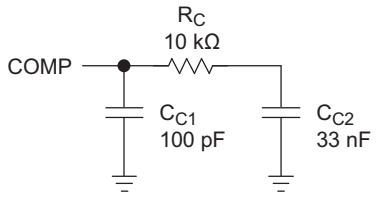


Figure 18. Compensation of the Control Loop

Resistor R_C and capacitor C_{C2} depend on the chosen inductance. For a 33-µH inductor, the capacitance of C_{C2} should be chosen to 33 nF, or in other words, if the inductor is xx µH, the chosen compensation capacitor should be xx nF, the same number value. The value of the compensation resistor is then chosen based on the requirement to have a time constant of 0.3 ms for the R/C network of R_C and C_{C2}; hence for a 33-nF capacitor, a 10-kΩ resistor should be chosen for R_C.

Capacitor C_{C1} is depending on the ESR and capacitance value of the output capacitor, and on the value chosen for R_C. Its value is calculated using following equation:

$$C_{C1} = \frac{C_O \times ESR_{COUT}}{3 \times R_C} \quad (7)$$

For a selected output capacitor of 22 µF with an ESR of 0.2 Ω, and R_C of 33 kΩ, the value of C_{C1} is in the range of 100 pF.

Table 5. Recommended Compensation Components

INDUCTOR [µH]	OUTPUT CAPACITOR		R_C [kΩ]	C_{C1} [pF]	C_{C2} [nF]
	CAPACITANCE [µF]	ESR [Ω]			
33	22	0.2	10	100	33
22	22	0.3	15	100	22
10	22	0.4	33	100	10
10	10	0.1	33	100	10

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10.2.3 Application Curves

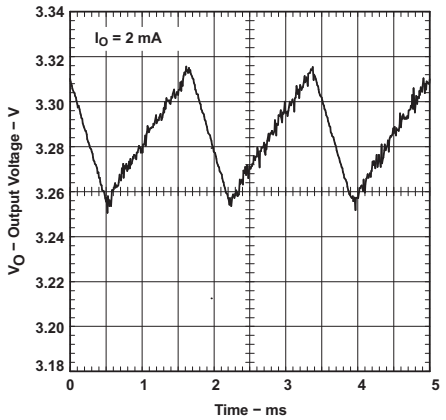


Figure 19. TPS61006 Output Voltage Ripple Amplitude

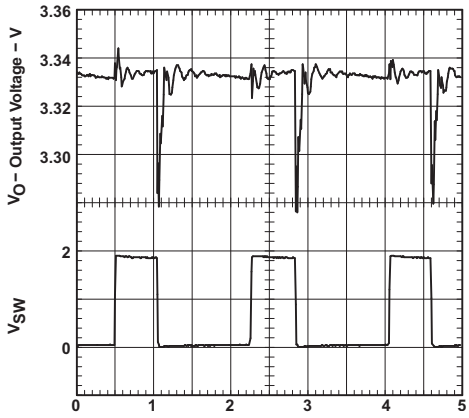


Figure 20. TPS61006 Output Voltage Ripple Amplitude

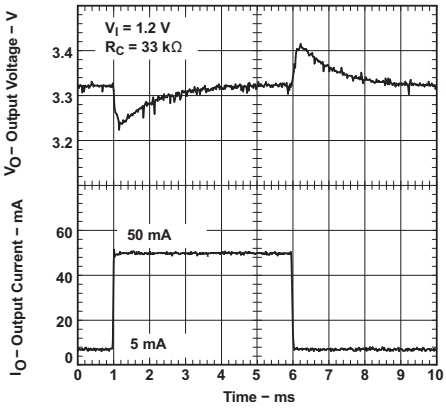


Figure 21. TPS61006 Load Transient Response

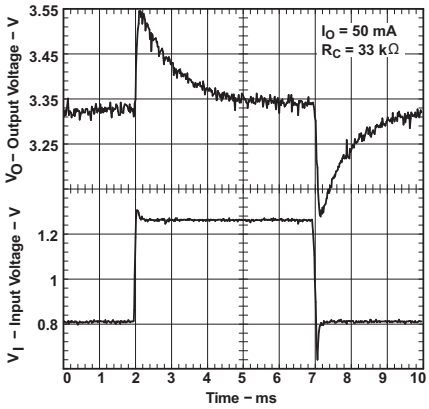


Figure 22. TPS61006 Line Transient Response

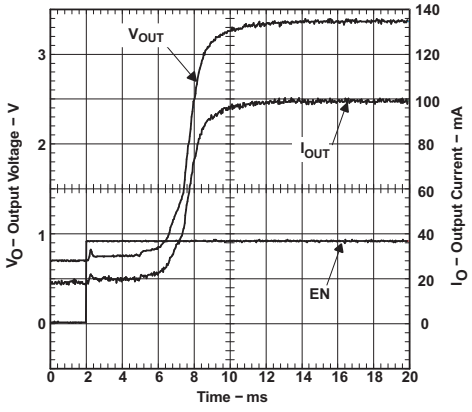


Figure 23. TPS61006 Start-up Timing Into 33-Ω Load

11 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 0.8 V and 3.3 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

12 Layout

12.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC. The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

12.2 Layout Example

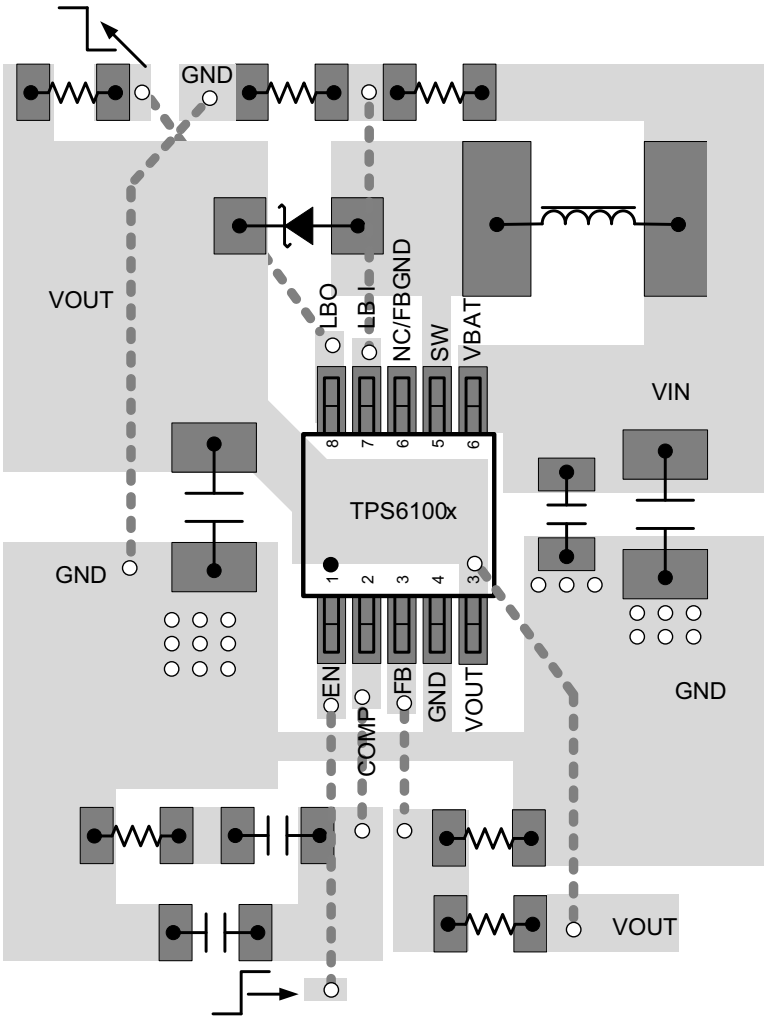


Figure 24. Layout Diagram

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12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in the system

The maximum junction temperature (T_J) of the TPS6100x devices is 125°C. The thermal resistance of the 10-pin MSOP package (DGS) is $R_{\theta JA}$ = 161°C/W. Specified regulator operation is assured to a maximum ambient temperature (T_A) of 85°C. Therefore, the maximum power dissipation is about 248 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - A}{R_{\Theta JA}} \quad (8)$$

Under normal operating conditions, the sum of all losses generated inside the converter IC is less than 50 mW, which is well below the maximum allowed power dissipation of 248 mW as calculated in Equation 8. Therefore, power dissipation is given no special attention.

Table 6 shows where the losses inside the converter are generated.

Table 6. Losses Inside the Converter

LOSSES	AMOUNTS
Conduction losses in the switch	36 mW
Switching losses	8 mW
Gate drive losses	2.3 mW
Quiescent current losses	< 1 mW
TOTAL	< 50 mW

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13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61000	Click here	Click here	Click here	Click here	Click here
TPS61001	Click here	Click here	Click here	Click here	Click here
TPS61002	Click here	Click here	Click here	Click here	Click here
TPS61003	Click here	Click here	Click here	Click here	Click here
TPS61004	Click here	Click here	Click here	Click here	Click here
TPS61005	Click here	Click here	Click here	Click here	Click here
TPS61006	Click here	Click here	Click here	Click here	Click here
TPS61007	Click here	Click here	Click here	Click here	Click here

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

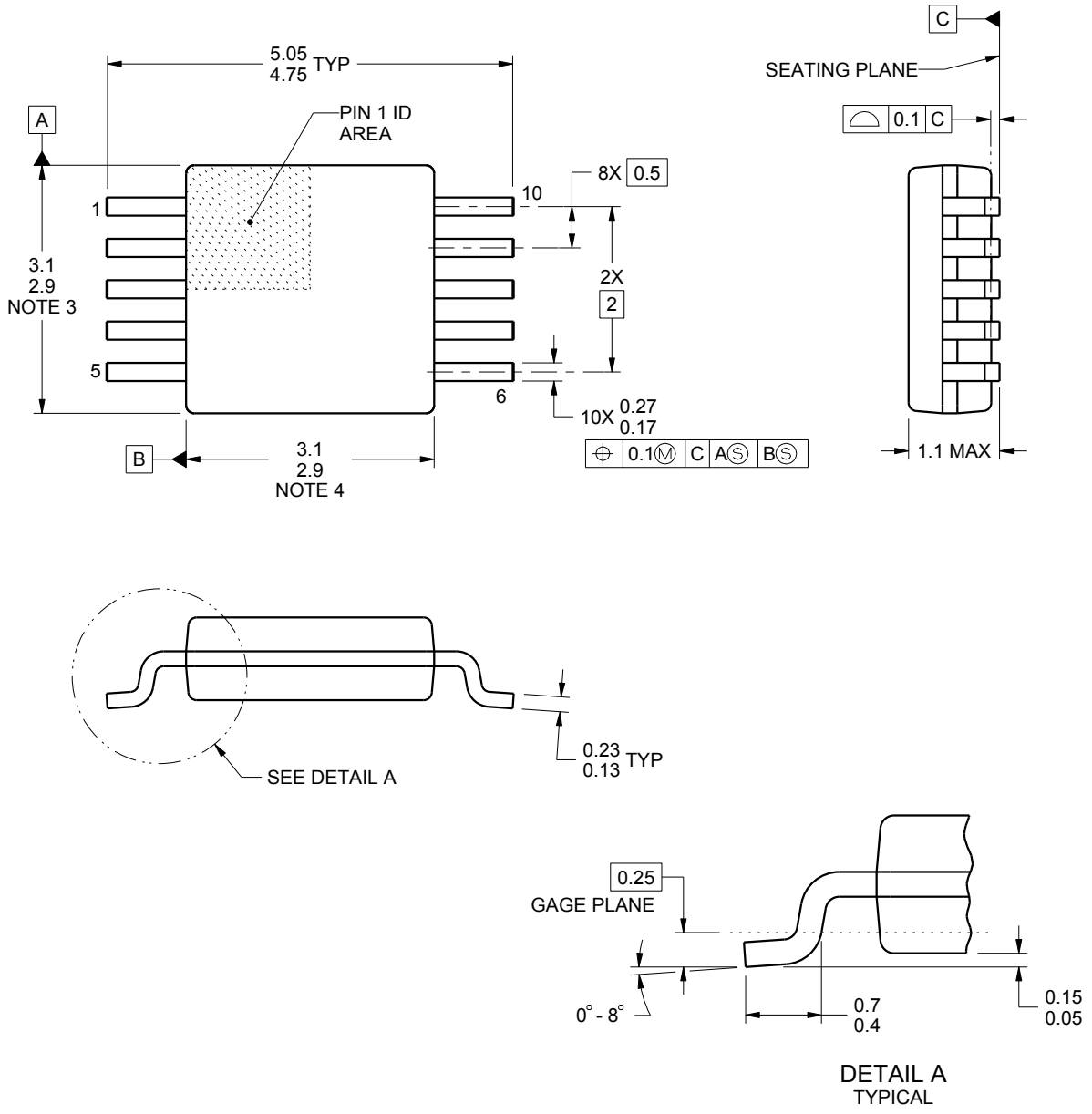
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PACKAGE OUTLINE

DGS0010A

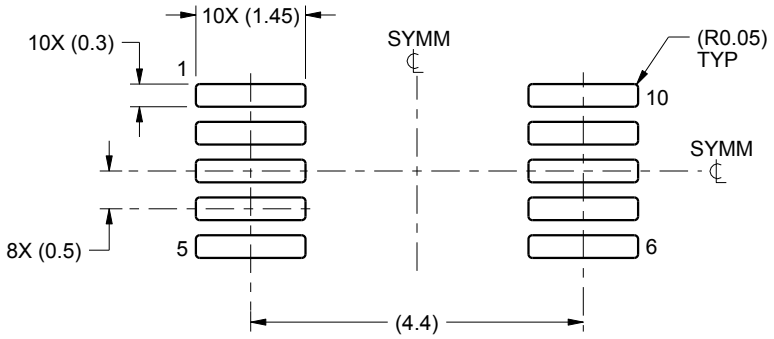
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

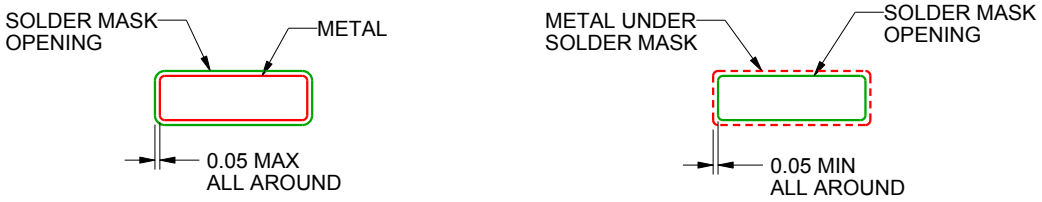


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

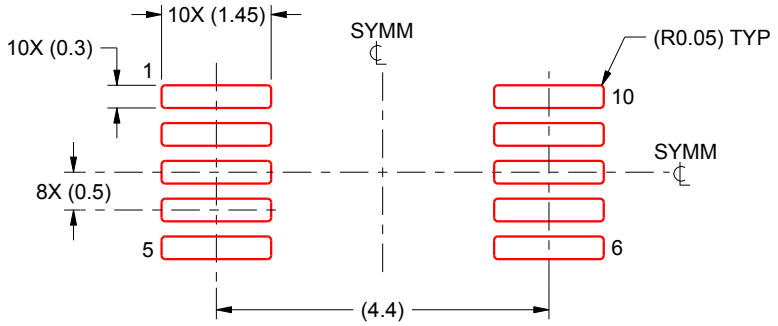


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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