ADS822
ADS825



SBAS069B – MARCH 2001 – REVISED AUGUST 2002

10-Bit, 40MHz Sampling ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- HIGH SNR: 60dB
- HIGH SFDR: 72dBFS
- LOW POWER: 190mW
- INTERNAL/EXTERNAL REFERENCE OPTION
- SINGLE-ENDED OR FULLY DIFFERENTIAL ANALOG INPUT
- PROGRAMMABLE INPUT RANGE
- LOW DNL: 0.5LSB
- SINGLE +5V SUPPLY OPERATION
- +3V OR +5V LOGIC I/O COMPATIBLE (ADS825)
- POWER DOWN: 20mW
- SSOP-28 PACKAGE

APPLICATIONS

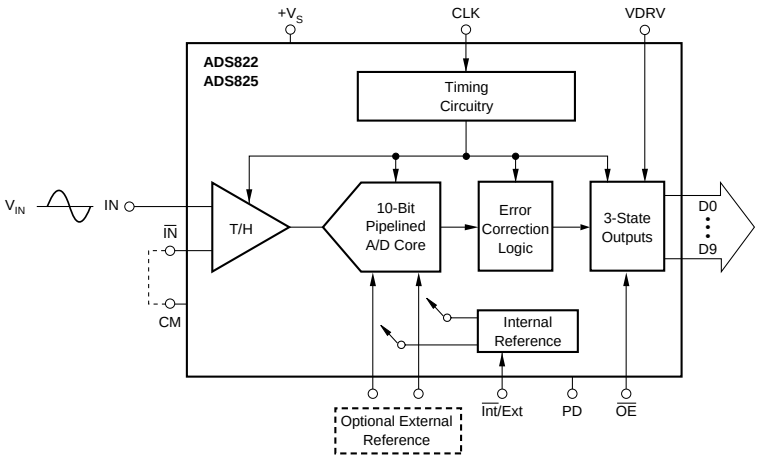
- MEDICAL IMAGING
- TEST EQUIPMENT
- COMPUTER SCANNERS
- COMMUNICATIONS
- VIDEO DIGITIZING

DESCRIPTION

The ADS822 and ADS825 are pipeline, CMOS Analog-to-Digital Converters (ADC) that operate from a single +5V power supply. These converters provide excellent performance with a single-ended input and can be operated with a differential input for added spurious performance. These high-performance converters include a 10-bit quantizer, high-bandwidth track-and-hold, and a high-accuracy internal reference. They also allow for the user to disable the internal reference and utilize external references. This external reference option provides excellent gain and offset matching when used in multichannel applications, or in applications where full-scale range adjustment is required.

The ADS822 and ADS825 employ digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for medical imaging, communications, video, and test instrumentation. The ADS822 and ADS825 offer power dissipation of 190mW and also provide a power-down mode, thus reducing power dissipation to only 20mW. The ADS825 is +3V or +5V logic I/O compatible.

The ADS822 and ADS825 are specified at a maximum sampling frequency of 40MSPS and a single-ended input range of 1.5V to 3.5V. The ADS822 and ADS825 are available in an SSOP-28 package and are pin-for-pin compatible with the 10-bit, 60MSPS ADS823 and ADS826, and the 10-bit, 75MSPS ADS828, providing an upgrade path to higher sampling frequencies.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2001, Texas Instruments Incorporated

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6V
Analog Input	–0.3V to ($+V_S$ + 0.3V)
Logic Input	–0.3V to ($+V_S$ + 0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DEMO BOARD ORDERING INFORMATION

PRODUCT	DEMO BOARD
ADS822E	DEM-ADS822E

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS822	SSOP-28	DB	–40°C to +85°C	ADS822E	ADS822E	Rails,
"	"	"	"	"	ADS822E/1K	Tape and Reel, 1000
ADS825	SSOP-28	DB	–40°C to +85°C	ADS825E	ADS825E	Rails,
"	"	"	"	"	ADS825E/1K	Tape and Reel, 1000

NOTES: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = full specified temperature range, V_S = +5V, single-ended input range = 1.5V to 3.5V, sampling rate = 40MHz and, external reference, unless otherwise noted.

PARAMETER	CONDITIONS	ADS822E			ADS825E[1]			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			10			10		Bits
SPECIFIED TEMPERATURE RANGE	Ambient Air		–40 to +85			–40 to +85		°C
ANALOG INPUT								
Standard Single-Ended Input Range	2Vp-p	1.5		3.5	*		*	V
Optional Single-Ended Input Range	1Vp-p	2		3	*		*	V
Common-Mode Range			2.5			*		V
Optional Differential Input Range	2Vp-p	2		3	*		*	V
Analog Input Bias Current			1			*		µA
Input Impedance			1.25 || 5			*		MΩ || pF
Track-Mode Input Bandwidth	–3dBFS Input		300			*		MHz
CONVERSION CHARACTERISTICS								
Sample Rate		10k		40M	*		*	Samples/s
Data Latency			5			*		Clk Cyc
DYNAMIC CHARACTERISTICS								
Differential Linearity Error (largest code error)								
f = 1MHz			±0.25	±1.0		*	*	LSB
f = 10MHz			±0.5			*		LSB
No Missing Codes			Tested			Tested		
Integral Nonlinearity Error, f = 1MHz			±0.5	±2.0		*	*	LSBs
Spurious-Free Dynamic Range[2]	Referred to Full-Scale							
f = 1MHz			72			71		dBFS[3]
f = 10MHz		63	66		60	65		dBFS
2-Tone Intermodulation Distortion[4]								
f = 9.5MHz and 9.9MHz (–7dB each tone)			–67			*		dBc
Signal-to-Noise Ratio (SNR)	Referred to Full-Scale							
f = 1MHz			60			*		dB
f = 10MHz		57	60		*	*		dB
Signal-to-(Noise + Distortion) (SINAD)	Referred to Full-Scale							
f = 1MHz			59			*		dB
f = 10MHz		56	58		*	*		dB
Effective Number of Bits[5], f = 1MHz			9.5			*		Bits
Output Noise	Input Tied to Common-Mode		0.2			*		LSBs rms
Aperture Delay Time			3			*		ns
Aperture Jitter			1.2			*		ps rms
Overvoltage Recovery Time			2			*		ns
Full-Scale Step Acquisition Time			5			*		ns

ELECTRICAL CHARACTERISTICS (Cont.)

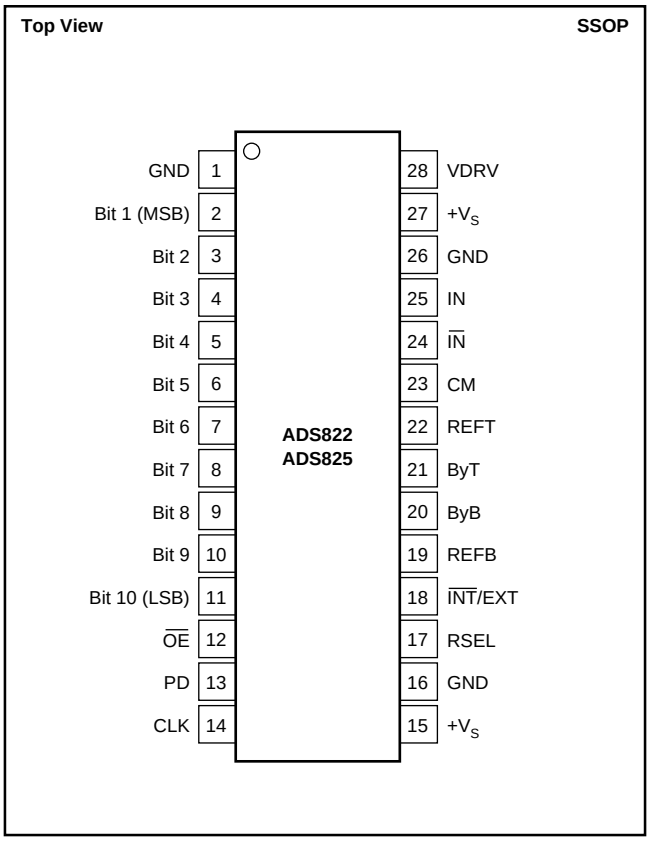
At T_A = full specified temperature range, V_S = +5V, single-ended input range = 1.5V to 3.5V, and sampling rate = 40MHz, external reference, unless otherwise noted.

PARAMETER	CONDITIONS	ADS822E MIN	ADS822E TYP	ADS822E MAX	ADS825E[1] MIN	ADS825E[1] TYP	ADS825E[1] MAX	UNITS
DIGITAL INPUTS								
Logic Family			CMOS-Compatible			TTL, +3V/+5V CMOS-Compatible		
Convert Command	Start Conversion		Rising Edge of Convert Clock			Rising Edge of Convert Clock		
High-Level Input Current[6] (V_{IN} = $5V_{DD}$)				100			*	µA
Low-Level Input Current (V_{IN} = 0V)				10			*	µA
High-Level Input Voltage		+3.5			+2.0			V
Low-Level Input Voltage				+1.0			+0.8	V
Input Capacitance			5			*		pF
DIGITAL OUTPUTS								
Logic Family			CMOS-Compatible			CMOS-Compatible		
Logic Coding			Straight Offset Binary			Straight Offset Binary		
Low Output Voltage (I_{OL} = 50µA to 1.6mA)	VDRV = 5V			+0.1			*	V
High Output Voltage, (I_{OH} = 50µA to 0.5mA)		+4.9			*			V
Low Output Voltage, (I_{OL} = 50µA to 1.6mA)	VDRV = 3V			+0.1			*	V
High Output Voltage, (I_{OH} = 50µA to 0.5mA)		+2.8			*			V
3-State Enable Time	$\overline{OE}$ = H to L		2	40		*	*	ns
3-State Disable Time	$\overline{OE}$ = L to H		2	10		*	*	ns
Output Capacitance			5			*		pF
ACCURACY (Internal Reference, 2Vp-p, Unless Otherwise Noted)	f_S = 2.5MHz							
Zero Error (referred to –FS)	at 25°C		±1.0	±3.0		*	*	% FS
Zero Error Drift (referred to –FS)			5			*		ppm/°C
Midscale Offset Error	at 25°C					±0.29		% FS
Gain Error[7]	at 25°C		±1.5	±3.5		*	*	% FS
Gain Error Drift[7]			38			*		ppm/°C
Gain Error[8]	at 25°C		±0.75	±2.5		*	*	% FS
Gain Error Drift[8]			25			*		ppm/°C
Power-Supply Rejection of Gain	ΔV_S = ±5%		70			*		dB
REFT Tolerance	Deviation From Ideal 3.5V		±10	±25		*	*	mV
REFB Tolerance[9]	Deviation From Ideal 1.5V		±10	±25		*	*	mV
External REFT Voltage Range		REFB + 0.8	3.5	V_S – 1.25	*	*	*	V
External REFB Voltage Range		1.25	1.5	REFT – 0.8	*	*	*	V
Reference Input Resistance	REFT to REFB		1.6			*		kΩ
POWER-SUPPLY REQUIREMENTS								
Supply Voltage: $+V_S$	Operating	+4.75	+5.0	+5.25	*	*	*	V
Supply Current: $+I_S$	Operating (External Reference)		40			*		mA
Power Dissipation: VDRV = 5V	External Reference		200	230		*	*	mW
VDRV = 3V	External Reference		190			*		mW
VDRV = 5V	Internal Reference		250			*		mW
VDRV = 3V	Internal Reference		240			*		mW
Power Down	Operating		20			*		mW
Thermal Resistance, θ_{JA}								
SSOP-28			89			*		°C/W

* Indicates the same specifications as the ADS822E.

NOTES: (1) ADS825E accepts a +3V clock input. (2) Spurious-Free Dynamic Range refers to the magnitude of the largest harmonic. (3) dBFS means dB relative to Full Scale. (4) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (5) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (6) A 50kΩ pull-down resistor is inserted internally on $\overline{OE}$ pin. (7) Includes internal reference. (8) Excludes internal reference. (9) Assured by design.

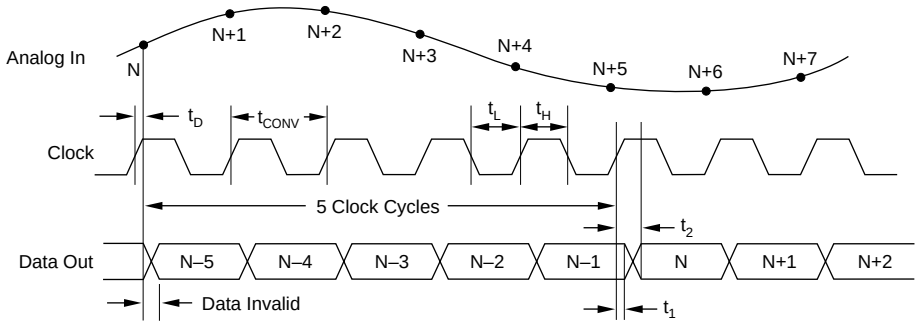
PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	GND	Ground
2	Bit 1	Data Bit 1 (D9) (MSB)
3	Bit 2	Data Bit 2 (D8)
4	Bit 3	Data Bit 3 (D7)
5	Bit 4	Data Bit 4 (D6)
6	Bit 5	Data Bit 5 (D5)
7	Bit 6	Data Bit 6 (D4)
8	Bit 7	Data Bit 7 (D3)
9	Bit 8	Data Bit 8 (D2)
10	Bit 9	Data Bit 9 (D1)
11	Bit 10	Data Bit 10 (D0) (LSB)
12	$\overline{OE}$	Output Enable. HI = high impedance state LO = normal operation (internal pull-down resistor)
13	PD	Power Down. HI = enable; LO = disable
14	CLK	Convert Clock Input
15	$+V_S$	+5V Supply
16	GND	Ground
17	RSEL	Input Range Select. HI = 2V; LO = 1V
18	$\overline{INT}$/EXT	Reference Select. HI = external, LO = internal
19	REFB	Bottom Reference
20	ByB	Bottom Ladder Bypass
21	ByT	Top Ladder Bypass
22	REFT	Top Reference
23	CM	Common-Mode Voltage Output
24	$\overline{IN}$	Complementary Input (–)
25	IN	Analog Input (+)
26	GND	Analog Ground
27	$+V_S$	+5V Supply
28	VDRV	Output Logic Driver Supply Voltage

TIMING DIAGRAM

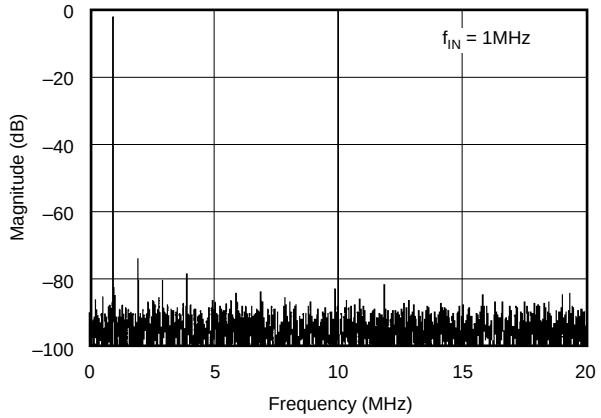


SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	25		100µs	ns
t_L	Clock Pulse Low	11.5	12.5		ns
t_H	Clock Pulse High	11.5	12.5		ns
t_D	Aperture Delay		3		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12	ns

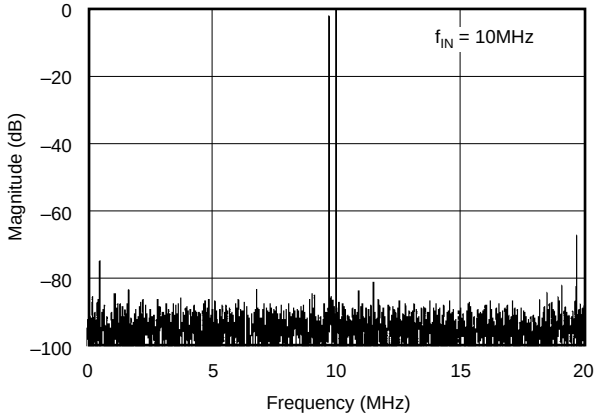
ELECTRICAL CHARACTERISTICS

At T_A = full specified temperature range, V_S = +5V, single-ended input range = 1.5V to 3.5V, sampling rate = 40MHz, and external reference, unless otherwise noted.

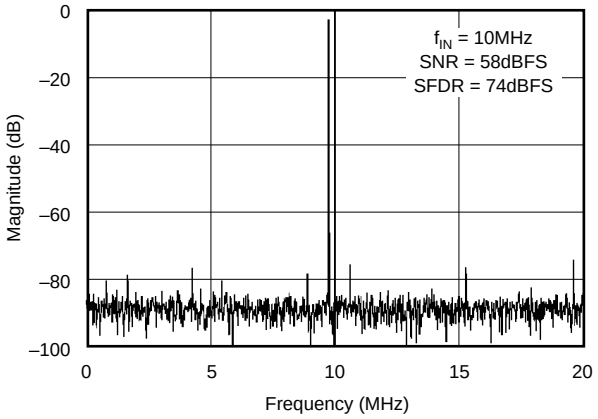
SPECTRAL PERFORMANCE



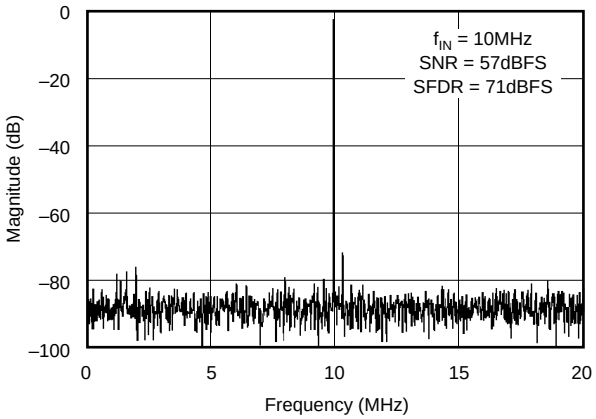
SPECTRAL PERFORMANCE



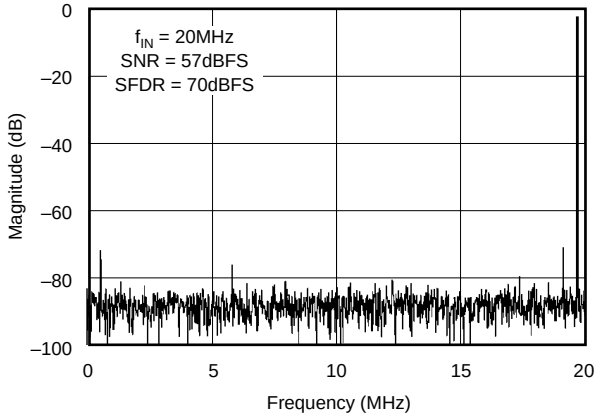
SPECTRAL PERFORMANCE
(Differential Input, 1Vp-p)



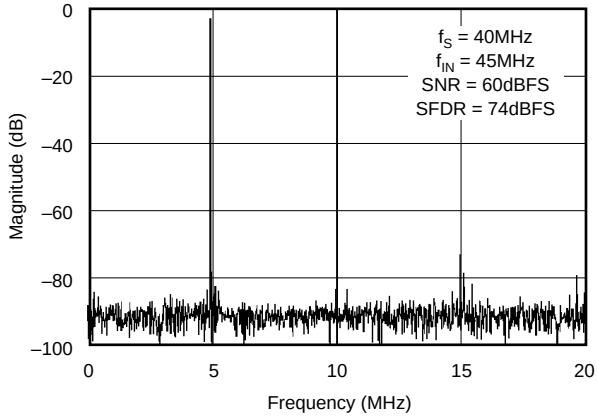
SPECTRAL PERFORMANCE
(Single-Ended, 1Vp-p)



SPECTRAL PERFORMANCE
(Single-Ended, 1Vp-p)



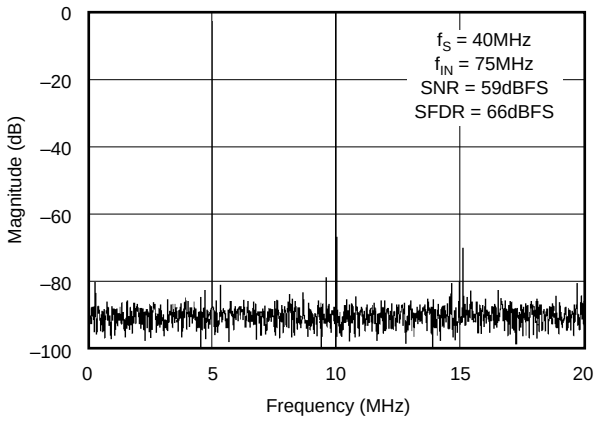
UNDERSAMPLING
(Differential Input, 2Vp-p)



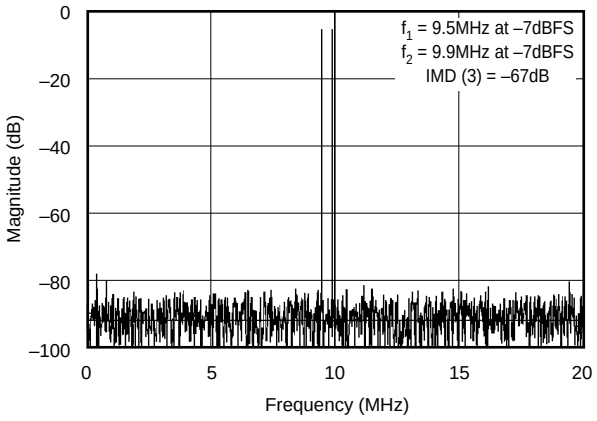
ELECTRICAL CHARACTERISTICS (Cont.)

At T_A = full specified temperature range, V_S = +5V, single-ended input range = 1.5V to 3.5V, sampling rate = 40MHz, and external reference, unless otherwise noted.

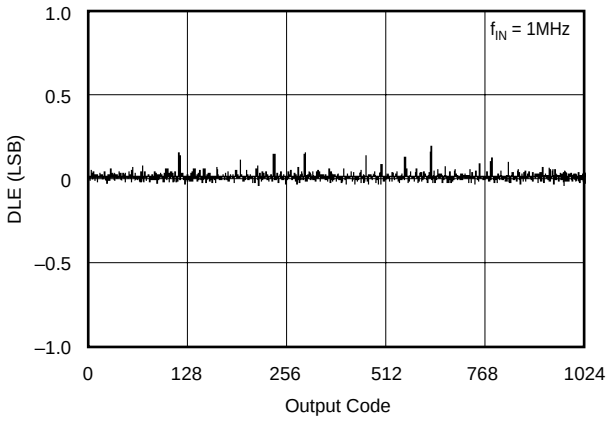
UNDERSAMPLING
(Differential Input, 2Vp-p)



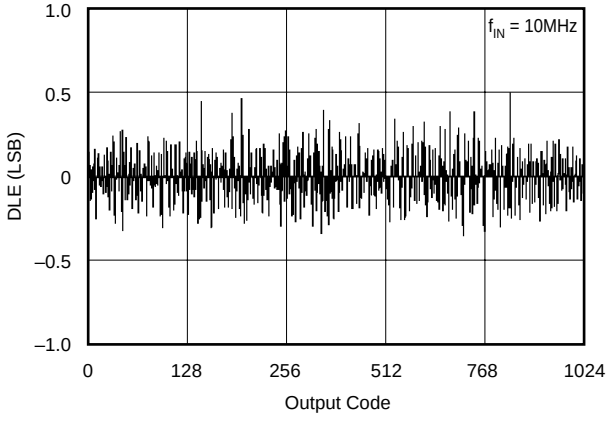
2-TONE INTERMODULATION DISTORTION



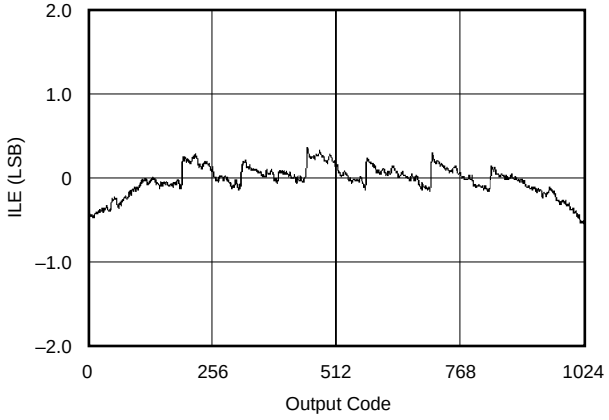
DIFFERENTIAL LINEARITY ERROR



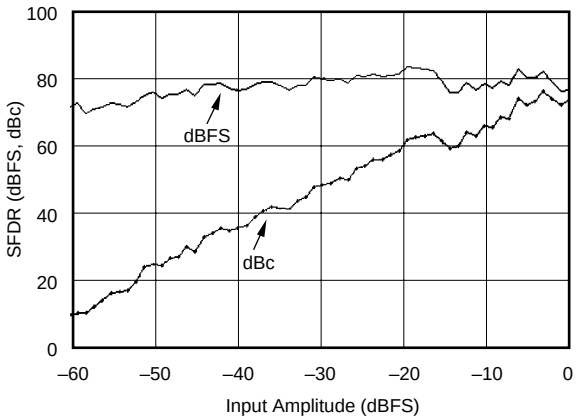
DIFFERENTIAL LINEARITY ERROR



INTEGRAL LINEARITY ERROR



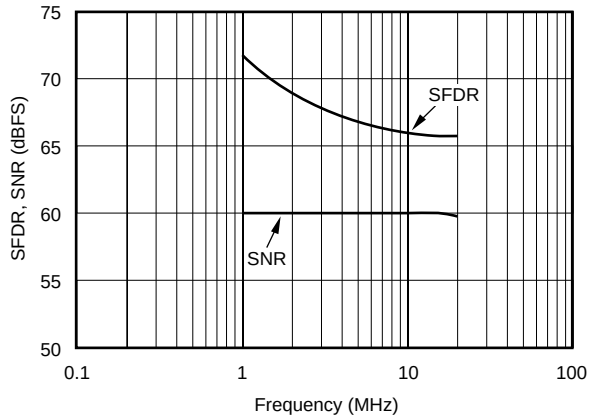
SWEPT POWER SFDR



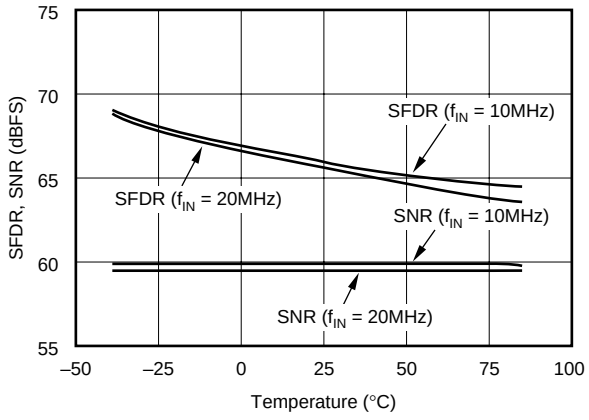
ELECTRICAL CHARACTERISTICS (Cont.)

At T_A = full specified temperature range, V_S = +5V, single-ended input range = 1.5V to 3.5V, sampling rate = 40MHz, and external reference, unless otherwise noted.

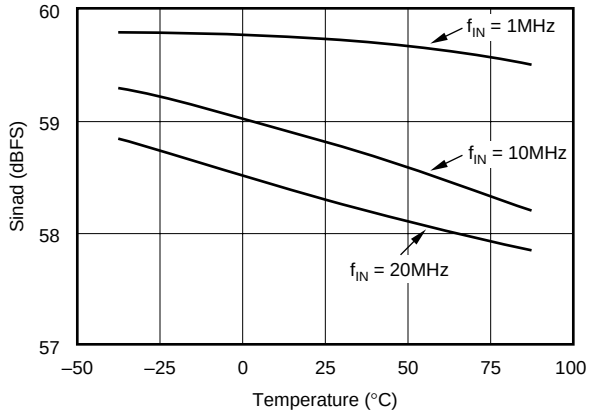
DYNAMIC PERFORMANCE vs INPUT FREQUENCY



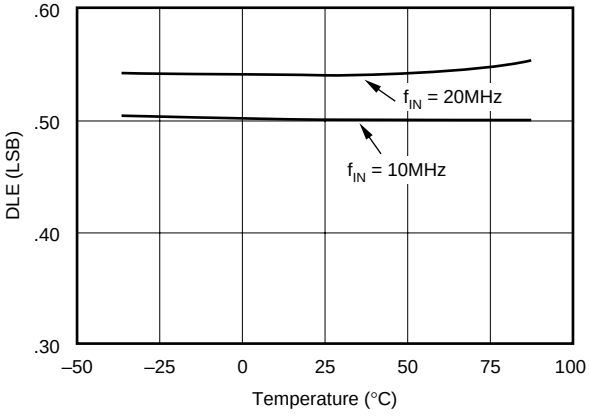
DYNAMIC PERFORMANCE vs TEMPERATURE



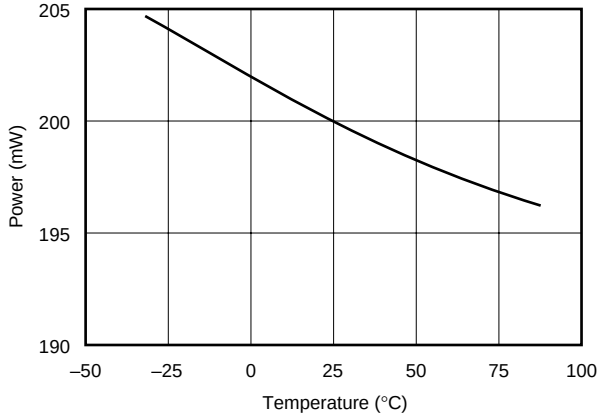
SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE



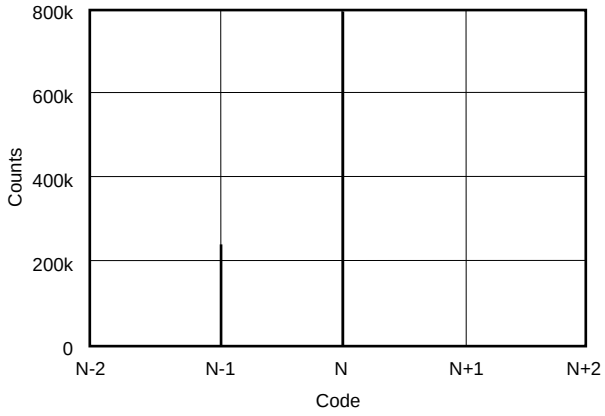
DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE



POWER DISSIPATION vs TEMPERATURE



OUTPUT NOISE (DC Input)



APPLICATION INFORMATION

THEORY OF OPERATION

The ADS822 and ADS825 are high-speed CMOS ADCs which employ a pipelined converter architecture consisting of nine internal stages. Each stage feeds its data into the digital error correction logic ensuring excellent differential linearity and no missing codes at the 10-bit level. The output data becomes valid on the rising clock edge (see Timing Diagram). The pipeline architecture results in a data latency of 5 clock cycles.

The analog inputs of the ADS822 and ADS825 are differential track-and-hold, as shown in Figure 1. The differential topology, along with tightly matched capacitors, produce a high level of AC performance while sampling at very high rates.

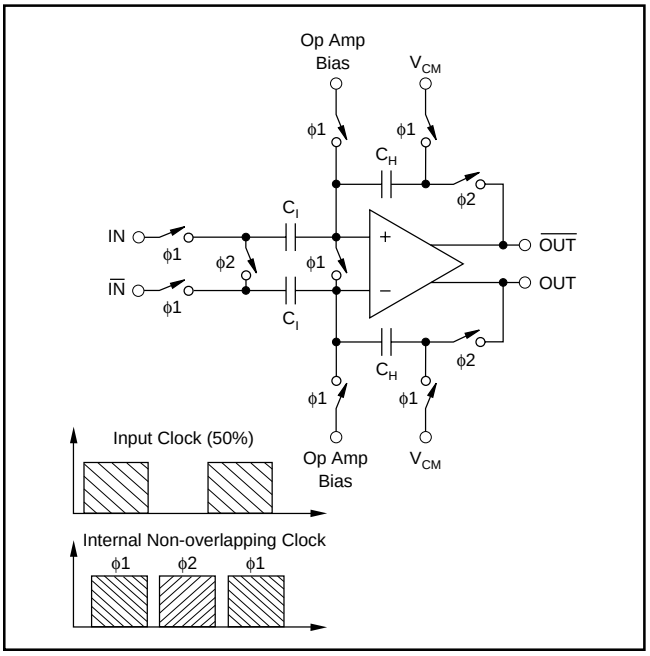


FIGURE 1. Simplified Circuit of Input Track-and-Hold with Timing Diagram.

The ADS822 and ADS825 allow their analog inputs to be driven either single-ended or differentially. The typical configuration for the ADS822 and ADS825 is the single-ended mode in which the input track-and-hold performs a single-ended-to-differential conversion of the analog input signal.

Both inputs (IN, $\overline{IN}$) require external biasing using a common-mode voltage that is typically at the mid-supply level ($+V_S/2$).

The following application discussion focuses on the single-ended configuration. Typically, its implementation is easier to achieve and the rated specifications for the ADS822 and ADS825 are characterized using the single-ended mode of operation.

DRIVING THE ANALOG INPUT

The ADS822 and ADS825 achieve excellent AC performance either in the single-ended or differential mode of operation. The selection for the optimum interface configuration will depend on the individual application requirements and system structure. For example, communications applications often process a band of frequencies that do not include DC, whereas in imaging applications, the previously restored DC level must be maintained correctly up to the ADC. Features on the ADS822 and ADS825, such as the input range select (RSEL pin) or the option for an external reference, provide the needed flexibility to accommodate a wide range of applications. In any case, the ADS822 and ADS825 should be configured such that the application objectives are met while observing the headroom requirements of the driving amplifier in order to yield the best overall performance.

INPUT CONFIGURATIONS

AC-Coupled, Single-Supply Interface

See Figure 2 for the typical circuit for an AC-coupled analog input configuration of the ADS822 and ADS825 while all components are powered from a single +5V supply.

With the RSEL pin connected HI, the full-scale input range is set to 2Vp-p. In this configuration, the top and bottom references (REFT, REFB) provide an output voltage of +3.5V and +1.5V, respectively. Two resistors (2x 1.62kΩ) are used to create a common-mode voltage (V_{CM}) of approximately +2.5V to bias the inputs of the driving amplifier A1. Using the OPA680 on a single +5V supply, its ideal common-mode point is at +2.5V which coincides with the recommended common-mode input level for the ADS822 and ADS825. This obviates the need of a coupling capacitor between the amplifier and the converter. Even though the OPA680 has an AC gain of +2, the DC gain is only +1 due to the blocking capacitor at resistor R_G.

The addition of a small series resistor (R_S) between the output of the op amp and the input of the ADS822 and ADS825 will be beneficial in almost all interface configurations. This will decouple the op amp's output from the capacitive load and avoid gain peaking, which can result in increased noise. For best spurious and distortion performance, the resistor value should be kept below 100Ω. Furthermore, the series resistor in combination with the 10pF capacitor establishes a passive low-pass filter limiting the bandwidth for the wideband noise, thus helping improve the SNR performance.

AC-Coupled, Dual Supply Interface

The circuit provided in Figure 3 illustrates typical connections for the analog input in case the selected amplifier operates on dual supplies. This might be necessary to take full advantage of very low distortion operational amplifiers, like the OPA642. The advantage is that the driving amplifier can be operated with a ground-referenced bipolar signal swing. This will keep the distortion performance at its lowest, since the signal range stays within the linear region of the op amp and sufficient headroom to the supply rails can be maintained. By capacitively coupling the single-ended signal to the input of the ADS822 and ADS825, its common-mode requirements can easily be satisfied with two resistors connected between the top and bottom references.

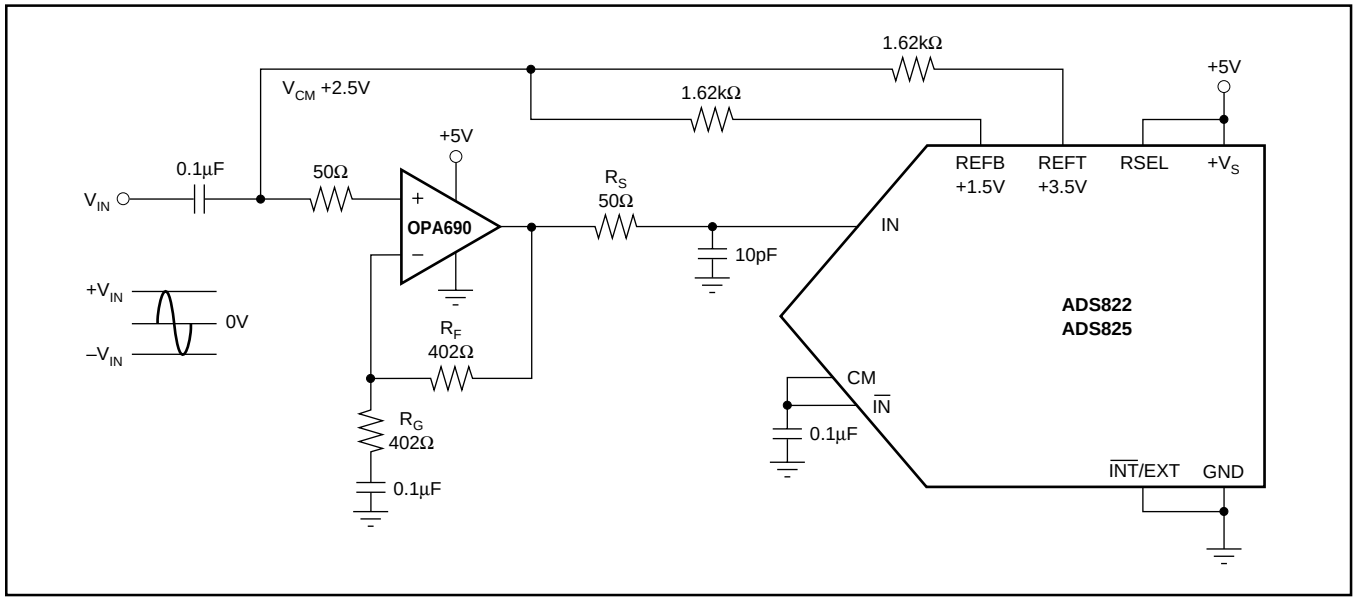


FIGURE 2. AC-Coupled Input Configuration for a 2Vp-p Full-Scale Range and a Common-Mode Voltage, V_{CM}, at +2.5V Derived From the Internal Top (REFT) and Bottom References (REFB).

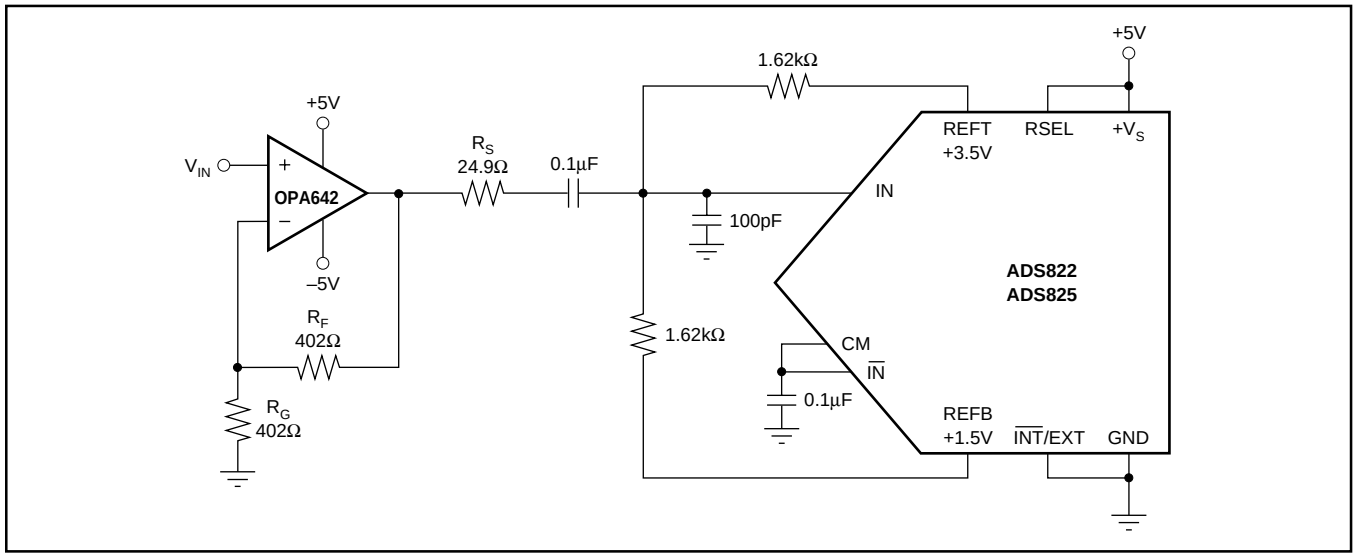


FIGURE 3. AC-Coupling the Dual Supply Amplifier, OPA642, to the ADS822 for a 2Vp-p Full-Scale Input Range.

For applications requiring the driving amplifier to provide a signal amplification, with a gain ≥ 5, consider using decompensated voltage-feedback op amps, like the OPA686, or current-feedback op amps like the OPA691.

DC-coupled with Level Shift

Several applications may require that the bandwidth of the signal path include DC, in which case, the signal has to be DC-coupled to the ADC. In order to accomplish this, the interface circuit has to provide a DC level shift to the analog input signal. See Figure 4 for a circuit that employs a dual op amp, A1, to drive the input of the ADS822 and ADS825, and level shifts the signal to be compatible with the selected input range. With the RSEL pin tied to the supply and the $\overline{INT}$/EXT pin to ground, the ADS822 and ADS825 are configured for a 2Vp-p input range and use the internal references. The complementary input ($\overline{IN}$) may be appropriately biased using the +2.5V common-mode voltage available at the CM pin. One half of amplifier A1 buffers the REFB pin and drives the voltage dividers R_1, R_2. Due to the op amp's noise gain of +2V/V, assuming $R_F = R_{IN}$, the common-mode voltage (V_{CM}) has to be re-scaled to +1.25V. This results in the correct DC level of +2.5V for the signal input (IN). Any DC voltage differences between the $\overline{IN}$ and IN inputs of the ADS822 and ADS825 effectively produces an offset, which can be corrected for by adjusting the resistor values of the divider, R_1 and R_2. The selection criteria for a suitable op amp should include the supply voltage, input bias current, output voltage swing, distortion, and noise specification. Note that in this example, the overall signal phase is inverted. To re-establish the original signal polarity, it is always possible to interchange the $\overline{IN}$ and IN connections.

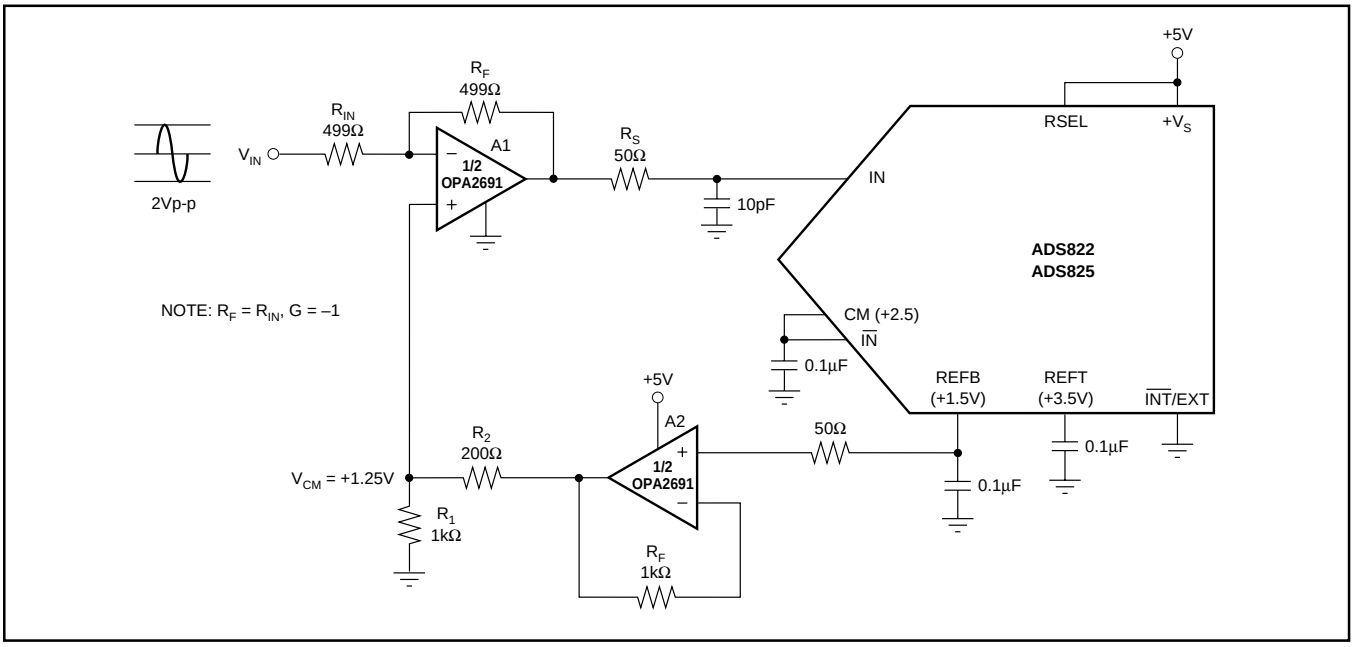


FIGURE 4. DC-Coupled Interface Circuit with Dual Current-Feedback Amplifier OPA2681.

SINGLE-ENDED-TO-DIFFERENTIAL CONFIGURATION (Transformer Coupled)

If the application requires a signal conversion from a single-ended source to feed the ADS822 and ADS825 differentially, a RF transformer might be a good solution. The selected transformer must have a center tap in order to apply the common-mode DC voltage necessary to bias the converter inputs. AC-grounding the center tap will generate the differential signal swing across the secondary winding. Consider a step-up transformer to take advantage of a signal amplification without the introduction of another noise source. Furthermore, the reduced signal swing from the source may lead to an improved distortion performance.

The differential input configuration may provide a noticeable advantage of achieving good SFDR performance over a wide range of input frequencies. In this mode, both inputs of the ADS822 and ADS825 see matched impedances, and the differential signal swing can be reduced to half of the swing required for single-ended drive. Figure 5 shows the schematic for the suggested transformer-coupled interface circuit.

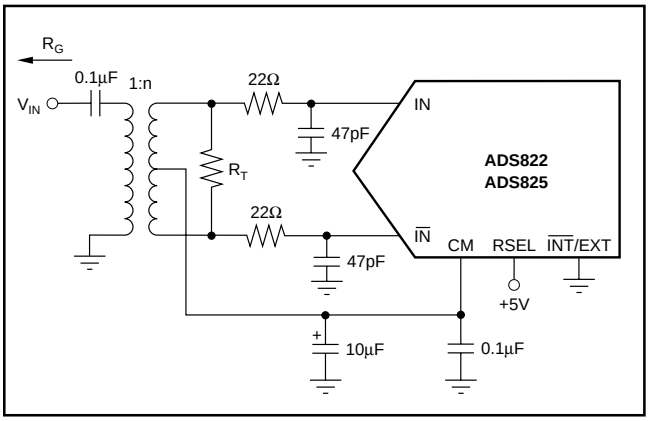


FIGURE 5. Transformer Coupled Input.

The component values of the R-C low-pass may be optimized depending on the desired roll-off frequency. The resistor across the secondary side (R_T) should be calculated using the equation $R_T = n^2 \bullet R_G$ to match the source impedance (R_G) for good power transfer and Voltage Standing Wave Ratio (VSWR).

REFERENCE OPERATION

Figure 6 depicts the simplified model of the internal reference circuit. The internal blocks are the bandgap voltage reference, the drivers for the top and bottom references, and the

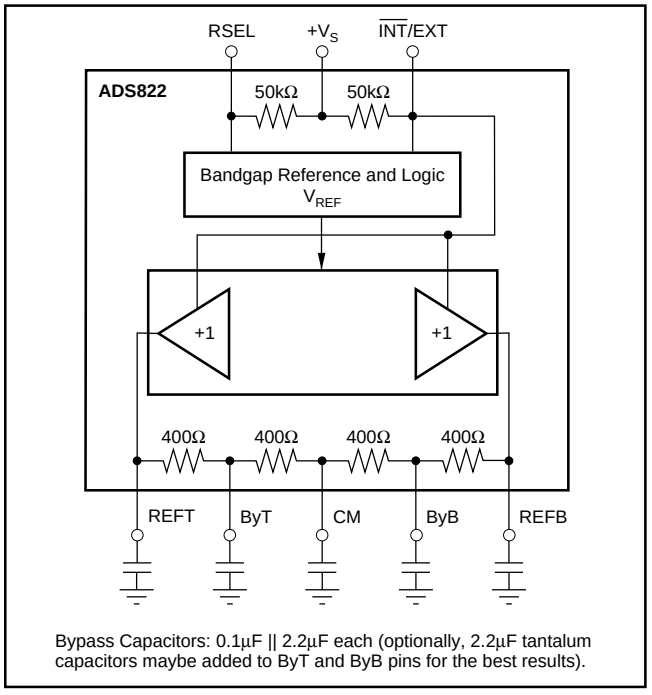


FIGURE 6. Equivalent Reference Circuit with Recommended Reference Bypassing.

resistive reference ladder. The bandgap reference circuit includes logic functions that allows setting the analog input swing of the ADS822 and ADS825 to either a 1Vp-p or 2Vp-p full-scale range simply by tying the RSEL pin to a Low or High potential, respectively. While operating the ADS822 in the external reference mode, the buffer amplifiers for the REFT and REFB are disconnected from the reference ladder.

As shown, the ADS822 and ADS825 have internal 50kΩ pull-up resistors at the range select pin (RSEL) and reference select pin ($\overline{INT}$/EXT). Leaving these pins open configures the ADS822 and ADS825 for a 2Vp-p input range and external reference operation. Setting the ADS822 and ADS825 up for internal reference mode requires bringing the $\overline{INT}$/EXT pin Low.

The reference buffers can be utilized to supply up to 1mA (sink and source) to external circuitry. The resistor ladders of the ADS822 and ADS825 are divided into several segments and have two additional nodes, ByT and ByB, which are brought out for external bypassing only (see Figure 6). To ensure proper operation with any reference configurations, it is necessary to provide solid bypassing at all reference pins in order to keep the clock feedthrough to a minimum. All bypassing capacitors should be located as close to their respective pins as possible.

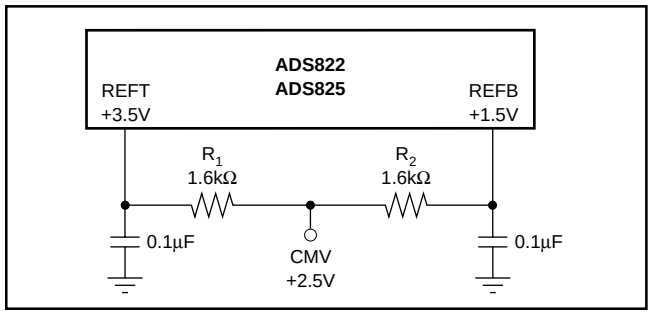


FIGURE 7. Alternative Circuit to Generate CM Voltage.

The common-mode voltage available at the CM pin may be used as a bias voltage to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this node, which is not buffered and has a high impedance. An alternative way of generating a common-mode voltage is given in Figure 7. Here, two external precision resistors (tolerance 1% or better) are located between the top and bottom reference pins. The common-mode voltage, CMV, will appear at the midpoint.

EXTERNAL REFERENCE OPERATION

For even more design flexibility, the internal reference can be disabled and an external reference voltage be used. The utilization of an external reference may be considered for applications requiring higher accuracy, improved temperature performance, or a wide adjustment range of the converter's full-scale range. Especially in multichannel applications, the use of a common external reference has the benefit of obtaining better matching of the full-scale range between converters.

The external references can vary as long as the value of the external top reference $REFT_{EXT}$ stays within the range of (V_S – 1.25V) and (REFB + 0.8V), and the external bottom reference $REFB_{EXT}$ stays within 1.25V and (REFT – 0.8V) (See Figure 8).

DIGITAL INPUTS AND OUTPUTS

Clock Input Requirements

Clock jitter is critical to the SNR performance of high-speed, high-resolution ADCs. Clock jitter leads to aperture jitter (t_A), which adds noise to the signal being converted. The ADS822 and ADS825 samples the input signal on the rising edge of the CLK input. Therefore, this edge should have the lowest possible jitter. The jitter noise contribution to total SNR is given by

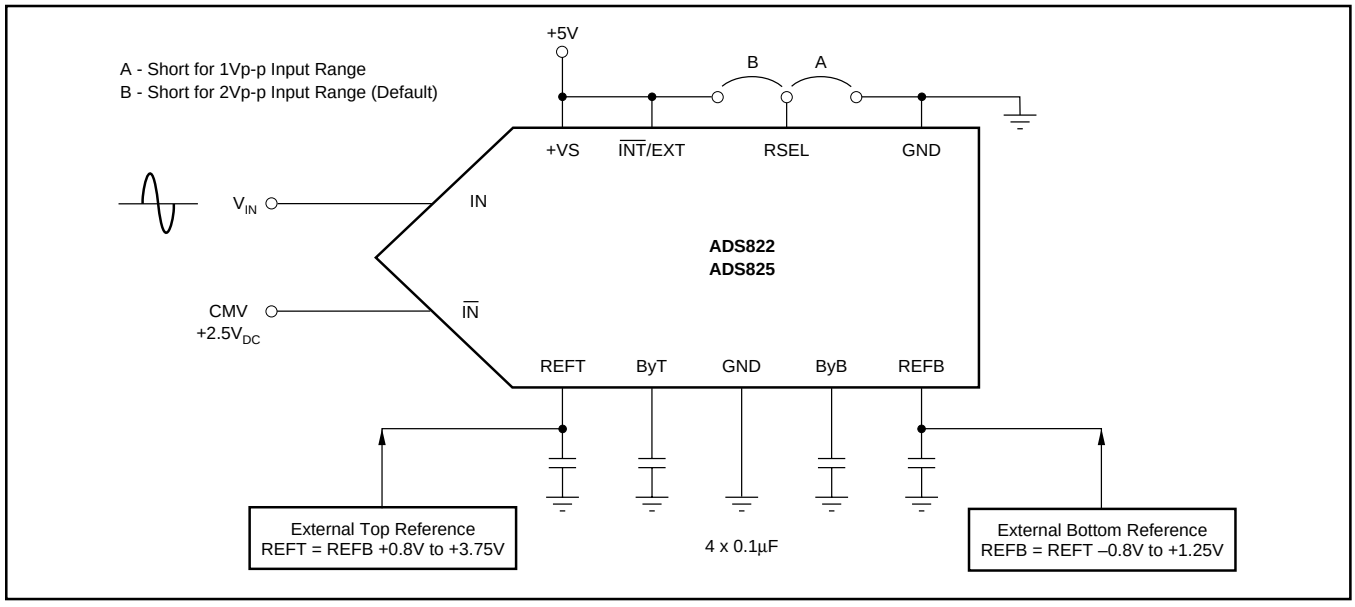


FIGURE 8. Configuration Example for External Reference Operation.

the following equation. If this value is near your system requirements, input clock jitter must be reduced.

$$\text{Jitter SNR} = 20\log\frac{1}{2\pi f_{IN}\, t_A}\text{ rms signal to rms noise}$$

where: f_{IN} is input signal frequency
t_A is rms clock jitter

Particularly in undersampling applications, special consideration should be given to clock jitter. The clock input should be treated as an analog input in order to achieve the highest level of performance. Any overshoot or undershoot of the clock signal may cause degradation of the performance. When digitizing at high sampling rates, the clock should have 50% duty cycle ($t_H = t_L$), along with fast rise and fall times of 2ns or less. The clock input of the ADS825 can be driven with either 3V or 5V logic levels. Using low-voltage logic (3V) may lead to improved AC performance of the converter.

Digital Outputs

The output data format of the ADS822 and ADS825 are in positive Straight Offset Binary code, as shown in Tables I and II. This format can easily be converted into the Binary Two's Complement code by inverting the MSB.

It is recommended to keep the capacitive loading on the data lines as low as possible (≤ 15pF). Higher capacitive loading will cause larger dynamic currents as the digital outputs are changing. Those high current surges can feed back to the analog portion of the ADS822 and ADS825 and affect the performance. If necessary, external buffers or latches close to the converter's output pins may be used to minimize the capacitive loading. They also provide the added benefit of isolating the ADS822 and ADS825 from any digital noise activities on the bus coupling back high frequency noise.

SINGLE-ENDED INPUT ($\overline{IN}$ = CMV)	STRAIGHT OFFSET BINARY (SOB)
+FS –1LSB (IN = REFT)	11 1111 1111
+1/2 Full Scale	11 0000 0000
Bipolar Zero (IN = CMV)	10 0000 0000
–1/2 Full Scale	01 0000 0000
–FS (IN = REFB)	00 0000 0000

TABLE I. Coding Table for Single-Ended Input Configuration with $\overline{IN}$ Tied to the Common-Mode Voltage (CMV).

DIFFERENTIAL INPUT	STRAIGHT OFFSET BINARY (SOB)
+FS –1LSB (IN = +3V, $\overline{IN}$ = +2V)	11 1111 1111
+1/2 Full Scale	11 0000 0000
Bipolar Zero (IN = $\overline{IN}$ = CMV)	10 0000 0000
–1/2 Full Scale	01 0000 0000
–FS (IN = +2V, $\overline{IN}$ = +3V)	00 0000 0000

TABLE II. Coding Table for Differential Input Configuration and 2Vp-p Full-Scale Range.

Digital Output Driver (VDRV)

The ADS822 features a dedicated supply pin for the output logic drivers, VDRV, which are not internally connected to the other supply pins. Setting the voltage at VDRV to +5V or +3V, the ADS822 and ADS825 produce corresponding logic levels and can directly interface to the selected logic family. The output stages are designed to supply sufficient current to drive a variety of logic families. However, it is recommended to use the ADS822 and ADS825 with +3V logic supply. This will lower the power dissipation in the output stages due to the lower output swing and reduce current glitches on the supply line which may affect the AC-performance of the converter. In some applications, it might be advantageous to decouple the VDRV pin with additional capacitors or a pi filter.

GROUNDING AND DECOUPLING

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Multilayer PC boards are recommended for best performance since they offer distinct advantages like minimizing ground impedance, separation of signal layers by ground layers, etc. The ADS822 and ADS825 should be treated as analog components. Whenever possible, the supply pins should be powered by the analog supply. This will ensure the most consistent results, since digital supply lines often carry high levels of noise which otherwise would be coupled into the converter and degrade the achievable performance. All ground connections on the ADS822 and ADS825 are internally joined together obviating the design of split ground planes. The ground pins (1, 16, 26) should directly connect to an analog ground plane which covers the PC board area around the converter. While designing the layout, it is important to keep the analog signal traces separated from any digital lines to prevent noise coupling onto the analog signal path. Due to their high sampling rates, the ADS822 and ADS825 generate high frequency current transients, and noise (clock feedthrough) that are fed back into the supply and reference lines. This requires that all supply and reference pins are sufficiently bypassed. Figure 9 shows the recommended decoupling scheme for the ADS822 and ADS825. In most cases, 0.1µF ceramic chip capacitors at each pin are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore, they should be located as close to the supply pins as possible. In addition, a larger bipolar capacitor (1µF to 22µF) should be placed on the PC board in proximity of the converter circuit.

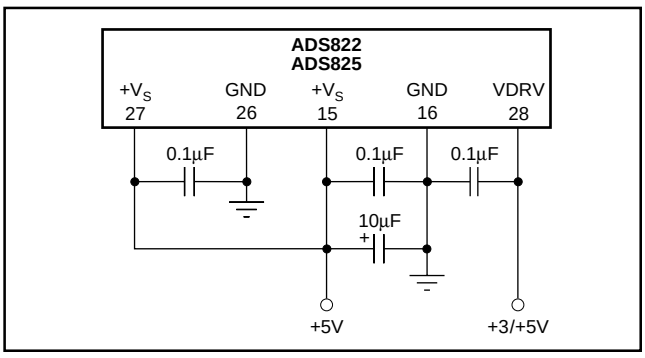


FIGURE 9. Recommended Bypassing for the Supply Pins.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS822E	ACTIVE	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS822E	Samples
ADS822E/1K	ACTIVE	SSOP	DB	28	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS822E	Samples
ADS825E	ACTIVE	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS825E	Samples
ADS825E/1K	ACTIVE	SSOP	DB	28	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS825E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

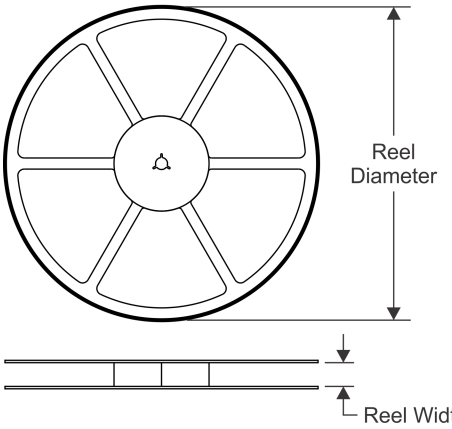
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

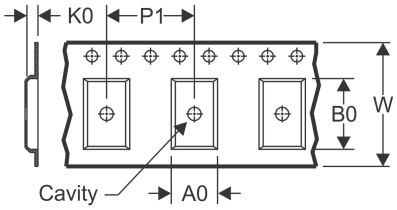
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

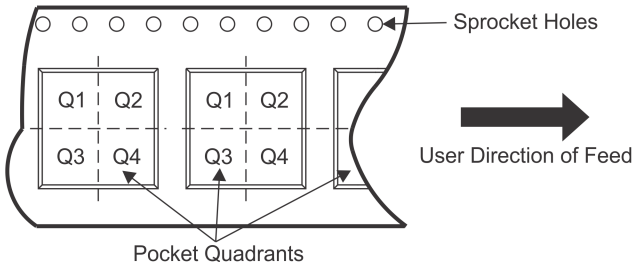


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

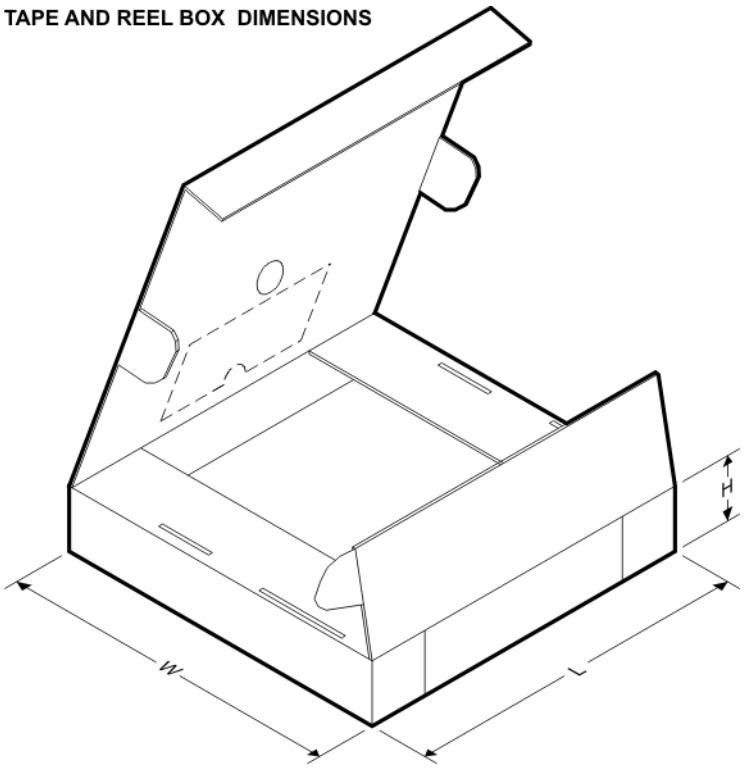
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS822E/1K	SSOP	DB	28	1000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
ADS825E/1K	SSOP	DB	28	1000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

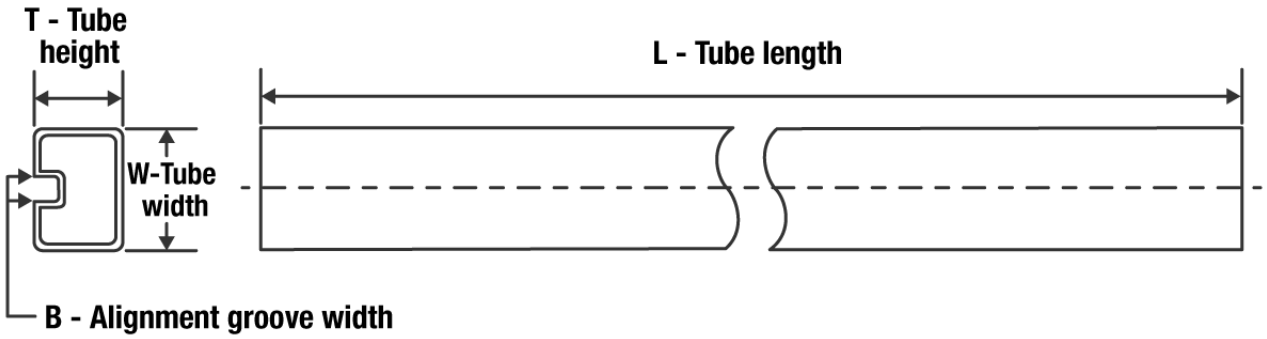
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS822E/1K	SSOP	DB	28	1000	350.0	350.0	43.0
ADS825E/1K	SSOP	DB	28	1000	367.0	367.0	38.0

TUBE



*All dimensions are nominal

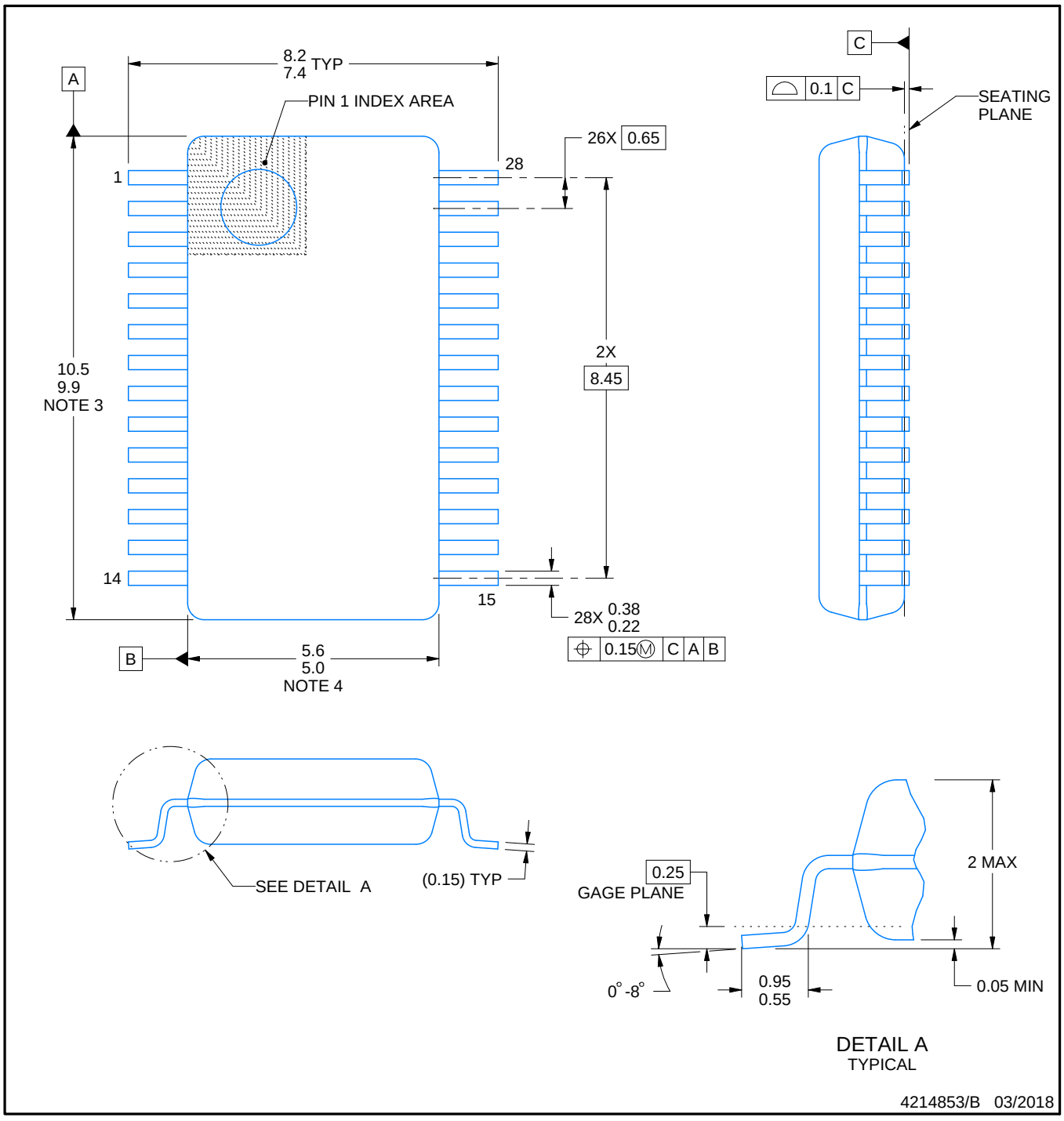
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS822E	DB	SSOP	28	50	530	10.5	4000	4.1
ADS825E	DB	SSOP	28	50	530	10.5	4000	4.1
ADS825E	DB	SSOP	28	50	530	10.5	4000	4.1

PACKAGE OUTLINE

DB0028A

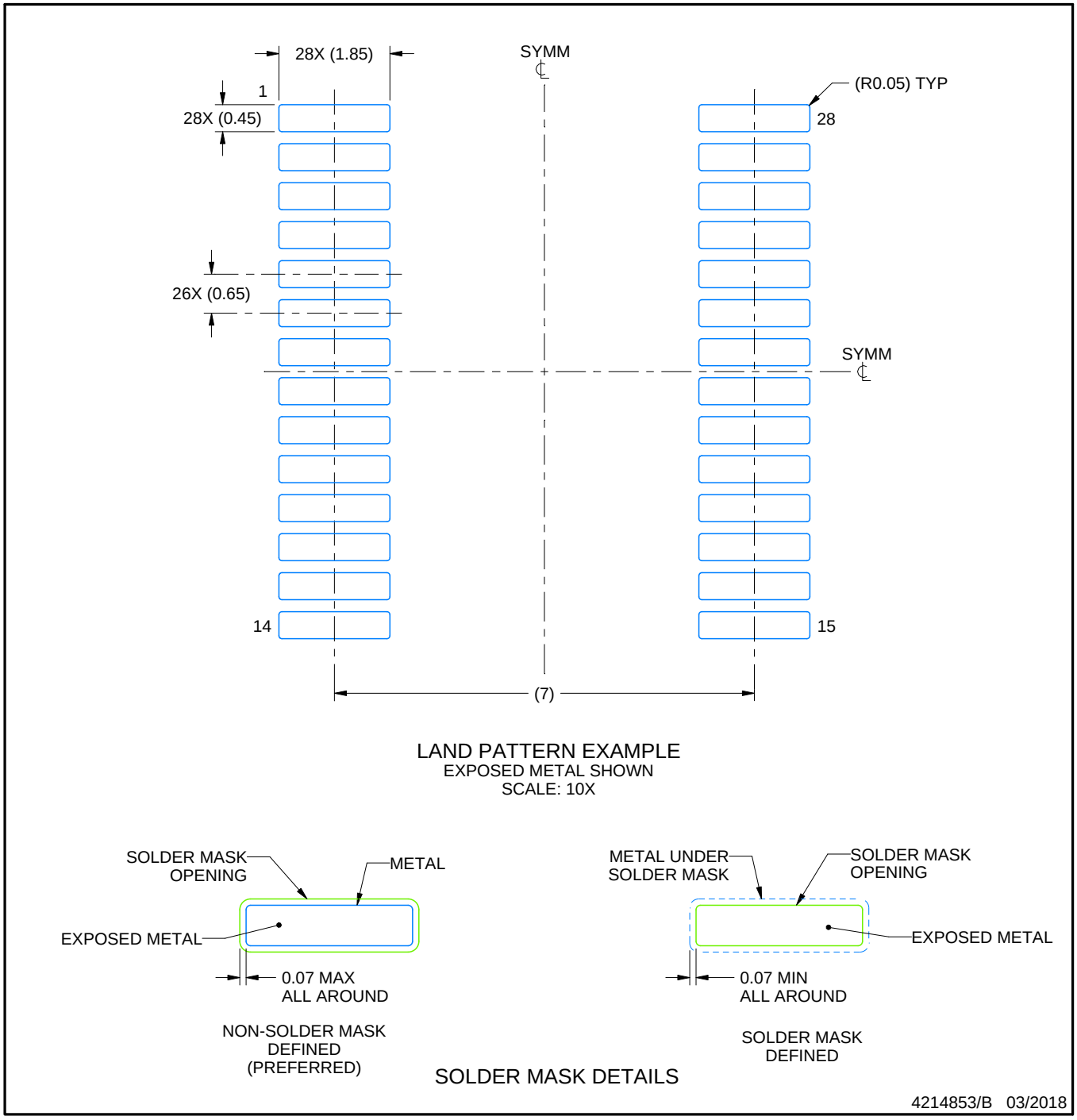
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



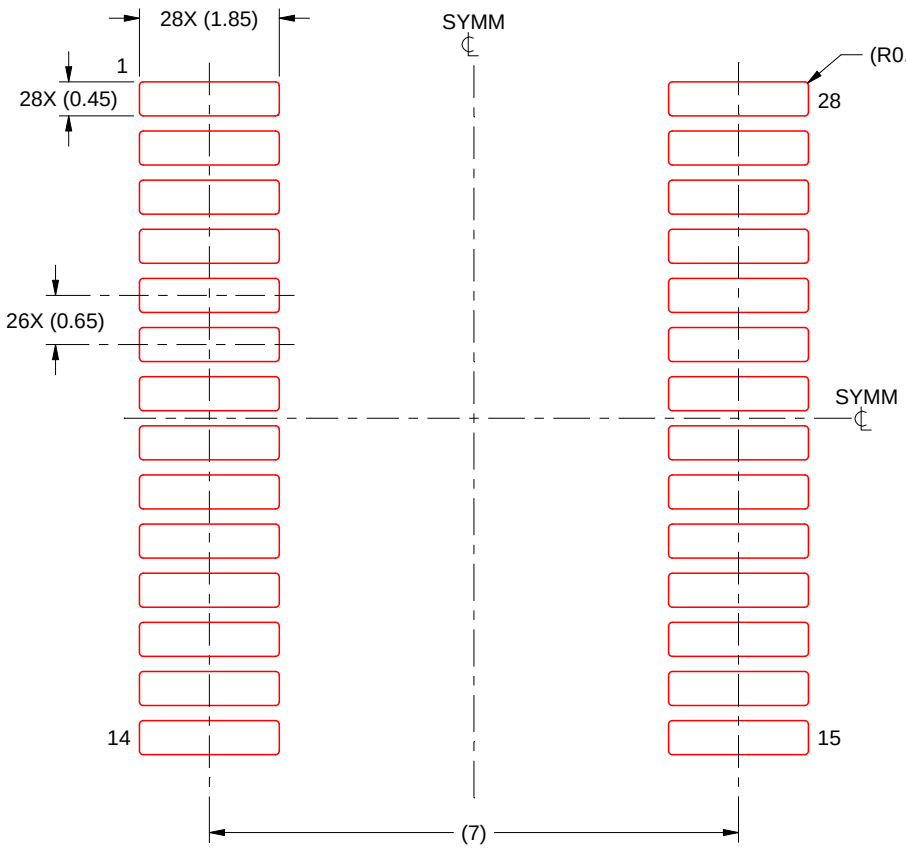
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated