采用芯片级封装的 3.5MHz 高效率升压转换器

查询样品: TPS61253, TPS61254, TPS61256, TPS61258, TPS61259

特性

- 运行频率为 **3.5MHz** 时，效率 **93%**
- 待机模式时，静态电流为 **22μA**
- 正常操作时，静态电流为 **36μA**
- **2.3V** 至 **5.5V** 的宽 V_{IN}范围
- $V_{IN} \geq V_{OUT}$运行
- V_{OUT}= 4.5V, V_{IN} ≥2.65V时，I_{OUT} ≥800mA
- V_{OUT} = 5.0V, V_{IN} ≥3.3V 时，I_{OUT} ≥1000mA
- V_{OUT} = 5.0V, V_{IN} ≥3.3V 时，I_{OUT} ≥1500mA（峰值）
- **DC** 电压输出总精度为 **±2%**
- 轻负载频率脉冲调制 **(PFM)** 模式
- 停机期间，可选待机模式或真实负载断开
- 热关断和过载保护
- 只需三个表面贴装外部组件
- 总解决方案尺寸 **< 25mm²**
- **9** 引脚 **NanoFree™(CSP)** 封装

应用范围

- 手机、智能电话
- 单声道、立体声 **APA** 应用
- **USB** 充电端口 **(5V)**

说明

TPS6125x 器件为电池供电类便携式应用提供了一个电源解决方案。 用于低功耗应用，TPS6125x 支持来自一个电池（充电电压低至 2.65V）的高达 800mA 的负载电流并且允许使用低成本芯片电感器和电容器。

2.3V 至 5.5V的宽输入电压使得此器件能够支持由锂离子电池（具有拓展电压范围）供电的应用。 不同固定电压输出版本支持介于 3.15V 至 5.0V 之间的电压。

TPS6125x 不但可在稳定的 3.5 MHz 开关频率下工作，而且还可在轻负载电流时进入节电模式，以维持整个负载电流范围内的高效率。 PFM 模式可在轻负载工作时将静态电流降至 36μA（典型值），从而可延长电池使用寿命。

此外，TPS6125x 还可保持其在输入电压电平的偏置输出。 在这个模式下，同步整流器的电流受到限制，从而使得外部负载（例如，音频放大器）由一个受限电源供电。 在此模式下，静态电流减少至 22μA。 关断模式下的输入电流少于 1μA（典型值），这样大大延长了电池寿命。

由于需要最小外部组件数量，TPS6125x 提供了一个非常小的解决方案尺寸。 为了实现小解决方案尺寸，允许使用小型电感器和输入电容器。 在关断期间，负载从电池上完全断开。

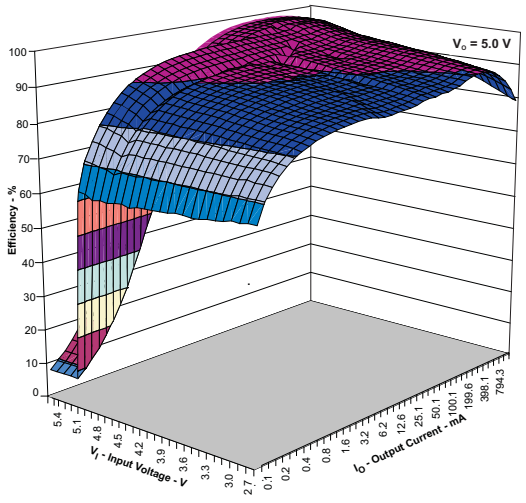


图 **1.** 效率与 负载电流间的关系

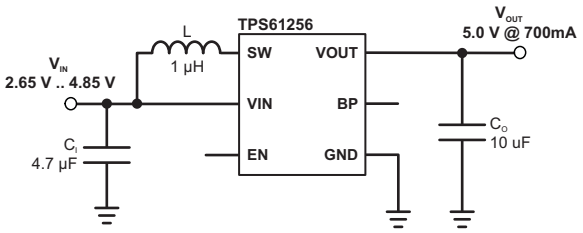


Figure 2. Smallest Solution Size Application

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2011–2012, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE DEVICE OPTION

T_A	PART NUMBER(1)	OUTPUT VOLTAGE	DEVICE SPECIFIC FEATURES	ORDERING(2)	PACKAGE MARKING CHIP CODE
–40°C to 85°C	TPS61253	5.0V	Supports 5V, up to 1500mA peak loading down to 3.3V input voltage	TPS61253YFF	SBF
	TPS61254	4.5V	Supports 4.5V/800mA loading down to 2.65V input voltage	TPS61254YFF	QWR
	TPS61255(3)	3.75V		TPS61255YFF	QWS
	TPS61256	5.0V	Supports 5V/900mA loading down to 3.3V input voltage	TPS61256YFF	RAV
	TPS61257(3)	4.3V		TPS61257YFF	RAO
	TPS61258	4.5V	Supports 4.5V, up to 1500mA peak loading down to 3.3V input voltage	TPS61258YFF	SAZ
	TPS61259	5.1V	Supports 5.1V, up to 1500mA peak loading down to 3.3V input voltage	TPS61259YFF	SAY

(1) For detailed ordering information please check the PACKAGE OPTION ADDENDUM section at the end of this datasheet.
(2) The YFF package is available in tape and reel. Add a R suffix (e.g. TPS61254YFFR) to order quantities of 3000 parts. Add a T suffix (e.g. TPS61254YFFT) to order quantities of 250 parts.
(3) Product preview.Contact TI factory for more information

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
Input voltage	Voltage at VIN(2), VOUT(2), SW(2), EN(2), BP(2)	–0.3 to 7	V
Input current	Continuous average current into SW (3)	1.8	A
	Peak current into SW (4)	3.5	A
Power dissipation		Internally limited	
Temperature range	Operating temperature range, T_A (5)	–40 to 85	°C
	Operating virtual junction, T_J	–40 to 150	°C
	Storage temperature range, T_{stg}	–65 to 150	°C
ESD rating(6)	Human Body Model - (HBM)	2000	V
	Charge Device Model - (CDM)	1000	V
	Machine Model - (MM)	200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) Limit the junction temperature to 105°C for continuous operation at maximum output power.
(4) Limit the junction temperature to 125°C for 5% duty cycle operation.
(5) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum junction temperature of 105°C.
(6) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

Copyright © 2011–2012, Texas Instruments Incorporated

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_I	Input voltage range	TPS61253	2.65(1)		4.85	V
		TPS61254	2.5		4.35	
		TPS61256	2.5		4.85	
		TPS61257	2.5		4.15	
		TPS61258	2.65(1)		4.35	
		TPS61259	2.65(1)		4.85	
R_L	Minimum resistive load for start-up	TPS6125X	55			Ω
L	Inductance		0.7	1.0	2.9	µH
C_O	Output capacitance		3.5	5	50	µF
T_A	Ambient temperature		–40		85	°C
T_J	Operating junction temperature		–40		125	°C

(1) Up to 1000mA peak output current.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS6125x YFF 9 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	110	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance		
θ_{JB}	Junction-to-board thermal resistance	35	
ψ_{JT}	Junction-to-top characterization parameter		
ψ_{JB}	Junction-to-board characterization parameter	50	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance		

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

Minimum and maximum values are at V_{IN} = 2.3V to 5.5V, V_{OUT} = 4.5V (or V_{IN}, whichever is higher), EN = 1.8V, T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V, V_{OUT} = 4.5V, EN = 1.8V, T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_Q	Operating quiescent current into V_{IN}	TPS6125x	I_{OUT} = 0mA, V_{IN} = 3.6V EN = V_{IN}, BP = GND Device not switching		30	45	µA
	Operating quiescent current into V_{OUT}				7	15	µA
	Standby mode quiescent current into V_{IN}		I_{OUT} = 0mA, V_{IN} = V_{OUT} = 3.6V EN = GND, BP = V_{IN} Device not switching		11	20	µA
	Standby mode quiescent current into V_{OUT}				9.5	15	µA
I_{SD}	Shutdown current	TPS6125x	EN = GND, BP = GND		0.85	5.0	µA
V_{UVLO}	Under-voltage lockout threshold	TPS6125x	Falling		2.0	2.1	V
			Hysteresis		0.1		V

Copyright © 2011–2012, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum values are at V_{IN} = 2.3V to 5.5V, V_{OUT} = 4.5V (or V_{IN}, whichever is higher), EN = 1.8V, T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V, V_{OUT} = 4.5V, EN = 1.8V, T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE, BYPASS							
V_{IL}	Low-level input voltage	TPS6125x				0.4	V
V_{IH}	High-level input voltage			1.0			V
I_{lkg}	Input leakage current		Input connected to GND or V_{IN}			0.5	µA
OUTPUT							
V_{OUT}	Regulated DC output voltage	TPS61253	2.3V ≤ V_{IN} ≤ 4.85V, I_{OUT} = 0mA PWM operation. Open Loop	4.92	5	5.08	V
			3.3V ≤ V_{IN} ≤ 4.85V, 0mA ≤ I_{OUT} ≤ 1000mA PFM/PWM operation	4.85	5	5.2	
			3.3V ≤ V_{IN} ≤ 4.85V, 0mA ≤ I_{OUT} ≤ 1500mA PFM/PWM operation Pulsed load test; Pulse width ≤ 20ms; Duty cycle ≤ 10%	4.75	5	5.2	
	Regulated DC output voltage	TPS61254	2.3V ≤ V_{IN} ≤ 4.35V, I_{OUT} = 0mA PWM operation. Open Loop	4.43	4.5	4.57	V
			2.65V ≤ V_{IN} ≤ 4.35V, 0mA ≤ I_{OUT} ≤ 800mA PFM/PWM operation	4.4	4.5	4.65	
	Regulated DC output voltage	TPS61256	2.3V ≤ V_{IN} ≤ 4.85V, I_{OUT} = 0mA PWM operation. Open Loop	4.92	5	5.08	V
			2.65V ≤ V_{IN} ≤ 4.85V, 0mA ≤ I_{OUT} ≤ 700mA PFM/PWM operation	4.9	5	5.2	
	Regulated DC output voltage	TPS61257	2.3V ≤ V_{IN} ≤ 4.15V, I_{OUT} = 0mA PWM operation. Open loop.	4.23	4.3	4.37	V
			2.65V ≤ V_{IN} ≤ 4.15V, 0mA ≤ I_{OUT} ≤ 800mA PFM/PWM operation	4.2	4.3	4.45	
	Regulated DC output voltage	TPS61258	2.3V ≤ V_{IN} ≤ 4.35V, I_{OUT} = 0mA PWM operation. Open Loop	4.43	4.5	4.57	V
			3.3V ≤ V_{IN} ≤ 4.35V, 0mA ≤ I_{OUT} ≤ 1500mA PFM/PWM operation Pulsed load test; Pulse width ≤ 20ms; Duty cycle ≤ 10%	4.3	4.5	4.65	
	Regulated DC output voltage	TPS61259	2.3V ≤ V_{IN} ≤ 4.85V, I_{OUT} = 0mA PWM operation. Open Loop	5.02	5.1	5.18	V
			3.4V ≤ V_{IN} ≤ 4.85V, 0mA ≤ I_{OUT} ≤ 1500mA PFM/PWM operation Pulsed load test; Pulse width ≤ 20ms; Duty cycle ≤ 10%	4.75	5.1	5.3	
ΔV_{OUT}	Power-save mode output ripple voltage	TPS61254 TPS61258	PFM operation, I_{OUT} = 1mA		45		mVpk
	Standby mode output ripple voltage		EN = GND, BP = V_{IN}, I_{OUT} = 0mA		80		
	PWM mode output ripple voltage		PWM operation, I_{OUT} = 200mA		20		
	Power-save mode output ripple voltage	TPS61253 TPS61256 TPS61259	PFM operation, I_{OUT} = 1mA		50		mVpk
	Standby mode output ripple voltage		EN = GND, BP = V_{IN}, I_{OUT} = 0mA		80		
	PWM mode output ripple voltage		PWM operation, I_{OUT} = 200mA		20		

Copyright © 2011–2012, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum values are at V_{IN} = 2.3V to 5.5V, V_{OUT} = 4.5V (or V_{IN}, whichever is higher), EN = 1.8V, T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V, V_{OUT} = 4.5V, EN = 1.8V, T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	High-side MOSFET on resistance	TPS6125x			170		mΩ
	Low-side MOSFET on resistance				100		
I_{lkg}	Reverse leakage current into VOUT	TPS6125x	EN = GND, BP = GND			3.5	µA
I_{LIM}	Switch valley current limit	TPS61253 TPS61258 TPS61259	EN = V_{IN}, BP = GND. Open Loop	3300	3620	3900	mA
		TPS61254 TPS61256 TPS61257	EN = V_{IN}, BP = GND. Open Loop	1900	2150	2400	
	Pre-charge mode current limit (linear mode)	TPS6125x	EN = GND, BP = V_{IN}	165	215	265	mA
	Overtemperature protection	TPS6125x			140		°C
	Overtemperature hysteresis				20		°C
OSCILLATOR							
f_{OSC}	Oscillator frequency	TPS6125x	V_{IN} = 3.6V V_{OUT} = 4.5V		3.5		MHz
TIMING							
	Start-up time	TPS6125x	BP = GND, I_{OUT} = 0mA. Time from active EN to start switching		70		µs
		TPS61253 TPS61254 TPS61256 TPS61258 TPS61259	BP = GND, I_{OUT} = 0mA. Time from active EN to V_{OUT}		400		µs

Copyright © 2011–2012, Texas Instruments Incorporated

PIN ASSIGNMENTS

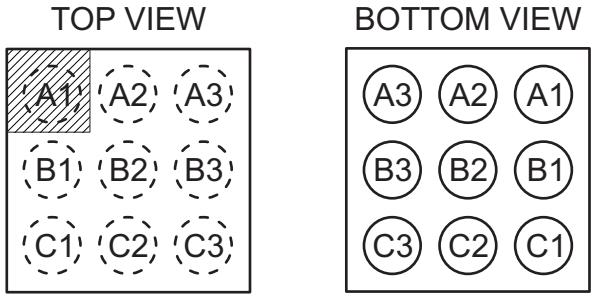
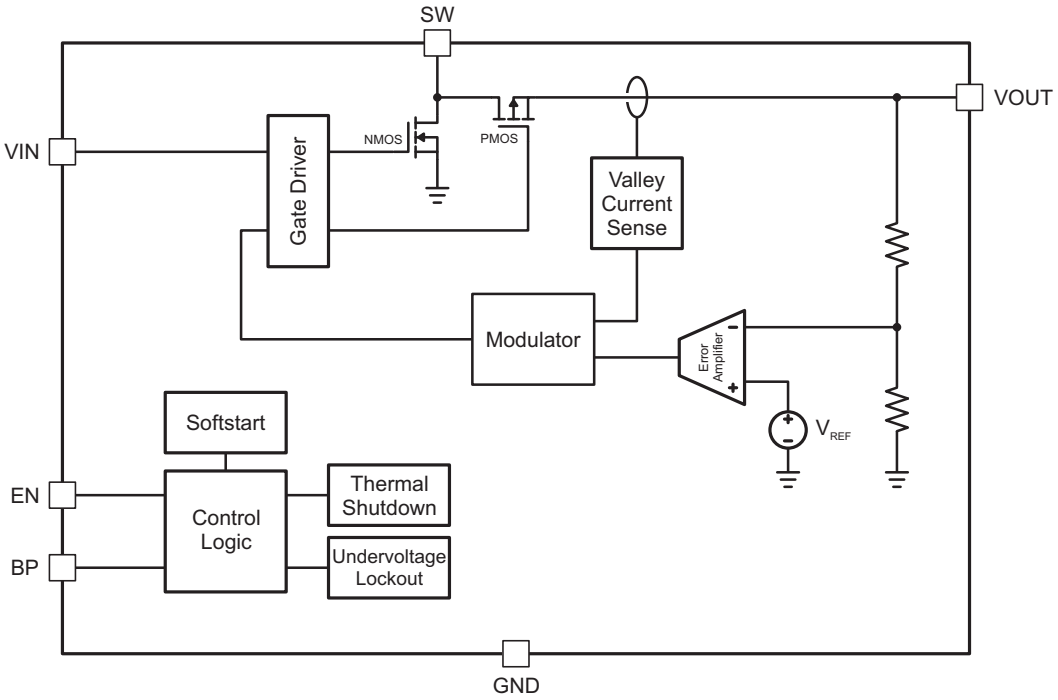


Table 1. TERMINAL FUNCTIONS

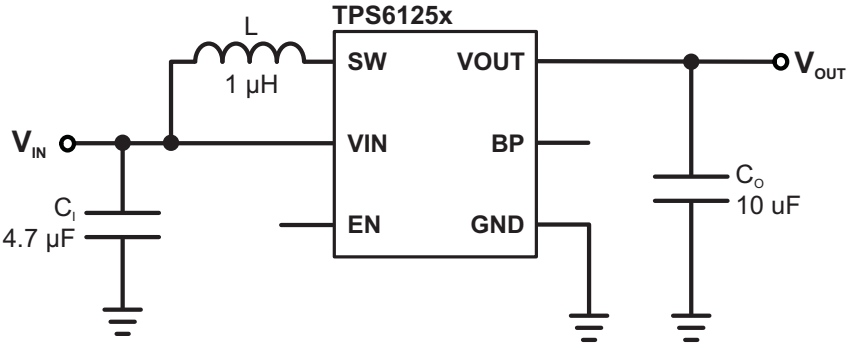
TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BP	C3	I	This is the mode selection pin of the device and is only of relevance when the device is disabled (EN = Low). This pin must not be left floating and must be terminated. Refer to Table 3 for more details.
			BP = Low: The device is in true shutdown mode. BP = High: The output is biased at the input voltage level with a maximum load current capability of ca. 150mA. In standby mode, the device only consumes a standby current of 22µA (typ).
EN	B3	I	This is the enable pin of the device. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin high enables the device. This pin must not be left floating and must be terminated.
GND	C1, C2		Ground pin.
SW	B1, B2	I/O	This is the switch pin of the converter and is connected to the drain of the internal Power MOSFETs.
VIN	A3	I	Power supply input.
VOUT	A1, A2	O	Boost converter output.

FUNCTIONAL BLOCK DIAGRAM



Copyright © 2011–2012, Texas Instruments Incorporated

PARAMETER MEASUREMENT INFORMATION



	EN	BP
Shutdown, True Load Disconnect (SD)	0	0
Standby Mode, Output Pre-Biased (SM)	0	1
Boost Operating Mode (BST)	1	X

Table 2. List of Components

REFERENCE	DESCRIPTION	PART NUMBER, MANUFACTURER
L (1)	1.0µH, 1.8A, 48mΩ, 3.2 x 2.5 x 1.0mm max. height	LQM32PN1R0MG0, muRata
L (2)	1.0µH, 3.7A, 37mΩ, 3.2 x 2.5 x 1.2mm max. height	DFE322512C, TOKO
C_I	4.7µF, 6.3V, 0402, X5R ceramic	GRM155R60J475M, muRata
C_O	10µF, 6.3V, 0603, X5R ceramic	GRM188R60J106ME84, muRata

(1) Inductor used to characterize TPS61254YFF, TPS61255YFF, TPS61256YFF and TPS61257YFF devices.
(2) Inductor used to characterize TPS61253YFF, TPS61258YFF and TPS61259YFF devices.

Copyright © 2011–2012, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
η	Efficiency	vs Output current	3, 4, 5, 7
		vs Input voltage	6
V_O	DC output voltage	vs Output current	8, 9, 10, 11, 12, 16
		vs Input voltage	13
I_O	Maximum output current	vs Input voltage	14, 15
ΔV_O	Peak-to-peak output ripple voltage	vs Output current	17, 18, 19
I_{CC}	Supply current	vs Input voltage	20, 21
I_{LIM}	DC pre-charge current	vs Differential input-output voltage	22, 23
	Valley current limit	vs Temperature	24, 25
$r_{DS(on)}$	MOSFET $r_{DS(on)}$	vs Temperature	26
	PFM operation		27
	PWM operation		28
	Combined line/load transient response		29
	Load transient response		30, 32
	AC load transient response		31, 33
	Start-up		34, 35

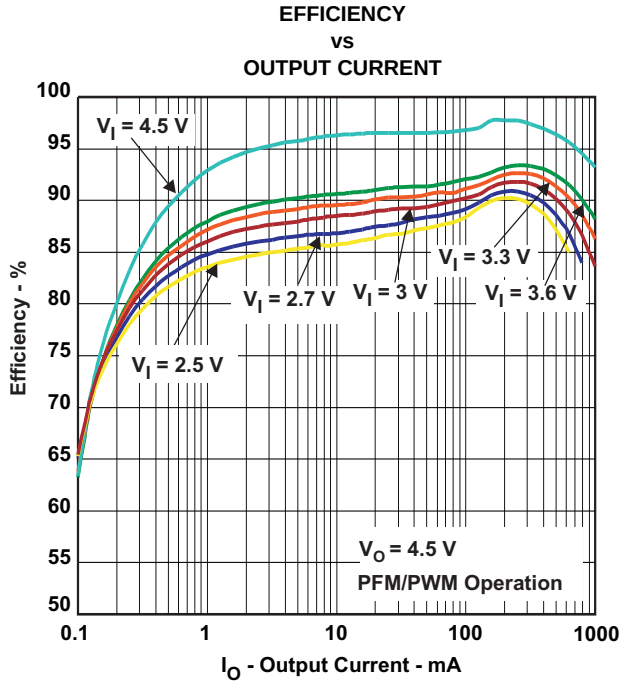


Figure 3.

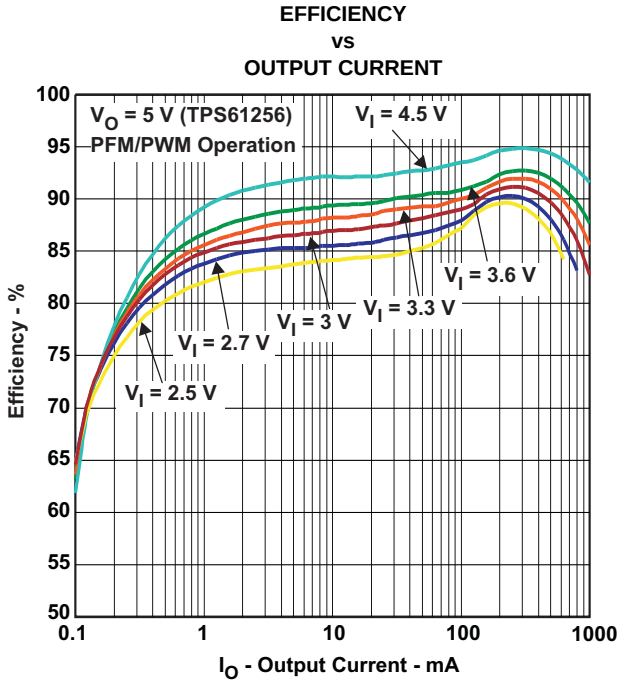


Figure 4.

Copyright © 2011–2012, Texas Instruments Incorporated

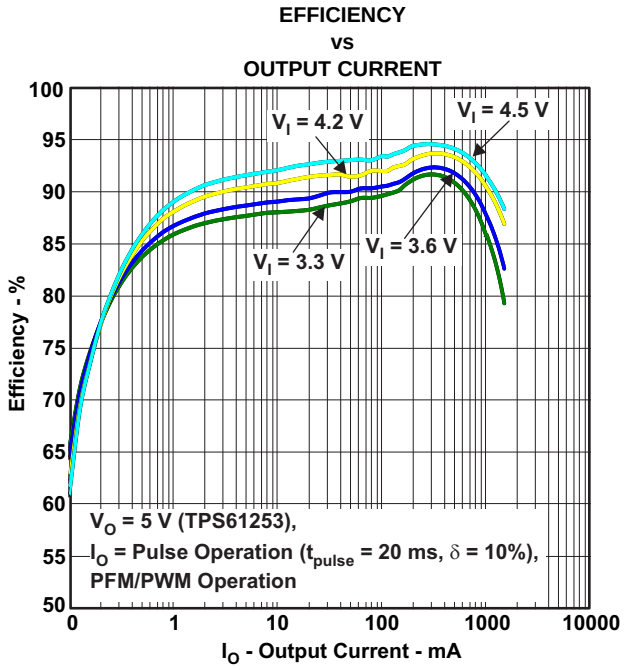


Figure 5.

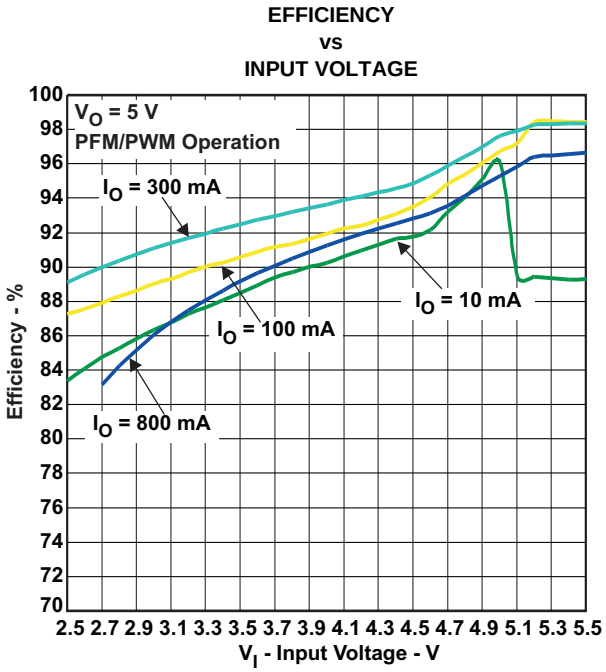


Figure 6.

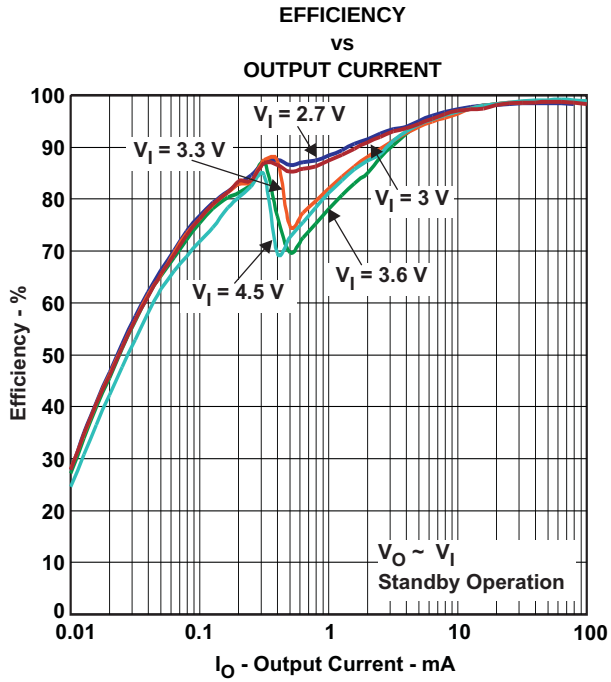


Figure 7.

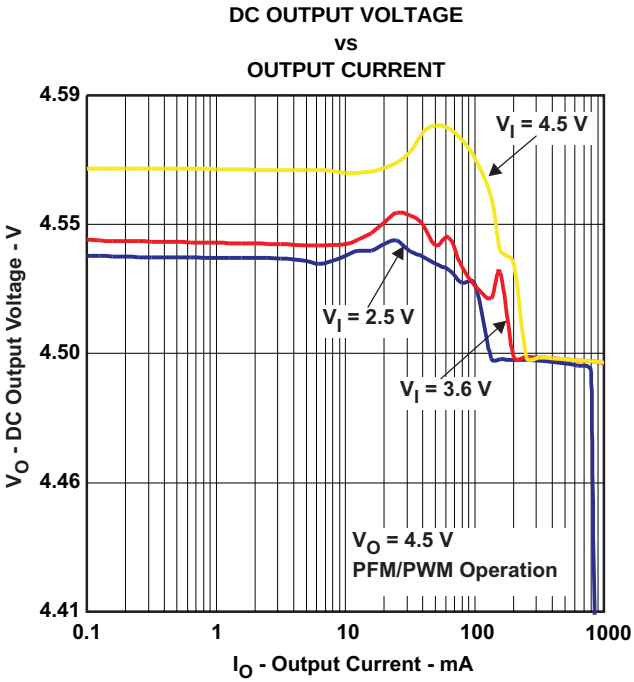


Figure 8.

Copyright © 2011–2012, Texas Instruments Incorporated

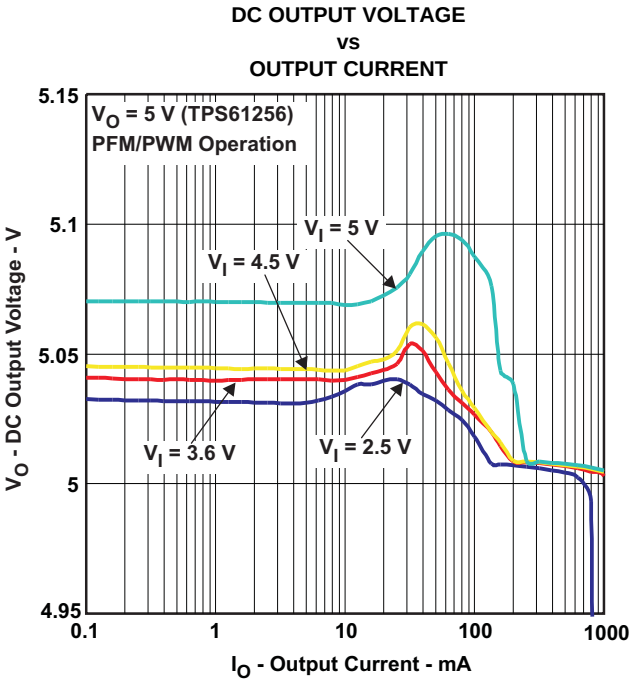


Figure 9.

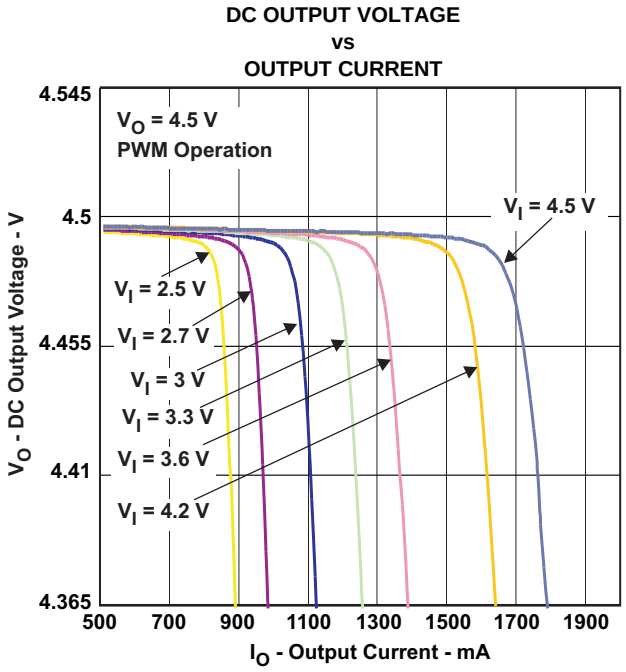


Figure 10.

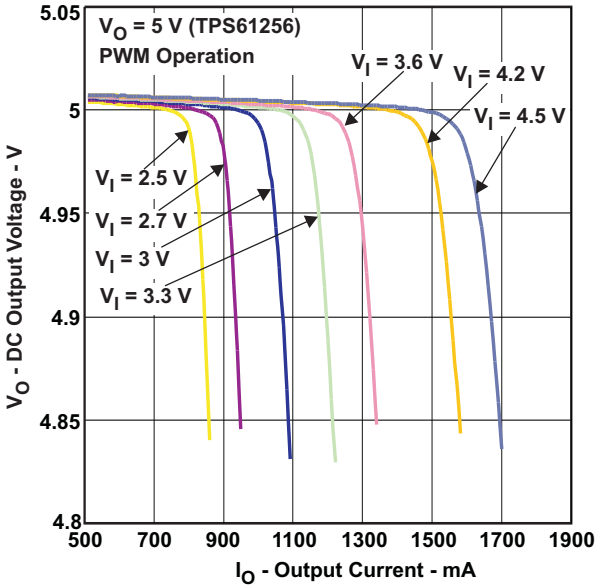


Figure 11.

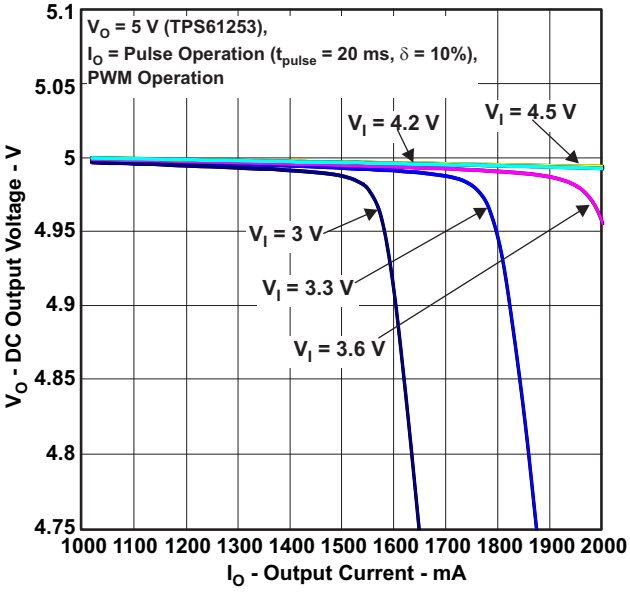


Figure 12.

Copyright © 2011–2012, Texas Instruments Incorporated

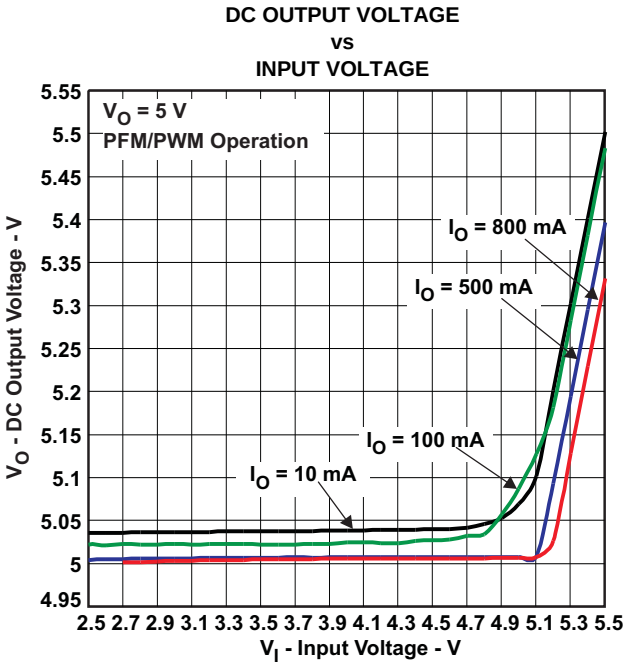


Figure 13.

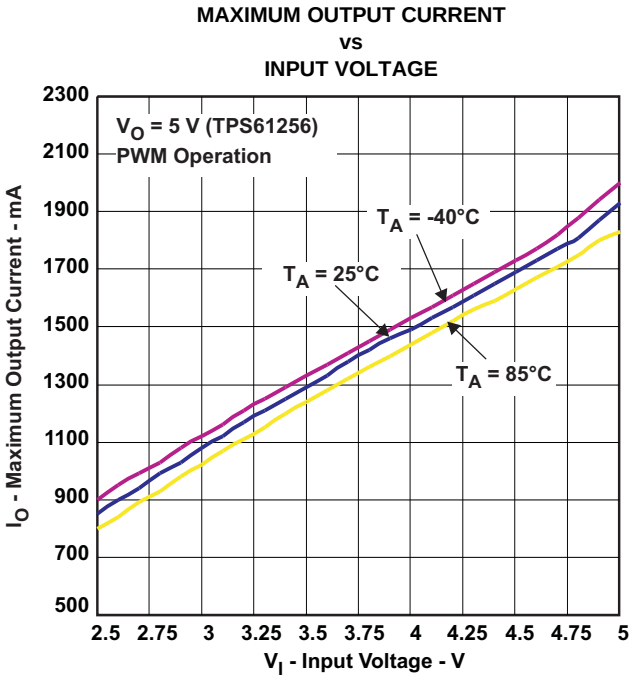


Figure 14.

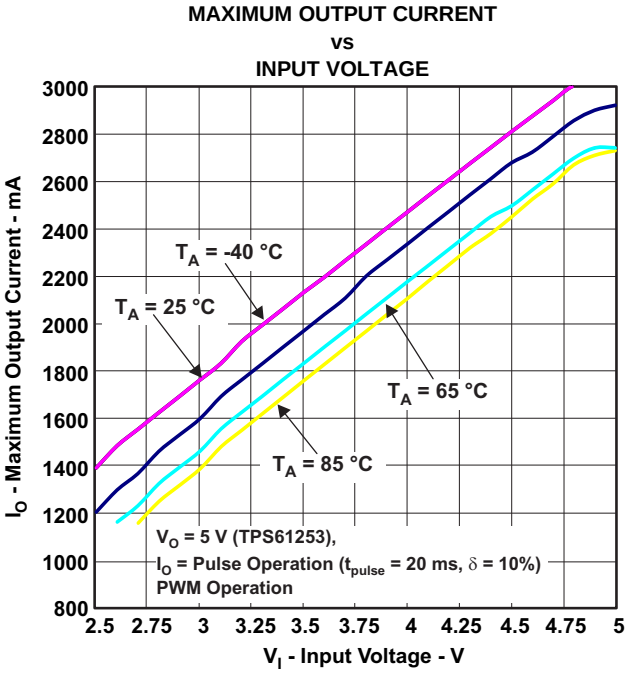


Figure 15.

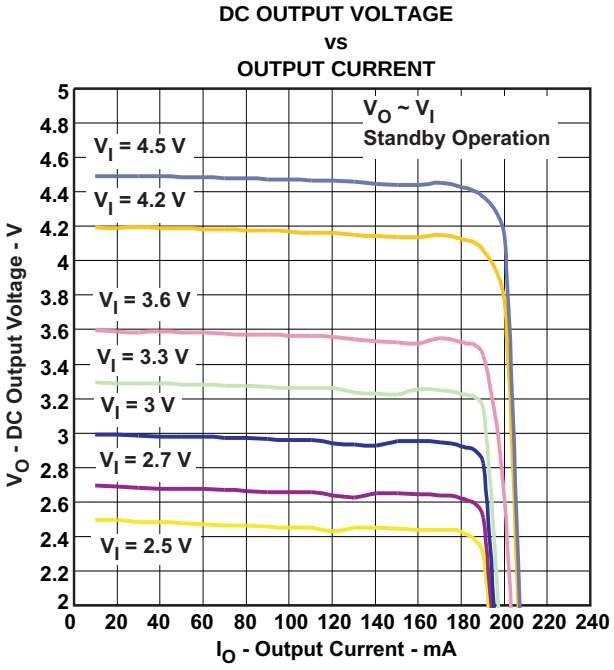


Figure 16.

Copyright © 2011–2012, Texas Instruments Incorporated

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE
vs
OUTPUT CURRENT

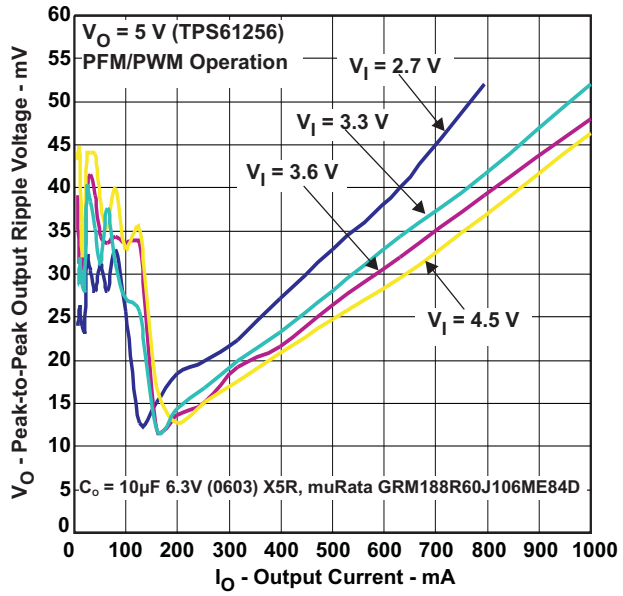


Figure 17.

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE
vs
OUTPUT CURRENT

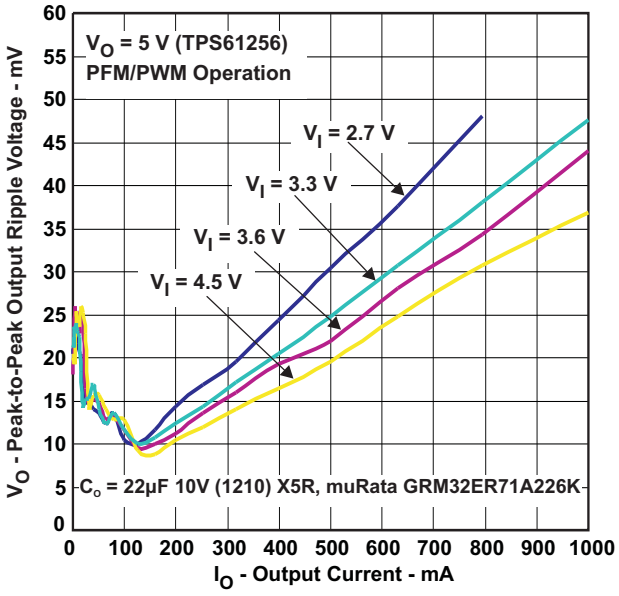


Figure 18.

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE
vs
OUTPUT CURRENT

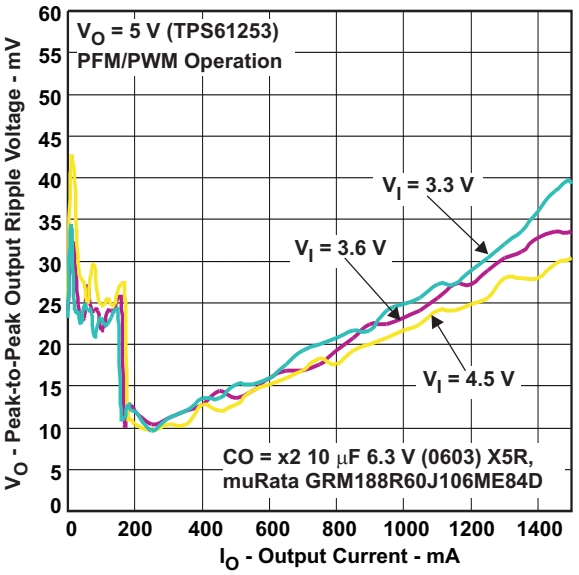


Figure 19.

SUPPLY CURRENT
vs
INPUT VOLTAGE

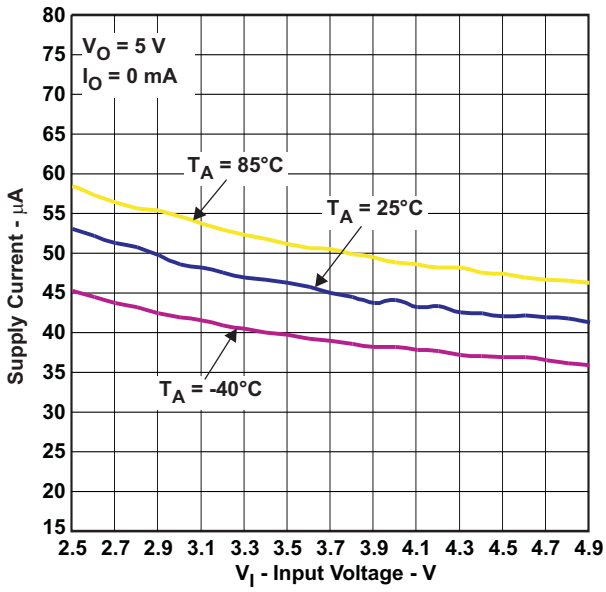


Figure 20.

Copyright © 2011–2012, Texas Instruments Incorporated

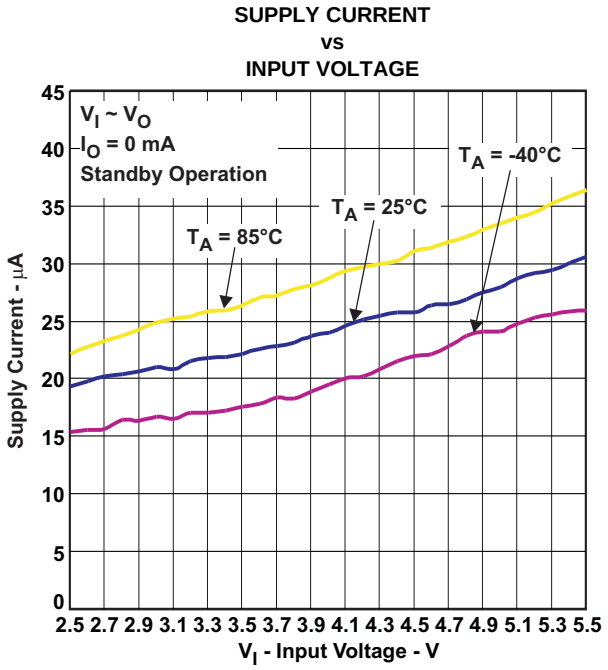


Figure 21.

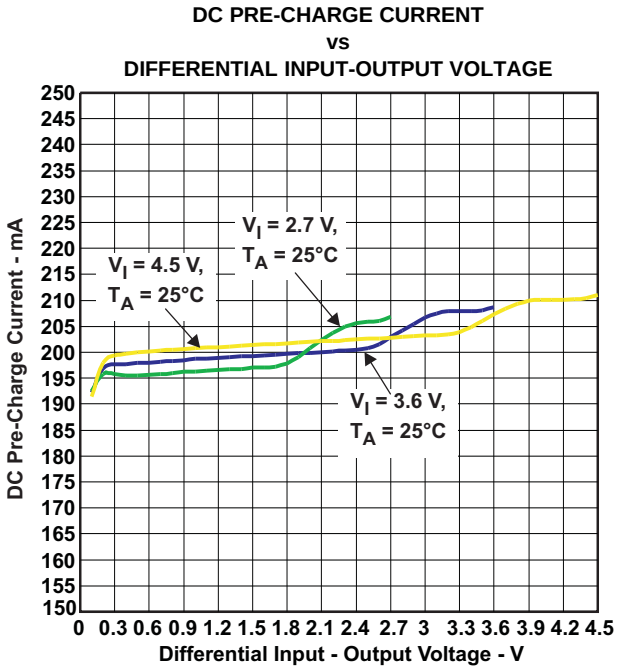


Figure 22.

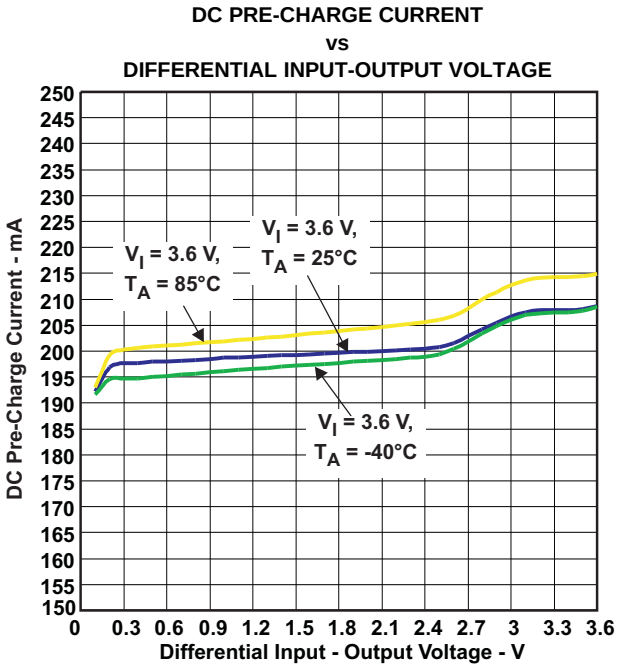


Figure 23.

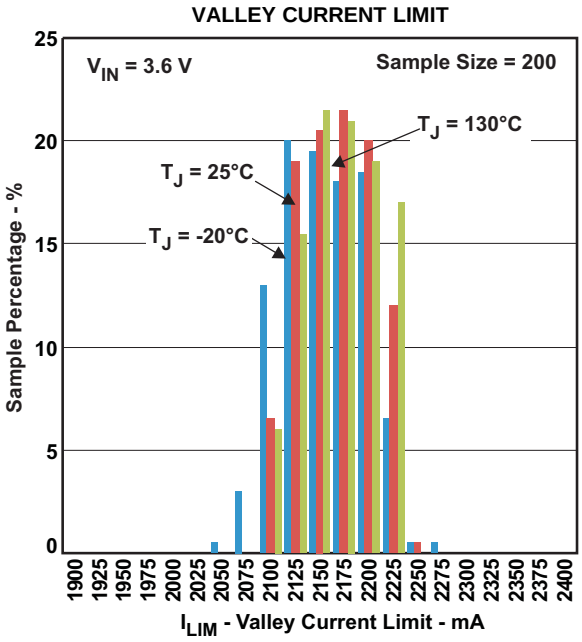


Figure 24.

Copyright © 2011–2012, Texas Instruments Incorporated

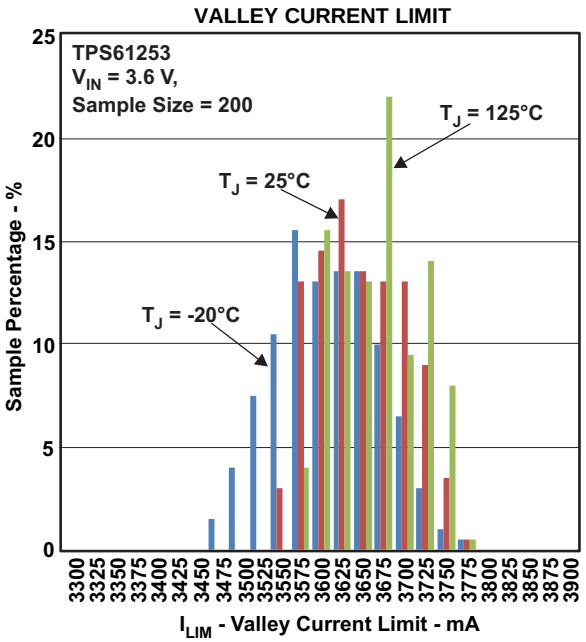


Figure 25.

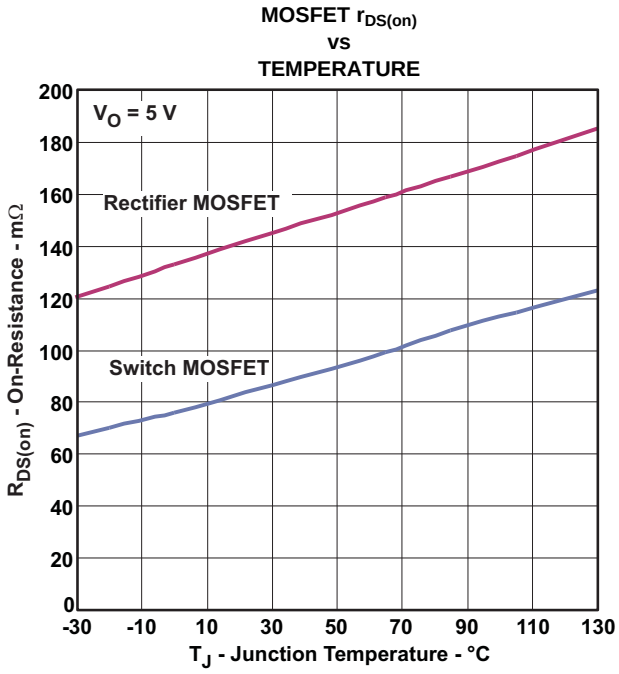


Figure 26.

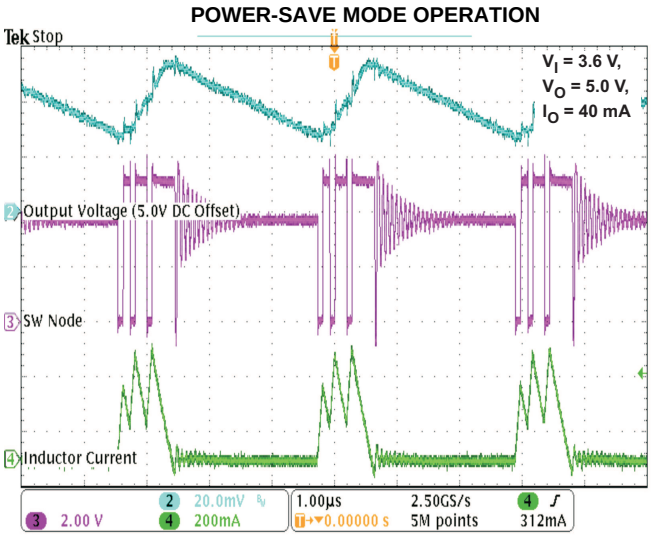


Figure 27.

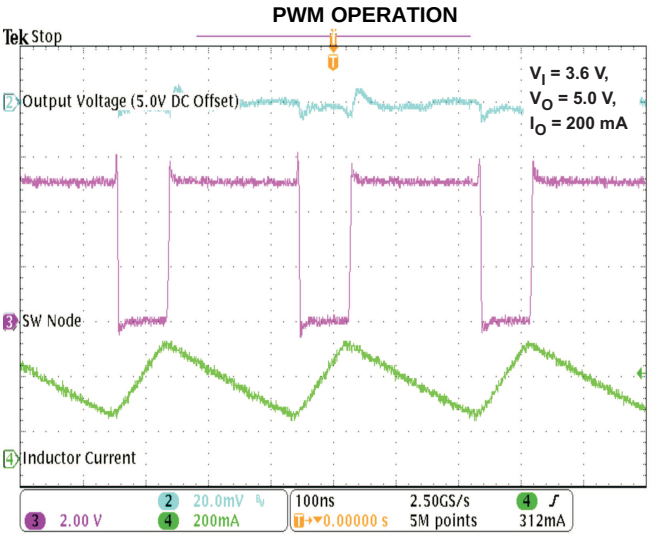


Figure 28.

Copyright © 2011–2012, Texas Instruments Incorporated

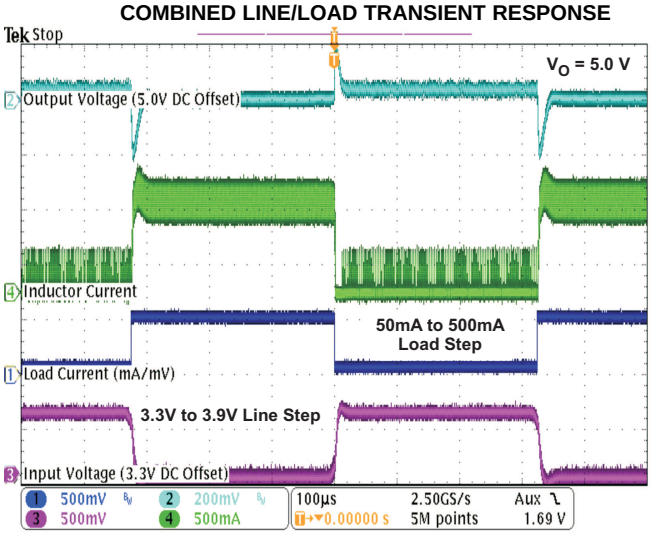


Figure 29.

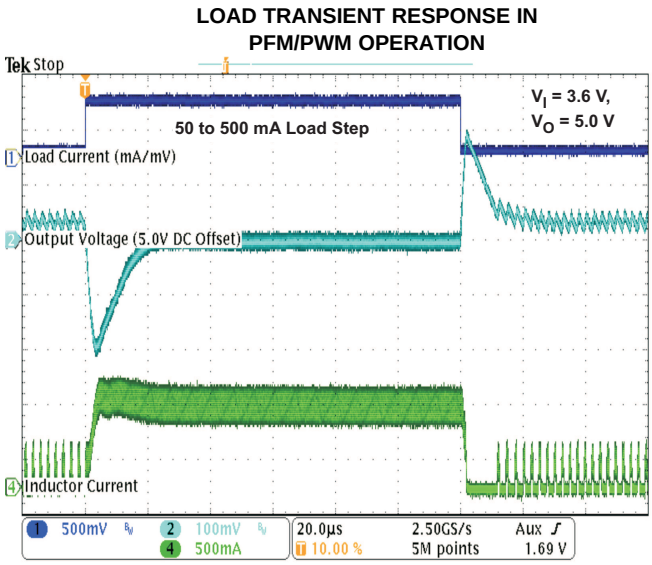


Figure 30.

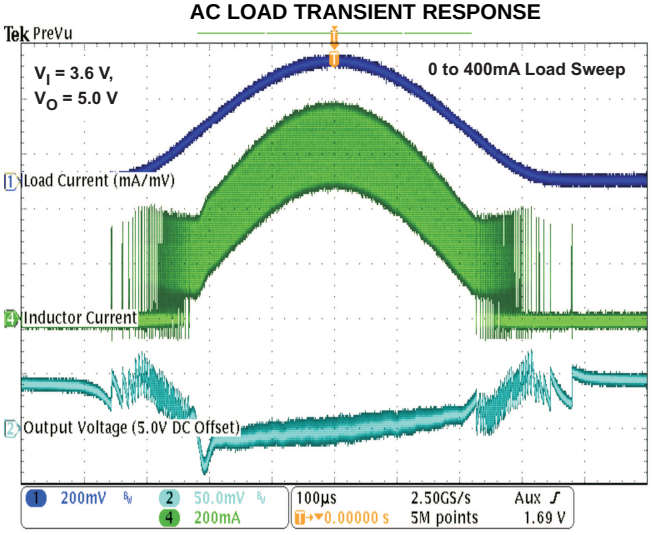


Figure 31.

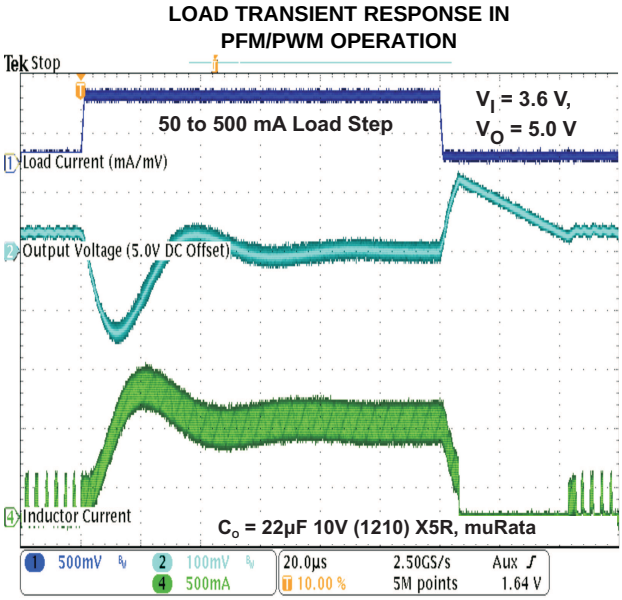


Figure 32.

Copyright © 2011–2012, Texas Instruments Incorporated

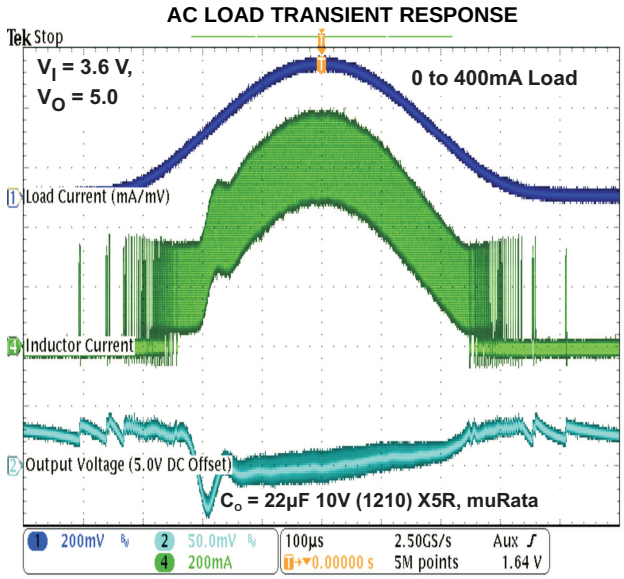


Figure 33.

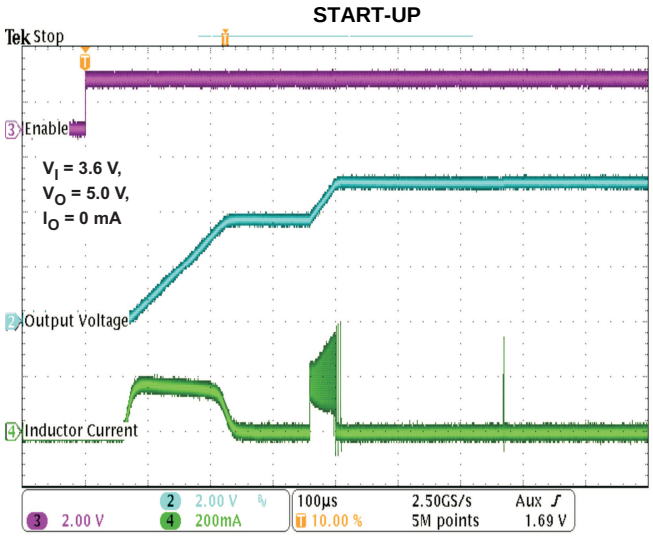


Figure 34.

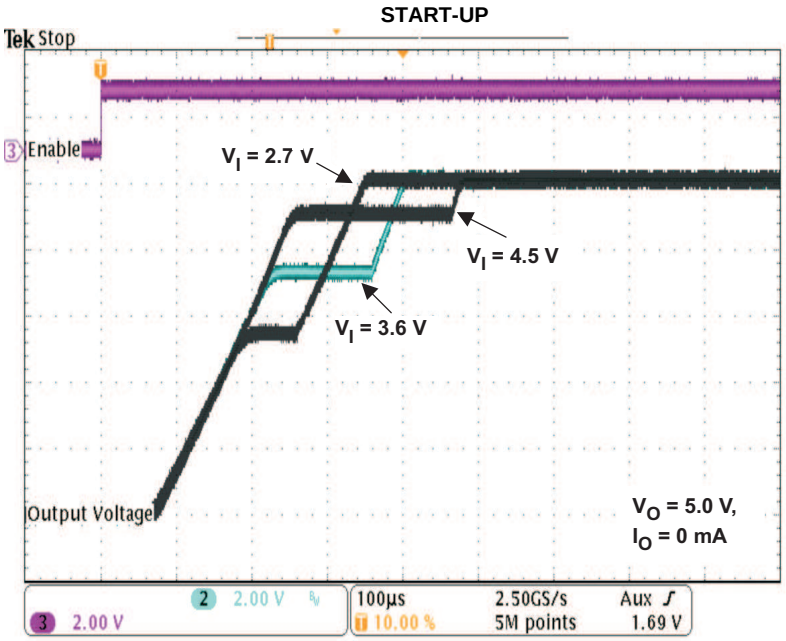


Figure 35.

Copyright © 2011–2012, Texas Instruments Incorporated

DETAILED DESCRIPTION

OPERATION

The TPS6125x synchronous step-up converter typically operates at a quasi-constant 3.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS6125x converter operates in power-save mode with pulse frequency modulation (PFM).

During PWM operation, the converter uses a novel quasi-constant on-time valley current mode control scheme to achieve excellent line/load regulation and allows the use of a small ceramic inductor and capacitors. Based on the V_{IN}/V_{OUT} ratio, a simple circuit predicts the required on-time.

At the beginning of the switching cycle, the low-side N-MOS switch is turned-on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once the on-timer has expired, the rectifier is turned-on and the inductor current decays to a preset valley current threshold. Finally, the switching cycle repeats by setting the on timer again and activating the low-side N-MOS switch.

In general, a dc/dc step-up converter can only operate in "true" boost mode, i.e. the output “boosted” by a certain amount above the input voltage. The TPS6125x device operates differently as it can smoothly transition in and out of zero duty cycle operation. Therefore the output can be kept as close as possible to its regulation limits even though the converter is subject to an input voltage that tends to be excessive. In this operation mode, the output current capability of the regulator is limited to ca. 150mA. Refer to the typical characteristics section (DC Output Voltage vs. Input Voltage) for further details.

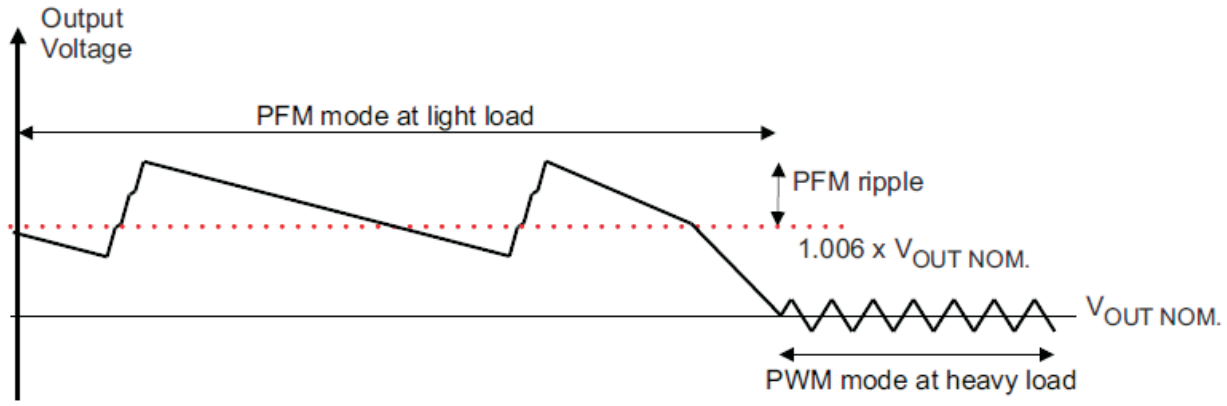
The current mode architecture with adaptive slope compensation provides excellent transient load response, requiring minimal output filtering. Internal soft-start and loop compensation simplifies the design process while minimizing the number of external components.

POWER-SAVE MODE

The TPS6125X integrates a power-save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage.

It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage.

The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.



Copyright © 2011–2012, Texas Instruments Incorporated

STANDBY MODE

The TPS6125x device is able to maintain its output biased at the input voltage level. In so called standby mode (EN = 0, BP = 1), the synchronous rectifier is current limited to ca. 150mA allowing an external load (e.g. audio amplifier) to be powered with a restricted supply. The output voltage is slightly reduced due to voltage drop across the rectifier MOSFET and the inductor DC resistance. The device consumes only a standby current of 22µA (typ).

Table 3. Operating Mode Control

OPERATING MODE	EN	BP
Shutdown, True Load Disconnect (SD)	0	0
Standby Mode, Output Pre-Biased (SM)	0	1
Boost Operating Mode (BST)	1	0
	1	1

CURRENT LIMIT OPERATION

The TPS6125x device employs a valley current limit sensing scheme. Current limit detection occurs during the off-time by sensing of the voltage drop across the synchronous rectifier.

The output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit (CL) operation, can be defined by Equation 1.

$$I_{OUT(CL)} = (1 - D) \cdot \left(I_{VALLEY} + \frac{1}{2} \Delta I_L\right) \quad (1)$$

The duty cycle (D) can be estimated by Equation 2

$$D = 1 - \frac{V_{IN} \cdot \eta}{V_{OUT}} \quad (2)$$

and the peak-to-peak current ripple (ΔI_L) is calculated by Equation 3

$$\Delta I_L = \frac{V_{IN}}{L} \cdot \frac{D}{f} \quad (3)$$

The output current, $I_{OUT(DC)}$, is the average of the rectifier ripple current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off-time is increased to allow the current to decrease to this threshold before the next on-time begins (so called frequency fold-back mechanism). When the current limit is reached the output voltage decreases during further load increase.

Figure 36 illustrates the inductor and rectifier current waveforms during current limit operation.

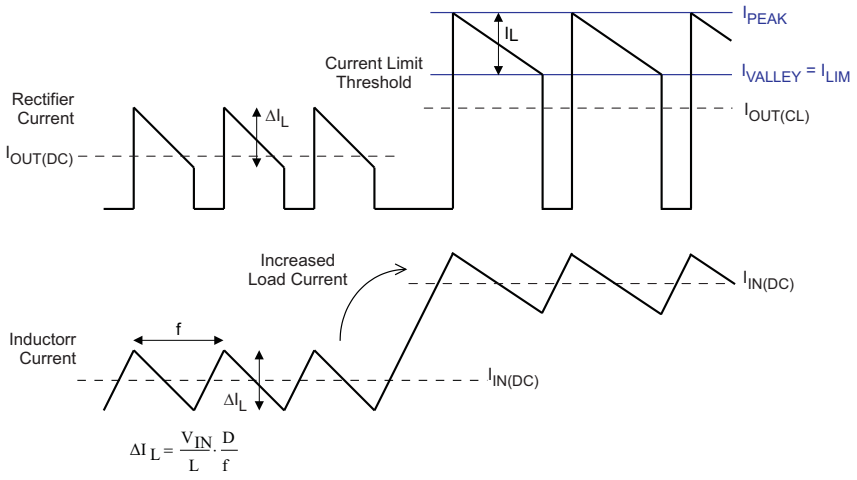


Figure 36. Inductor/Rectifier Currents in Current Limit Operation

Copyright © 2011–2012, Texas Instruments Incorporated

ENABLE

The TPS6125x device starts operation when EN is set high and starts up with the soft-start sequence. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN and BP pins low forces the device in shutdown, with a shutdown current of typically 1µA. In this mode, true load disconnect between the battery and load prevents current flow from V_{IN} to V_{OUT}, as well as reverse flow from V_{OUT} to V_{IN}.

Pulling the EN pin low and the BP pin high forces the device in standby mode, refer to the STANDBY MODE section for more details.

LOAD DISCONNECT AND REVERSE CURRENT PROTECTION

Regular boost converters do not disconnect the load from the input supply and therefore a connected battery will be discharge during shutdown. The advantage of TPS6125x is that this converter is disconnecting the output from the input of the power supply when it is disabled (so called true shutdown mode). In case of a connected battery it prevents it from being discharge during shutdown of the converter.

SOFTSTART

The TPS6125x device has an internal softstart circuit that limits the inrush current during start-up. The first step in the start-up cycle is the pre-charge phase. During pre-charge, the rectifying switch is turned on until the output capacitor is charged to a value close to the input voltage. The rectifying switch is current limited (approx. 200mA) during this phase. This mechanism is used to limit the output current under short-circuit condition.

Once the output capacitor has been biased to the input voltage, the converter starts switching. The soft-start system progressively increases the on-time as a function of the input-to-output voltage ratio. As soon as the output voltage is reached, the regulation loop takes control and full current operation is permitted.

UNDERVOLTAGE LOCKOUT

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and the battery from excessive discharge. It disables the output stage of the converter once the falling V_{IN} trips the under-voltage lockout threshold V_{UVLO} which is typically 2.0V. The device starts operation once the rising V_{IN} trips V_{UVLO} threshold plus its hysteresis of 100 mV at typ. 2.1V.

THERMAL REGULATION

The TPS6125x device contains a thermal regulation loop that monitors the die temperature during the pre-charge phase. If the die temperature rises to high values of about 110 °C, the device automatically reduces the current to prevent the die temperature from increasing further. Once the die temperature drops about 10 °C below the threshold, the device will automatically increase the current to the target value. This function also reduces the current during a short-circuit condition.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds 140°C (typ.) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned-off. When the junction temperature falls below the thermal shutdown minus its hysteresis, the device continuous the operation.

Copyright © 2011–2012, Texas Instruments Incorporated

APPLICATION INFORMATION

INDUCTOR SELECTION

A boost converter normally requires two main passive components for storing energy during the conversion, an inductor and an output capacitor are required. It is advisable to select an inductor with a saturation current rating higher than the possible peak current flowing through the power switches.

The inductor peak current varies as a function of the load, the input and output voltages and can be estimated using Equation 4.

$$I_{L(PEAK)} = \frac{V_{IN} \cdot D}{2 \cdot f \cdot L} + \frac{I_{OUT}}{(1-D) \cdot \eta} \quad \text{with} \quad D = 1 - \frac{V_{IN} \cdot \eta}{V_{OUT}} \tag{4}$$

Selecting an inductor with insufficient saturation performance can lead to excessive peak current in the converter. This could eventually harm the device and reduce it's reliability.

When selecting the inductor, as well as the inductance, parameters of importance are: maximum current rating, series resistance, and operating temperature. The inductor DC current rating should be greater (by some margin) than the maximum input average current, refer to Equation 5 and CURRENT LIMIT OPERATION section for more details.

$$I_{L(DC)} = \frac{V_{OUT}}{V_{IN}} \cdot \frac{1}{\eta} \cdot I_{OUT} \tag{5}$$

The TPS6125x series of step-up converters have been optimized to operate with a effective inductance in the range of 0.7µH to 2.9µH and with output capacitors in the range of 10µF to 47µF. The internal compensation is optimized for an output filter of L = 1µH and C_O = 10µF. Larger or smaller inductor values can be used to optimize the performance of the device for specific operating conditions. For more details, see the CHECKING LOOP STABILITY section.

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance, $R_{(DC)}$, and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS6125x converters.

Table 4. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS (in mm)
HITACHI METALS	KSLI-322512BL1-1R0	3.2 x 2.5 x 1.2 max. height
MURATA	LQM32PN1R0MG0	3.2 x 2.5 x 1.0 max. height
	LQM2HPN1R0MG0	2.5 x 2.0 x 1.0 max. height
TOKO	DFE322512C-1R0	3.2 x 2.5 x 1.2 max. height

Copyright © 2011–2012, Texas Instruments Incorporated

OUTPUT CAPACITOR

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is highly recommended. This small capacitor should be placed as close as possible to the V_{OUT} and GND pins of the IC. To get an estimate of the recommended minimum output capacitance, Equation 6 can be used.

$$C_{MIN} = \frac{I_{OUT} \cdot (V_{OUT} - V_{IN})}{f \cdot \Delta V \cdot V_{OUT}} \quad (6)$$

Where f is the switching frequency which is 3.5MHz (typ.) and ΔV is the maximum allowed output ripple.

With a chosen ripple voltage of 20mV, a minimum effective capacitance of 9µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 7

$$V_{ESR} = I_{OUT} \cdot R_{ESR} \quad (7)$$

An MLCC capacitor with twice the value of the calculated minimum should be used due to DC bias effects. This is required to maintain control loop stability. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. There are no additional requirements regarding minimum ESR. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients but the total output capacitance value should not exceed ca. 50µF.

DC bias effect: high cap. ceramic capacitors exhibit DC bias effects, which have a strong influence on the device's effective capacitance. Therefore the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and it's effective capacitance. For instance, a 10µF X5R 6.3V 0603 MLCC capacitor would typically show an effective capacitance of less than 4µF (under 5V bias condition, high temperature).

In applications featuring high pulsed load currents (e.g. TPS61253 based solution) it is recommended to run the converter with a reasonable amount of effective output capacitance, for instance x2 10µF X5R 6.3V 0603 MLCC capacitors connected in parallel.

INPUT CAPACITOR

Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 4.7µF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_I and the power source lead to reduce ringing than can occur between the inductance of the power source leads and C_I.

Copyright © 2011–2012, Texas Instruments Incorporated

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

LAYOUT CONSIDERATIONS

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to the ground pins of the IC.

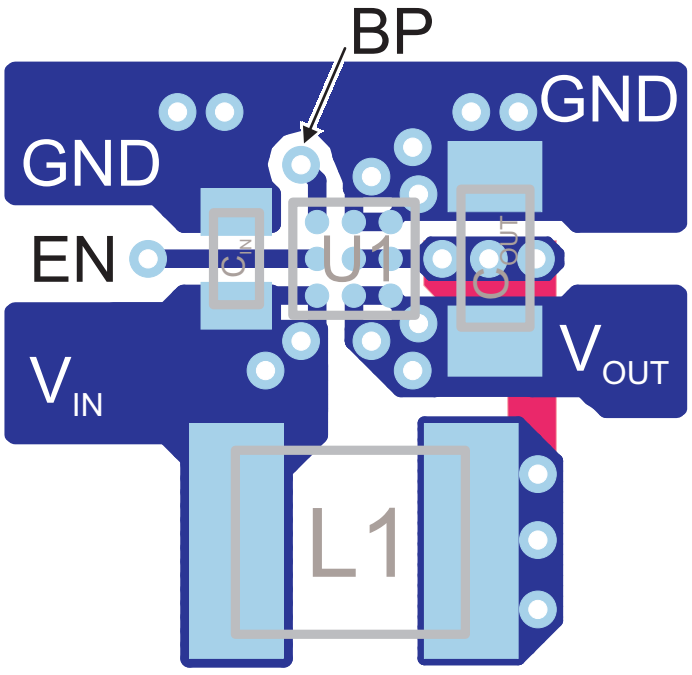


Figure 37. Suggested Layout (Top)

Copyright © 2011–2012, Texas Instruments Incorporated

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

As power demand in portable designs is more and more important, designers must figure the best trade-off between efficiency, power dissipation and solution size. Due to integration and miniaturization, junction temperature can increase significantly which could lead to bad application behaviors (i.e. premature thermal shutdown or worst case reduce device reliability).

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists (e.g. TPS61253 or TPS61259 based solutions), special care must be paid to thermal dissipation issues in board design. The device operating junction temperature (T_J) should be kept below 125°C.

Copyright © 2011–2012, Texas Instruments Incorporated

TYPICAL APPLICATION

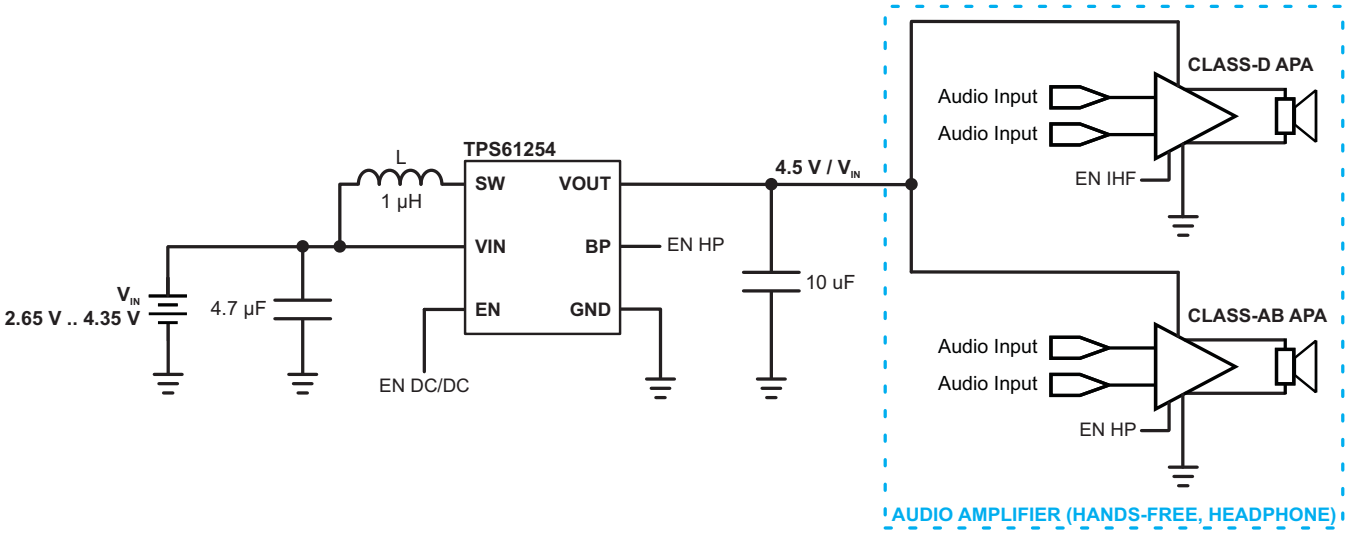


Figure 38. Combined Audio Amplifier Power Supply

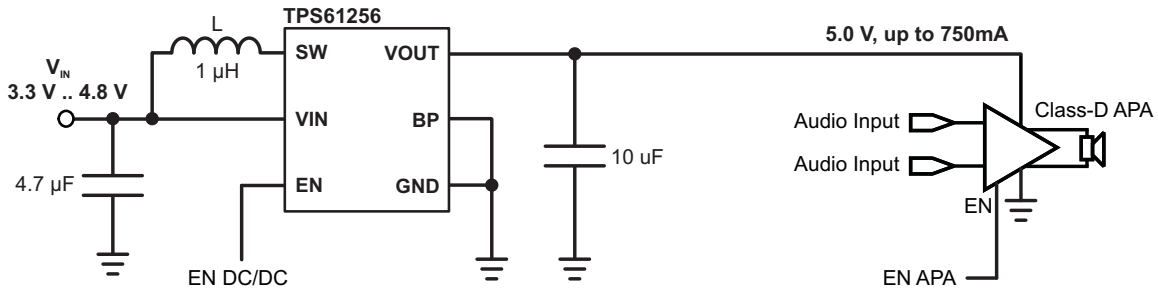


Figure 39. "Boosted" Audio Power Supply

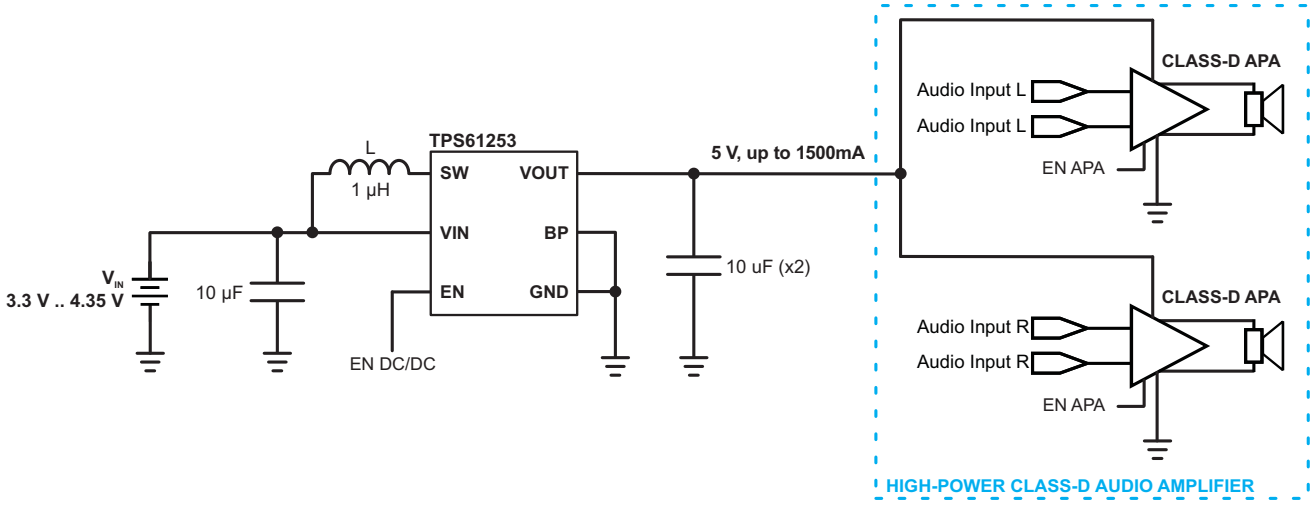


Figure 40. "Boosted" Stereo Audio Power Supply

Copyright © 2011–2012, Texas Instruments Incorporated

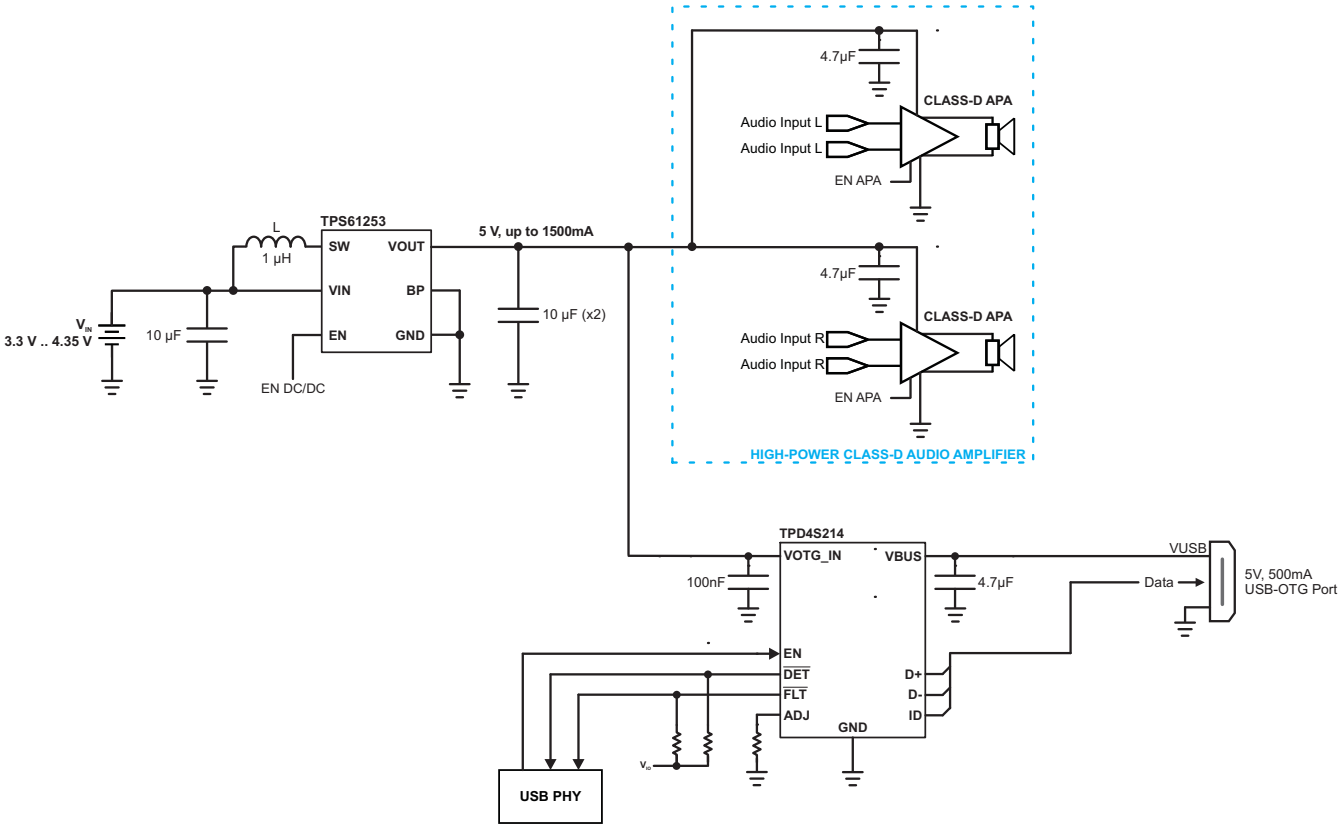


Figure 41. Single Cell Li-Ion Power Solution for Tablet PCs featuring "Boosted" Audio Power Supply and USB-OTG I/F

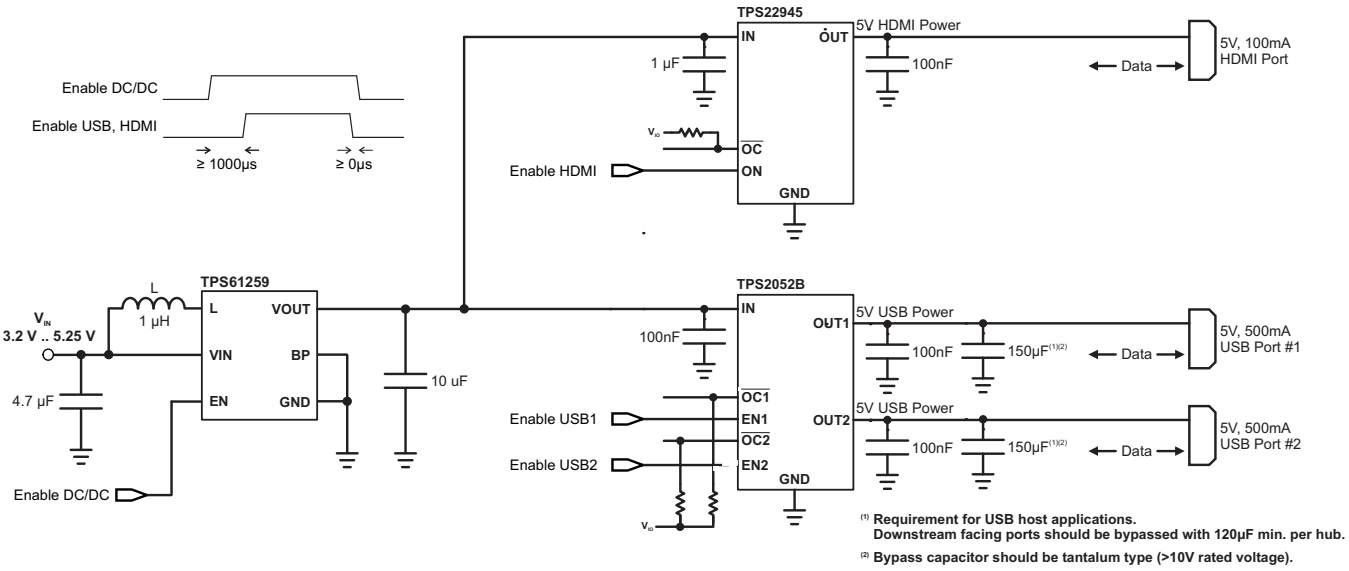
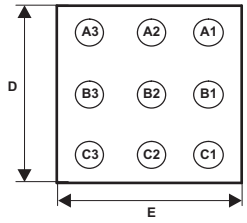


Figure 42. Single Cell Li-Ion Power Solution for Tablet PCs featuring x2 USB Host Ports, HDMI I/F

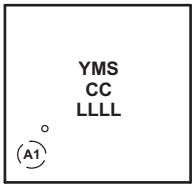
Copyright © 2011–2012, Texas Instruments Incorporated

PACKAGE SUMMARY

CHIP SCALE PACKAGE (BOTTOM VIEW)



CHIP SCALE PACKAGE (TOP VIEW)



Code:

- YM - 2 digit date code
- S - assembly site code
- CC - chip code (see ordering table)
- LLLL - lot trace code

PACKAGE DIMENSIONS

The dimensions for the YFF-9 package are shown in Table 5. See the package drawing at the end of this data sheet.

Table 5. YFF-9 Package Dimensions

Packaged Devices	D	E
TPS6125xYFF	1.206 ±0.03 mm	1.306 ±0.03 mm

Copyright © 2011–2012, Texas Instruments Incorporated

REVISION HISTORY

Note: Page numbers of current revision may differ from previous versions.

Changes from Original (September 2011) to Revision A **Page**

- Changed device TPS61256 to production status 2

Changes from Revision A (October 2011) to Revision B **Page**

- Added TPS61253 and TPS61258 to data sheet header as production devices 1
- Changed devices TPS61253 and TPS61258 to production status 2
- Changed graphic entity for Figure 5 9
- Changed graphic entity for Figure 12 10
- Changed graphic entity for Figure 15 11
- Changed graphic entity for Figure 25 14

Changes from Revision B (May 2012) to Revision C **Page**

- Added TPS61259 to data sheet header as production device 1
- Changed device TPS61259 to production status 2

Copyright © 2011–2012, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61253YFFR	ACTIVE	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SBF	Samples
TPS61253YFFT	ACTIVE	DSBGA	YFF	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SBF	Samples
TPS61254YFFR	ACTIVE	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	QWR	Samples
TPS61254YFFT	ACTIVE	DSBGA	YFF	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	QWR	Samples
TPS61256YFFR	ACTIVE	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RAV	Samples
TPS61256YFFT	ACTIVE	DSBGA	YFF	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RAV	Samples
TPS61258YFFR	ACTIVE	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SAZ	Samples
TPS61258YFFT	ACTIVE	DSBGA	YFF	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SAZ	Samples
TPS61259YFFR	ACTIVE	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SAY	Samples
TPS61259YFFT	ACTIVE	DSBGA	YFF	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SAY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

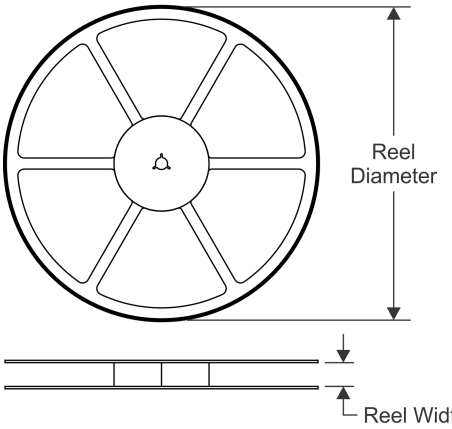
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

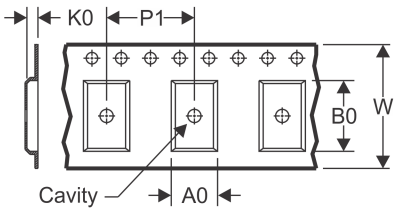
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

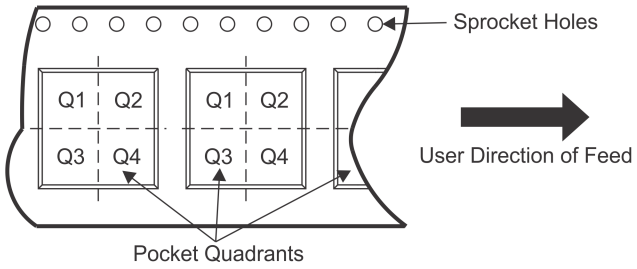


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

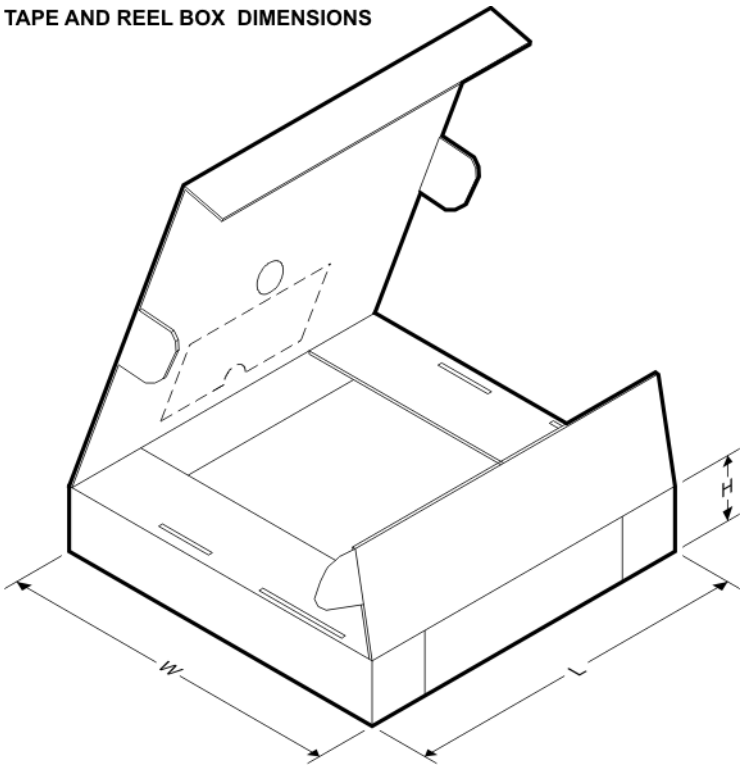
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61253YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	4.0	8.0	Q1
TPS61253YFFT	DSBGA	YFF	9	250	180.0	8.4	1.41	1.31	0.69	4.0	8.0	Q1
TPS61254YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	4.0	8.0	Q1
TPS61254YFFT	DSBGA	YFF	9	250	180.0	8.4	1.41	1.31	0.69	4.0	8.0	Q1
TPS61256YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	4.0	8.0	Q1
TPS61256YFFT	DSBGA	YFF	9	250	180.0	8.4	1.41	1.31	0.69	4.0	8.0	Q1
TPS61258YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	4.0	8.0	Q1
TPS61258YFFT	DSBGA	YFF	9	250	180.0	8.4	1.41	1.31	0.69	4.0	8.0	Q1
TPS61259YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	4.0	8.0	Q1
TPS61259YFFT	DSBGA	YFF	9	250	180.0	8.4	1.41	1.31	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

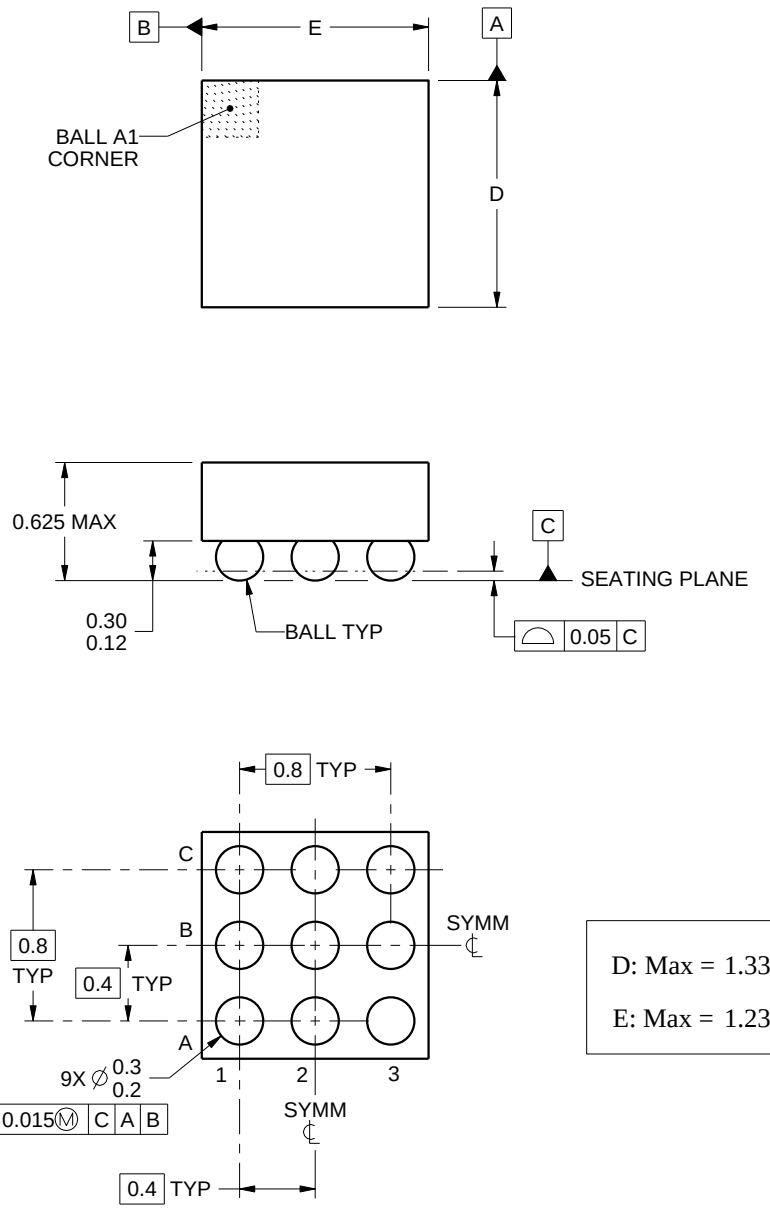
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61253YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61253YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0
TPS61254YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61254YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0
TPS61256YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61256YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0
TPS61258YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61258YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0
TPS61259YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61259YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



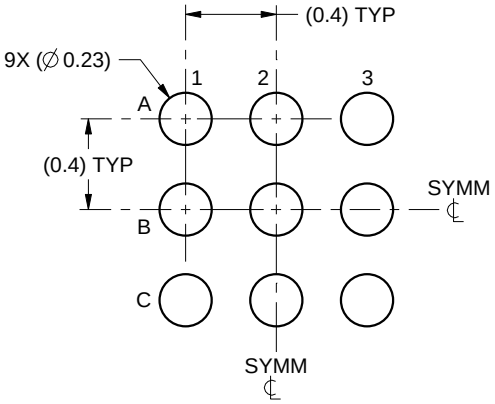
D: Max = 1.336 mm, Min =1.276 mm

E: Max = 1.236 mm, Min =1.176 mm

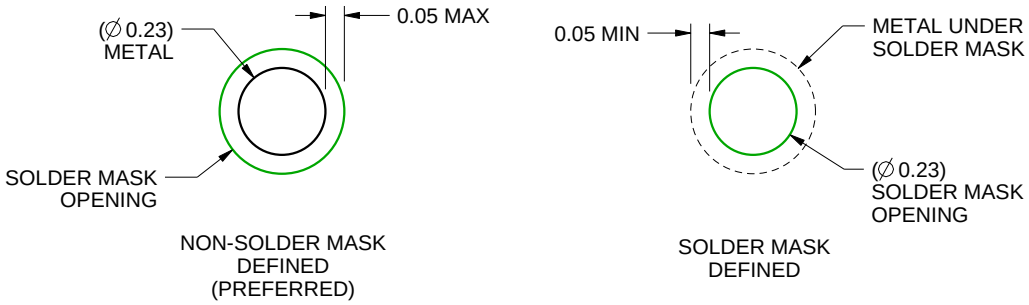
4219552/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

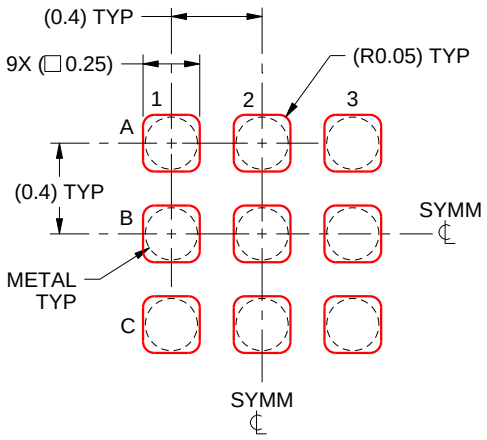


SOLDER MASK DETAILS
NOT TO SCALE

4219552/A 05/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219552/A 05/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022，德州仪器 (TI) 公司