

Crystal Oscillator / Clock Generator with optional SSC

FEATURES

- Part of a Family of Easy to use Clock Generator Devices With Optional SSC
- Crystal Oscillator With Integrated Crystal Capacitors, Selectable Output Frequency and Selectable SSC
- SSC Controllable via 2 External Pins
 - $\pm 0\%$, $\pm 0.5\%$, $\pm 1\%$, $\pm 2\%$ Center Spread
- Frequency Multiplication Selectable Between x1 or x4 With one External Control Pin
- Single 3.3V Device Power Supply
- Wide Temperature Range -40°C to 85°C
- Low space Consumption by 8 pin TSSOP Package

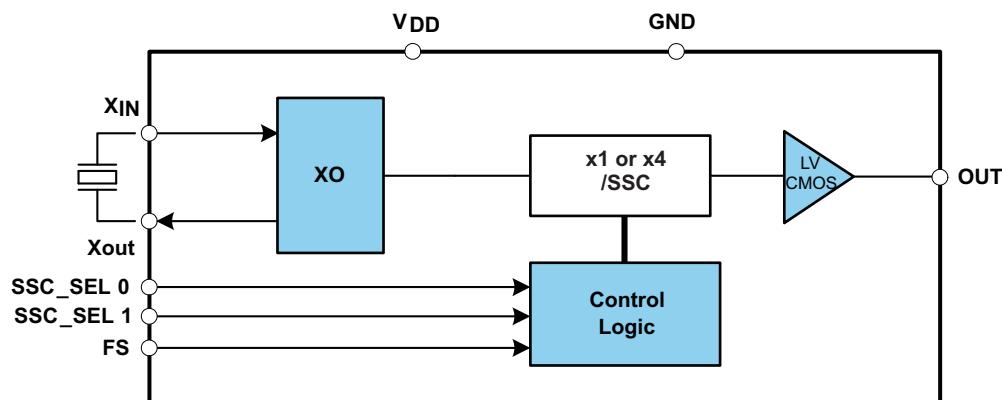
APPLICATIONS

- Consumer and Industrial Applications requiring Crystal Oscillator with the possibility of EMI reduction through Spread Spectrum Clocking

PACKAGE

XIN	1	8	XOUT
SSC_SEL 0	2	7	VDD
SSC_SEL 1	3	6	OUT
GND	4	5	FS
CDCS502			

BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The CDCS502 is a spread spectrum capable, fundamental mode crystal oscillator with selectable frequency multiplication.

It features an advanced gain controlled fundamental mode crystal oscillator stage with a built-in load capacitance of 10pF. This oscillator stage accepts crystals from 8MHz to 32MHz with an ESR of up to 180Ω. The stage can be used with crystals with power dissipation of 50μW and up.

The input signal is processed by a PLL, whose output frequency is either equal to the input frequency or multiplied by the factor of 4.

The PLL is also able to spread the clock signal by ±0%, ±0.5%, ±1% or ±2% centered around the output clock frequency with an triangular modulation.

By this, the device can generate output frequencies between 8MHz and 108MHz with or without SSC from a fundamental mode crystal.

In x1 Mode with an SSC amount of 0%, the device works as a standard crystal oscillator and does not make use of the built in PLL.

The CDCS502 operates in 3.3V environment.

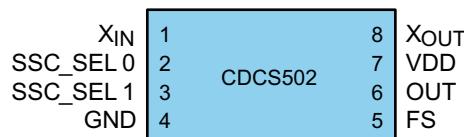
It is characterized for operation from -40°C to 85°C. It is offered in an 8 Pin TSSOP package.

FUNCTION TABLE

FS	SSC_SEL 0	SSC_SEL 1	SSC Amount	f _{OUT} /f _{IN}	f _{OUT} at f _{in} = 27 MHz
0	0	0	±0.00%	1	27 MHz ⁽¹⁾
0	0	1	±0.50%	1	27 MHz
0	1	0	±1.00%	1	27 MHz
0	1	1	±2.00%	1	27 MHz
1	0	0	±0.00%	4	108 MHz
1	0	1	±0.50%	4	108 MHz
1	1	0	±1.00%	4	108 MHz
1	1	1	±2.00%	4	108 MHz

(1) In this mode the signal from the crystal bypasses the internal PLL for maximum performance.

PACKAGE



PIN FUNCTIONS

SIGNAL	PIN	TYPE	DESCRIPTION
X _{IN}	1	I	Crystal Input
X _{OUT}	8	O	Crystal Output
OUT	6	O	LVCMS Clock Output
SSC_SEL 0, 1	2, 3	I	Spread Selection Pins, internal pull-up
FS	5	I	Frequency Multiplication Selection, internal pull-up
V _{DD}	7	Power	3.3V Power Supply
GND	4	Ground	Ground

PACKAGE THERMAL RESISTANCE FOR TSSOP (PW) PACKAGE⁽¹⁾

CDCV304PW 8-PIN TSSOP		THERMAL AIR FLOW (CFM)				UNIT
		0	150	250	500	
$R_{\theta JA}$	High K	149	142	138	132	°C/W
$R_{\theta JA}$	Low K	230	185	170	150	°C/W
$R_{\theta JC}$	High K	65				°C/W
$R_{\theta JC}$	High K	69				°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{DD}	Supply voltage range	-0.5 to 4.6	V
V_{IN}	Input voltage range	-0.5 to 4.6	V
V_{out}	Output voltage range	-0.5 to 4.6	V
I_{IN}	Input current ($V_I < 0$, $V_I > VDD$)	± 20	mA
I_{out}	Continuous output current	± 50	mA
T_{ST}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3.0	3.6		V
f_{IN}	Input Frequency	8	32		MHz
V_{IL}	Low level input voltage LVC MOS			0.3 VDD	V
V_{IH}	High level input voltage LVC MOS	0.7 VDD			V
V_I	Input Voltage threshold LVC MOS		0.5 VDD		V
C_L	Output Test Load LVC MOS			10	pF
I_{OH}/I_{OL}	Output Current			12	mA
T_A	Operating free-air temperature	-40	85		°C

RECOMMENDED CRYSTAL SPECIFICATIONS⁽¹⁾

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
f_{X-tal}	Crystal input frequency range	FS = 0	8	32	MHz
		FS = 1	8	27	
ESR	Effective series resistance ⁽²⁾			180	Ω
C_L	On-chip load capacitance at Xin and Xout		10		pF
T_{X-tal}	Crystal power dissipation		50		μW

(1) For further details on the crystal, see the crystal part in the Applications section
(2) With 5 pF crystal package parallel capacitance

DEVICE CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
IDD Device supply current	$f_{out} = 20$ MHz; FS = 0, no SSC		8		mA
	$f_{out} = 20$ MHz; FS = 0, SSC = 2%		18		
	$f_{out} = 70$ MHz; FS = 1, SSC = 2%		22		
f_{out} Output frequency	FS = 0	8	32	32	MHz
	FS = 1	32	108	108	MHz
I_{IH}	LVCMOS input current $V_I = VDD; VDD = 3.6$ V			10	μ A
I_{IL}	LVCMOS input current $V_I = 0$ V; VDD = 3.6 V			-10	μ A
V_{OH} LVCMOS high-level output voltage	$I_{OH} = -0.1$ mA	2.9			V
	$I_{OH} = -8$ mA	2.4			
	$I_{OH} = -12$ mA	2.2			
V_{OL} LVCMOS low-level output voltage	$I_{OL} = 0.1$ mA		0.1		V
	$I_{OL} = 8$ mA		0.5		
	$I_{OL} = 12$ mA		0.8		
$t_{jit(CC)}$	Cycle to cycle jitter $f_{out} = 108$ MHz; FS = 1, SSC = 1%, 10000 Cycles		100		ps
t_r/t_f	Rise and fall time	20%-80%	0.75		ns
O_{dc}	Output duty cycle	PLL active	45%	55%	
f_{MOD}	Modulation frequency		30		kHz

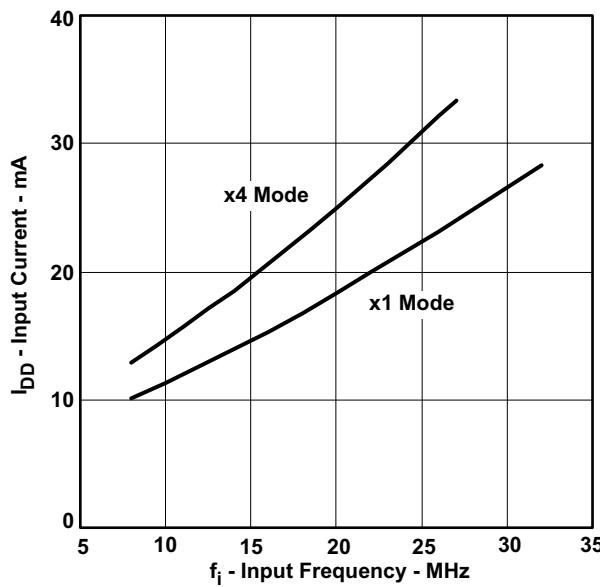


Figure 1. IDD vs Input Frequency, VCC = 3.3V, SSC = 2%

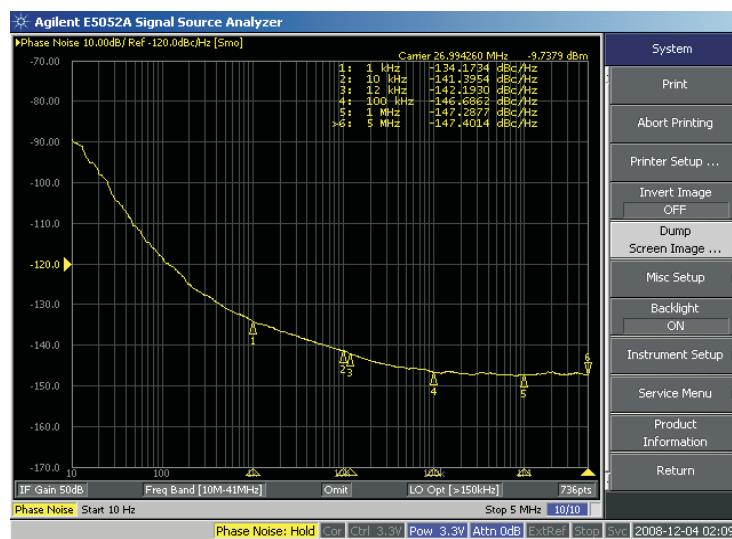


Figure 2. Phase Noise Plot, x1 Mode, 0% SSC, 27 MHz Crystal

APPLICATION INFORMATION

SELECTION OF A CRYSTAL

The CDCS502 requires a crystal with a frequency between 8 and 32 MHz (27MHz in x4 Mode). The crystal stage is designed with an internal load capacitance of 10pF for crystals with this shunt load capacitance. If a slightly bigger capacity then 10pF is needed, small external capacitors can be used to get to this value. This solution however might influence the power-up behavior of the crystal stage, so using a 10pF load capacitance crystal is highly recommended.

For further details on capacitive load calculation, see application report ([SCAA085](#)).

NOTE:

Even though the CDCS502 is characterized down to -40°C , a standard crystal is usually not rated for operation at this low temperature.

SSC MODULATION

The exact implementation of the SSC modulation plays a vital role for the EMI reduction. The CDCS502 uses a triangular modulation scheme implemented in a way that the modulation frequency depends on the VCO frequency of the internal PLL and the spread amount is independent from the VCO frequency.

The modulation frequency can be calculated by using one of the below formulas chosen by frequency multiplication mode.

$$\text{FS =0: } f_{\text{mod}} = f_{\text{IN}} / 708$$

$$\text{FS =1: } f_{\text{mod}} = f_{\text{IN}} / 620$$

PARAMETER MEASUREMENT INFORMATION

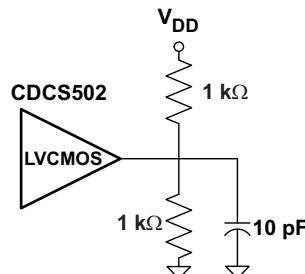


Figure 3. Test Load

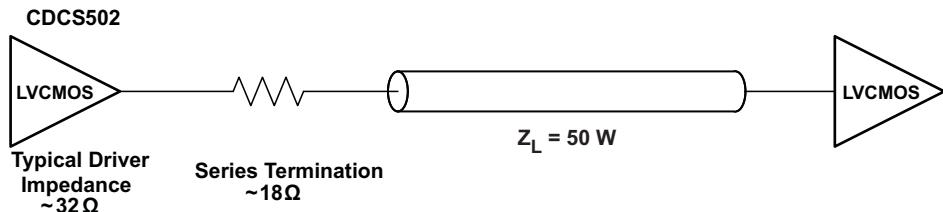


Figure 4. Test Load for 50-Ω Board Environment

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCS502PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CS502	Samples
CDCS502PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CS502	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



www.ti.com

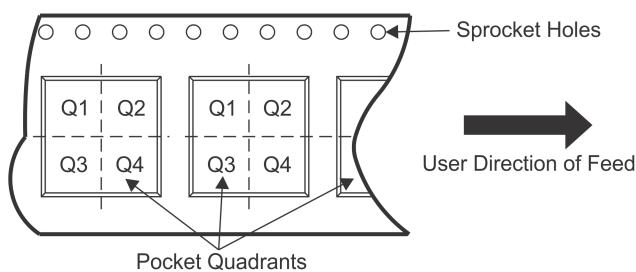
PACKAGE OPTION ADDENDUM

10-Dec-2020

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


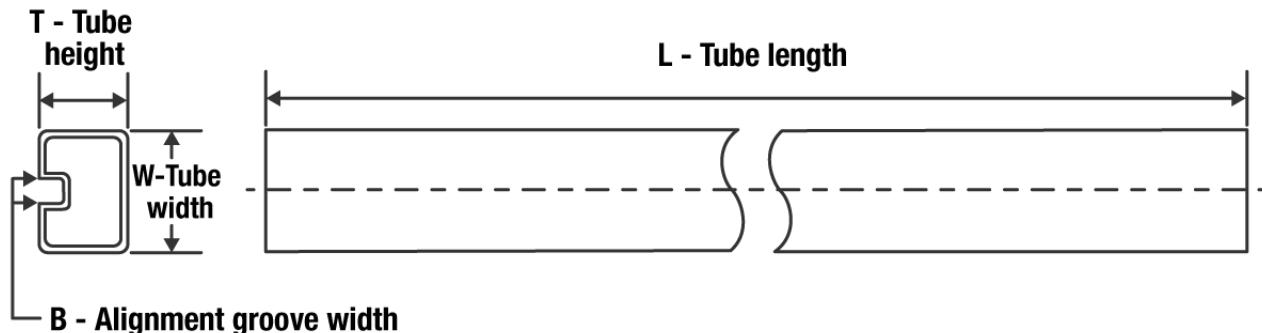
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCS502PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCS502PWR	TSSOP	PW	8	2000	853.0	449.0	35.0

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CDCS502PW	PW	TSSOP	8	150	530	10.2	3600	3.5

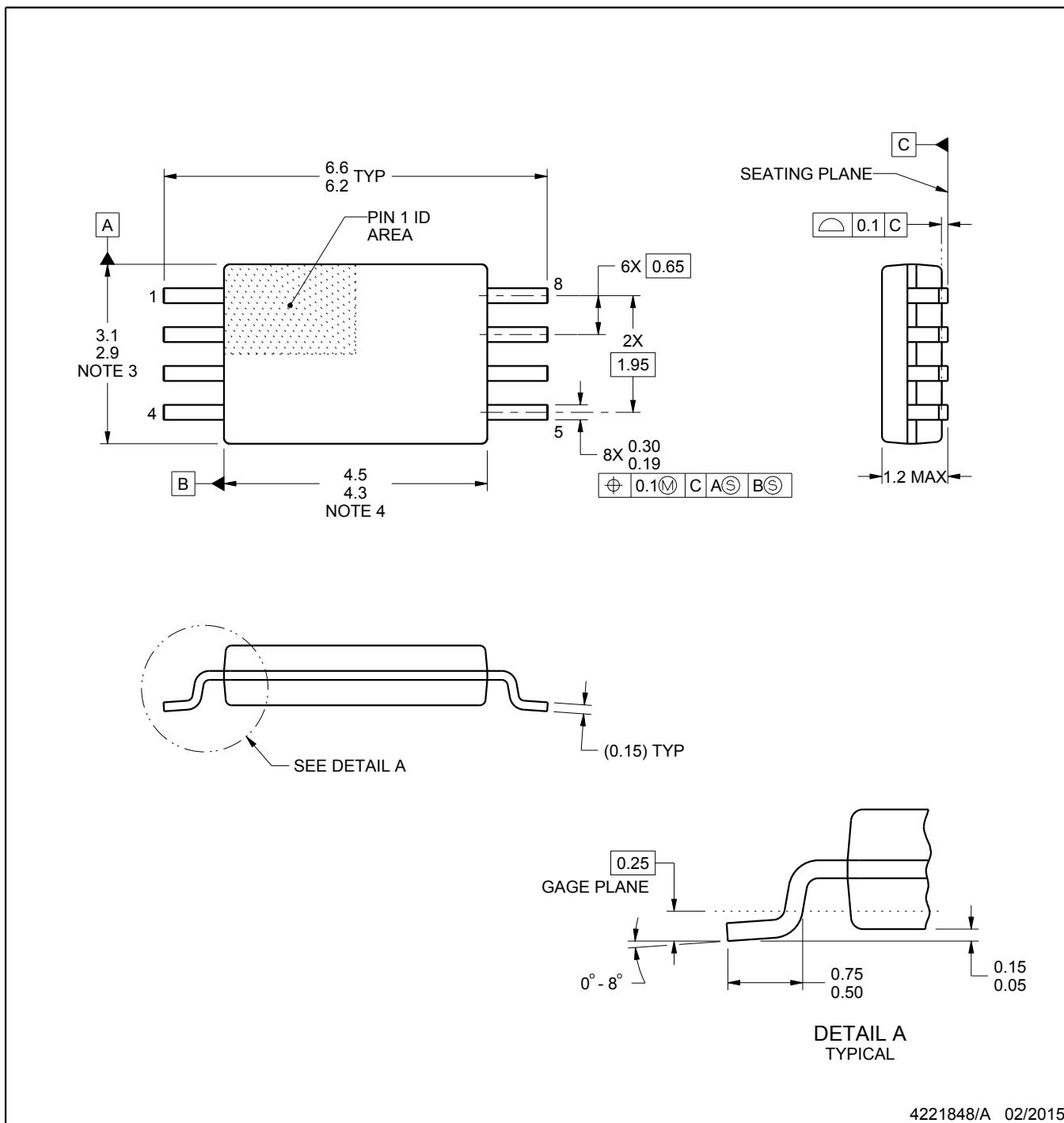
PACKAGE OUTLINE

PW0008A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

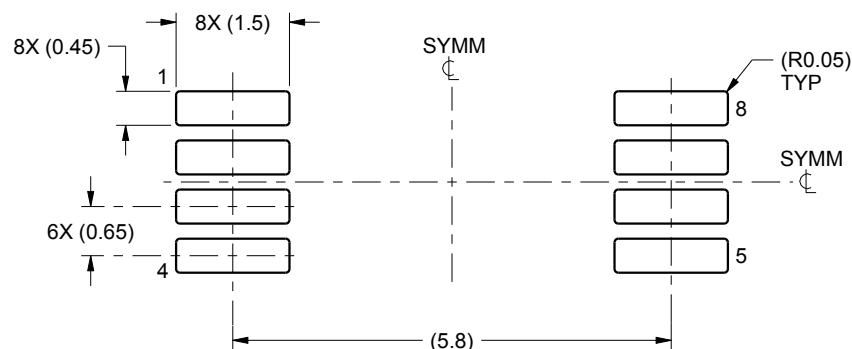
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

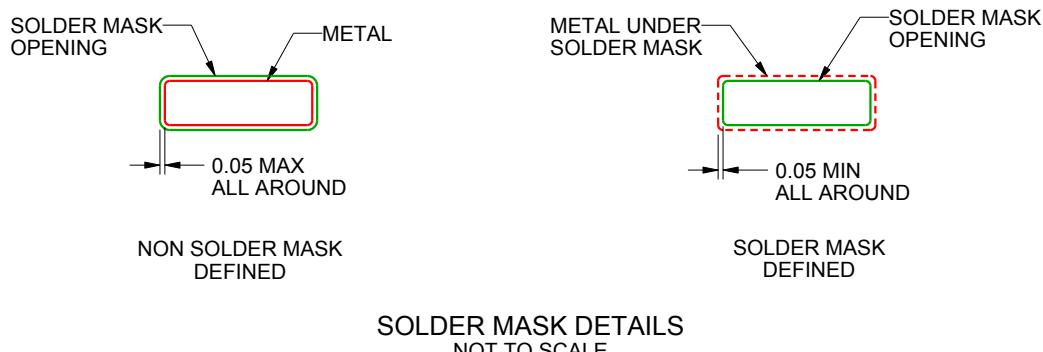
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



4221848/A 02/2015

NOTES: (continued)

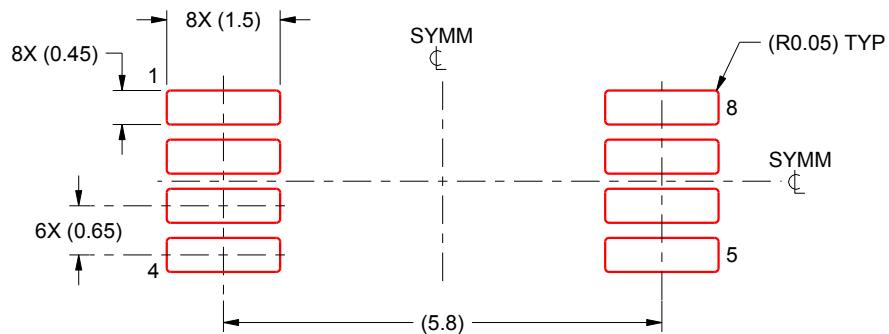
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated