

CMOS Dual 4-Stage Static Shift Register

With Serial Input/Parallel Output

High-Voltage Types (20-Volt Rating)

■ CD4015B consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015B package, or to more than 8 stages using additional CD4015B's is possible.

The CD4015B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic package (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Medium speed operation
- 12 MHz (typ.) clock rate at $V_{DD} - V_{SS} = 10$ V
- Fully static operation
- 8 master-slave flip-flops plus input and output buffering
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =

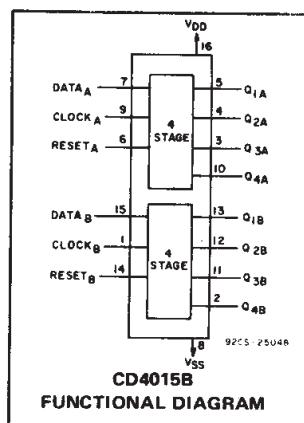
1 V at $V_{DD} = 5$ V
 2 V at $V_{DD} = 10$ V
 2.5 V at $V_{DD} = 15$ V

- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Serial-input/parallel-output data queueing
- Serial to parallel data conversion
- General-purpose register

CD4015B Types



TERMINAL DIAGRAM

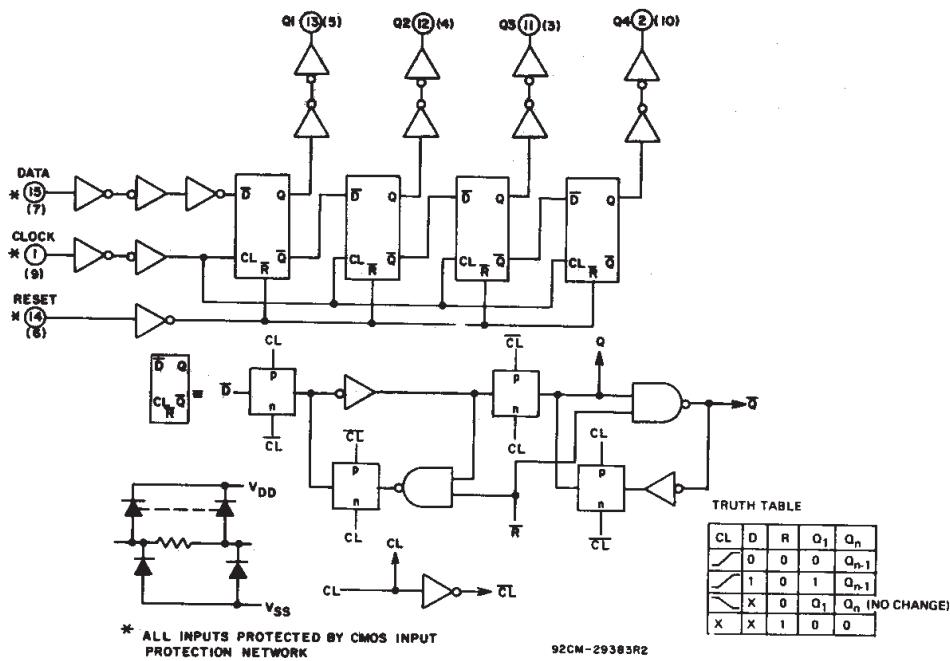
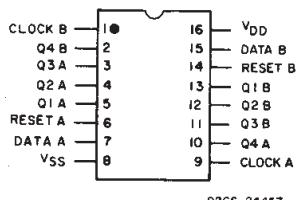


Fig. 1 - Logic diagram (1 register).

CD4015B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS

..... -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT

..... $\pm 10\text{mA}$

POWER DISSIPATION PER PACKAGE (P_D)

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55C to +125C

STORAGE TEMPERATURE RANGE (T_{STG}) -65C to +150C

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79\text{mm}$) from case for 10s max +265C

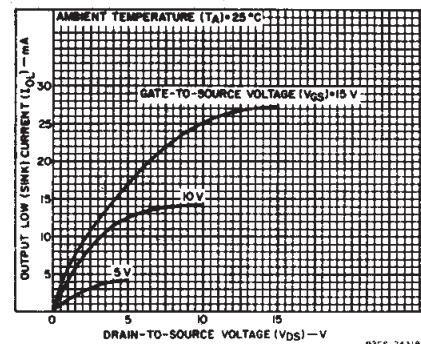


Fig. 2 — Typical output low (sink) current characteristics.

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A = \text{Full Package- Temperature Range}$)		3	18	V
Clock Pulse Width, t_{WCL}	5	180	—	ns
	10	80	—	
	15	50	—	
Clock Rise and Fall Time, t_{rCL}, t_{fCL}	5	—	15	\mu\text{s}
	10	—	6	
	15	—	2	
Clock Input Frequency, f_{CL}	5	—	3	MHz
	10	DC	6	
	15	—	8.5	
Data Setup Time, t_{SU}	5	70	—	ns
	10	40	—	
	15	30	—	
Reset Pulse Width, t_{WR}	5	200	—	ns
	10	80	—	
	15	60	—	

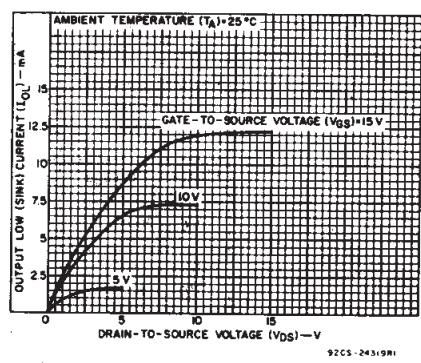


Fig. 3 — Minimum output low (sink) current characteristics.

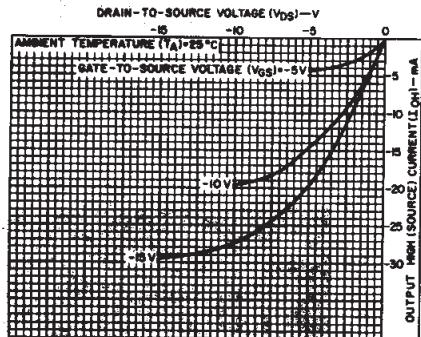


Fig. 4 — Typical output high (source) current characteristics.

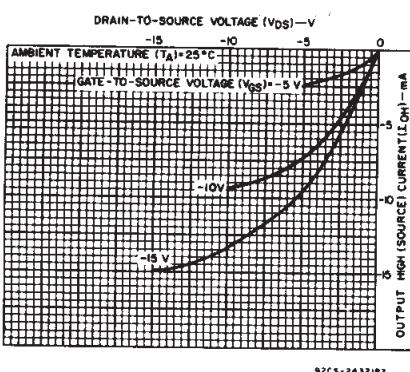


Fig. 5 — Minimum output high (source) current characteristics.

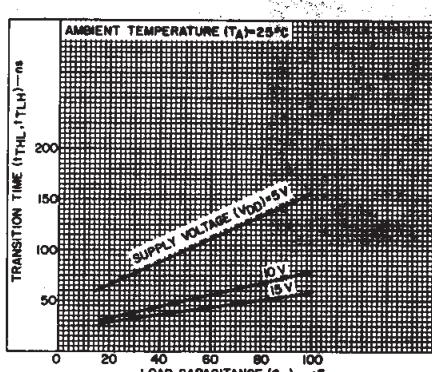


Fig. 6 — Typical transition time as a function of load capacitance.

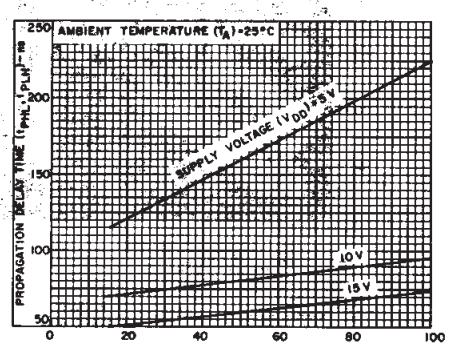
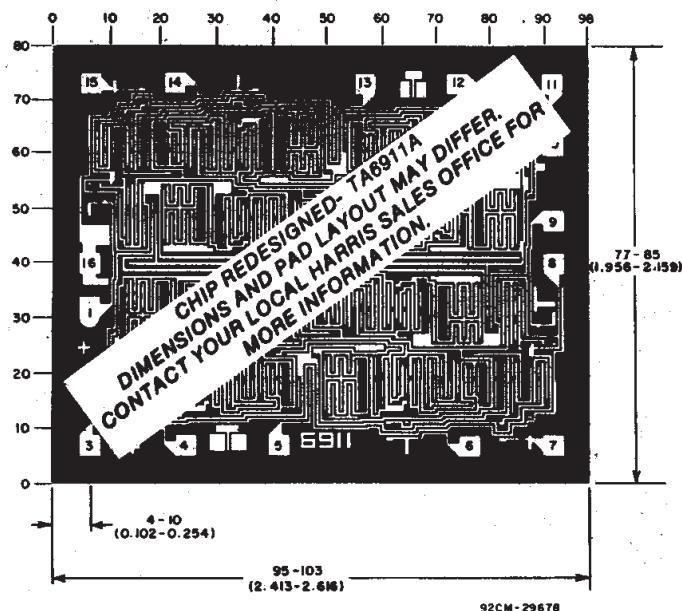


Fig. 7 — Typical propagation delay time as a function of load-capacitance.

CD4015B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS
				+25				Min.	Typ.	
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	Min.	Typ.	
Quiescent Device Current, I _{DD} Max.	-	0,5	5	5	5	150	150	-	0.04	5
	-	0,10	10	10	10	300	300	-	0.04	10
	-	0,15	15	20	20	600	600	-	0.04	20
	-	0,20	20	100	100	3000	3000	-	0.08	100
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-
	0,5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-
	1,5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-
	2,5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-
	9,5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-
	13,5	0,15	15	-4,2	-4	-2.8	-2.4	-3.4	-6.8	-
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5	0.05				-	0	0.05
	-	0,10	10	0.05				-	0	0.05
	-	0,15	15	0.05				-	0	0.05
Output Voltage: High-Level, V _{OH} Min.	-	0,5	5	4.95				4.95	5	-
	-	0,10	10	9.95				9.95	10	-
	-	0,15	15	14.95				14.95	15	-
Input Low Voltage, V _{IL} Max.	0,5, 4,5	-	5	1.5				-	-	1.5
	1,9	-	10	3				-	-	3
	1,5,13,5	-	15	4				-	-	4
Input High Voltage, V _{IH} Min.	0,5, 4,5	-	5	3.5				3.5	-	-
	1,9	-	10	7				7	-	-
	1,5,13,5	-	15	11				11	-	-
Input Current I _{IN} Max.	-	0,18	18	±0,1	±0,1	±1	±1	-	±10 ⁻⁵	±0,1



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Photograph of Chip Layout for CD4015B.

CD4015B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$, Input $t_i, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS			UNITS
		MIN.	TYP.	MAX.	
CLOCKED OPERATION					
Propagation Delay Time, T_{PHL}, T_{PLH}	5	—	160	320	ns
	10	—	80	160	
	15	—	60	120	
Transition Time, t_{THL}, t_{TLH}	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Minimum Clock Pulse Width, t_{wCL}	5	—	90	180	ns
	10	—	40	80	
	15	—	25	50	
Clock Rise and Fall Time, t_{rCL}, t_{fCL}	5	—	—	15	μs
	10	—	—	6	
	15	—	—	2	
Minimum Data Setup Time, t_{SU}	5	—	35	70	ns
	10	—	20	40	
	15	—	15	30	
Minimum Data Hold Time, t_{H}	5	—	—	0	ns
	10	—	—	0	
	15	—	—	0	
Maximum Clock Input Frequency, f_{CL}	5	3	6	—	MHz
	10	6	12	—	
	15	8.5	17	—	
Input Capacitance, C_{IN}	Any Input	—	5	7.5	pF
RESET OPERATION					
Propagation Delay Time, T_{PHL}, T_{PLH}	5	—	200	400	ns
	10	—	100	200	
	15	—	80	160	
Minimum Reset Pulse Width, t_{wR}	5	—	100	200	ns
	10	—	40	80	
	15	—	30	60	

*If more than one unit is cascaded t_{CL} should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

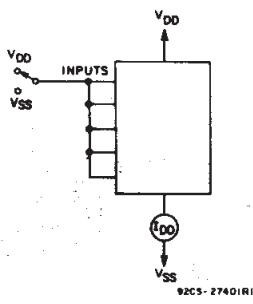


Fig. 10 – Quiescent device current test circuit.

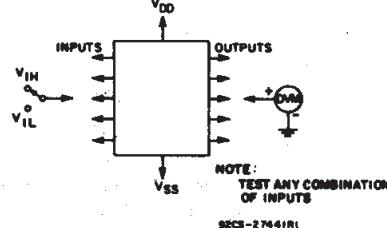


Fig. 11 – Input voltage test circuit.

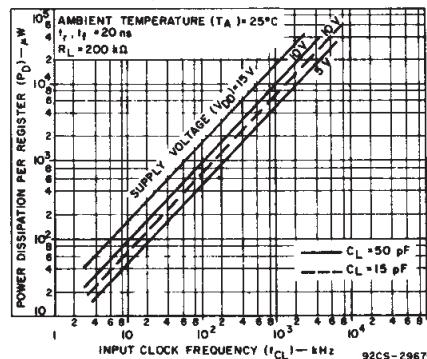


Fig. 8 – Typical power dissipation as a function of frequency.

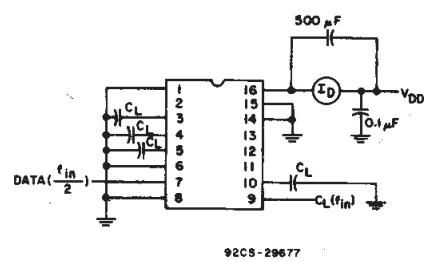


Fig. 9 – Power dissipation test circuit.

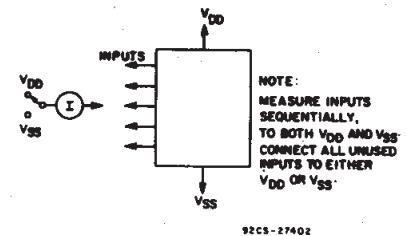


Fig. 12 – Input current test circuit.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4015BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4015BE	Samples
CD4015BEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4015BE	Samples
CD4015BF	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4015BF	Samples
CD4015BF3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4015BF3A	Samples
CD4015BM	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4015BM	Samples
CD4015BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4015BM	Samples
CD4015BMT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4015BM	Samples
CD4015BPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM015B	Samples
CD4015BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM015B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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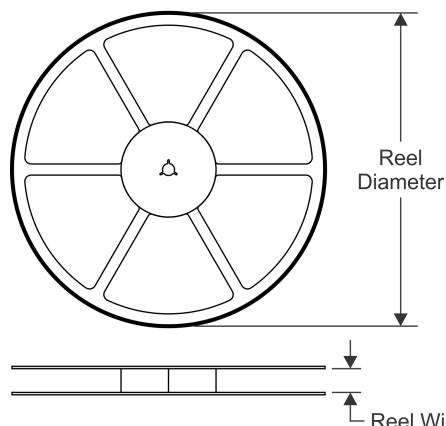
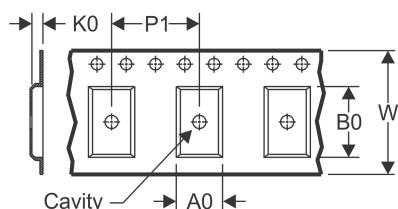
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4015B, CD4015B-MIL :

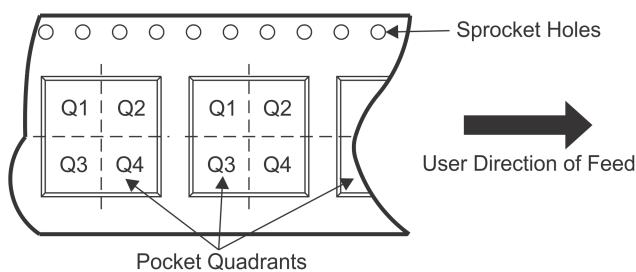
- Catalog : [CD4015B](#)
- Military : [CD4015B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


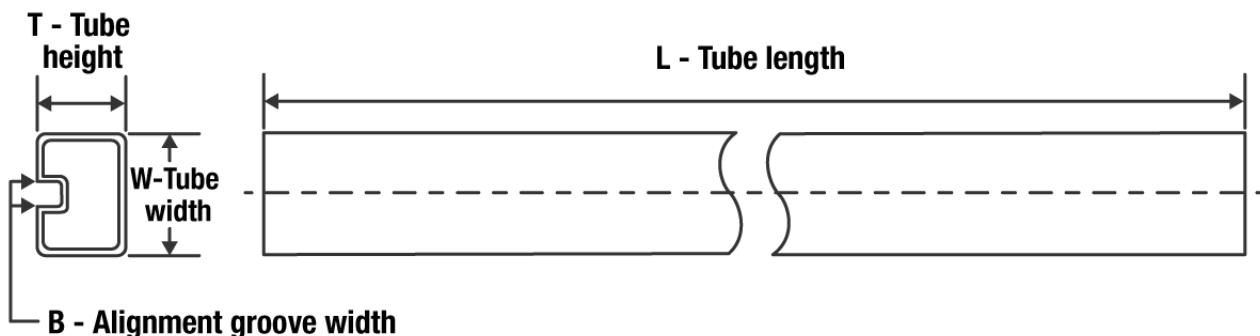
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4015BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4015BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4015BM96	SOIC	D	16	2500	340.5	336.1	32.0
CD4015BPWR	TSSOP	PW	16	2000	853.0	449.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4015BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4015BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4015BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4015BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4015BM	D	SOIC	16	40	507	8	3940	4.32
CD4015BPW	PW	TSSOP	16	90	530	10.2	3600	3.5

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

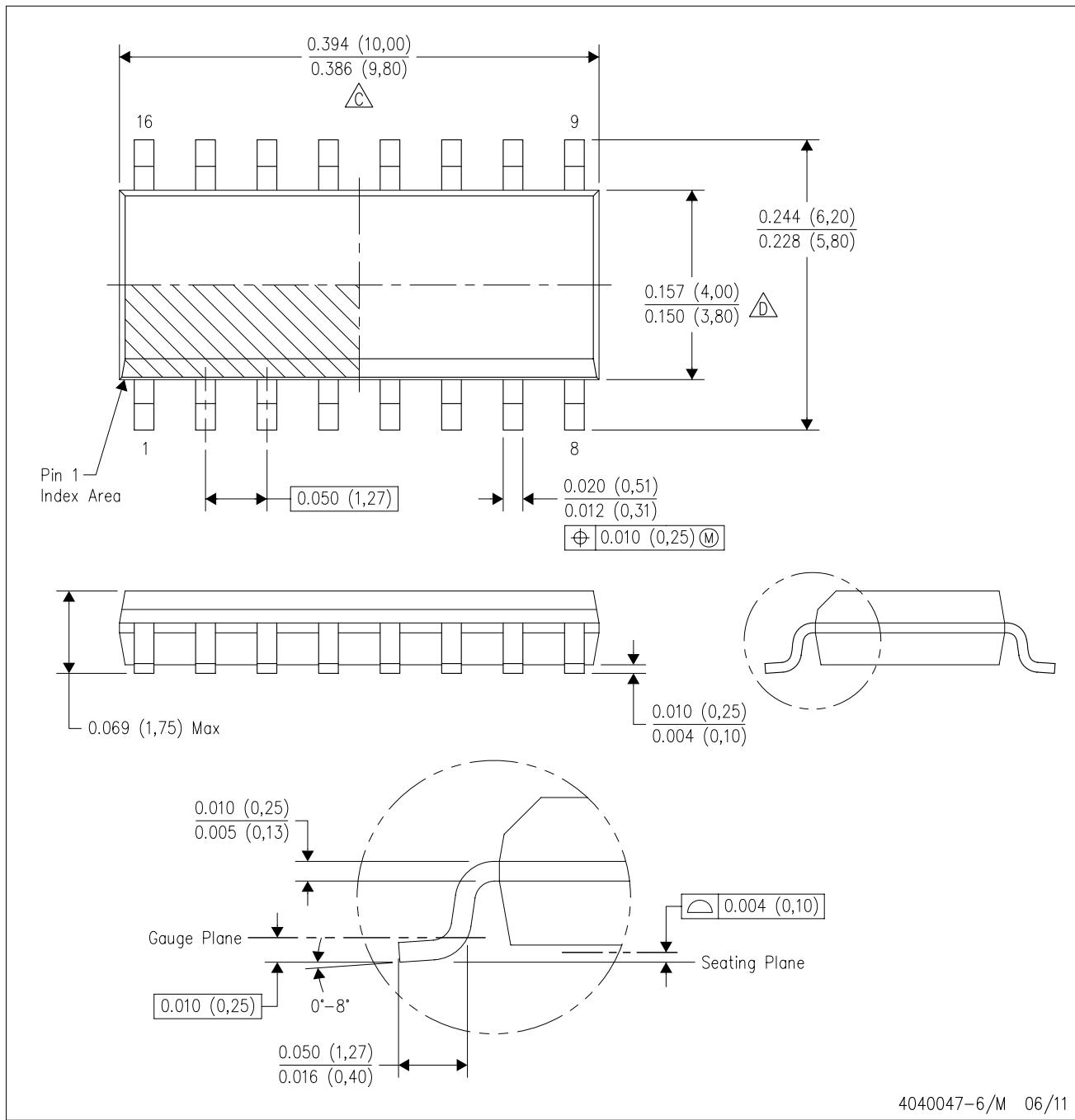
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

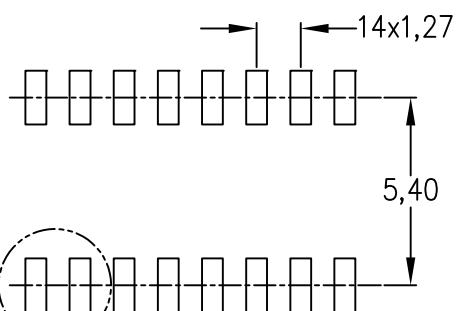
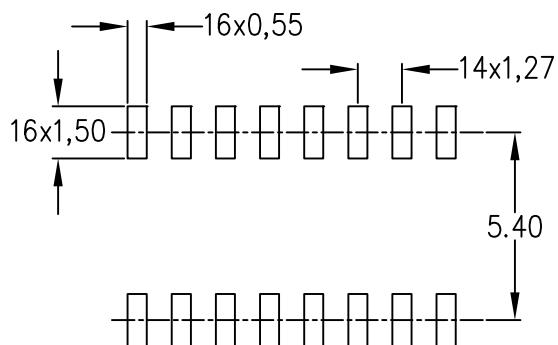
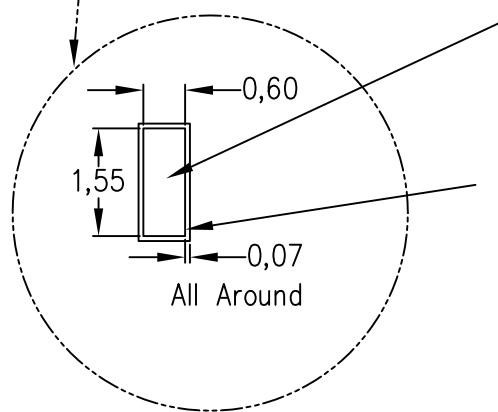
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

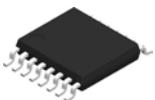
4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

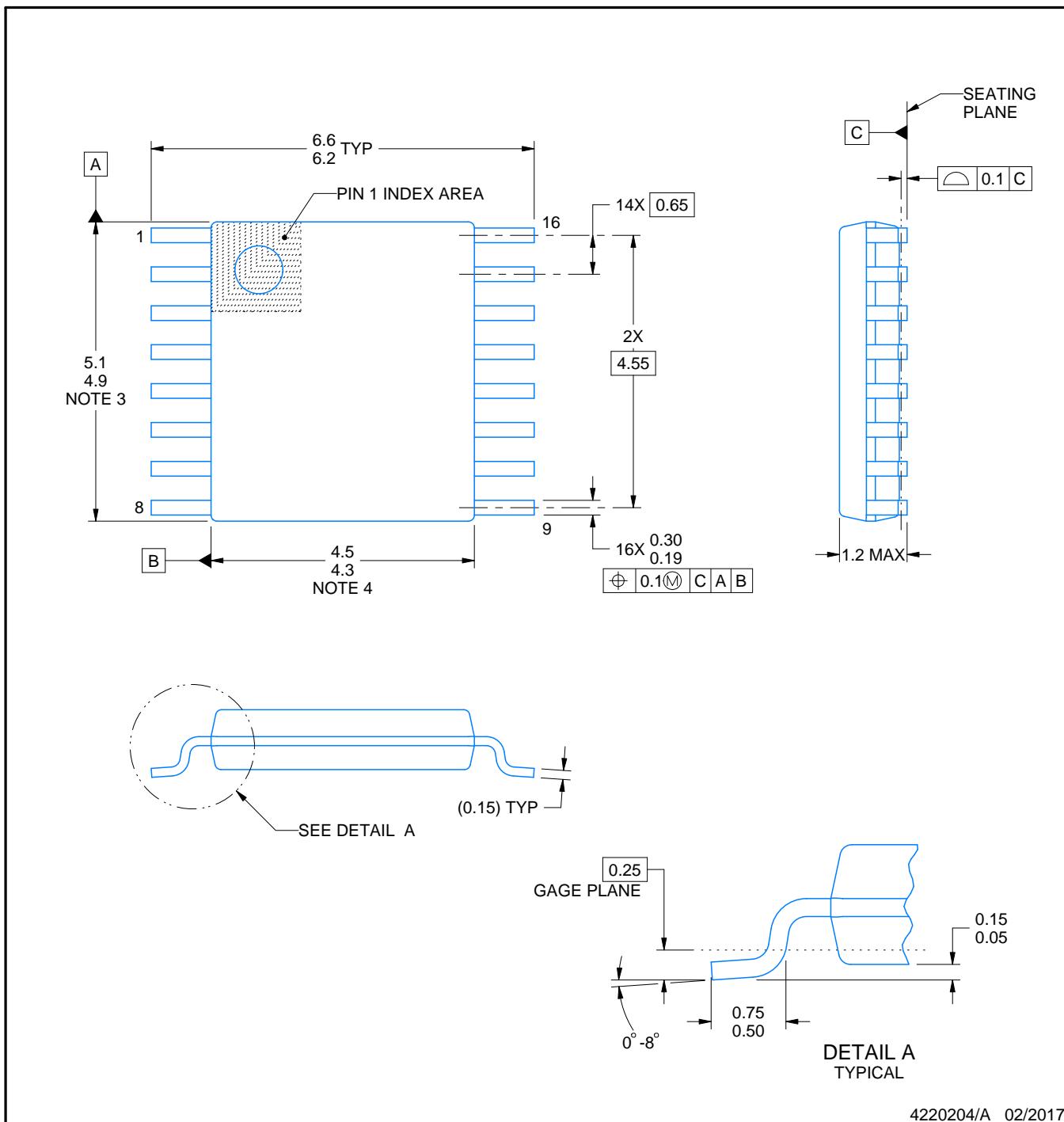
PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

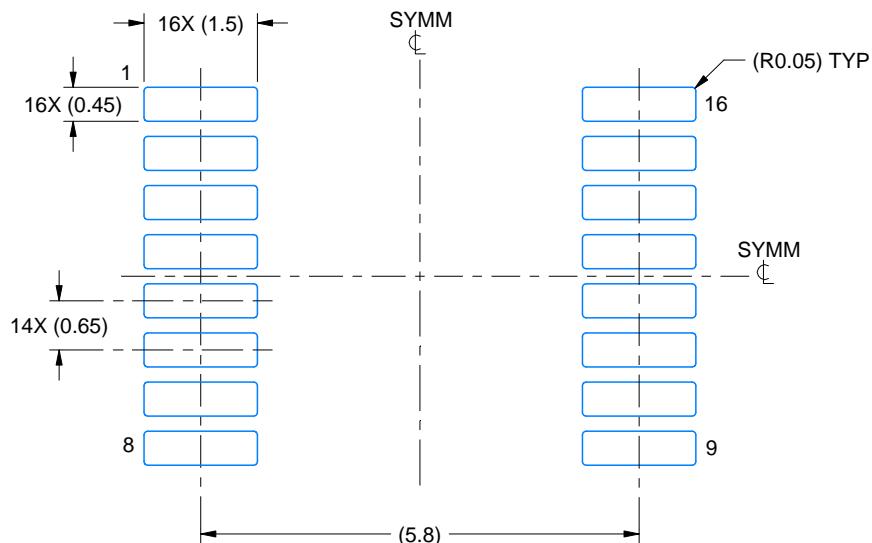
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

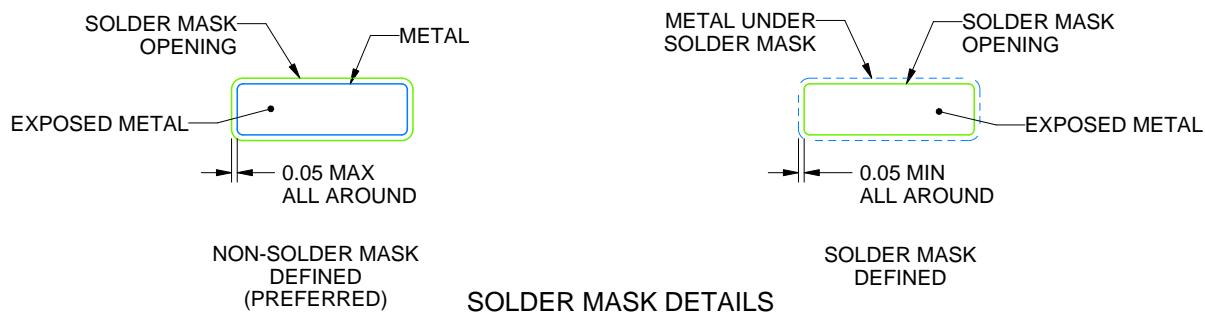
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

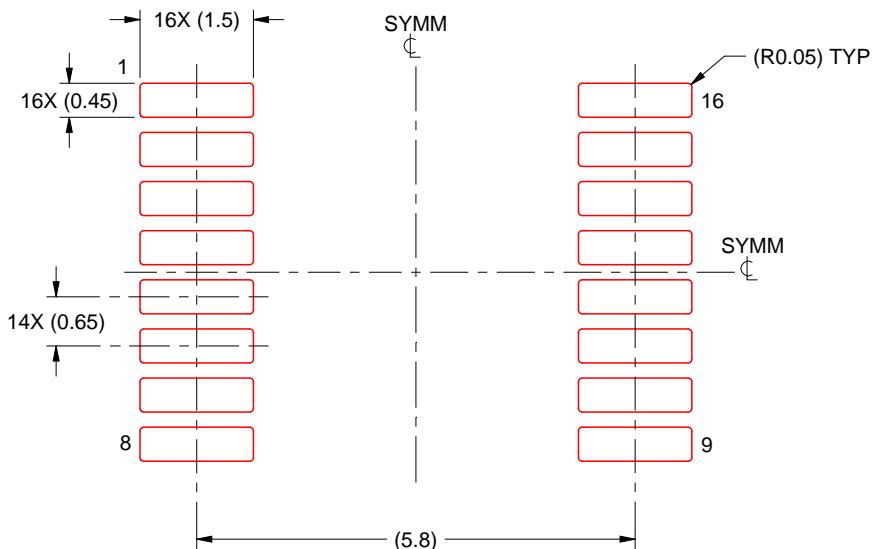
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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