具有可调节恒流模式和睡眠模式且用于备用电池充电的 TPS61251 升压转换器

1 特性

- 电阻可编程输入电流限制
  - 电流为 500mA 时，在整个温度范围内电流精度为 ±10%
  - 可编程电流：100mA 至 1500mA
- 睡眠模式仅消耗 2μA（典型值）的静态电流
- 适用于为大电容器充电（值在法拉范围内）
- 效率高达 92%
- 电源正常指示即使在关断状态下的输出电压电平仍处于正常水平
- 输入电压范围为 2.3V 至 6V
- 可调节输出电压高达 6.5V
- 输入电压大于输出电压时为 100% 占空比模式
- 负载断开和反向电流保护
- 短路保护
- 典型工作频率：3.5MHz
- 采用 2 × 2mm WSON-8 封装
- 使用 TPS61251 并借助 WEBENCH® 电源设计器创建定制设计

2 应用

- 带有高峰值功率负载（SSD、PCMCIA Tx 突发、存储器、GPRS/GSM Tx）的 电流限制 应用
- 锂离子电池 应用
- 备用电池 应用
- 音频 应用
- RF-PA 缓冲器

3 说明

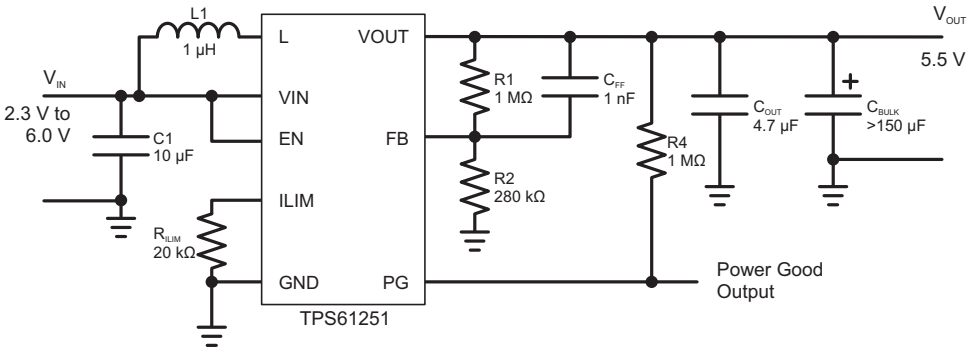
TPS61251器件可以为由 3 节镍镉或镍氢电池或者单节锂离子或锂聚合物电池供电的产品提供电源解决方案。输入电压范围很宽，非常适合为手机、固态硬盘 (SSD) 和无线调制解调器等便携式 应用 供电。该转换器适合为大电容器（法拉范围）充电，支持备用电池应用。在电容器充电过程中，TPS61251 器件作为恒流源工作，直到输出电压达到编程值。可通过外部电阻器 R_{ILIM} 对充电电流进行编程，并针对 500mA 平均输入电流限制提供 ±10% 的精度。 中增加了“500mA 平均输入电流限制的精度为 ±10%”

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS61251	WSON (8)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

Changes from Revision B (July 2015) to Revision C — **Page**

- 已添加 在*特性* 和*说明* 1
- 已添加 增加了 Webench 链接 1
- 已添加 *接收文档更新通知* 20

Changes from Revision A (May 2015) to Revision B — **Page**

- Deleted package suffix from device number in the Device Options table. 3

Changes from Original (September 2010) to Revision A — **Page**

- 已添加 添加了 *ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1

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5 说明 （续）

将 TPS61251 器件与充电电容器结合使用，使转换器能够提供超出供电电路（PC 插槽、USB）能力的高电流脉冲，并使插槽电源安全地在其能力范围内工作。在轻负载下，该器件会自动进入增强省电模式（睡眠模式），从而使转换器维持需要的输出电压，同时只消耗 2μA 的电池电流。这样就能以最低的静态电流实现最高的效率。

为了实现小解决方案尺寸，TPS61251 器件允许使用小型电感器和输入电容器。在关断期间，负载与电池完全断开连接，这时既不会对电池放电，也不会对已充电的大容量电容器放电。TPS61251 器件采用 2mm × 2mm 8 引脚 QFN 封装 (DSG)。

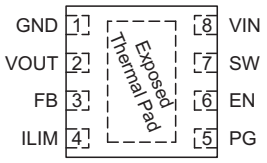
6 Device Options

OUTPUT VOLTAGE(1)	PART NUMBER(2)
Adjustable	TPS61251

(1) Contact TI for other fixed output voltage options
(2) For detailed ordering information check the *机械、封装和可订购信息* section at the end of this data sheet.

7 Pin Configuration and Functions

DSG Package
8-Pin WSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	6	I	Enable input (1 enabled, 0 disabled)
FB	3	I	Voltage feedback pin
GND	1		Ground
ILIM	4	I	Adjustable average input current limit. Can be connected to V_{IN} for maximum current limit or to GND for minimum current limit.
PG	5	O	Output power good (1 good, 0 failure; open drain)
SW	7	I	Connection for Inductor
VIN	8	I	Supply voltage for power stage
VOUT	2	O	Boost converter output
Exposed Thermal Pad			Must be soldered to achieve appropriate power dissipation and for mechanical reasons. Must be connected to GND.

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage[2]	VIN, VOUT, SW, EN, PG, FB, ILIM	–0.3	7	V
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage at VIN	2.3		6	V
Output voltage at VOUT	3		6.5	V
Programable input current limit set by R_{ILIM}	100		1500	mA
Operating free air temperature, T_A	–40		85	°C
Operating junction temperature, T_J	–40		125	°C

8.4 Thermal Information

THERMAL METRIC[1]		TPS61251 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	93.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.3	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	20	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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8.5 Electrical Characteristics

Over recommended free air temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V, V_{OUT} = 5.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback voltage		1.182	1.2	1.218	V
	Maximum line regulation	2.3 V ≤ V_{IN} ≤ 6 V		0.5%		
	Maximum load regulation			0.5%		
f	Oscillator frequency			3500		kHz
$r_{DS(on)}$	High side switch ON resistance			200		mΩ
	Low side switch ON resistance			130		mΩ
	Reverse leakage current into V_{OUT}	EN = GND			3.5	µA
$I_{IN(DC)}$	Programmable input average switch current limit	ILIM pin set to V_{IN}		1500		mA
		ILIM pin set to GND		100		mA
		R_{ILIM} = 20 kΩ (500 mA)	–10%		10%	
I_Q	Quiescent current	PFM enabled, device is not switching		30		µA
		SNOOZE mode, I_{OUT} = 0 mA, current into V_{IN} pin		2		
I_{SD}	Shutdown current(1)	V_{IN} turned on when EN is connected to GND and no voltage is present at V_{OUT}		0.85	3.5	µA
OVP	Input over voltage protection threshold	Falling		6.4		V
		Rising		6.5		
CONTROL STAGE						
V_{UVLO}	Under voltage lockout threshold	Falling		2	2.1	V
		Hysteresis		0.1		V
V_{IL}	EN input low voltage	2.3 V ≤ V_{IN} ≤ 6 V			0.4	V
V_{IH}	EN input high voltage	2.3 V ≤ V_{IN} ≤ 6 V	1			V
	EN, PG input leakage current	Clamped on GND or V_{IN}			0.5	µA
	Power Good threshold voltage	Rising referred to V_{FB}	92.5%	95%	97.5%	
		Falling referred to V_{OUT}		2.3		V
	Power good delay			50		µs
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C

(1) When the power good threshold is triggered the first time a comparator is turned on to observe the output voltage increasing the shutdown current.

8.6 Typical Characteristics

Table 1. Table Of Graphs

DESCRIPTION		FIGURE
Efficiency	vs Output current (V_{OUT} = 5.5 V, I_{LIM} = 1.5 A, R1 = 2320 kΩ and R2 = 649 kΩ)	Figure 1
	vs Output current in 100% Duty-Cycle Mode (V_{OUT} = 5.5V, I_{LIM} = 1.5 A, R1 = 2320 kΩ and R2 = 649 kΩ)	Figure 2
	vs Input voltage (V_{OUT} = 5.5 V, I_{LOAD} = {0.01;0.1; 1.0; 10; 100; 500 mA}, R1 = 2320 kΩ and R2 = 649 kΩ)	Figure 3
Maximum output current	vs Input voltage (V_{OUT} = 5.5 V, I_{LIM} = {100; 200; 500; 1000; 1500 mA}, R1 = 1000 kΩ and R2 = 280 kΩ)	Figure 4
Output voltage	vs Output current (V_{OUT} = 5.5 V, I_{LIM} = 1.5 A, R1 = 1000 kΩ and R2 = 280 kΩ)	Figure 5

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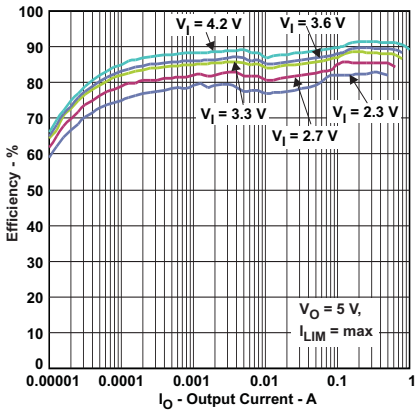

Figure 1. Efficiency vs Output Current

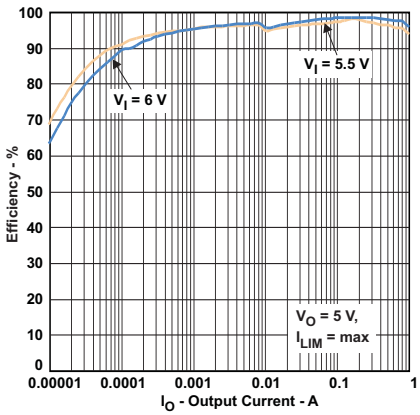

Figure 2. Efficiency vs Output Current In 100% Duty-Cycle Mode

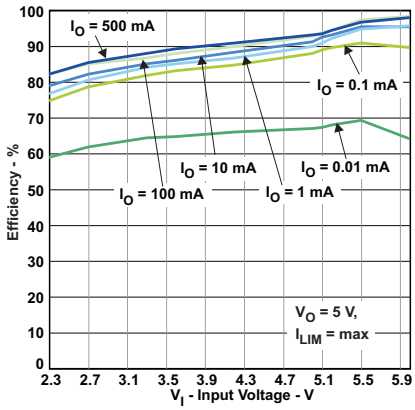

Figure 3. Efficiency vs Input Voltage

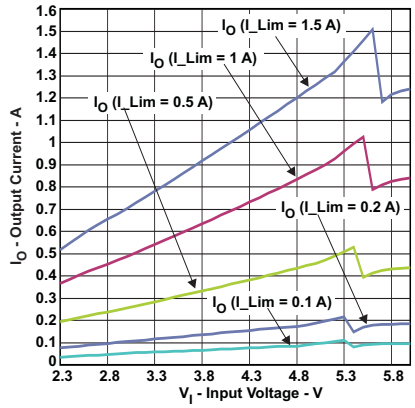

Figure 4. Maximum Output Current vs Input Voltage

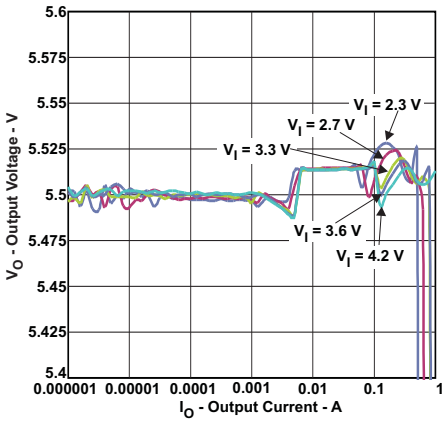

Figure 5. Output Voltage vs Output Current

9 Detailed Description

9.1 Overview

The TPS61251 boost converter operates as a quasi-constant frequency adaptive on-time controller. In a typical application the frequency is 3.5 MHz and is defined by the input to output voltage ratio and does not vary from moderate to heavy load currents. At light load the converter automatically enters power-save mode and operates in pulse frequency modulation (PFM) mode. During PWM operation the converter uses a unique fast response quasi-constant on-time valley current mode controller scheme which offers excellent line and load regulation and the use of small ceramic input capacitors.

Based on the V_{IN}/V_{OUT} ratio, a simple circuit predicts the required on-time. At the beginning of the switching cycle, the low-side N-MOS switch is turned on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once the on-timer has expired, the rectifier is turned on and the inductor current decays to a preset valley current threshold. Finally, the switching cycle repeats by setting the on timer again and activating the low-side N-MOS switch.

The TPS61251 device directly and accurately controls the average input current through intelligent adjustment of the valley current limit, allowing an accuracy of ±10% at 500-mA average input current. Together with an external bulk capacitor the TPS61251 device allows an application to be interfaced directly to its load, without overloading the input source due to appropriate set average input current limit.

High values of output capacitance are mainly achieved by putting capacitors in parallel. This reduces the overall series resistance (ESR) to very low values. This results in almost no voltage ripple at the output and therefore the regulation circuit has no voltage drop to react on. Nevertheless to ensure accurate output voltage regulation even with very low ESR the regulation loop can switch to a pure comparator regulation scheme. During this operation the output voltage is regulated between two thresholds. The upper threshold is defined by the programmed output voltage and the lower value is about 10 mV lower. If the upper threshold is reached the off-time is increased to reduce the current in the inductor. Therefore the output voltage will slightly drop until the lower threshold is tripped. Now the off-time is reduced to increase the current in the inductor to charge up the output voltage to the steady-state value. The current swing during this operation mode is strongly depending on the current drawn by the load but will not exceed the programmed current limit. The output voltage during comparator operation stays within the specified accuracy with minimum voltage ripple.

This architecture with adaptive slope compensation provides excellent transient load response and requiring minimal output filtering. Internal softstart and loop compensation simplifies the design process while minimizing the number of external components.

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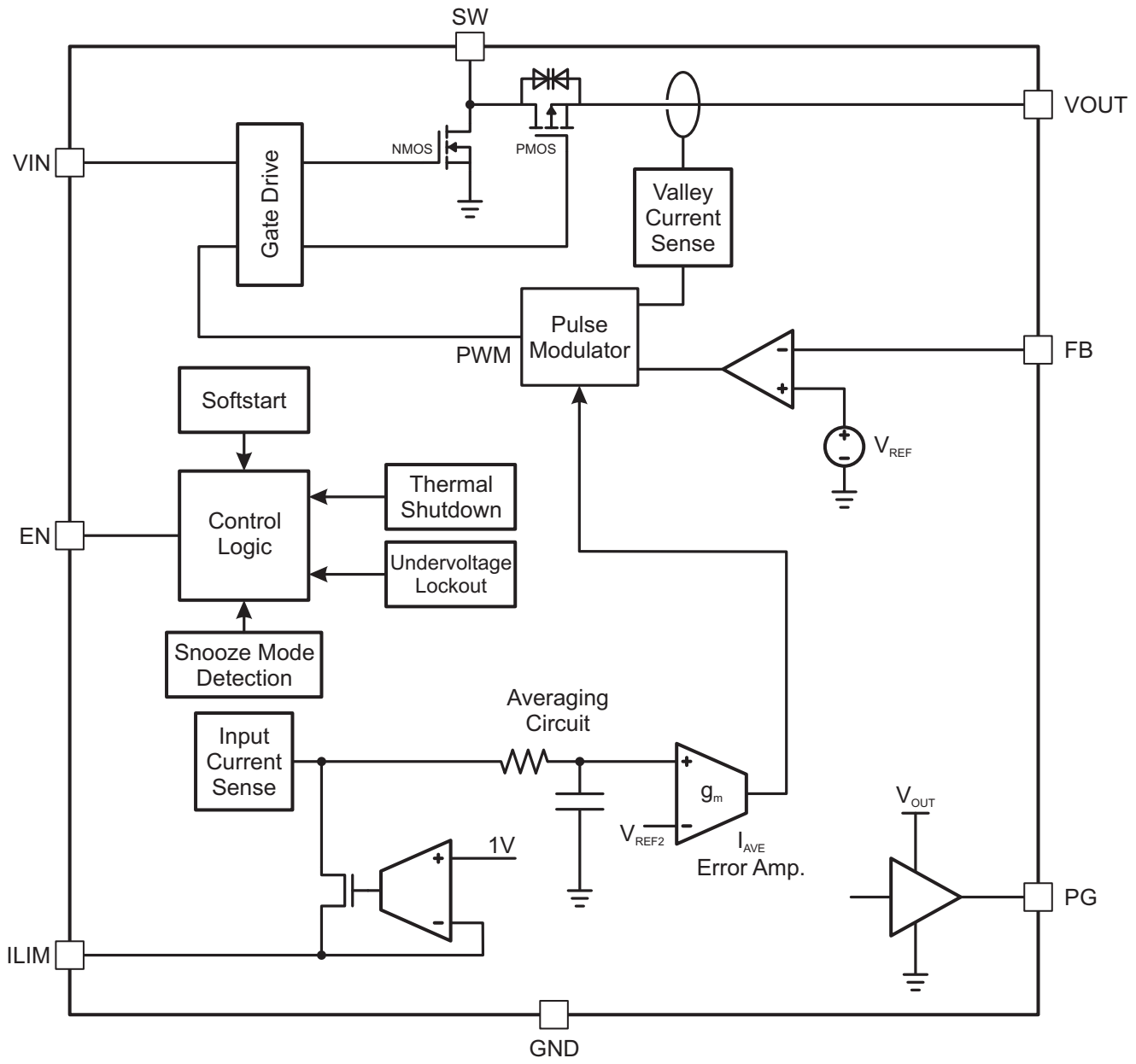
9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Current Limit Operation

The current limit circuit employs a valley current sensing scheme. Current limit detection occurs during the off-time through sensing of the voltage drop across the synchronous rectifier. The output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit (CL) operation, can be defined by Equation 1 as shown below:

$$I_{OUT(CL)} = (1 - D) \cdot I_{IN(DC)} \tag{1}$$

The duty cycle (D) can be estimated by following Equation 2

$$D = 1 - \frac{V_{IN} \cdot \eta}{V_{OUT}} \tag{2}$$

Feature Description (continued)

9.3.2 Soft Start

The TPS61251 device has an internal charging circuit that controls the current during the output capacitor charging and prevents the converter from inrush current that exceeds the set current limit. For typical 100 µs the current is ramped to the set current limit. After reaching the current limit threshold the output capacitor is charged with a constant current until the programmed output voltage is reached. During the phase where $V_{IN} > V_{OUT}$ the rectifying switch is controlled by the current limit circuit and works as a linear regulator in constant current mode. If then $V_{IN} = V_{OUT}$, the converter starts switching and boosting up the voltage to its nominal output voltage by still charging the capacitor with a constant current set by resistor R_{ILIM}. During constant current charging power dissipation in the TPS61251 device is increased resulting in a thermal rise or heating of the device. If the output capacitor is very large charging time can be long and thermal rise high. To prevent overheating of the device during the charge phase the current will be limited to a lower value when device temperature is high. Please refer to *Thermal Regulation*.

9.3.3 Enable

The device is enabled by setting EN pin to a voltage above 1 V. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the softstart is activated and the output voltage ramps up. The output voltage reaches its nominal value as fast as the current limit settings and the load condition allows it.

The EN input can be used to control power sequencing in a system with several DC-DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the device enters shutdown mode.

9.3.4 Undervoltage Lockout (UVLO)

The UVLO prevents the device from malfunctioning at low input voltages and the battery from excessive discharge. It disables the output stage of the converter once the falling V_{IN} trips the undervoltage lockout threshold V_{UVLO} which is typically 2 V. The device starts operation once the rising V_{IN} trips V_{UVLO} threshold plus its hysteresis of 100 mV at typical 2.1 V.

9.3.5 Power Good

The device has a built-in power good function to indicate whether the output voltage has reached the programmed value and therefore the capacitor is fully charged. The power good output (PG) is set high if the feedback voltage reaches 95% of its nominal value. The power good comparator operates even in shut down mode when EN is set to low and/or V_{IN} is turned off. This guaranties power good functionality until the capacitor is discharged. The PG output goes low when V_{OUT} drops below 2.3 V and indicates the discharge of the capacitor. If the output voltage decreases further and goes below 2 V the converter disables all internal circuitry. Therefore the PG open drain output becomes high resistive and follows the voltage the pullup resistor is connected to.

Because power good functionality is active as long as the output capacitors are charged the converter can be disconnected from its supply but is still supplying the following circuitry with energy. A connected buck converter or buck-boost converter can use this energy to support a follow-on circuit that needs additional energy for a secured shut down.

9.3.6 Input Overvoltage Protection

This converter has a input overvoltage protection that protects the device from damage due to a voltage higher than the absolute maximum rating of the input allows. If 6.5 V (typical) at the input is exceeded, the converter completely shuts down to protect its inner circuitry as well as the circuit connected to V_{OUT}. If the input voltage drops below 6.4 V (typical), the device turns on again and enters normal start-up again.

9.3.7 Load Disconnect and Reverse Current Protection

The TPS61251 device has an intelligent load disconnect circuit that prevents current flow in any direction during shutdown. In case of a connected battery and $V_{IN} > V_{OUT}$ the converter will not discharge the battery during shutdown of the converter. In the opposite case when a bulk capacitor is connected to VOUT and charged to a higher voltage than V_{IN} the converter prevents the capacitor from being discharged through the input load (battery).

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Feature Description (continued)

9.3.8 Thermal Regulation

The TPS61251 device contains a thermal regulation loop that monitors the die temperature. If the die temperature rises to values above 110°C, the device automatically reduces the current to prevent the die temperature from further increasing. Once the die temperature drops about 10°C below the threshold, the device will automatically increase the current to the target value. This function also reduces the current during a short-circuit-condition.

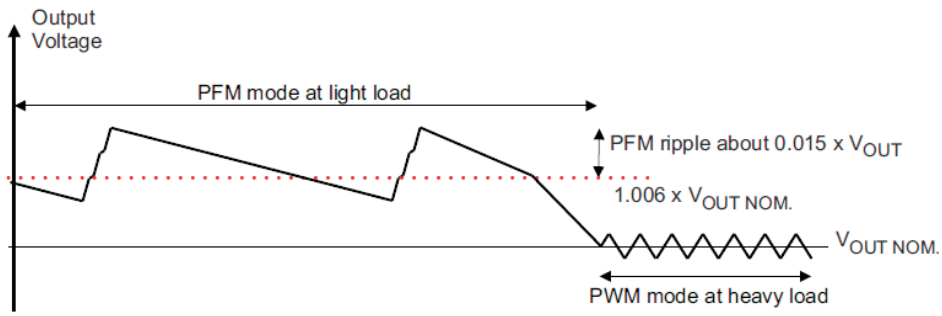
9.3.9 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 140°C (typical) the device enters thermal shutdown. In this mode, the High Side and Low Side MOSFETs are turned off. When the junction temperature falls about 20°C below the thermal shutdown, the device continues the operation.

9.4 Device Functional Modes

9.4.1 Power-Save Mode

The TPS61251 device integrates a power save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage. During the power save operation when the output voltage is above the set threshold the converter turns off some of the inner circuits to save energy.



The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.

9.4.2 Snooze Mode

During this enhanced power save mode, the converter still maintains the output voltage with a tolerance of ±2%. The operating current in snooze mode is, however, drastically reduced to a typical value of 2 µA. This will be achieved by turning off as much as possible of the inner regulation circuits. Load current in snooze mode is limited to 2 mA. If the load current increases above 2 mA, the controller recognizes a further drop of the output voltage and the device turns on again to charge the output capacitor to the programmed output voltage again.

9.4.3 100% Duty-Cycle Mode

If $V_{IN} > V_{OUT}$ the TPS61251 device offers the lowest possible input-to-output voltage difference while still maintaining current limit operation with the use of the 100% duty-cycle mode. In this mode, the PMOS switch is constantly turned on. During this operation the output voltage follows the input voltage and will not fall below the programmed value if the input voltage decreases below V_{OUT}. The output voltage drop during 100% mode depends on the load current and input voltage, and the resulting output voltage is calculated using Equation 3.

$$V_{OUT} = V_{IN} - \left(DCR + r_{DS(on)}\right) \cdot I_{OUT}$$

where

- DCR is the DC resistance of the inductor
- $r_{DS(on)}$ is the typical on-resistance of the PMOS switch (3)

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS61251 device provides a power supply solution for products powered by either a three-cell, NiCd or NiMH battery, or a one-cell Li-Ion or Li-polymer battery. The wide input voltage range is ideal to power portable applications like mobile phones, solid state drives (SSD) and wireless modems. The converter is designed to charge large capacitors in the Farad range to support battery back up applications.

10.2 Typical Application

Figure 6 shows a typical application for 5.5-V output voltage with input current limit.

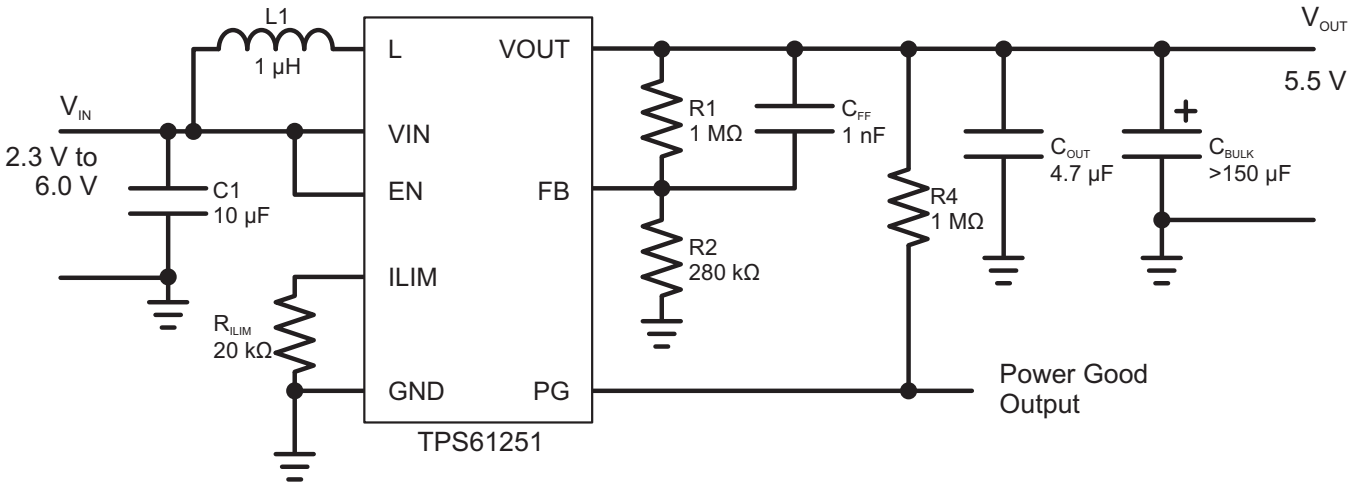


Figure 6. Typical Application Schematic

10.2.1 Design Requirements

Table 2 lists the design requirements.

Table 2. Design Parameters

PARAMETER	SYMBOL	VALUE	UNIT
Input voltage	V_{IN}	3.6	V
Minimum input voltage	$V_{IN(min)}$	2.9	V
Output voltage	V_{OUT}	5.5	V
Input current limit set by R_{ILIM}	I_{LIM}	500	mA
Feedback voltage	V_{FB}	1.2	V
Switching frequency	f	3.5	MHz
Estimated efficiency	η	90%	
Inductor value of choice	L1	1	µH

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10.2.2 Detailed Design Procedure

10.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS61251 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2.2.2 Output Voltage Setting

The output voltage can be calculated using Equation 4.

$$V_{OUT} = V_{FB} \cdot \left(1 + \frac{R_1}{R_2}\right) \tag{4}$$

To minimize the current through the feedback divider network and therefore increase efficiency during snooze mode operation, R2 must be > 240 k. To keep the network robust against noise the resistor divider can also be in the lower 100-k values. In this case, R1 is 1000 kΩ and R2 is 280 kΩ.

An external feed forward capacitor C1 is required for optimum load transient response. The value of C1 must be 1000 pF. The connection from FB pin to the resistor divider should be kept short and away from noise sources, such as the inductor or the SW line.

10.2.2.3 Average Input Current Limit

The average input current is set by selecting the correct external resistor value correlating to the required current limit. Equation 5 is a guideline for selecting the correct resistor value.

$$R_{ILIM} = \frac{1.0V}{I_{LIM}} \cdot 10{,}000 \tag{5}$$

For a current limit of 500 mA the resistor value is 20 kΩ

To allow maximum current limit (1500 mA) the ILIM pin can be directly connected to V_{IN}. If ILIM is connected to GND the minimum current (100 mA) limit is set.

10.2.2.4 Maximum Output Current

The maximum output current is set by R_{ILIM} and the input to output voltage ratio and can be calculated using Equation 6.

$$I_{OUT(max)} \approx I_{LIM} \cdot \frac{V_{IN} \cdot \eta}{V_{OUT}} \tag{6}$$

Following the example, $I_{OUT(max)}$ will be 295 mA at 3.6 V input voltage and will decrease with lower input voltage values due to the energy conservation.

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10.2.2.5 Inductor Selection

As for all switch mode power supplies two main passive components are required for storing the energy during operation. This is done by an inductor and an output capacitor. The inductor must be connected between VIN and SW pin to make sure that the TPS61251 device operates. To select the right inductor current rating the programmed input current limit as well as the current ripple through the inductor is necessary. Estimation of the maximum peak inductor current can be done using Equation 7.

$$I_{L(max)} = I_{LIM} + \Delta I_L = I_{LIM} + \frac{V_{IN(min)} \cdot D}{L \cdot f} \quad \text{with} \quad D = 1 - \frac{V_{IN(min)} \cdot \eta}{V_{OUT}} \tag{7}$$

Regarding the example from above the current ripple (ΔI_L) will be 290 mA and therefore an inductor with a rated current of about 800 mA should be used.

The TPS61251 device is designed to work with inductor values between 1 µH and 2.2 µH. TI recommends a 1.5 µH inductor for typical applications. In space constrained applications, it might be possible to consider smaller inductor values depending on the targeted inductor ripple current. Therefore, the inductor value can be reduced down to 1 µH without degrading the stability.

In regular boost converter designs the current through the inductor is defined by the switch current limit of the converters switches and therefore bigger inductors have to be chosen. The TPS61251 device allows the design engineer to reduce the current limit to the needs of the application regardless the maximum switch current limit of the converter. Programming a lower current value allows the use of smaller inductors without the danger to get into saturation.

10.2.2.6 Output Capacitor

The second energy storing device is the output capacitor. When selecting output capacitors for large pulsed loads, the magnitude and duration of the pulsing current, together with the ripple voltage specification, determine the choice of the output capacitor. Both the ESR of the capacitor and the charge stored in the capacitor each cycle contribute to the output voltage ripple. The ripple due to the charge is approximately what results from Equation 8.

$$V_{RIPPLE(mV)} = \frac{I_{PULSE} - I_{STANDBY} \cdot t_{on}}{C_{OUT}}$$

where

- I_{PULSE} and t_{ON} are the peak current and on time during transmission burst.
- $I_{STANDBY}$ is the current in standby mode. (8)

The above is a worst-case approximation assuming all the pulsing energy comes from the output capacitor.

The ripple due to the capacitor ESR is defined by Equation 9.

$$\Delta V_{ESR} = \left(I_{PULSE} - I_{STANDBY}\right) \cdot ESR \tag{9}$$

High capacitance values and low ESR can lead to instability in some internally compensated boost converters. The internal loop compensation of the TPS61251 device is optimized to be stable with output capacitor values greater than 150 µF with very low ESR.

Because big bulk capacitors can not be placed very close to the IC, it is required to put a small ceramic capacitor of about 4.7 µF as close as possible to the output terminals. This will reduce parasitic effects that can influence the functionality of the converter.

Table 3. List Of Bulk Capacitors

VENDOR (alphabetical order)	CAPACITANCE	PART NUMBER
Kemet	470 µF, 6.3 V, 55 mΩ	T520W477M006ATE055
Sanyo	470 µF, 6.3 V, 35 mΩ	6TPE470MAZU

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10.2.2.7 Input Capacitor

Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small form factors. Input capacitors should be located as close as possible to the device. While a 10-µF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple on the supply rail without limitations. Although low ESR tantalum capacitors may be used.

NOTE

DC Bias effect: High capacitance ceramic capacitors have a DC Bias effect, which has a strong influence on the final effective capacitance. Therefore, the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and the effective capacitance. A 10-V rated 0805 capacitor with 10 µF can have an effective capacitance of less 5 µF at an output voltage of 5 V.

10.2.2.8 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the load transient takes place and the turn on of the PMOS switch, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ × ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45°C of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

10.2.3 Application Curves

Table 4. Table Of Graphs

DESCRIPTION		FIGURE
Waveforms	Load transient response (Tantal Capacitor 2.3 mF with >60 mΩ ESR, VOUT = 5.5 V, VIN = 3.6 V, ILIM = 1000 mA, Load change from 50 mA to 550 mA)	Figure 7
	Load transient response (6 × 330-uF Polymer Tantal <5 mΩ ESR in total, V_{OUT} = 5.5 V, V_{IN} = 3.6 V, I_{LIM} = 1000 mA, Load change from 500 mA to 1500 mA)	Figure 8
	Start-up after enable (V_{OUT} = 5.5 V, V_{IN} = 3.6 V, I_{LIM} = 1000 mA)	Figure 9
	Start-up after enable (V_{OUT} = 5.5 V, V_{IN} = 3.6 V, I_{LIM} = 500 mA)	Figure 10

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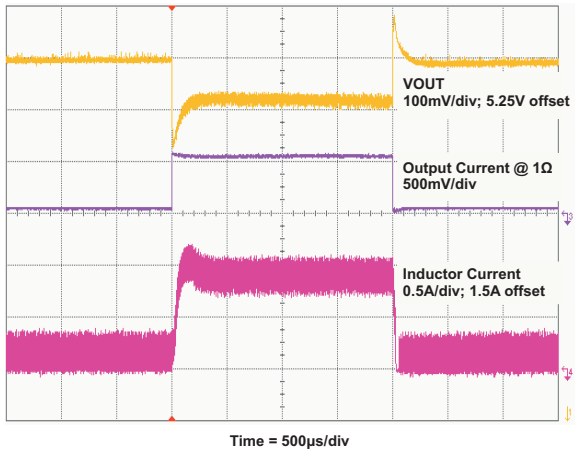

Figure 7. Load Transient Response (Tantal Capacitor)

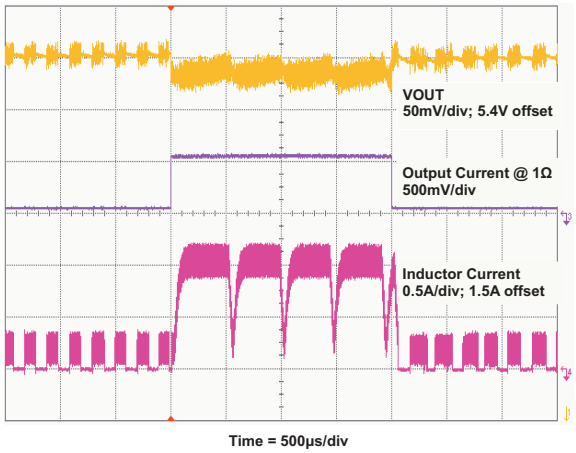

Figure 8. Load Transient Response (Low ESR Polymer Tantal)

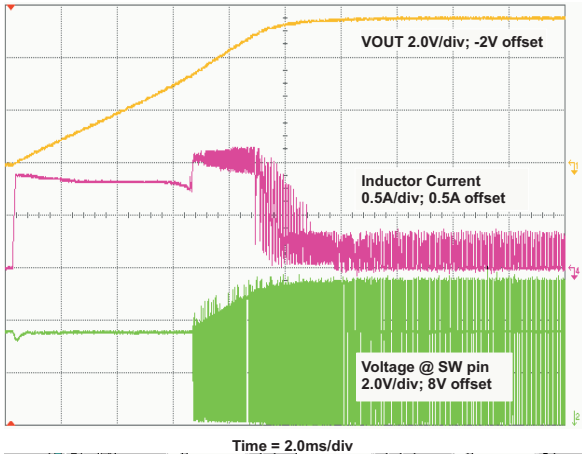

Figure 9. Start-Up After Enable I_{LIM} = 1000 mA, No Load

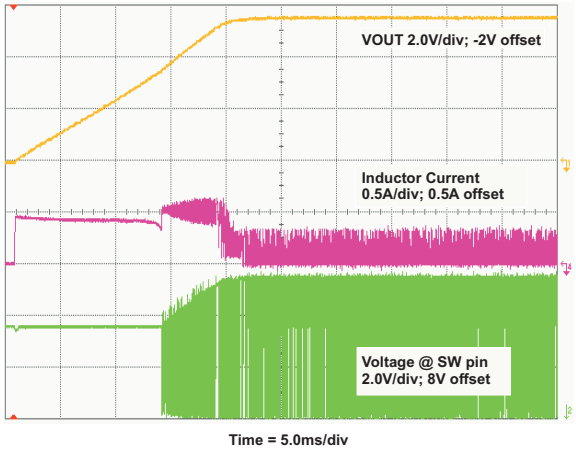

Figure 10. Start-Up After Enable I_{LIM} = 500 mA, No Load

Table 5 lists the components used for the waveform measurements.

Table 5. List Of Components

REFERENCE	DESCRIPTION	MANUFACTURER
U1	TPS61251	Texas Instruments
L1	1 µH, 2.1 A, 27 mΩ, 2.8 mm × 2.8 mm × 1.5 mm	DEM2815C, TOKO
C1	1 × 4.7 µF, 10 V, 0805, X7R ceramic	GRM21BR71A475KA73, Murata
C2	1 × 1000 pF, 50 V, 0603, COG ceramic	GRM1885C1H102JA01B, Murata
C3	1 × 4.7 µF, 10 V, 0805, X7R ceramic	GRM21BR71A475KA73, Murata
C4	20 × 100 uF, 6.3 V, 1206, X5R	GRM31CR60J107ME39B, Murata
R1	Depending on the output voltage of TPS61251, 1% (all waveform measurements with 5.5 V output voltage uses 1000 kΩ)	
R2	Depending on the output voltage of TPS61251, 1% (all waveform measurements with 5 V output voltage uses 280 kΩ)	
R3	Depending on the input current limit of TPS61251, 1%	

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Table 5. List Of Components (continued)

REFERENCE	DESCRIPTION	MANUFACTURER
R4	1 MΩ, 1%	any

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11 Power Supply Recommendations

The power supply can be a three-cell alkaline, NiCd or NiMH battery, or a one-cell Li-Ion or Li-polymer battery. The input supply should be well regulated with the rating of the TPS61251 device. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

12 Layout

12.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed close to the IC to keep the feedback connection short. To lay out the ground, short traces and wide are recommended. This avoids ground shift problems, which can occur due to superimposition of power ground current and the feedback divider.

12.2 Layout Example

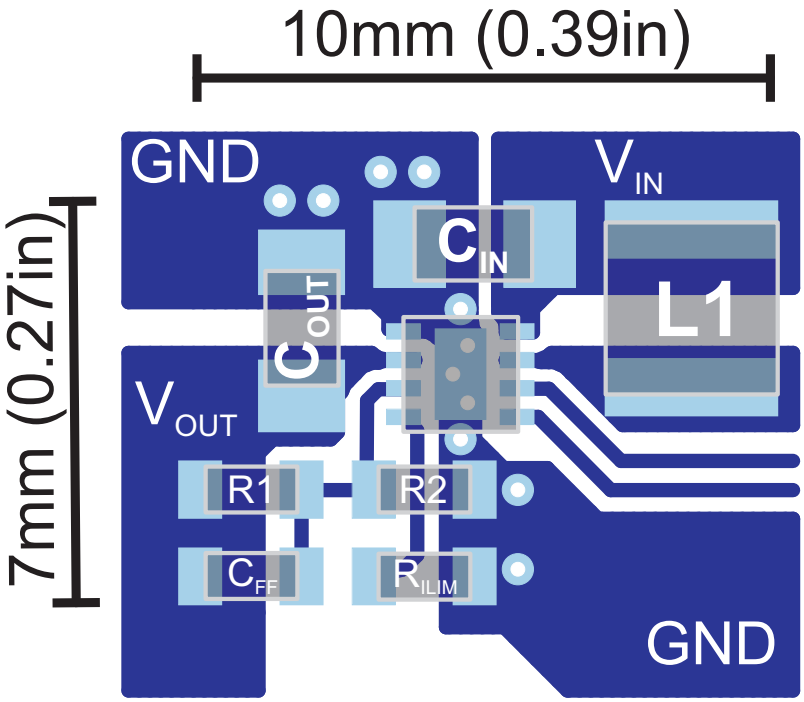

Figure 11. Suggested Layout Without Bulk Capacitors (Top)

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12.3 Thermal Consideration

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
  - For example, increase of the GND plane on the top layer which is connected to the exposed thermal pad
  - Use thicker cupper layer
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The maximum junction temperature (T_J) of the TPS61251 device is 150°C.

13 器件和文档支持

13.1 器件支持

13.1.1 第三方产品免责声明

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13.2 开发支持

13.2.1 使用 WEBENCH® 工具创建定制设计

单击此处，使用 TPS61251 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

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13.3 接收文档更新通知

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13.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

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14 机械、封装和可订购信息

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61251DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QTH	Samples
TPS61251DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QTH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

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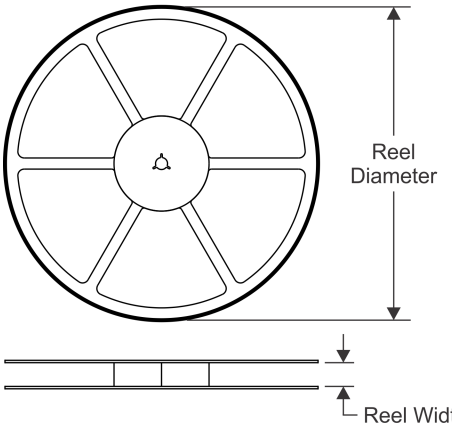
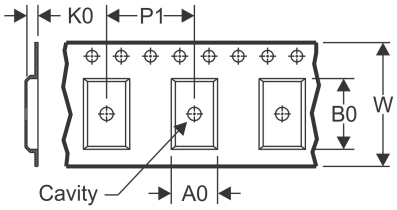
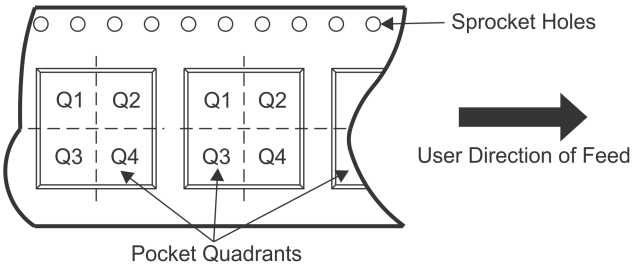


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

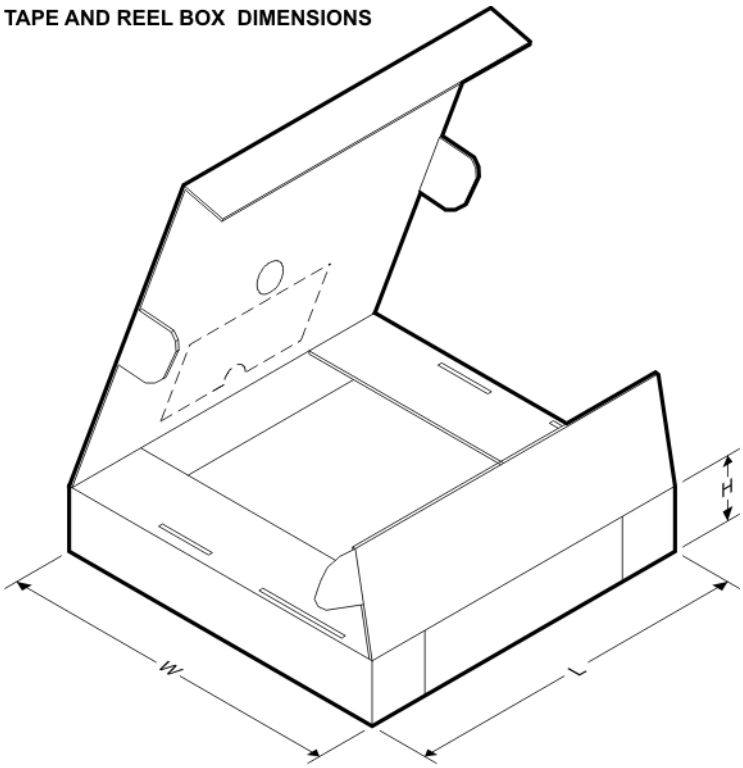
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61251DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS61251DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS61251DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS61251DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61251DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS61251DSGR	WSON	DSG	8	3000	213.0	191.0	35.0
TPS61251DSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS61251DSGT	WSON	DSG	8	250	213.0	191.0	35.0

GENERIC PACKAGE VIEW

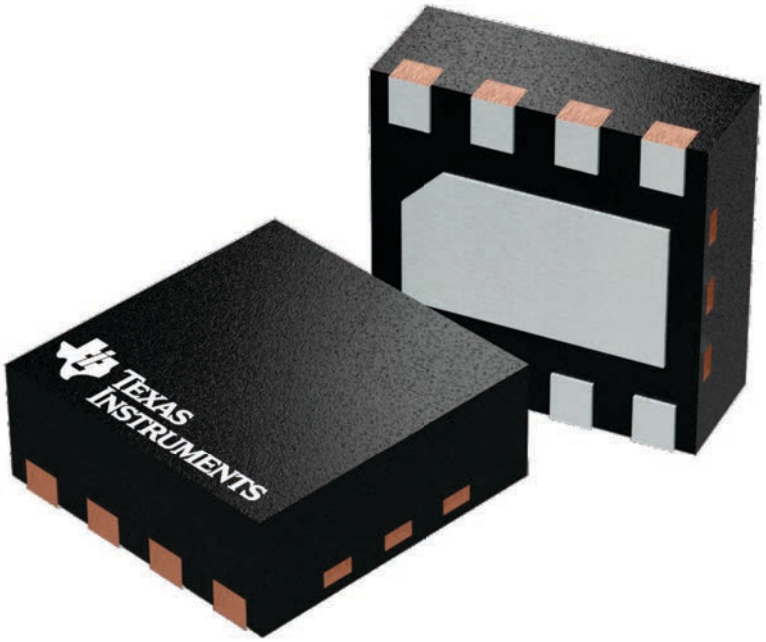
DSG 8

WSON - 0.8 mm max height

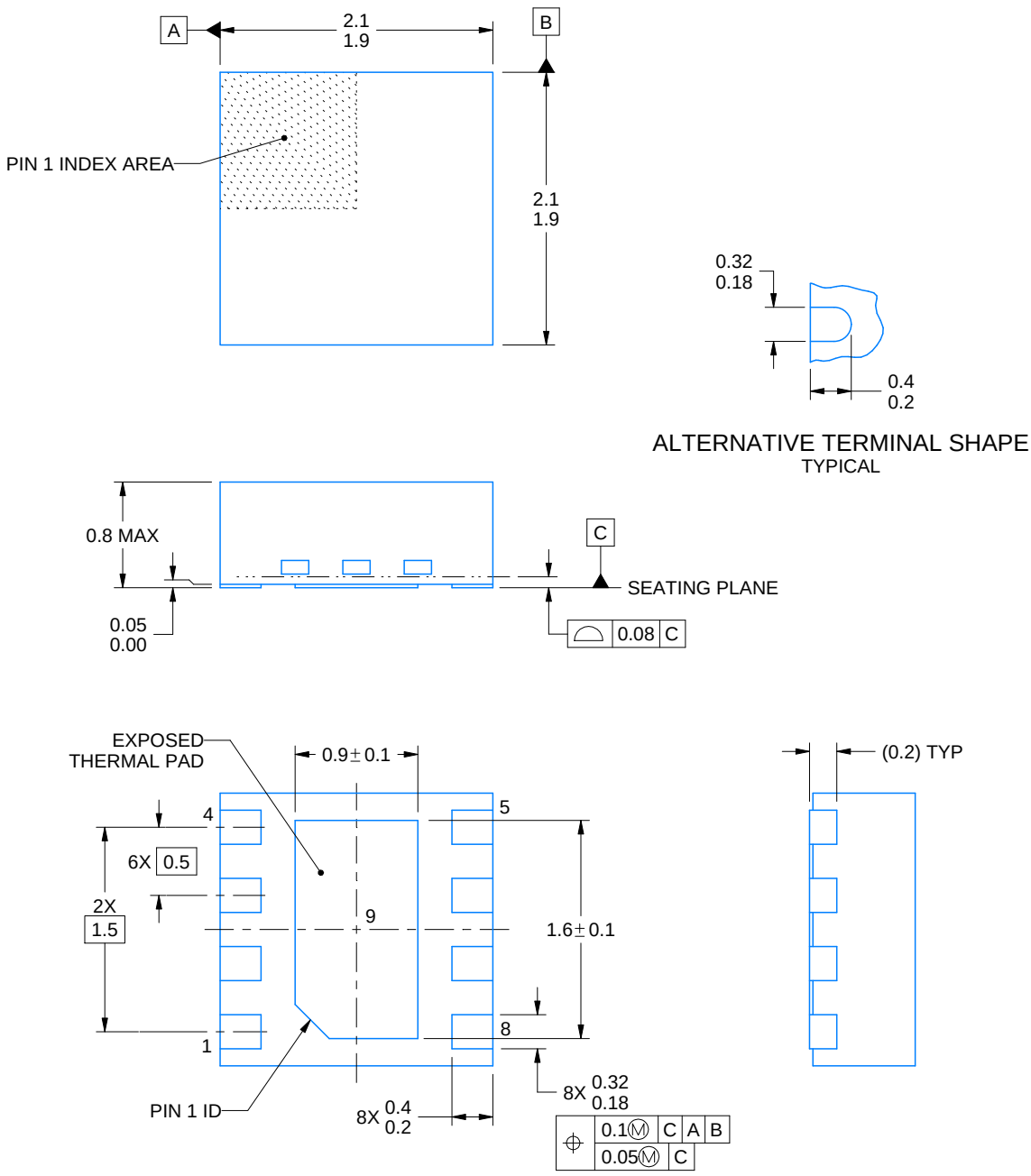
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

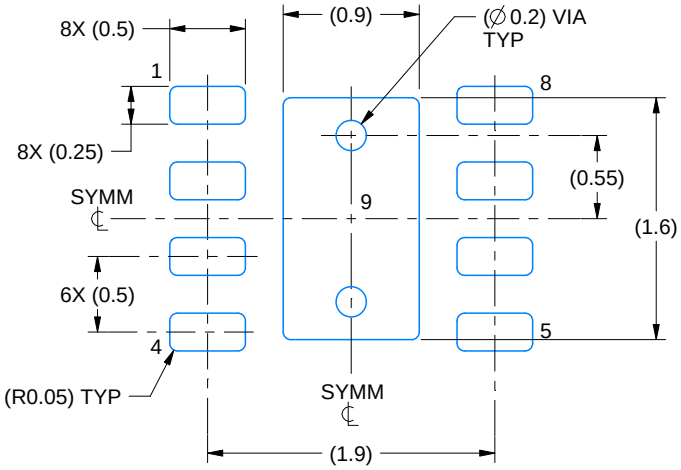


4224783/A

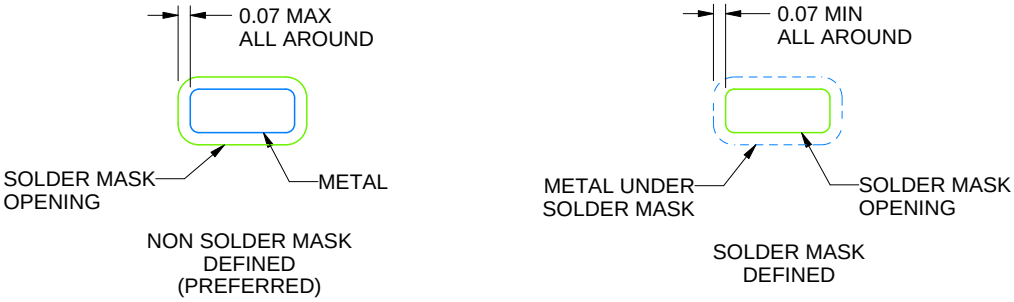


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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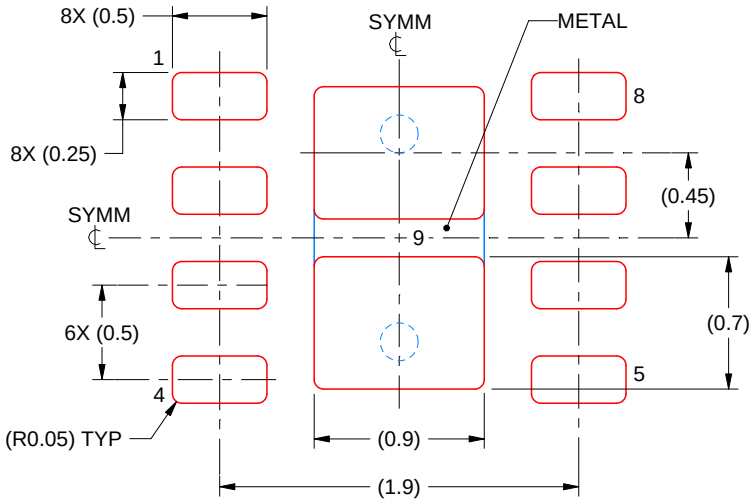
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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