CSD17483F4 30V N 沟道 FemtoFET™MOSFET

1 特性

- 低导通电阻
- 低 Q_g 和 Q_{gd}
- 低阈值电压
- 超小型封装尺寸（0402 外壳尺寸）
  - 1.0mm × 0.6mm
- 超薄
  - 高度为 0.35mm
- 集成 ESD 保护二极管
  - 额定值 > 4kV HBM
  - 额定值 > 2kV CDM
- 无铅且无卤素
- 符合 RoHS 标准

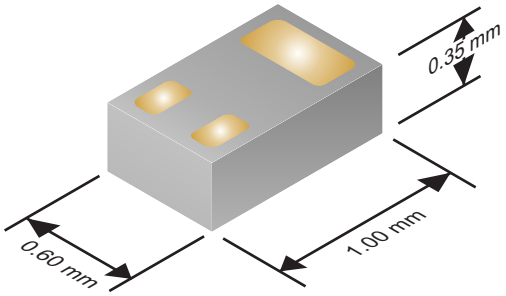
2 应用

- 针对负载开关应用 进行了优化
- 针对通用开关应用进行了 优化
- 单节电池 应用
- 手持式和移动类 应用

3 说明

这款 200mΩ、30V N 沟道 FemtoFET™MOSFET 技术经过特别设计和优化，能够在许多手持式和移动应用中最大限度地减小 占用空间。这项技术能够在替代标准小信号 MOSFET 的同时将封装尺寸减小至少 60%。

典型部件尺寸



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	总栅极电荷 (4.5V)	1010		pC
Q_{gd}	栅极电荷（栅极到漏极）	130		pC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 1.8V	370	mΩ
		V_{GS} = 2.5V	240	
		V_{GS} = 4.5V	200	
$V_{GS(th)}$	阈值电压	0.85		V

器件信息(1)

器件	数量	包装介质	封装	配送
CSD17483F4	3000	7 英寸卷带	Femto(0402) 1.00mm × 0.60mm SMD 无引线	卷带
CSD17483F4T	250			

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

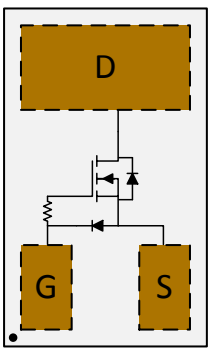
绝对最大额定值

T_A = 25°C 时测得，除非另外注明		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	12	V
I_D	持续漏极电流，T_A = 25°C 时测得(1)	1.5	A
I_{DM}	脉冲漏极电流，T_A = 25°C(2)	5	A
I_G	持续栅极钳位电流	35	mA
	脉冲栅极钳位电流(2)	350	
P_D	功率耗散(1)	500	mW
$V_{(ESD)}$	人体模型 (HBM)	4	kV
	带电器件模型 (CDM)	2	
T_J、T_{stg}	运行结温、贮存温度	–55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 7.4A，L = 0.1mH，R_G = 25Ω	2.7	mJ

(1) 典型 $R_{\theta JA}$ = 90°C/W（当在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上将其安装在 1 平方英寸 (6.45cm²)、2oz (0.071mm) 厚的铜焊盘上时）。

(2) 脉冲持续时间 ≤ 300μs，占空比 ≤ 2%.

顶视图



目录

4 修订历史记录

Changes from Revision D (Decermber 2016) to Revision E — **Page**

- Raised I_{DSS} Test Condition Voltage ... 3
- Raised I_{GSS} Test Condition Voltage ... 3

Changes from Revision C (September 2014) to Revision D — **Page**

- 已添加 在*器件和文档支持* 部分*接收文档更新通知* ... 7
- 已添加 在*器件和文档支持* 部分*社区资源* ... 7
- 在*推荐的模版布局* 部分中更新了所有机械制图，并增加了焊盘尺寸。 ... 8

Changes from Revision B (January 2014) to Revision C — **Page**

- Corrected timing V_{DS} to read 15 V ... 3

Changes from Revision A (November 2013) to Revision B — **Page**

- 添加了 I_G 参数 ... 1
- Lowered I_{DSS} limit ... 3
- Lowered I_{GSS} limit ... 3

Changes from Original (July 2013) to Revision A — **Page**

- 删除了大型卷带信息，添加了小型卷带信息 ... 1

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 μA	30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 24 V			100	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 10 V			50	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	0.65	0.85	1.10	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 1.8 V, I_{DS} =0.5 A		370	550	mΩ
		V_{GS} = 2.5 V, I_{DS} =0.5 A		240	310	
		V_{GS} = 4.5 V, I_{DS} = 0.5 A		200	260	
		V_{GS} = 8 V, I_{DS} = 0.5 A		185	240	
g_{fs}	Transconductance	V_{DS} = 15 V, I_{DS} = 0.5 A		2.4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		145	190	pF
C_{oss}	Output capacitance			42	55	pF
C_{rss}	Reverse transfer capacitance			2	3	pF
R_G	Series gate resistance			23		Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_{DS} = 0.5 A		1010	1300	pC
Q_{gd}	Gate charge gate-to-drain			130		pC
Q_{gs}	Gate charge gate-to-source			220		pC
$Q_{g(th)}$	Gate charge at V_{th}			145		pC
Q_{oss}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		1095		pC
$t_{d(on)}$	Turnon delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 0.5 A,R_G = 2 Ω		3.3		ns
t_r	Rise time			1.3		ns
$t_{d(off)}$	Turnoff delay time			10.6		ns
t_f	Fall time			3.4		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 0.5 A, V_{GS} = 0 V		0.73	0.9	V
Q_{rr}	Reverse recovery charge	V_{DS}= 15 V, I_F = 0.5 A, di/dt = 300 A/μs		1475		pC
t_{rr}	Reverse recovery time			5.5		ns

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	90	°C/W
	Junction-to-ambient thermal resistance(2)	250	

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

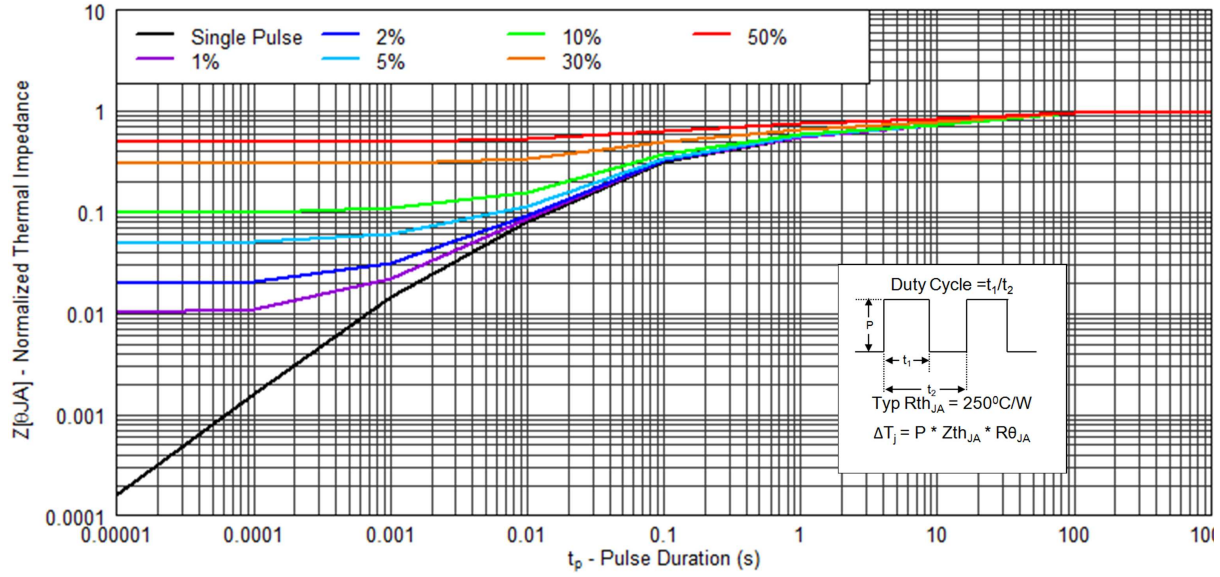


Figure 1. Transient Thermal Impedance

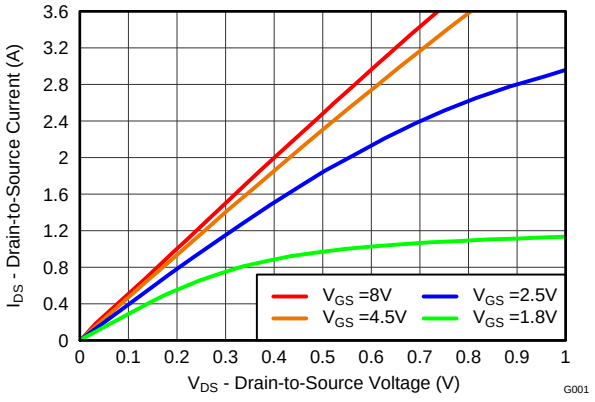


Figure 2. Saturation Characteristics

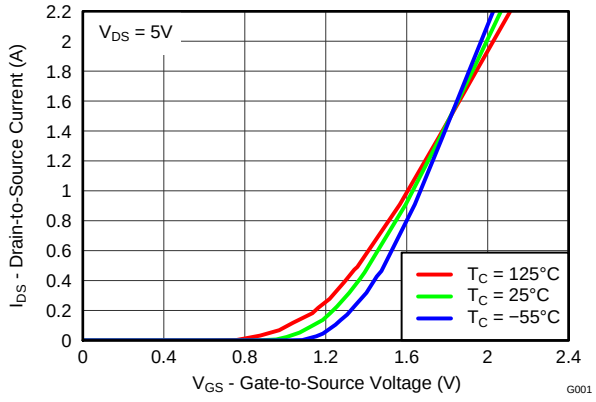


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

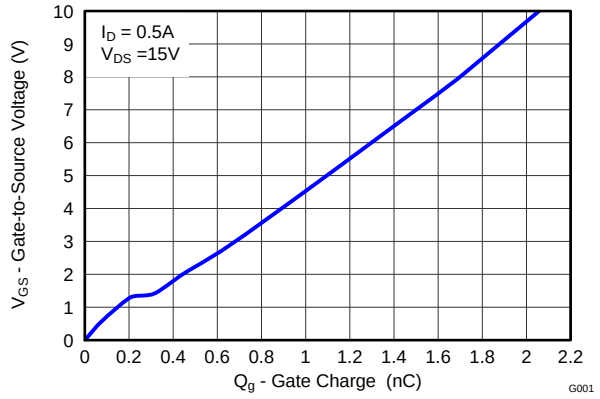


Figure 4. Gate Charge

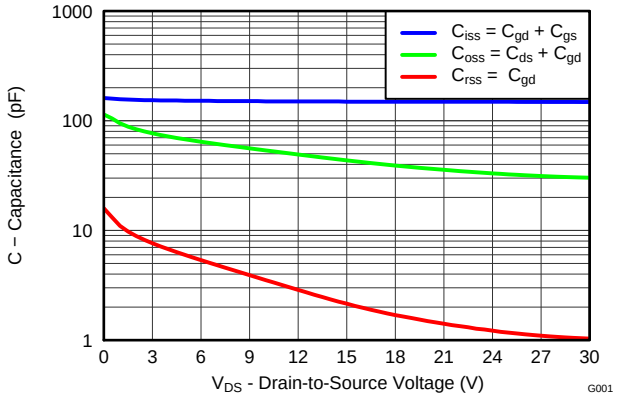


Figure 5. Capacitance

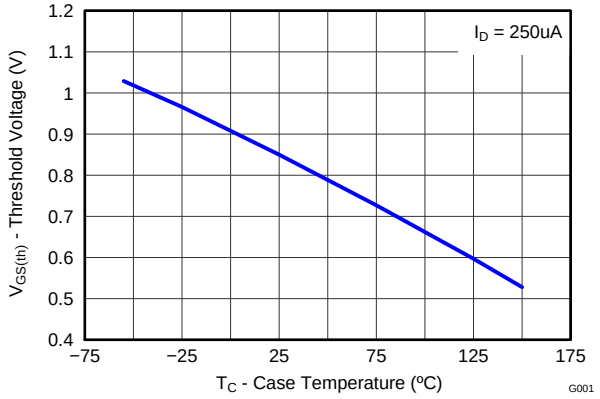


Figure 6. Threshold Voltage vs Temperature

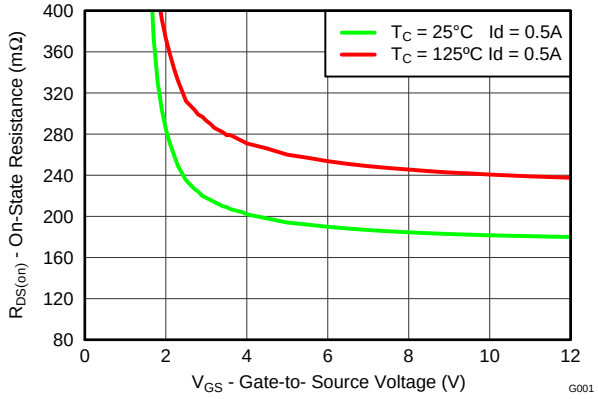


Figure 7. On-State Resistance vs Gate-to-Source Voltage

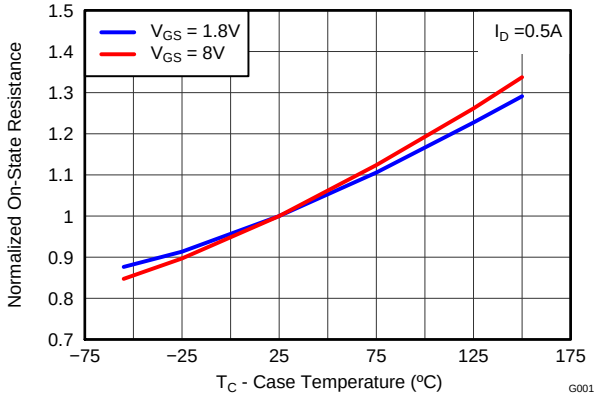


Figure 8. Normalized On-State Resistance vs Temperature

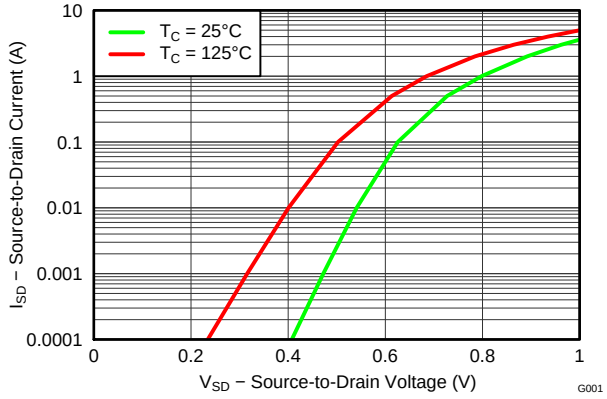


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

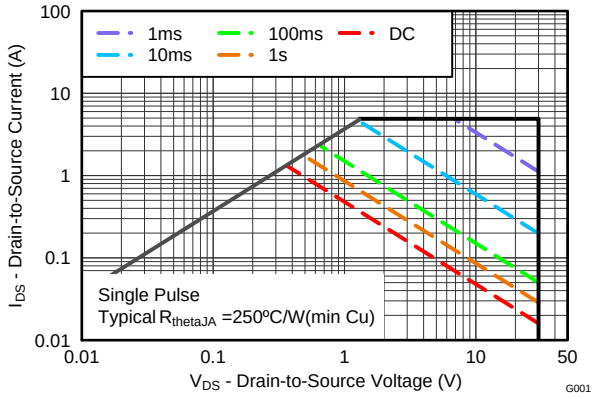


Figure 10. Maximum Safe Operating Area

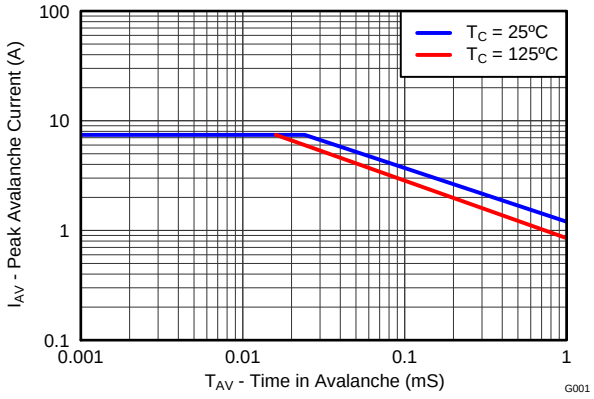


Figure 11. Single Pulse Unclamped Inductive Switching

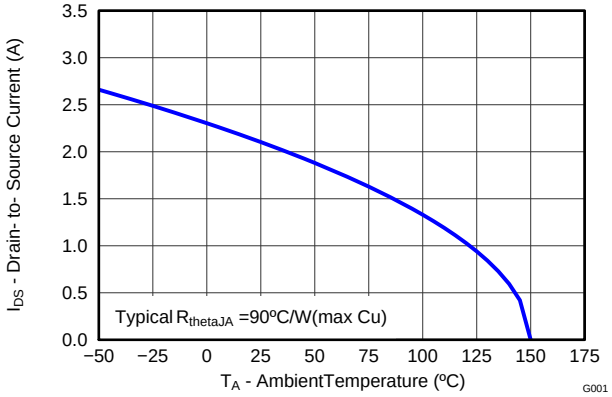


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

6.3 商标

FemtoFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 术语表

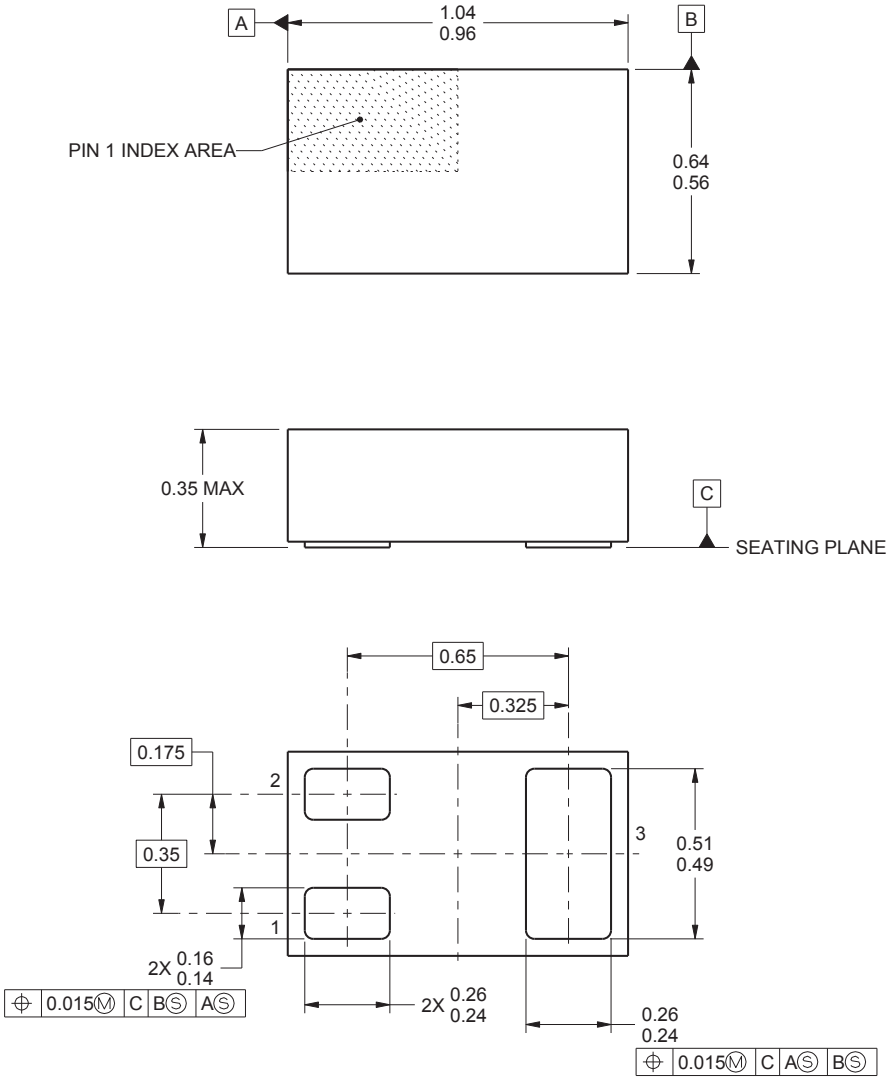
SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查看左侧的导航栏。

7.1 机械尺寸

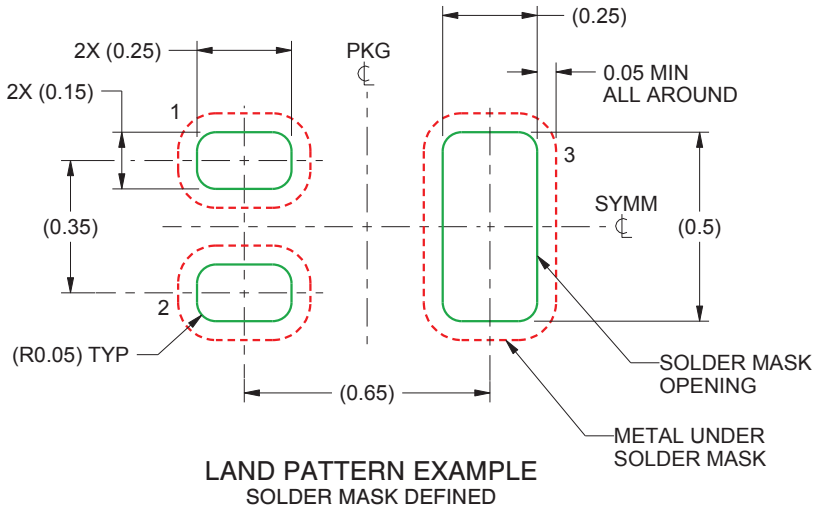


(1) 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。

(2) 本图如有变更，恕不另行通知。

(3) 此封装为无铅凸点设计。凸点涂料可能有所不同。要确定确切的涂料，请参阅器件产品说明书或联系当地的 TI 代表。

7.2 建议的最小 PCB 布局

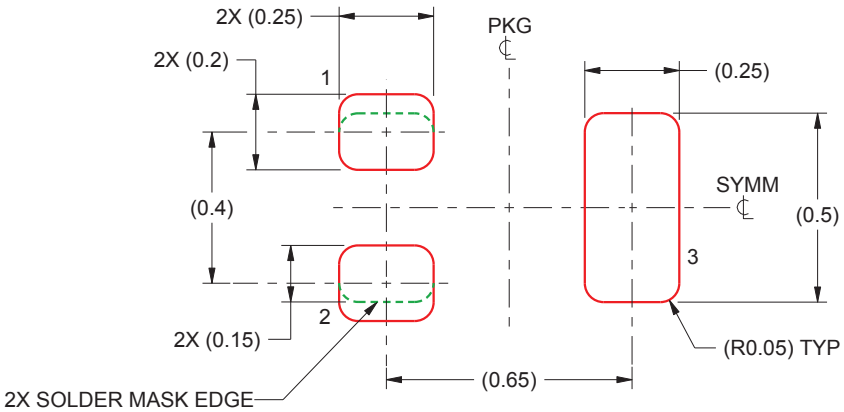


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED

(1) 所有尺寸的单位均为毫米。

(2) 有关更多信息，请参阅《*QFN/SON PCB 连接*》(SLUA271)。

7.3 推荐的模版布局



SOLDER PASTE EXAMPLE

(1) 所有尺寸的单位均为毫米。

(2) 具有漏斗形壁和圆角的激光切割孔可提供更佳的锡膏脱离。IPC-7525 可能提供替代设计建议。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17483F4	ACTIVE	PICOSTAR	YJC	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	DP	Samples
CSD17483F4T	ACTIVE	PICOSTAR	YJC	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	DP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

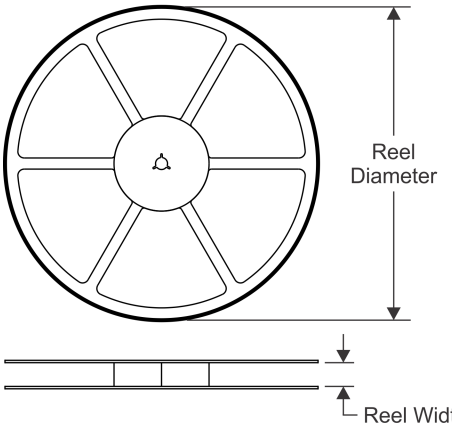
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

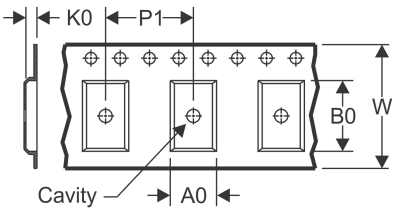
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

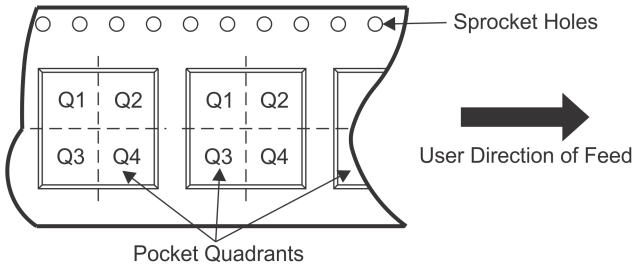


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

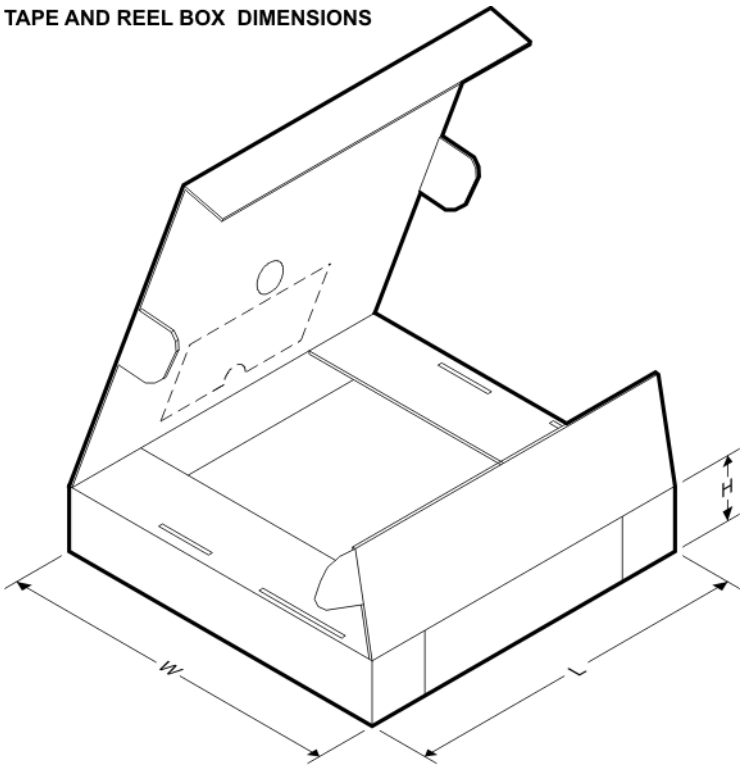
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17483F4	PICOSTAR	YJC	3	3000	178.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD17483F4	PICOSTAR	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD17483F4T	PICOSTAR	YJC	3	250	178.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD17483F4T	PICOSTAR	YJC	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17483F4	PICOSTAR	YJC	3	3000	220.0	220.0	35.0
CSD17483F4	PICOSTAR	YJC	3	3000	182.0	182.0	20.0
CSD17483F4T	PICOSTAR	YJC	3	250	220.0	220.0	35.0
CSD17483F4T	PICOSTAR	YJC	3	250	182.0	182.0	20.0

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