LMP7300 Micropower Precision Comparator and Precision Reference With Adjustable Hysteresis

1 Features

- (For V_S = 5 V, typical unless otherwise noted)
- Supply Current 13 µA
- Propagation Delay 4 µs
- Input Offset Voltage 0.3 mV
- CMRR 100 dB
- PSRR 100 dB
- Positive and Negative Hysteresis Control
- Adjustable Hysteresis 1 mV/mV
- Reference Voltage 2.048 V
- Reference Voltage Accuracy 0.25%
- Reference Voltage Source Current 1 mA
- Wide Supply Voltage Range 2.7 V to 12 V
- Operating Temperature Range Ambient −40°C to 125°C

2 Applications

- Precision Threshold Detection
- Battery Monitoring
- Battery Management Systems
- Zero Crossing Detectors

3 Description

The LMP7300 is a combination comparator and reference with ideal specifications for precision threshold detecting. The precision 2.048-V reference comes with a 0.25% maximum error. The comparator features micropower (35 µW), low offset voltage (0.75-mV maximum), and independent adjustable positive and negative hysteresis.

Hysteresis control for the comparator is accomplished through two external pins. The HYSTP pin sets the positive hysteresis, and the HYSTN pin sets the negative hysteresis. The comparator design isolates the V_{IN} source impedance and the programmable hysteresis components. This isolation prevents any undesirable interaction allowing the IC to maintain a precise threshold voltage during level detection.

The combination of low offset voltage, external hysteresis control, and precision voltage reference provides an easy-to-use micropower precision threshold detector.

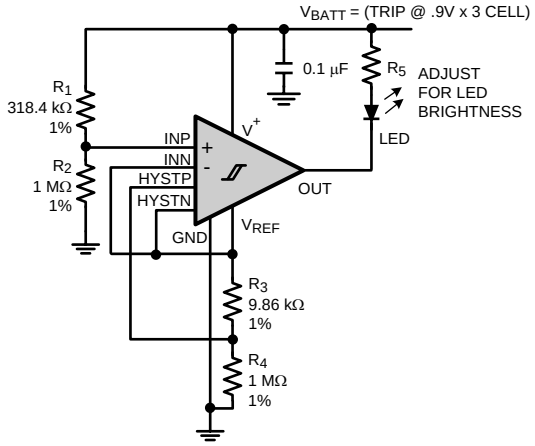
The LMP7300 open collector output is ideal for mixed-voltage system designs. The output voltage upper rail is unconstrained by V_{CC} and can be pulled above V_{CC} to a maximum of 12 V. The LMP7300 is a member of the LMP precision amplifier family.

Device Information(1)

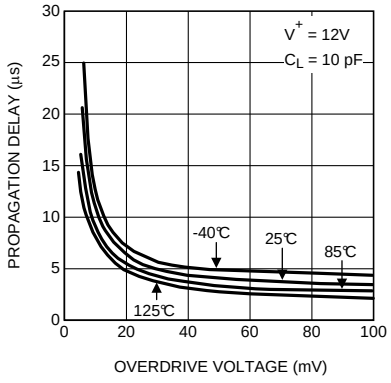
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMP7300	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	3.91 mm × 4.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



Propagation Delay vs Overdrive Voltage



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2013) to Revision G **Page**

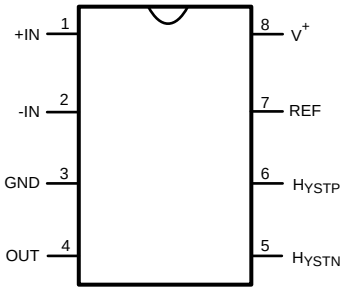
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision E (March 2013) to Revision F **Page**

- Changed layout of National Data Sheet to TI format ... 19

5 Pin Configuration and Functions

DGK or D Package
8-Pin VSSOP or SOIC
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
+IN	1	I	Noninverting Comparator Input. The +IN has a common-mode voltage range from 1 V above the negative rail to, and including, the positive rail. Internal ESD diodes, connected from the +IN pin to the rails, protect the input stage from overvoltage. If the input voltage exceeds the rails, the diodes turn on and clamp the input to a safe level.
-IN	2	I	Inverting Comparator Input. The −IN has a common-mode voltage range from 1 V above the negative rail to, and including, the positive rail. Internal ESD diodes, connected from the −IN pin to the rails, protects the input stage from overvoltage. If the input voltage exceeds the rails, the diodes turn on and clamp the input to a safe level.
GND	3	G	Ground. This pin may be connected to a negative DC voltage source for applications requiring a dual supply. If connected to a negative supply, decouple this pin with 0.1-µF ceramic capacitor to ground. The internal reference output voltage is referenced to this pin. GND is the die substrate connection.
OUT	4	O	Comparator Output. The output is an open-collector. It can drive voltage loads by using a pullup resistor, or it can drive current loads by sinking a maximum output current. This pin may be taken to a maximum of +12 V with respect to the ground pin, irrespective of supply voltage.
HYSTN	5	I	Negative Hysteresis pin. This pin sets the lower trip voltage V_{IL}. The common mode range is from 1V above the negative rail to V_{CC}. The input signal must fall below V_{IL} for the comparator to switch from high to low state.
HYSTP	6	I	Positive Hysteresis pin. This pin sets the upper trip voltage V_{IH}. The common mode range is from 1V above the negative rail to V_{CC}. The input signal must rise above V_{IH} for the comparator to switch from low to high state.
REF	7	O	Reference Voltage Output pin. This is the output pin of a 2.048-V band gap precision reference.
V^+	8	P	Positive Supply Terminal. The supply voltage range is 2.7 V to 12 V. Decouple this pin with 0.1-µF ceramic capacitor to ground.

(1) P= Power, G=Ground, I=Input, O=Output, A=Analog

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{IN} differential			$\pm V_S$	V
Supply voltage ($V_S = V^+ - V^-$)			13.6	V
Voltage at input/output pins		$V^+ + 0.3$	$V^- - 0.3$	V
Soldering information	Infrared or convection (20 s)		235	°C
	Wave soldering lead temperature (10 s)		260	°C
Junction temperature, T_J(3)			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
Temperature(2)	–40		125	°C
Supply Voltage ($V_S = V^+ - V^-$)	2.7		12	V

(1) *Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.*
(2) The maximum power dissipation is a function of TJ(MAX), θJA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(MAX) – TA)/θJA. All numbers apply for packages soldered directly onto a PC Board.

6.4 Thermal Information

THERMAL METRIC(1)		LMP7300		UNIT
		DGK (VSSOP)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	175.5	121.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.1	67.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	95.6	61.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10	18.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	94.2	61	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953..
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

6.5 Electrical Characteristics: 2.7-V

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 2.7 V, V^- = 0 V, and V_{CM} = V^+/2, R_{PULLUP} = 100 kΩ, C_{LOAD} = 10 pF.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Supply Current	R_{PULLUP} = Open	T_A = 25°C		9	12	µA
			T_J = T_A			17	
COMPARATOR							
V_{OS}	Input Offset Voltage	V_{CM} = V^+/2 SOIC	T_A = 25°C		±0.07	±0.75	mV
			T_J = T_A			±2	
		V_{CM} = V^+/2 VSSOP	T_A = 25°C		±0.07	±1	mV
			T_J = T_A			±2.2	
TCV_{OS}	Input Offset Average Drift	See(1)			1.8		µV/°C
I_B	Input Bias Current(2)	$\|V_{ID}\|$ < 2.5 V	T_A = 25°C		1.2	3	nA
			T_J = T_A			4	
I_{OS}	Input Offset Current				0.15	0.5	nA
CMRR	Common Mode Rejection Ratio	1 V < V_{CM} < 2.7 V		80	100		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7 V to 12 V		80	100		dB
V_{OL}	Output Low Voltage	I_{LOAD} = 10 mA	T_A = 25°C		0.25	0.4	V
			T_J = T_A			0.5	
I_{LEAK}	Output Leakage Current	Comparator Output in High State			1		pA
HC_{LIN}	Hysteresis Control Voltage Linearity	0 < Ref-H_{YS}TP,N < 25 mV			1		mV/V
		25 mV < Ref-H_{YS}TP,N < 100 mV			0.950		
I_{HYS}	Hysteresis Leakage Current	T_A = 25°C			1.2	3	nA
		T_J = T_A				4	
T_{PD}	Propagation Delay (High to Low)	Overdrive = 10 mV, C_L = 10 pF			12	17	µs
		Overdrive = 100 mV, C_L = 10 pF			4.5	7.6	
REFERENCE							
V_O	Reference Voltage	SOIC		2.043	2.048	2.053	V
		VSSOP		2.043	2.048	2.056	V
	Line Regulation	V_{CC} = 2.7 V to 12 V			14	80	µV/V
	Load Regulation	I_{OUT} = 0 to 1 mA			0.2	0.5	mV/mA
$TCV_{REF/°C}$	Temperature Coefficient	−40°C to 125°C				55	ppm/°C
V_N	Output Noise Voltage	0.1 Hz to 10 Hz			80		$µV_{PP}$
		10 Hz to 10 kHz			100		$µV_{RMS}$

(1) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes, by the total temperature change.
(2) Positive current corresponds to current flowing into the device.

6.6 Electrical Characteristics: 5-V

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5 V, V^- = 0 V, and V_{CM} = V^+/2, R_{PULLUP} = 100 kΩ, C_{LOAD} = 10 pF. (1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
I_S	Supply Current	R_{PULLUP} = Open	T_A = 25°C		10	13	µA
			T_J = T_A			18	
COMPARATOR							
V_{OS}	Input Offset Voltage	V_{CM} = V^+/2 SOIC	T_A = 25°C		±0.07	±0.75	mV
			T_J = T_A			±2	
		V_{CM} = V^+/2 VSSOP	T_A = 25°C		±0.07	±1	mV
			T_J = T_A			±2.2	
TCV_{OS}	Input Offset Average Drift	See(4)			1.8		µV/°C
I_B	Input Bias Current(5)	$\|V_{ID}\|$ < 2.5 V	T_A = 25°C		1.2	3	nA
			T_J = T_A			4	
I_{OS}	Input Offset Current				0.15	0.5	nA
CMRR	Common Mode Rejection Ratio	1 ≤ V_{CM} ≤ 5 V		80	100		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7 V to 12 V		80	100		dB
V_{OL}	Output Voltage Low	I_{LOAD} = 10 mA			0.25	0.4	V
I_{LEAK}	Output Leakage Current	Comparator Output in High State			1		pA
HC_{LIN}	Hysteresis Control Voltage Linearity	0 < Ref-V_{HYS}TP,N < 25 mV			1		mV/V
		25 mV < Ref-V_{HYS}TP,N < 100 mV			0.950		
I_{HYS}	Hysteresis Leakage Current	T_A = 25°C			1.2	3	nA
		T_J = T_A				4	
TPD	Propagation Delay (High to Low)	Overdrive = 10 mV, C_L = 10 pF			12	15	µs
		Overdrive = 100 mV, C_L = 10 pF			4	7	
REFERENCE							
V_O	Reference Voltage	SOIC		2.043	2.048	2.053	V
		VSSOP		2.043	2.048	2.056	V
	Line Regulation	V_{CC} = 2.7 V to 12 V			14	80	µV/V
	Load Regulation	I_{OUT} = 0 to 1 mA			0.2	0.5	mV/mA
$TCV_{REF/°C}$	Temperature Coefficient	−40°C to 125°C				55	ppm/°C
V_N	Output Noise Voltage	0.1 Hz to 10 Hz			80		$µV_{PP}$
		10 Hz to 10 kHz			100		$µV_{RMS}$

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes, by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

6.7 Electrical Characteristics: 12-V

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 12 V, V^- = 0 V, and V_{CM} = V^+/2, R_{PULLUP} = 100 kΩ, C_{LOAD} = 10 pF. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Supply Current	R_{PULLUP} = Open	T_A = 25°C		11	14	µA
			T_J = T_A			20	
COMPARATOR							
V_{OS}	Input Offset Voltage	V_{CM} = V^+/2 SOIC	T_A = 25°C		±0.08	±0.75	mV
			T_J = T_A			±2	
		V_{CM} = V^+/2 VSSOP	T_A = 25°C		±0.08	±1	mV
			T_J = T_A			±2.2	
TCV_{OS}	Input Offset Average Drift	See (2)			1.8		µV/°C
I_B	Input Bias Current (3)	$\|V_{ID}\|$ > 2.5 V	T_A = 25°C		1.2	3	nA
			T_J = T_A			4	
I_{OS}	Input Offset Current				0.15	0.5	nA
CMRR	Common Mode Rejection Ratio	1 V ≤ V_{CM} ≤ 12 V		80	100		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7 V to 12 V		80	100		dB
V_{OL}	Output Voltage Low	I_{LOAD} = 10 mA			0.25	0.4	V
I_{LEAK}	Output Leakage Current	Comparator Output in High State			1		pA
HC_{LIN}	Hysteresis Control Voltage Linearity	0 < Ref-V_{+HYS}TP, N < 25 mV			1		mV/V
		25 mV < Ref-V_{+HYS}TP, N < 100 mV			0.95		
I_{HYS}	Hysteresis Leakage Current	T_A = 25°C			1.2	3	nA
		T_J = T_A				4	
TPD	Propagation Delay (High to Low)	Overdrive = 10 mV, C_L = 10 pF			11	15	µs
		Overdrive = 100 mV, C_L = 10 pF			3.5	6.8	
REFERENCE							
V_O	Reference Voltage	T_J = 25°C SOIC		2.043	2.048	2.053	V
		T_J = 25°C VSSOP		2.043	2.048	2.056	V
	Line Regulation	V_{CC} = 2.7 V to 12 V			14	80	µV/V
	Load Regulation	I_{OUT} = 0 to 1 mA			0.2	0.5	mV/mA
$TCV_{REF/°C}$	Temperature Coefficient	−40°C to 125°C				55	ppm/°C
V_N	Output Noise Voltage	0.1 Hz to 10 Hz			80		$µV_{PP}$
		10 Hz to 10 kHz			100		$µV_{RMS}$

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes, by the total temperature change.
(3) Positive current corresponds to current flowing into the device.

6.8 Typical Characteristics

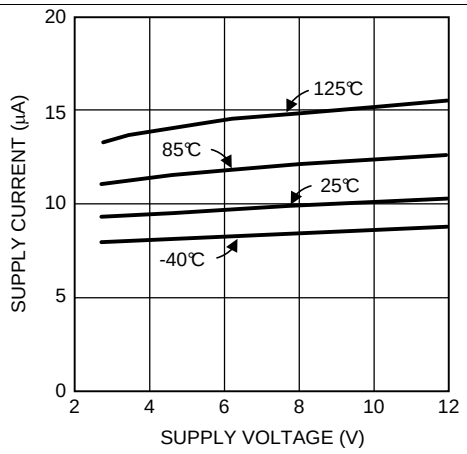


Figure 1. Supply Current vs Supply Voltage

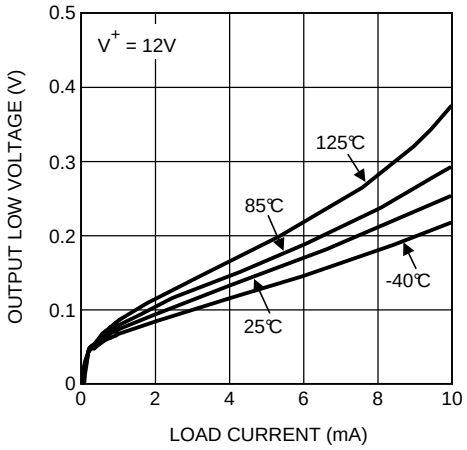


Figure 2. Output Low Voltage vs Load Current

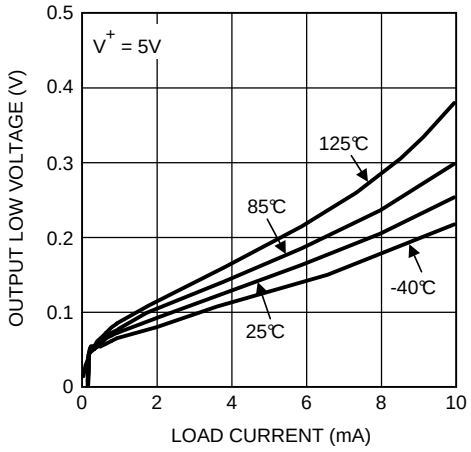


Figure 3. Output Low Voltage vs Load Current

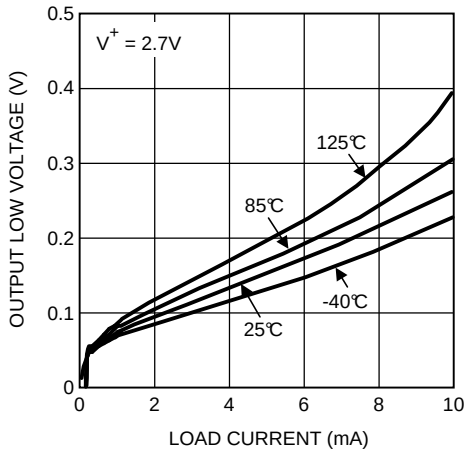


Figure 4. Output Low Voltage vs Load Current

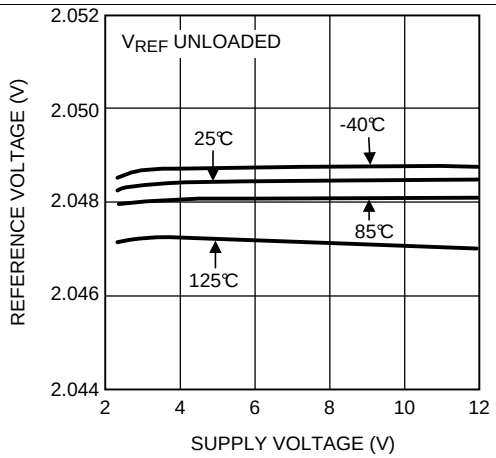


Figure 5. Reference Voltage vs Supply Voltage

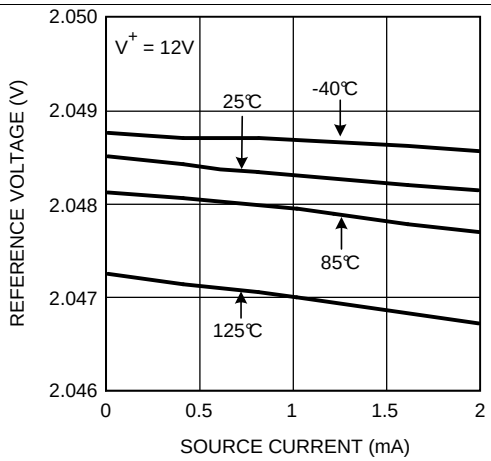


Figure 6. Reference Voltage vs Source Current

Typical Characteristics (continued)

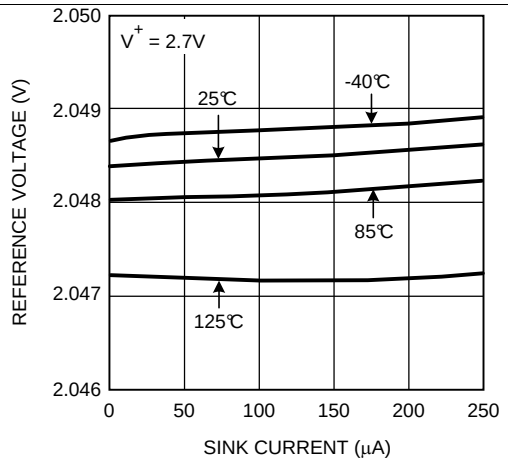


Figure 7. Reference Voltage vs Sink Current

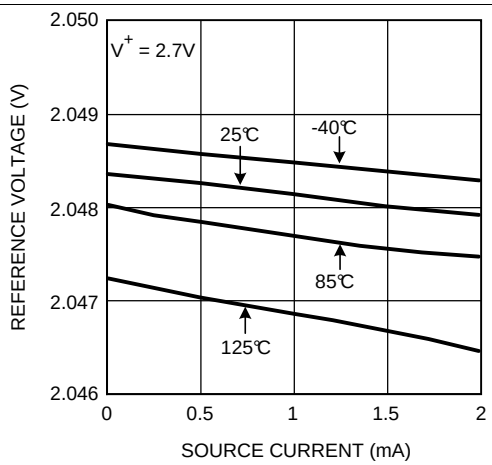


Figure 8. Reference Voltage vs Source Current

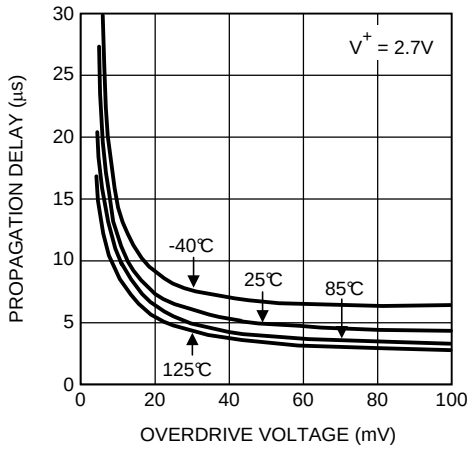


Figure 9. Propagation Delay vs Overdrive Voltage

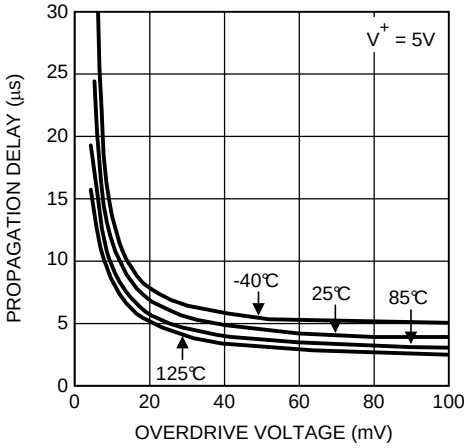


Figure 10. Propagation Delay vs Overdrive Voltage

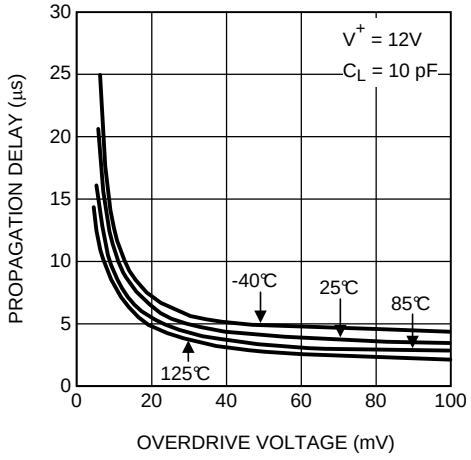


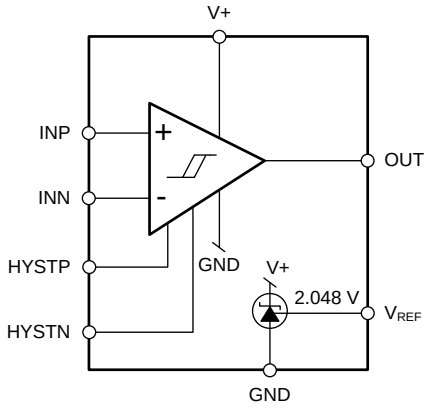
Figure 11. Propagation Delay vs Overdrive Voltage

7 Detailed Description

7.1 Overview

The LMP7300 device is a unique combination of micropower and precision. The open collector comparator has low offset, high CMRR, high PSRR, programmable hysteresis and microamp supply current. The precision 2.048-V reference provides a DAC or ADC with an accurate binary divisible voltage. The comparator and reference combination forms an ideal single IC solution for low power sensor or portable applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Voltage Reference

The reference output voltage is a band gap derived 2.048 V that is trimmed to achieve typically 0.2% accuracy over the full operating temperature range of −40°C to 125°C. The trim procedure employs a curvature correction algorithm to compensate for the base emitter thermal nonlinearity inherent in band gap design topologies. The reference accuracy and the set resistor tolerance determine the magnitude and precision of the programmable hysteresis. In situations where reference noise filtering is required, TI recommends a 5-µF capacitor in series with a 190-Ω resistor to ground.

7.3.2 Comparator

7.3.2.1 Output Stage

The comparator employs an open collector output stage that can switch microamp loads for micropower precision threshold detection to applications requiring activating a solenoid, a lamp, or an LED. The wired-OR type output easily interfaces to TTL, CMOS, or multiple outputs, as in a window comparator application, over a range of 0.5 V to 12 V. The output is capable of driving greater than 10-mA output current and yet maintaining a saturation voltage less than 0.4 V over temperature. The supply current increases linearly when driving heavy loads, so TI recommends a pullup resistor of 100 kΩ or greater for micropower applications.

7.3.2.2 Fault Detection Rate

The user's choice of a pullup resistor and capacitive load determines the minimum response time and the event detection rate. By optimizing overdrive, the pullup resistor and capactive load fault update rates of 200 kHz to 250 kHz or greater can be achieved.

Feature Description (continued)

7.3.3 Hysteresis

False triggering on noise coupled into the signal path is a common problem for comparator based threshold detectors. One of the most effective solutions is to add hysteresis. Hysteresis is a circuit signal path characteristic where an amplitude delay is introduced to the normal input. Positive hysteresis forces the signal to pass the normal switch point before the output makes a low to high transition while negative hysteresis does the opposite. This is a memory effect. The comparator behaves differently based on which direction the signal is going.

The LM7300 has been designed with a unique way of introducing hysteresis. The set points are completely independent of each other, the power supply, and the input or output conditions. The HYSTP pin sets positive hysteresis and the HYSTN pin sets the negative hysteresis in a simple way using two resistors. The pins can be tied together for the same hysteresis or tied to separate voltage taps for asymmetric hysteresis, or tied to the reference for no hysteresis. When the precision reference is used to drive the voltage tap resistor divider precise, stable threshold levels can be obtained. The maximum recommended hysteresis is about 130 mV. This places the HYSTP and HYSTN pin voltages at V_{REF} – 130 mV, which is approximately the center of their input common mode range at 2.7 V. For the typical example, a differential input signal voltage, V_{IN}, is applied between INP and INN, the noninverting and inverting inputs of the comparator. A DC switch or threshold voltage, V_{TH}, is set on the negative input to keep the output off when the signal is above and on when it goes below this level. For a precision threshold tie the INN pin to V_{REF}. With the output, off the circuit is in the minimum power state. Figure 13 through Figure 21 demonstrate the different configurations for setting the upper threshold V_{IH} and the lower threshold V_{IL} and their relationship to the input trip point V_{REF}, by the following formulas.

$$V_{IL} = V_{REF} - V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)$$
$$V_{IH} = V_{REF} + V_{REF}\left(\frac{R_1}{R_1 + R_2}\right) \quad (1)$$

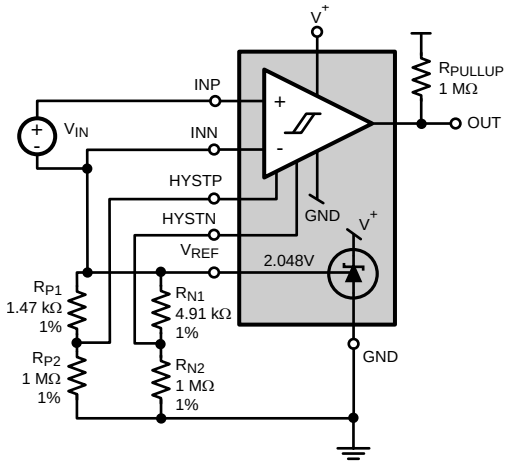


Figure 12. Typical Micropower Application to Set Asymmetric Positive and Negative Hysteresis of −10 mV, 3 mV

Feature Description (continued)

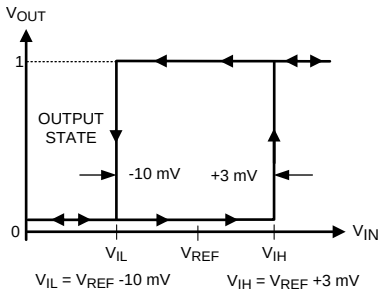


Figure 13. Typical Micropower Application to Set Asymmetric Positive and Negative Hysteresis of −10 mV, 3 mV

When V_{ID} = 0, INN = INP = V_{TH}

Figure 15 shows the configuration with no hysteresis when the HYSTP and HYSTN pins are connected together to V_{REF}. TI does not recommend this configuration because it has the highest level of false triggers due to the system noise.

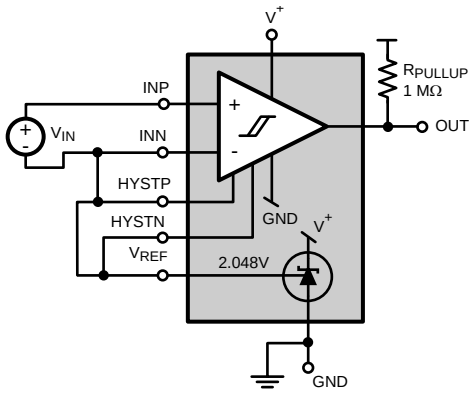


Figure 14. Typical Configuration for No Hysteresis

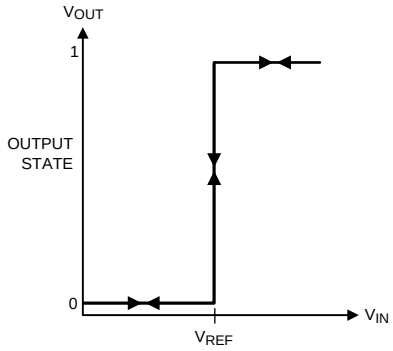


Figure 15. Typical Configuration for No Hysteresis

Figure 17 shows the configuration with symmetric hysteresis when the HYSTP and HYSTN pins are connected to the same voltage that is less than V_{REF}. The two trip points set a hysteresis band around the input threshold voltage V_{REF}, such that the positive band is equal to the negative band.

This configuration controls the false triggering mentioned in Figure 15. For precise level detection applications, TI recommends symmetric hysteresis values less than 5 mV to 10 mV.

Feature Description (continued)

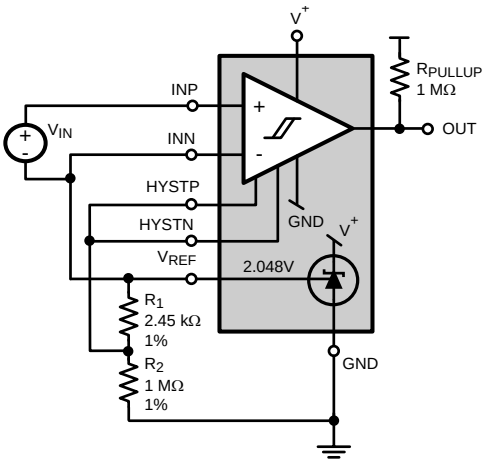


Figure 16. Symmetric Hysteresis ±5 mV

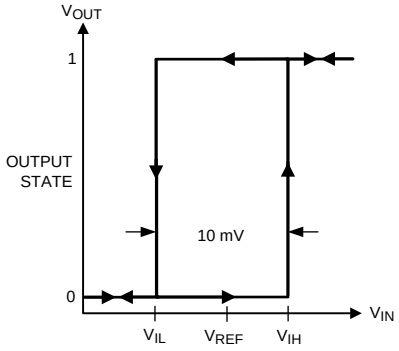


Figure 17. Symmetric Hysteresis ±5 mV

Figure 19 shows the case for negative hysteresis by biasing only the HYSN pin to a voltage less than V_{REF}.

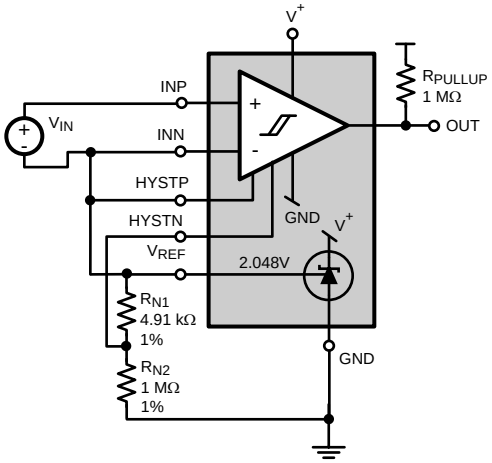


Figure 18. Typical Configuration for Negative Hysteresis = −10 mV

Feature Description (continued)

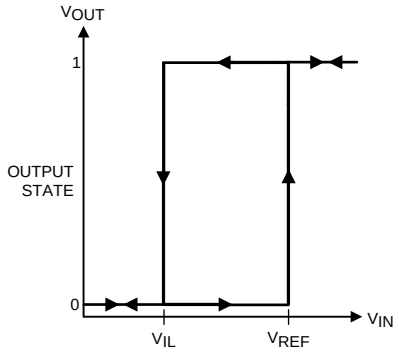


Figure 19. Typical Configuration for Negative Hysteresis = −10 mV

The case for setting only a positive hysteresis is demonstrated in Figure 21.

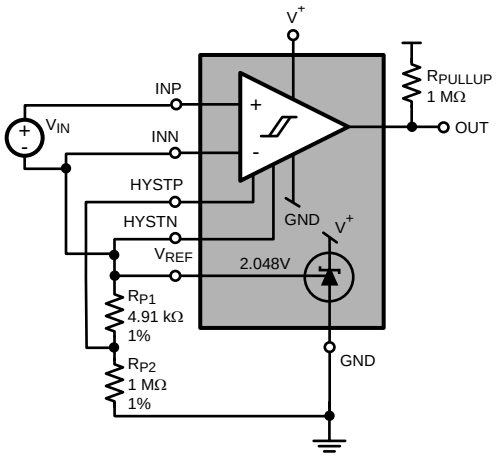


Figure 20. Connections for Positive Hysteresis = 10 mV

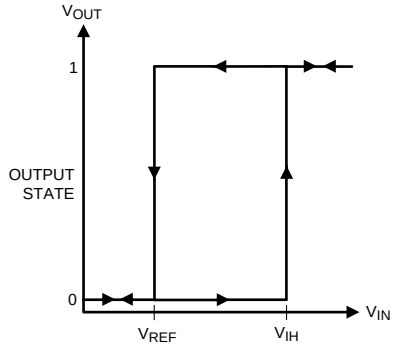


Figure 21. Connections for Positive Hysteresis = 10 mV

In the general case, as demonstrated with both positive and negative hysteresis bands in Figure 22, noise within these bands has no effect on the state of the comparator output. In Example 1 the noise is well behaved and in band. The output is clean and well behaved. In Example 2, a significant amount of out of band noise is present; however, due to hysteresis no false triggers occur on the rising positive or falling negative edges. The hysteresis forces the signal level to move higher or lower before the output is set to the opposite state.

Feature Description (continued)

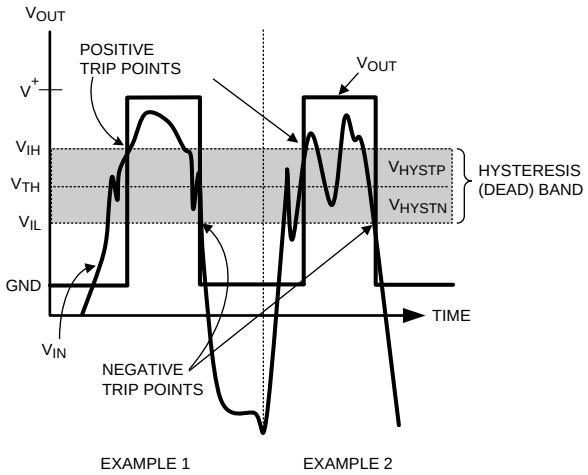


Figure 22. Output Response With Input Noise Less than Hysteresis Band

7.3.3.1 How Much Hysteresis Is Correct?

An effective way of determining the minimum hysteresis necessary for clean switching is to decrease the amount of hysteresis until false triggering is observed, and then use a multiple of say three times that amount of hysteresis in the final circuit. This is most easily accomplished in the breadboard phase by making R_1 and R_2 potentiometers. For applications near or above 100°C, TI recommends a minimum of 5-mV hysteresis due to peaking of the LMP7300 noise sensitivity at high temperatures.

7.4 Device Functional Modes

The LMP7300 device may be used as a voltage reference or as a comparator with HIGH and LOW output states. A LOW output will occur when the noninverting input (INP) is less than the inverting input (INN). A HIGH output will occur when the noninverting input (INP) is greater than the inverting input (INN).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMP7300 device may be used in a variety of applications including precision threshold detection, battery monitoring, battery management systems, and zero crossing detectors. The externally controlled hysteresis functionality allows the user to determine how robust the device is against noise and false triggering.

8.2 Typical Applications

8.2.1 Window Comparator

Figure 23 shows two LMP7300s configured as a micropower window detector in a temperature level detection application.

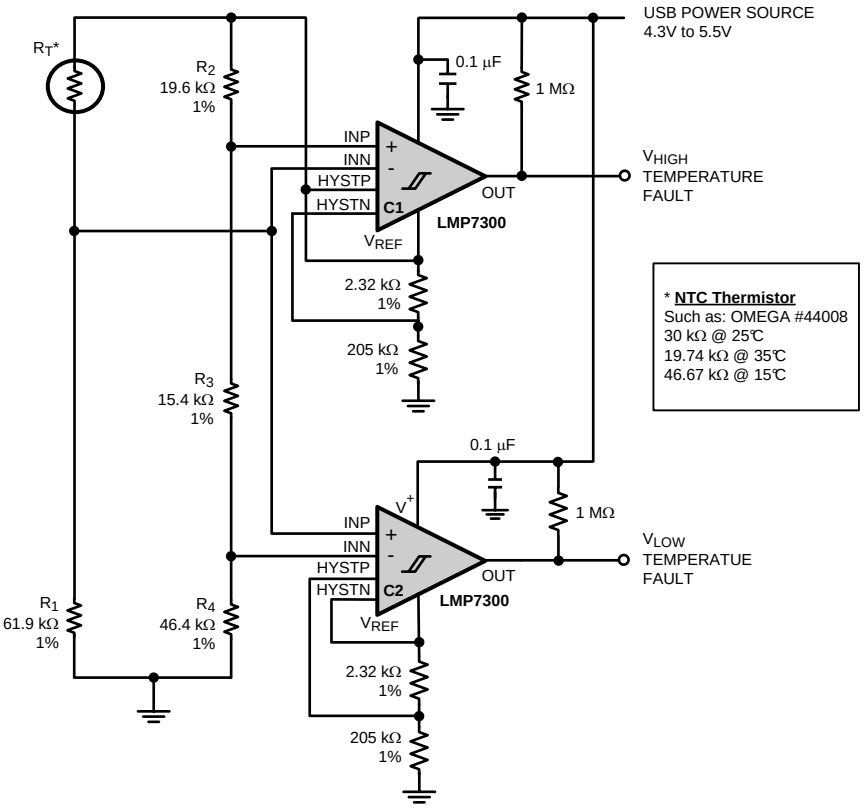


Figure 23. Temperature-Controlled Window Detector to Monitor Ambient Temperature

Typical Applications (continued)

8.2.1.1 Design Requirements

Figure 23 monitors the ambient temperature change. If the temperature rises outside the 15°C to 35°C window, either comparator 1 for high temperature, or comparator 2 for low temperature, sets low, indicating a fault condition has occurred. The open collector outputs are pulled up separately but can be wire-OR'd for a single fault indication. If the temperature returns inside the window, it must overcome the 22-mV asymmetric hysteresis band established on either comparator. For the high side, the temperature must drop below 34°C, and for the low side the temperature must rise above 16°C for the outputs to reset high and remove the fault indication. The temperature is sensed by a 30 kΩ @ 25°C Omega Precision NTC Thermistor #44008 (±0.2% tol).

8.2.1.2 Detailed Design Procedure

To set a fixed temperature threshold, the thermistor resistance (R_T*) must first be approximated at the specified temperatures. For a temperature of 35°C, R_T* =19.74 kΩ from Figure 23. A resistor divider with R_1 =61.9 kΩ and V_{REF} can be formed on INN of comparator 1 to set the high side tripping voltage according to Equation 1. An equivalent resistor divider must be formed on INP of comparator 1 by using the nearest 1% matching resistors of R_2=19.6 kΩ and a combination of R_3=15.4 kΩ and R_4=46.4 kΩ.

NOTE

a combination of resistors was chosen with R_4=46.4 kΩ to set the low side tripping threshold where R_T* = 46.67 kΩ at 15°C .

A similar technique can be applied for comparator 2 to set the low side temperature of 15°C. The total change in Volts can be computed by subtracting the two tripping thresholds to get a range of approximately 390 mV. Given a total temperature change of 20°C, the hysteresis should be set to 19.5 mV to give an equivalent hysteresis of 1°C. A hysteresis value of 22.9 mV is calculated through the resistor divider of V_{REF}, 2.32 kΩ, and 205 kΩ.

8.2.1.3 Application Curve

The results of the circuit shown in Figure 23 above can be plotted for various temperatures. A temperature change of ±100°C/hour was chosen to demonstrate the functionality. Figure 24 shows that when the temperature drops to 15°C the output of comparator 2 trips, which signifies a low temperature fault. When the temperature returns and crosses the 22-mV hysteresis, comparator 2 returns to its normally high-output state. Similarly, when the temperature reaches 35°C, comparator 1 trips and signifies a high temperature fault. When the temperature returns below the hysteresis, comparator 1 returns to its normally high-output state.

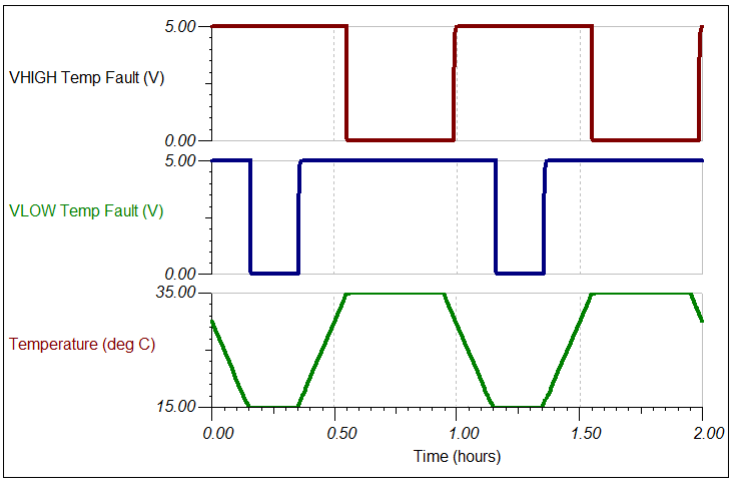


Figure 24. Window Detector Output Response

Typical Applications (continued)

8.2.2 Precision High-Temperature Switch

The LMP7300 brings accuracy and stability to simple sensor switch applications. Figure 26 shows the LMP7300 setup in a high temperature switch configuration. The input bridge is used to establish the temperature at which the LMP7300 will trip and the temperature at which it resets.

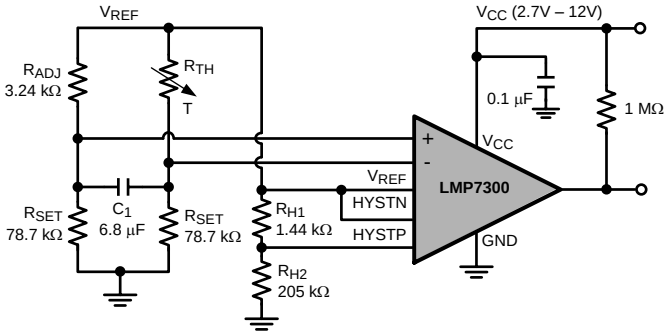


Figure 25. Precision High-Temperature Switch

8.2.2.1 Design Requirements

In Figure 25, the input bridge establishes the trip point at 85°C and the reset temperature at 80°C. The comparator is set up with positive hysteresis of 14.3 mV and no negative hysteresis. When the temperature is rising, it trips at 85°C. The 14.3-mV hysteresis allows the temperature to drop to 80°C before reset.

The temperature sensor used is an Omega 44008 Precision NTC Thermistor. The 44008 has an accuracy of ±0.2°C. The resistance at 85°C is 3270.9 Ω and at 80°C is 3840.2 Ω. The trip voltage threshold is established by one half of the bridge, which is the ratio of R_{ADJ} and R_{SET}. The input signal bias is set by the second half, which is the ratio of the thermistor resistance R_{TH} and R_{SET}. The resistance values are chosen for approximately 50-µA bridge current to minimize the power in the thermistor. The thermistor specification states it has a 1°C/mW dissipation error. The reference voltage establishes the supply voltage for the bridge to make the circuit independent of supply voltage variation. Capacitor C_1 establishes a low-frequency pole at $F_{CORNER} = 1/(2\pi C_1 \times 2(R_{SET}//R_{ADJ}))$. With the resistance values chosen C_1 should be selected for Fc < 10 Hz. This will limit the thermal noise in the bridge.

The accuracy of the circuit can be calculated from the nearest resistance values chosen. For 1% resistors RADJ is 3.24 kΩ, and R_{SET} is 78.7 kΩ. The bridge gain becomes 2.488 mV/C at 85°C. In general, the higher the bridge current is allowed to be, the higher the bridge gain will be. The actual trip point found during simulation is 85.3°C and the reset point is 80.04°C. With the values chosen the worst case trip temperature uncertainty is ±1.451°C and the reset uncertainty is ±1.548°C. Accuracy could be maximized with resistors chosen to 0.1% values, 0.1% tolerance and by using the 0.1% model of the Omega 44008 thermistor.

8.2.3 Micropower Precision-Battery Low-Voltage Detector

The ability of the LMP7300 device to operate at very low supply voltages makes it an ideal choice for low battery detection application in portable equipment. The circuit in Figure 26 performs the function of low voltage threshold detection in a battery monitor application.

Typical Applications (continued)

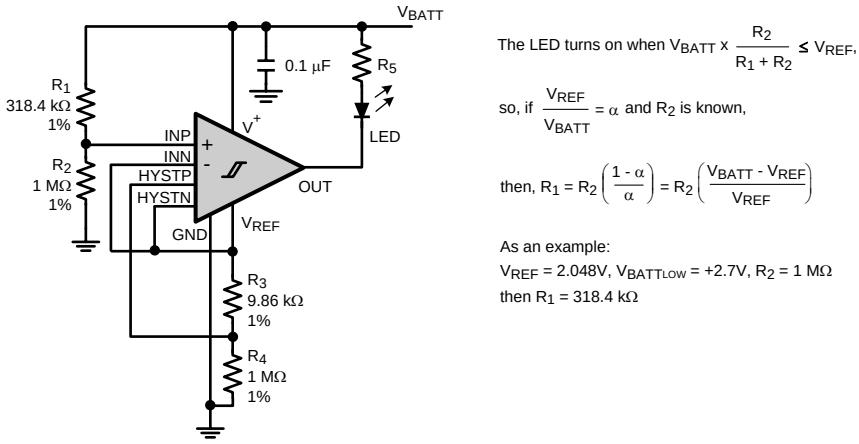


Figure 26. Battery Voltage Monitor for 3-Cell Discharge Voltage

8.2.3.1 Design Requirements

The circuit in Figure 26 is configured to detect the low voltage threshold detection in a 3 cell, 0.9-V discharge voltage, battery monitor application. R_1 and R_2 are chosen to set the inverting input voltage equal to the noninverting input voltage when the battery voltage is equal to the minimum operating voltage of the system. Here, the very precise reference output voltage is directly connected to the noninverting input on the comparator and sets an accurate threshold voltage. The hysteresis is set to 0-mV negative and 20-mV positive. The output is off for voltages higher than the minimum V_{BATT}, and turns on when the circuit detects a minimum battery voltage condition.

9 Power Supply Recommendations

Even in low-frequency applications, the LMP7300 can have internal transients which are extremely quick. For this reason, bypassing the power supply with 1-µF to ground will provide improved performance; the supply bypass capacitor should be placed as close as possible to the supply pin and have a solid connection to ground. The bypass capacitors should have a low ESR.

10 Layout

10.1 Layout Guidelines

A good PCB layout is always important to reduce output to input coupling. Positive feedback noise reduces performance. For the LMP7300, output coupling is minimized by the unique package pinout. The output is kept away from the noninverting and inverting inputs, the reference and the hysteresis pins.

10.2 Layout Example

The following section shows an example schematic and layout for the LMP7300MA 8-pin SOIC package.

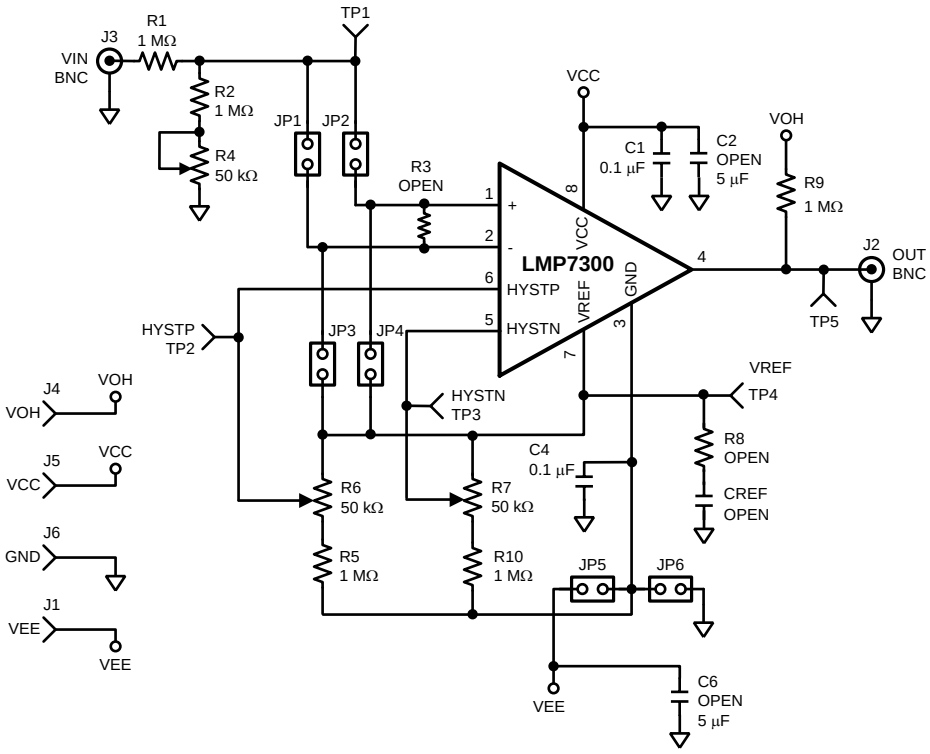


Figure 27. LMP7300MA-EVAL Schematic

Layout Example (continued)

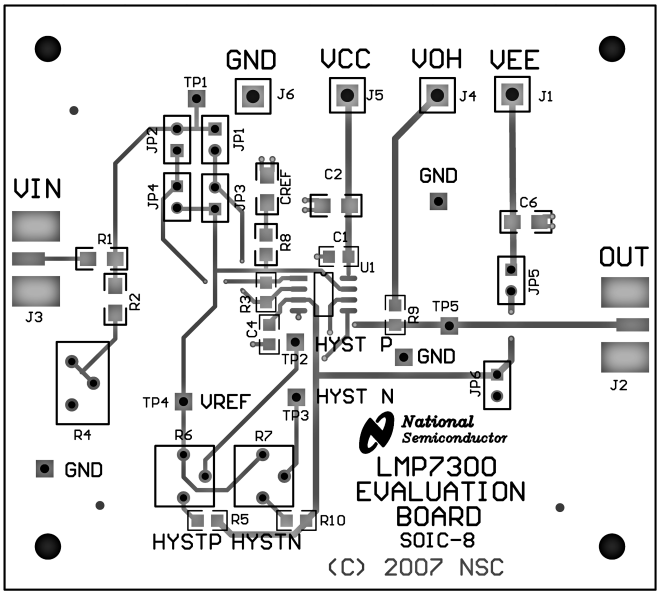


Figure 28. LMP7300MA-EVAL Layout Top View

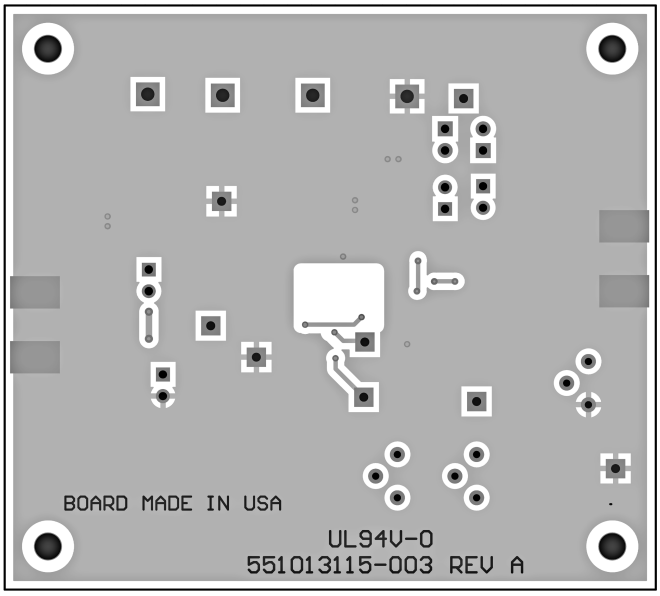


Figure 29. LMP7300MA-EVAL Layout Bottom View

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Boards

Texas Instruments provides the following PCB boards as an aid in evaluating the LMP7300 performance in the 8-pin SOIC package. For more information on the evaluation board, LMP7300MA-EVAL, of the LMP7300MA device option, see *AN-1639 LMP7300 Single Precision Comparator With Reference Evaluation Boards (SOIC and VSSOP)*, SNOA491.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP7300MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP73 00MA	Samples
LMP7300MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP73 00MA	Samples
LMP7300MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	C31A	Samples
LMP7300MME/NOPB	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	C31A	Samples
LMP7300MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	C31A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

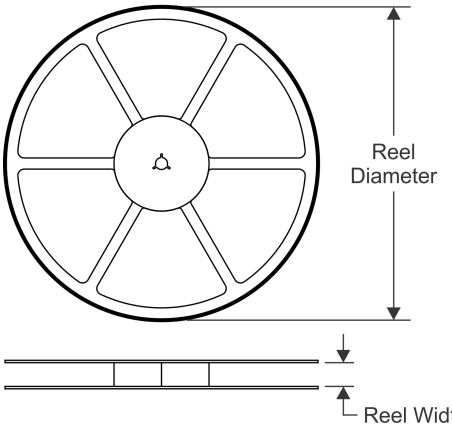
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

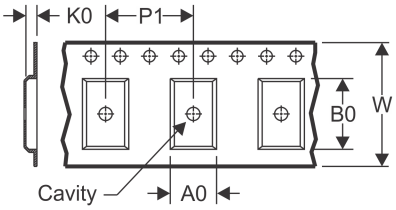
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

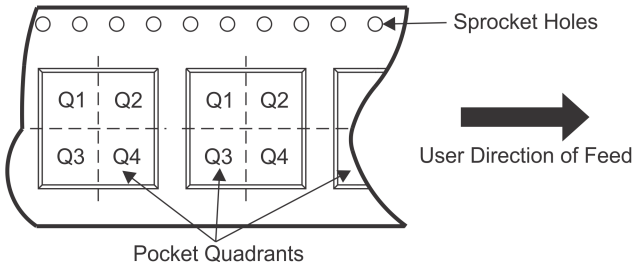


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

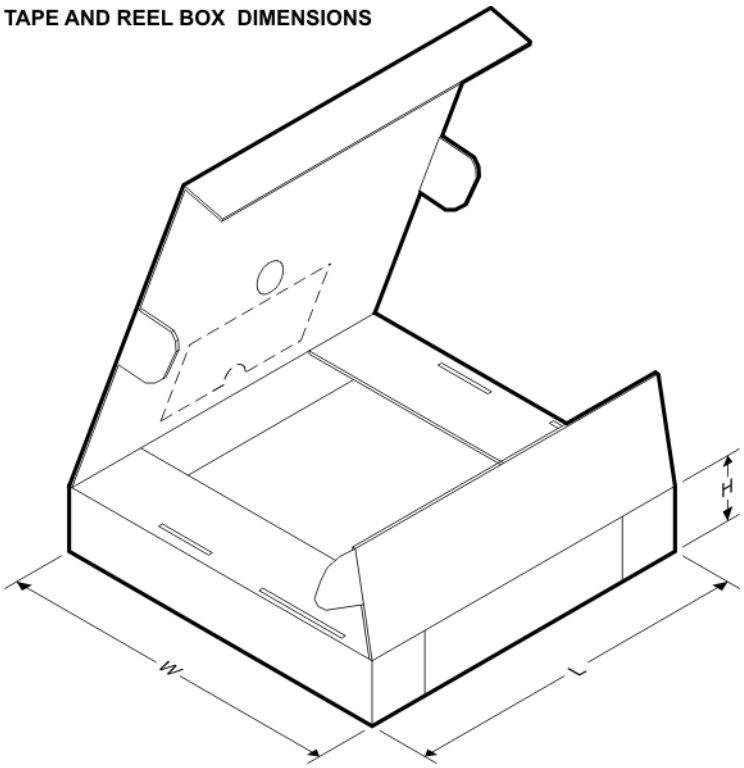
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP7300MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP7300MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7300MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7300MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

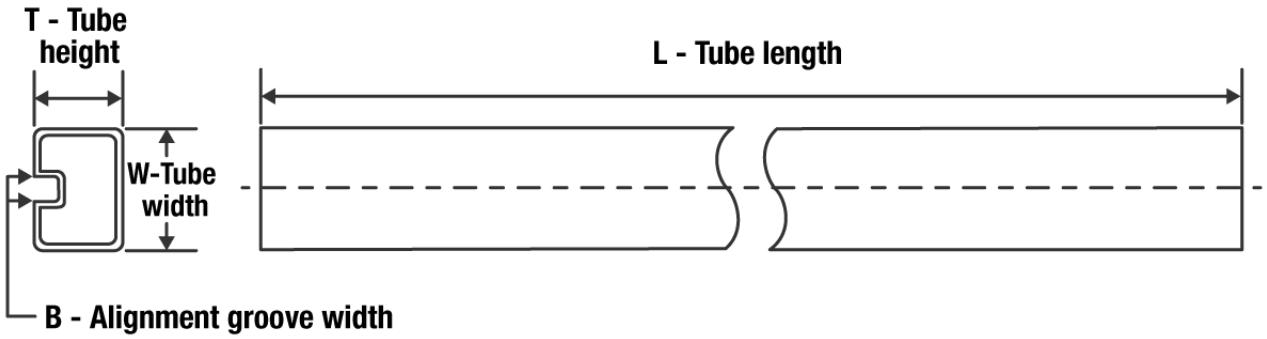
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

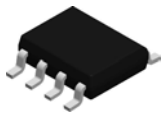
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP7300MAX/NOPB	SOIC	D	8	2500	853.0	449.0	35.0
LMP7300MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMP7300MME/NOPB	VSSOP	DGK	8	250	208.0	191.0	35.0
LMP7300MMX/NOPB	VSSOP	DGK	8	3500	853.0	449.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMP7300MA/NOPB	D	SOIC	8	95	495	8	4064	3.05

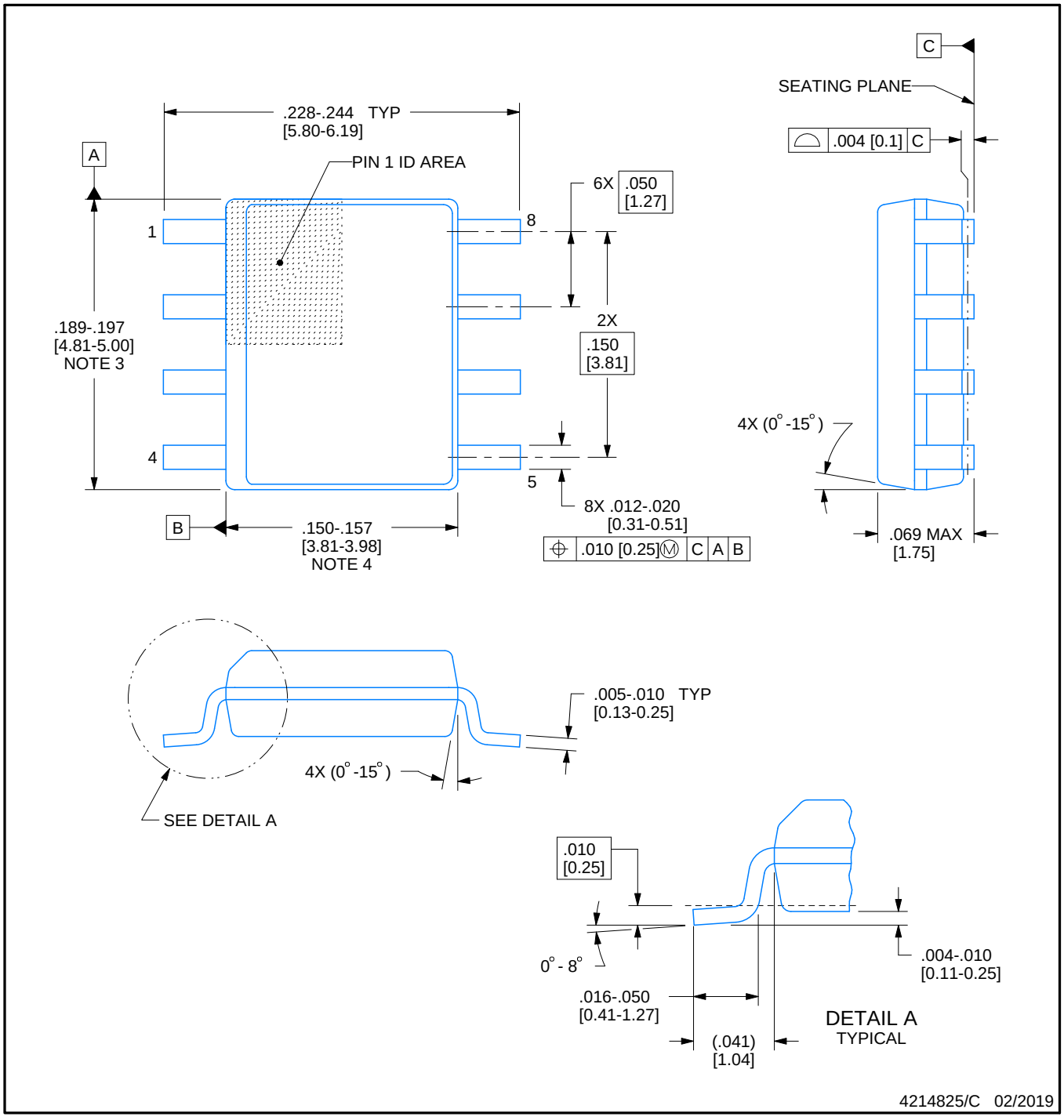


PACKAGE OUTLINE

D0008A

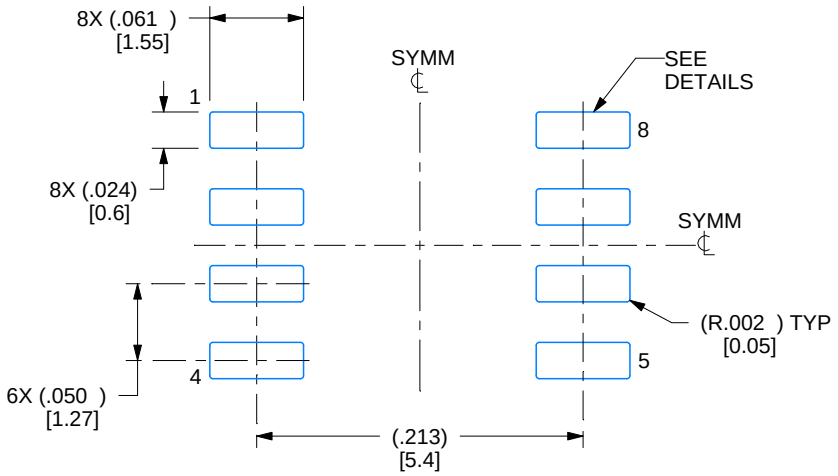
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

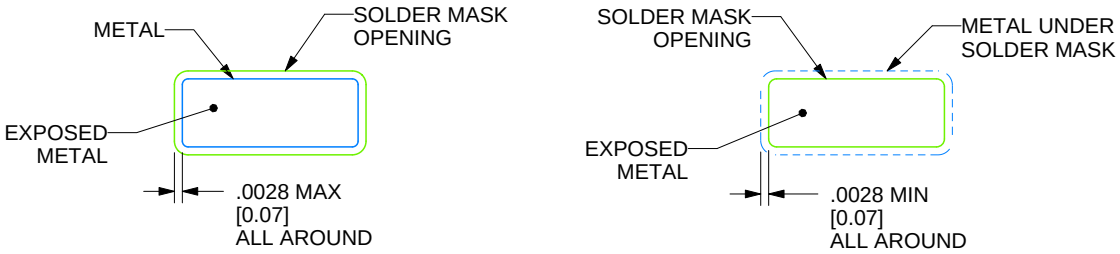


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

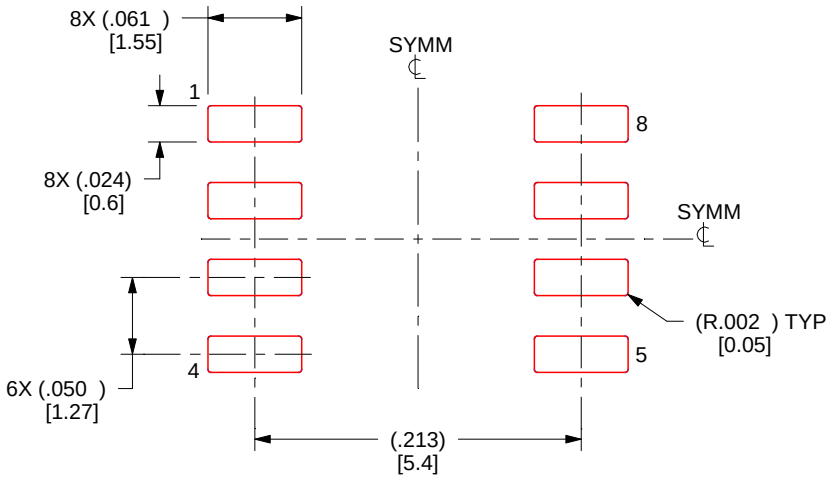
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



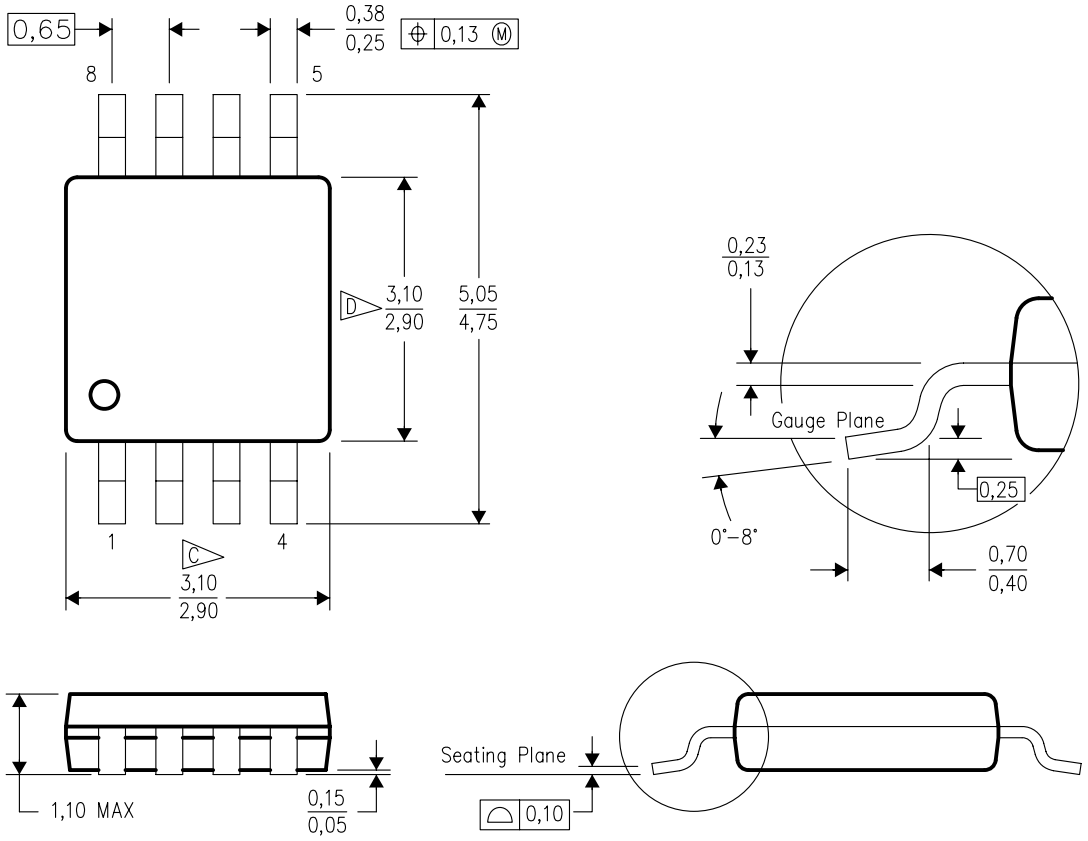
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

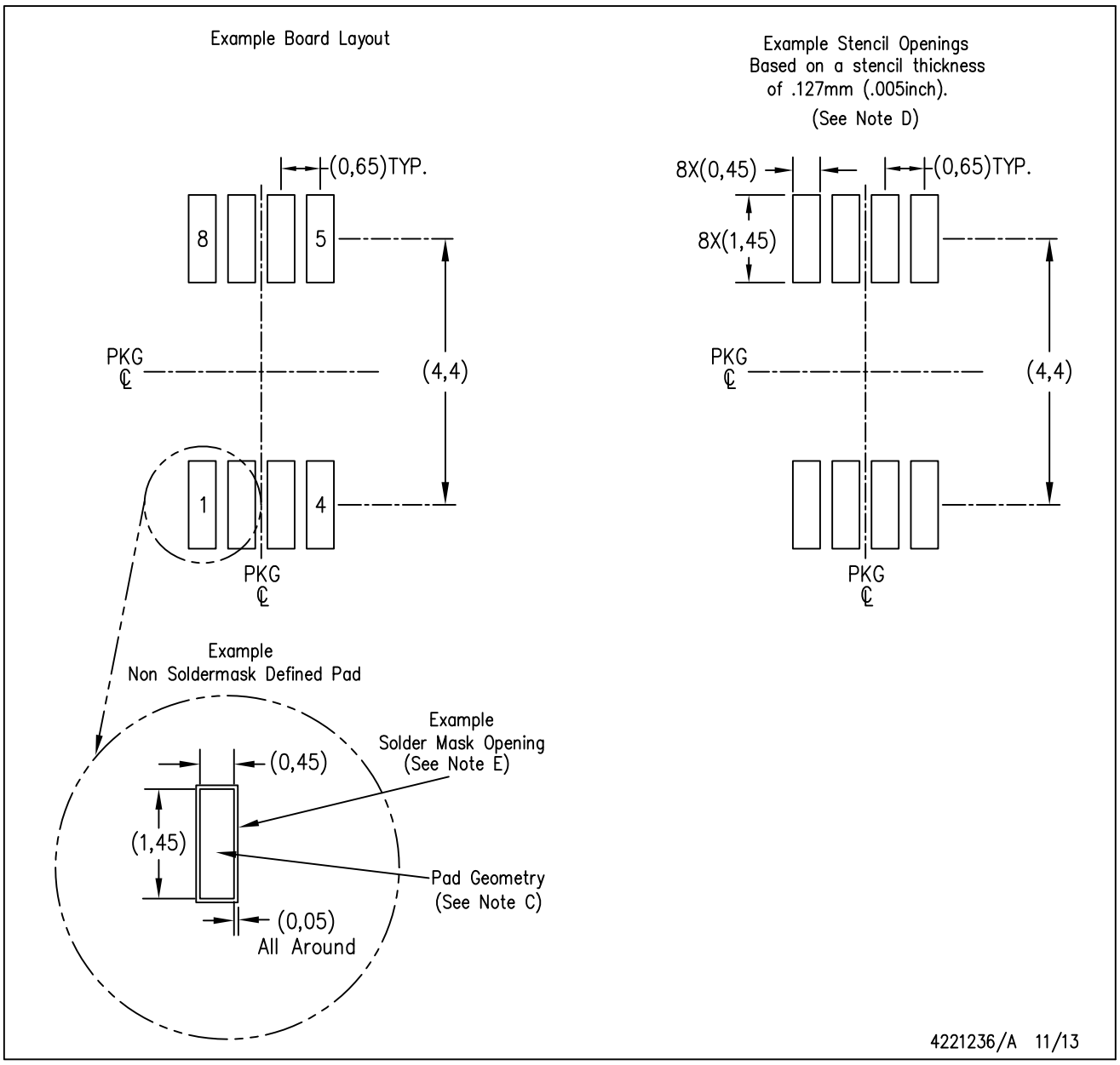
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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