

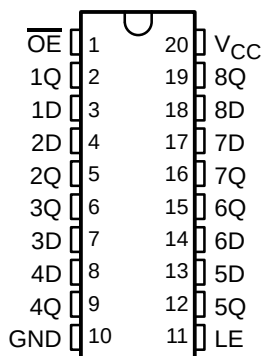
SN54AHC373, SN74AHC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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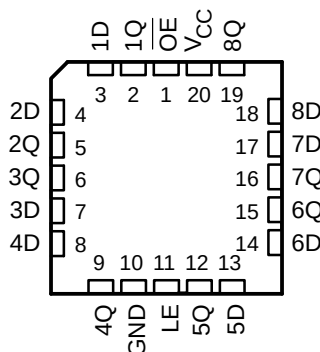
- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17

- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54AHC373 . . . J OR W PACKAGE
SN74AHC373 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC373 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

The 'AHC373 devices are octal transparent D-type latches designed for 2-V to 5.5-V V_{CC} operation.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHC373N	SN74AHC373N
	SOIC – DW	Tube	SN74AHC373DW	AHC373
		Tape and reel	SN74AHC373DWR	
	SOP – NS	Tape and reel	SN74AHC373NSR	AHC373
	SSOP – DB	Tape and reel	SN74AHC373DBR	HA373
	TSSOP – PW	Tube	SN74AHC373PW	HA373
		Tape and reel	SN74AHC373PWR	
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHC373DGV	HA373
	CDIP – J	Tube	SNJ54AHC373J	SNJ54AHC373J
	CFP – W	Tube	SNJ54AHC373W	SNJ54AHC373W
	LCCC – FK	Tube	SNJ54AHC373FK	SNJ54AHC373FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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$\overline{\text{OE}}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

INPUTS			OUTPUT Q
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

Supply voltage range, V _{CC}	-0.5 V to 7 V
Input voltage range, V _I (see Note 1)	-0.5 V to 7 V
Output voltage range, V _O (see Note 1)	-0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	-20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±20 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±25 mA
Continuous current through V _{CC} or GND	±75 mA
Package thermal impedance, θ _{JA} (see Note 2): DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

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recommended operating conditions (see Note 3)

			SN54AHC373		SN74AHC373		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 3 V	2.1		2.1		
		V _{CC} = 5.5 V	3.85		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V
		V _{CC} = 3 V		0.9		0.9	
		V _{CC} = 5.5 V		1.65		1.65	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		–50		–50	μA
		V _{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V _{CC} = 5 V ± 0.5 V		–8		–8	
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 3.3 V ± 0.3 V		4		4	mA
		V _{CC} = 5 V ± 0.5 V		8		8	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V _{CC} = 5 V ± 0.5 V		20		20	
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC373		SN74AHC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA	2 V	1.9			1.9		1.9		V
		3 V	2.9			2.9		2.9		
		4.5 V	4.4			4.4		4.4		
	I _{OH} = –4 mA	3 V	2.58			2.48		2.48		
		4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I _{OL} = 4 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		±1	μA
I _{OZ}	V _I = V _{IH} or V _{IL} , V _O = V _{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		40	μA
C _i	V _I = V _{CC} or GND	5 V			4				10	pF
C ₀	V _O = V _{CC} or GND	5 V			6					pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.



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timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54AHC373		SN74AHC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, LE high	5		5		5		ns
t_{su}	Setup time, data before LE↓	4		4		4		ns
t_h	Hold time, data after LE↓	1		1		1		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54AHC373		SN74AHC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, LE high	5		5		5		ns
t_{su}	Setup time, data before LE↓	4		4		4		ns
t_h	Hold time, data after LE↓	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC373		SN74AHC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	$C_L = 15\text{ pF}$	7.3*	11.4*		1*	13.5*	1	13.5	ns
t_{PHL}				7.3*	11.4*		1*	13.5*	1	13.5	
t_{PLH}	LE	Q	$C_L = 15\text{ pF}$	7*	11*		1*	13*	1	13	ns
t_{PHL}				7*	11*		1*	13*	1	13	
t_{PZH}	$\overline{OE}$	Q	$C_L = 15\text{ pF}$	7.3*	11.4*		1*	13.5*	1	13.5	ns
t_{PZL}				7.3*	11.4*		1*	13.5*	1	13.5	
t_{PHZ}	$\overline{OE}$	Q	$C_L = 15\text{ pF}$	7*	10*		1*	12*	1	12	ns
t_{PLZ}				7*	10*		1*	12*	1	12	
t_{PLH}	D	Q	$C_L = 50\text{ pF}$	9.8	14.9		1	17	1	17	ns
t_{PHL}				9.8	14.9		1	17	1	17	
t_{PLH}	LE	Q	$C_L = 50\text{ pF}$	9.5	14.5		1	16.5	1	16.5	ns
t_{PHL}				9.5	14.5		1	16.5	1	16.5	
t_{PZH}	$\overline{OE}$	Q	$C_L = 50\text{ pF}$	9.8	14.9		1	17	1	17	ns
t_{PZL}				9.8	14.9		1	17	1	17	
t_{PHZ}	$\overline{OE}$	Q	$C_L = 50\text{ pF}$	9.5	13.2		1	15	1	15	ns
t_{PLZ}				9.5	13.2		1	15	1	15	
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1.5**					1.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.



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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC373		SN74AHC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	C _L = 15 pF	5*	7.2*	1*	8.5*	1	8.5	ns	
t _{PHL}				5*	7.2*	1*	8.5*	1	8.5		
t _{PLH}	LE	Q	C _L = 15 pF	4.9*	7.2*	1*	8.5*	1	8.5	ns	
t _{PHL}				4.9*	7.2*	1*	8.5*	1	8.5		
t _{PZH}	$\overline{OE}$	Q	C _L = 15 pF	5.5*	8.1*	1*	9.5*	1	9.5	ns	
t _{PZL}				5.5*	8.1*	1*	9.5*	1	9.5		
t _{PHZ}	$\overline{OE}$	Q	C _L = 15 pF	5*	7.2*	1*	8.5*	1	8.5	ns	
t _{PLZ}				5*	7.2*	1*	8.5*	1	8.5		
t _{PLH}	D	Q	C _L = 50 pF	6.5	9.2	1	10.5	1	10.5	ns	
t _{PHL}				6.5	9.2	1	10.5	1	10.5		
t _{PLH}	LE	Q	C _L = 50 pF	6.4	9.2	1	10.5	1	10.5	ns	
t _{PHL}				6.4	9.2	1	10.5	1	10.5		
t _{PZH}	$\overline{OE}$	Q	C _L = 50 pF	7	10.1	1	11.5	1	11.5	ns	
t _{PZL}				7	10.1	1	11.5	1	11.5		
t _{PHZ}	$\overline{OE}$	Q	C _L = 50 pF	6.5	9.2	1	10.5	1	10.5	ns	
t _{PLZ}				6.5	9.2	1	10.5	1	10.5		
t _{sk(o)}			C _L = 50 pF	1**					1	ns	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER		SN74AHC373		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}	0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	–0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.1		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage	1.5		V

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	18	pF



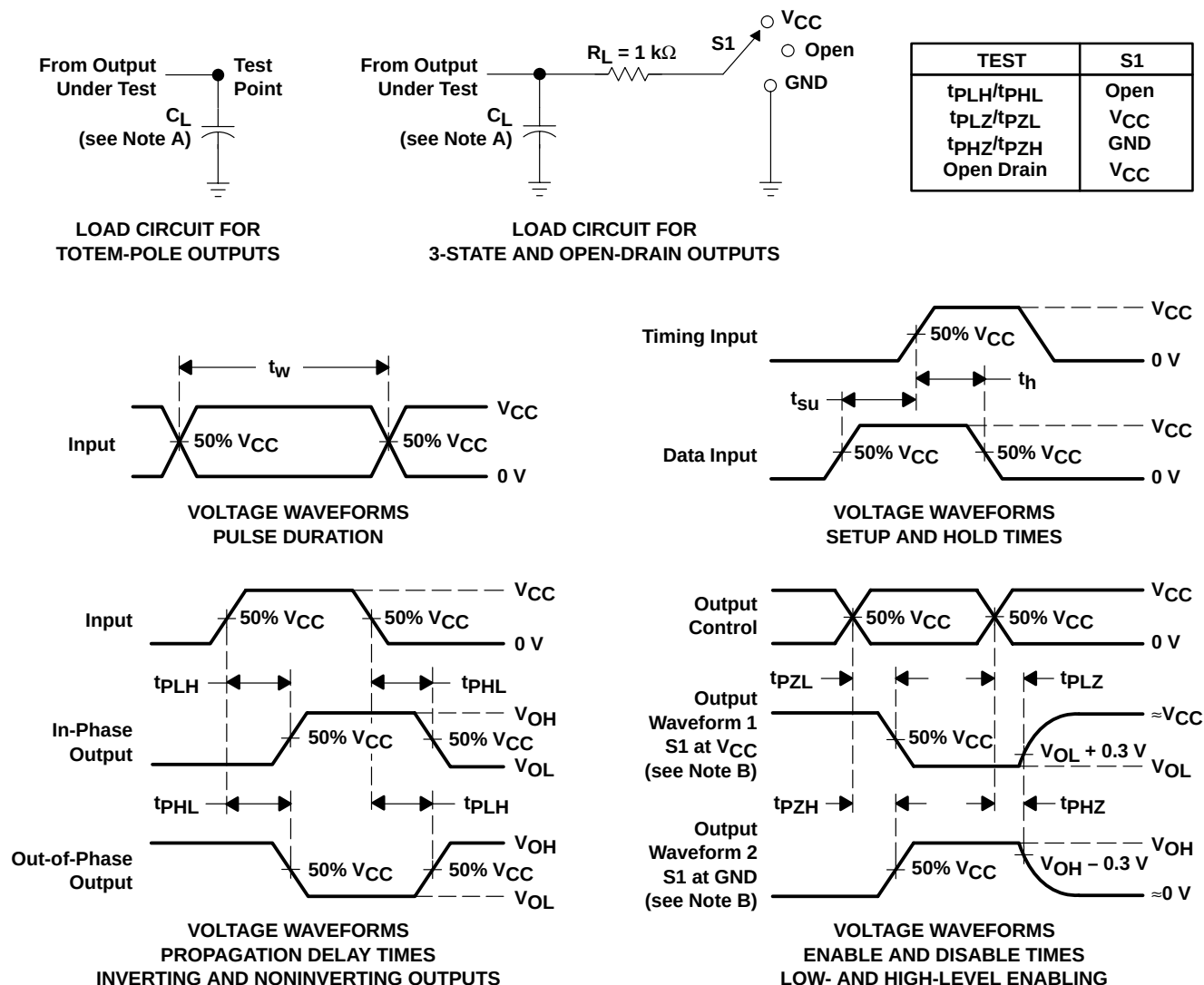
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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9686601Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9686601Q2A SNJ54AHC 373FK	Samples
5962-9686601QRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686601QR A SNJ54AHC373J	Samples
5962-9686601QSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686601QS A SNJ54AHC373W	Samples
SN74AHC373DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA373	Samples
SN74AHC373DGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA373	Samples
SN74AHC373DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC373	Samples
SN74AHC373DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC373	Samples
SN74AHC373N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC373N	Samples
SN74AHC373NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC373	Samples
SN74AHC373PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA373	Samples
SN74AHC373PWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA373	Samples
SN74AHC373PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA373	Samples
SNJ54AHC373FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9686601Q2A SNJ54AHC 373FK	Samples
SNJ54AHC373J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686601QR A SNJ54AHC373J	Samples
SNJ54AHC373W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686601QS A SNJ54AHC373W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AHC373, SN74AHC373 :

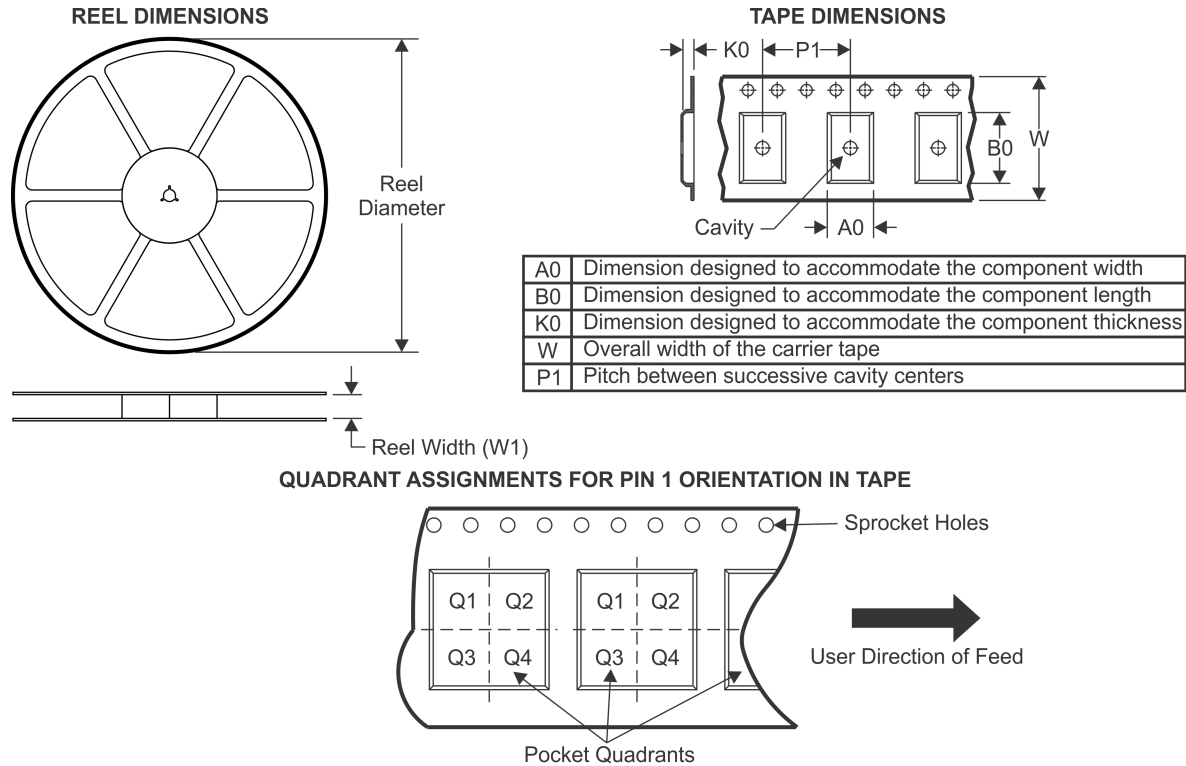
● Catalog : [SN74AHC373](#)

● Military : [SN54AHC373](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

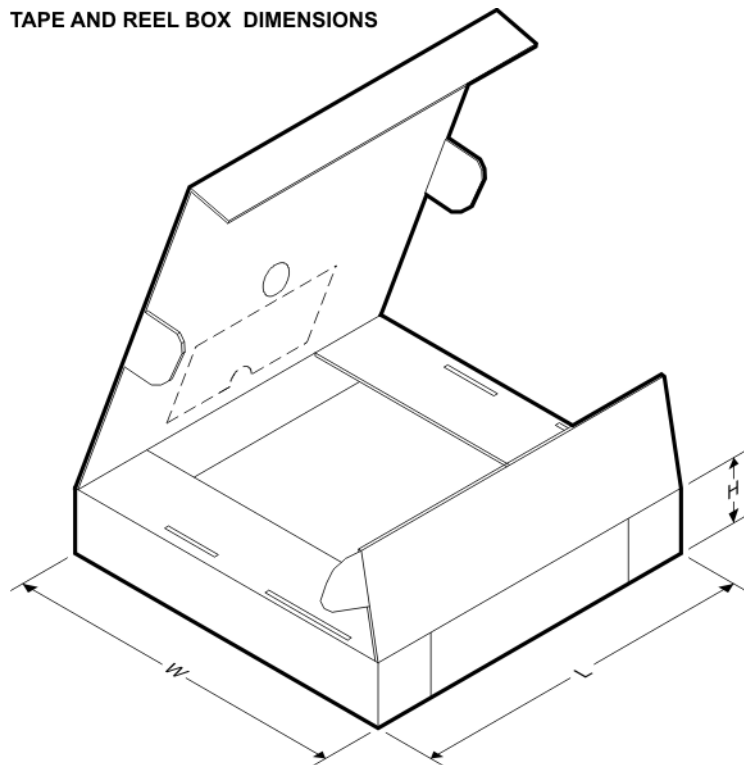
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC373DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC373DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC373NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC373PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

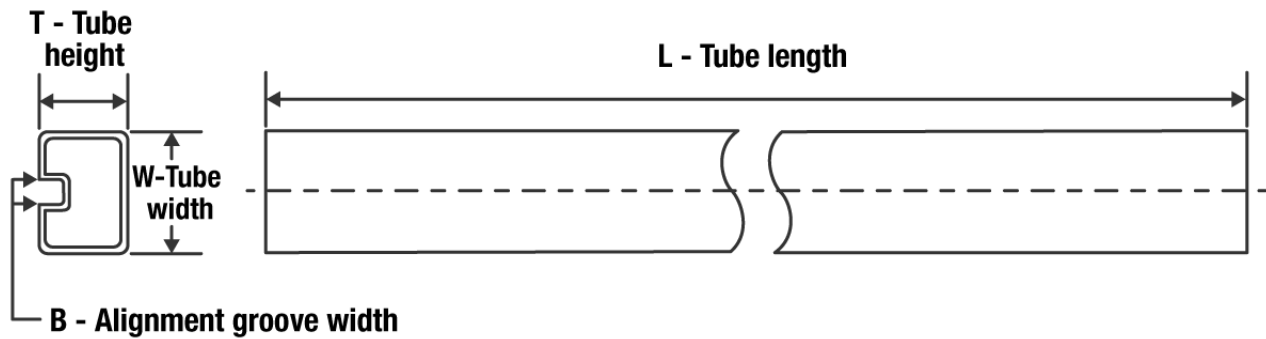
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC373DBR	SSOP	DB	20	2000	853.0	449.0	35.0
SN74AHC373DGVR	TVSOP	DGV	20	2000	853.0	449.0	35.0
SN74AHC373DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHC373NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AHC373PWR	TSSOP	PW	20	2000	853.0	449.0	35.0

TUBE



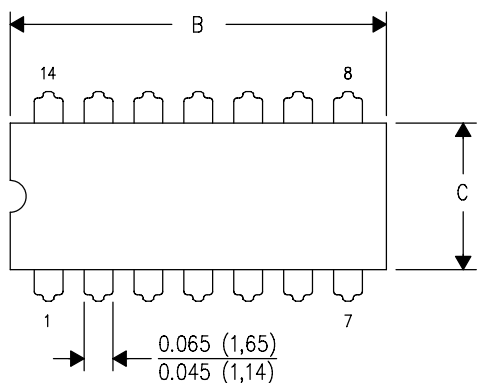
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9686601Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74AHC373DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AHC373N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHC373PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74AHC373PWG4	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54AHC373FK	FK	LCCC	20	1	506.98	12.06	2030	NA

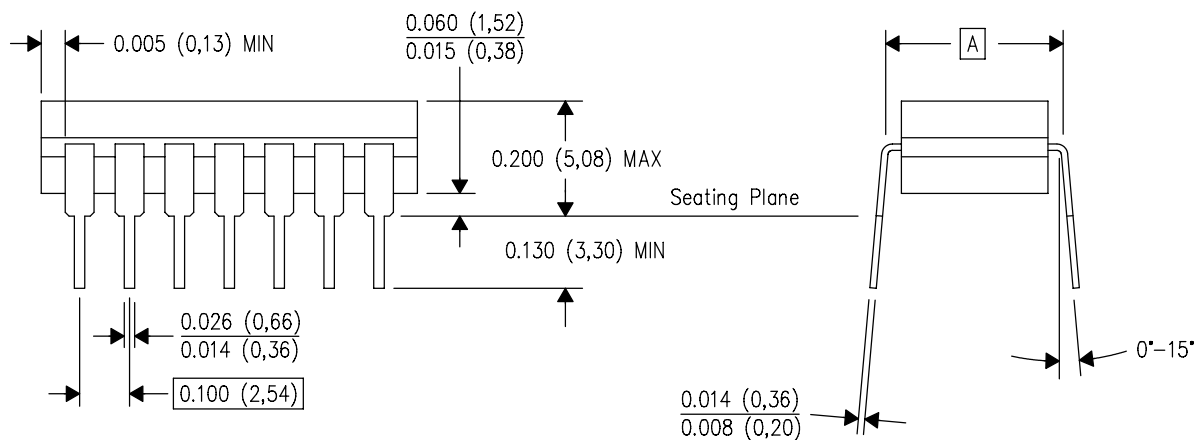
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



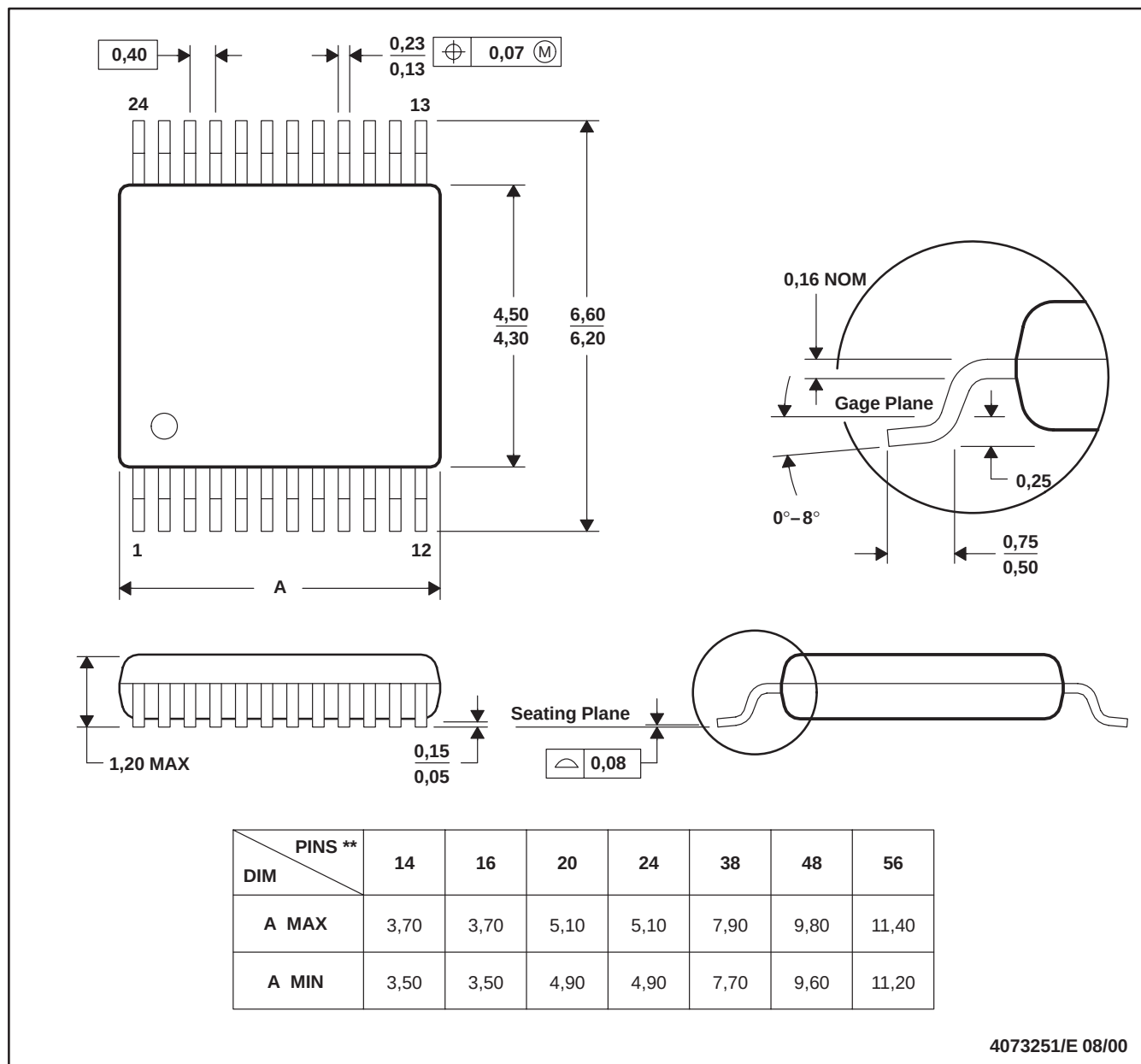
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

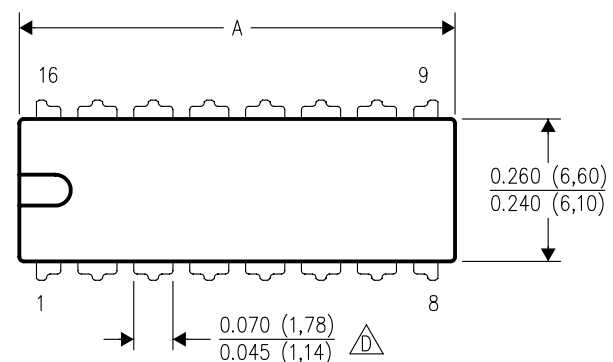


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

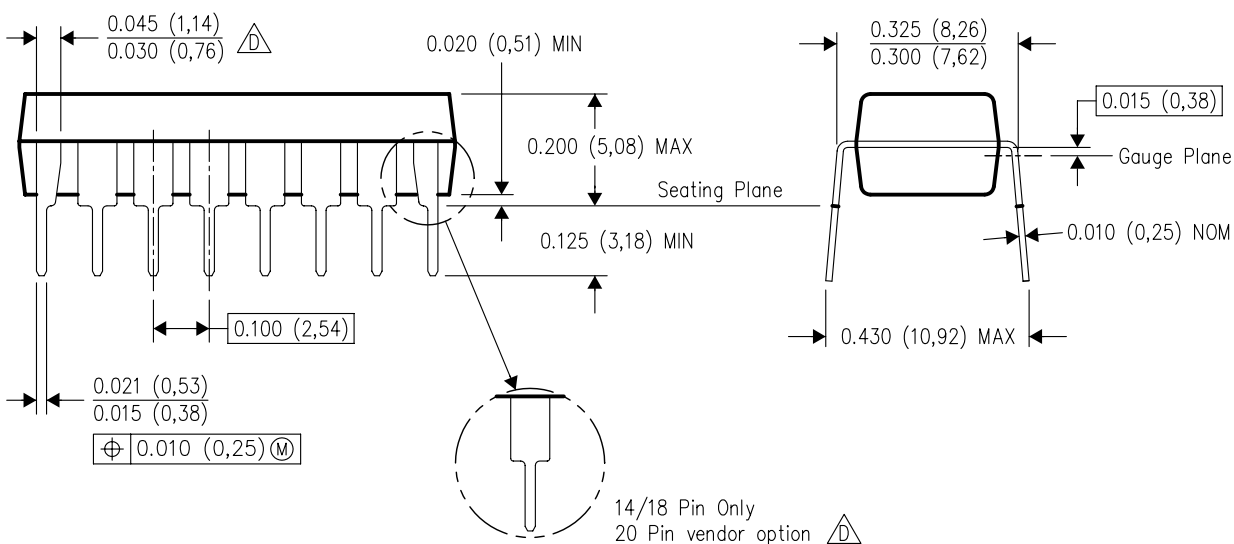
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



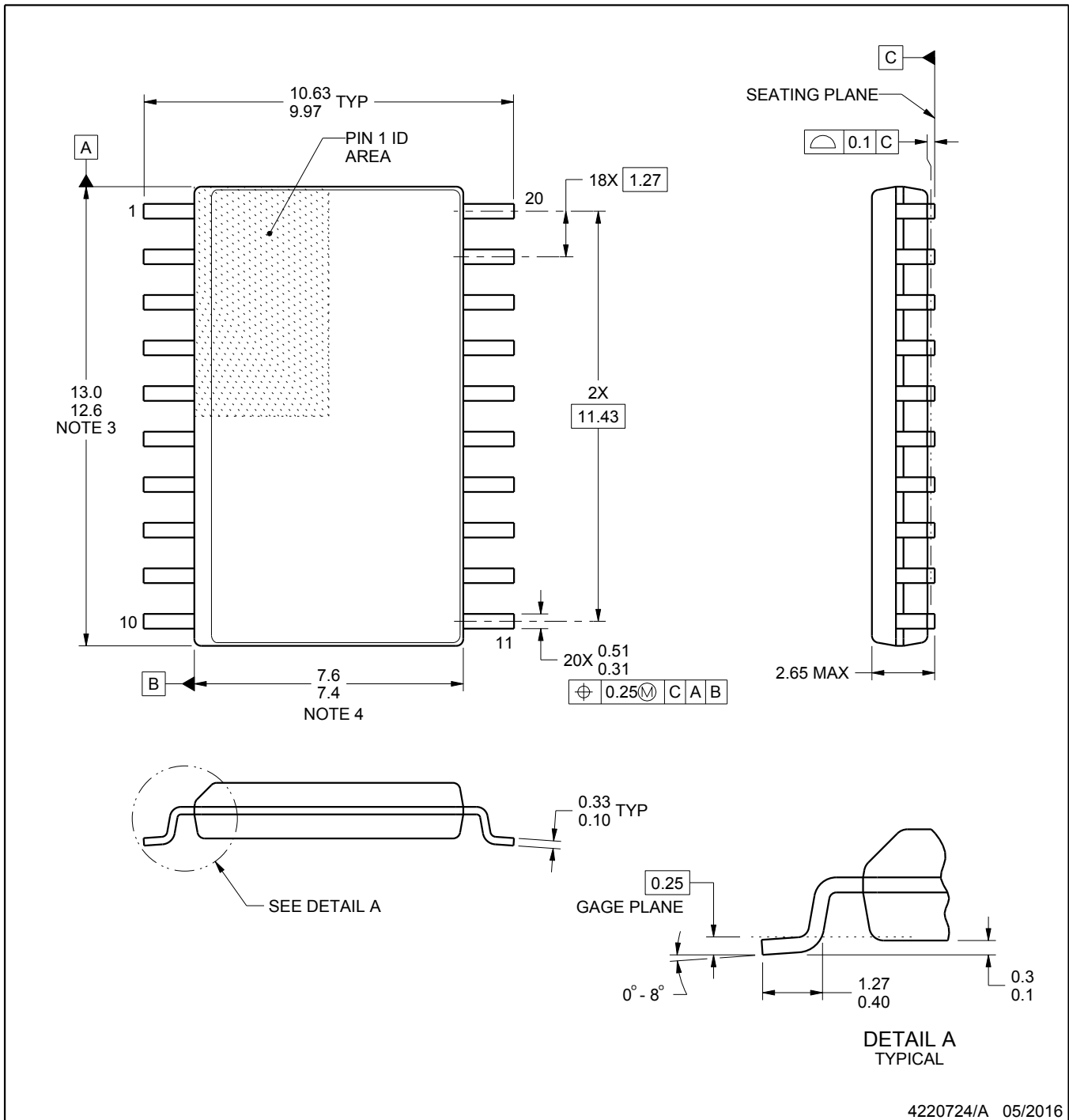
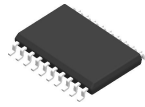
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



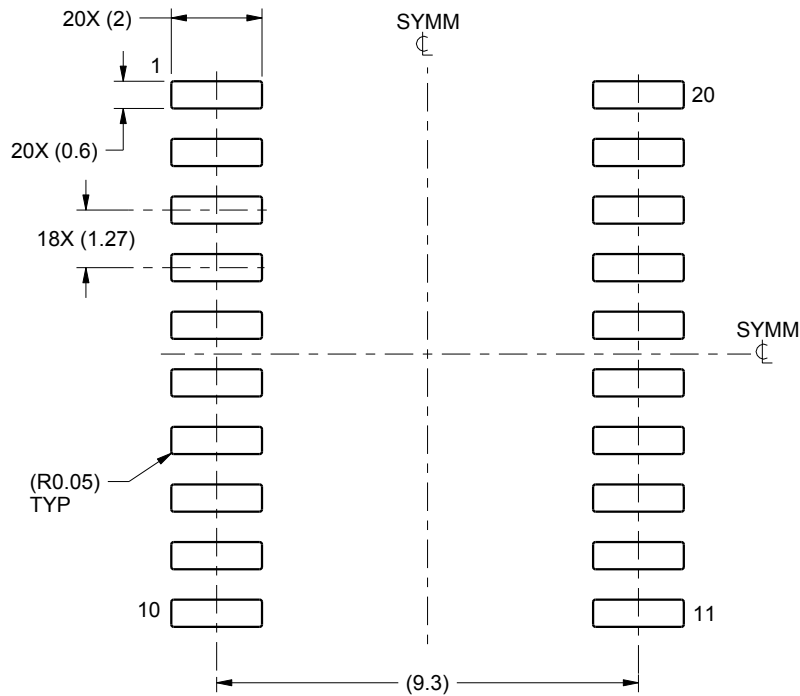
4220724/A 05/2016

EXAMPLE BOARD LAYOUT

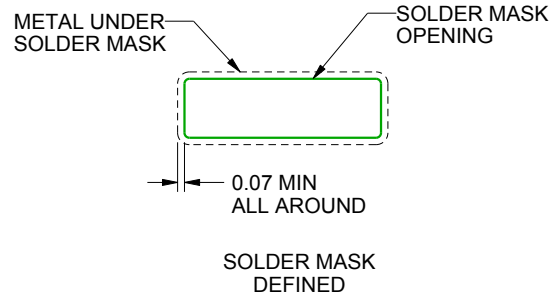
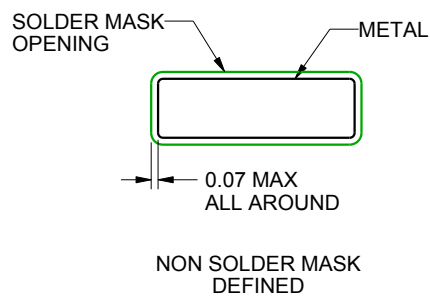
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

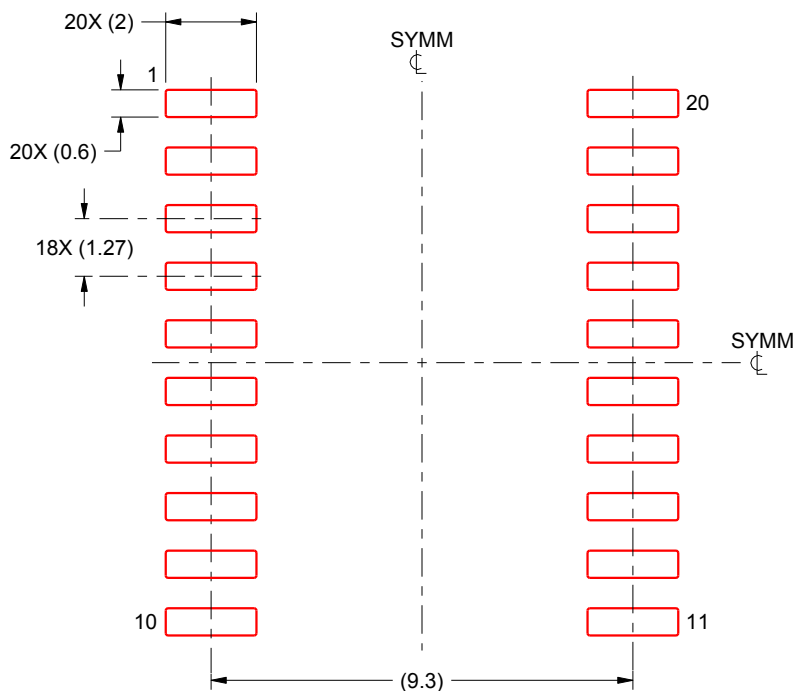
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

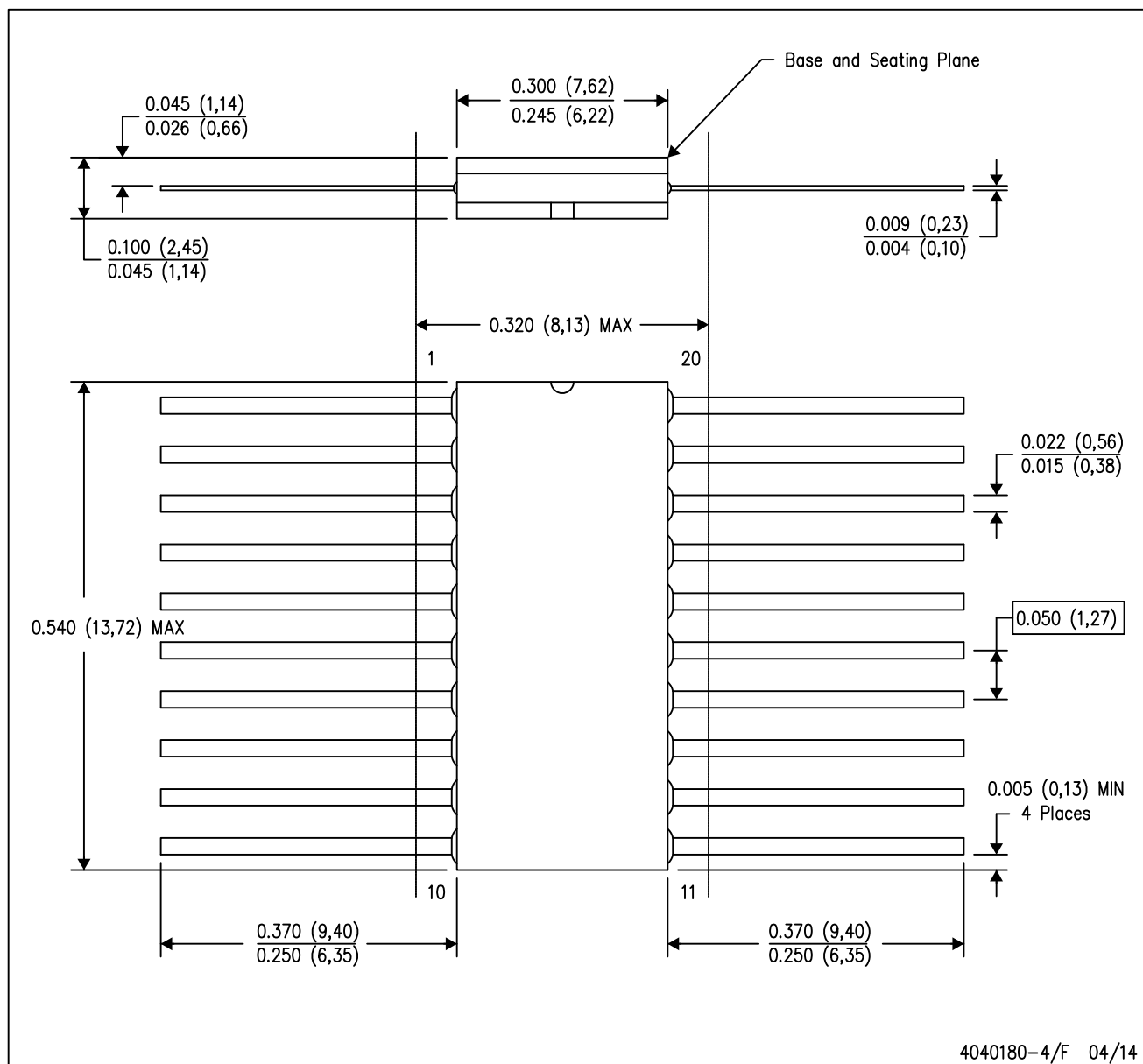
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

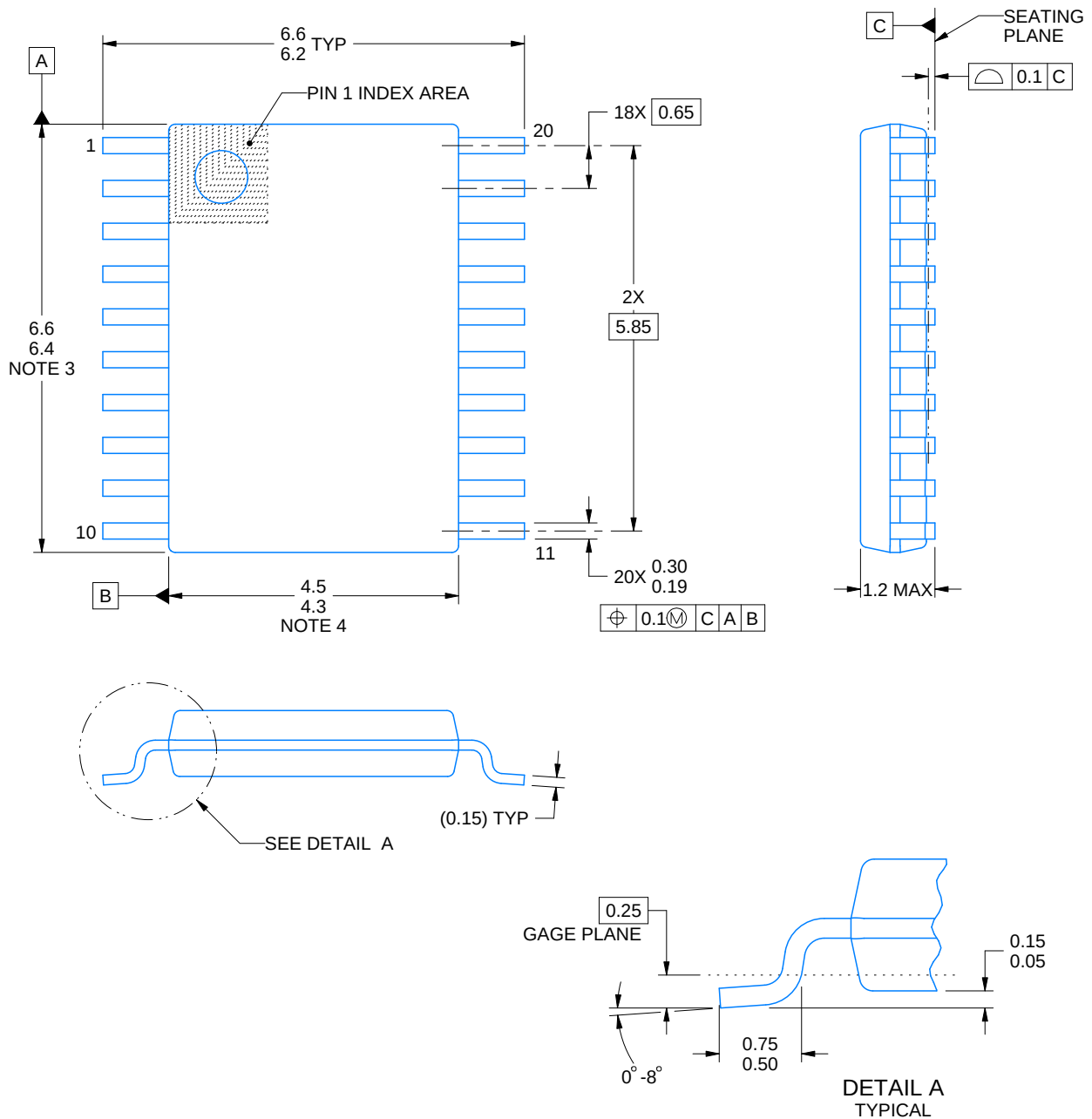
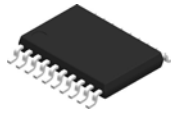
W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



4220206/A 02/2017

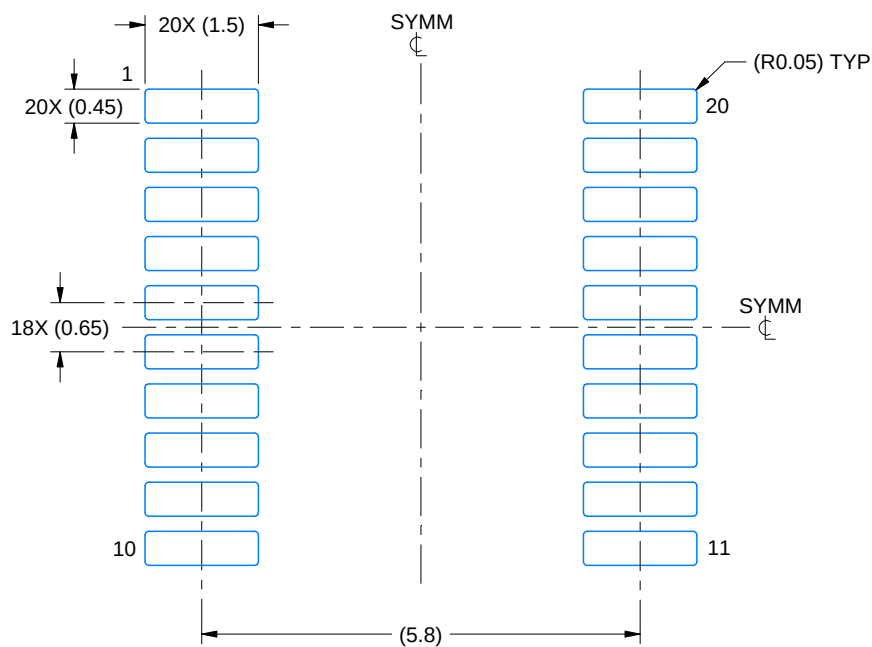
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

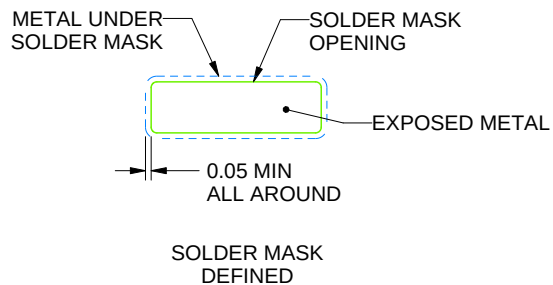
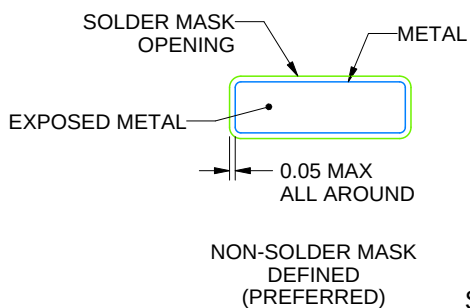
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

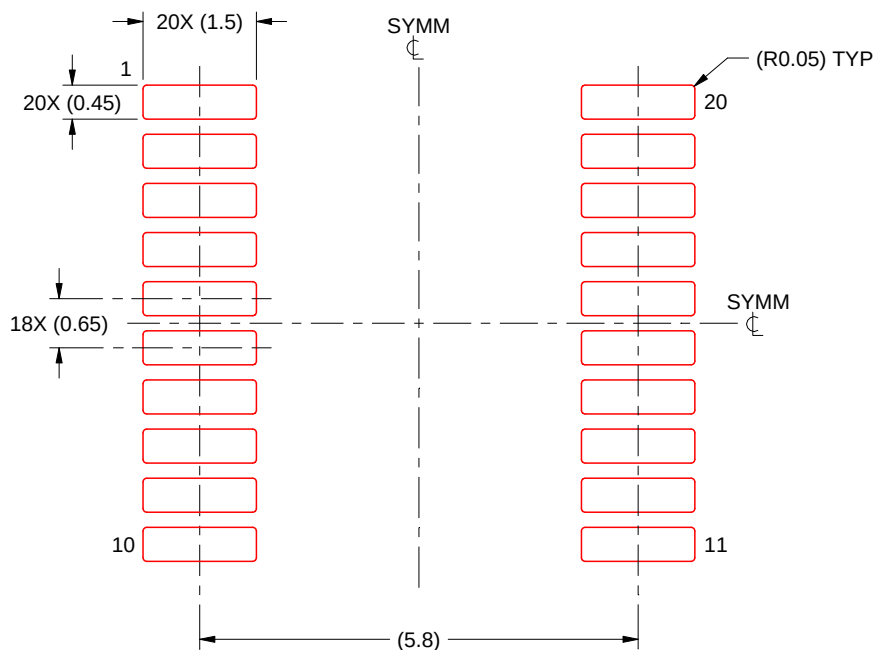
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

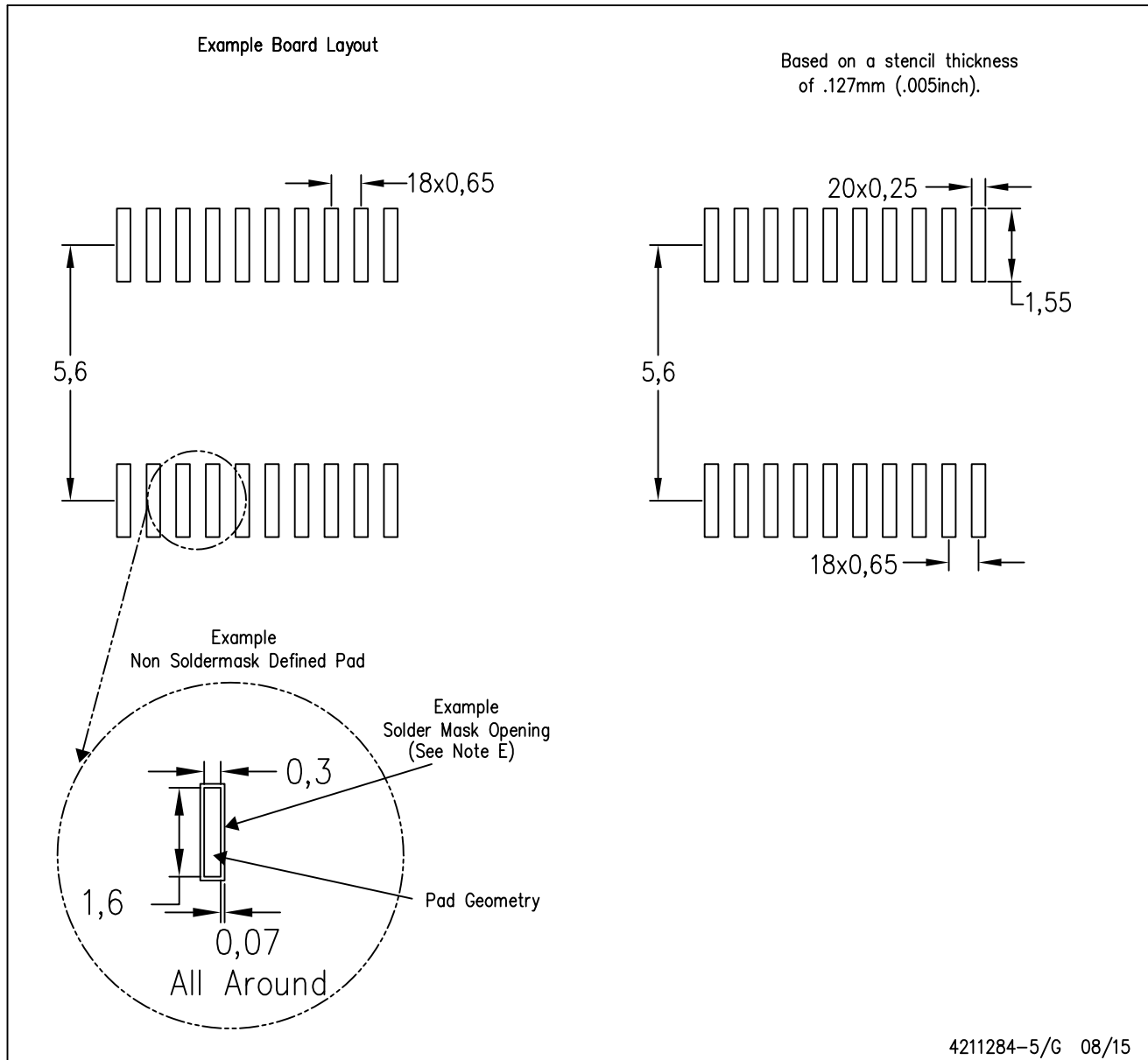
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

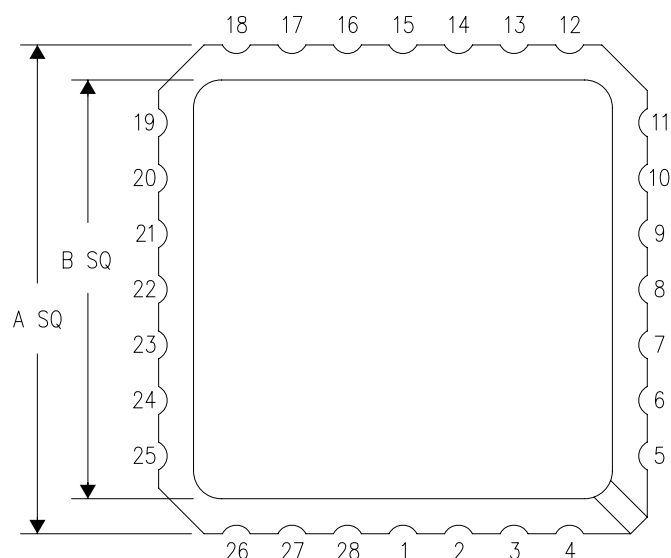


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

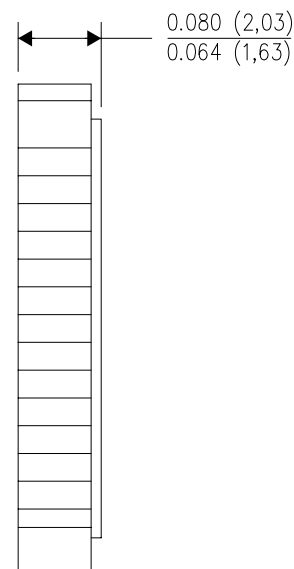
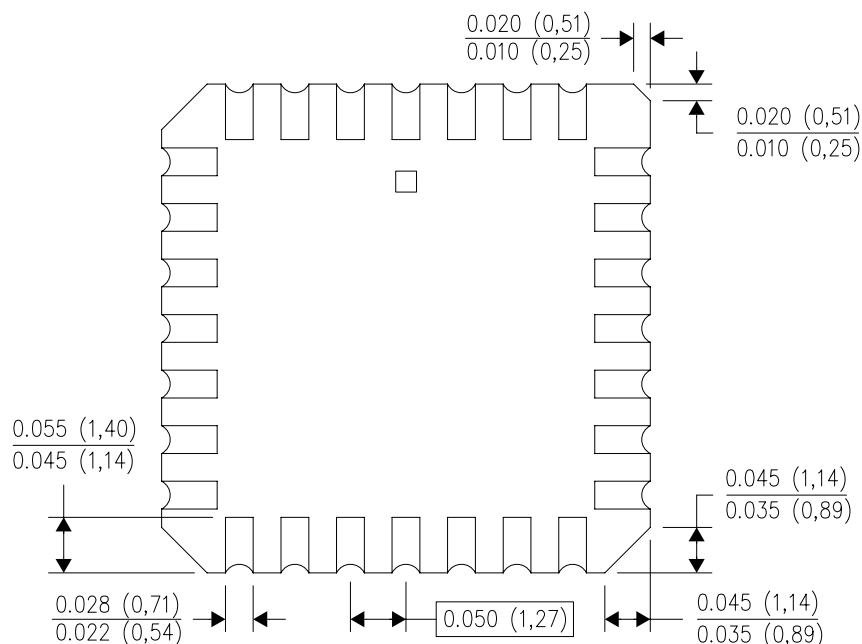
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

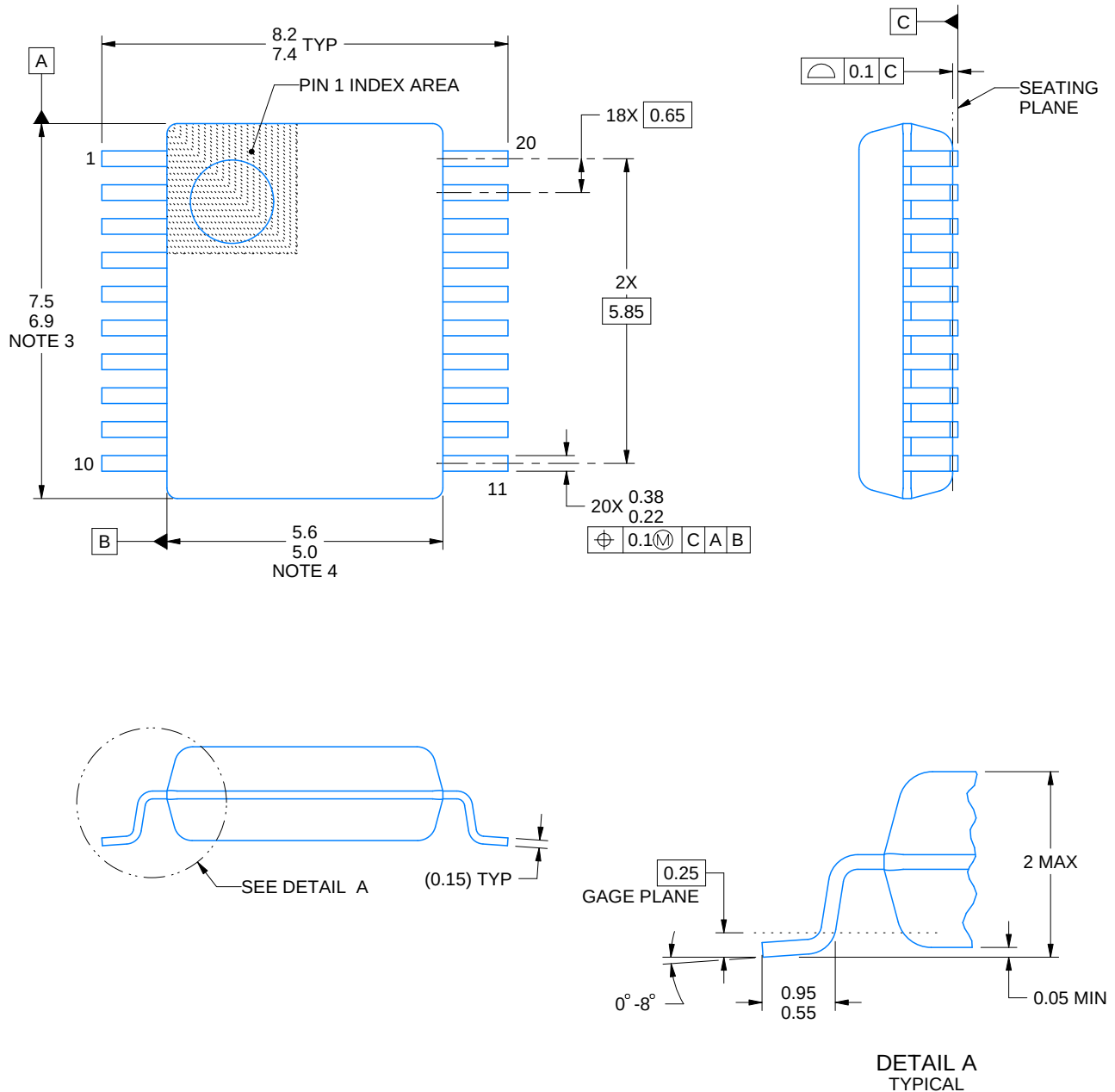
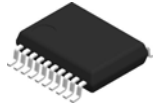


NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004



4214851/B 08/2019

NOTES:

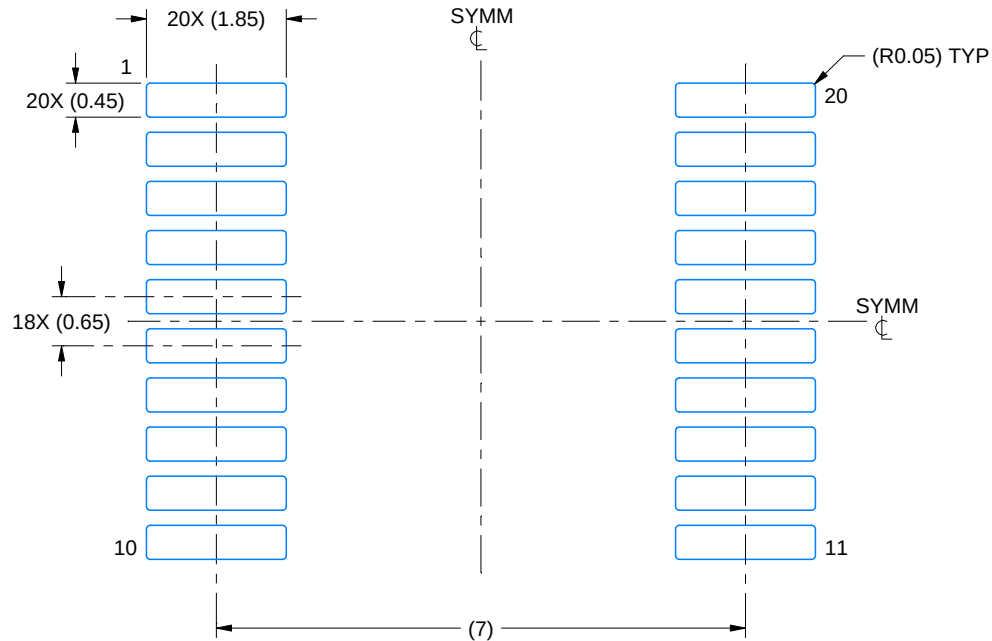
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

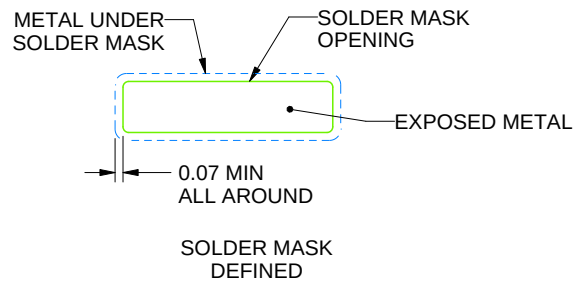
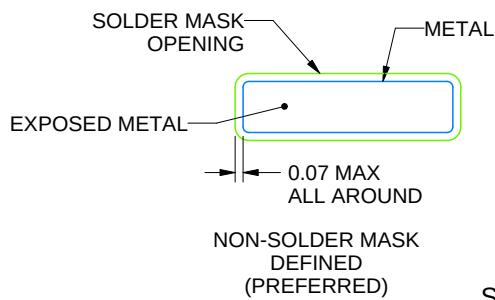
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

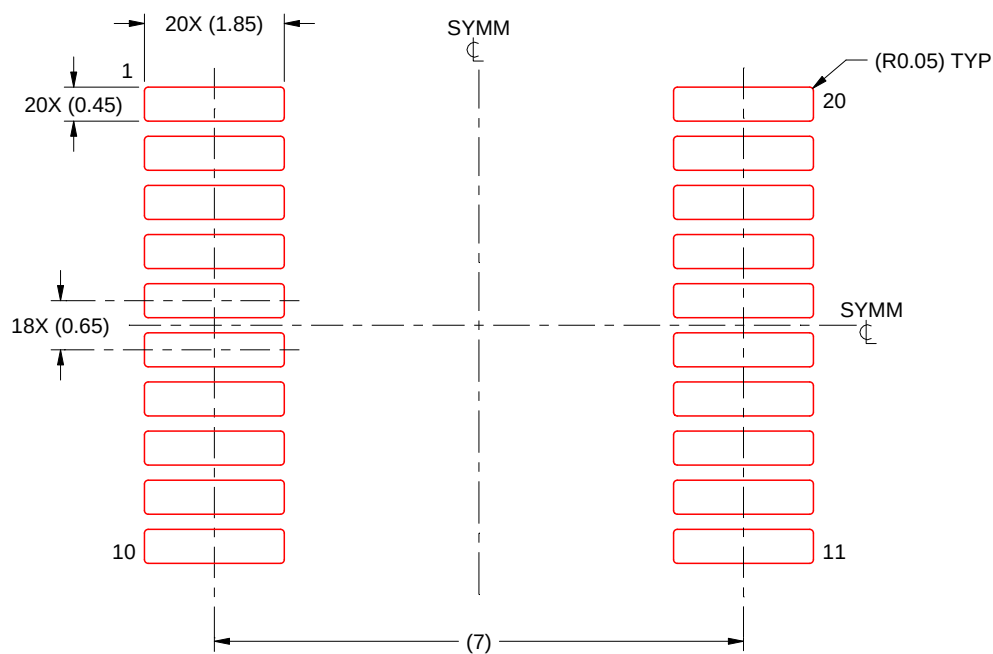
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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