LP8900 200-mA Ultra-Low-Noise Dual LDO For RF and Analog Circuits

1 Features

- Input Voltage Operation: 1.8 V to 5.5 V
- Output Voltage: 1.2 V to 3.6 V
- Accuracy Over Temperature: 1%
- Output Voltage Noise: 6 μV_{RMS}
- PSRR: 75 dB at 1 kHz
- Dropout: 110 mV at 200 mA Load
- Quiescent Current: 48 µA per Regulator
- Start-Up Time: 80 µs
- Stable With Ceramic Capacitors as Small as 0402
- Thermal-Overload and Short-Circuit Protection

2 Applications

- Battery-Operated Devices
- Hand-Held Information Appliances
- Noise Sensitive RF Applications
- DC-DC Convertor Post Regulation and Filter

3 Description

The LP8900 is a dual LDO capable of supplying 200-mA output current per regulator. Designed to meet the requirements of RF and analog circuits, the LP8900 provides low device noise, high PSRR, low quiescent current, and superior line transient response figures.

Using new innovative design techniques, the LP8900 offers class-leading device noise performance without a noise bypass capacitor.

The LP8900 is designed to be stable with space saving ceramic capacitors as small as 0402 case size, enabling a solution size < 4 mm^2. Performance is specified for a –40°C to +125°C junction temperature range.

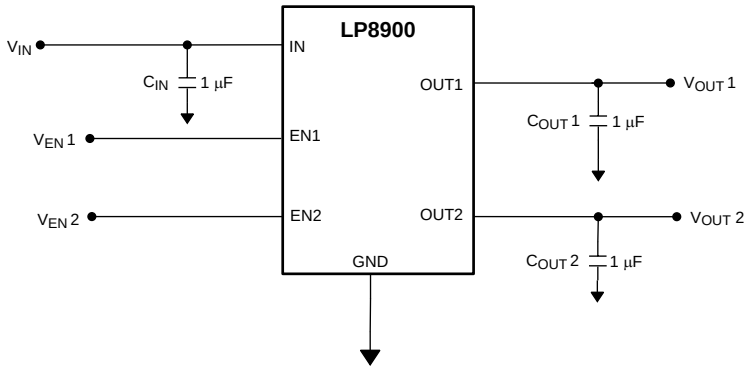
Output voltage options from 1.2 V to 3.6 V are available; for availability, contact your local TI sales office.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LP8900	DSBGA (6)	1.49 mm × 1.09 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Default Device Options ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 4
7.5 Electrical Characteristics ... 5
7.6 Timing Requirements ... 6
7.7 Typical Characteristics ... 7
8 Detailed Description ... 9
8.1 Overview ... 9
8.2 Functional Block Diagram ... 9
8.3 Feature Description ... 9
8.4 Device Functional Modes ... 10
9 Application and Implementation ... 11
9.1 Application Information ... 11
9.2 Typical Application ... 11
10 Power Supply Recommendations ... 15
11 Layout ... 16
11.1 Layout Guidelines ... 16
11.2 Layout Example ... 16
11.3 DSBGA Mounting ... 16
11.4 DSBGA Light Sensitivity ... 16
12 Device and Documentation Support ... 17
12.1 Documentation Support ... 17
12.2 Community Resources ... 17
12.3 Trademarks ... 17
12.4 Electrostatic Discharge Caution ... 17
12.5 Glossary ... 17
13 Mechanical, Packaging, and Orderable Information ... 17

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2015) to Revision E — **Page**

- Changed "linear regulator" to "LDO" on page 1 ... 1

Changes from Revision C (July 2013) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation section*, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section; add updated *Thermal Information* values; delete lead temperature from Ab Max (which is in POA); update pin names to TI nomenclature ... 1

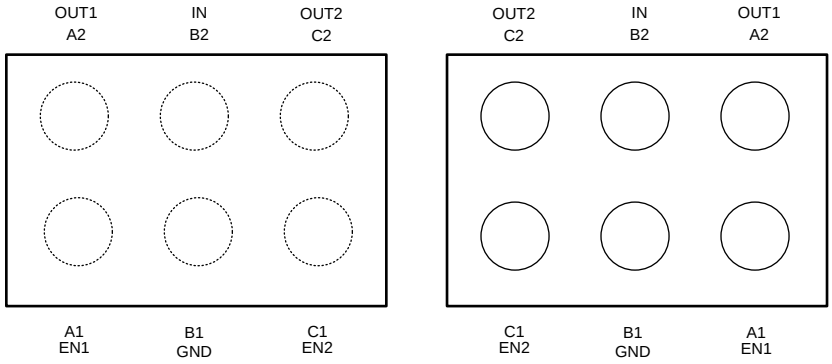
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5 Default Device Options

ORDERABLE NUMBER	OUT1	OUT2
LP8900TLE-3333	2.8 V	2.8 V
LP8900TLE-AAAH	2.7 V	2.7 V
LP8900TLE-AAEB	2.8 V	2.7 V
LP8900TLE-AAEC	2.8 V	1.2 V

6 Pin Configuration and Functions

YZR Package
6-Pin DSBGA



Top View **Bottom View**

Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
A1	EN1	I	Enable input; enables the regulator when ≥ 1.2 V. Enable Input has an internal 3-MΩ pulldown resistor to GND. Disables the regulator when ≤ 0.4 V.
A2	OUT1	O	Voltage output. A low ESR ceramic capacitor must be connected from this pin to GND. (See *Application and Implementation*.) Connect this output to the load circuit.
B1	GND	G	Common ground.
B2	IN	I	Voltage supply input. A 1-µF capacitor must be connected from this pin to GND.
C1	EN2	I	Enable input; enables the regulator when ≥ 1.2 V. Enable input has an internal 3-MΩ pulldown resistor to GND. Disables the regulator when ≤ 0.4 V.
C2	OUT2	O	Voltage output. A low ESR ceramic capacitor must be connected from this pin to GND. (See *Application and Implementation*.) Connect this output to the load circuit.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
IN, OUT pins: Voltage to GND	–0.3	6.5	V
EN pin: Voltage to GND	–0.3 to (V_{IN} + 0.3V)	6.5	°C
Continuous power dissipation(3)	Internally limited		
Junction temperature		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) Internal thermal shutdown circuitry protects the device from permanent damage.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
Input voltage	1.8		5.5	V
Recommended load current per channel			200	mA
Junction temperature, T_J	–40		125	°C
Ambient temperature, T_A(2)	–40		85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum ambient temperature ($T_{A(MAX)}$) is dependant on the maximum operating junction temperature ($T_{J(MAX-OP)}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D(MAX)}$), and the junction to ambient thermal resistance of the part / package in the application ($R_{\theta JA}$), as given by: $T_{A(MAX)} = T_{J(MAX-OP)} – (R_{\theta JA} \times P_{D(MAX)})$.

7.4 Thermal Information

THERMAL METRIC(1)		LP8900 YZR (DSBGA) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	140.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Unless otherwise noted, V_{EN} = 1.2 V, V_{IN} = V_{OUT} + 0.5 V, or 1.8 V, whichever is higher (where V_{OUT} is the higher of V_{OUT1} and V_{OUT2}), C_{IN} = C_{OUT} = 1 µF, and I_{OUT} = 1 mA. Typical values apply for T_A = 25°C; minimum and maximum values apply over the full junction temperature range for operation, −40 to +125°C, unless otherwise specified.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	T_A = 25°C, see(2)		1.8		5.5	V
ΔV_{OUT}	Output voltage tolerance	V_{IN} = $V_{OUT(NOM)}$ + 0.5 V to 5.5 V I_{LOAD} = 1 mA		1%		1%	
		V_{IN} = 1.8 V to 5.5 V I_{LOAD} = 1 mA, V_{OUT} = 1.2 V		–2.25%		2.25%	
	Line regulation error	V_{IN} = $V_{OUT(NOM)}$ + 0.5 V to 5.5 V I_{OUT} = 1 mA			0.05		%/V
	Load regulation error	I_{OUT} = 1 mA to 200 mA			4	9	mV
V_{DO}	Dropout voltage(3)	I_{OUT} = 200 mA	V_{OUT} = 3.6 V		55	82	mV
			V_{OUT} = 2.8 V		110	164	
			V_{OUT} = 1.8 V		185	260	
I_{LOAD}	Load current	T_A = 25°C, see(4)		0			mA
		See(4)				200	
I_Q	Quiescent current	V_{EN1} = 1.2 V, V_{EN2} = 0 V, I_{OUT} = 0 mA			48	120	µA
		V_{EN1} = 1.2 V, V_{EN2} = 1.2 V, I_{OUT} = 0 mA			85	200	
		V_{EN1} = 1.2 V, V_{EN2} = 1.2 V, I_{OUT} = 200 mA			210		
		V_{EN} ≤ 0.4 V			0.003	1	
I_{SC}	Short-circuit current limit	V_{IN} = 3.6 V(5)			600	900	mA
PSRR	Power supply rejection ratio(6)	f = 1 kHz, I_{OUT} = 200 mA			75		dB
		f = 10 kHz, I_{OUT} = 200 mA			65		
		f = 100 kHz, I_{OUT} = 200 mA			45		
		f = 1 MHz, I_{OUT} = 200 mA			30		
e_n	Output noise voltage(6)	BW = 10 Hz to 100 kHz, V_{IN} = 4.2 V, C_{OUT} = 1 µF	I_{OUT} = 0 mA		6		μV_{RMS}
			I_{OUT} = 1 mA		10		
			I_{OUT} = 200 mA		6		
$T_{SHUTDOWN}$	Thermal shutdown	Temperature			155		°C
		Hysteresis			15		
ENABLE CONTROL CHARACTERISTICS							
I_{EN}	Maximum input current at EN input(7)	V_{EN} = 0 V, V_{IN} = 5.5 V			0.003		µA
		V_{EN} = V_{IN} = 5.5 V				4	
V_{IL}	Low input threshold	V_{IN} = 1.8 V to 5.5 V				0.4	V
V_{IH}	High input threshold	V_{IN} = 1.8 V to 5.5 V		1.2			V

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production at T_J = 25°C or correlated using Statistical Quality Control methods. Operation over the temperature specification is ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The minimum input voltage = $V_{OUT(NOM)}$ + 0.5 V or 1.8 V, whichever is greater.
(3) Dropout voltage is voltage difference between input and output at which the output voltage drops to 100 mV below its nominal value. This parameter is only specified for output voltages above 1.8 V.
(4) The device maintains the regulated output voltage without a load.
(5) Short circuit current is measured with V_{OUT} pulled to 0 V.
(6) This electrical specification is ensured by design.
(7) EN Pin has an internal 3-MΩ typical, resistor connected to GND.

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Electrical Characteristics (continued)

Unless otherwise noted, V_{EN} = 1.2 V, V_{IN} = V_{OUT} + 0.5 V, or 1.8 V, whichever is higher (where V_{OUT} is the higher of V_{OUT1} and V_{OUT2}), C_{IN} = C_{OUT} = 1 µF, and I_{OUT} = 1 mA. Typical values apply for T_A = 25°C; minimum and maximum values apply over the full junction temperature range for operation, −40 to +125°C, unless otherwise specified.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TRANSIENT CHARACTERISTICS							
	Line transient response $\lvert\delta V_{OUT}\rvert$	T_{rise} = T_{fall} = 30 µs δV_{IN} = 600 mV			1		mV (pk - pk)
Transient response	Load transient response $\lvert\delta V_{OUT}\rvert$	T_{rise} = T_{fall} = 1 µs	I_{OUT} = 1 mA to 200 mA		80		mV
			I_{OUT} = 200 mA to 1 mA		70		
	Overshoot on start-up				0%	1%	

7.6 Timing Requirements

Nominal values apply for T_A = 25°C; minimim and maximum values apply over the full junction temperature range for operation, −40 to +125°C, unless otherwise specified.

		MIN	NOM	MAX	UNIT
T_{ON}	Turnon time to 95% level, $V_{OUT(NOM)}$		80	200	µs
T_{OFF}	Turnoff Time, 5% of $V_{OUT(NOM)}$, I_{OUT} = 0 mA		0.4	1	ms

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7.7 Typical Characteristics

Unless otherwise specified, C_{IN} = C_{OUT} = 1 µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1 V or 1.8 V, whichever is greater, T_A = 25°C, $V_{OUT(NOM)}$ = 2.85 V, and the EN pin is tied to V_{IN}.

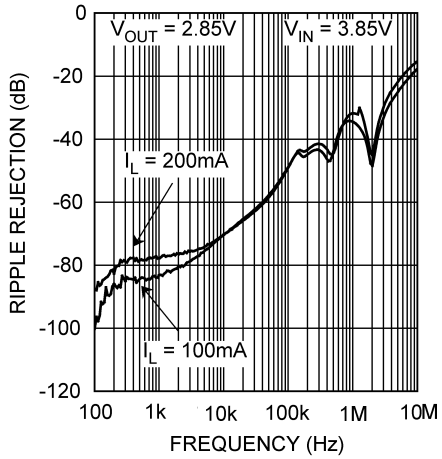


Figure 1. Power Supply Rejection Ratio

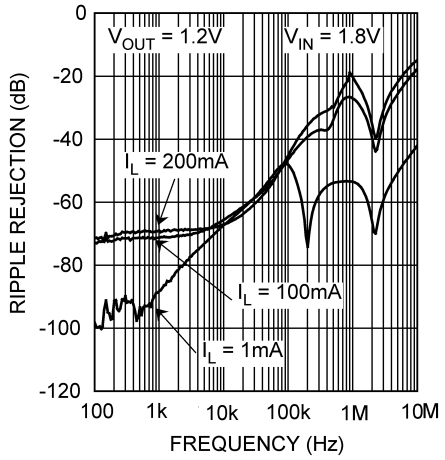


Figure 2. Power Supply Rejection Ratio

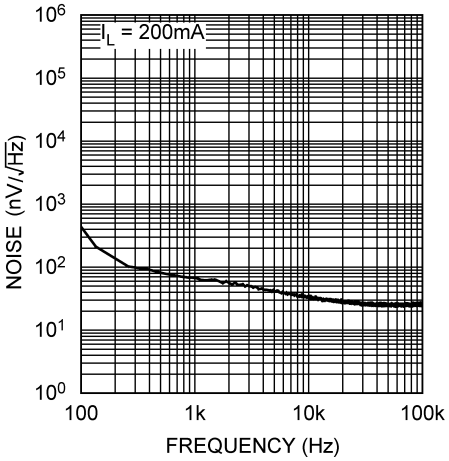


Figure 3. Noise Density

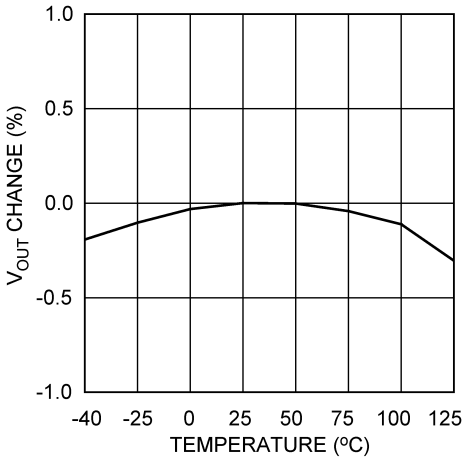


Figure 4. Output Voltage Change vs Temperature

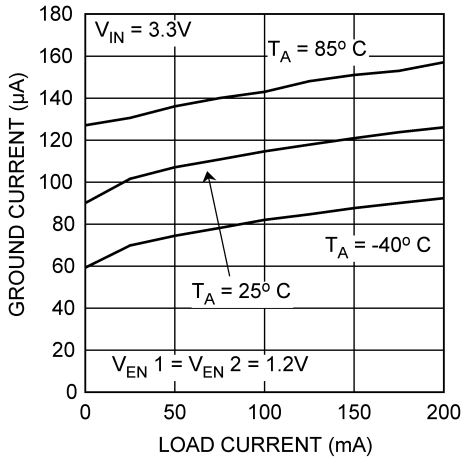


Figure 5. Ground Current vs Load Current

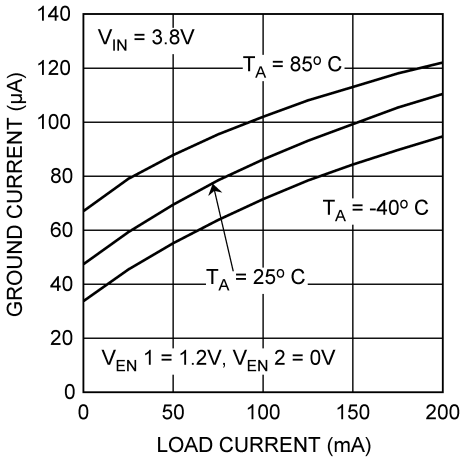


Figure 6. Ground Current vs Load Current

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Typical Characteristics (continued)

Unless otherwise specified, C_{IN} = C_{OUT} = 1 µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1 V or 1.8 V, whichever is greater, T_A = 25°C, $V_{OUT(NOM)}$ = 2.85 V, and the EN pin is tied to V_{IN}.

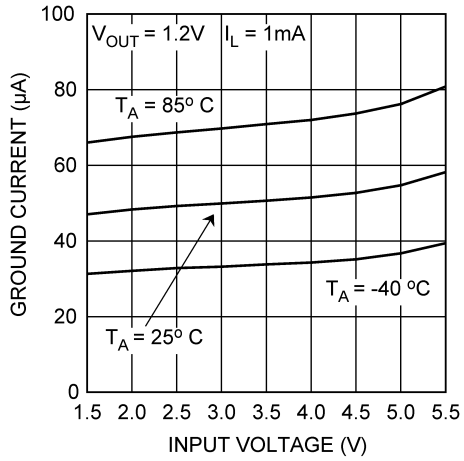


Figure 7. Ground Current vs V_{IN}

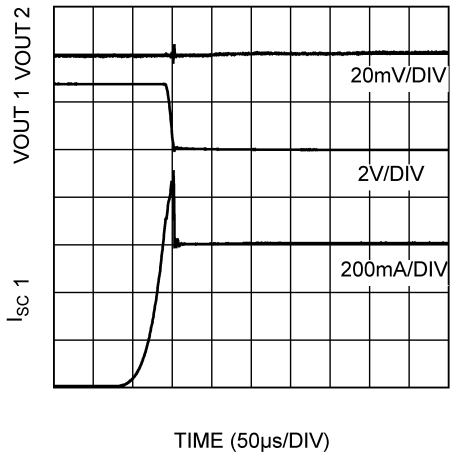


Figure 8. Short Circuit Current

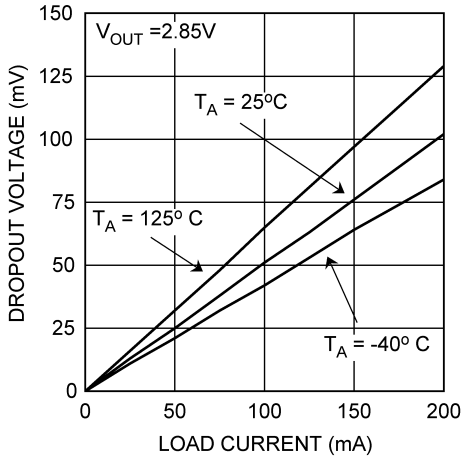


Figure 9. Dropout Voltage

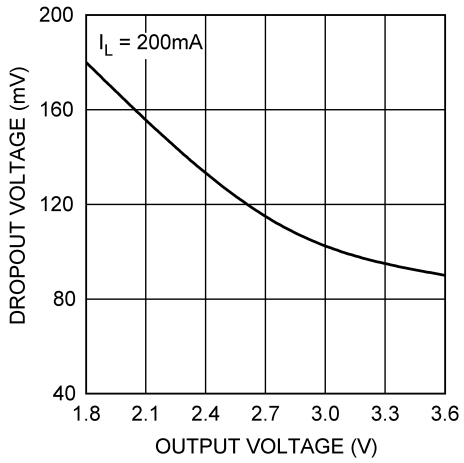


Figure 10. Dropout Voltage vs Output Voltage

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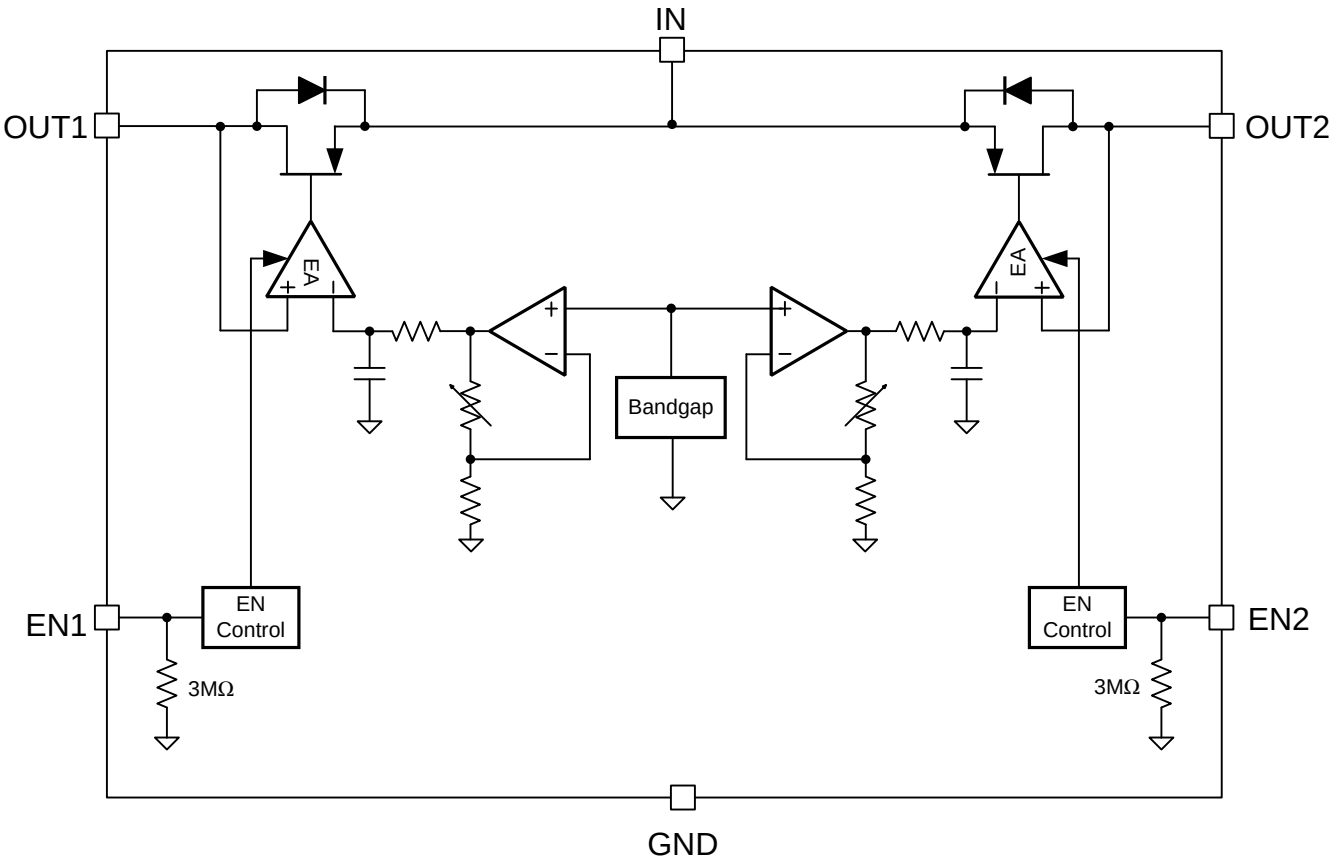
8 Detailed Description

8.1 Overview

The LP8900 is a dual linear regulator capable of supplying 200 mA output current per regulator. Designed to meet the requirements of RF and analog circuits, the LP8900 provides low device noise, high PSRR, low quiescent current, and superior line transient response figures.

Using new innovative design techniques the LP8900 offers class-leading device noise performance without a noise bypass capacitor. The LP8900 is designed to perform with a single 1-µF input capacitor and a single 1-µF ceramic output capacitor.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable Control

The LP8900 may be switched ON or OFF by a logic input at the EN pin. A high voltage at this pin turns the device on. When the enable pin is low, the regulator output is off and the device typically consumes 3 nA. However if the application does not require the shutdown feature, the EN pin can be tied to V_{IN} to keep the regulator permanently on. To ensure fast start-up is achieved, EN must be driven separately.

A 3-MΩ pulldown resister ties the EN input to ground, this ensures that the device remains off when the enable pin is left open circuit. To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turnon or turnoff voltage thresholds listed in *Electrical Characteristics* under V_{IL} and V_{IH}.

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8.4 Device Functional Modes

8.4.1 Enable (EN)

The LP8900 EN pin is internally held low by a 3-MΩ resistor to GND. The Enable pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions.

When the EN pin is pulled low, the output is off and the device typically consumes 3 nA.

8.4.2 Minimum Operating Input Voltage (V_{IN})

The LP8900 does not include any dedicated UVLO circuitry. The LP8900 internal circuitry is not fully functional until V_{IN} is at least 1.8 V. The output voltage is not regulated until V_{IN} has reached at least the greater of 1.8 V or (V_{OUT} + V_{DO}).

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP8900 is designed to meet the requirements of RF and analog circuits, providing low device noise, high PSRR, low quiescent current, and superior line transient response. The device offers class-leading device noise performance without a noise bypass capacitor and is stable with input and output capacitors with a value of 1 µF. The LP8900 delivers this performance in an industry standard DSBGA package which, for this device, is specified with an operating junction temperature (T_J) of –40°C to +125°C.

9.2 Typical Application

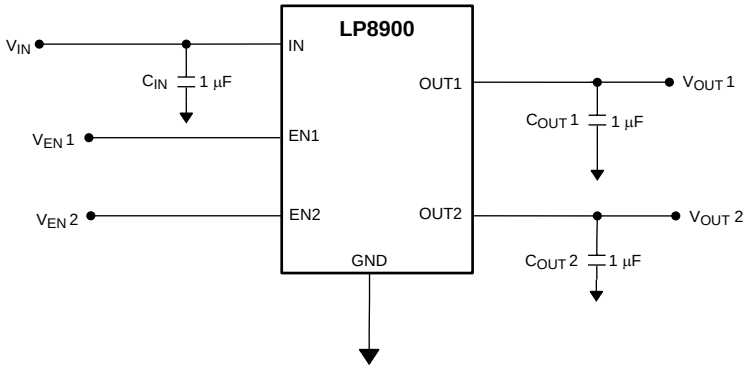


Figure 11. LP8900 Typical Application

Typical Application (continued)

9.2.1 Design Requirements

Some of the design requirements for this dual linear regulator include:

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	1.8 V
Minimum output voltage	1.2 V
Output current	200 mA/Channel

Table 2. Recommended Capacitor Specifications

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(1)	MAX(1)	UNIT
C_{IN}	Input capacitor	Capacitance(2)	0.33	1	10	µF
C_{OUT}	Output capacitor		0.33	1	4.7	µF
		ESR	5		500	mΩ

(1) Typical values apply for T_A = 25°C; minimim and maximum values apply over the full junction temperature range for operation, −40 to +125°C, unless otherwise specified.
(2) The capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R or X5R. (See *External Capacitors*.)

9.2.2 Detailed Design Procedure

9.2.2.1 External Capacitors

In common with most regulators, the LP8900 requires external capacitors for regulator stability. The LP8900 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

9.2.2.2 Input Capacitor

An input capacitor is required for stability. It is recommended that a 1-µF capacitor be connected between the LP8900 IN pin and ground. (This capacitance value may be increased to 10 µF.)

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance, temperature, and voltage coefficients must be considered when selecting the capacitor to ensure the capacitance remains ≅ 1 µF over the entire operating temperature range.

9.2.2.3 Output Capacitor

Correct selection of the output capacitor is critical to ensure stable operation in the intended application.

The output capacitor must meet all the requirements specified in the recommended capacitor table over all conditions in the application. These conditions include DC bias, frequency and temperature. Unstable operation results if the capacitance drops below the minimum specified value.

The LP8900 is designed specifically to work with very small ceramic output capacitors. A 1-µF ceramic capacitor (dielectric type X7R or X5R) with an ESR between 5 mΩ to 500 mΩ, is suitable in the LP8900 application circuit.

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Other ceramic types such as Y5V and Z5U are less suitable owing to their inferior temperature characteristics. (See *Capacitor Characteristics*.)

It is also recommended that the output capacitor is placed within 1 cm of the output pin and returned to a clean, low impedance, ground connection.

It is possible to use tantalum or film capacitors at the device output, OUT, but these are not as attractive for reasons of size and cost. (See *Capacitor Characteristics*.)

9.2.2.4 No-Load Stability

The LP8900 remains stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

9.2.2.5 Capacitor Characteristics

The LP8900 is designed to work with ceramic capacitors on the input and outputs to take advantage of the benefits they offer. For capacitance values around 1 µF, ceramic capacitors give the circuit designer the best design options in terms of low cost and minimal area.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly dependant on the conditions of operation and capacitor type.

In particular, to ensure stability, the output capacitor selection must take account of all the capacitor parameters, to ensure that the specification is met within the application. Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values may also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller sizes giving poorer performance figures in general.

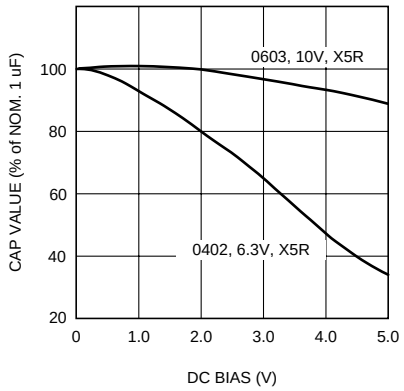


Figure 12. Effect of DC Bias on Capacitance Value

As an example Figure 12 shows a typical graph showing a comparison of capacitor case sizes in a capacitance vs. DC bias plot. As shown in Figure 12, as a result of the DC bias condition, the capacitance value may drop below the minimum capacitance value given in Table 2. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions as some capacitor sizes (for example, 0402) may not be suitable in the actual application. Ceramic capacitors have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 4.7-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP8900. The temperature performance of ceramic capacitors varies by type. Capacitor type X7R is specified with a tolerance of ±15% over the temperature range –55°C to +125°C. The X5R has a similar tolerance over the reduced temperature range of –55°C to +85°C. Some large value ceramic capacitors (4.7 µF) are manufactured with Z5U or Y5V temperature characteristics, which can result in the capacitance dropping by more than 50% as the temperature varies from 25°C to 85°C. Therefore, X7R or X5R types are recommended in applications where the temperature changes significantly above or below 25°C.

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Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 4.7-µF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. The ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

9.2.3 Application Curves

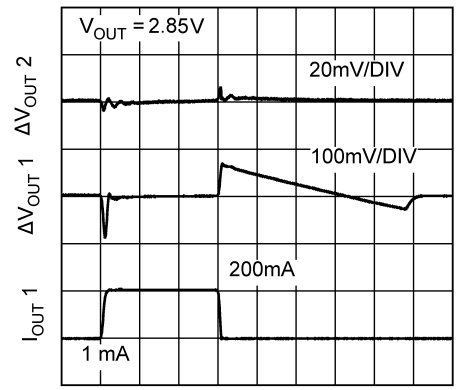


Figure 13. OUT1 Load Transient

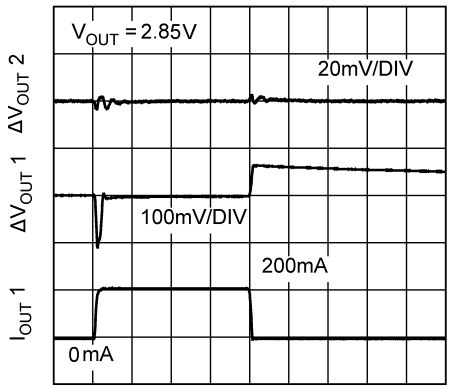


Figure 14. OUT1 Load Transient

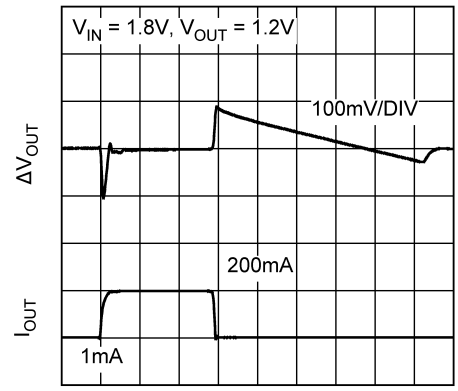


Figure 15. Load Transient

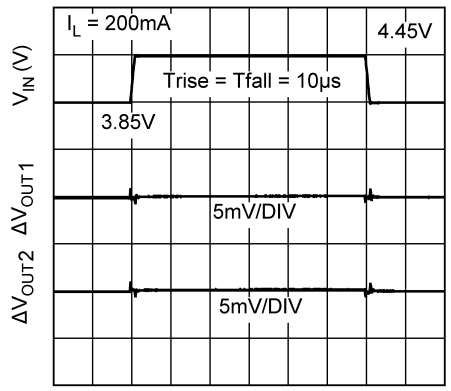


Figure 16. Line Transient

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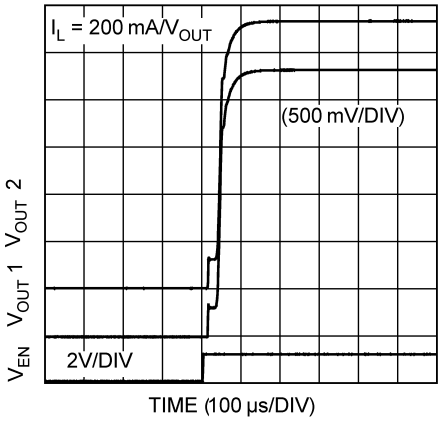


Figure 17. Enable Start-Up Characteristics

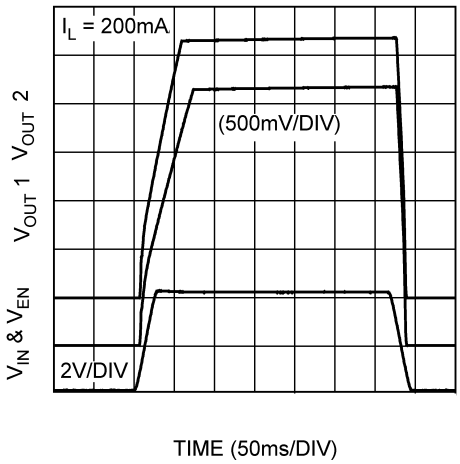


Figure 18. V_{IN} and EN Tied Together

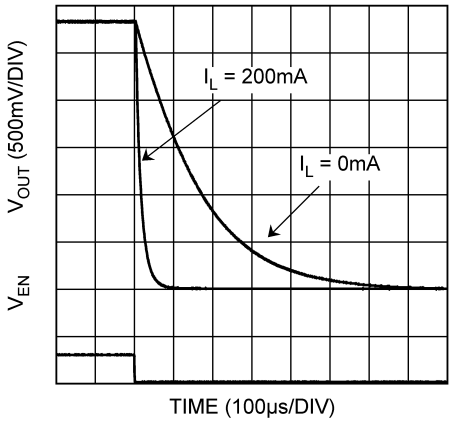


Figure 19. Shutdown Characteristics

10 Power Supply Recommendations

The LP8900 device is designed to operate from an input voltage supply range from 1.8 V to 5.5 V. This input supply must be well regulated. A minimum capacitor value of 1 µF is required to be within 1 cm of the IN pin.

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11 Layout

11.1 Layout Guidelines

The dynamic performance of the LP8900 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP8900.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the device, and placing them as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} must be back to the LP8900 ground pin using as wide and as short of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through vias must be avoided. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

11.2 Layout Example

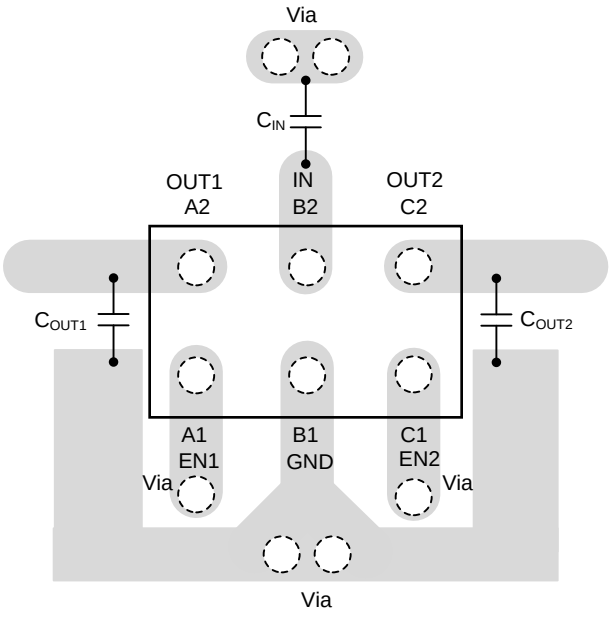


Figure 20. LP8900 Example Layout

11.3 DSBGA Mounting

The DSBGA package requires specific mounting techniques which are detailed in the TI Application Note (AN-1112) *DSBGA Wafer Level Chip Scale Package* (SNVA009). Referring to the section *Surface Mount Technology (SMT) Assembly Considerations*, the pad style that must be used with the 6-pin package is a NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PCB may be used to facilitate placement of the DSBGA device.

11.4 DSBGA Light Sensitivity

Exposing the DSBGA device to direct sunlight may cause mis-operation of the device. Light sources such as halogen lamps can affect the electrical performance if brought near to the device.

The wavelengths that have the most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has little effect on performance.

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

AN-1112 DSBGA Wafer Level Chip Scale Package (SNVA009)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8900TLE-3333/NOPB	ACTIVE	DSBGA	YZR	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		B	Samples
LP8900TLE-AAAH/NOPB	ACTIVE	DSBGA	YZR	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		3	Samples
LP8900TLE-AAEC/NOPB	ACTIVE	DSBGA	YZR	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
LP8900TLX-3333/NOPB	ACTIVE	DSBGA	YZR	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

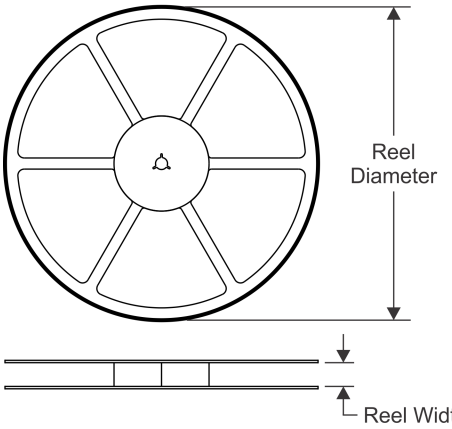
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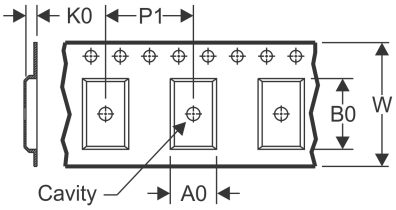
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

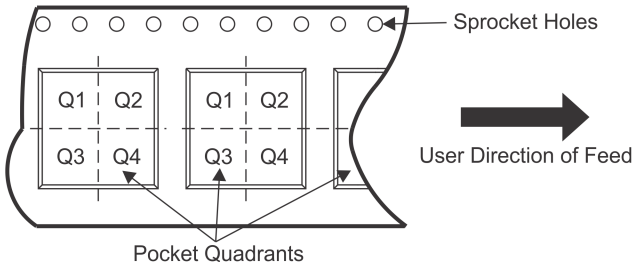


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

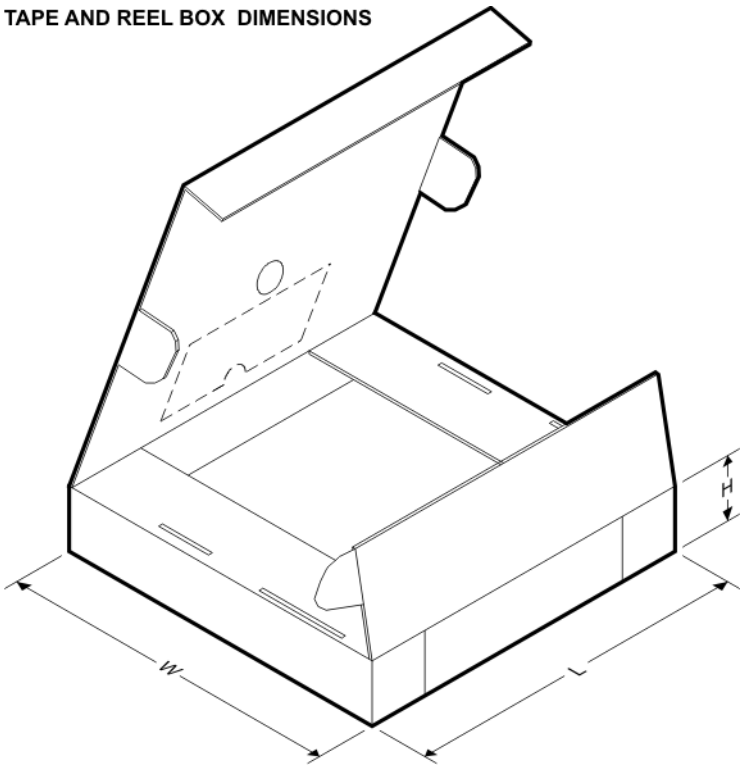
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8900TLE-3333/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.15	1.63	0.7	4.0	8.0	Q1
LP8900TLE-AAAH/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.15	1.63	0.7	4.0	8.0	Q1
LP8900TLE-AAEC/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.15	1.63	0.7	4.0	8.0	Q1
LP8900TLX-3333/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.15	1.63	0.7	4.0	8.0	Q1

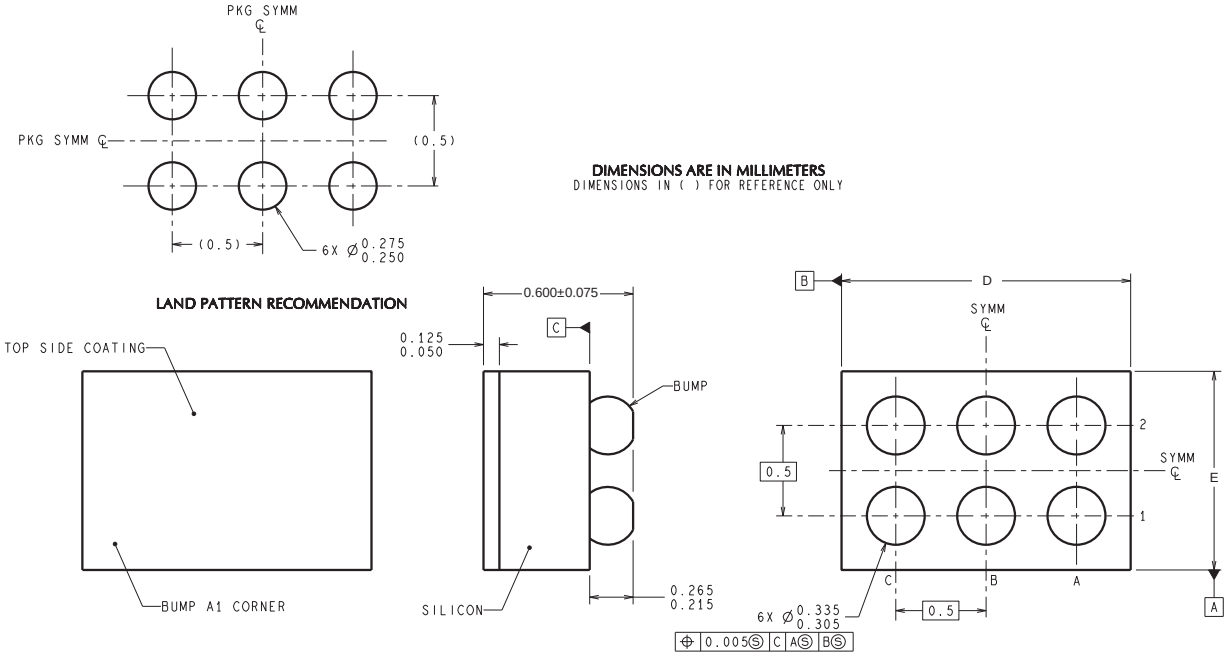
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8900TLE-3333/NOPB	DSBGA	YZR	6	250	208.0	191.0	35.0
LP8900TLE-AAAH/NOPB	DSBGA	YZR	6	250	208.0	191.0	35.0
LP8900TLE-AAEC/NOPB	DSBGA	YZR	6	250	208.0	191.0	35.0
LP8900TLX-3333/NOPB	DSBGA	YZR	6	3000	208.0	191.0	35.0

YZR0006



TLA06XXX (Rev C)

D: Max = 1.49 mm, Min = 1.43 mm

E: Max = 1.09 mm, Min = 1.03 mm

4215044/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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