TEXAS INSTRUMENTS

LM2651

SNVS032E – FEBRUARY 2000 – REVISED JANUARY 2016

LM2651 1.5 A High-Efficiency Synchronous Switching Regulator

1 Features

- Ultrahigh Efficiency up to 97%
- High-Efficiency Over a 1.5-A to 1.5-mA Load Range
- 4-V to 14-V Input Voltage Range
- 1.8-V, 2.5-V, 3.3-V, or ADJ Output Voltage
- Internal MOSFET Switch With Low $R_{DS(on)}$ of 75 mΩ
- 300-kHz Fixed Frequency Internal Oscillator
- 7-µA Shutdown Current
- Patented Current Sensing for Current Mode Control
- Input Undervoltage Lockout
- Adjustable Soft-Start
- Current Limit and Thermal Shutdown
- 16-Pin TSSOP Package

2 Applications

- Personal Digital Assistants (PDAs)
- Computer Peripherals
- Battery-Powered Devices
- Handheld Scanners
- High-Efficiency 5-V Conversion

3 Description

The LM2651 switching regulator provides high-efficiency power conversion over a 100:1 load range (1.5 A to 15 mA). This feature makes the LM2651 an ideal fit in battery-powered applications that demand long battery life in both run and standby modes.

Synchronous rectification is used to achieve up to 97% efficiency. At light loads, the LM2651 enters a low power hysteretic or *sleep* mode to maintain high efficiency. In many applications, the efficiency still exceeds 80% at 15-mA load. A shutdown pin is available to disable the LM2651 and reduce the supply current to less than 10 µA.

The LM2651 contains a patented current sensing circuitry for current mode control. This feature eliminates the external current sensing resistor required by other current-mode DC-DC converters.

The LM2651 has a 300-kHz fixed frequency internal oscillator. The high oscillator frequency allows the use of extremely small, low-profile components.

A programmable soft-start feature limits current surges from the input power supply at start-up and provides a simple means of sequencing multiple power supplies.

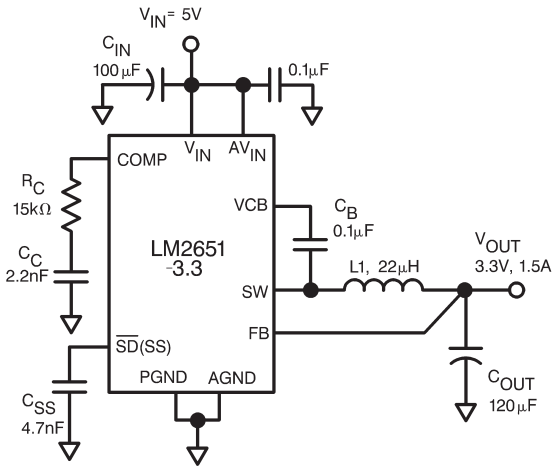
Other protection features include input undervoltage lockout, current limiting, and thermal shutdown.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2651	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision D (April 2013) to Revision E **Page**

- Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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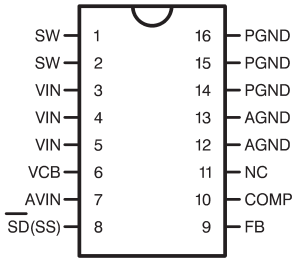
5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1, 2	SW	O	Switched-node connection, which is connected with the source of the internal high-side MOSFET.
3 to 5	VIN	I	Main power supply pin
6	VCB	I	Bootstrap capacitor connection for high-side gate drive
7	AVIN	I	Input supply voltage for control and driver circuits
8	$\overline{SD}$(SS)	I	Shutdown and soft-start control pin. Pulling this pin below 0.3 V shuts off the regulator. A capacitor connected from this pin to ground provides a control ramp of the input current. Do not drive this pin with an external source or erroneous operation may result.
9	FB	I	Output voltage feedback input. Connected to the output voltage.
10	COMP	I	Compensation network connection. Connected to the output of the voltage error amplifier.
11	NC	G	No internal connection
12 to 13	AGND	G	Low-noise analog ground
14 to 16	PGND	G	Power ground

(1) I = Input, O = Output, and G = Ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Input voltage		15	V
Feedback pin voltage	−0.4	5	V
Power dissipation (T_A = 25°C)(3)		893	mW
Junction temperature, T_J	−40	125	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The maximum allowable power dissipation is calculated by using $P_{Dmax} = (T_{Jmax} – T_A) / \theta_{JA}$, where T_{Jmax} is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance of the specified package. The 893-mW rating results from using 150°C, 25°C, and 140°C/W for T_{Jmax}, T_A, and θ_{JA} respectively. A θ_{JA} of 140°C/W represents the worst-case condition of no heat sinking of the 16-pin TSSOP package. Heat sinking allows the safe dissipation of more power. The absolute maximum power dissipation must be derated by 7.1 4 mW per °C above 25°C ambient. The LM2651 actively limits its junction temperature to about 165°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	4		14	V

6.4 Thermal Information

THERMAL METRIC(1)		LM2651 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

specifications are T_J = 25°C and V_{IN} = 10 V (unless otherwise specified)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
LM2651-1.8							
V_{OUT}	Output voltage	I_{LOAD} = 900 mA	T_J = 25°C	1.761	1.8	1.836	V
			Over full operating junction temperature range	1.719		1.854	
	Output voltage line regulation	V_{IN} = 4 V to 14 V, I_{LOAD} = 900 mA			0.2%		
	Output voltage load regulation	I_{LOAD} = 10 mA to 1.5 A, V_{IN} = 5 V			1.3%		
		I_{LOAD} = 200 mA to 1.5 A, V_{IN} = 5 V			0.3%		
V_{HYST}	Sleep mode output voltage hysteresis				35		mV
LM2651-2.5							
V_{OUT}	Output voltage	I_{LOAD} = 900 mA	T_J = 25°C	2.43	2.5	2.574	V
			Over full operating junction temperature range	2.388		2.575	
	Output voltage line regulation	V_{IN} = 4 V to 12 V, I_{LOAD} = 900 mA			0.2%		
	Output voltage load regulation	I_{LOAD} = 10 mA to 1.5 A, V_{IN} = 5 V			1.3%		
		I_{LOAD} = 200 mA to 1.5 A, V_{IN} = 5 V			0.3%		
V_{HYST}	Sleep mode output voltage hysteresis				48		mV
LM2651-3.3							
V_{OUT}	Output voltage	I_{LOAD} = 900 mA	T_J = 25°C	3.265	3.3	3.379	V
			Over full operating junction temperature range	3.201		3.399	
	Output voltage line regulation	V_{IN} = 4 V to 14 V, I_{LOAD} = 900 mA			0.2%		
	Output voltage load regulation	I_{LOAD} = 10 mA to 1.5 A, V_{IN} = 5 V			1.3%		
		I_{LOAD} = 200 mA to 1.5 A, V_{IN} = 5 V			0.3%		
V_{HYST}	Sleep mode output voltage hysteresis				60		mV
LM2651-ADJ(3)							
V_{FB}	Feedback voltage	I_{LOAD} = 900 mA	T_J = 25°C		1.238		V
			Over full operating junction temperature range	1.2		1.263	
V_{OUT}	Output voltage line regulation	V_{IN} = 4 V to 14 V, I_{LOAD} = 900 mA			0.2%		
	Output voltage load regulation	I_{LOAD} = 10 mA to 1.5 A, V_{IN} = 5 V			1.3%		
		I_{LOAD} = 200 mA to 1.5 A, V_{IN} = 5 V			0.3%		
V_{HYST}	Sleep mode output voltage hysteresis				24		mV
ALL OUTPUT VOLTAGE VERSIONS							
I_Q	Quiescent current	T_J = 25°C			1.6		mA
		Over full operating junction temperature range				2	
I_{QSD}	Quiescent current in shutdown mode	Shutdown pin pulled low	T_J = 25°C		7	12	µA
			Over full operating junction temperature range			20	

(1) All limits are ensured at room temperature (standard typeface) and at temperature extremes. All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) V_{OUT} = 2.5 V

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Electrical Characteristics (continued)

specifications are T_J = 25°C and V_{IN} = 10 V (unless otherwise specified)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
$R_{SW(ON)}$	High-Side or low-side switch on resistance (MOSFET on resistance + bonding wire resistance)	I_{SWITCH} = 1 A			110		mΩ
$R_{DS(ON)}$	MOSFET on resistance (high-side or low-side)	I_{SWITCH} = 1 A	T_J = 25°C		75		mΩ
			Over full operating junction temperature range			130	
I_L	Switch leakage current - high side				130		nA
	Switch leakage current - low side				130		
V_{BOOT}	Bootstrap regulator voltage	I_{BOOT} = 1 mA	T_J = 25°C	6.45	6.75	6.95	V
			Over full operating junction temperature range	6.4		7	
G_M	Error amplifier transconductance				1250		µmho
V_{INUV}	V_{IN} undervoltage lockout threshold voltage	Rising edge	T_J = 25°C		3.8		V
			Over full operating junction temperature range			3.95	
$V_{UV-HYST}$	Hysteresis for the undervoltage lockout				210		mV
I_{CL}	Switch current limit	V_{IN} = 5 V	T_J = 25°C		2		A
			Over full operating junction temperature range	1.55		2.6	
I_{SM}	Sleep mode threshold current	V_{IN} = 5 V			100		mA
A_V	Error amplifier voltage gain				100		V/V
I_{EA_SOURCE}	Error amplifier source current	T_J = 25°C		25	40		µA
		Over full operating junction temperature range		15			
I_{EA_SINK}	Error amplifier sink current	T_J = 25°C			65		µA
		Over full operating junction temperature range		30			
V_{EAH}	Error amplifier output swing upper limit	T_J = 25°C		2.5	2.7		V
		Over full operating junction temperature range		2.4			
V_{EAL}	Error amplifier output swing lower limit	T_J = 25°C			1.25	1.35	V
		Over full operating junction temperature range				1.5	
V_D	Body diode voltage	I_{DIODE} = 1.5 A			1		V
f_{OSC}	Oscillator frequency	V_{IN} = 4 V	T_J = 25°C	280	300	330	kHz
			Over full operating junction temperature range	255		345	
D_{MAX}	Maximum duty cycle	V_{IN} = 4 V	T_J = 25°C		95%		
			Over full operating junction temperature range	92%			
I_{SS}	Soft-Start current	Voltage at the SS pin = 1.4 V	T_J = 25°C		11		µA
			Over full operating junction temperature range	7		14	

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Electrical Characteristics (continued)

specifications are T_J = 25°C and V_{IN} = 10 V (unless otherwise specified)[1]

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
$I_{SHUTDOWN}$	Shutdown pin current	Shutdown pin pulled low	T_J = 25°C	0.8	2.2	3.7	µA
			Over full operating junction temperature range	0.5		4	
$V_{SHUTDOWN}$	Shutdown pin threshold voltage	Falling edge	T_J = 25°C		0.6		V
			Over full operating junction temperature range	0.3		0.9	
T_{SD}	Thermal shutdown temperature				165		°C
T_{SD_HYST}	Thermal shutdown hysteresis temperature				25		°C

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6.6 Typical Characteristics

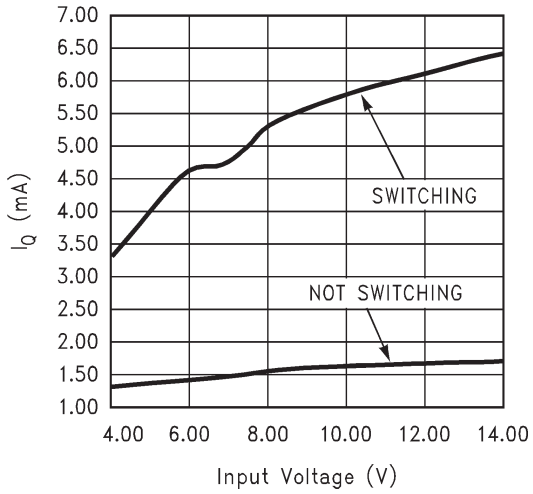

Figure 1. I_Q vs Input Voltage

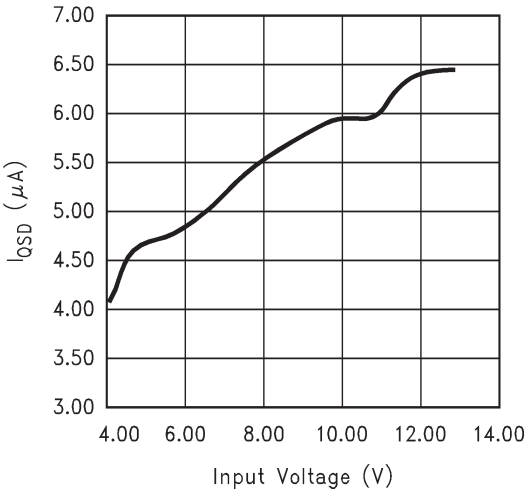

Figure 2. I_{QSD} vs Input Voltage

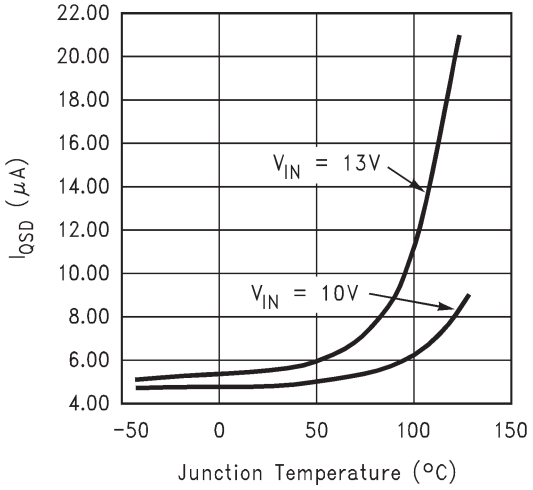

Figure 3. I_{QSD} vs Junction Temperature

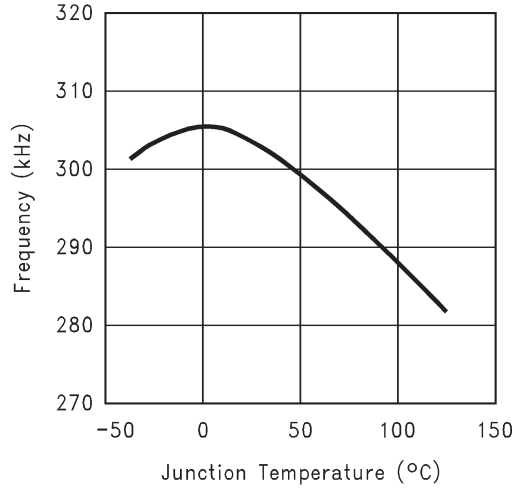

Figure 4. Frequency vs Junction Temperature

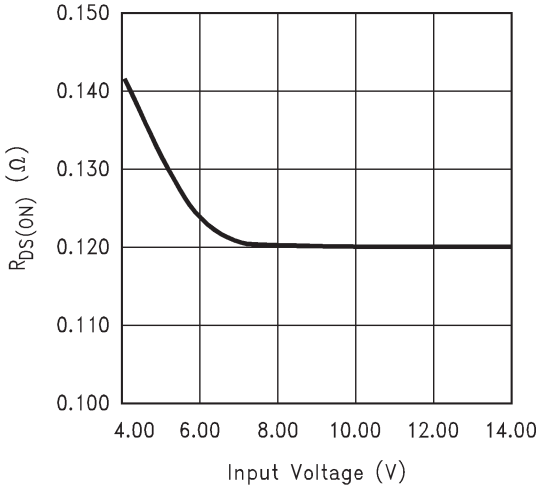

Figure 5. $R_{DS(ON)}$ vs Input Voltage

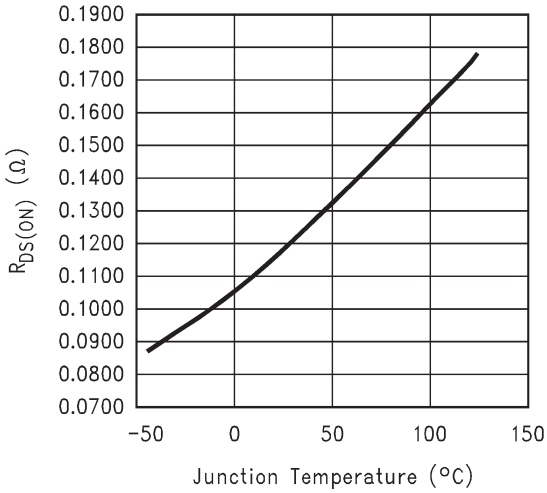

Figure 6. $R_{DS(ON)}$ vs Junction Temperature

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Typical Characteristics (continued)

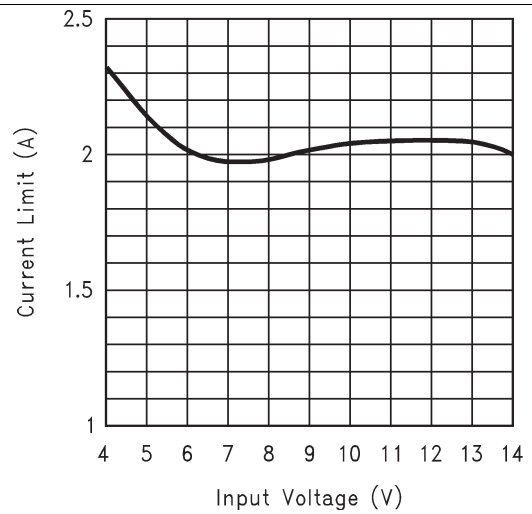

Figure 7. Current Limit vs Input Voltage (V_{OUT} = 2.5 V)

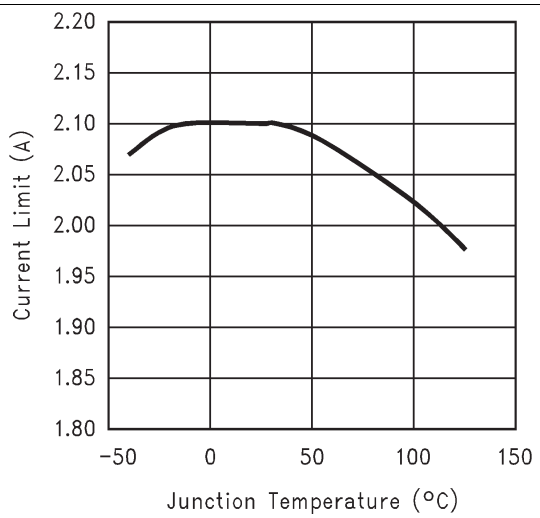

Figure 8. Current Limit vs Junction Temperature (V_{OUT} = 2.5 V)

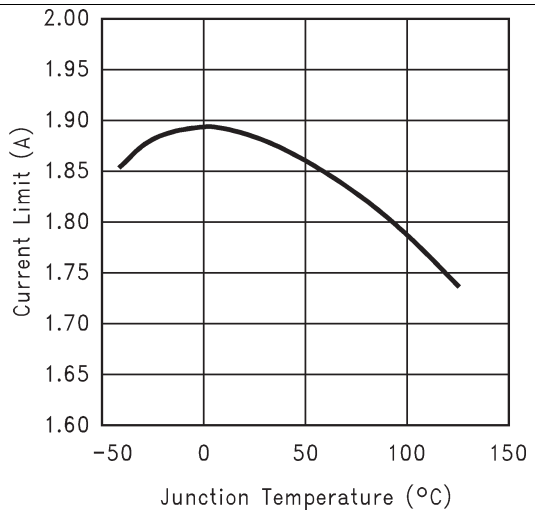

Figure 9. Current Limit vs Junction Temperature (V_{OUT} = 3.3 V)

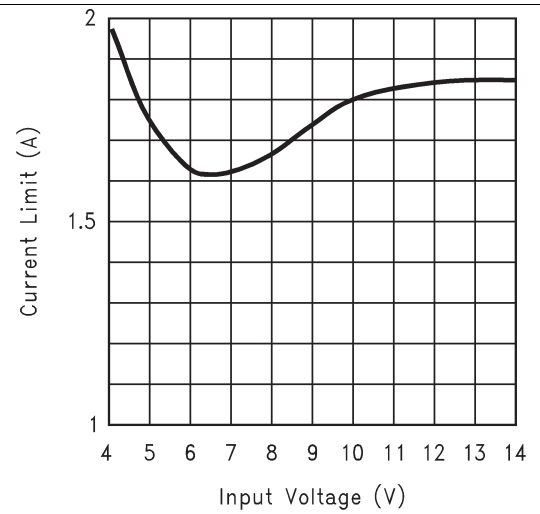

Figure 10. Current Limit vs Input Voltage (V_{OUT} = 3.3 V)

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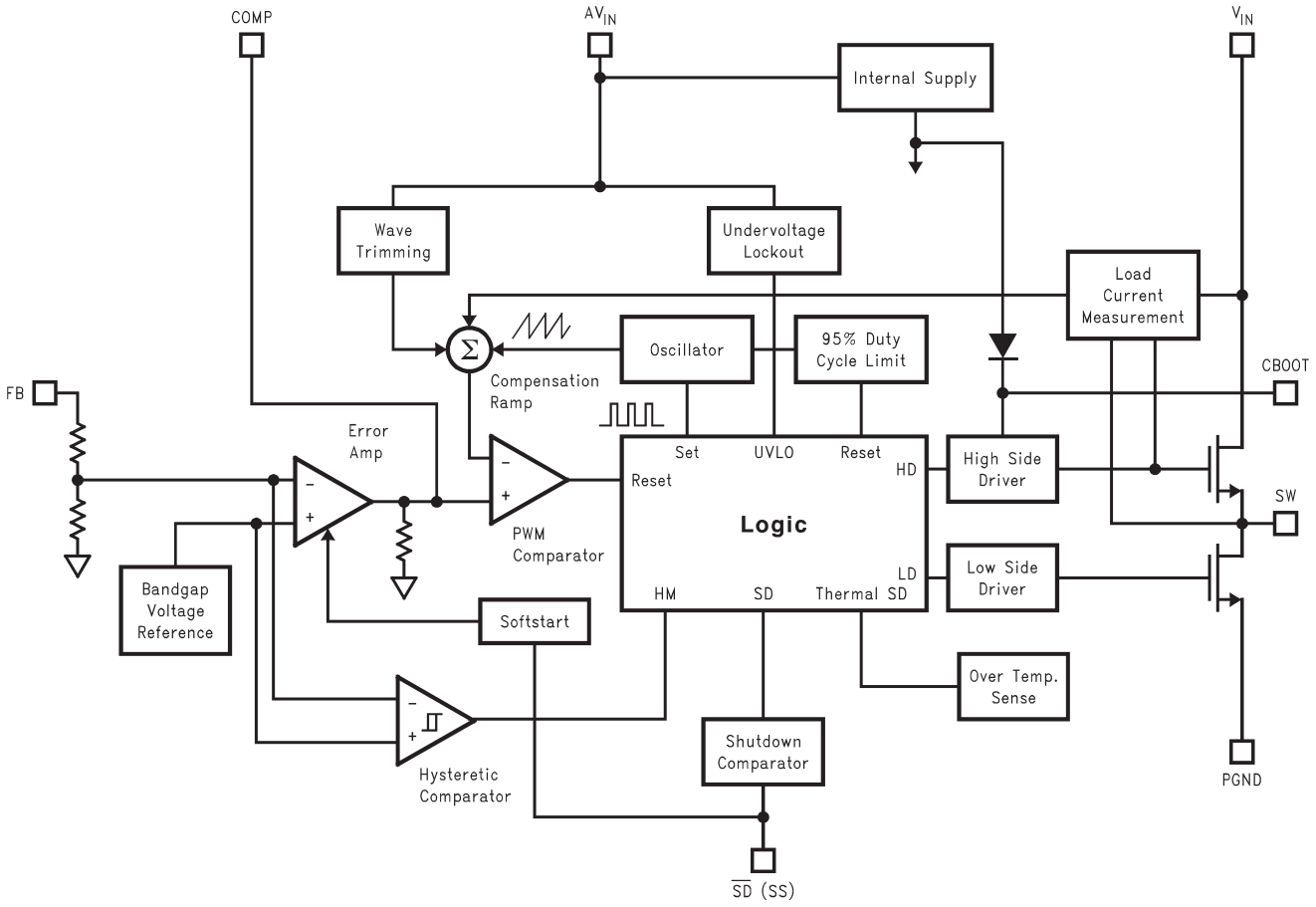
7 Detailed Description

7.1 Overview

The LM2651 operates in a constant frequency (300 kHz), current-mode PWM for moderate to heavy loads, and automatically switches to hysteretic mode for light loads. In hysteretic mode, the switching frequency is reduced to maintain high efficiency.

7.2 Functional Block Diagram



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7.3 Feature Description

When the load current is higher than the sleep mode threshold, the part is always operating in PWM mode. At the beginning of each switching cycle, the high-side switch is turned on, the current from the high-side switch is sensed and compared with the output of the error amplifier (COMP pin). When the sensed current reaches the COMP pin voltage level, the high-side switch is turned off; after 40 ns (deadtime), the low-side switch is turned on. At the end of the switching cycle, the low-side switch is turned off; and the same cycle repeats.

When the load current decreases below the sleep mode threshold, the output voltage rises slightly, this rise is sensed by the hysteretic mode comparator which makes the part go into the hysteretic mode with both the high and low side switches off. The output voltage starts to drop until it hits the low threshold of the hysteretic comparator, and the part immediately goes back to the PWM operation. The output voltage keeps increasing until it reaches the top hysteretic threshold, then both the high- and low-side switches turn off again, and the cycle repeats.

7.4 Device Functional Modes

The cycle-by-cycle current limit circuitry turns off the high-side MOSFET whenever the current in MOSFET reaches 2 A. A shutdown pin is available to disable the LM2651 and reduce the supply current to 7 µA.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

LM2651 operates in a constant frequency (300 kHz), current-mode PWM for moderate to heavy loads; and it automatically switches to hysteretic mode for light loads. The current of the top switch is sensed by a patented internal circuitry. This unique technique gets rid of the external sense resistor, saves cost and size, and improves noise immunity of the sensed current. A feed forward from the input voltage is added to reduce the variation of the current limit over the input voltage range.

8.2 Typical Application

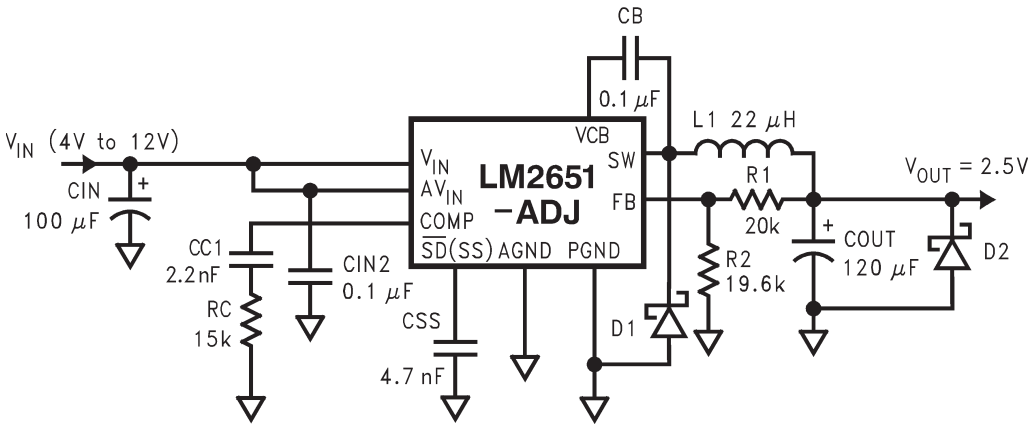

Figure 11. Schematic for the Typical Board Layout

8.2.1 Design Requirements

To properly size the components for the application, the designer needs the following parameters: input voltage range, output voltage, output current range, and the switching frequency. These four main parameters affect the choices of component available to achieve a proper system behavior. TI recommends a Schottky diode to prevent the intrinsic body diode of the low-side MOSFET from conducting during deadtime. See *Detailed Design Procedure* for more information.

8.2.2 Detailed Design Procedure

This section presents guidelines for selecting external components.

8.2.2.1 Input Capacitor

A low ESR aluminum, tantalum, or ceramic capacitor is needed between the input pin and power ground. This capacitor prevents large voltage transients from appearing at the input. The capacitor is selected based on the RMS current and voltage requirements. The RMS current is given by Equation 1.

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \quad (1)$$

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Typical Application (continued)

The RMS current reaches its maximum ($I_{OUT}/2$) when V_{IN} equals 2 V_{OUT}. For an aluminum or ceramic capacitor, the voltage rating should be at least 25% higher than the maximum input voltage. If a tantalum capacitor is used, the voltage rating required is about twice the maximum input voltage. The tantalum capacitor should be surge-current tested by the manufacturer to prevent being shorted by the inrush current. TI also recommends putting a small ceramic capacitor (0.1 µF) between the input pin and ground pin to reduce high-frequency spikes.

8.2.2.2 Inductor

The most critical parameters for the inductor are the inductance, peak current, and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input and the output voltages, as given by Equation 2.

$$L = \frac{(V_{IN} - V_{OUT})V_{OUT}}{V_{IN} \times I_{RIPPLE} \times 300\ kHz} \quad (2)$$

A higher value of ripple current reduces inductance, but increases the conductance loss, core loss, current stress for the inductor and switch devices. It also requires a bigger output capacitor for the same output voltage ripple requirement. A reasonable value is setting the ripple current to be 30% of the DC output current. Since the ripple current increases with the input voltage, the maximum input voltage is always used to determine the inductance. The DC resistance of the inductor is a key parameter for the efficiency. Lower DC resistance is available with a bigger winding area. A good tradeoff between the efficiency and the core size is letting the inductor copper loss equal 2% of the output power.

8.2.2.3 Output Capacitor

The selection of C_{OUT} is driven by the maximum allowable output voltage ripple. The output ripple in the constant frequency, PWM mode is approximated by using Equation 3.

$$V_{RIPPLE} = I_{RIPPLE}\left(ESR + \frac{1}{8F_S C_{OUT}}\right) \quad (3)$$

The ESR term usually plays the dominant role in determining the voltage ripple. A low ESR aluminum electrolytic or tantalum capacitor (such as Nichicon PL series, Sanyo OS-CON, Sprague 593D, 594D, AVX TPS, and CDE polymer aluminum) is recommended. An electrolytic capacitor is not recommended for temperatures below −25°C since its ESR rises dramatically at cold temperature. A tantalum capacitor has a much better ESR specification at cold temperature and is preferred for low temperature applications.

The output voltage ripple in constant frequency mode has to be less than the sleep mode voltage hysteresis to avoid entering the sleep mode at full load as given by Equation 4.

$$V_{RIPPLE} < 20\ mV \times V_{OUT} / V_{FB} \quad (4)$$

8.2.2.4 Boost Capacitor

TI recommends a 0.1-µF ceramic capacitor for the boost capacitor. The typical voltage across the boost capacitor is 6.7 V.

8.2.2.5 Soft-Start Capacitor

A soft-start capacitor is used to provide the soft-start feature. When the input voltage is first applied, or when the $\overline{SD}$(SS) pin is allowed to go high, the soft-start capacitor is charged by a current source (approximately 2 µA). When the $\overline{SD}$(SS) pin voltage reaches 0.6 V (shutdown threshold), the internal regulator circuitry starts to operate. The current charging the soft-start capacitor increases from 2 µA to approximately 10 µA. With the $\overline{SD}$(SS) pin voltage between 0.6 V and 1.3 V, the level of the current limit is zero, which means the output voltage is still zero. When the $\overline{SD}$(SS) pin voltage increases beyond 1.3 V, the current limit starts to increase. The switch duty cycle, which is controlled by the level of the current limit, starts with narrow pulses and gradually gets wider. At the same time, the output voltage of the converter increases towards the nominal value, which brings down the output voltage of the error amplifier. When the output of the error amplifier is less than the current limit voltage, it takes over the control of the duty cycle. The converter enters the normal current-mode PWM operation. The $\overline{SD}$(SS) pin voltage is eventually charged up to about 2 V.

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Typical Application (continued)

The soft-start time can be estimated using Equation 5.

$$T_{SS} = C_{SS} \times 0.6\ V/2\ \mu A + C_{SS} \times (2\ V - 0.6\ V)/10\ \mu A \quad (5)$$

8.2.2.6 R_1 and R_2 (Programming Output Voltage)

Use Equation 6 to select the appropriate resistor values.

$$V_{OUT} = V_{REF}(1 + R_1/R_2)$$

where

- $V_{REF} = 1.238\ V$ (6)

Select resistors between 10 kΩ and 100 kΩ. (1% or higher accuracy metal film resistors for R_1 and R_2.)

8.2.2.7 Compensation Components

In the control to output transfer function, the first pole F_{p1} can be estimated as $1/(2\pi R_{OUT}C_{OUT})$; The ESR zero F_{z1} of the output capacitor is $1/(2\pi ESRC_{OUT})$; Also, there is a high-frequency pole F_{p2} in the range of 45 kHz to 150 kHz as given by Equation 7.

$$F_{p2} = F_s/(\pi n(1-D))$$

where

- $D = V_{OUT}/V_{IN}$
- $n = 1+0.348L/(V_{IN}-V_{OUT})$ (L is in µHs and V_{IN} and V_{OUT} in volts). (7)

The total loop gain G is approximately $500/I_{OUT}$ where I_{OUT} is in amperes.

A Gm amplifier is used inside the LM2651. The output resistor R_o of the Gm amplifier is about 80 kΩ. C_{c1} and R_C together with R_o give a lag compensation to roll off the gain as given by Equation 8.

$$F_{pc1} = 1/(2\pi C_{c1}(R_o+R_c)),\ F_{zc1} = 1/2\pi C_{c1}R_c. \quad (8)$$

In some applications, the ESR zero F_{z1} cannot be cancelled by F_{p2}. Then, C_{c2} is needed to introduce F_{pc2} to cancel the ESR zero, $F_{p2} = 1/(2\pi C_{c2}R_o \| R_c)$.

The rule of thumb is to have more than 45° phase margin at the crossover frequency (G = 1).

If C_{OUT} is higher than 68 µF, C_{c1} = 2.2 nF, and R_c = 15 kΩ are good choices for most applications. If the ESR zero is too low to be cancelled by F_{p2}, add C_{c2}.

If the transient response to a step load is important, choose R_C to be higher than 10 kΩ.

8.2.2.8 External Schottky Diode

TI recommends a Schottky diode D_1 to prevent the intrinsic body diode of the low-side MOSFET from conducting during the deadtime in PWM operation and hysteretic mode when both MOSFETs are off. If the body diode turns on, there is extra power dissipation in the body diode because of the reverse-recovery current and higher forward voltage; the high-side MOSFET also has more switching loss since the negative diode reverse-recovery current appears as the high-side MOSFET turnon current in addition to the load current. These losses degrade the efficiency by 1–2%. The improved efficiency and noise immunity with the Schottky diode become more obvious with increasing input voltage and load current.

The breakdown voltage rating of D_1 is preferred to be 25% higher than the maximum input voltage. Since D_1 is only on for a short period of time, the average current rating for D_1 only requires being higher than 30% of the maximum output current. It is important to place D_1 very close to the drain and source of the low-side MOSFET, extra parasitic inductance in the parallel loop slows the turnon of D_1 and direct the current through the body diode of the low-side MOSFET.

When an undervoltage situation occurs, the output voltage can be pulled below ground as the inductor current is reversed through the synchronous FET. For applications that require protection from a negative voltage, TI recommends a clamping diode D2. When used, D2 should be connected cathode to V_{OUT} and anode to ground. TI recommends a diode rated for a minimum of 2 A.

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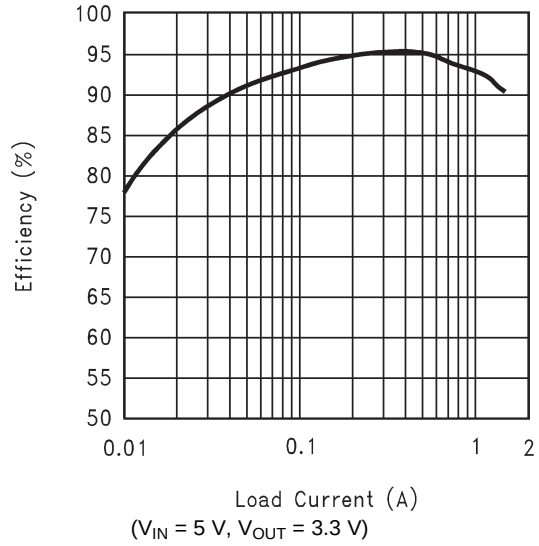
Typical Application (continued)

8.2.3 Application Curves



(V_{IN} = 5 V, V_{OUT} = 3.3 V)

Figure 12. Efficiency vs Load Current

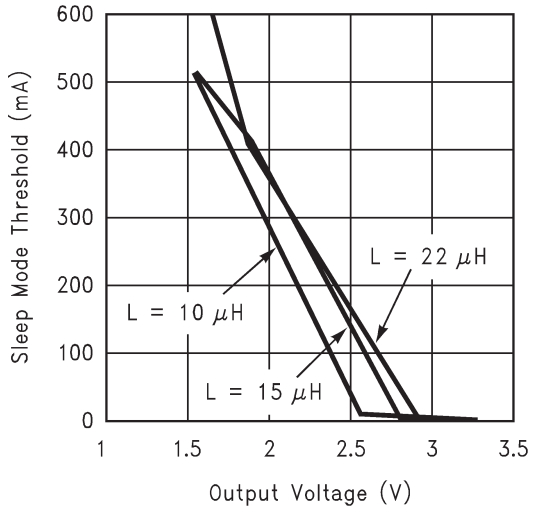


Figure 13. Sleep Mode Threshold vs Output Voltage For ADJ Version (V_{IN} = 5 V)

9 Power Supply Recommendations

The LM2651 is designed to operate from various DC power supplies. If so, VIN input should be protected from reversal voltage and voltage dump over 15 V. The impedance of the input supply rail should be low enough that the input current transient does not cause drop below VIN UVLO level. If the input supply is connected by using long wires, additional bulk capacitance may be required in addition to normal input capacitor.

10 Layout

10.1 Layout Guidelines

Layout is critical to reduce noises and ensure specified performance. The important guidelines are listed as follows:

1. Minimize the parasitic inductance in the loop of input capacitors and the internal MOSFETs by connecting the input capacitors to V_{IN} and PGND pins with short and wide traces. This is important because the rapidly switching current, together with wiring inductance can generate large voltage spikes that may result in noise problems.
2. Minimize the trace from the center of the output resistor divider to the FB pin and keep it away from noise sources to avoid noise pickup. For applications requiring tight regulation at the output, TI recommends a dedicated sense trace (separated from the power trace) to connect the top of the resistor divider to the output.
3. If the Schottky diode D_1 is used, minimize the traces connecting D_1 to SW and PGND pins.

10.2 Layout Example

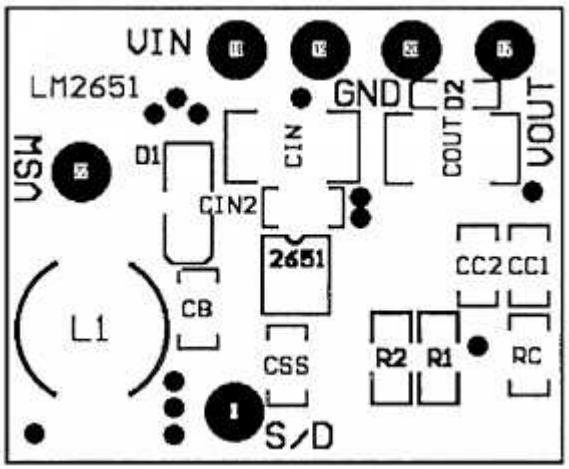


Figure 14. LM2651 Layout Recommendation

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11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2651MTC-3.3/NOPB	ACTIVE	TSSOP	PW	16	92	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2651MTC -3.3	Samples
LM2651MTC-ADJ	NRND	TSSOP	PW	16	92	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	2651MTC -ADJ	
LM2651MTC-ADJ/NOPB	ACTIVE	TSSOP	PW	16	92	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2651MTC -ADJ	Samples
LM2651MTCX-3.3/NOPB	ACTIVE	TSSOP	PW	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2651MTC -3.3	Samples
LM2651MTCX-ADJ/NOPB	ACTIVE	TSSOP	PW	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2651MTC -ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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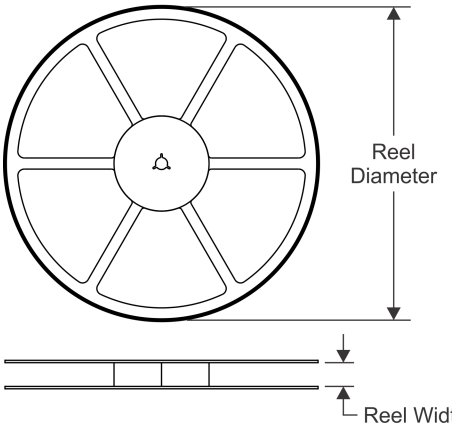
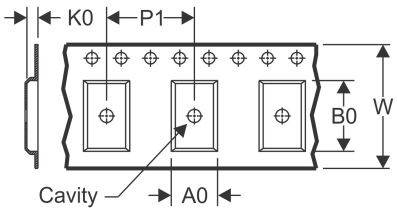
TAPE AND REEL INFORMATION

REEL DIMENSIONS

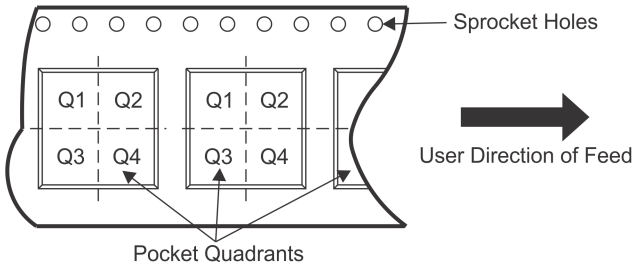


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

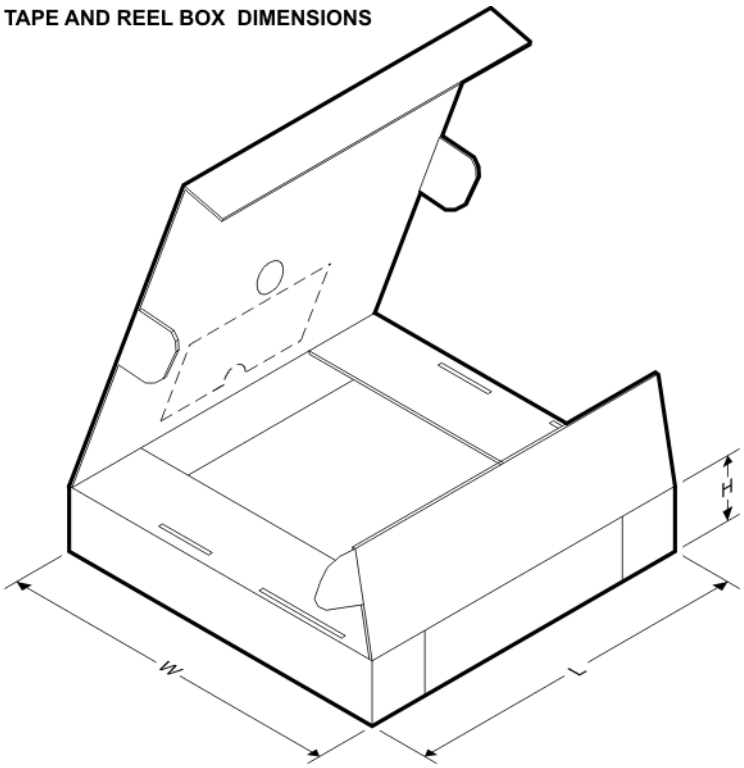
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2651MTCX-3.3/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM2651MTCX-ADJ/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

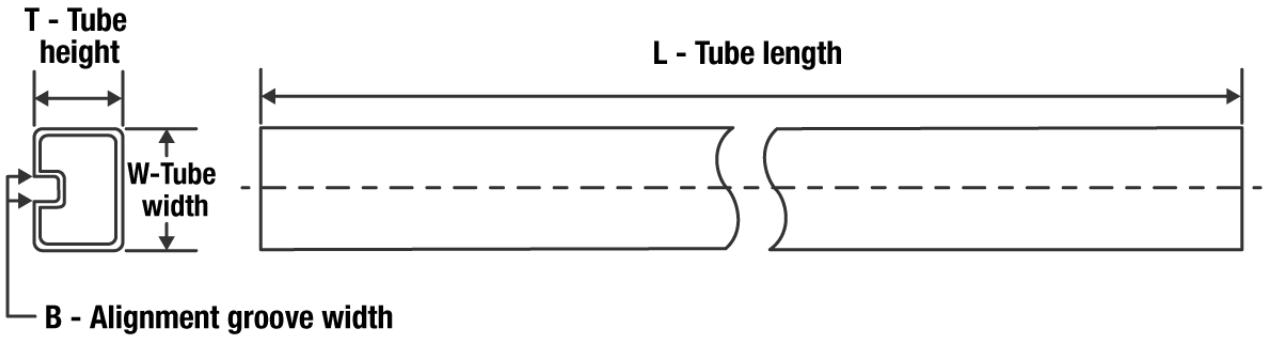
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2651MTCX-3.3/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
LM2651MTCX-ADJ/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

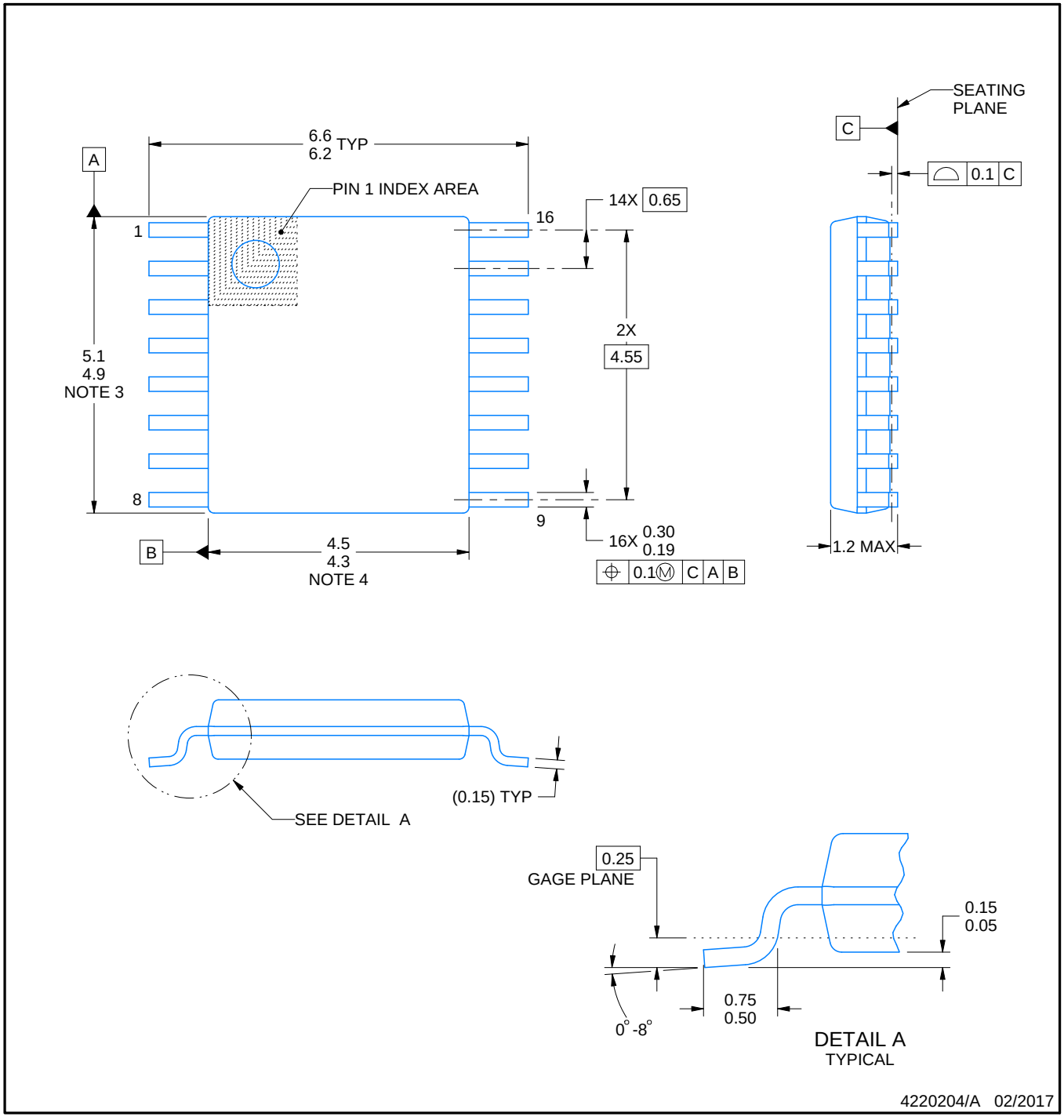
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM2651MTC-3.3/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06
LM2651MTC-ADJ	PW	TSSOP	16	92	495	8	2514.6	4.06
LM2651MTC-ADJ	PW	TSSOP	16	92	495	8	2514.6	4.06
LM2651MTC-ADJ/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06

PACKAGE OUTLINE

PW0016A

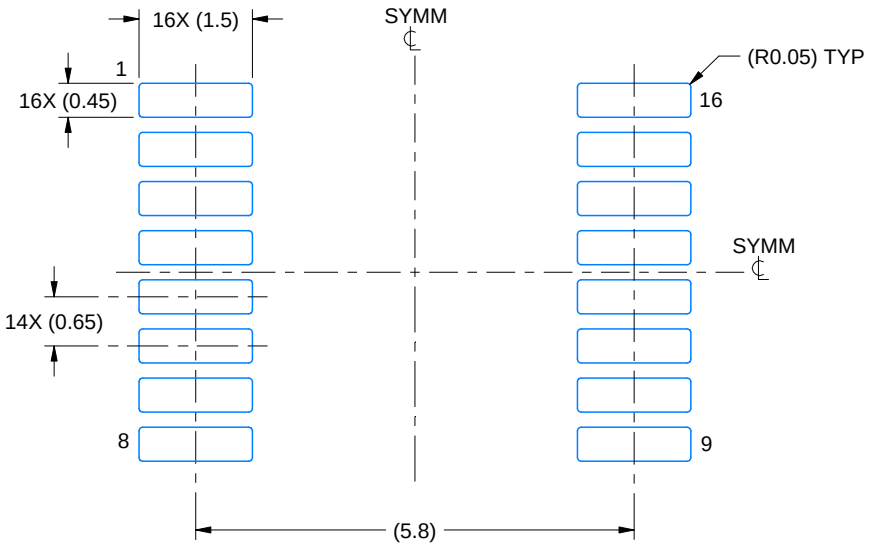
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

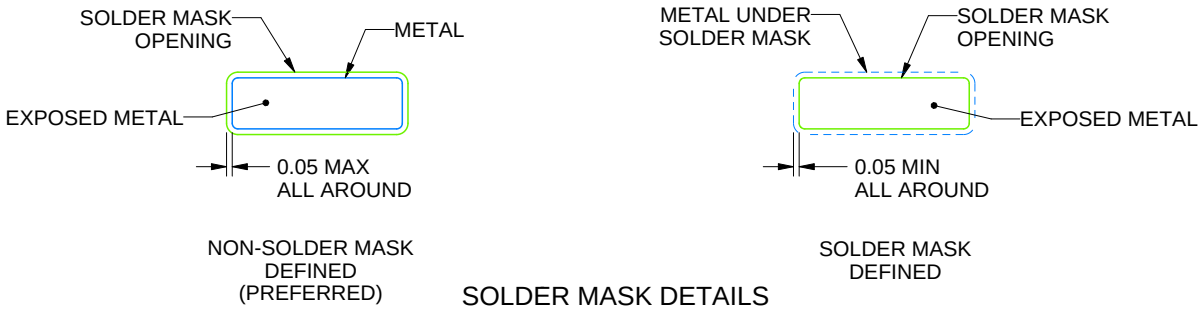


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

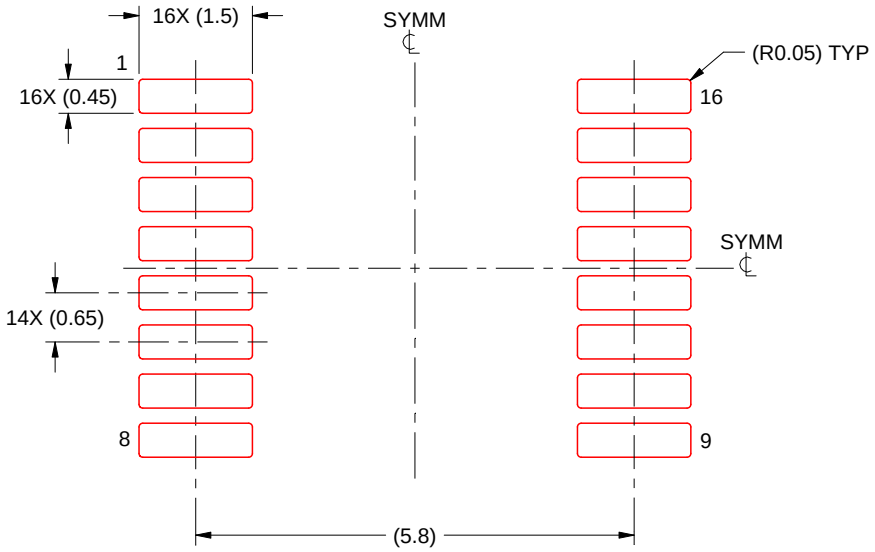


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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