TEXAS INSTRUMENTS
OPA2206
ZHCSLB2B – MARCH 2020 – REVISED AUGUST 2021

OPA2206 具有输入过压保护功能的 2μV、0.04μV/°C 低功耗精密运算放大器

1 特性

- 集成了高达 ±40V（超过电源电压范围）的输入过压保护
- e-trim™ 运算放大器性能
  - 低失调电压：50μV（最大值）
  - 低失调电压漂移：±0.5μV/°C（最大值）
- 超 β 输入
  - 输入偏置电流：0.5nA（最大值）
  - 输入电流噪声：110fA/√Hz
- 低噪声
  - 0.1Hz 至 10Hz：0.2μV_{PP}
  - 电压噪声：8nV/√Hz
- A_{OL}、CMRR 和 PSRR：> 124dB（全温度范围）
- 增益带宽积：3.6MHz
- 低静态电流：240μA（最大值）
- 压摆率：4V/μs
- 过载功率限制器
- 轨到轨输出
- 输入已滤除 EMI 和 RFI
- 宽电源电压：4.5V 至 36V
- 温度范围：–40°C 至 +125°C

2 应用

- 模拟输入模块
- 混合模块（AI、AO、DI、DO）
- 实验室和现场仪表
- 源测量单元 (SMU)
- 数字万用表 (DMM)
- 火车控制和管理
- 串式逆变器
- 数据采集 (DAQ)

3 说明

OPA2206 是业界通用 OPAx277 系列的新一代版本，额外具有输入过压保护特性。该器件是一款具有超 β 输入的精密双极 e-trim™ 运算放大器。该器件使用 TI 的专有微调技术来实现 ±8μV（典型值）的输入失调电压和 ±0.08μV/°C（典型值）的输入失调电压漂移。当输入信号超出电源电压范围时，将会激活输入过压保护，并提供 40V 保护（超过任一电源电压范围）。借助此特性，无需再使用外部繁琐电路即可防止放大器损坏。

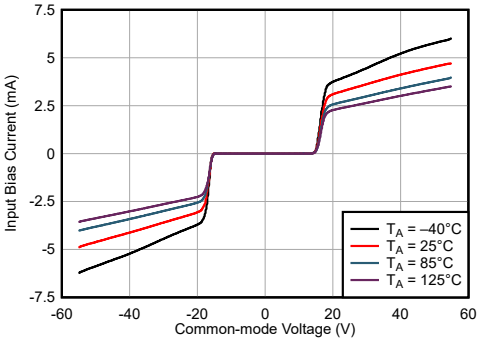
OPA2206 采用双极工艺设计，可针对仅 220μA（典型值）的电流提供 3.6MHz 的速度功率比。该器件还可在 1kHz 下实现仅 8nV/√Hz 的低电压噪声密度。得益于超 β 输入，OPA2206 具有 100pA（典型值）的超低输入偏置电流和 110fA/√Hz 的电流噪声密度。

OPA2206 的高性能使该器件成为了高精度和低功耗系统的理想选择，例如可编程逻辑控制器中的高密度模拟输入模块、现场和便携式仪表系统以及源测量单元。OPA2205 是一款使用相同运算放大器内核、无输入保护、具有低宽带噪声 (7.2nV/√Hz) 的相关产品。

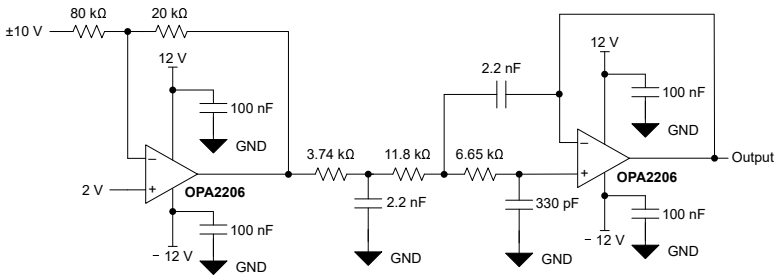
器件信息

器件型号	封装(1)	封装尺寸（标称值）
OPA2206	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



OPA2206 输入过压保护



OPA2206 典型应用

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4 Revision History

Changes from Revision A (March 2021) to Revision B (August 2021) **Page**

- 删除了 OPA2206 高级版本和相关内容 1
- 将静态电流特性要点从 220μA 更改为 240μA 1
- Changed Figure 6-27, *Current Noise vs Frequency*, to more accurately show the device performance 9

Changes from Revision * (April 2020) to Revision A (March 2021) **Page**

- 将 OPA2206 从“预告信息（预发布）”更改为“量产数据（正在供货）” 1
- Changed both *Electrical Characteristics* tables to show differentiated performance between OPA2206 (high grade) and OPA2206A (standard grade) 5

5 Pin Configuration and Functions

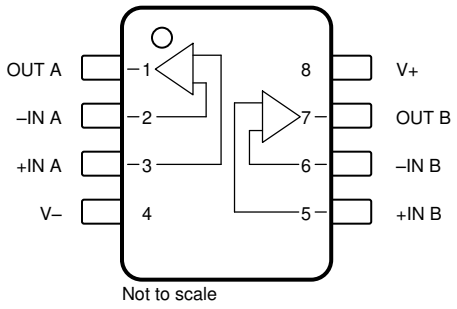

图 5-1. DGK (8-Pin VSSOP) Package, Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
–IN A	2	I	Inverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, Vs = (V+) – (V–)	Single supply		40	V
		Dual supply		±20	
	Signal input pin voltage		(V–) – 40	(V+) + 40	V
	Output short-circuit(2)		Continuous		
T_A	Operating temperature		–40	150	°C
T_J	Junction temperature			150	°C
T_{STG}	Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply	4.5		36	V
		Dual supply	±2.25		±18	
T_A	Operating temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA2206 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175.6	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.1	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	97.2	℃/W
ψ_{JT}	Junction-to-top characterization parameter	7.8	℃/W
ψ_{JB}	Junction-to-board characterization parameter	95.5	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	℃/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics: V_S = ±5 V

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±8	±50	µV
		T_A = –40°C to +125°C				±80	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.08	±0.5	µV/°C
PSRR	Power supply rejection ratio	V_S = ±2.25 V to ±18 V			±0.05	±0.5	µV/V
			T_A = –40°C to +125°C			±1	
	Channel separation	f = DC			130		dB
		f = 100 kHz			110		
INPUT BIAS CURRENT							
I_B	Input bias current				±0.1	±0.5	nA
		T_A = 0°C to 85°C				±0.75	
		T_A = –40°C to +125°C				±1	
I_{OS}	Input offset current				±0.1	±0.4	nA
		T_A = 0°C to 85°C				±0.5	
		T_A = –40°C to +125°C				±0.6	
NOISE							
$e_{n\ p\text{-}p}$	Input voltage noise	f = 0.1 Hz to 10 Hz			0.2		μV_{PP}
e_n	Input voltage noise density	f = 10 Hz			8.4		nV/√Hz
		f = 100 Hz			8.1		
		f = 1 kHz			8		
i_n	Input current noise	f = 1 kHz			110		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 1		(V+) – 1.4	V
CMRR	Common-mode rejection ratio	(V–) + 1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to +125°C		124	140		dB
INPUT OVERVOLTAGE							
	Input overvoltage protection	T_A = –40℃ to +125℃		(V–) – 40		(V+) + 40	V
	Input current in overvoltage protected mode	V_S = 0 V, (V–) – 40 V < V_{CM} < (V+) + 40 V			4.8	10	mA
			T_A = –40℃ to +125℃	See typical curves			
INPUT IMPEDANCE							
Z_{ID}	Differential				9 || 4.4		MΩ || pF
Z_{ICM}	Common-mode				300 || 4.4		GΩ || pF

6.5 Electrical Characteristics: V_S = ±5 V (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	OPA2206A, T_A = –40°C to +125°C, (V–) + 200 mV < V_O < (V+) – 200 mV	R_L = 10 kΩ	126	132		dB
			R_L = 2 kΩ	126	130		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				3.6		MHz
SR	Slew rate	4-V step, G = –1			3.2		V/μs
	Phase margin	R_L = 10 kΩ, C_L = 25 pF			67		degrees
t_S	Settling time	To 0.024% (12-bit), 4-V step, G = 1, C_L = 30 pF	Falling		2.2		μs
			Rising		2.8		
	Overload recovery time	G = –10			0.3		μs
THD+N	Total harmonic distortion + noise	V_O = 5 V_{PP}, G = +1, f = 1 kHz, R_L = 2 kΩ			0.0004		%
OUTPUT							
	Voltage output swing from rail	A_{OL} > 126 dB	R_L = 10 kΩ	(V–) + 0.2		(V+) – 0.2	V
			R_L = 2 kΩ	(V–) + 0.2		(V+) – 0.2	
		T_A = –40°C to +125°C, R_L = 10 kΩ		(V–) + 0.2		(V+) – 0.2	
I_{SC}	Short-circuit current				±25		mA
C_{LOAD}	Capacitive load drive			See Typical Characteristics			
R_O	Open-loop output impedance			See Typical Characteristics			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			220	240	μA
			T_A = –40°C to +125°C			310	

6.6 Electrical Characteristics: V_S = ±15 V

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±8	±50	µV
		T_A = –40°C to +125°C				±80	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.08	±0.5	µV/°C
PSRR	Power supply rejection ratio	V_S = ±2.25 V to ±18 V			±0.05	±0.5	µV/V
			T_A = –40°C to +125°C			±1	
	Channel separation	f = DC			130		dB
		f = 100 kHz			110		
INPUT BIAS CURRENT							
I_B	Input bias current				±0.1	±0.5	nA
		T_A = 0°C to 85°C				±1	
		T_A = –40°C to +125°C				±1.2	
I_{OS}	Input offset current				±0.1	±0.4	nA
		T_A = 0°C to 85°C				±0.8	
		T_A = –40°C to +125°C				±0.9	
NOISE							
$e_{n\ p\text{-}p}$	Input voltage noise	f = 0.1 Hz to 10 Hz			0.2		$µV_{PP}$
e_n	Input voltage noise density	f = 10 Hz			8.4		nV/√Hz
		f = 100 Hz			8.1		
		f = 1 kHz			8		
i_n	Input current noise	f = 1 kHz			110		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 1		(V+) – 1.4	V
CMRR	Common-mode rejection ratio	(V–) + 1 V < V_{CM} < (V+) – 1.4 V		126	140		dB
			T_A = –40°C to +125°C	124	140		
INPUT OVERVOLTAGE							
	Input overvoltage protection	T_A = –40℃ to +125℃		(V–) – 40		(V+) + 40	V
	Input current in overvoltage protected mode	V_S = 0 V, (V–) – 40 V < V_{CM} < (V+) + 40 V			4.8	10	mA
			T_A = –40°C to +125°C	See typical curves			
INPUT IMPEDANCE							
Z_{ID}	Differential				9 || 4.4		MΩ || pF
Z_{ICM}	Common-mode				300 || 4.3		GΩ || pF

6.6 Electrical Characteristics: V_S = ±15 V (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	R_L = 10 kΩ, (V –) + 200 mV < V_O < (V+) – 200 mV, T_A = –40°C to +125°C		126	132		dB
		R_L = 2 kΩ, (V –) + 350 mV < V_O < (V+) – 350 mV, T_A = –40°C to +125°C		126	130		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 30 pF			3.6		MHz
SR	Slew rate	10-V step, G = –1			4		V/µs
	Phase margin	R_L = 10 kΩ, C_L = 25 pF			67		degrees
t_S	Settling time	To 0.024% (12-bit), 10-V step, G = 1, C_L = 30 pF	Falling		2.8		µs
			Rising		4.5		
	Overload recovery time	G = –10			0.2		µs
THD+N	Total harmonic distortion + noise	V_O = 5 V_{PP}, G = +1, f = 1 kHz, R_L = 2 kΩ			0.0004		%
OUTPUT							
	Voltage output swing from rail	A_{OL} > 126 dB	R_L = 10 kΩ	(V –) + 0.2		(V+) + 0.2	V
			R_L = 2 kΩ	(V –) + 0.35		(V+) + 0.35	
		T_A = –40°C to +125°C, R_L = 10 kΩ		(V –) + 0.2		(V+) + 0.2	
I_{SC}	Short-circuit current				±25		mA
C_{LOAD}	Capacitive load drive			See Typical Characteristics			
R_O	Open-loop output impedance			See Typical Characteristics			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			220	240	µA
			T_A = –40°C to +125°C			310	

6.7 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

表 6-1. Table of Graphs

DESCRIPTION	FIGURE
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6.7 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

表 6-1. Table of Graphs (continued)

DESCRIPTION	FIGURE
Quiescent Current vs Supply Voltage	图 6-45
Quiescent Current vs Temperature	图 6-46

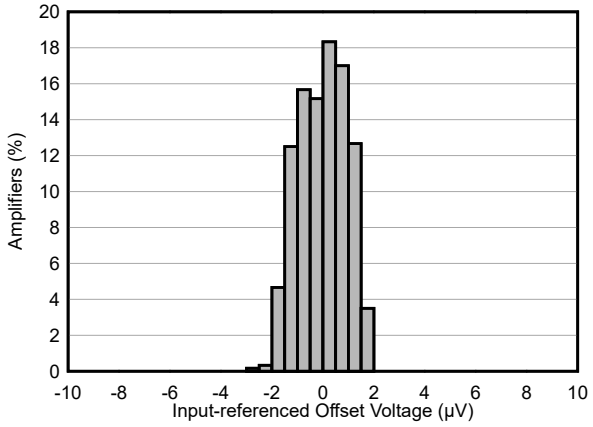


图 6-1. Offset Voltage Production Distribution at 25°C

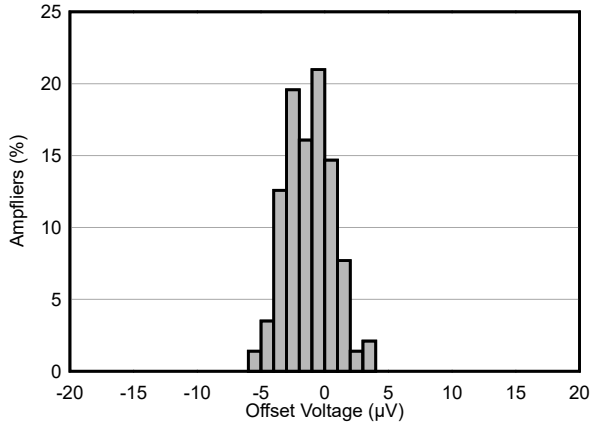


图 6-2. Offset Voltage Distribution at 125°C

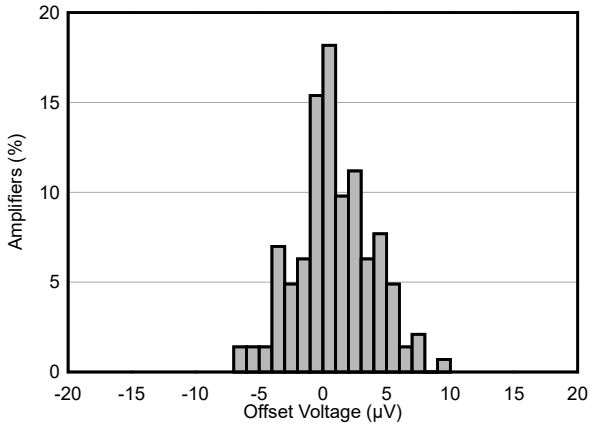


图 6-3. Offset Voltage Distribution at -40°C

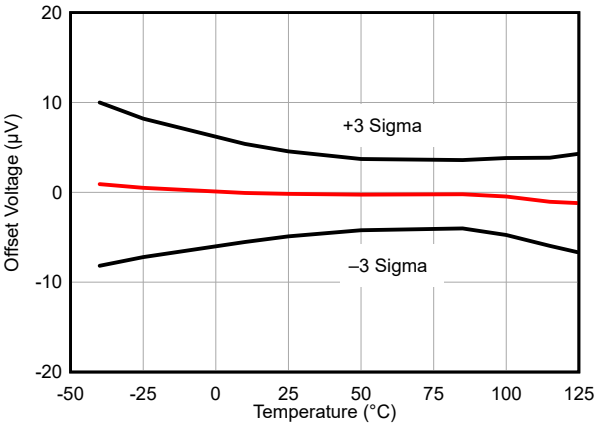


图 6-4. Offset Voltage vs Temperature

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

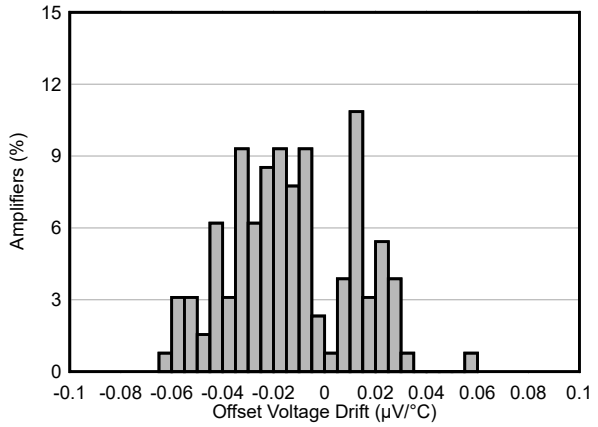


图 6-5. Offset Voltage Drift Production Distribution

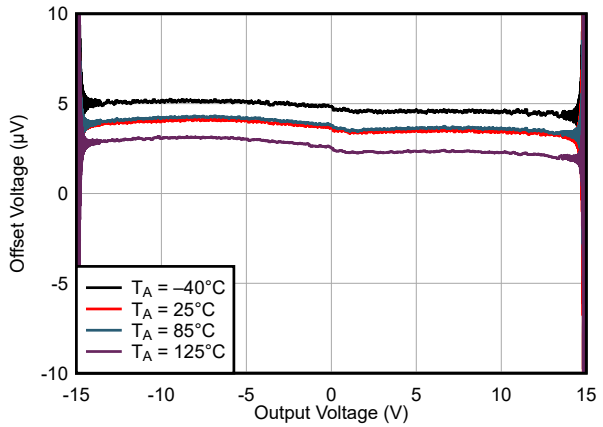


图 6-6. Offset Voltage vs Output Voltage

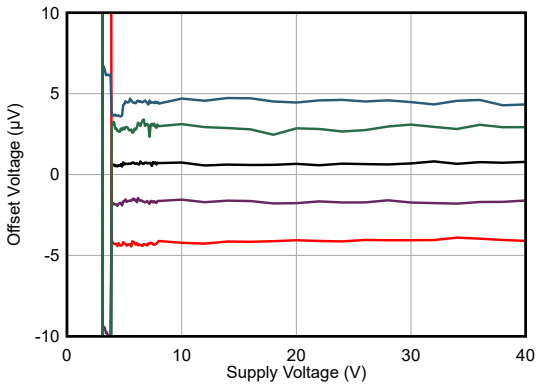


图 6-7. Offset Voltage vs Power Supply Voltage

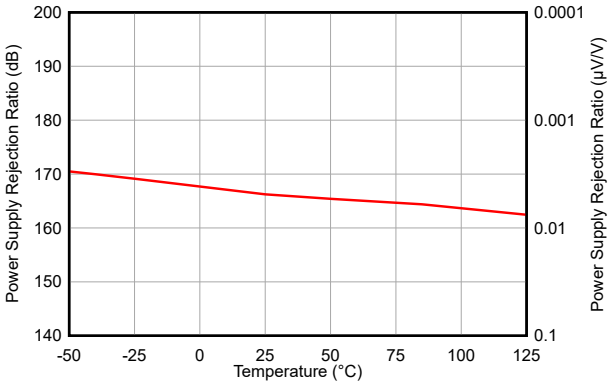


图 6-8. Power-Supply Rejection Ratio vs Temperature

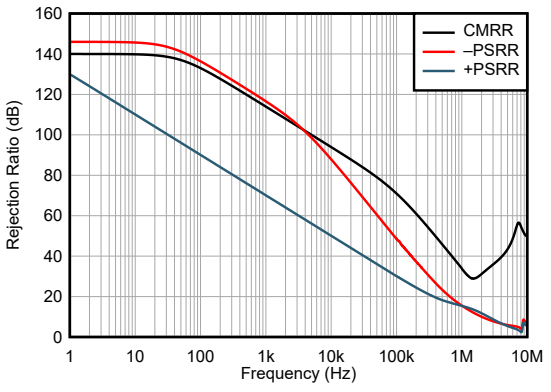


图 6-9. Power-Supply and Common-Mode Rejection Ratio vs Frequency

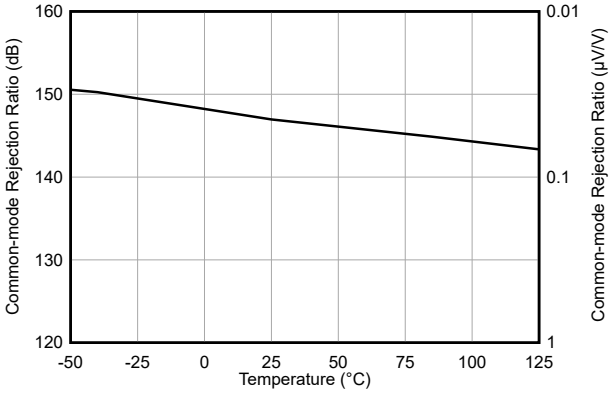


图 6-10. Common-Mode Rejection Ratio vs Temperature

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

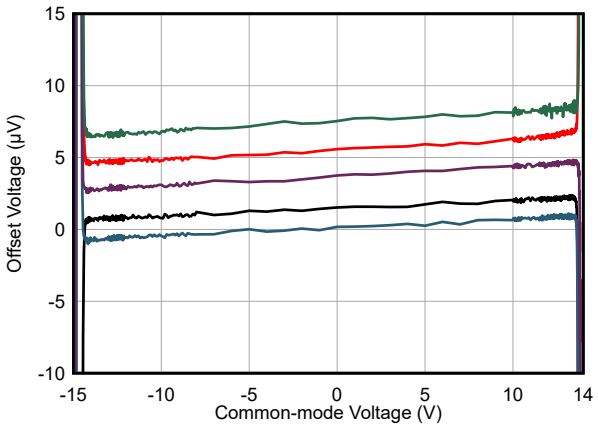


图 6-11. Offset Voltage vs Common-Mode Voltage

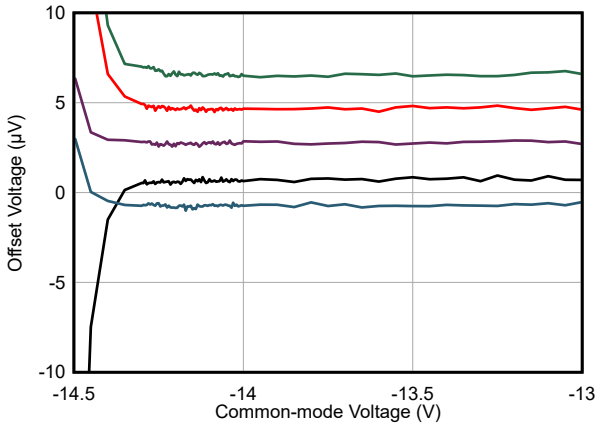


图 6-12. Offset Voltage vs Vcm at Low Supply

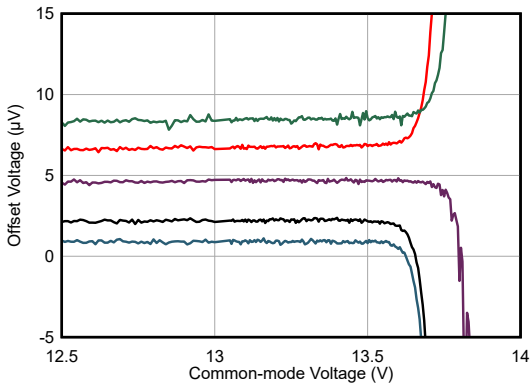


图 6-13. Offset Voltage vs Vcm at High Supply

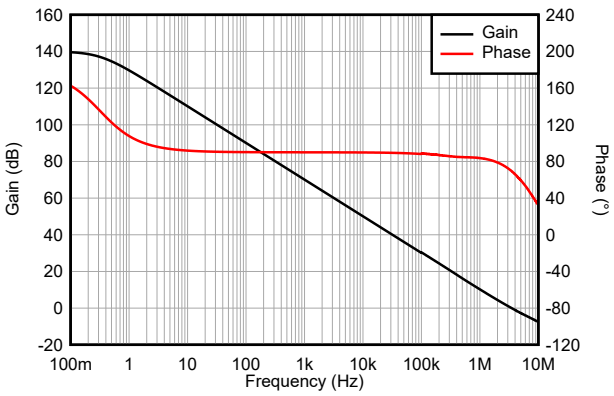


图 6-14. Open-Loop Gain and Phase vs Frequency

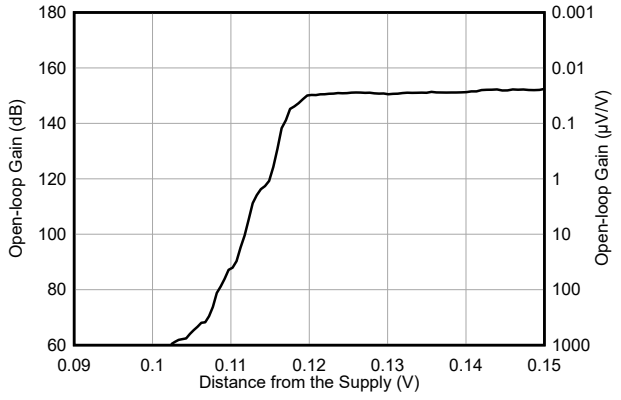


图 6-15. Open-Loop Gain vs Distance from Supply

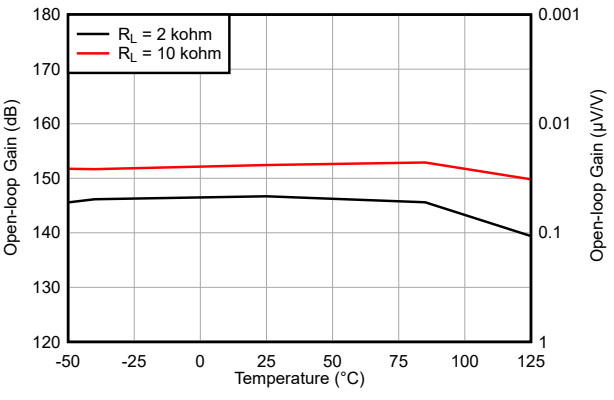


图 6-16. Open-Loop Gain vs Temperature

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

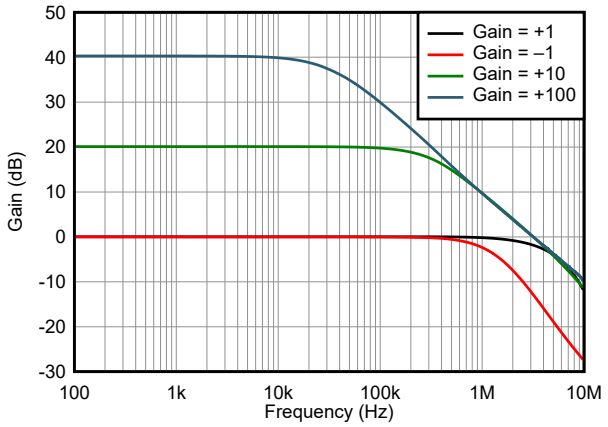


图 6-17. Closed-Loop Gain vs Frequency

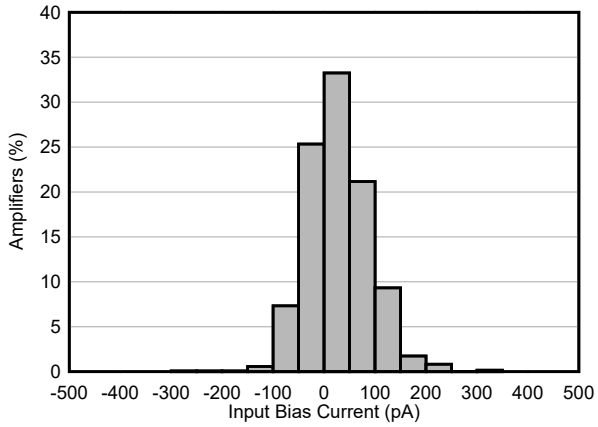


图 6-18. Input Bias Production Distribution

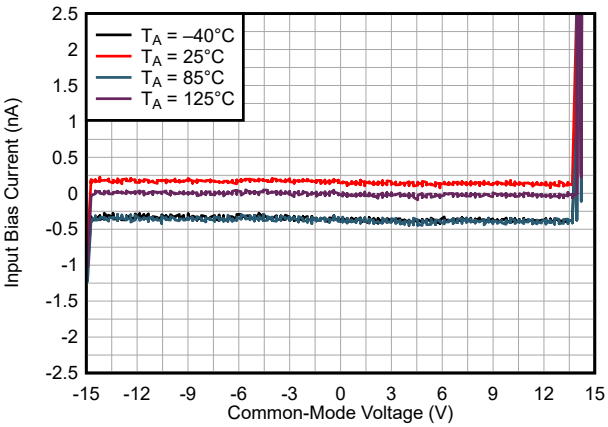


图 6-19. Input Bias vs Common-Mode Voltage

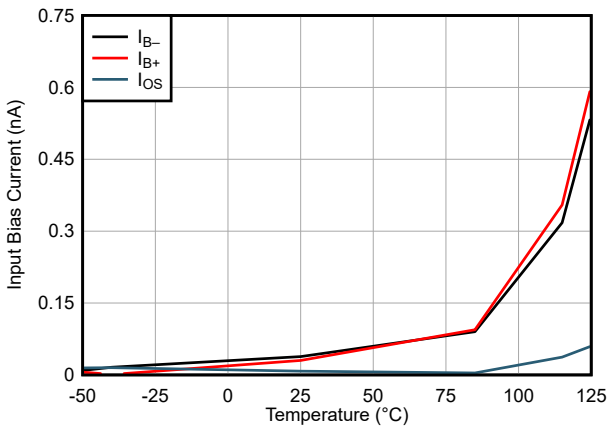


图 6-20. Input Bias and Input Offset Current vs Temperature

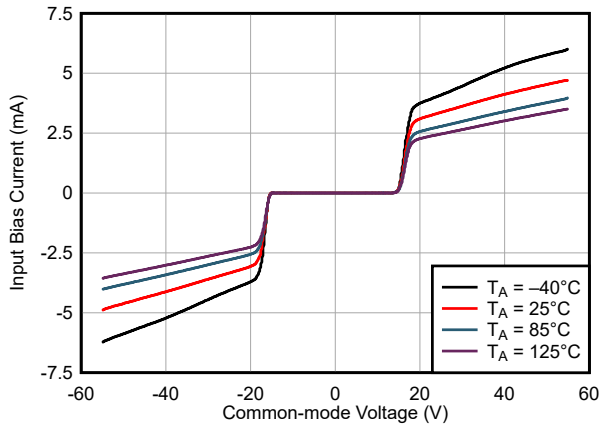


图 6-21. Input Bias vs Overvoltage Protected Common Mode Range

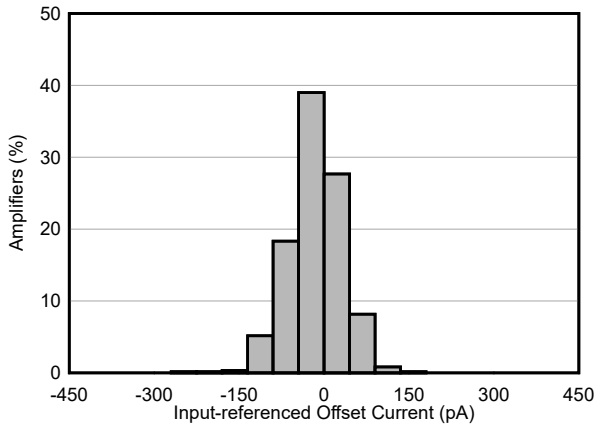


图 6-22. Input Offset Current Production Distribution

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

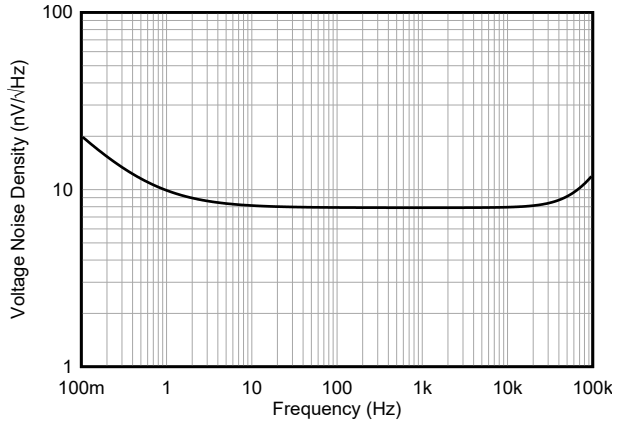


图 6-23. Voltage Noise Density vs Frequency

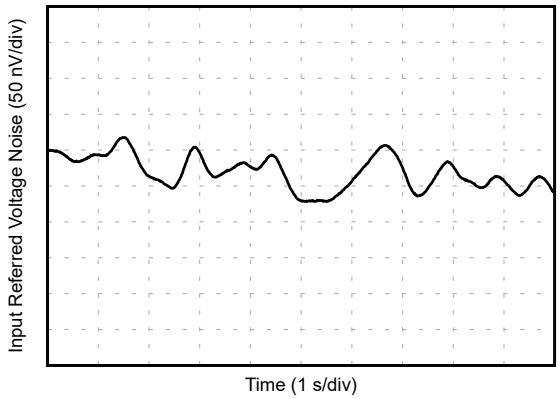


图 6-24. 0.1-Hz To 10-Hz Noise

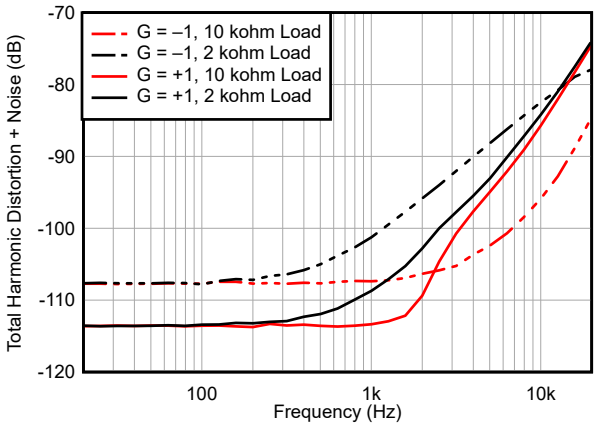


图 6-25. Total Harmonic Distortion + Noise Ratio vs Frequency

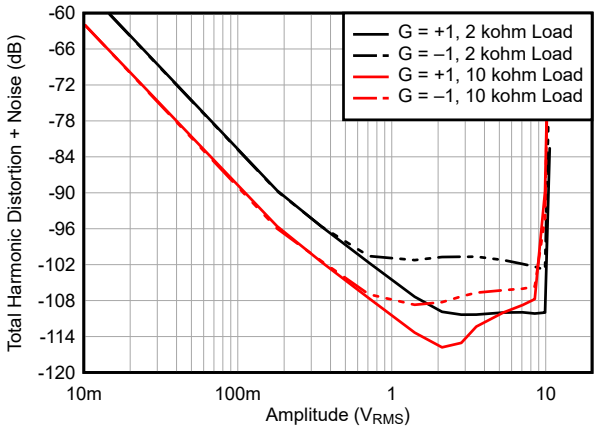


图 6-26. Total Harmonic Distortion + Noise Ratio vs Output Amplitude

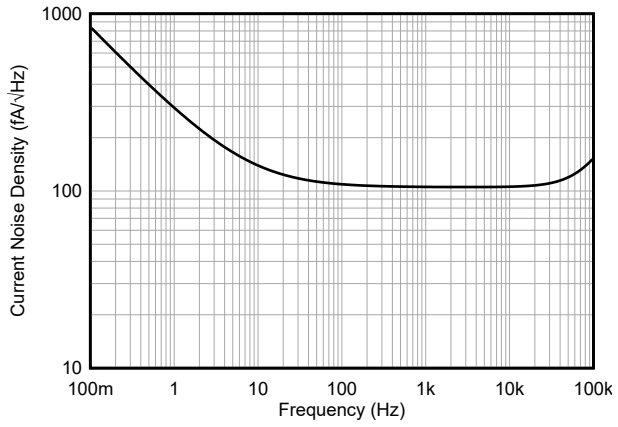


图 6-27. Current Noise vs Frequency

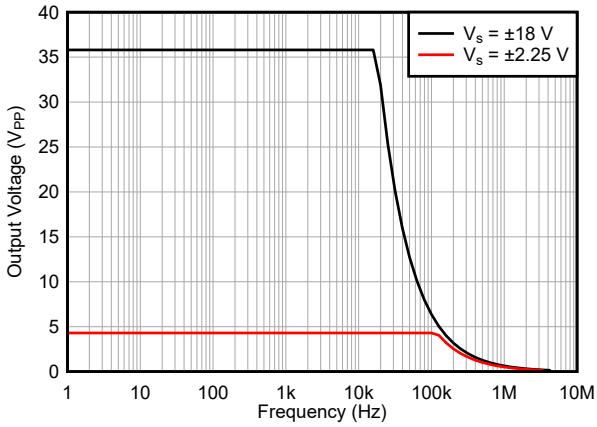


图 6-28. Maximum Output Voltage vs Frequency

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

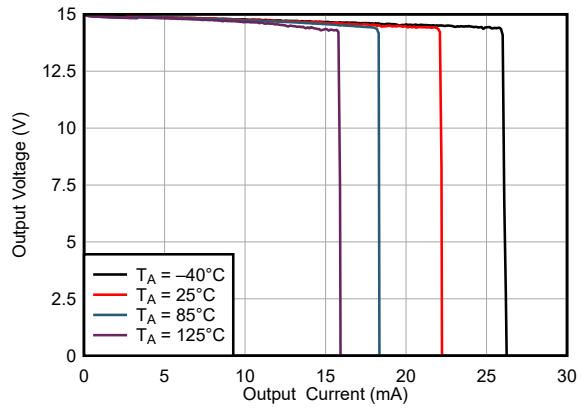


图 6-29. Output Voltage Swing vs Output Sourcing Current

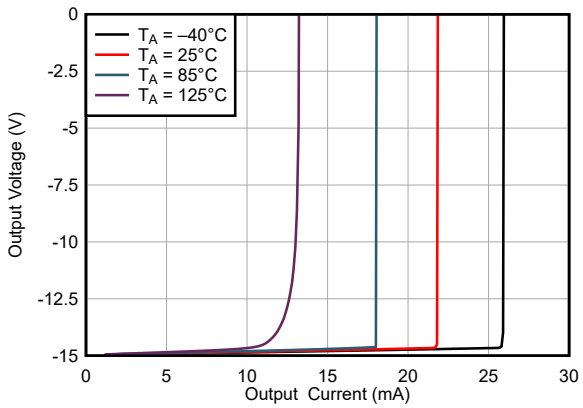


图 6-30. Output Voltage Swing vs Output Sinking Current

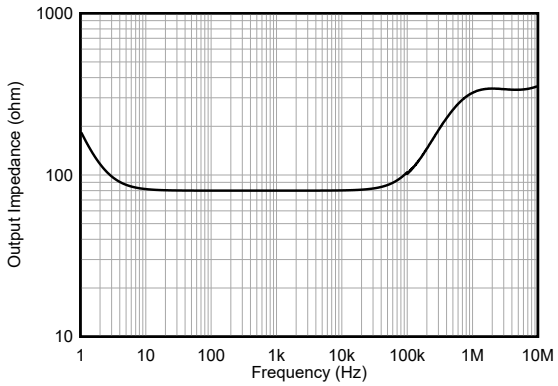


图 6-31. Open-Loop Output Impedance vs Frequency

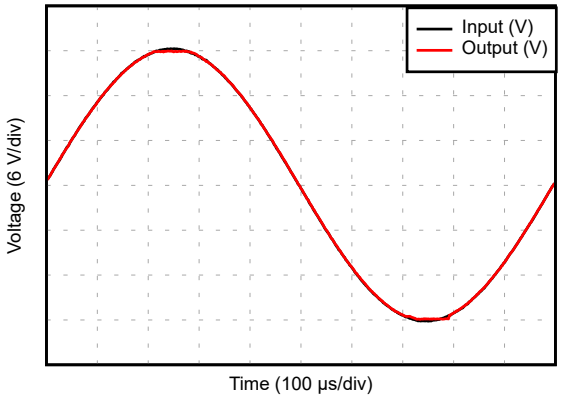


图 6-32. No Phase Reversal

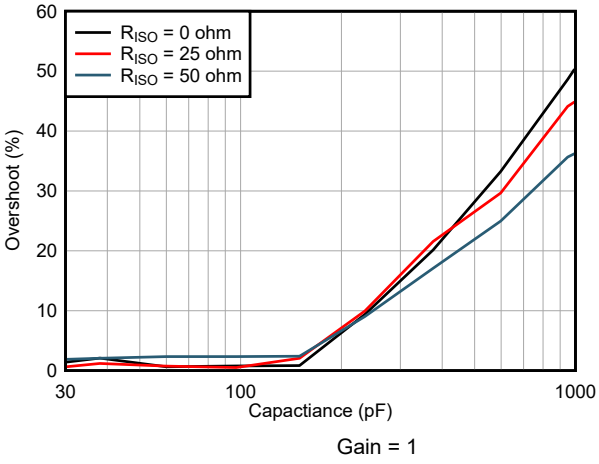


图 6-33. Small-Signal Overshoot vs Capacitive Load

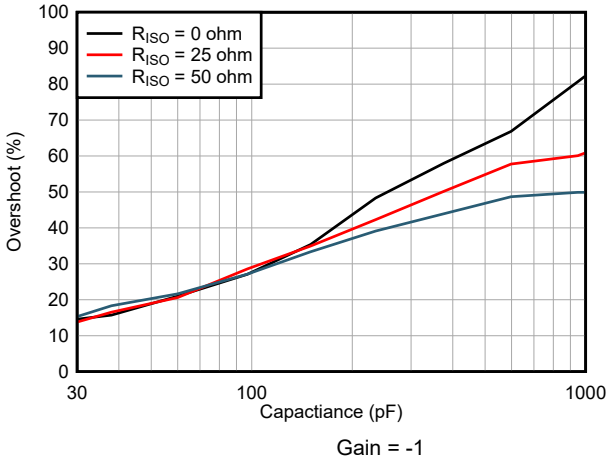


图 6-34. Small-Signal Overshoot vs Capacitive Load

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

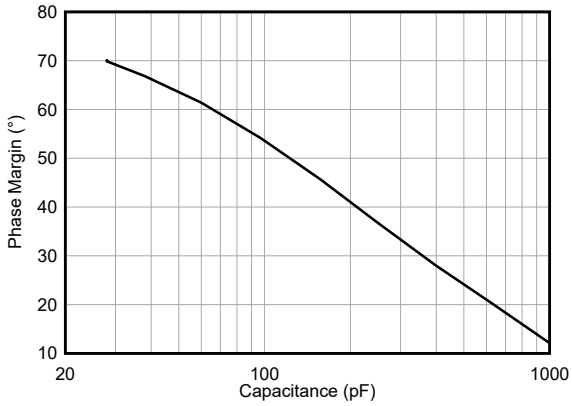


图 6-35. Phase Margin vs Capacitive Load

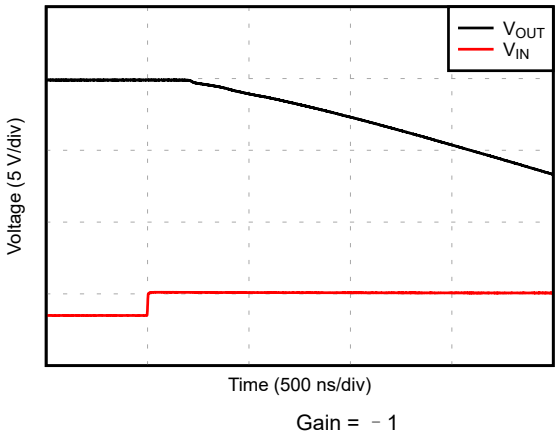


图 6-36. Positive Overload Recovery

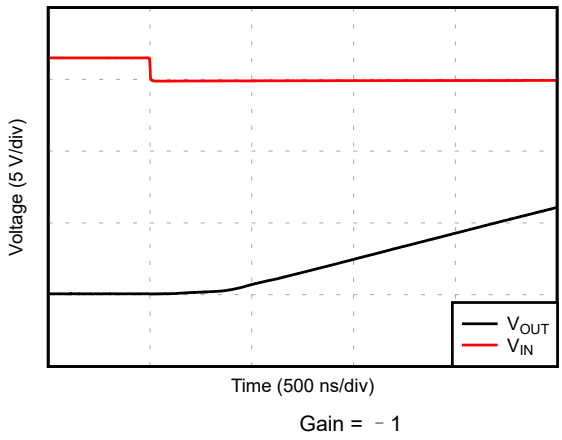


图 6-37. Negative Overload Recovery

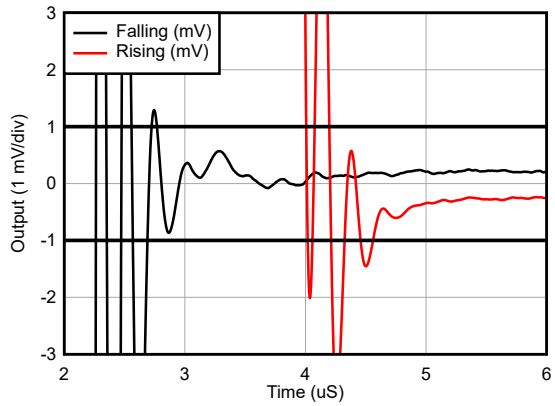


图 6-38. Settling Time

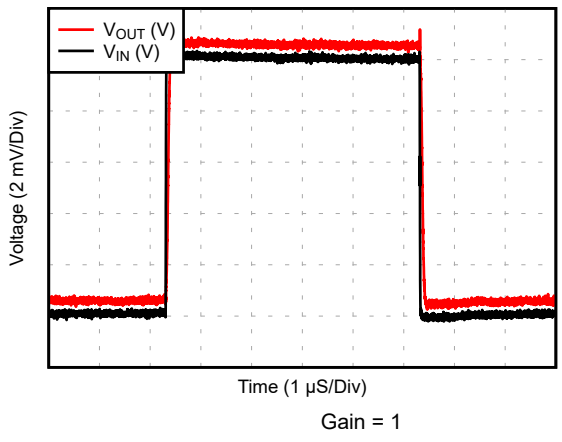


图 6-39. Small-Signal Step Response

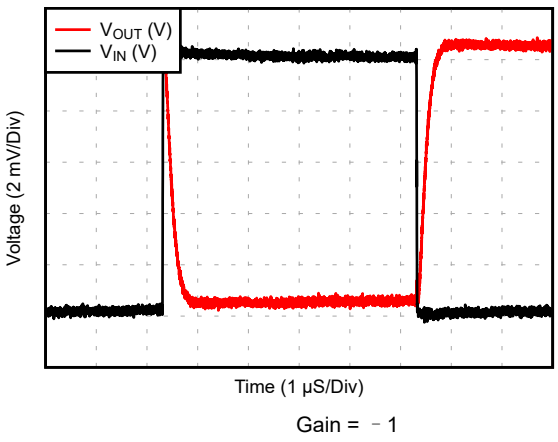


图 6-40. Small-Signal Step Response

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

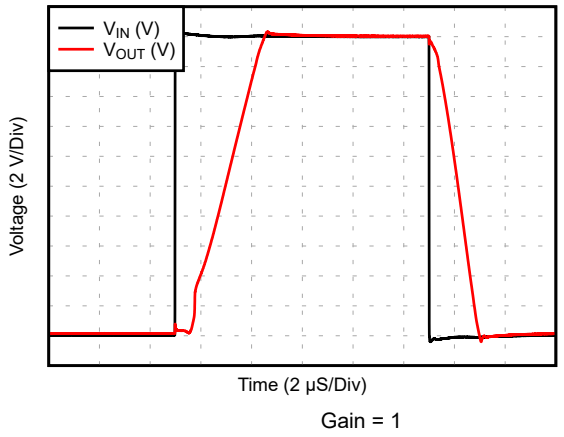


图 6-41. Large-Signal Step Response

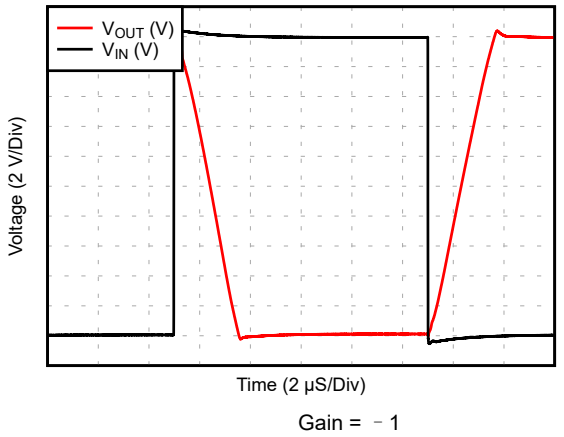


图 6-42. Large-Signal Step Response

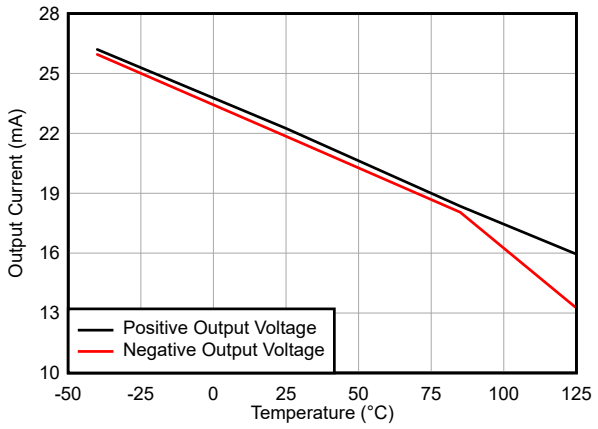


图 6-43. Short-Circuit Current vs Temperature

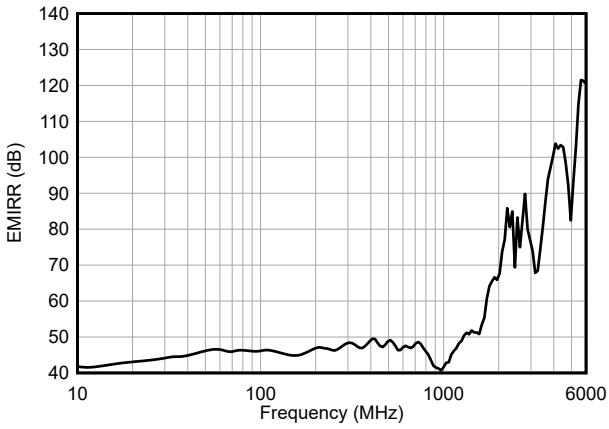


图 6-44. Electromagnetic Interference Rejection (EMIRR)

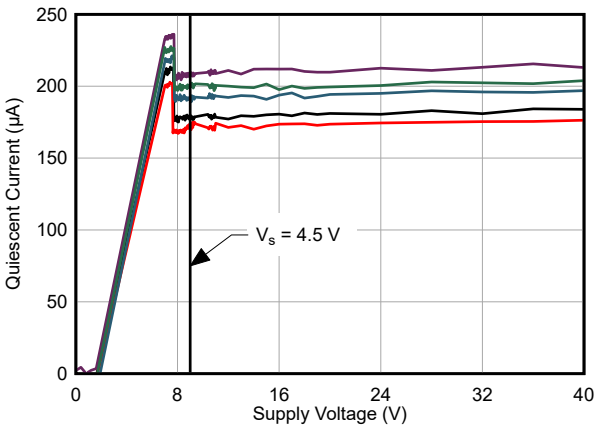


图 6-45. Quiescent Current vs Supply Voltage

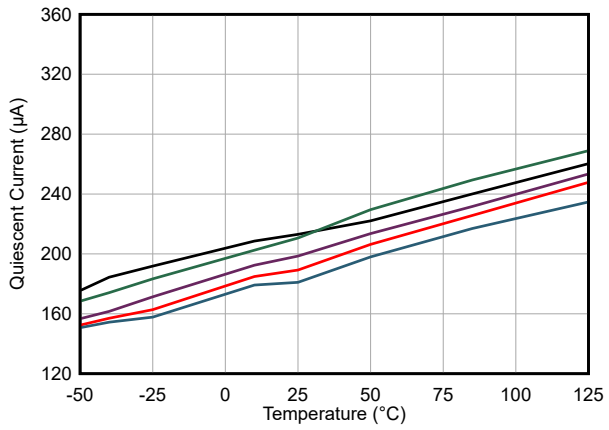


图 6-46. Quiescent Current vs Temperature

7 Parameter Measurement Information

7.1 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. As a result of natural variations in process technology and manufacturing procedures, every specification of an amplifier exhibits some amount of deviation from the ideal value, such as the input bias current of an amplifier. These deviations often follow *Gaussian* (bell curve), or *normal* distributions. Circuit designers can leverage this information to guardband their system, even when there is no minimum or maximum specification in the *Electrical Characteristics*.

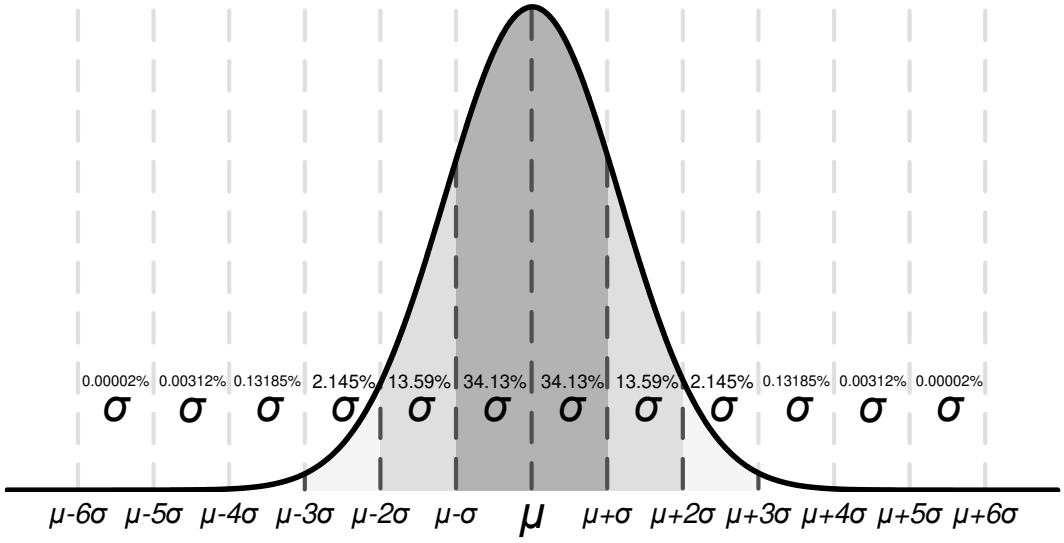


图 7-1. Ideal Gaussian Distribution

图 7-1 shows an example distribution, where *μ*, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from *μ* – σ to *μ*+ σ).

Depending on the specification, values listed in the *typical* column of *Electrical Characteristics* are represented in different ways. As a general guideline, if a specification naturally has a nonzero mean (for example, gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (for example, input bias current), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

Use this chart to calculate the approximate probability of a specification in a unit. For example, the OPA2206 typical input bias current is ±0.1 nA; therefore, 68.2% of all devices are expected to have an input bias from ±0.1 nA. At 4 σ, 99.9937% of the distribution has an input bias less than ±0.28 nA, which means that 0.0063% of the population is outside of these limits, and corresponds to approximately 1 in 15,873 units.

Units that are found to exceed any tested minimum or maximum specifications are removed from production material. For example, the OPA2206 has a maximum input bias of ±0.4 nA at 25°C, and although this value corresponds to approximately 6 σ (~1 in 500 million units), TI removes any unit with a larger input bias from production material.

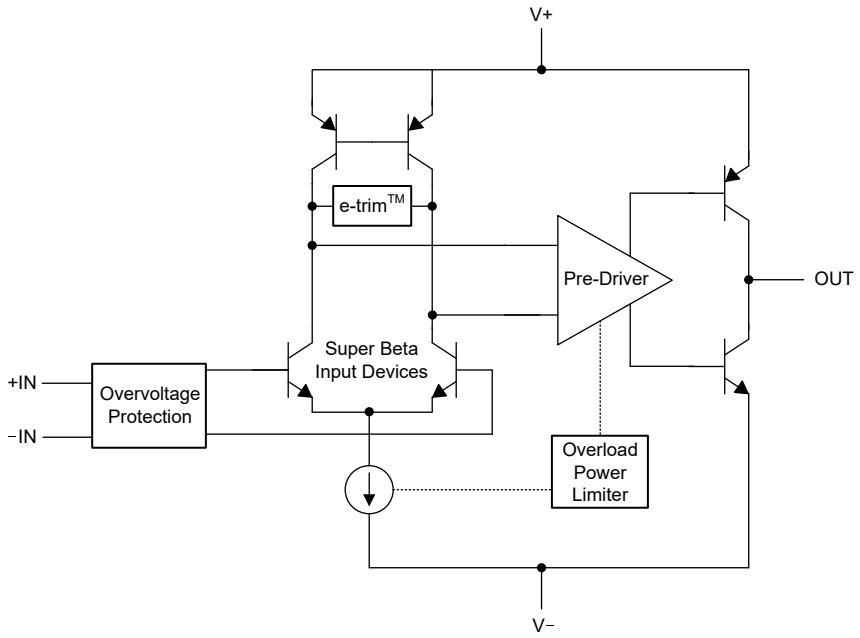
For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. This information should only be used to estimate the performance of a device.

8 Detailed Description

8.1 Overview

The OPA2206 is the first 36-V, bipolar, e-trim operational amplifier. This device uses a package-level offset trim to minimize the offset voltage and offset voltage drift introduced during the manufacturing process. This trim is performed after the device is assembled to remove any offset errors introduced throughout the manufacturing process, and trim communication is disabled afterward. The device features super beta inputs that decrease the input bias current and input current noise. The device also features input overvoltage protection that protects the device for input voltages up to ±40 V beyond either supply rail.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Overvoltage Protection

The inputs of the OPA2206 are individually protected for voltages up to ±40 V beyond either supply. For example, a common-mode voltage anywhere between –55 V and +55 V does not cause damage when powered from ±15-V supplies. Internal circuitry on each input provides low series impedance under normal signal conditions thus maintaining high performance under normal operating conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 4.8 mA.

During an input overvoltage condition, current flows through the input protection diodes into the power supplies, as shown in 图 8-1. If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2) must be placed on the power supplies to provide a current pathway to ground. During an overvoltage condition, the input bias current of the inputs increase as shown in 图 8-2.

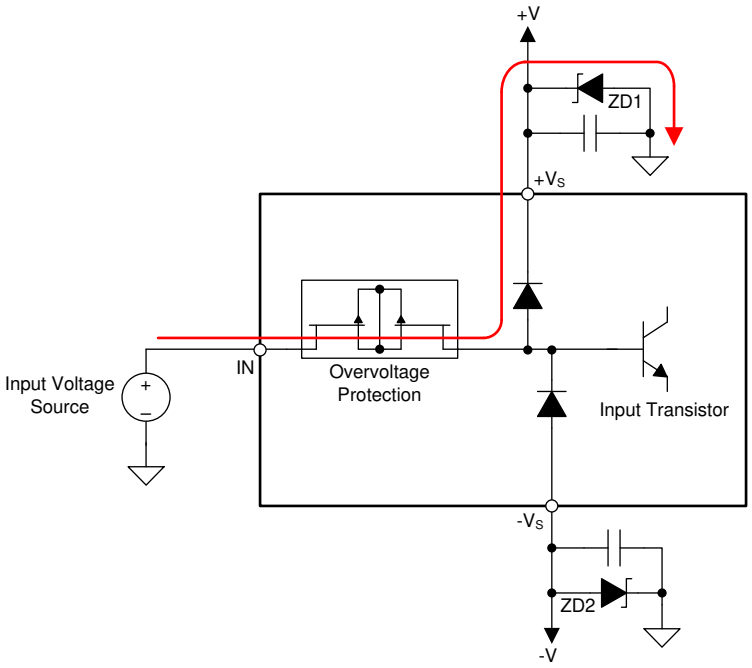


图 8-1. OPA2206 Input Overvoltage Current Path

图 8-2 shows the input current for input voltages from –55 V to +55 V when the OPA2206 is powered by ±15-V supplies.

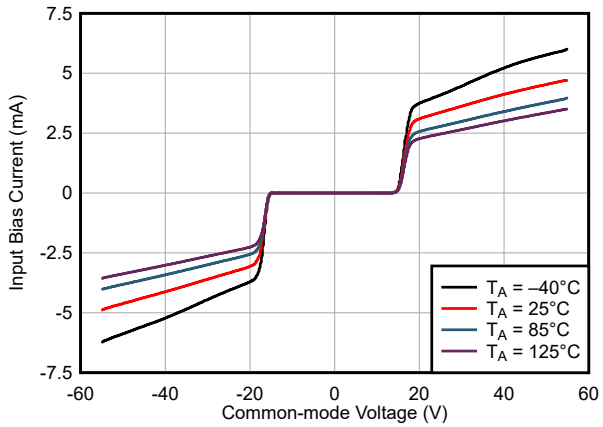


图 8-2. OPA2206 Input Current vs Input Voltage (V_S = ±15 V)

8.3.2 Input Offset Trimming

The OPA2206 is the industry's first e-trim operational amplifier built on a bipolar process. The input offset voltage of an amplifier is determined by the inherent mismatch between the input transistors. The offset can be minimized using laser-trimming performed during the manufacturing process while the device is still in the bare silicon form. However, when the silicon is packaged, the packaging process introduces additional offset due to mechanic stresses. TI's new trimming processes are used to trim the offset after the packaging process is complete to minimize both inherent and package-induced offsets. After trimming, communication is disabled to make sure the amplifier operates properly in the final system.

A comparison between production offset values for a the industry popular, laser-trimmed OPA2277 amplifier and the OPA2206 proprietary trim can be seen in 图 8-3 and 图 8-4.

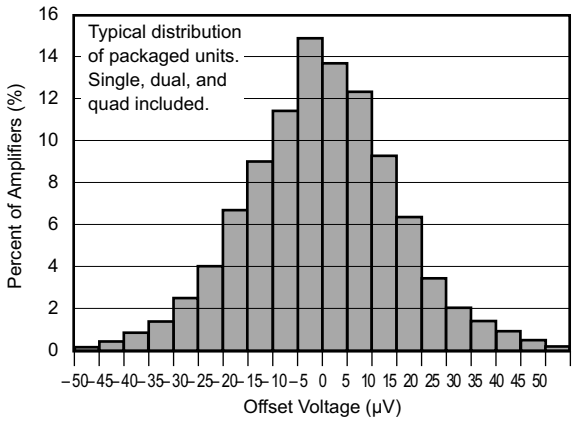


图 8-3. OPA2277 Laser-Trimmed Operational Amplifier Offset

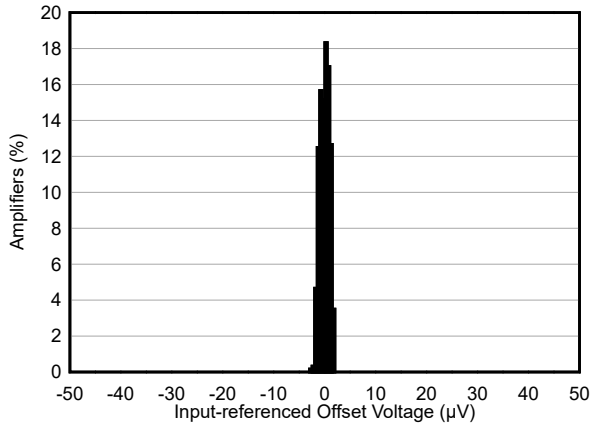


图 8-4. OPA2206 e-trim™ Operational Amplifier Offset

The OPA2206 is also trimmed at two temperatures to minimize the input offset voltage drift over temperature. The final performance of the offset drift can be seen in 图 8-5.

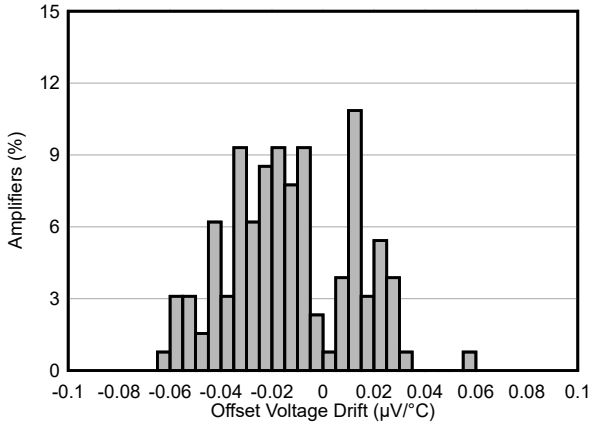


图 8-5. OPA2206 e-trim™ Operational Amplifier Drift

8.3.3 Lower Input Bias With Super-Beta Inputs

The OPA2206 has a super-beta input transistor architecture. In a transistor, the beta value is the ratio between the current flowing into the base and the current flowing from the collector to the emitter. A super-beta transistor is one where the beta value has been increased from several hundred to thousands. In a bipolar amplifier, the input bias current is the current flowing into the base of the input transistor pair, as well as a small leakage current that flows through the ESD diodes. A super-beta input reduces the input bias current of the amplifier. In addition, the super-beta inputs lower the input current noise that is directly related to the input bias current of the device. A comparison between the input bias current of the OPA2277 and the OPA2206 super-beta input bias currents can be seen in 图 8-6 and 图 8-7.

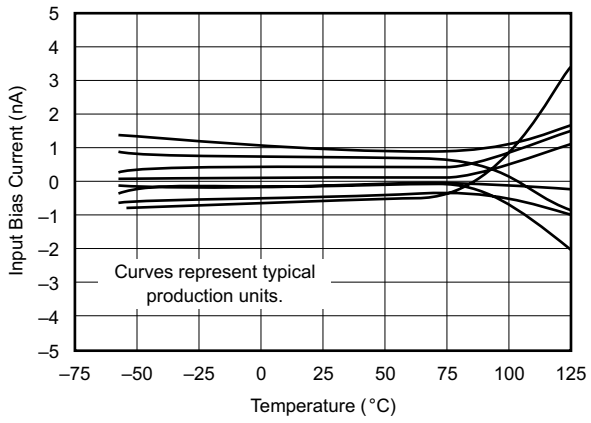


图 8-6. OPA2277 Input Bias Current

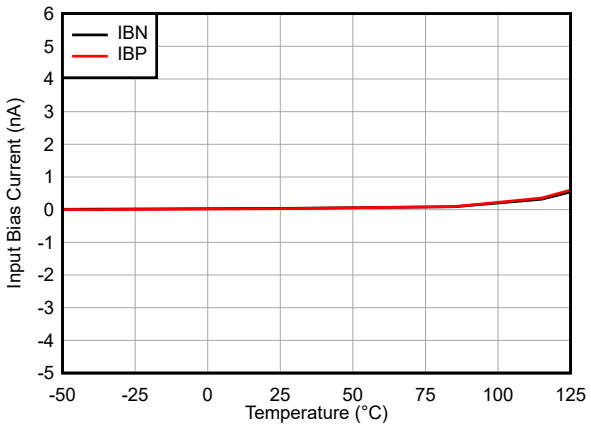


图 8-7. OPA2206 Super-Beta Input Bias Current

8.3.4 Overload Power Limiter

In many bipolar-based amplifiers, the output stage of the amplifier can draw significant (several milliamperes) of quiescent current if the output voltage becomes clipped (meaning the output voltage becomes limited by the negative or positive supply voltage). This condition can cause the system to enter a high-power consumption state, and potentially cause oscillations between the power supply and signal chain. The OPA2206 has an advanced output stage design that eliminates this problem. When the output voltage reaches the either supply (V+ or V –), there is virtually no additional current consumption from the nominal quiescent current. This feature helps eliminate any potential system problems when the signal chain is disrupted by a large external transient voltage.

8.3.5 EMI Rejection

The OPA2206 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources, such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved through circuit design techniques that improve the system performance. Additional information can be found in the *EMI Rejection Ratio of Operation Amplifiers* application report.

8.4 Device Functional Modes

The OPA2206 has two functional modes. The device enters normal operation with any supply between 4.5 V (±2.25 V) and 36 V (±18 V), and an input voltage that meets the input common-mode voltage range shown in 节 6.

If the input voltage exceeds the device specifications, the device will enter an overvoltage protection mode. In this mode the input overvoltage protection sub-circuit will limit the voltage and current seen by the amplifier core by adding additional impedance between the input pins and the amplifier core. Additional current that is generated from the voltage drop across this input impedance is routed through the ESD structure of the OPA2206, as shown in 图 8-1.

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The OPA2206 is a unity-gain stable operational amplifier with very low offset voltage, offset voltage drift, voltage noise, current noise, and power consumption. The built-in overvoltage protection allows the device to protect against signals outside of the expected range, a reverse connection, or in cases where the inputs are shorted to a system supply. These features make this device a great choice for a variety of space-constrained and power-constrained systems by removing the need for discrete protection such as clamping diodes.

9.2 Typical Applications

9.2.1 Voltage Attenuator

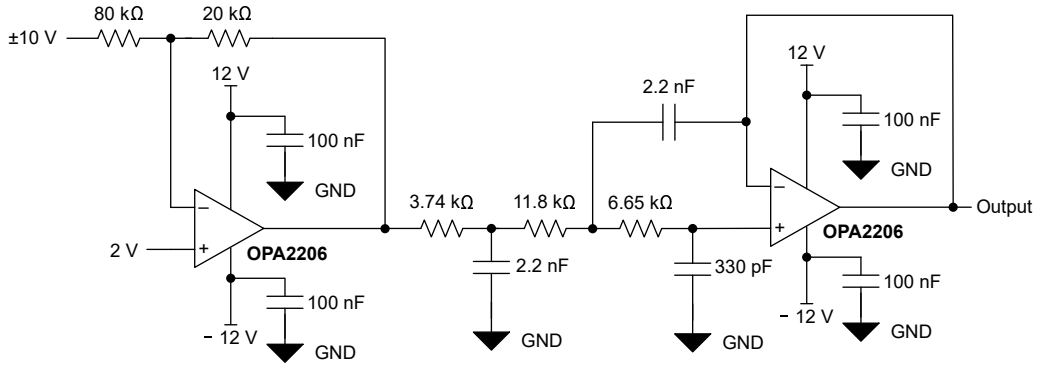


图 9-1. OPA2206 Configured as a Voltage Attenuator

9.2.1.1 Design Requirements

The design requirements for this system are:

- Input signal range: ±10 V
- Input signal frequency: up to 10 kHz
- 3rd-order Butterworth filter -3-dB frequency: 20 kHz
- Output voltage: 0 V to 5 V
- Input protection: up to ±52 V

9.2.1.2 Detailed Design Procedure

In this design, a ±10-V, 10-kHz bandwidth, bipolar signal is attenuated and converted to a single-ended signal and filtered by a 3rd-order Butterworth filter to drive a single-ended analog-to-digital converter (ADC). By using the OPA2206, the input of the signal chain is protected from overvoltages up to 40 V beyond either supply. This signal-chain design is common for programmable logic controllers (PLCs), low-power data acquisition systems (DAQs) and field instruments where high precision, low power and signal fault protection are needed.

The OPA2206 was selected for this application because of the high supply range, high dc precision (2-µV offset and 0.04-µV/°C offset drift), and low power consumption (220-µA quiescent current) that minimizes thermal dissipation requirements. Because of the internal OVP topology, the device provides better dc and ac accuracy under normal operating conditions compared to passive external protection and results in a smaller system solution. Be sure to connect a zener diode between each supply to ground to provide a return path for the current that is generated during a fault condition.

The first stage of the signal chain is an attenuator and level-shifter. The input signal to this stage is bipolar ±10 V that is attenuated to ±2.5 V, and then level-shifted so that the output is a single-ended, 0-V to 5-V signal. The

feedback and gain resistors were selected as 20 kΩ and 80 kΩ, respectively. Thus, the combined impedance is 100 kΩ, which lowers the input current to the signal chain, and minimizes errors resulting from higher output impedance sensors.

The second stage of the signal chain uses the second channel of the OPA2206 to create a 3rd-order Butterworth filter with a –3-dB response of 20 kHz. For more information on filter design, refere to Texas Instrument's filter design tool.

The output of this signal chain is shown in 图 9-2 and the filter response is shown in 图 9-3.

9.2.1.3 Application Curves

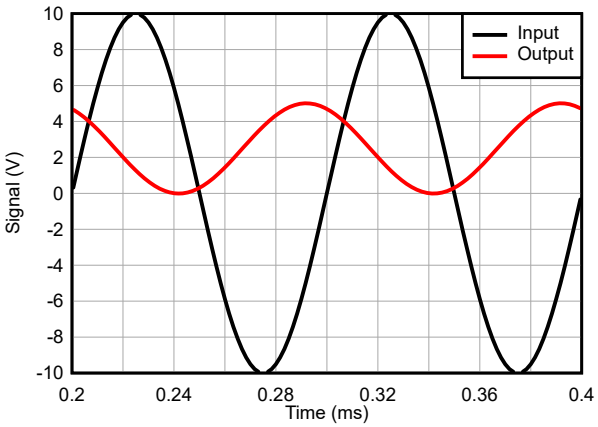


图 9-2. Input and Output Signal

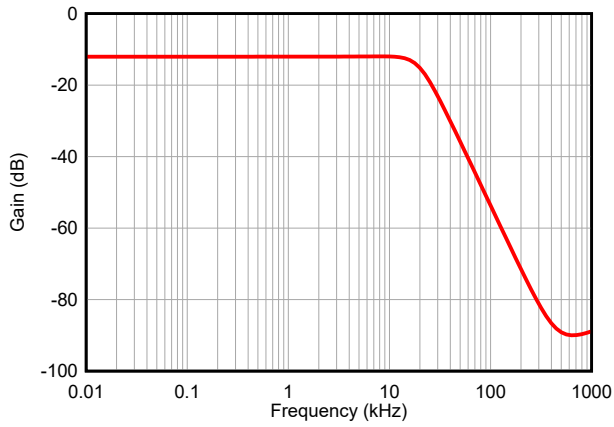


图 9-3. Attenuator + Filter Response

9.2.2 Discrete, Two-Op-Amp Instrumentation Amplifier

图 9-4 shows the OPA2206 configured as a two op amp, discrete instrumentation amplifier. This configuration allows for a differential signal measurement, such as the signal from a load cell, with higher input impedance to the signal chain than most monolithic instrumentation amplifiers. Additionally, the input overvoltage protection of the OPA2206 protects the signal chain from being damaged by fault conditions where the input signal exceeds the supply voltage of the amplifier.

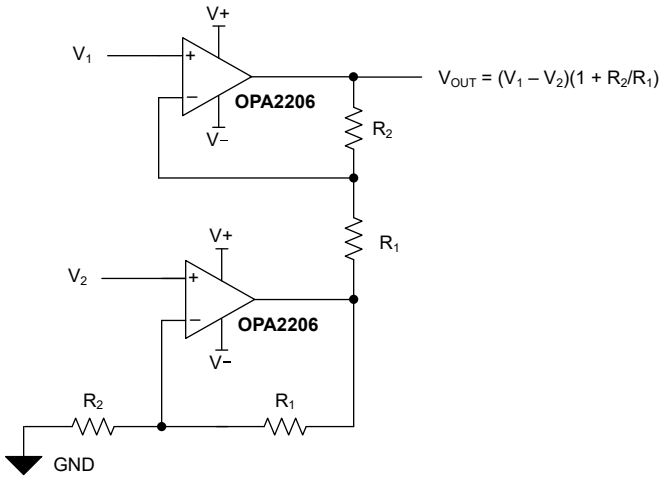


图 9-4. OPA2206 Configured as a Two Op Amp, Discrete Instrumentation Amplifier

9.2.3 Input Buffer and Protection for ADC Driver

节 9.2.1.1 shows the OPA2206 configured as an input buffer for an ADC driver using the THP210. The high dc precision and low noise of the OPA2206 make this device an excellent choice for precision signal chain

conditioning. The low input bias of the amplifier minimizes dc errors created for higher output impedance sensors. The integrated input overvoltage protection prevents damage to the signal chain due to an input fault condition where the signal exceeds the supply range of the OPA2206, or if the inputs are shorted to a higher supply rail. For more information on designing a precision ADC driver,see .

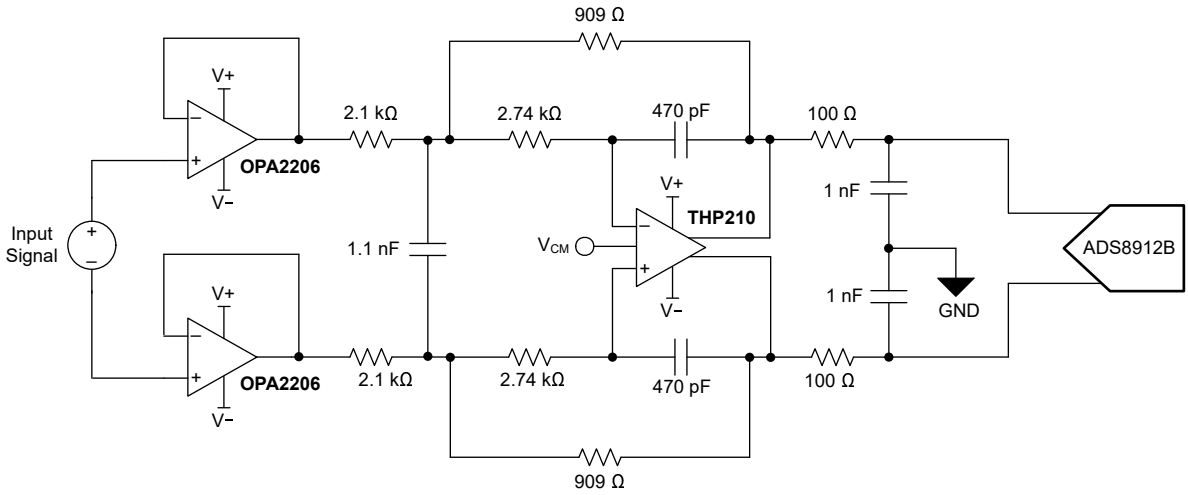


图 9-5. OPA2206 Configured as Input-Signal-Chain Buffer

10 Power Supply Recommendations

The OPA2206 operates with a supply between 4.5 V (±2.25 V) and 36 V (±18 V). Parameters that can exhibit significant variance with regard to operating voltages are presented in 节 6.7.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications. Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as through the individual op amp. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Make sure to physically separate digital and analog grounds and pay attention to the flow of the ground current. Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better, as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 图 11-1, keep RF and RG close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

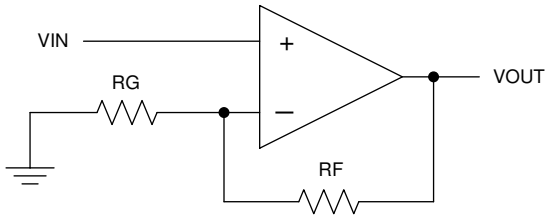


图 11-1. Schematic Representation

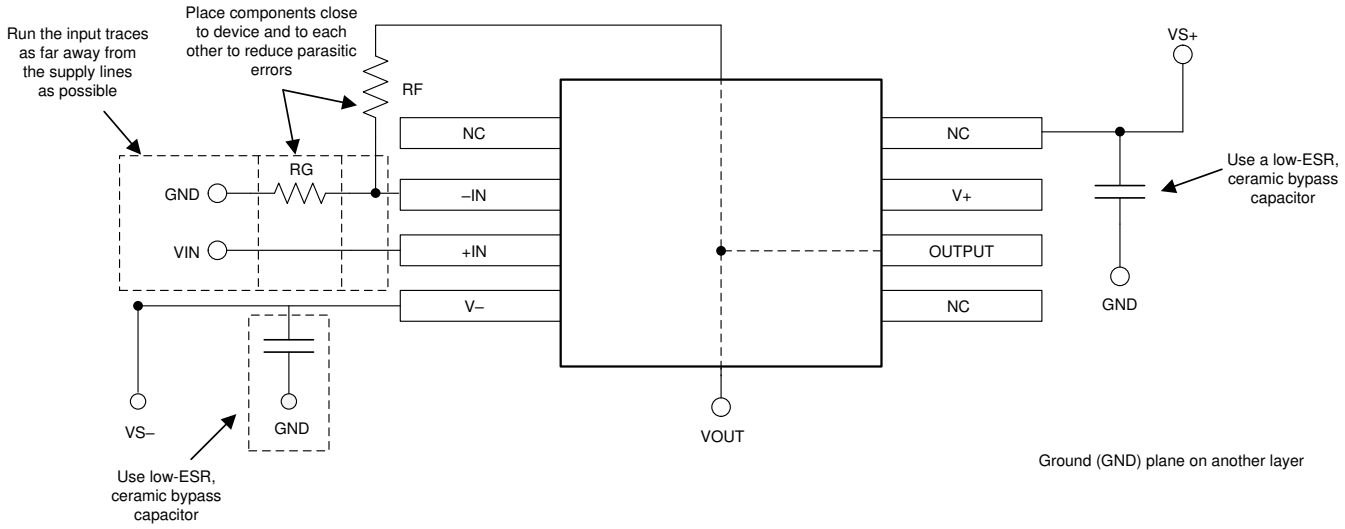


图 11-2. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

The following evaluation modules are available:

- DIP-ADAPTER-EVM
- DIYAMP-EVM

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2206ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22A6	Samples
OPA2206ADGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22A6	Samples
XOPA2206DGKR	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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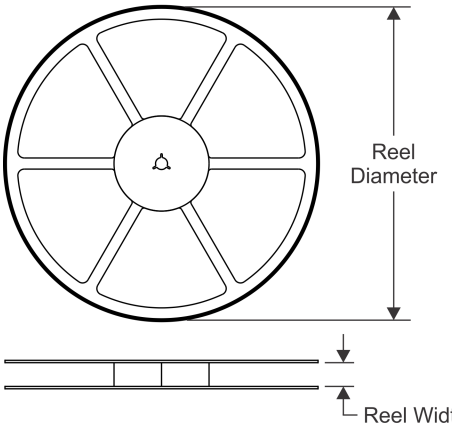
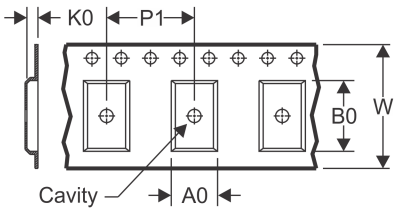
TAPE AND REEL INFORMATION

REEL DIMENSIONS

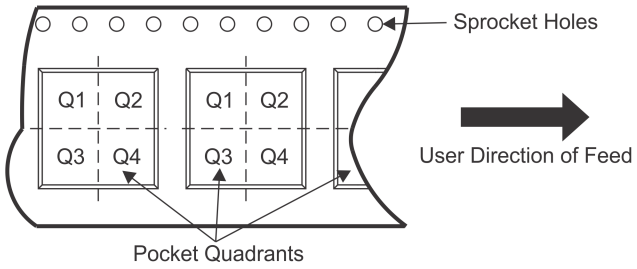


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

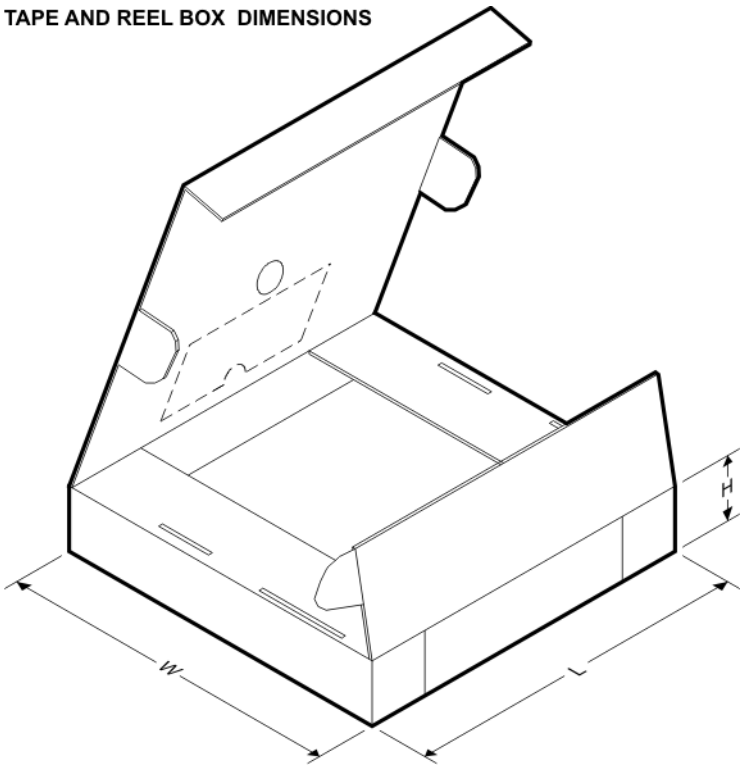
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2206ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2206ADGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

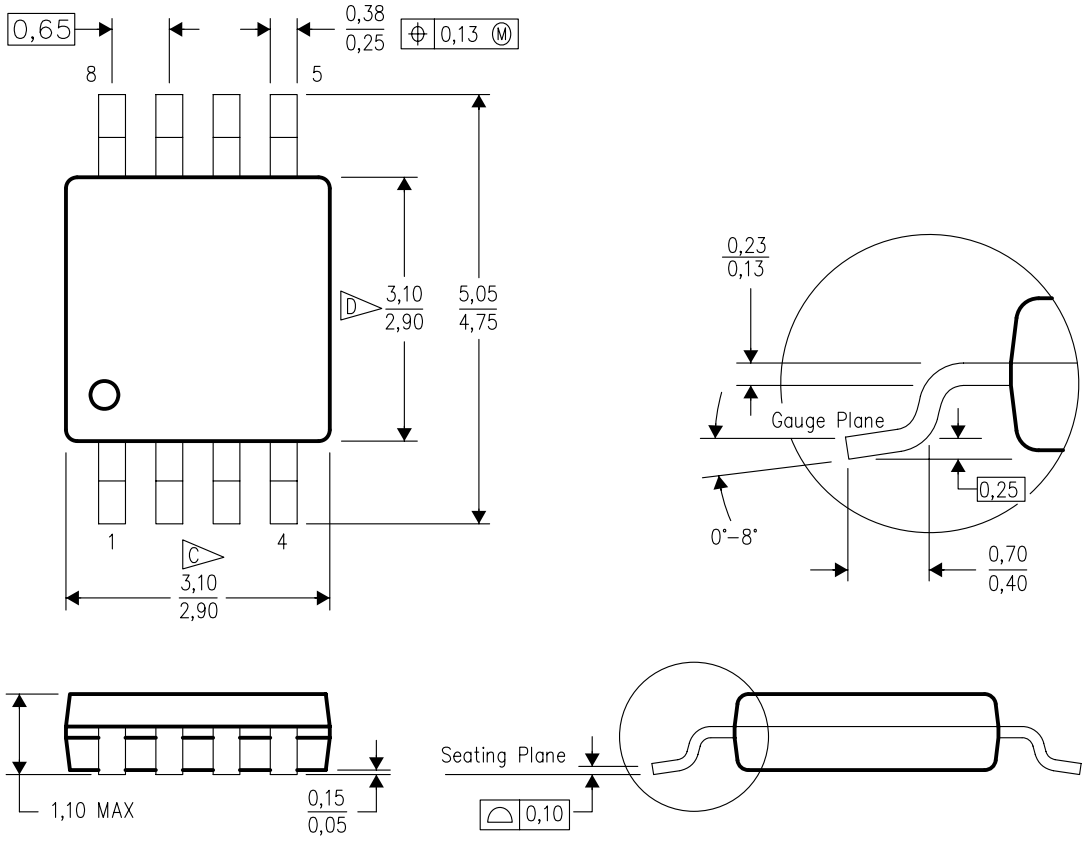
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2206ADGKR	VSSOP	DGK	8	2500	853.0	449.0	35.0
OPA2206ADGKT	VSSOP	DGK	8	250	210.0	185.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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