

SN75174

QUADRUPLE DIFFERENTIAL LINE DRIVER

SLLS039B – OCTOBER 1980 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11.
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Output Voltage Range of -7 V to 12 V
- Active-High Enable
- Thermal Shutdown Protection
- Positive- and Negative-Current Limiting
- Operates From Single 5-V Supply
- Low Power Requirements
- Functionally Interchangeable With MC3487

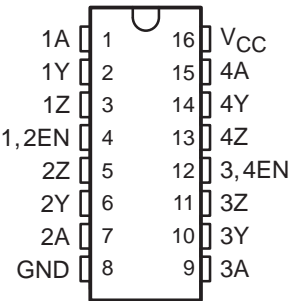
description

The SN75174 is a monolithic quadruple differential line driver with 3-state outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11. The device is optimized for balanced multipoint bus transmission at rates up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

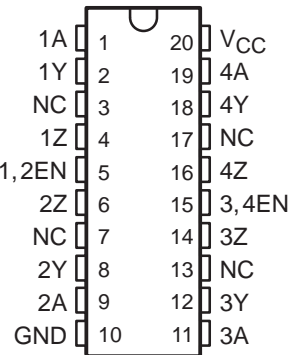
The SN75174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C . This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

The SN75174 is characterized for operation from 0°C to 70°C .

**N PACKAGE
(TOP VIEW)**



**DW PACKAGE
(TOP VIEW)**



NC – No internal connection

**FUNCTION TABLE
(each driver)**

INPUT	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = TTL high level, X = irrelevant,
L = TTL low level, Z = high impedance (off)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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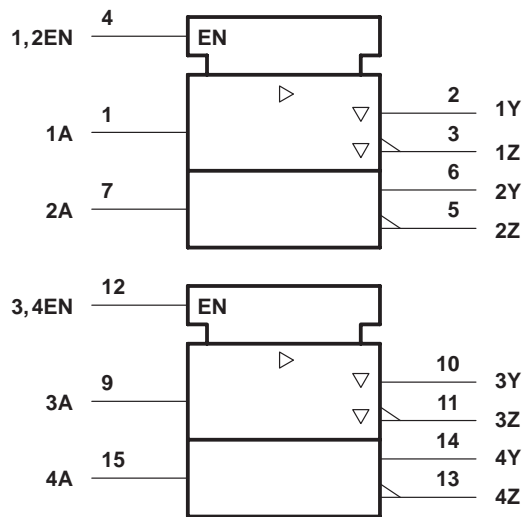
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SN75174

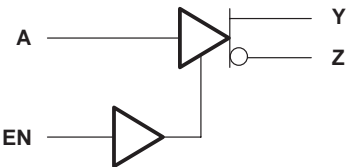
QUADRUPLE DIFFERENTIAL LINE DRIVER

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logic symbol†

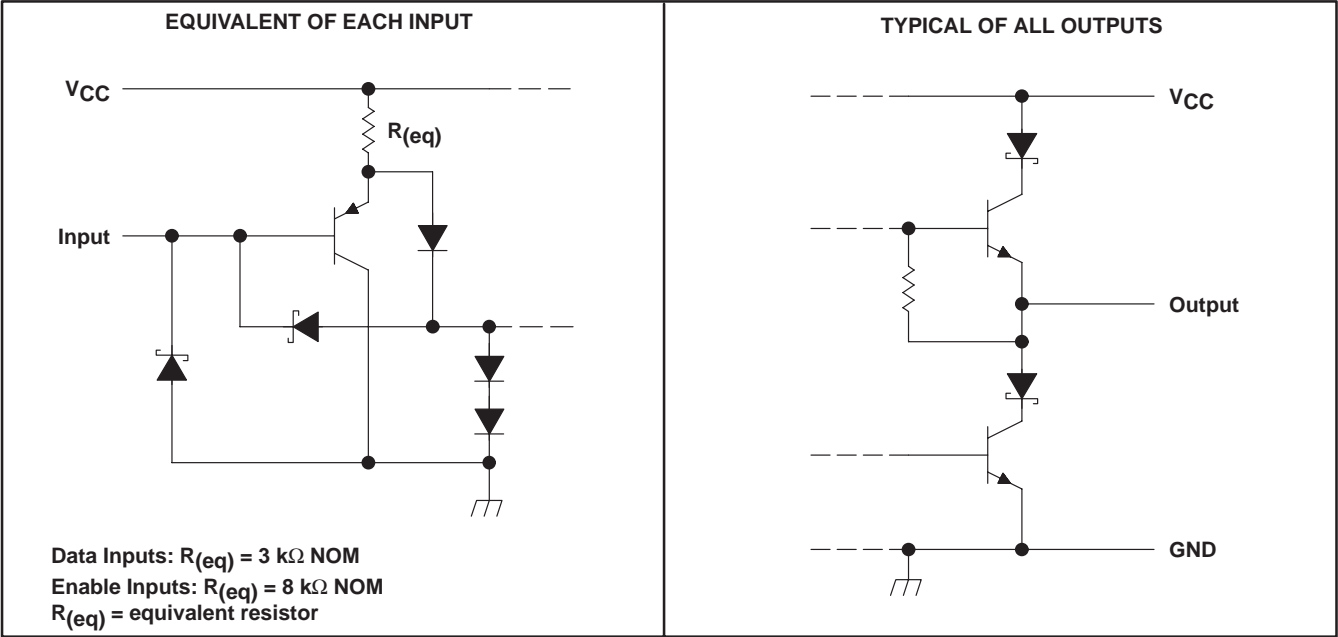


logic diagram, each driver (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Output voltage range, V_O	–10 V to 15 V
Input voltage, V_I	5.5 V
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}		–7 to 12		V
High-level output current, I_{OH}			–60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -18\text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{IH} = 2\text{ V}$, $I_{OH} = -33\text{ mA}$ $V_{IL} = 0.8\text{ V}$		3.7		V
V_{OL} Low-level output voltage	$V_{IH} = 2\text{ V}$, $I_{OL} = 33\text{ mA}$ $V_{IL} = 0.8\text{ V}$		1.1		V
V_O Output voltage	$I_O = 0$	0		6	V
$ V_{OD1} $ Differential output voltage	$I_O = 0$	1.5	6	6	V
$ V_{OD2} $ Differential output voltage	$R_L = 100\ \Omega$, See Figure 1	$\frac{1}{2} V_{OD1}$ or $2\ddagger$			V
	$R_L = 54\ \Omega$, See Figure 1	1.5	2.5	5	V
V_{OD3} Differential output voltage	See Note 2	1.5		5	V
$\Delta V_{OD} $ Change in magnitude of differential output voltage§	$R_L = 54\ \Omega$ or $100\ \Omega$, See Figure 1			± 0.2	V
V_{OC} Common-mode output voltage¶				+3 -1	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage§				± 0.2	V
I_O Output current with power off	$V_{CC} = 0$, $V_O = -7\text{ V to }12\text{ V}$			± 100	μA
I_{OZ} High-impedance-state output current	$V_O = -7\text{ V to }12\text{ V}$			± 100	μA
I_{IH} High-level input current	$V_I = 2.7\text{ V}$			20	μA
I_{IL} Low-level input current	$V_I = 0.5\text{ V}$			-360	μA
I_{OS} Short-circuit output current	$V_O = -7\text{ V}$			-180	mA
	$V_O = V_{CC}$			180	
	$V_O = 12\text{ V}$			500	
I_{CC} Supply current (all drivers)	No load	Outputs enabled	38	60	mA
		Outputs disabled	18	40	

† All typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

‡ The minimum V_{OD2} with a $100\text{-}\Omega$ load is either $\frac{1}{2} V_{OD1}$ or 2 V , whichever is greater.

§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

¶ In ANSI Standard EIA/TIA-422-B, V_{OC} , which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS} .

NOTE 2: See EIA Standard RS-485.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_d(\text{OD})$ Differential-output delay time	$R_L = 54\ \Omega$, See Figure 2		45	65	ns
$t_t(\text{OD})$ Differential-output transition time			80	120	ns
t_{PZH} Output enable time to high level	$R_L = 110\ \Omega$, See Figure 3		80	120	ns
t_{PZL} Output enable time to low level	$R_L = 110\ \Omega$, See Figure 4		55	80	ns
t_{PHZ} Output disable time from high level	$R_L = 110\ \Omega$, See Figure 3		75	115	ns
t_{PLZ} Output disable time from low level	$R_L = 110\ \Omega$, See Figure 3		18	30	ns



SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$ V_{OD1} $	V_o	V_o
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $		V_t (Test Termination) Measurement 2)
$\Delta V_{OD} $	$ V_t - \bar{V}_t $	$ V_t - \bar{V}_t $
V_{OC}	$ V_{os} $	$ V_{os} $
$\Delta V_{OC} $	$ V_{os} - \bar{V}_{os} $	$ V_{os} - \bar{V}_{os} $
I_{OS}	$ I_{sa} , I_{sb} $	
I_O	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}

PARAMETER MEASUREMENT INFORMATION

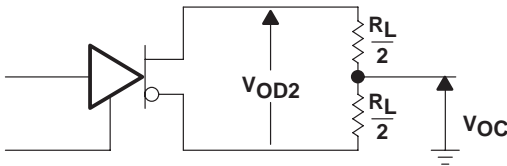
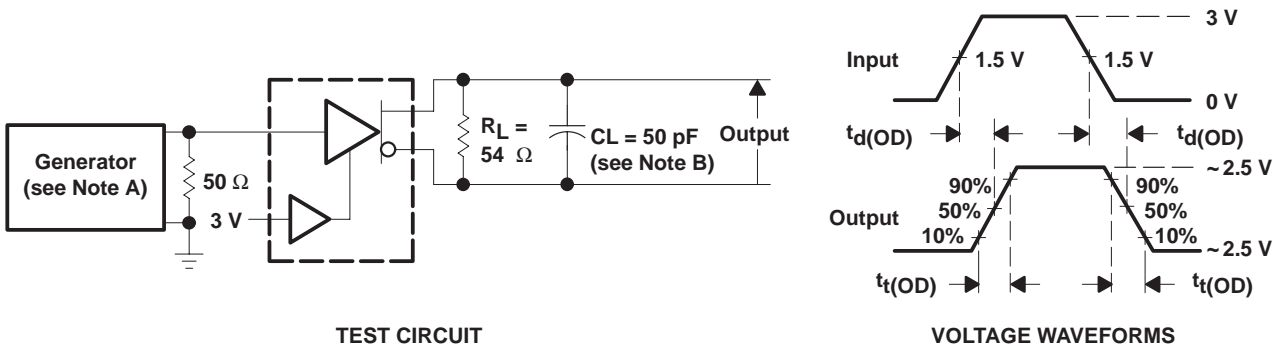


Figure 1. Differential and Common-Mode Output Voltages



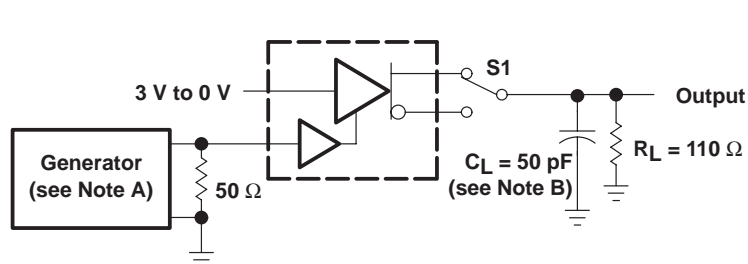
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5 \text{ ns}$, $t_f \leq 5 \text{ ns}$, $\text{PRR} \leq 1 \text{ MHz}$, duty cycle = 50%, $Z_O = 50 \Omega$.
B. C_L includes probe and stray capacitance.

Figure 2. Differential-Output Test Circuit and Voltage Waveforms

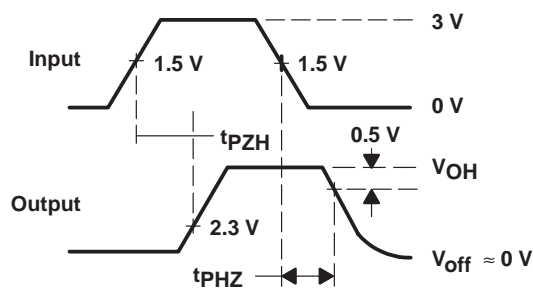
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PARAMETER MEASUREMENT INFORMATION



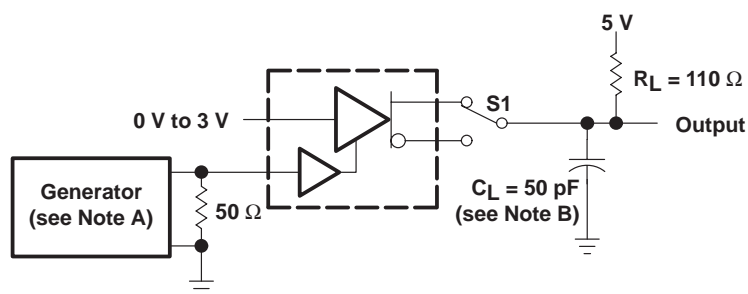
TEST CIRCUIT



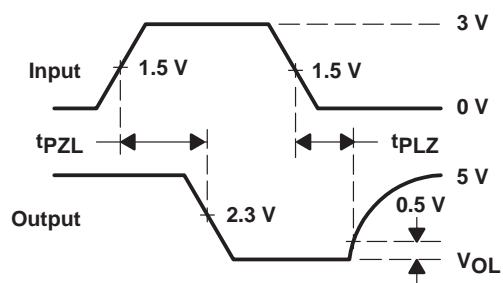
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, duty cycle = 50%, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and stray capacitance.

Figure 3. Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, duty cycle = 50%, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and stray capacitance.

Figure 4. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

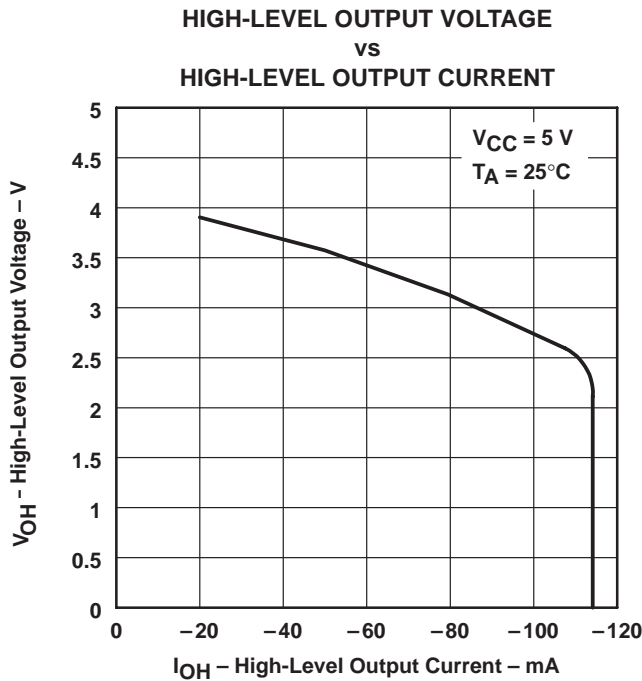


Figure 5

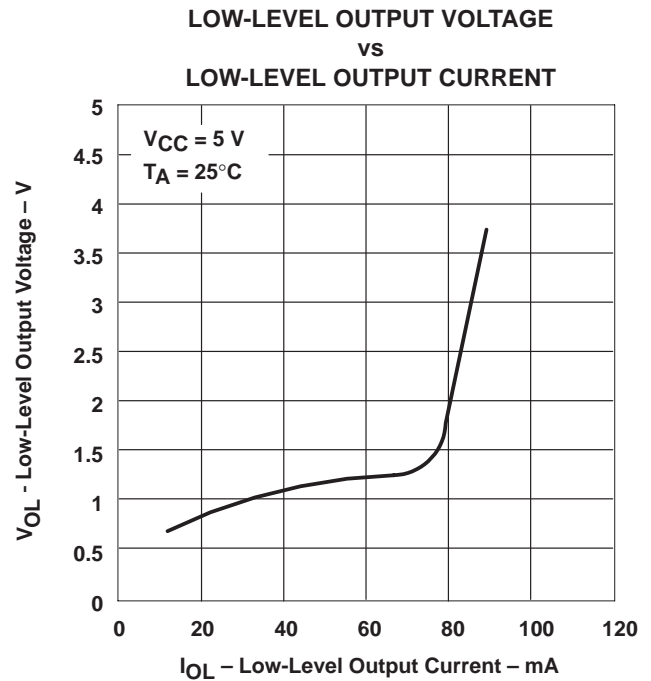


Figure 6

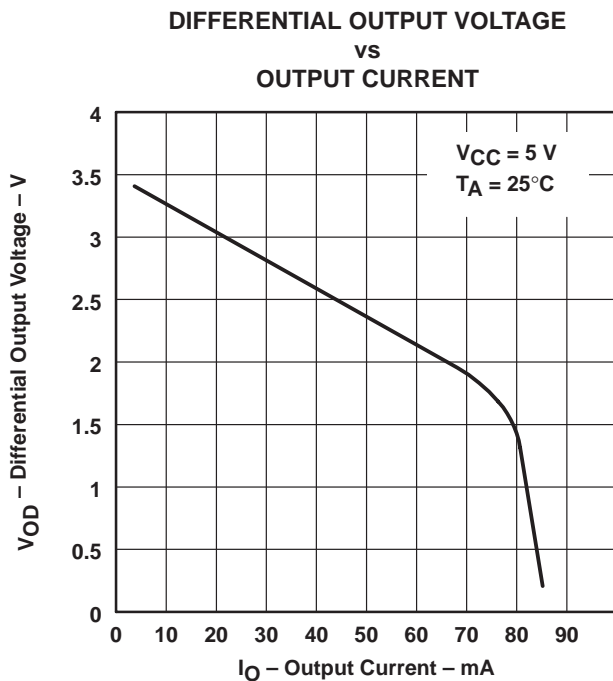


Figure 7

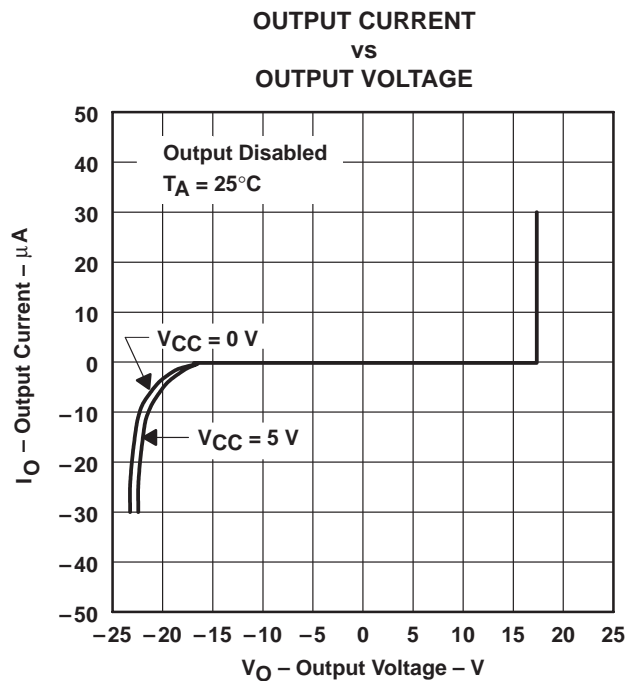


Figure 8

SN75174 QUADRUPLE DIFFERENTIAL LINE DRIVER

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TYPICAL CHARACTERISTICS

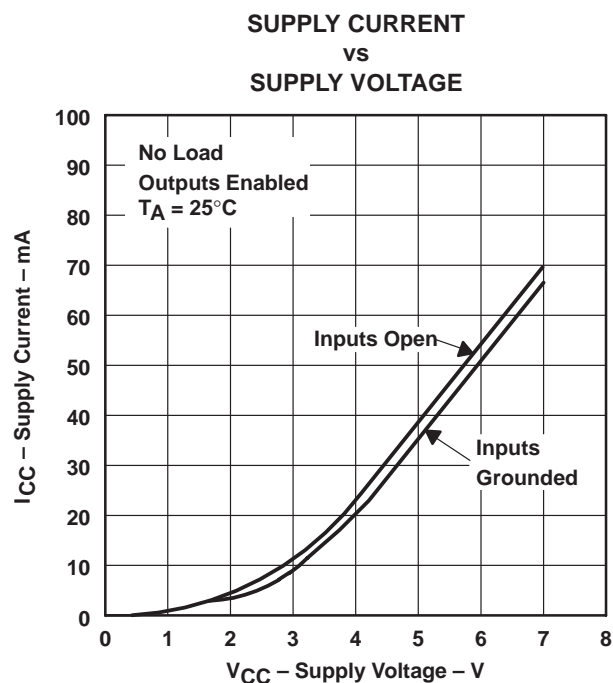


Figure 9

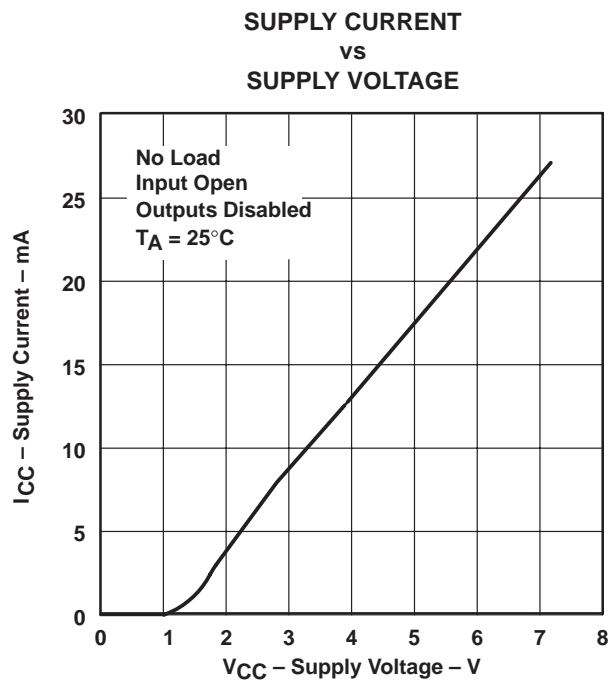
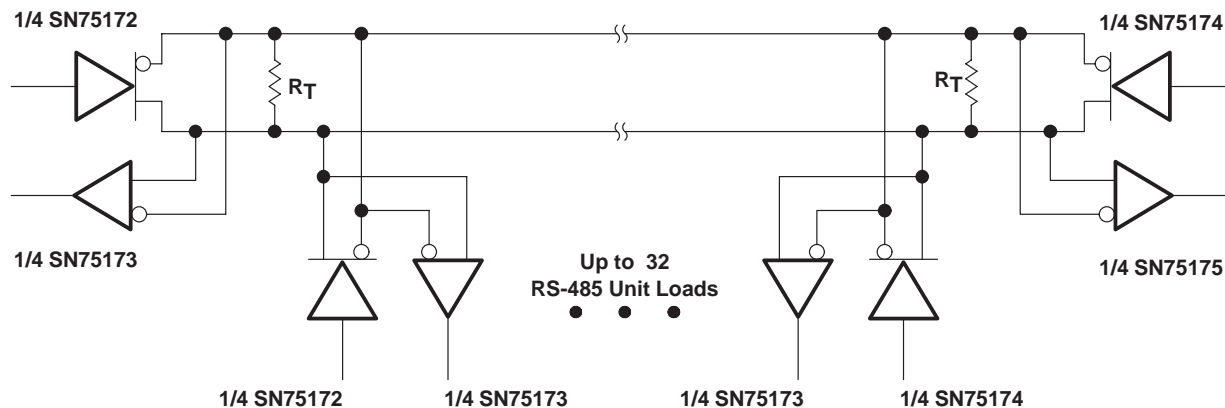


Figure 10

APPLICATION INFORMATION



NOTE: The line length should be terminated at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 11. Typical Application Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75174DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75174	Samples
SN75174DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75174	Samples
SN75174DWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75174	Samples
SN75174DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75174	Samples
SN75174N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75174N	Samples
SN75174NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75174N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

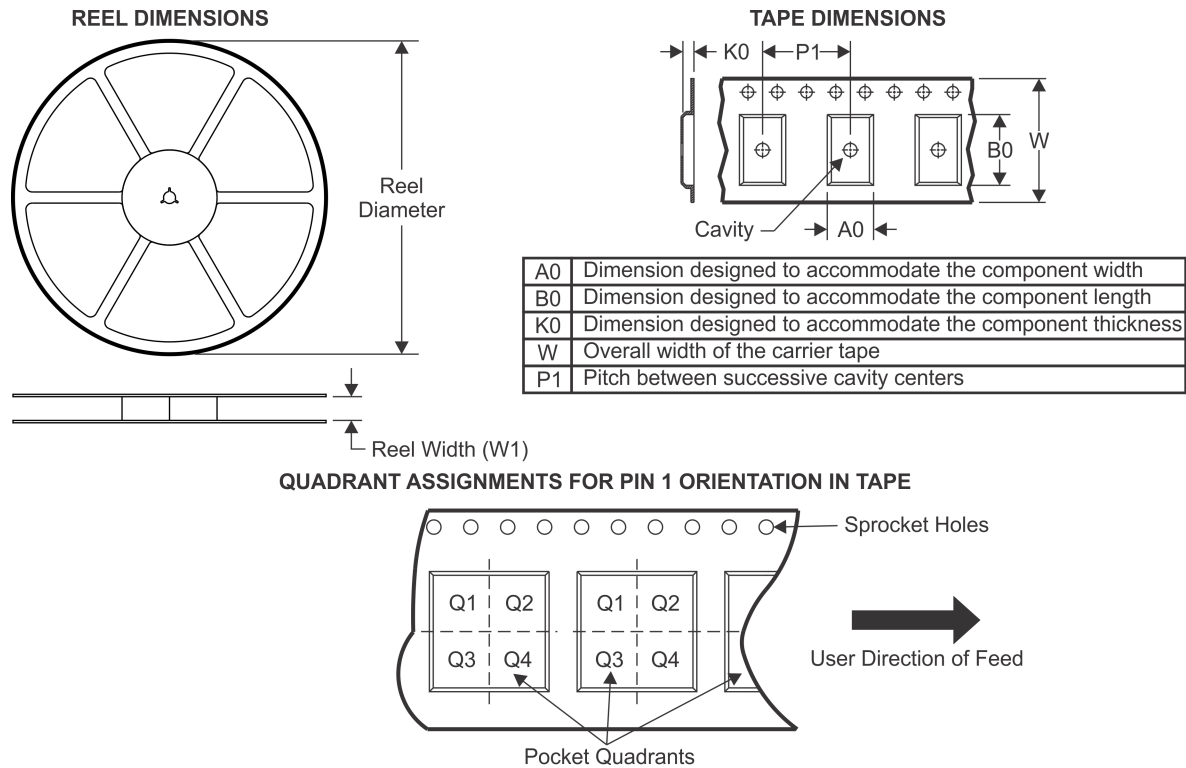
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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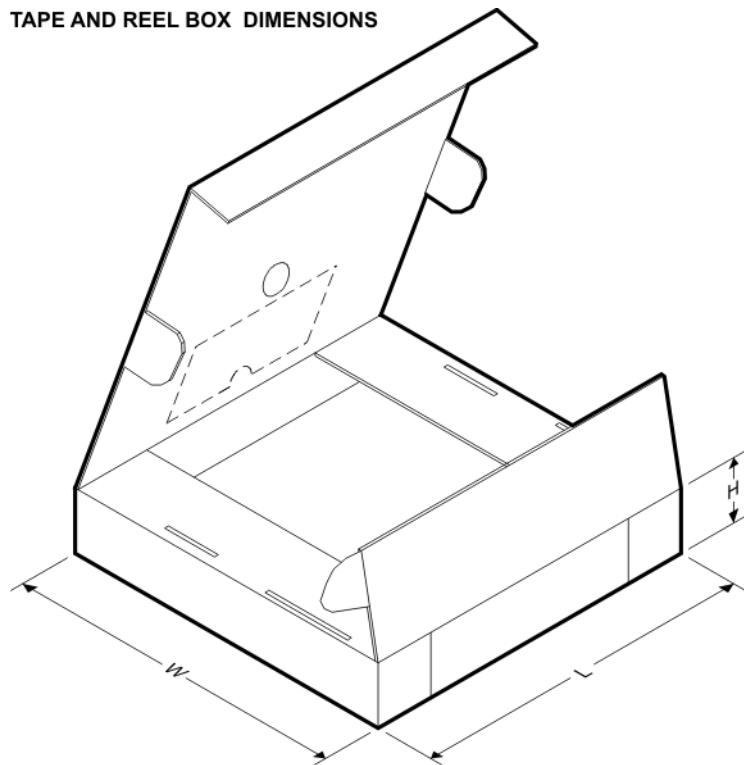
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75174DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

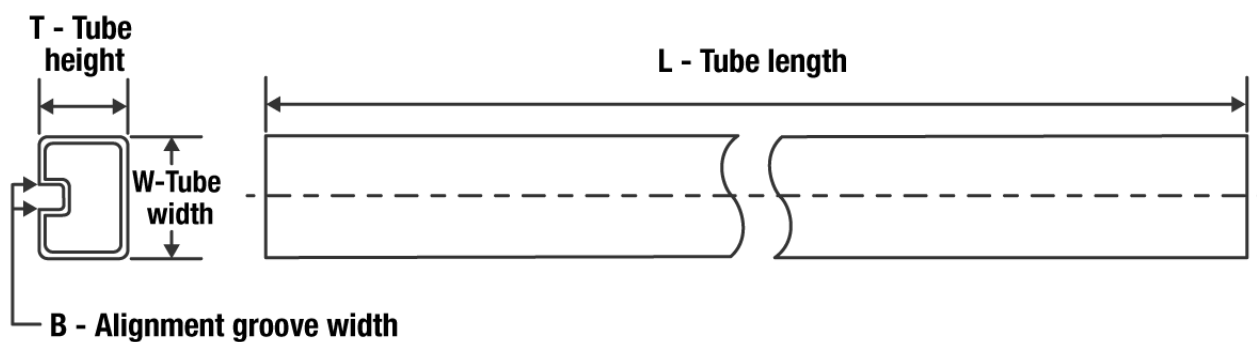
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75174DWR	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE



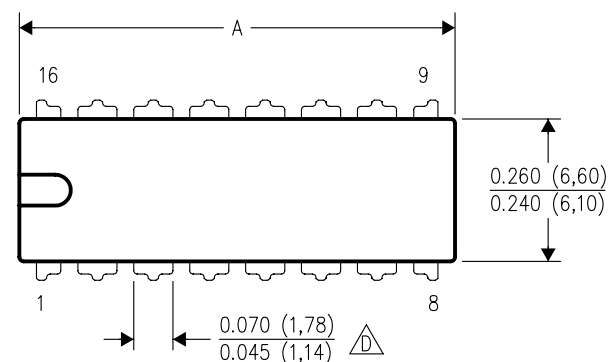
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75174DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75174DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN75174N	N	PDIP	16	25	506	13.97	11230	4.32
SN75174NE4	N	PDIP	16	25	506	13.97	11230	4.32

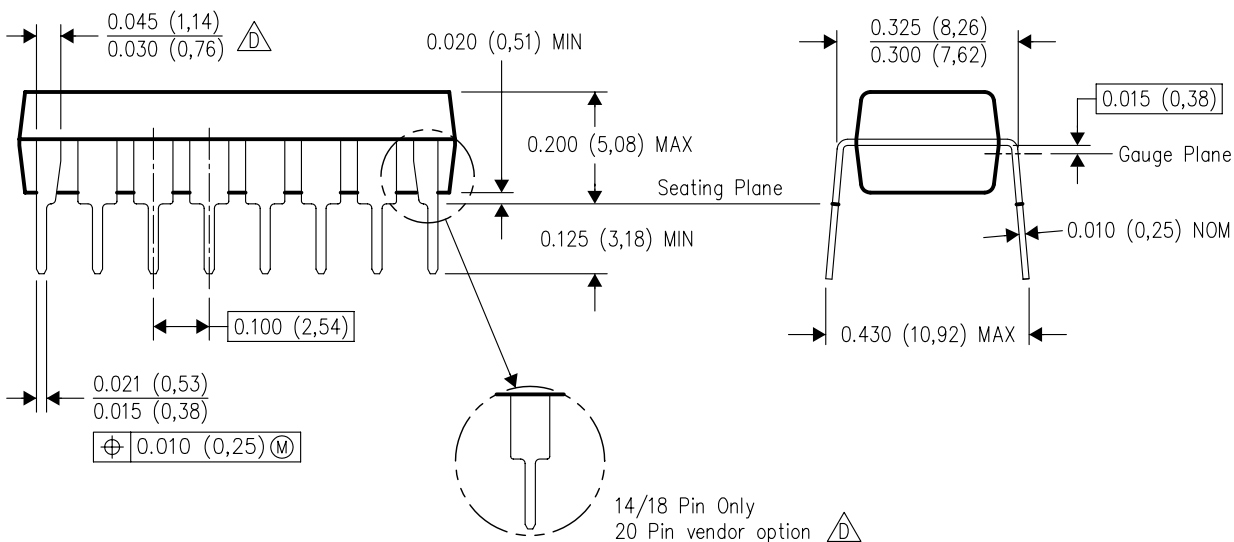
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE





PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



SOIC - 2.65 mm max height

Technical drawing of a 20-pin connector showing top, side, and detail views with dimensions and callouts.

Top View:

- Overall width: 10.63 (9.97 TYP)
- Overall height: 13.0 (12.6 NOTE 3)
- Pin 1 ID AREA (dotted pattern)
- Pin 1 location: 1
- Pin 10 location: 10
- Pin 11 location: 11
- Pin 20 location: 20
- Pin 18 location: 18X 1.27
- Pin 2 location: 2X 11.43
- Pin 20X location: 20X 0.51 0.31
- Pin 7.6 location: 7.6 (7.4 NOTE 4)
- Pin 10.63 location: 10.63 (9.97 TYP)
- Pin 13.0 location: 13.0 (12.6 NOTE 3)
- Pin 16.5 location: 16.5 (16.0 NOTE 3)
- Pin 19.5 location: 19.5 (19.0 NOTE 3)
- Pin 22.5 location: 22.5 (22.0 NOTE 3)
- Pin 25.5 location: 25.5 (25.0 NOTE 3)
- Pin 28.5 location: 28.5 (28.0 NOTE 3)
- Pin 31.5 location: 31.5 (31.0 NOTE 3)
- Pin 34.5 location: 34.5 (34.0 NOTE 3)
- Pin 37.5 location: 37.5 (37.0 NOTE 3)
- Pin 40.5 location: 40.5 (40.0 NOTE 3)
- Pin 43.5 location: 43.5 (43.0 NOTE 3)
- Pin 46.5 location: 46.5 (46.0 NOTE 3)
- Pin 49.5 location: 49.5 (49.0 NOTE 3)
- Pin 52.5 location: 52.5 (52.0 NOTE 3)
- Pin 55.5 location: 55.5 (55.0 NOTE 3)
- Pin 58.5 location: 58.5 (58.0 NOTE 3)
- Pin 61.5 location: 61.5 (61.0 NOTE 3)
- Pin 64.5 location: 64.5 (64.0 NOTE 3)
- Pin 67.5 location: 67.5 (67.0 NOTE 3)
- Pin 70.5 location: 70.5 (70.0 NOTE 3)
- Pin 73.5 location: 73.5 (73.0 NOTE 3)
- Pin 76.5 location: 76.5 (76.0 NOTE 3)
- Pin 79.5 location: 79.5 (79.0 NOTE 3)
- Pin 82.5 location: 82.5 (82.0 NOTE 3)
- Pin 85.5 location: 85.5 (85.0 NOTE 3)
- Pin 88.5 location: 88.5 (88.0 NOTE 3)
- Pin 91.5 location: 91.5 (91.0 NOTE 3)
- Pin 94.5 location: 94.5 (94.0 NOTE 3)
- Pin 97.5 location: 97.5 (97.0 NOTE 3)
- Pin 100.5 location: 100.5 (100.0 NOTE 3)
- Pin 103.5 location: 103.5 (103.0 NOTE 3)
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- Pin 127.5 location: 127.5 (127.0 NOTE 3)
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- Pin 136.5 location: 136.5 (136.0 NOTE 3)
- Pin 139.5 location: 139.5 (139.0 NOTE 3)
- Pin 142.5 location: 142.5 (142.0 NOTE 3)
- Pin 145.5 location: 145.5 (145.0 NOTE 3)
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- Pin 178.5 location: 178.5 (178.0 NOTE 3)
- Pin 181.5 location: 181.5 (181.0 NOTE 3)
- Pin 184.5 location: 184.5 (184.0 NOTE 3)
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- Pin 196.5 location: 196.5 (196.0 NOTE 3)
- Pin 199.5 location: 199.5 (199.0 NOTE 3)
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- Pin 211.5 location: 211.5 (211.0 NOTE 3)
- Pin 214.5 location: 214.5 (214.0 NOTE 3)
- Pin 217.5 location: 217.5 (217.0 NOTE 3)
- Pin 220.5 location: 220.5 (220.0 NOTE 3)
- Pin 223.5 location: 223.5 (223.0 NOTE 3)
- Pin 226.5 location: 226.5 (226.0 NOTE 3)
- Pin 229.5 location: 229.5 (229.0 NOTE 3)
- Pin 232.5 location: 232.5 (232.0 NOTE 3)
- Pin 235.5 location: 235.5 (235.0 NOTE 3)
- Pin 238.5 location: 238.5 (238.0 NOTE 3)
- Pin 241.5 location: 241.5 (241.0 NOTE 3)
- Pin 244.5 location: 244.5 (244.0 NOTE 3)
- Pin 247.5 location: 247.5 (247.0 NOTE 3)
- Pin 250.5 location: 250.5 (250.0 NOTE 3)
- Pin 253.5 location: 253.5 (253.0 NOTE 3)
- Pin 256.5 location: 256.5 (256.0 NOTE 3)
- Pin 259.5 location: 259.5 (259.0 NOTE 3)
- Pin 262.5 location: 262.5 (262.0 NOTE 3)
- Pin 265.5 location: 265.5 (265.0 NOTE 3)
- Pin 268.5 location: 268.5 (268.0 NOTE 3)
- Pin 271.5 location: 271.5 (271.0 NOTE 3)
- Pin 274.5 location: 274.5 (274.0 NOTE 3)
- Pin 277.5 location: 277.5 (277.0 NOTE 3)
- Pin 280.5 location: 280.5 (280.0 NOTE 3)
- Pin 283.5 location: 283.5 (283.0 NOTE 3)
- Pin 286.5 location: 286.5 (286.0 NOTE 3)
- Pin 289.5 location: 289.5 (289.0 NOTE 3)
- Pin 292.5 location: 292.5 (292.0 NOTE 3)
- Pin 295.5 location: 295.5 (295.0 NOTE 3)
- Pin 298.5 location: 298.5 (298.0 NOTE 3)
- Pin 301.5 location: 301.5 (301.0 NOTE 3)
- Pin 304.5 location: 304.5 (304.0 NOTE 3)
- Pin 307.5 location: 307.5 (307.0 NOTE 3)
- Pin 310.5 location: 310.5 (310.0 NOTE 3)
- Pin 313.5 location: 313.5 (313.0 NOTE 3)
- Pin 316.5 location: 316.5 (316.0 NOTE 3)
- Pin 319.5 location: 319.5 (319.0 NOTE 3)
- Pin 322.5 location: 322.5 (322.0 NOTE 3)
- Pin 325.5 location: 325.5 (325.0 NOTE 3)
- Pin 328.5 location: 328.5 (328.0 NOTE 3)
- Pin 331.5 location: 331.5 (331.0 NOTE 3)
- Pin 334.5 location: 334.5 (334.0 NOTE 3)
- Pin 337.5 location: 337.5 (337.0 NOTE 3)
- Pin 340.5 location: 340.5 (340.0 NOTE 3)
- Pin 343.5 location: 343.5 (343.0 NOTE 3)
- Pin 346.5 location: 346.5 (346.0 NOTE 3)
- Pin 349.5 location: 349.5 (349.0 NOTE 3)
- Pin 352.5 location: 352.5 (352.0 NOTE 3)
- Pin 355.5 location: 355.5 (355.0 NOTE 3)
- Pin 358.5 location: 358.5 (358.0 NOTE 3)
- Pin 361.5 location: 361.5 (361.0 NOTE 3)
- Pin 364.5 location: 364.5 (364.0 NOTE 3)
- Pin 367.5 location: 367.5 (367.0 NOTE 3)
- Pin 370.5 location: 370.5 (370.0 NOTE 3)
- Pin 373.5 location: 373.5 (373.0 NOTE 3)
- Pin 376.5 location: 376.5 (376.0 NOTE 3)
- Pin 379.5 location: 379.5 (379.0 NOTE 3)
- Pin 382.5 location: 382.5 (382.0 NOTE 3)
- Pin 385.5 location: 385.5 (385.0 NOTE 3)
- Pin 388.5 location: 388.5 (388.0 NOTE 3)
- Pin 391.5 location: 391.5 (391.0 NOTE 3)
- Pin 394.5 location: 394.5 (394.0 NOTE 3)
- Pin 397.5 location: 397.5 (397.0 NOTE 3)
- Pin 4

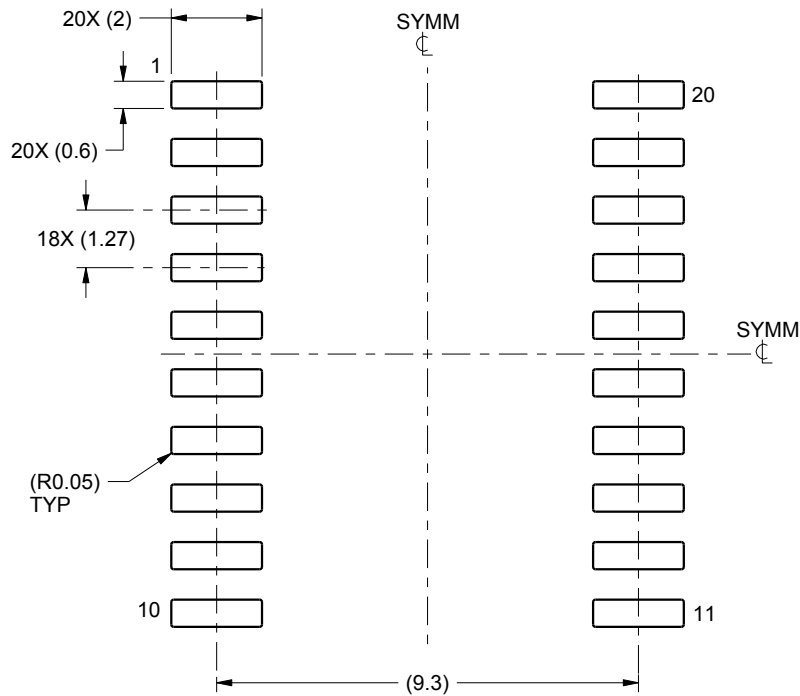
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

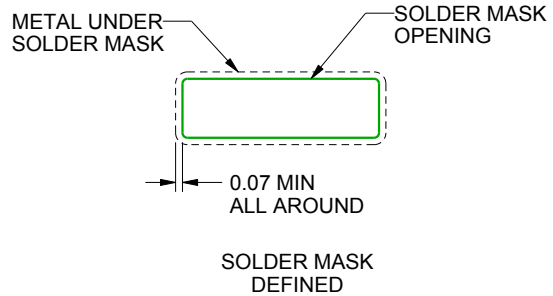
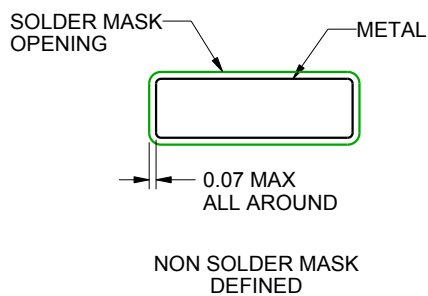
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

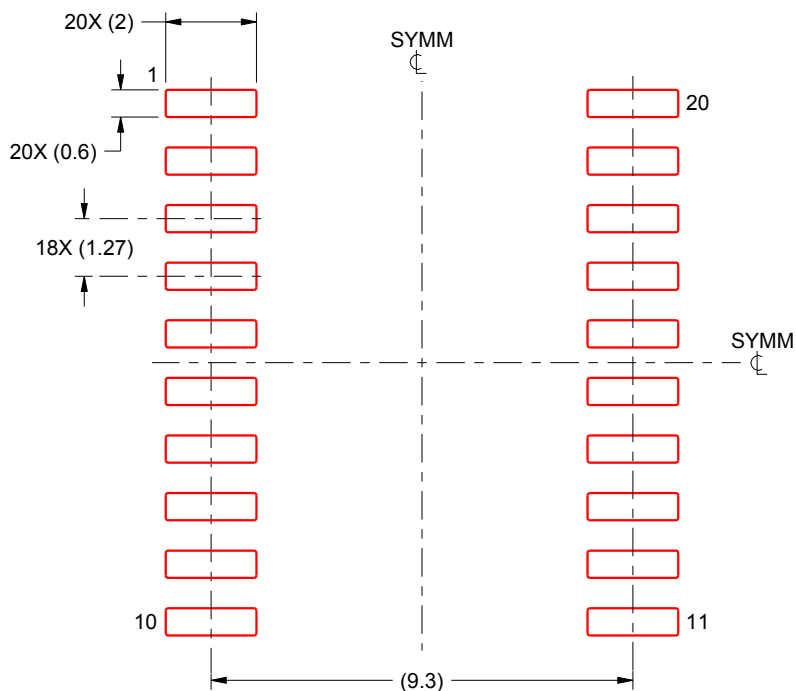
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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