

TPS22933 具有自动选择功能和低压降稳压器的三路输入电源多路复用器

1 特性

- 三个集成负载开关，自动选择最高电平输入
- 集成 3.6V 固定电压低压降 (LDO) 稳压器
- 提供开关控制式和始终开启式两种 LDO 输出
- 采用 1.5mm × 1.5mm μ QFN 封装
- 输入电压范围：2.5V 至 12V
- 低导通电阻 (r_{ON})
 - $V_{IN} = 5.0V$ 时， $r_{ON} = 2.4\Omega$
 - $V_{IN} = 4.2V$ 时， $r_{ON} = 2.6\Omega$
- 50mA 的最大持续电流
- 低阈值控制输入 (EN)
- 切换时间：18 μ s (典型值)

2 应用范围

- 智能电话
- 全球卫星定位 (GPS) 设备
- 数码摄像机
- 便携式工业设备
- 便携式医疗设备
- 便携式媒体播放器
- 便携式仪表

3 说明

TPS22933 器件是一款具有自动输入选择功能和低压降线性稳压器的三路输入电源多路复用器，同时兼具小尺寸和低 r_{ON} 特性。此器件包含三个 P 沟道金属氧化物半导体场效应晶体管 (MOSFET)，它们的工作输入电压范围为 2.5V 到 12V。TPS22933 能够自动选择电平最高的输入 (从 BAT、USB 和 DC_IN 三者中选择) 并将其提供给 LDO。LOUT 是 LDO 始终开启的输出。通过使能功能 (EN 引脚)，可以对 VOUT 进行开关控制，接通快速放电电阻，而且能够直接连接低电压控制信号。

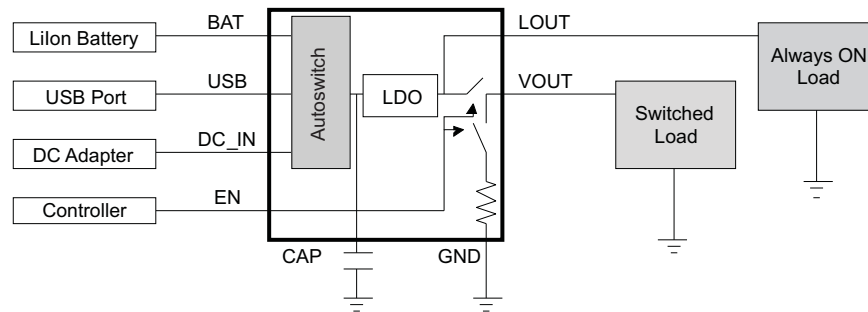
TPS22933 采用小型、节省空间的 8 引脚 μ QFN 封装，并可在 -40°C 至 85°C 温度范围内的自然通风条件下额定运行。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TPS22933	UQFN (8)	1.50mm x 1.50mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用图



目录

1	特性	1	8.3	Feature Description.....	11
2	应用范围.....	1	8.4	Device Functional Modes.....	12
3	说明.....	1	9	Application and Implementation	13
4	修订历史记录	2	9.1	Application Information.....	13
5	Pin Configuration and Functions	3	9.2	Typical Application	13
6	Specifications.....	3	10	Power Supply Recommendations	15
6.1	Absolute Maximum Ratings	3	11	Layout.....	15
6.2	ESD Ratings.....	4	11.1	Layout Guidelines	15
6.3	Recommended Operating Conditions.....	4	11.2	Layout Example	16
6.4	Thermal Information	4	12	器件和文档支持	17
6.5	Electrical Characteristics.....	5	12.1	社区资源.....	17
6.6	Typical Characteristics.....	6	12.2	商标.....	17
7	Parametric Measurement Information	10	12.3	静电放电警告.....	17
8	Detailed Description	11	12.4	Glossary	17
8.1	Overview	11	13	机械、封装和可订购信息.....	17
8.2	Functional Block Diagram	11			

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (October 2011) to Revision A

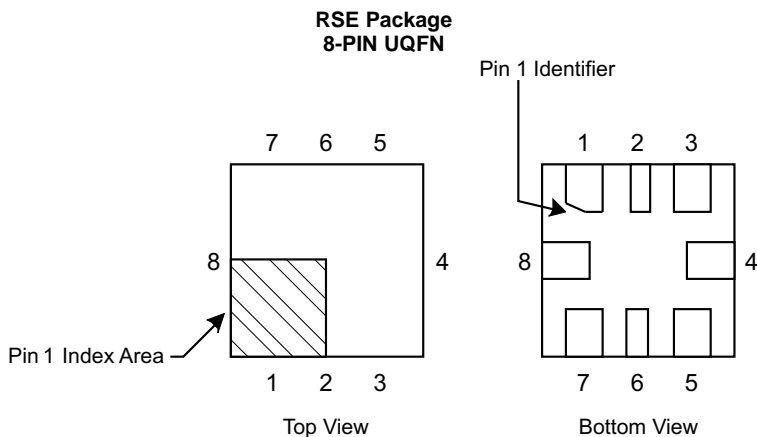
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- 已添加 引脚配置和功能部分，ESD 额定值表，特性说明部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分

1

S

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	BAT	I	Source Voltage 1 (Battery)
2	USB	I	Source Voltage 2 (V+ USB)
3	DC_IN	I	Source Voltage 3 (DC Adapter)
4	GND	—	Ground
5	EN	I	VOUT Enable (Cannot be left floating)
6	CAP	O	Capacitor for LDO
7	VOUT	O	Switched LDO Output
8	LOUT	O	Always on LDO Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{IN}	Input voltage	BAT, USB, DC_IN	−0.3	14	V
V _{OUTPUT}	Output voltage	VOUT, LOUT	−0.3	6	V
V _{EN}	Input voltage	EN	−0.3	6	V
I _{MAX}	Maximum continuous switch current			75	mA
I _{PULSE}	Maximum pulsed switch current, pulse <300 μs, 2% duty cycle			100	mA
T _A	Operating free-air temperature		−40	85	°C
T _{lead}	Maximum lead temperature (10-s soldering time)			300	°C
T _{stg}	Storage temperature		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	BAT, USB, DC_IN	2.5		12	V
V_{EN}		EN	0		5.5	V
V_{IH}	EN pin High-level input voltage, (EN > V_{IH} Min, VOUT = LDO Output)	BAT = 2.5 V to 5.5 V, USB, DC_IN = 2.5 V to 12 V	1.15		5.5	V
V_{IL}	EN pin Low-level input voltage, (EN < V_{IL} Max, VOUT = pulldown)	BAT = 2.5 V to 5.5 V, USB, DC_IN = 2.5 V to 12 V	0		0.6	V
$I_{OUT-LOUT}$	LOUT Current	$V_{BAT} = 4.2$ V OR $V_{USB} = 5$ V OR $V_{DC_IN} = 5$ V, EN = 3.4 V, $I_{OUT-VOUT} = 0$ mA			50	mA
$I_{OUT-VOUT}$	VOUT Current	$V_{BAT} = 4.2$ V OR $V_{USB} = 5$ V OR $V_{DC_IN} = 5$ V, EN = 3.4 V, $I_{OUT-LOUT} = 0$ mA			50	mA
$I_{OUT-TOTAL}$	LOUT + VOUT current	$V_{BAT} = 4.2$ V OR $V_{USB} = 5$ V OR $V_{DC_IN} = 5$ V, EN = 3.4 V			50	mA
CAP	LDO Capacitor (on CAP pin)		20 ⁽¹⁾			nF
	LOUT Capacitor				1	μF
	VOUT Capacitor				1	μF

- (1) Refer to [Application and Implementation](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS22933	UNIT
		RSE (UQFN)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

BAT = 2.5 V to 12.0 V, USB = 2.5 V to 12.0 V, DC_IN = 2.5 V to 12.0 V, T_A = –40°C to +85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS ^{(1) (2) (3)}	T _A	MIN	TYP ⁽⁴⁾	MAX	UNIT
I _{IN-BAT}	Operating current	I _{OUT} = 0 mA, V _{BAT} = 4.2 V, V _{USB} = 3 V, V _{DC_IN} = 3 V, EN = 3.4 V	Full		9.2	15	μA
	Quiescent current	I _{OUT} = 0, V _{BAT} = 4.2 V, V _{USB} = 5 V, V _{DC_IN} = 3 V, EN = 3.4 V			0.7	2	
I _{IN-USB}	Operating current	I _{OUT} = 0 mA, V _{BAT} = 4.2 V, V _{USB} = 5 V, V _{DC_IN} = 3 V, EN = 3.4 V	Full		9.2	15	μA
	Quiescent current	I _{OUT} = 0, V _{BAT} = 4.2V, V _{USB} = 5V, V _{DC_IN} = 5.5V, EN = 3.4 V			0.7	2	
I _{IN-DC_IN}	Operating current	I _{OUT} = 0 mA, V _{BAT} = 4.2 V, V _{USB} = 3 V, V _{DC_IN} = 5 V, EN = 3.4 V	Full		9.2	15	μA
	Quiescent current	I _{OUT} = 0, V _{BAT} = 4.2V, V _{USB} = 5.5V, V _{DC_IN} = 5V, EN = 3.4 V			0.7	2	
I _{IN-USB}	Hi-Voltage operating current	I _{OUT} = 0 mA, V _{BAT} = 4.2 V, V _{USB} = 12 V, V _{DC_IN} = 5 V, EN = 3.4 V	Full		10.8	20	μA
I _{IN-DC_IN}	Hi-Voltage operating current	I _{OUT} = 0 mA, V _{BAT} = 4.2 V, V _{USB} = 5 V, V _{DC_IN} = 12 V, EN = 3.4 V	Full		10.8	20	μA
R _{ON}	ON resistance (USB to CAP, BAT to CAP, DC_IN to CAP)	V _{IN} = 5.0 V, I _{OUT} = 10 mA	25°C		2.4	3.3	Ω
			Full			3.5	
		V _{IN} = 4.2 V, I _{OUT} = 10 mA	25°C		2.6	3.5	Ω
			Full			4	
V _{IN} = 2.5 V, I _{OUT} = 10 mA	25°C		3.8	5	Ω		
	Full			6			
R _{ONVOUT}	ON resistance (LDO output to VOUT)	V _{IN} = 4.2 V, I _{OUT-VOUT} = 10 mA	25°C		1.3	2.5	Ω
			Full			3	
R _{PD}	Output pulldown resistance	V _{IN} = 4.2 V, V _{EN} = 0 V, I(into VOUT) = 10 mA	25°C		63.8	120	Ω
I _{EN}	EN input leakage	V _{EN} = 1.6 V to 5.5 V or GND	Full			1	μA
V _{DO-VOUT}	Dropout voltage VOUT ^{(5) (6)}	I _{OUT} = 10 mA	Full		0.11		V
V _{DO-LOUT}	Dropout voltage LOUT	I _{OUT} = 10 mA ^{(5) (6)}	Full		0.1		V
V _{LOUT}	Always on LDO output voltage (LOUT pin)	V _{IN} < 3.4 V, I _{OUT} = 10 mA, V _{EN} = 1.8 V	Full		V _{IN} – V _{DO-LOUT}		V
		V _{IN} > 4 V, I _{OUT} = 10 mA, V _{EN} = 1.8 V	Full	3.42	3.6	3.78	
V _{VOUT}	Switched LDO output voltage (VOUT pin)	V _{IN} < 3.4 V, I _{OUT} = 10 mA, V _{EN} = 1.8 V	Full		V _{IN} – V _{DO-VOUT}		V
		V _{IN} > 4 V, I _{OUT} = 10 mA, V _{EN} = 1.8 V	Full	3.39	3.57	3.75	
V _{CO}	Changeover voltage	V _{BAT} = 4.2 V, V _{USB} = 4.0 V rising to 4.4 V	Full		0.15		V
t _{CO}	Changeover time	V _{BAT} =4.2 V, V _{USB} = 4.0 V rising to 4.4 V, CAP = 0.01 μF, I _{OUT} = 10 mA	25°C		18		μs
			Full			50	
t _{OFF}	VOUT OFF-time	EN high to low, C(VOUT) = 1 μF, VOUT load = 360 Ω	Full		32		μs
t _{ON}	VOUT ON-time	EN low to high, C(VOUT) = open, VOUT load = 360 Ω	Full		65		μs

(1) V_{IN} is defined as the highest voltage present on the BAT, USB and DC_IN pins.

(2) One of the voltages on BAT, USB and DC_IN must be > V_{IN} (Min), others can be 0 V.

(3) V_{BAT}, V_{USB} and V_{DC_IN} refer to the voltages on BAT, USB and DC_IN respectively. I_{OUT}, I_{OUT-VOUT} and I_{OUT-LOUT} refer to the currents for the combined output current for VOUT and LOUT, the current on VOUT and the current on LOUT respectively.

(4) TYP is 25°C, BAT = 4.2-V, USB = 0-V, DC_IN = 0-V.

(5) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to: V_{IN} – V_{DROPOUT}.

(6) Dropout voltage is measured at the V_{IN} that causes the output to drop to 100mV below its nominal voltage. For VOUT, the voltage drop across the output switch is included (10mA × R_{ONVOUT}).

6.6 Typical Characteristics

Table 1. Performance Graphs and Plots

Type	Description	Figure
Graph	RON versus VIN (BAT, USB, DC_IN) 25°C	Figure 1
Graph	RON versus VIN (Any input)	Figure 2
Graph	Quiescent Current versus Input Voltage (Any input)	Figure 3
Graph	Operating Current versus Input Voltage (Any Input)	Figure 4
Scope Plot	t_{OFF} (VIN = 4.2 V, C(VOUT) = 1 uF, 25°C)	Figure 5
Scope Plot	t_{OFF} (VIN = 4.2 V, C(VOUT) = open, 25°C)	Figure 6
Scope Plot	t_{ON} (VIN = 4.2 V, C(VOUT) = 1 uF, 25°C)	Figure 7
Scope Plot	t_{ON} (VIN = 4.2 V, C(VOUT) = open, 25°C)	Figure 8
Graph	LOUT and VOUT versus Temperature at VIN = 4.2 V	Figure 9
Graph	LOUT and VOUT versus IOU (VIN = 4.2 V, Temp = 25°C)	Figure 10
Graph	LOUT Dropout Voltage versus Temperature (VIN = 2.5 V)	Figure 11
Graph	VOUT Dropout Voltage versus Temperature (VIN = 2.5 V)	Figure 12
Graph	Output Pulldown Resistance (R_{PD}) versus Temperature (10 mA into VOUT)	Figure 13

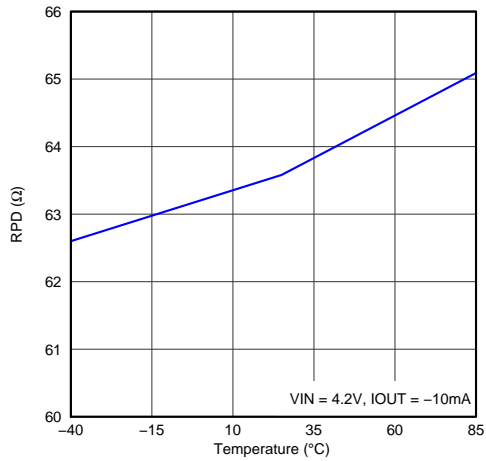


Figure 1. RPD vs Temperature

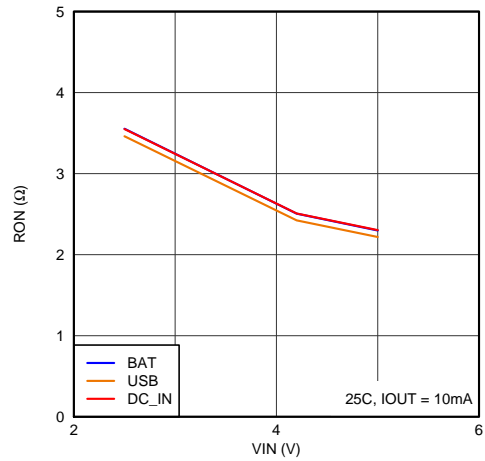


Figure 2. RON vs VIN (Typical)

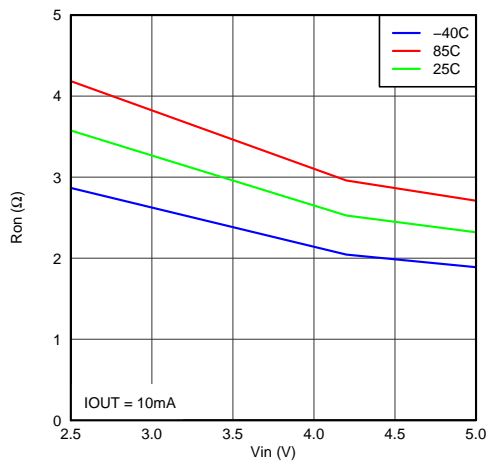


Figure 3. RON vs VIN

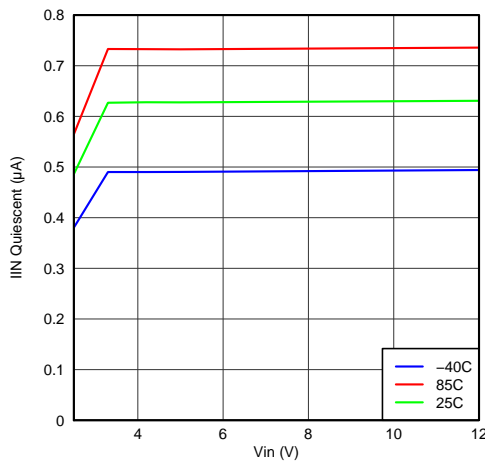


Figure 4. IIN (Quiescent) vs VIN

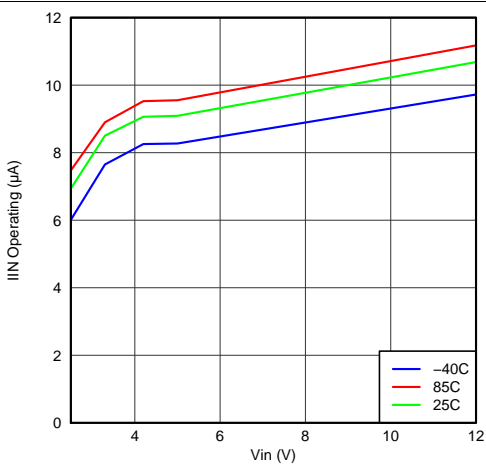


Figure 5. IIN (Operating) vs VIN

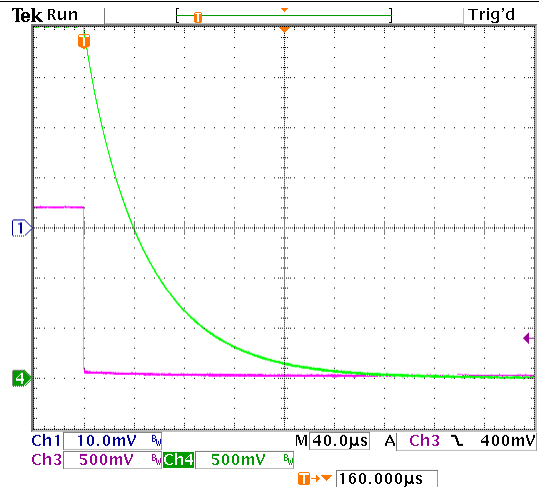


Figure 6. VOUT toff (1 μF on VOUT)

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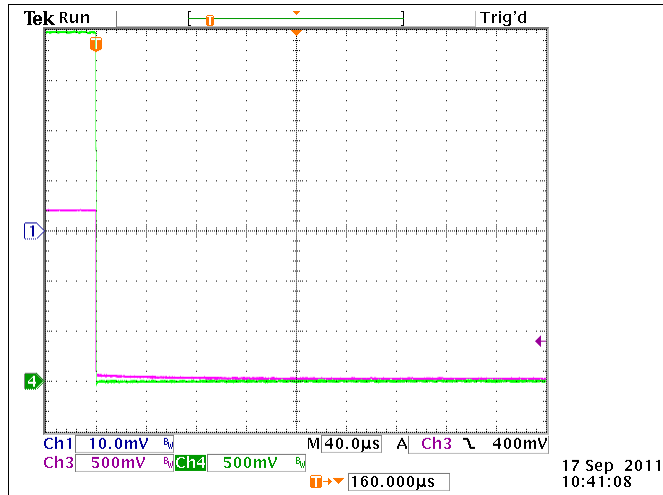


Figure 7. VOUT t_{OFF} (No Capacitor on VOUT)

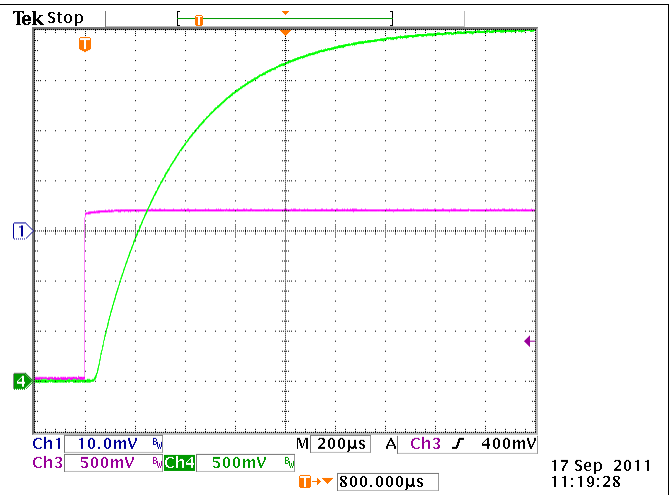


Figure 8. VOUT t_{ON} (1 μ F on VOUT)

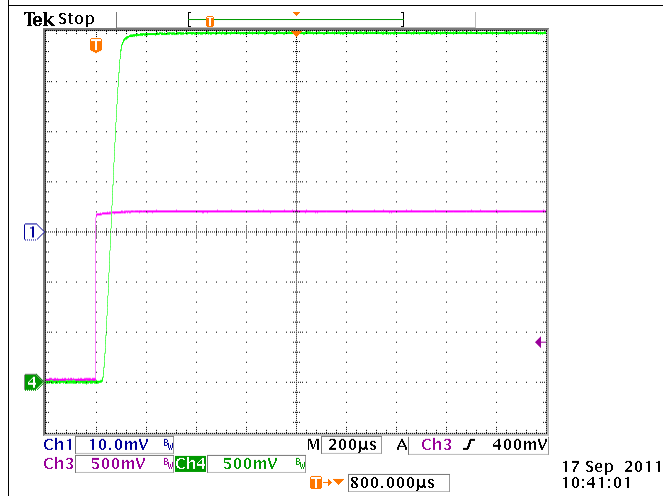


Figure 9. VOUT t_{ON} (No Capacitor on VOUT)

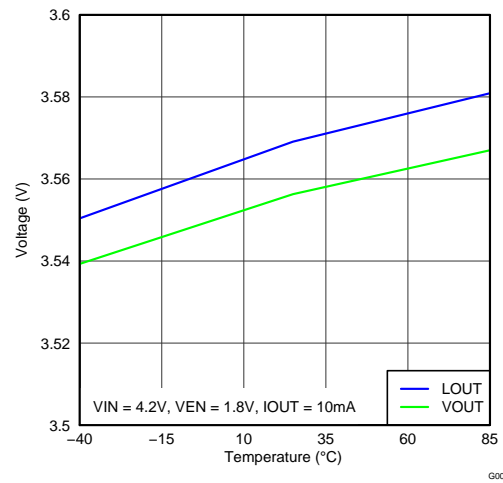


Figure 10. LOU-VOUT vs Temperature VIN 4.2 V

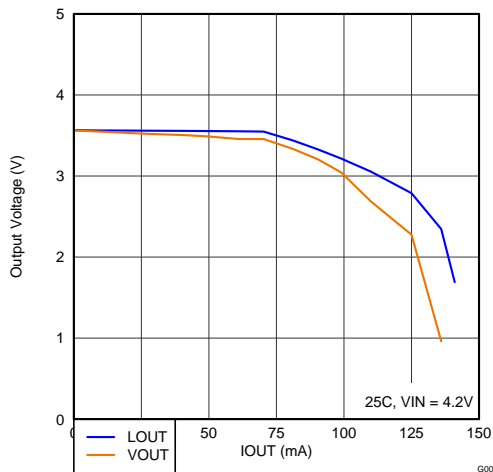


Figure 11. LOU-VOUT vs IOU

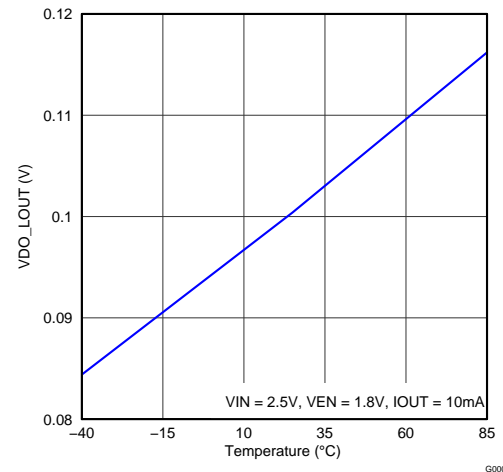


Figure 12. VDOLOU vs Temperature VIN 2.5 V

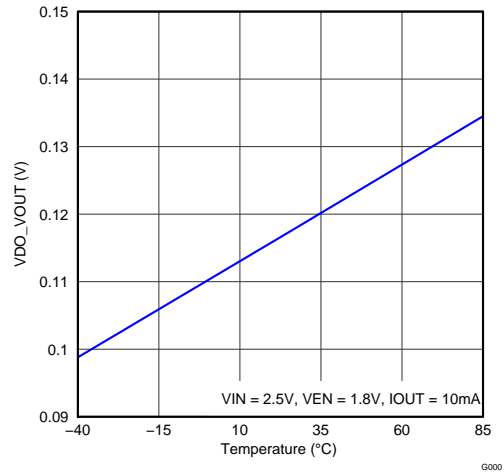


Figure 13. VDOVOUT vs Temperature VIN 2.5 V

7 Parametric Measurement Information

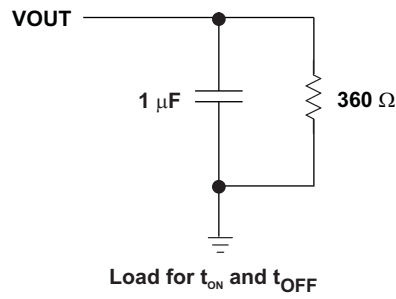


Figure 14. Test Circuit and t_{ON} / t_{OFF} Waveforms

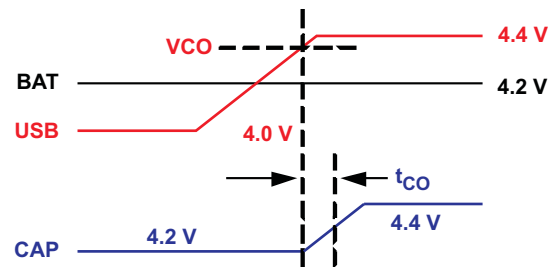


Figure 15. Switchover Timing

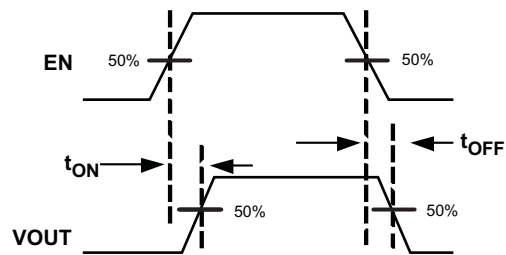


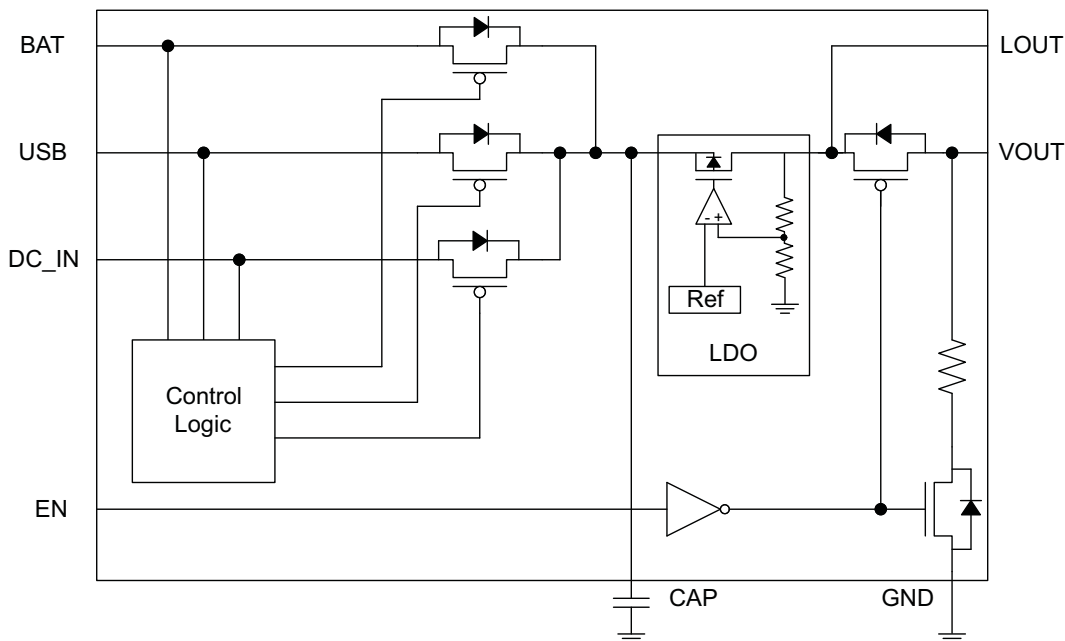
Figure 16. VOUT Enable Timing

8 Detailed Description

8.1 Overview

The TPS22933 is a triple-input power multiplexer with auto-input selection and a low dropout linear regulator. The device contains three P-channel MOSFETs that can operate over an input voltage range of 2.5 V to 12 V. The TPS22933 automatically selects the highest voltage level (from BAT, USB, and DC_IN) and enables that input to source the LDO. LOUT is an always-on output from the LDO, but VOUT can be switched on and off using the EN pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 ON and OFF Control

The EN pin controls the state of the VOUT switch and VOUT pulldown switch. EN has no control over LOUT. Asserting EN enables the VOUT switch and disables the Quick Output Discharge (QOD) switch. Deasserting EN disables the VOUT switch and enables the QOD switch. EN is active high and has a low threshold, making it capable of interfacing with low voltage signals. The EN pin is compatible with standard GPIO Logic threshold and can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs.

8.3.2 Power Changeover

The TPS22933 LDO is powered by the highest level input. When input voltages change, the TPS22933 may change which input powers the LDO. During initial power up, the input that reaches the highest value first will power the LDO. Once that decision is made, changing between input sources is based on VCO. When an input source becomes VCO over the input currently supplying power to the LDO, changeover will occur and the new, higher input will power the LDO.

8.4 Device Functional Modes

Table 2 and Table 3 show the behavior of the device with various voltage conditions for the inputs and enable pin.

Table 2. Function Table

EN	LDO TO LOUT	LDO TO VOUT	VOUT TO GND
L	ON	OFF	ON
H	ON	ON	OFF

Table 3. Input Selection Table (V1 > V2 > V3)

BAT	USB	DC_IN	LDO SUPPLY
V1	V2 or V3	V2 or V3	BAT
V2 or V3	V1	V2 or V3	USB
V2 or V3	V2 or V3	V1	DC_IN
V1	V1	V1	See ⁽¹⁾

(1) Whichever source achieves the highest level the fastest will supply the LDO.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 LDO Capacitor (for CAP Pin)

An optional capacitor on the CAP pin helps stabilize the integrated LDO. Take care in capacitor sizing to reduce inrush currents. The voltage on the CAP pin will follow the highest input. Since the max input voltage is 12 V, the capacitor voltage rating must be higher than 12 V.

9.1.2 Using the CAP Pin as a Power Output

Figure 17 shows three power inputs multiplexed to source only through the CAP pin. In this case, the LDO outputs are not used (EN is tied low). The highest of the inputs is chosen to drive the voltage at the CAP pin.

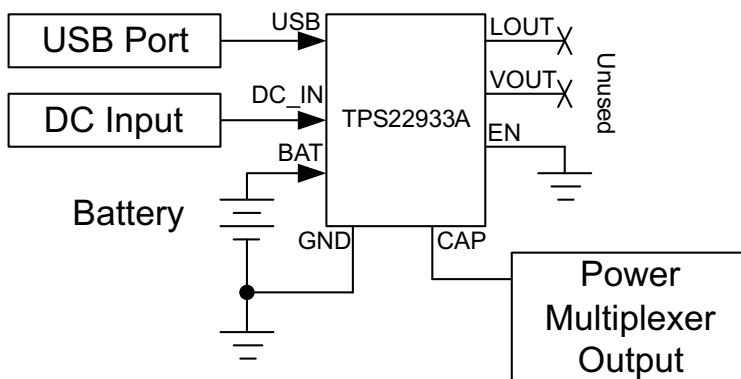


Figure 17. Using the CAP Pin as a Multiplexer Output

9.2 Typical Application

Figure 18 shows three power inputs multiplexed to source the LDO. The LDO always on output (LOUT) is tied to an MSP430. The MSP430 then determines when to enable the switched output (VOUT) by driving the EN pin.

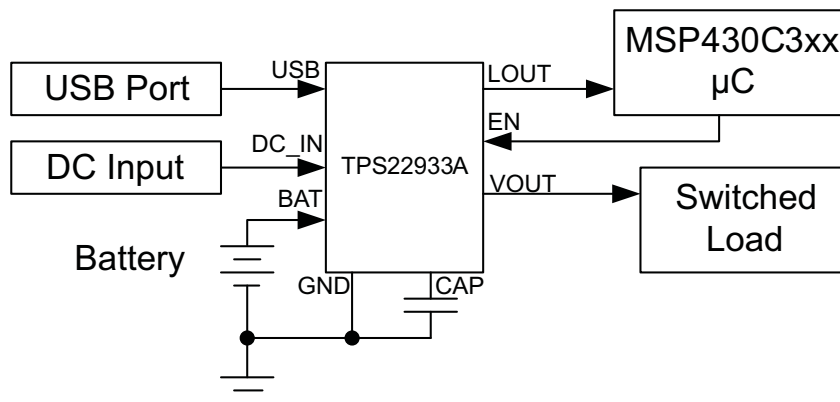


Figure 18. Application Example

Typical Application (continued)

9.2.1 Design Requirements

Table 4 lists the design parameters for TPS22933.

Table 4. Design Parameters

INPUT	VOLTAGE
USB Port	5.0V
DC Input	5.0V
Battery	4.2V

9.2.2 Detailed Design Procedure

Initial power up:

DC_IN = 0 V; USB = 0 V; EN = 0 V

BAT is applied at 4.2 V

LDO power comes from BAT

LOUT = 3.6 V; CAP = 4.2 V; VOUT = 0 V

USB power is connected at 5 V, BAT remains 4.2 V and DC_IN remains 0 V

LDO power is changed from BAT to USB in t_{CO}

LOUT = 3.6 V; CAP = 5 V; VOUT = 0 V

DC_IN power is connected at 5.0 V, BAT remains 4.2 V and USB remains 5 V

No change in LDO power

LOUT = 3.6 V; CAP = 5 V; VOUT = 0 V

EN = VIH, BAT remains 4.2 V, USB remains 5 V and DC_IN remains 5 V

LOUT = 3.6 V, CAP = 5 V; VOUT = 3.6 V

USB power is removed, BAT remains 4.2 V and DC_IN remains 5 V

LDO power is changed from USB to DC_IN

LOUT = 3.6 V; CAP = 5 V; VOUT = 3.6 V

DC_IN power is removed, BAT remains 4.2 V and USB remains 0 V:

LDO power is changed from DC_IN to BAT

LOUT = 3.6 V; CAP = 4.2 V; VOUT = 3.6 V

9.2.3 Application Curve

Figure 19 shows the device behavior in the last step of the design procedure, when DC_IN power is removed and the LDO is powered by the battery. The capacitor on the CAP pin discharges as DC_IN is removed but then charges to the battery voltage when the input is automatically switched. LOUT remains a constant 3.6 V throughout this power switching.

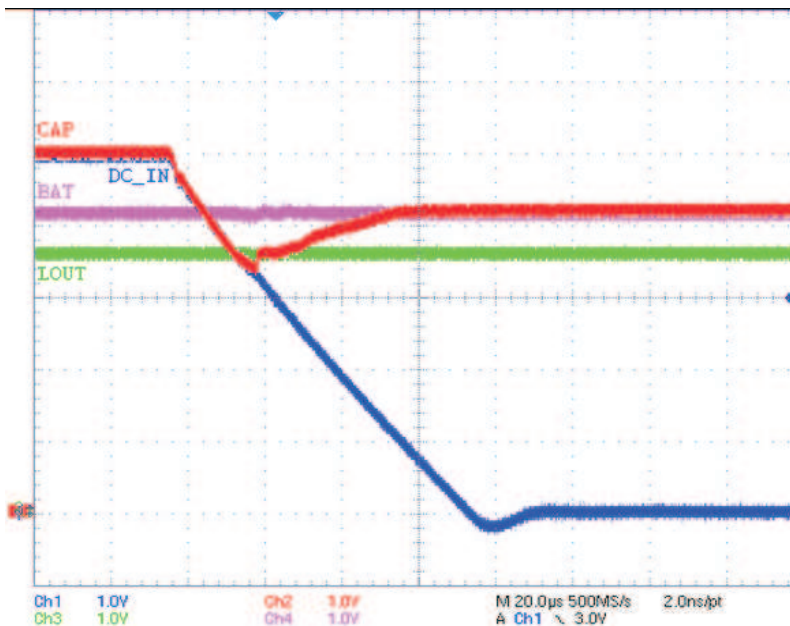


Figure 19. DC_IN Removed, BAT Powers LDO (LOUT = 3.6 V)

10 Power Supply Recommendations

The device is designed to operate with an input voltage range of 2.5 V to 12 V. This supply must be well regulated and placed as close to the device terminals as possible.

11 Layout

11.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for BAT, USB, DC_IN, LOUT, VOUT, and GND will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

11.2 Layout Example

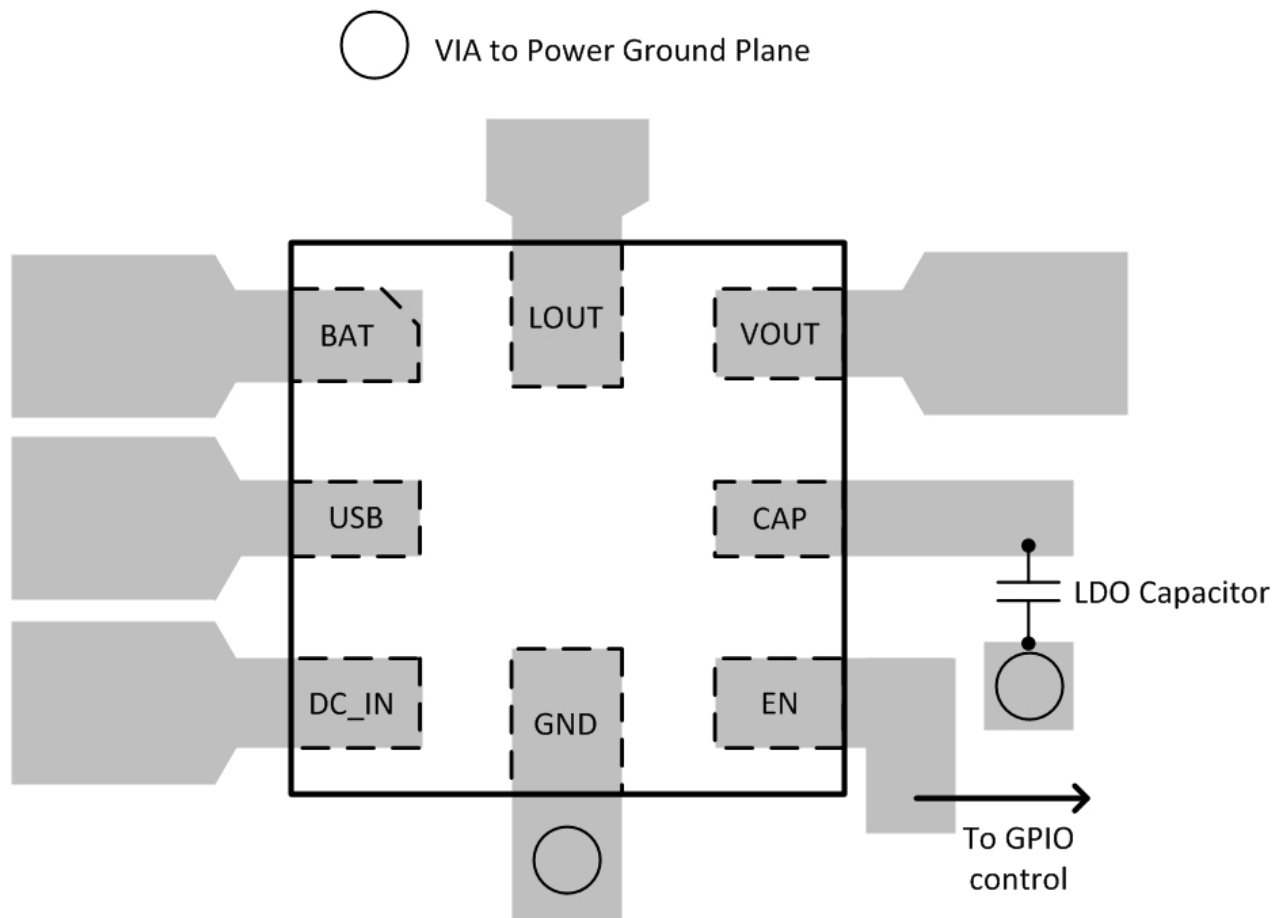


Figure 20. TPS22933 Layout Example

12 器件和文档支持

12.1 社区资源

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12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

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数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22933ARSER	ACTIVE	UQFN	RSE	8	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	4Q	Samples
TPS22933ARSET	ACTIVE	UQFN	RSE	8	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	4Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

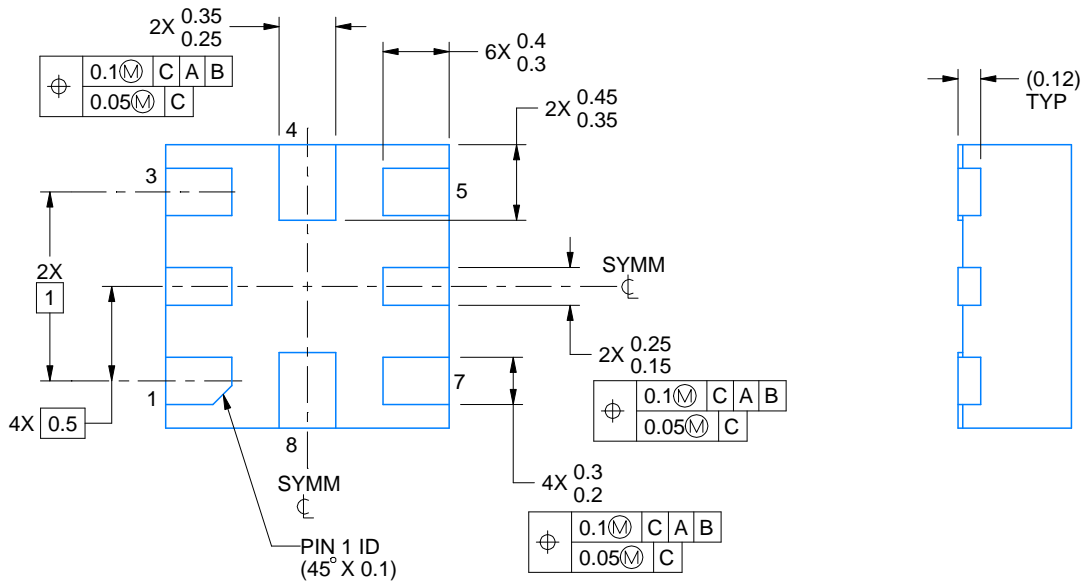
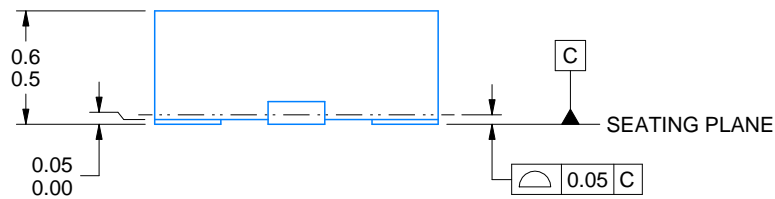
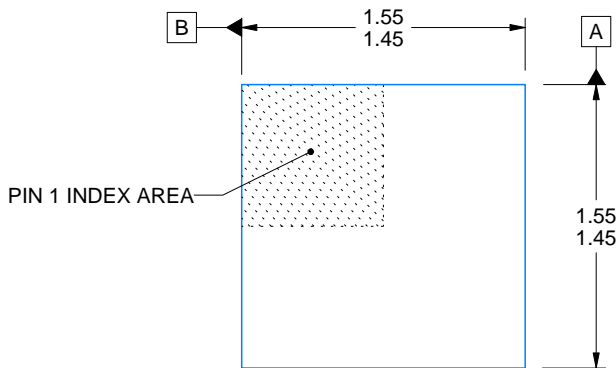
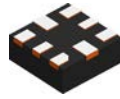

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22933ARSER	UQFN	RSE	8	3000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
TPS22933ARSET	UQFN	RSE	8	250	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22933ARSER	UQFN	RSE	8	3000	202.0	201.0	28.0
TPS22933ARSET	UQFN	RSE	8	250	202.0	201.0	28.0



4220323/B 03/2018

NOTES:

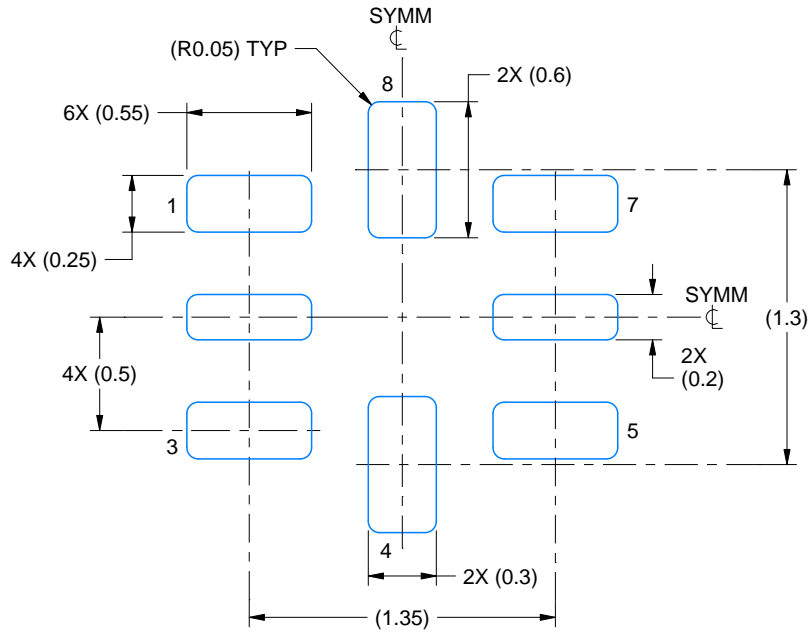
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

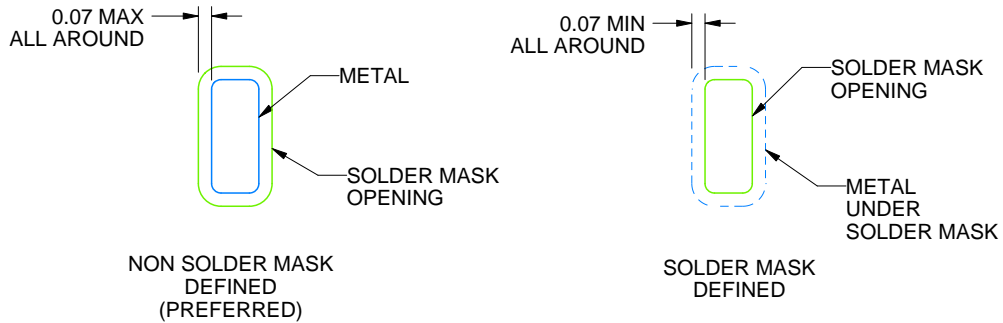
RSE0008A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4220323/B 03/2018

NOTES: (continued)

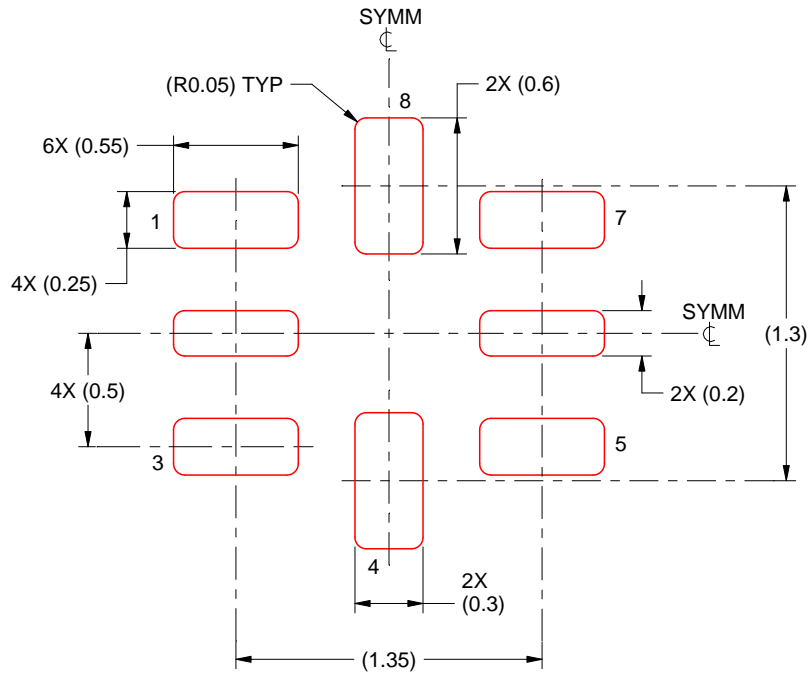
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RSE0008A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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