采用 0402 封装的 TMP64-Q1 ±1% 47kΩ 线性热敏电阻

1 特性

- 具有符合 AEC-Q100 标准的下列特性：
  - 温度等级 1：-40°C ≤ T_A ≤ 125°C
  - HBM ESD 分类等级 H2
  - CDM ESD 分类等级 C6
- 具有正温度系数 (PTC) 的硅基热敏电阻
- 线性电阻随温度变化
- 在 25°C 下具有 47kΩ 标称电阻 (R25)
  - ±1% 最大值（0°C 至 70°C）
- –40°C 至 +125°C 的宽工作温度范围
- 在整个温度范围内具有稳定的灵敏度
  - 6400ppm/°C TCR (25°C)
  - 在整个温度范围内具有 0.2% 的典型 TCR 容差
- 快速热响应时间为 0.6s (DEC)
- 长寿命和稳健性能
  - 内置失效防护，能够在发生短路故障时提供保护
  - 传感器长期温漂典型值为 0.5%

2 应用

- 温度监控
  - HVAC 和恒温器
  - 工业控制和电器
- 热补偿
  - 显示屏背光
  - 楼宇自动化
- 热阈值检测
  - 电机控制
  - 充电器
- 热补偿
  - 显示屏背光
  - 电池管理系统
- 热阈值检测
  - 电机控制
  - 车载充电器和直流/直流转换器

3 说明

立即开始使用热敏电阻设计工具，它提供了完整的电阻与温度关系表（R-T 表）的计算以及用于推导温度和示例 C 代码的有用方法。

线性热敏电阻可在整个温度范围内提供线性度和一致的灵敏度，支持使用简单而准确的方法进行温度转换。低功耗和较小的热质量可最大限度地减小自发热的影响。凭借内置的高温失效防护以及对环境变化的强大抵抗力，这类器件可长时间提供高性能。TMP6 系列器件外型小巧，可靠近热源放置，并具有快速响应时间。

与 NTC 热敏电阻相比，它具有以下优点：无需额外的线性化电路、最大程度减少校准工作量、电阻容差变化更小、高温下灵敏度更高以及可节省处理器时间和内存的简化转换方法。

TMP64 目前采用与 0402 封装外形兼容的 X1SON 封装。

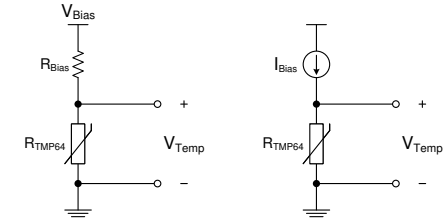
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TMP64-Q1	X1SON	0.60mm × 1.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

ADVANCE INFORMATION

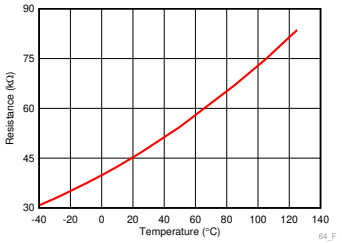
典型实施电路



$$V_{Temp} = \frac{V_{Bias} * R_{TMP64}}{R_{Bias} + R_{TMP64}}$$

$$V_{Temp} = I_{Bias} * R_{TMP64}$$

典型电阻与环境温度间的关系



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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ADVANCE INFORMATION

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

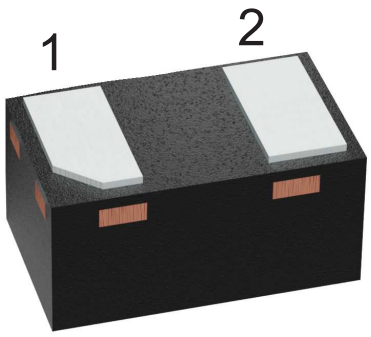
Changes from Revision Original (December 2019) to Revision A — **Page**

- 更新了标题 ... 1
- 更新了 特性 ... 1
- 更新了 应用 ... 1
- 更新了 说明） ... 1
- Increased ESD CDM Rating from ±750 V to ± 1000 V ... 4
- Changed minimum 'Long Term Drift' spec for RH = 85 % from 0.1 % to -1 % ... 5
- Added typical. 'Long Term Drift' spec for RH = 85 % ... 5
- Changed maximum 'Long Term Drift' spec for RH = 85 % from 0.8 % to 1 % ... 5
- Changed minimum 'Long Term Drift' spec from 0.1 % to -1% ... 5
- Added typical. 'Long Term Drift' spec ... 5
- Changed maximum 'Long Term Drift' spec from 1 % to 1.8 % ... 5
- Added 'Supply Dependence Resistance vs. Bias Current' graph ... 6
- Added 'Supply Dependence Resistance vs. Bias Voltage' graph ... 6
- Added 'Step Response' graph ... 6
- Added 'Thermal Response time' graphs ... 6
- Updated Thermistor Design Tool link ... 9

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5 Pin Configuration and Functions

DEC Package
2-Pin X1SON
Top View (Angled)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
–	1	—	Thermistor (–) and (+) terminals. For proper operation, ensure a positive bias where the + terminal is at a higher voltage potential than the – terminal.
+	2		

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Voltage across pins 2 (+) and 1 (–)		+6	V
Current through the device		+450	µA
Junction temperature (T_J)	–65	+150	°C
Storage temperature (T_{stg})	–65	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) per JESD22-A114 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{Sns}	Voltage across pins 2 (+) and 1 (–)	0		5.5	V
I_{Sns}	Current passing through the device	0		400	µA
T_A	Operating free-air temperature (specified performance) (X1SON/DEC Package)	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TMP64 DEC (X1SON) 2 PINS	Units
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)(3)	443.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	195.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	254.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	254.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bot) thermal resistance	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction to ambient thermal resistance ($R\theta_{JA}$) under natural convection is obtained in a simulation on a JEDEC-standard, High-K board as specified in JESD51-7, in an environment described in JESD51-2. Exposed pad packages assume that thermal vias are included in the PCB, per JESD 51-5.
(3) Changes in output due to self heating can be computed by multiplying the internal dissipation by the thermal resistance.

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6.5 Electrical Characteristics

T_A = -40 °C - 125 °C, I_{Sns} = 42.553 µA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{25}	Thermistor Resistance at 25 °C	T_A = 25 °C	46.53	47	47.47	kΩ
R_{TOL}	Resistance Tolerance	T_A = 25 °C	–1		1	%
		T_A = 0 °C - 70 °C	–1		1	
		T_A = -40 °C - 125 °C	–1.5		1.5	
TCR_{-35}	Temperature Coefficient of Resistance	T1 = -40 °C, T2 = -30 °C		+6220		ppm/°C
TCR_{25}		T1 = 20 °C, T2 = 30 °C		+6400		
TCR_{85}		T1 = 80 °C, T2 = 90 °C		+5910		
TCR_{-35} %	Temperature Coefficient of Resistance Tolerance	T1 = -40 °C, T2 = -30 °C		±0.4		%
TCR_{25} %		T1 = 20 °C, T2 = 30 °C		±0.2		
TCR_{85} %		T1 = 80 °C, T2 = 90 °C		±0.3		
ΔR	Sensor Long Term Drift (Reliability)	96 hours continuous operation at RH = 85% and T_A = 130 °C V_{Bias} = 5.5 V	-1	±0.1	1	%
		600 hours continuous operation at T_A = 150 °C V_{Bias} = 5.5V	-1	0.5	1.8	
$t_{RES\ (stirred\ liquid)}$	Thermal response to 63%	T1 = 25 °C in Still Air to T2 = 125 °C in Stirred Liquid		0.6		s
$t_{RES\ (still\ air)}$	Thermal response to 63%	T1 = 25 °C to T2 = 70 °C in Still Air		3.2		s

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6.6 Typical Characteristics

at T_A = 25 °C, (unless otherwise noted)

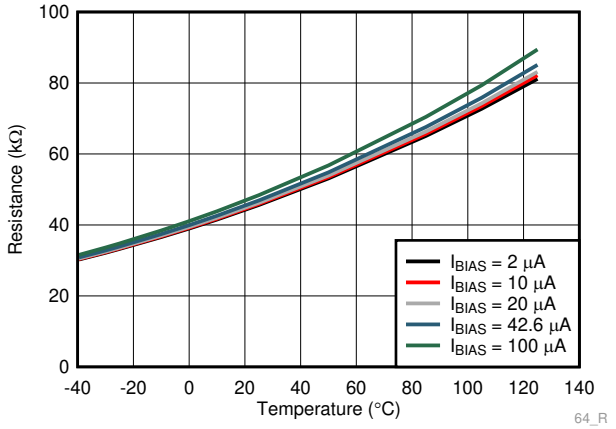
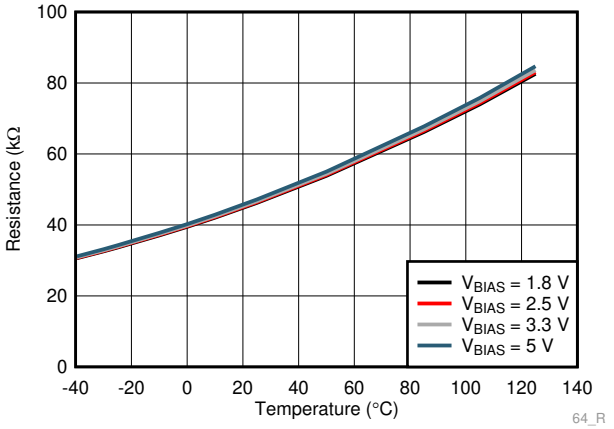


图 1. Resistance vs. Ambient Temperature Using Multiple Bias Currents



R_{Bias} = 47 kΩ with ±0.01 % Tolerance

图 2. Resistance vs. Ambient Temperature Using Multiple Bias Voltages

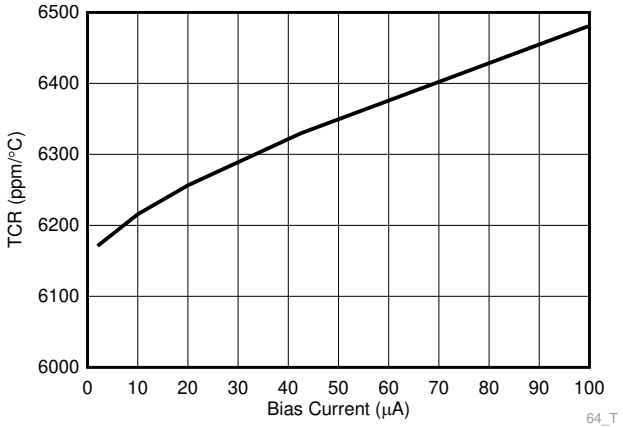
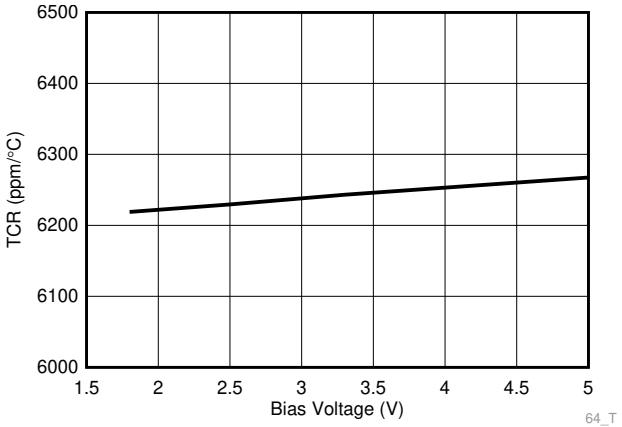


图 3. TCR as a Function of Sense Current, I_{SNS}



R_{Bias} = 47 kΩ with ±0.01% Tolerance

图 4. TCR as a Function of Sense Voltage, V_{SNS}

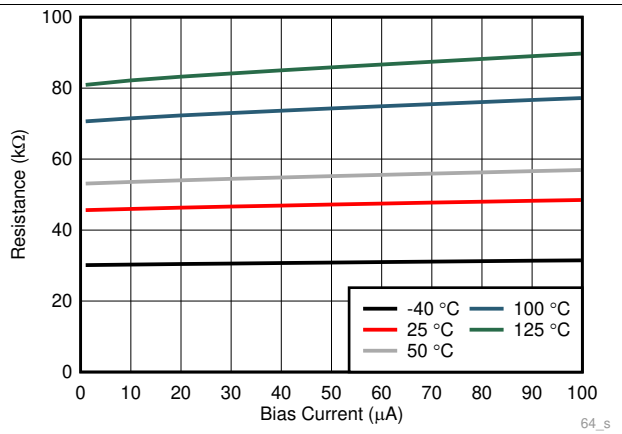
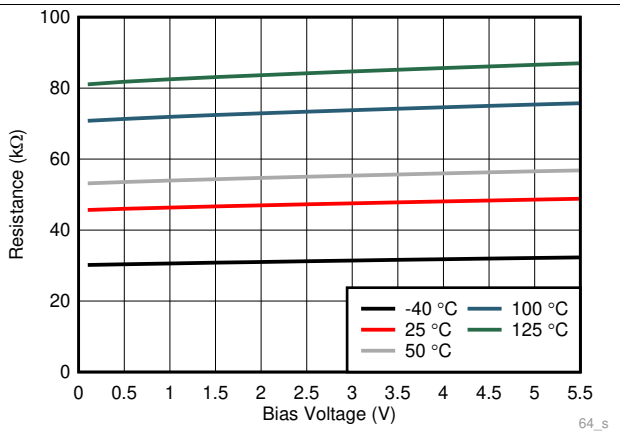


图 5. Supply Dependence Resistance vs. Bias Current



R_{Bias} = 47 kΩ with ±0.01% Tolerance

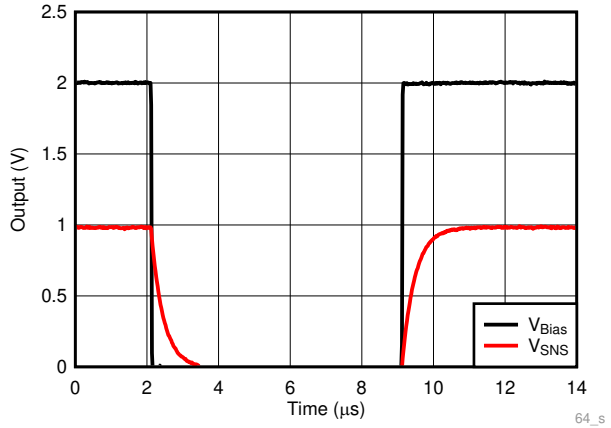
图 6. Supply Dependence R vs. V_{Bias}

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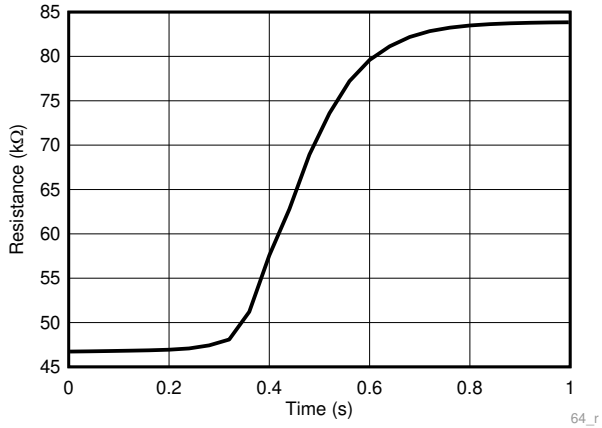
Typical Characteristics (接下页)

at T_A = 25 °C, (unless otherwise noted)



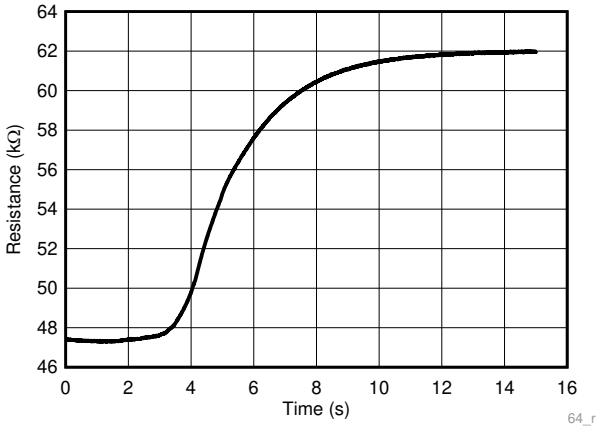
TMP64: V_{SNS} = 1 V

图 7. Step Response



TMP64: Stirred Liquid

图 8. Thermal Response Time



TMP64: Still Air

图 9. Thermal Response Time

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The TMP64 silicon linear thermistor has a linear positive temperature coefficient (PTC) that results in a uniform and consistent temperature coefficient resistance (TCR) across a wide operating temperature range. TI uses a special silicon process where the the doping level and active region areas devices control the key characteristics (the temperature coefficient resistance (TCR) and nominal resistance (R25)) . The device has an active area and a substrate due to the polarized terminals. Connect the positive terminal to the highest voltage potential. Connect the negative terminal to the lowest voltage potential.

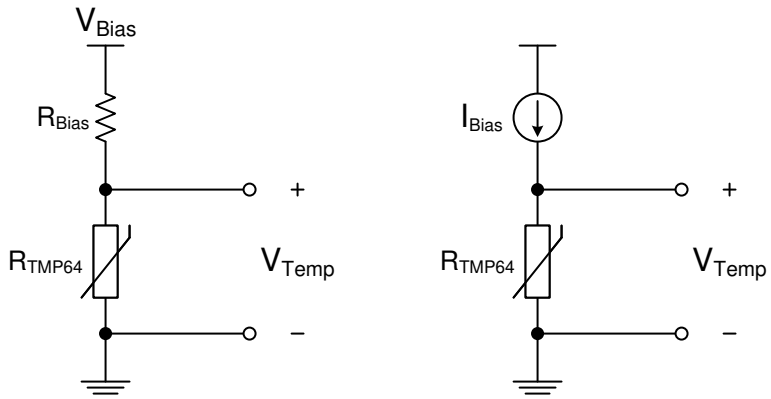
Unlike an NTC, which is a purely resistive device, the TMP64 resistance is affected by the current across the device and the resistance changes when the temperature changes. In a voltage divider circuit, it is recommended to maintain the top resistor value at 47 kΩ. Changing the top resistor value or the V_{BIAS} value changes the resistance vs temperature table (R-T table) of the TMP64, and subsequently the polynomials as described in *Design Requirements*. Consult the *TMP64 R-T table* section for more information.

$$TCR\ (ppm/°C) = (R_{T2} – R_{T1}) / ((T_2 – T_1) \times R_{(T2+T1)/2}) \quad (1)$$

Below are the definitions of the key terms used throughout this document:

- I_{SNS}: Current flowing through the TMP64.
- V_{SNS}: Voltage across the two TMP64 terminals.
- I_{Bias}: Current supplied by the biasing circuit.
- V_{Bias}: Voltage supplied by the biasing circuit.
- V_{Temp}: Output voltage that corresponds to the measured temperature. Note that this is different from V_{Sns}. In the use case of a voltage divider circuit with the TMP64 in the high side, V_{Temp} is taken across R_{Bias}.

7.2 Functional Block Diagram



$$V_{Temp} = \frac{V_{Bias} * R_{TMP64}}{R_{Bias} + R_{TMP64}} \qquad V_{Temp} = I_{Bias} * R_{TMP64}$$

图 10. Typical Implementation Circuits

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7.3 TMP64 R-T table

The TMP64 R-T table must be re-calculated for any change in the bias voltage, bias resistor, or bias current. TI provides a Thermistor Design Tool to calculate the R-T table. The system designer should always validate the calculations provided.

7.4 Feature Description

7.4.1 Linear resistance curve

The TMP64 has good linear behavior across the whole temperature range as shown in 图 1. This range allows a simpler resistance-to-temperature conversion method that reduces look-up table memory requirements. The linearization circuitry or midpoint calibration associated with traditional NTCs is not necessary with the device.

The linear resistance across the entire temperature range allows the device to maintain sensitivity at higher operating temperatures.

7.4.2 Positive Temperature Coefficient (PTC)

The TMP64 has a positive temperature coefficient. As temperature increases the device resistance increases leading to a reduction in power consumption of the bias circuit. In comparison, a negative coefficient system increases power consumption with temperature as the resistance decreases.

The TMP64 benefits from the reduced power consumption of the bias circuit with less self-heating than a typical NTC system.

7.5 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP64 is a positive temperature coefficient (PTC) linear silicon thermistor. The device behaves like a temperature-dependent resistor, and may be configured in a variety of ways to monitor temperature based on the system-level requirements. The TMP64 has a nominal resistance at 25 °C (R25) of 47 kΩ, a maximum operating voltage of 5.5 V (V_{Sns}), and maximum supply current of 400 µA (I_{Sns}). This device may be used in a variety of applications to monitor temperature close to a heat source with the very small DEC package option compatible with the typical 0402 (inch) footprint. Some of the factors that influence the total measurement error include the ADC resolution (if applicable), the tolerance of the bias current or voltage, the tolerance of the bias resistance in the case of a voltage divider configuration, and the location of the sensor with respect to the heat source.

8.2 Typical Application

8.2.1 Thermistor Biasing Circuits

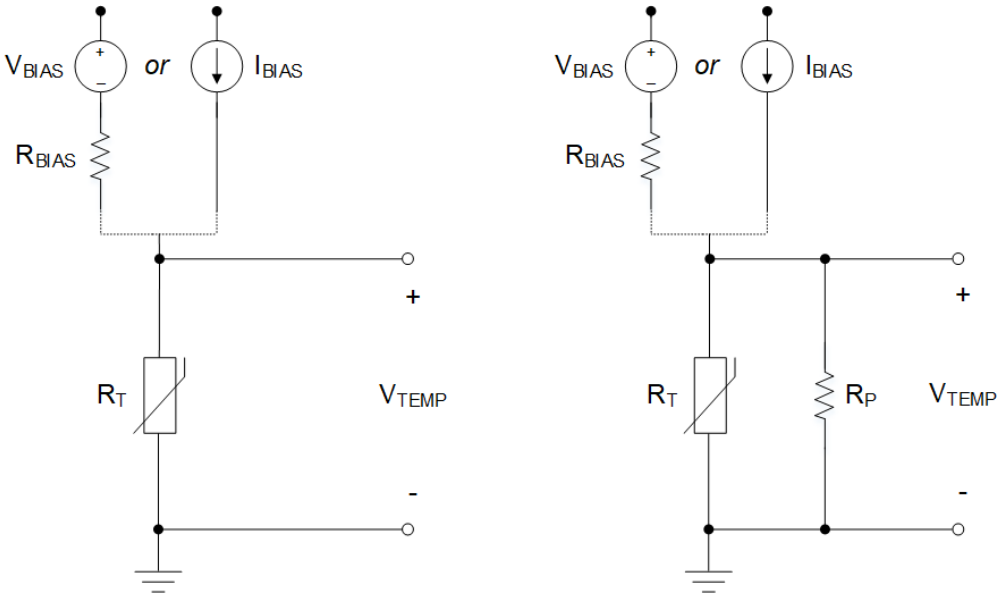


Figure 11. Biasing Circuit Implementations With Linear Thermistor (Left) vs. Non-Linear Thermistor (Right)

8.2.1.1 Design Requirements

Existing thermistors, in general, have a non-linear temperature vs. resistance curve. To linearize the thermistor response, the engineer can use a voltage linearization circuit with a voltage divider configuration, or a resistance linearization circuit by adding another resistance in parallel with the thermistor, R_P. The *Thermistor Biasing Circuits* section highlights the two implementations where R_T is the thermistor resistance. To generate an output voltage across the thermistor, the engineer can use a voltage divider circuit with the thermistor placed at either the high side (close to supply) or low side (close to ground), depending on the desired voltage response (negative or positive). Alternatively, the thermistor can be biased directly using a precision current source

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Typical Application (continued)

(yielding the highest accuracy and voltage gain). It is common to use a voltage divider with thermistors because of its simple implementation and lower cost. The TMP64, on the other hand, has a linear positive temperature coefficient (PTC) of resistance such that the voltage measured across it increases linearly with temperature. As such, the need for a linearization circuits is no longer a requirement, and a simple current source or a voltage divider circuit can be used to generate the temperature voltage.

This output voltage can be interpreted using a comparator against a voltage reference to trigger a temperature trip point that is either tied directly to an ADC to monitor temperature across a wider range or used as feedback input for an active feedback control circuit.

The voltage across the TMP64, as described in Equation 2, can be translated to temperature using either a lookup table method (LUT) or a fitting polynomial, V(T). The Thermistor Design Tool must be used to translate Vtemp to Temperature. The temperature voltage must first be digitized using an ADC. The necessary resolution of this ADC is dependent on the biasing method used. Additionally, for best accuracy, the bias voltage (V_{BIAS}) should be tied to the reference voltage of the ADC to create a measurement where the difference in tolerance between the bias voltage and the reference voltage cancels out. The engineer can also implement a low-pass filter to reject system level noise, and the user should place the filter as close to the ADC input as possible.

8.2.1.2 Detailed Design Procedure

The resistive circuit divider method produces an output voltage (V_{TEMP}) scaled according to the bias voltage (V_{BIAS}). When V_{BIAS} is also used as the reference voltage of the ADC, any fluctuations or tolerance error due to the voltage supply is canceled and does not affect the temperature accuracy. This type of configuration is shown in Figure 12. Equation 2 describes the output voltage (V_{TEMP}) based on the variable resistance of the TMP64 (R_{TMP64}) and bias resistor (R_{BIAS}). The ADC code that corresponds to that output voltage, ADC full-scale range, and ADC resolution is given in Equation 3.

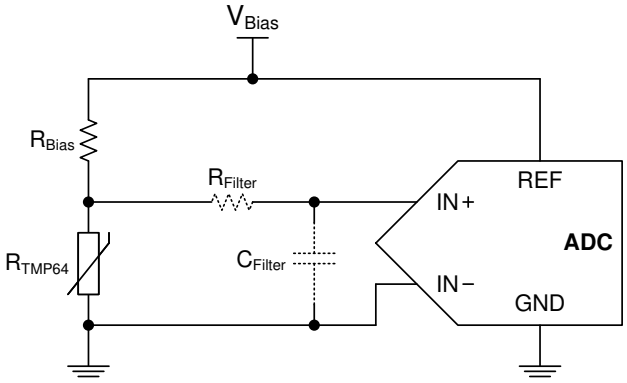


Figure 12. TMP64 Voltage Divider With an ADC

$$V_{TEMP} = V_{BIAS} \times \left(\frac{R_{TMP64}}{R_{BIAS} + R_{TMP64}} \right) \quad (2)$$

$$\text{ADC Code} = \left(\frac{V_{TEMP}}{FSR} \right) \times 2^n \quad (3)$$

where

- FSR is the full-scale range of the ADC, which is the voltage at REF to GND (V_{REF})
- n is the resolution of the ADC

Equation 4 shows whenever $V_{REF} = V_{BIAS}$, V_{BIAS} cancels out.

$$\text{ADC Code} = \left(\frac{V_{BIAS} \times \left(\frac{R_{TMP64}}{R_{BIAS} + R_{TMP64}} \right)}{V_{BIAS}} \right) \times 2^n = \left(\frac{R_{TMP64}}{R_{BIAS} + R_{TMP64}} \right) \times 2^n \quad (4)$$

ADVANCE INFORMATION

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Typical Application (continued)

The engineer can use a polynomial equation or a LUT to extract the temperature reading based on the ADC code read in the microcontroller. The Thermistor Design Tool should be used to translate the TMP64 resistance to temperature.

The cancellation of V_{BIAS} is one benefit to using a voltage-divider (ratiometric approach), but the sensitivity of the output voltage of the divider circuit cannot increase much. Therefore, not all of the ADC codes are used due to the small voltage output range compared to the FSR. This application is very common, however, and is simple to implement.

The engineer can use a current source-based circuit, like the one shown in Figure 13, to have better control over the sensitivity of the output voltage and achieve higher accuracy. In this case, the output voltage is simply V = I × R. For example, if a current source of 100 µA is used with the TMP64, the output voltage spans approximately 5.5 V and has a gain up to 40 mV/°C. Having control over the voltage range and sensitivity allows for full utilization of the ADC codes and full-scale range. Similar to the ratiometric approach above, if the ADC has a built-in current source that shares the same bias as the reference voltage of the ADC, the tolerance of the supply current cancels out. In this case, a precision ADC is not required. This method yields the best accuracy, but can increase the system implementation cost.

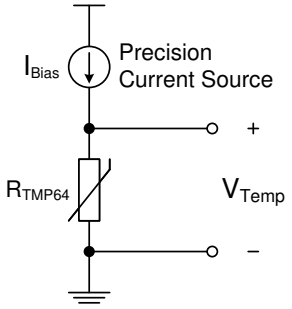


Figure 13. TMP64 Biasing Circuit With Current Source

In comparison to the non-linear NTC thermistor in a voltage divider, the TMP64 has an enhanced linear output characteristic. The two voltage divider circuits with and without a linearization parallel resistor, R_P, are shown in Figure 14. Consider an example where V_{BIAS} = 5 V, R_{BIAS} = 47 kΩ, and a parallel resistor (R_P) is used with the NTC thermistor (R_{NTC}) to linearize the output voltage with an additional 47-kΩ resistor. The TMP64 produces a linear curve across the entire temperature range while the NTC curve is only linear across a small temperature region. When the parallel resistor (R_P) is added to the NTC circuit, the added resistor makes the curve much more linear but greatly affects the output voltage range.

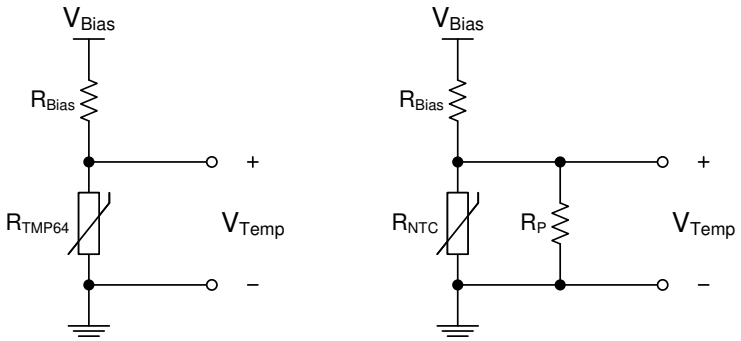


Figure 14. TMP64 vs. NTC With Linearization Resistor (R_P) Voltage Divider Circuits

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Typical Application (continued)

8.2.1.2.1 Thermal Protection With Comparator

The engineer can use the TMP64, a voltage reference, and a comparator to program the thermal protection. As shown in Figure 15, the output of the comparator remains low until the voltage of the thermistor divider, with R_{BIAS} and R_{TMP64}, rises above the threshold voltage set by R_1 and R_2. When the output goes high, the comparator signals an overtemperature warning signal. The engineer can also program the hysteresis to prevent the output from continuously toggling around the temperature threshold when the output returns low. Either a comparator with built-in hysteresis or feedback resistors may be used.

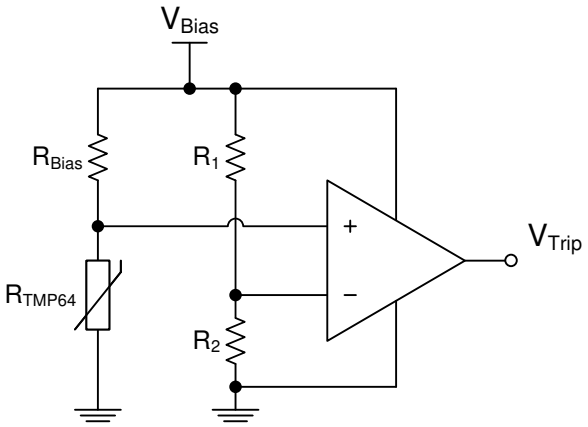


Figure 15. Temperature Switch Using TMP64 Voltage Divider and a Comparator

8.2.1.2.2 Thermal Foldback

One application that uses the output voltage of the TMP64 in an active control circuit is thermal foldback. This is performed to reduce, or fold back, the current driving a string of LEDs, for example. At high temperatures, the LEDs begin to heat up due to environmental conditions and self heating. Thus, at a certain temperature threshold based on the LED's safe operating area, the driving current must be reduced to cool down the LEDs and prevent thermal runaway. The TMP64 voltage output increases with temperature when the output is in the lower position of the voltage divider and can provide a response used to fold back the current. Typically, the current is held at a specified level until a high temperature is reached, known as the knee point, where the current must be rapidly reduced. To better control the temperature/voltage sensitivity of the TMP64, a rail-to-rail operational amplifier is used. In the example shown in Figure 16, the temperature “knee” where the foldback begins is set by the reference voltage (2.5 V) at the positive input, and the feedback resistors set the response of the foldback curve. The foldback knee point may be chosen based on the output of the voltage divider and the corresponding temperature from Equation 5 (like 110 °C, for example). A buffer is used in-between the voltage divider with R_{TMP64} and the input to the op amp to prevent loading and variations in V_{TEMP}.

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Typical Application (continued)

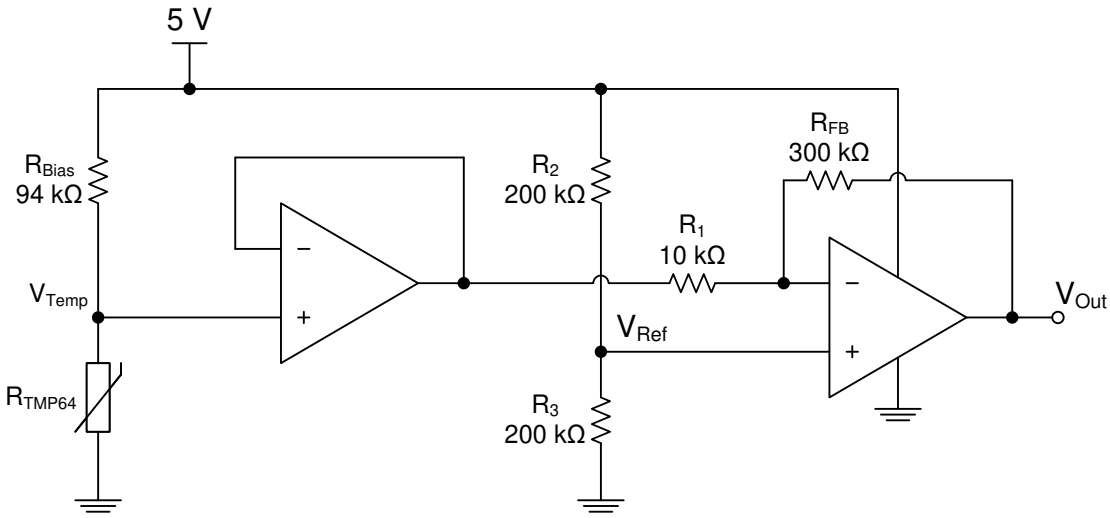


Figure 16. Thermal Foldback Using TMP64 Voltage Divider and a Rail-to-Rail Op Amp

The op amp remains high as long as the voltage output is below V_{Ref}. When the temperature goes above 110 °C, then the output swings low to the 0-V rail of the op amp. The rate at which the foldback occurs is dependent on the feedback network, R_{FB} and R_1, which varies the gain of the op amp, G, given by Equation 6. This in return controls the voltage/temperature sensitivity of the circuit. This voltage output is fed into a LED driver IC that adjusts output current accordingly. The final output voltage used for thermal foldback is V_{OUT}, and is given in Equation 7. In this example where the knee point is set at 110 °C, the output voltage curve is as shown in Figure 17.

$$V_{TEMP} = V_{BIAS} \times \left(\frac{R_{TMP64}}{R_{BIAS} + R_{TMP64}} \right) \tag{5}$$

$$G = \frac{R_{FB}}{R_1} \tag{6}$$

$$V_{OUT} = -G \times V_{TEMP} + (1 + G) \times V_{REF} \tag{7}$$

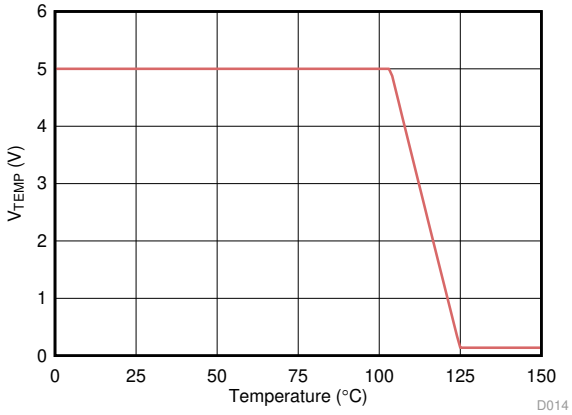


Figure 17. Thermal Foldback Voltage Output Curve

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9 Power Supply Recommendations

The maximum recommended operating voltage of the TMP64 is 5.5 V (V_{Sns}), and the maximum current through the device is 400 µA (I_{Sns}).

10 Layout

10.1 Layout Guidelines

The layout of the TMP64 is similar to that of a passive component. If the device is biased with a current source, the positive pin 2 is connected to the source, while the negative pin 1 is connected to ground. If the circuit is biased with a voltage source, and the device is placed on the lower side of the resistor divider, V– is connected to ground, and V+ is connected to the output (V_{TEMP}). If the device is placed on the upper side of the divider, V+ is connected to the voltage source and V– is connected to the output voltage (V_{TEMP}). Figure 18 shows the device layout.

10.2 Layout Example

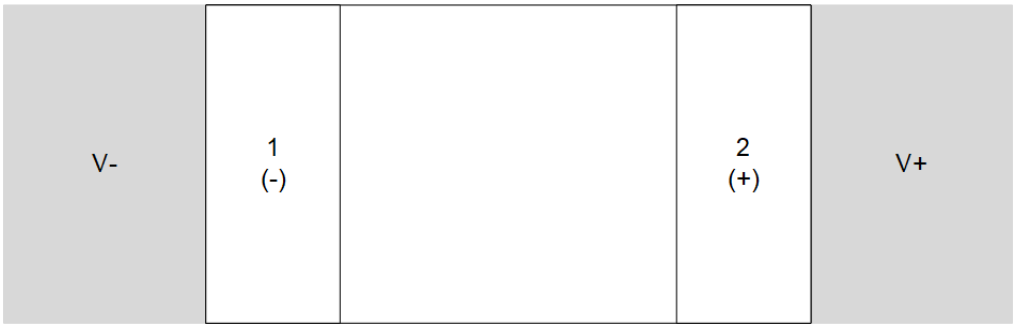


Figure 18. Recommended Layout: DEC Package

ADVANCE INFORMATION

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

ADVANCE INFORMATION

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP6431QDECRQ1	ACTIVE	X1SON	DEC	2	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HJ	Samples
TMP6431QDECTQ1	ACTIVE	X1SON	DEC	2	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HJ	Samples
TMP6431QDYARQ1	ACTIVE	SOT-5X3	DYA	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	1HH	Samples
TMP6431QDYATQ1	ACTIVE	SOT-5X3	DYA	2	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	1HH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

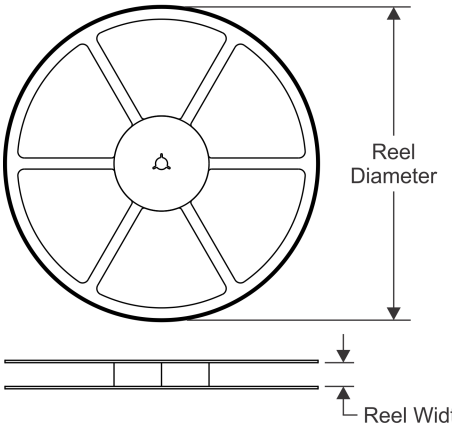
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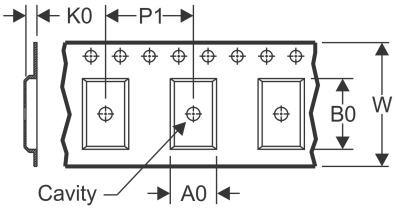
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

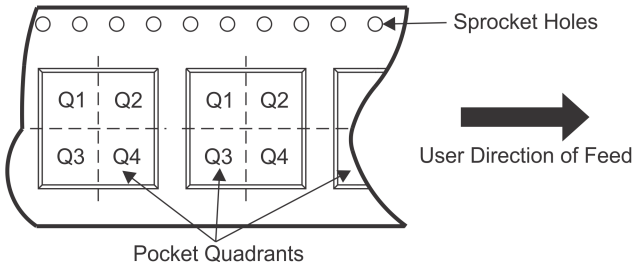


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

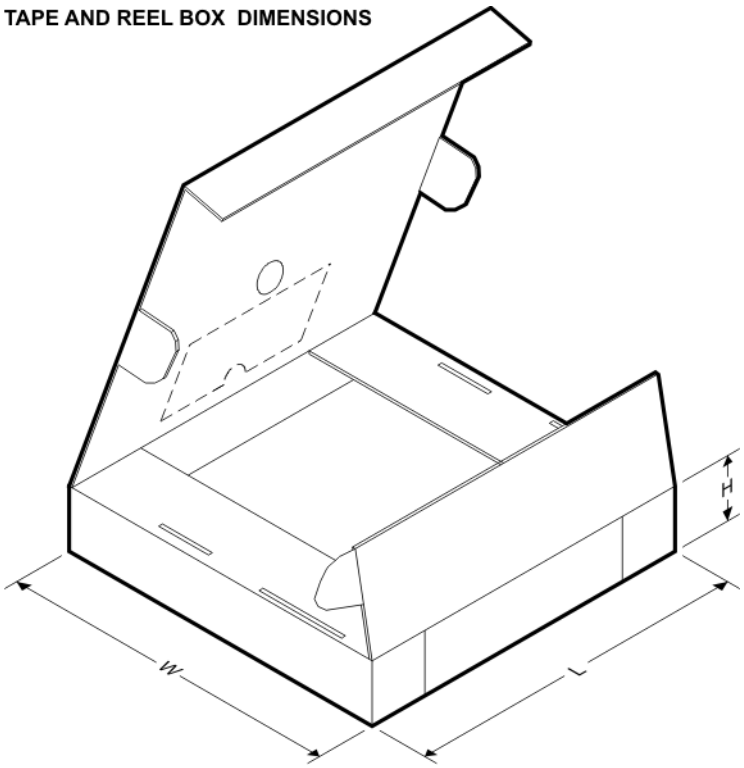
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP6431QDECRQ1	X1SON	DEC	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
TMP6431QDECTQ1	X1SON	DEC	2	250	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
TMP6431QDYARQ1	SOT-5X3	DYA	2	3000	178.0	9.5	0.5	1.94	0.73	4.0	8.0	Q1
TMP6431QDYATQ1	SOT-5X3	DYA	2	250	178.0	9.5	0.5	1.94	0.73	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

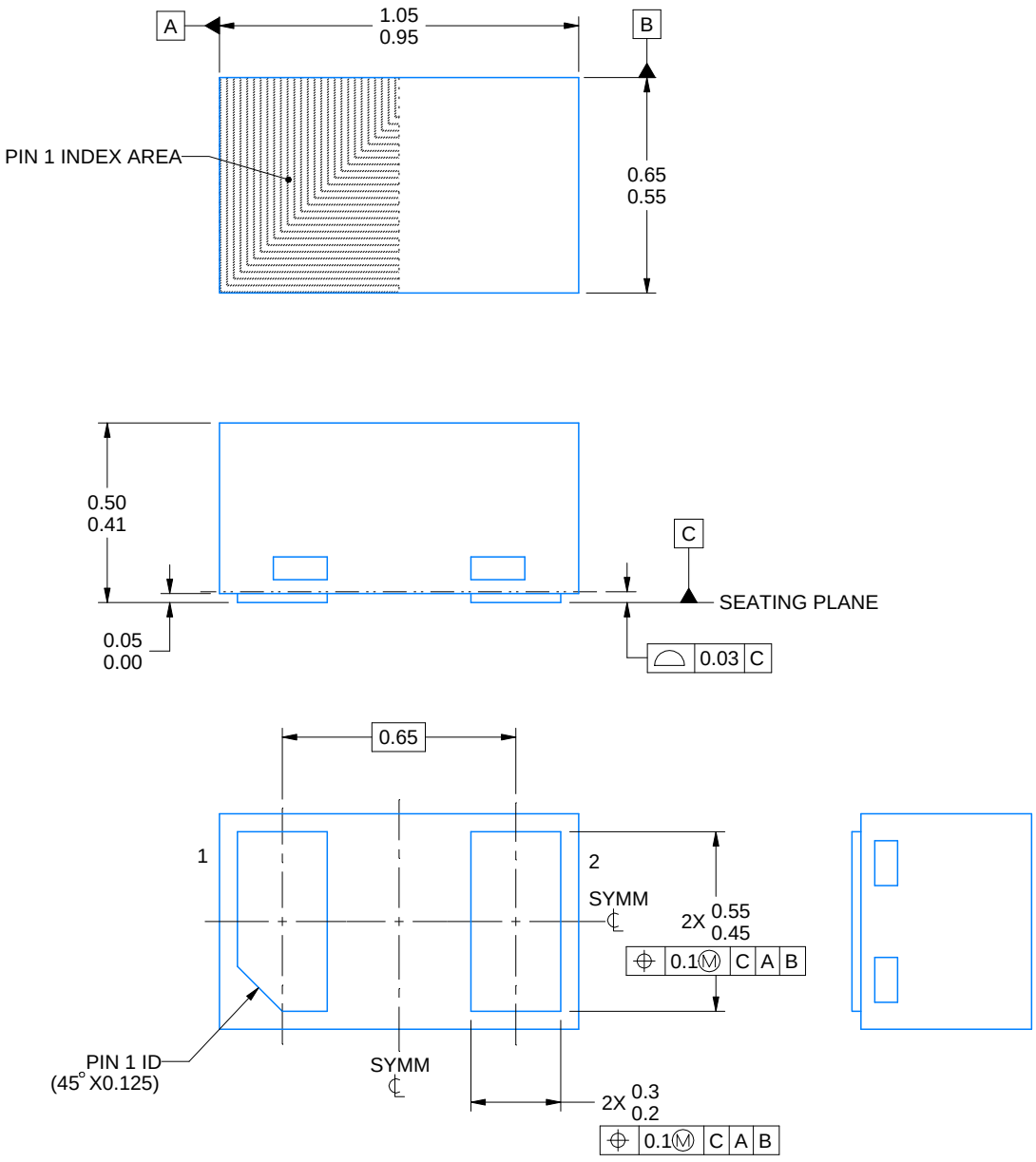
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP6431QDECRQ1	X1SON	DEC	2	10000	205.0	200.0	33.0
TMP6431QDECTQ1	X1SON	DEC	2	250	205.0	200.0	33.0
TMP6431QDYARQ1	SOT-5X3	DYA	2	3000	210.0	200.0	42.0
TMP6431QDYATQ1	SOT-5X3	DYA	2	250	210.0	200.0	42.0

PACKAGE OUTLINE

DEC0002A

X1SON - 0.5 mm max height

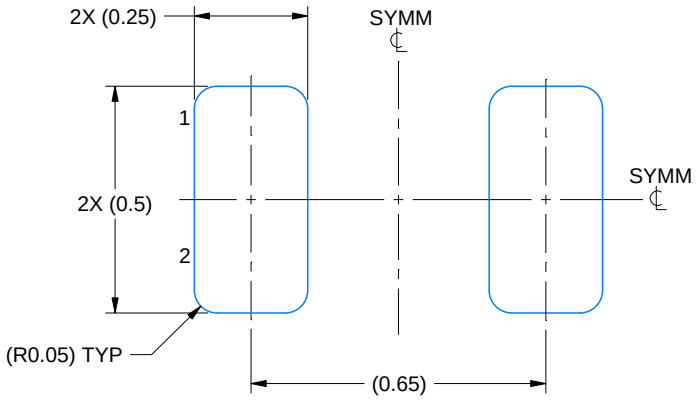
PLASTIC SMALL OUTLINE - NO LEAD



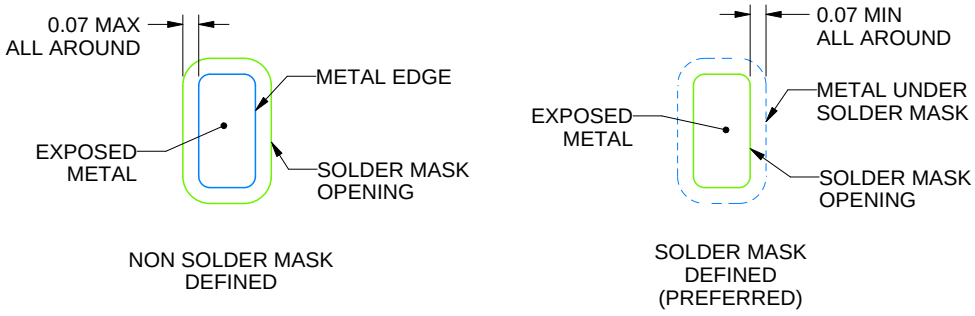
4224506/A 08/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

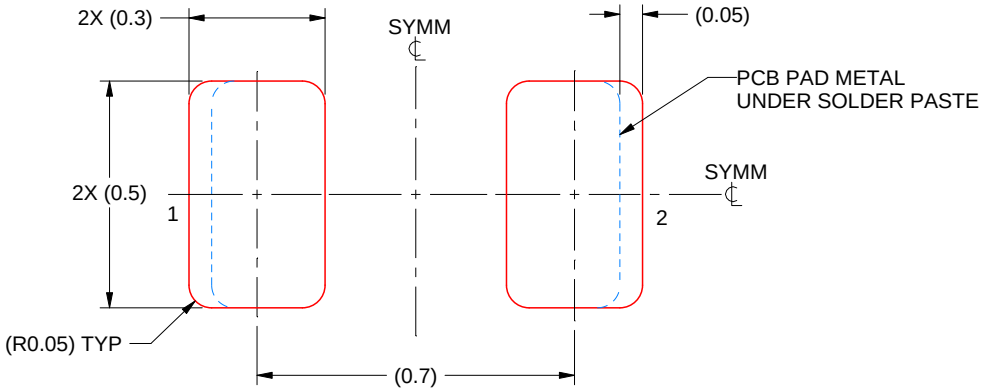


SOLDER MASK DETAILS

4224506/A 08/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224506/A 08/2018

NOTES: (continued)

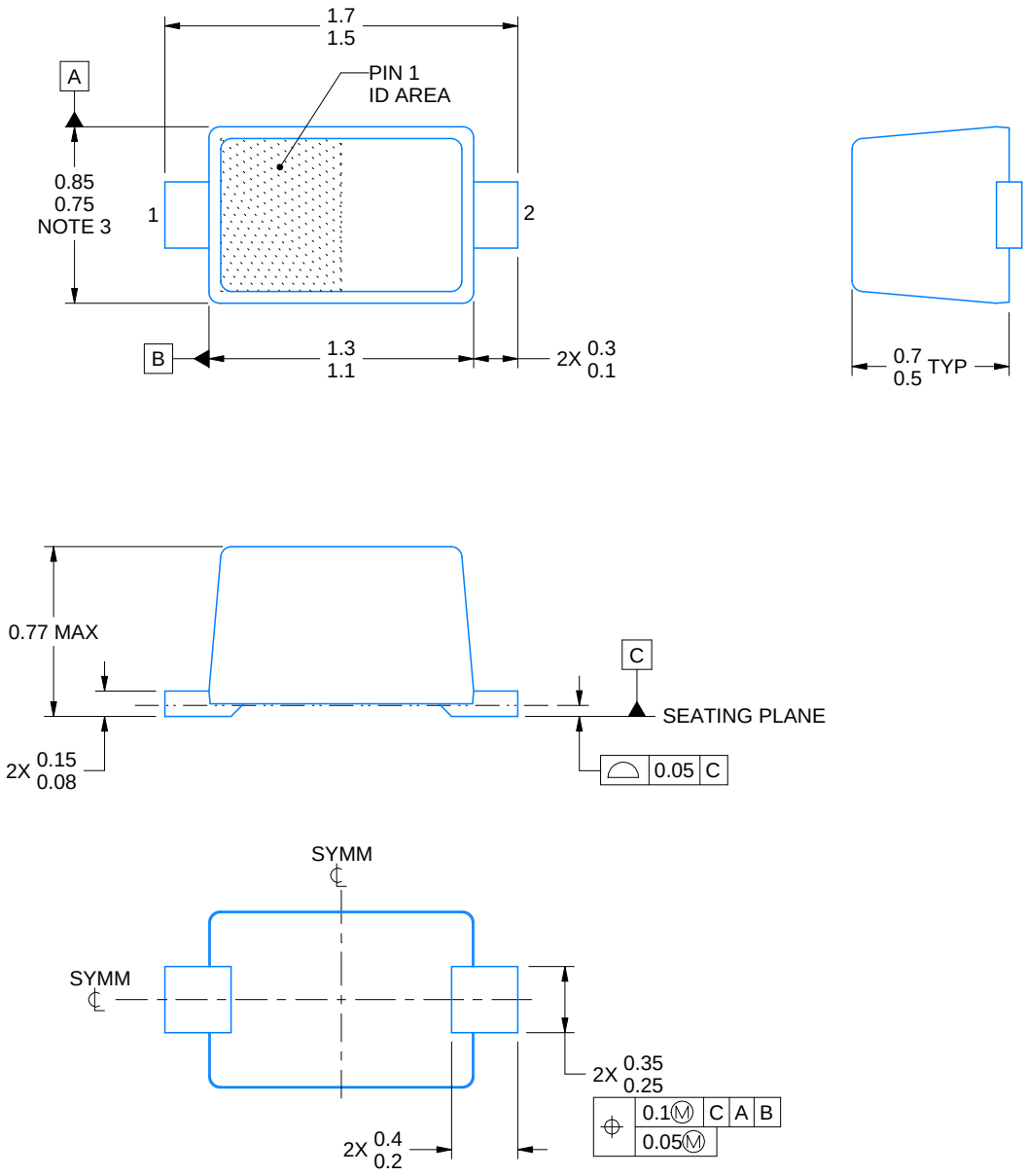
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYA0002A

SOT (SOD-523) - 0.77 mm max height

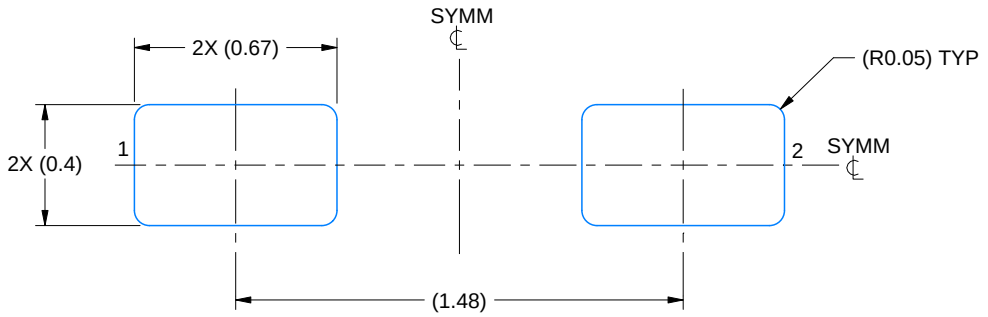
PLASTIC SMALL OUTLINE



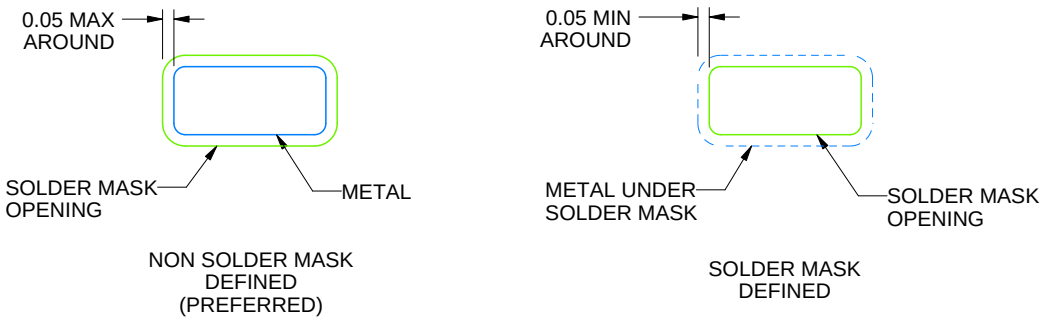
4224978/B 09/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEITA SC-79 registration except for package height



LAND PATTERN EXAMPLE
SCALE:40X



SOLDERMASK DETAILS

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NOTES: (continued)

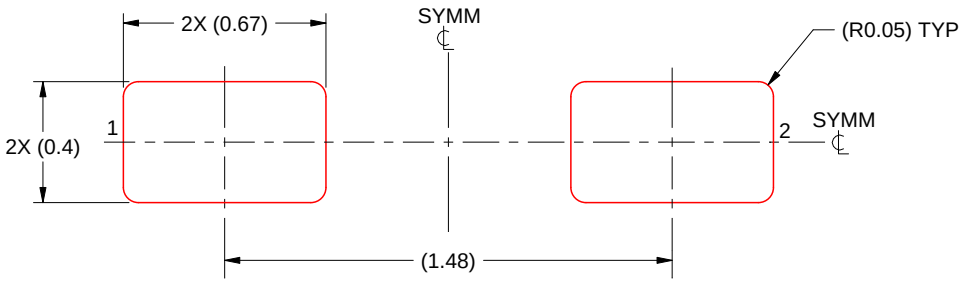
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4224978/B 09/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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