LP2985 150-mA, Low-Noise, Low-Dropout Regulator With Shutdown

1 Features

- Output tolerance of:
  - 1% (A grade)
  - 1.5% (standard grade)
- Ultra-low dropout, typically:
  - 280 mV at full load of 150 mA
  - 7 mV at 1 mA
- Wide V_{IN} range: 16 V max
- Low I_Q: 850 µA at full load at 150 mA
- Shutdown current: 0.01 µA typ
- Low noise: 30 μV_{RMS} with 10-nF bypass capacitor
- Stable with low-ESR capacitors, including ceramic
- Overcurrent and thermal protection
- High peak-current capability
- ESD protection exceeds JESD 22 :
  - 2000-V human-body model (A114-A)
  - 200-V machine model (A115-A)

2 Applications

- Washer and dryer
- Land mobile radio
- Active antenna system mMIMO
- Cordless power tool

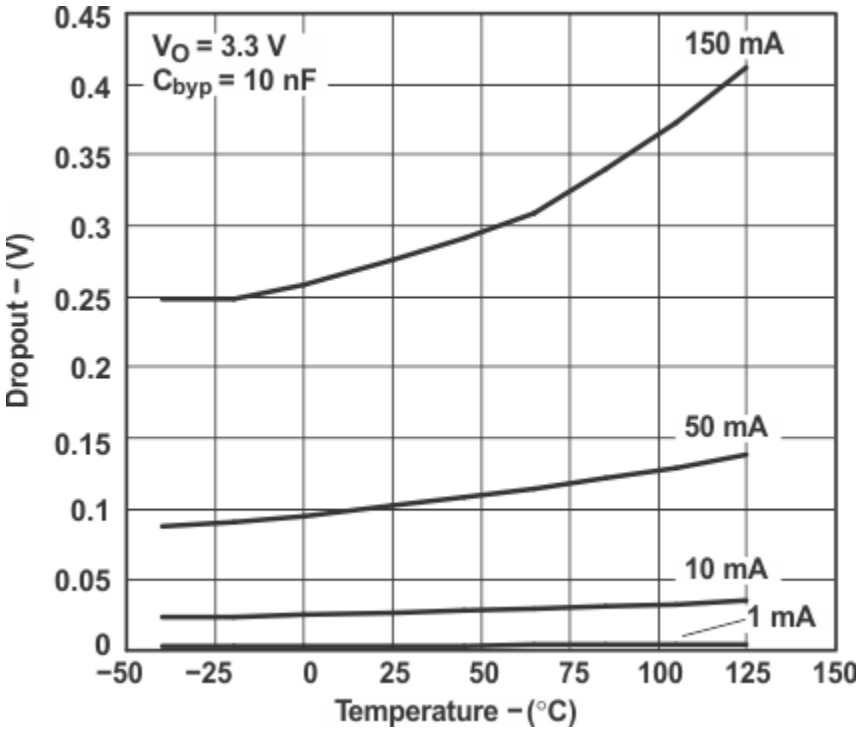
3 Description

The LP2985 family of fixed-output, low-dropout regulators offers exceptional, cost-effective performance for both portable and nonportable applications. Available in voltages of 1.8 V, 2.5 V, 2.8 V, 2.9 V, 3 V, 3.1 V, 3.3 V, 5 V, and 10 V, the family has an output tolerance of 1% for the A version (1.5% for the non-A version) and is capable of delivering 150-mA continuous load current. Standard regulator features, such as overcurrent and overtemperature protection, are included.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2985	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Dropout Voltage vs Temperature

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (January 2015) to Revision P (February 2022)	Page
• Changed *Applications* section	1
• Changed *Thermal Information* table: changed $R_{\theta JA}$ value from *206°C/W* to *205.4°C/W* and added $R_{\theta JC(top)}$, $R_{\theta JB}$, Ψ_{JT}, and Ψ_{JB} rows	4
• Changed *Application Information* section	13
• Changed *Typical Application* section to follow current standards	15

Changes from Revision N (June 2011) to Revision O (January 2015)	Page
• Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table	1

5 Pin Configuration and Functions

DBV (SOT-23) PACKAGE
(TOP VIEW)

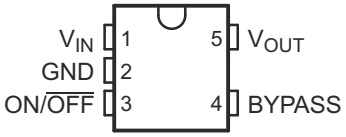


Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
BYPASS	4	I/O	Attach a 10-nF capacitor to improve low-noise performance.
GND	2	—	Ground
ON/$\overline{\text{OFF}}$	3	I	Active-low shutdown pin. Tie to V_{IN} if unused.
V_{IN}	1	I	Supply input
V_{OUT}	5	O	Voltage output

6 Specifications

6.1 Absolute Maximum Ratings

over virtual junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Continuous input voltage range(3)	–0.3	16	V
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage range	–0.3	16	V
	Output voltage range(2)	–0.3	9	V
I_O	Output current(4)	Internally limited (short-circuit protected)		—
$R_{\theta JA}$	Package thermal impedance(4) (5)		206	°C/W
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If load is returned to a negative power supply in a dual-supply system, the output must be diode clamped to GND.
(3) The PNP pass transistor has a parasitic diode connected between the input and output. This diode normally is reverse biased ($V_{IN} > V_{OUT}$), but is forward biased if the output voltage exceeds the input voltage by a diode drop (see the *Application and Implementation* section for more details).
(4) Maximum power dissipation is a function of $T_J(max)$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Supply input voltage	2.2(1)	16	V
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage	0	V_{IN}	V
I_{OUT}	Output current		150	mA
T_J	Virtual junction temperature	–40	125	°C

(1) Recommended minimum V_{IN} is the greater of 2.5 V or $V_{OUT(max)}$ + rated dropout voltage (max) for operating I_L.

6.4 Thermal Information

THERMAL METRIC(1)		LP2985 DBV 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	46.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at specified virtual junction temperature range, V_{IN} = $V_{OUT(NOM)}$ + 1 V, $V_{ON/\overline{OFF}}$ = 2 V, C_{IN} = 1 µF, and I_L = 1 mA, C_{OUT} = 4.7 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	LP2985A-xx			LP2985-xx			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_{OUT}	Output voltage tolerance	I_L = 1 mA	25°C	–1		1	–1.5		1.5	$\%V_{NOM}$
		1 mA ≤ I_L ≤ 50 mA	25°C	–1.5		1.5	–2.5		2.5	
			–40°C to 125°C	–2.5		2.5	–3.5		3.5	
		1 mA ≤ I_L ≤ 150 mA	25°C	–2.5		2.5	–3		3	
			–40°C to 125°C	–3.5		3.5	–4		4	
	Line regulation	V_{IN} = [$V_{OUT(NOM)}$ + 1 V] to 16 V	25°C		0.007	0.014		0.007	0.014	%/V
			–40°C to 125°C			0.032			0.032	
$V_{IN} – V_{OUT}$	Dropout voltage(1)	I_L = 0	25°C		1	3		1	3	mV
			–40°C to 125°C			5			5	
		I_L = 1 mA	25°C		7	10		7	10	
			–40°C to 125°C			15			15	
		I_L = 10 mA	25°C		40	60		40	60	
			–40°C to 125°C			90			90	
		I_L = 50 mA	25°C		120	150		120	150	
			–40°C to 125°C			225			225	
		I_L = 150 mA	25°C		280	350		280	350	
			–40°C to 125°C			575			575	
I_{GND}	GND pin current	I_L = 0 mA	25°C		65	95		65	95	µA
			25°C (LP2985-10)			125			125	
			–40°C to 125°C			125			125	
			–40°C to 125°C (LP2985-10)			160			160	
		I_L = 1 mA	25°C		75	110		75	110	
			25°C (LP2985-10)			140			140	
			–40°C to 125°C			170			170	
		I_L = 10 mA	25°C		120	220		120	220	
			25°C (LP2985-10)			250			250	
			–40°C to 125°C			400			400	
		I_L = 50 mA	25°C		350	600		350	600	
			25°C (LP2985-10)			650			650	
			–40°C to 125°C			1000			1000	
		I_L = 150 mA	25°C		850	1500		850	1500	
			25°C (LP2985-10)			1800			1800	
			–40°C to 125°C			2500			2500	
		$V_{ON/\overline{OFF}}$ < 0.3 V (OFF)	25°C		0.01	0.8		0.01	0.8	
		$V_{ON/\overline{OFF}}$ < 0.15 V (OFF)	–40°C to 105°C		0.05	2		0.05	2	
			–40°C to 125°C			5			5	
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage(2)	$V_{ON/\overline{OFF}}$ = HIGH → output ON	25°C		1.4			1.4		V
			–40°C to 125°C	1.6			1.6			
		$V_{ON/\overline{OFF}}$ = LOW → output OFF	25°C		0.55			0.55		
			–40°C to 125°C			0.15			0.15	
$I_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input current	$V_{ON/\overline{OFF}}$ = 0 V	25°C		0.01			0.01		µA
			–40°C to 125°C			–2			–2	
		$V_{ON/\overline{OFF}}$ = 5 V	25°C		5			5		
			–40°C to 125°C			15			15	

6.5 Electrical Characteristics (continued)

at specified virtual junction temperature range, $V_{IN} = V_{OUT(NOM)} + 1$ V, $V_{ON/\overline{OFF}} = 2$ V, $C_{IN} = 1$ µF, and $I_L = 1$ mA, $C_{OUT} = 4.7$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	LP2985A-xx			LP2985-xx			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_n	Output noise (RMS)	BW = 300 Hz to 50 kHz, C_{OUT} = 10 µF, C_{BYPASS} = 10 nF	25°C		30			30		µV
$\Delta V_{OUT}/\Delta V_{IN}$	Ripple rejection	f = 1kHz, C_{OUT} = 10 µF, C_{BYPASS} = 10 nF	25°C		45			45		dB
$I_{OUT(PK)}$	Peak output current	$V_{OUT} \geq V_{O(NOM)} - 5\%$	25°C		350			350		mA
$I_{OUT(SC)}$	Short-circuit current	$R_L = 0$ (steady state)(3)	25°C		400			400		mA

(1) Dropout voltage is defined as the input-to-output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential.
(2) The ON/$\overline{OFF}$ input must be driven properly for reliable operation (see the *Application and Implementation* section).
(3) See Figure 6-6 in the *Typical Characteristics* section.

6.6 Typical Characteristics

C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, and ON/$\overline{OFF}$ pin tied to V_{IN} (unless otherwise specified)

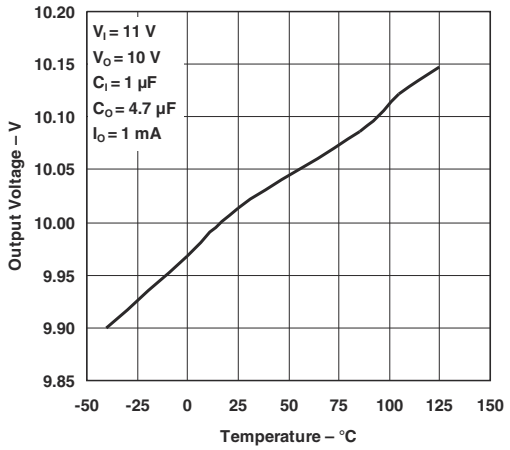


Figure 6-1. Output Voltage vs Temperature

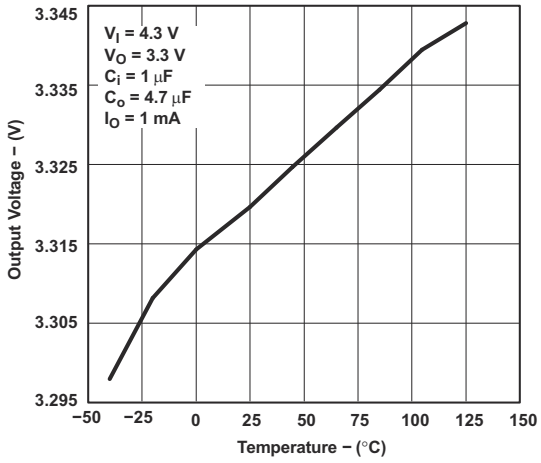


Figure 6-2. Output Voltage vs Temperature

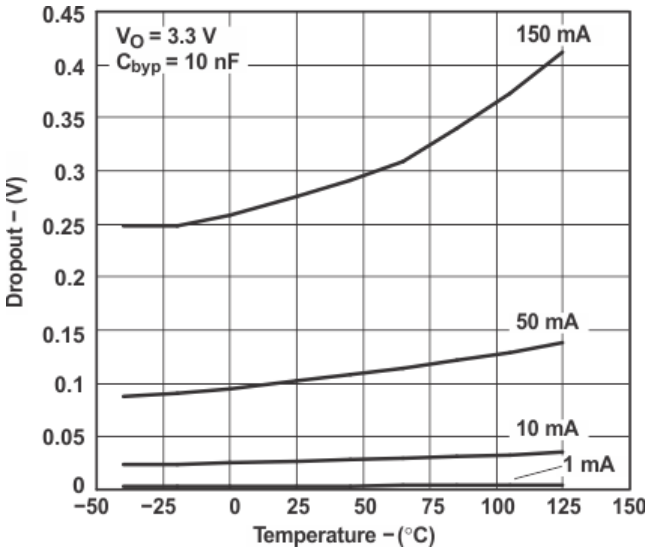


Figure 6-3. Dropout Voltage vs Temperature

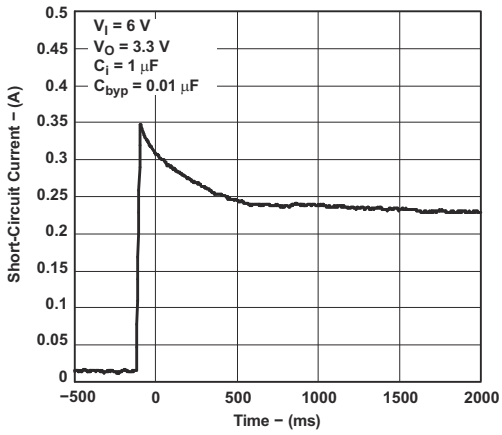


Figure 6-4. Short-Circuit Current vs Time

6.6 Typical Characteristics (continued)

C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, and ON/$\overline{OFF}$ pin tied to V_{IN} (unless otherwise specified)

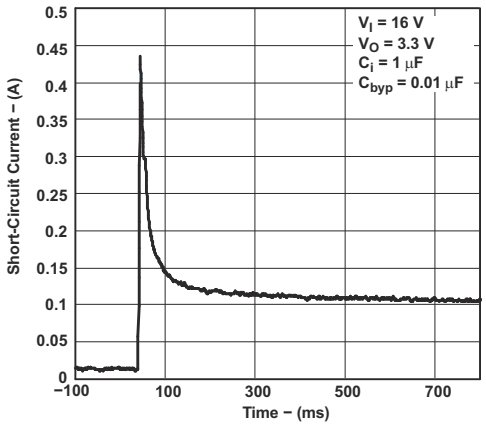


Figure 6-5. Short-Circuit Current vs Time

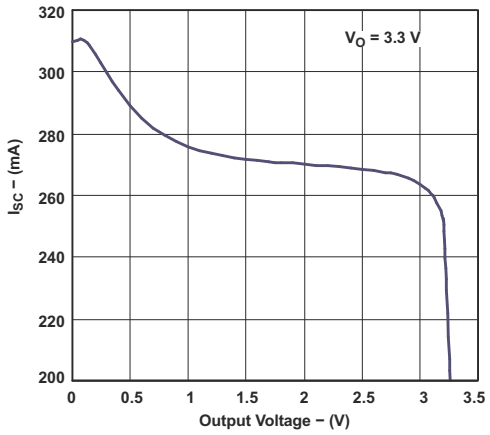


Figure 6-6. Short-Circuit Current vs Output Voltage

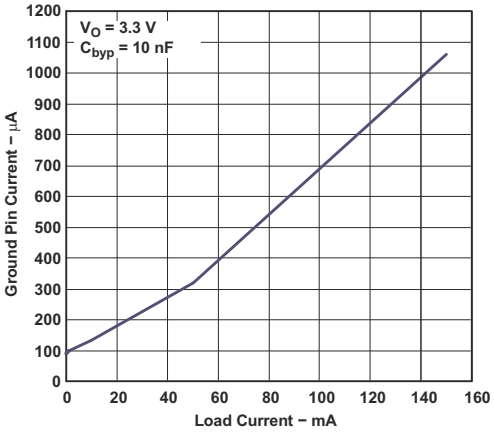


Figure 6-7. Ground Pin Current vs Load Current

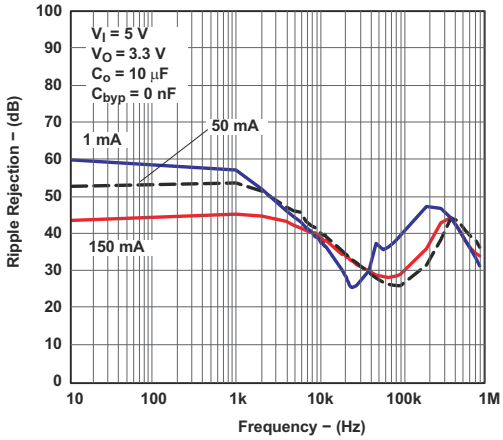


Figure 6-8. Ripple Rejection vs Frequency

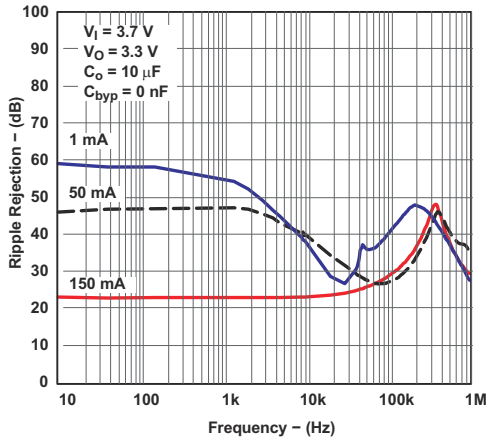


Figure 6-9. Ripple Rejection vs Frequency

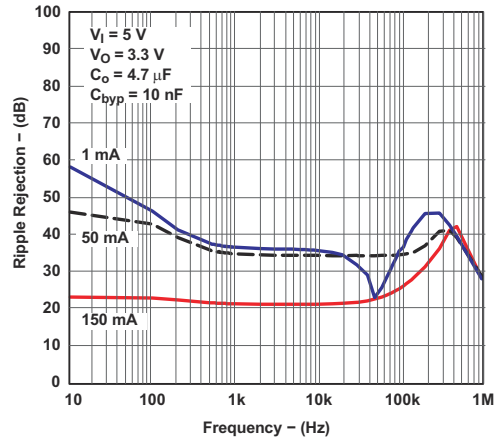


Figure 6-10. Ripple Rejection vs Frequency

6.6 Typical Characteristics (continued)

C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, and ON/$\overline{OFF}$ pin tied to V_{IN} (unless otherwise specified)

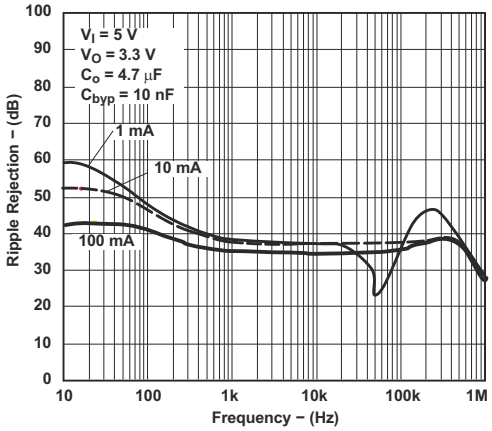


Figure 6-11. Ripple Rejection vs Frequency

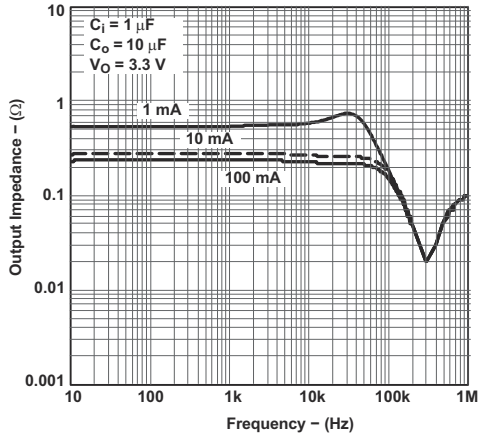


Figure 6-12. Output Impedance vs Frequency

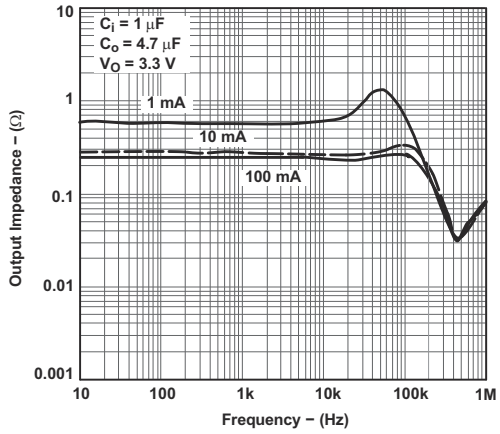


Figure 6-13. Output Impedance vs Frequency

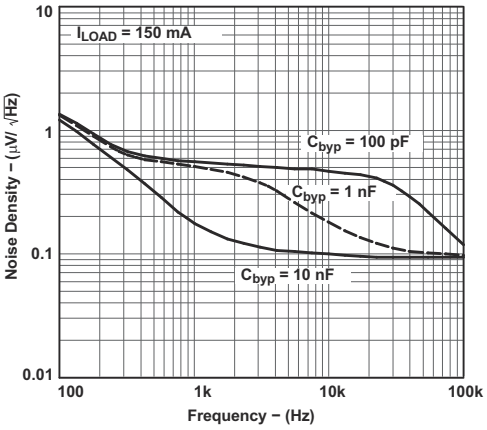


Figure 6-14. Output Noise Density vs Frequency

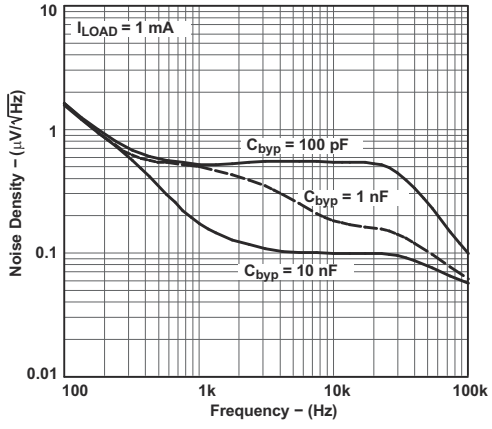


Figure 6-15. Output Noise Density vs Frequency

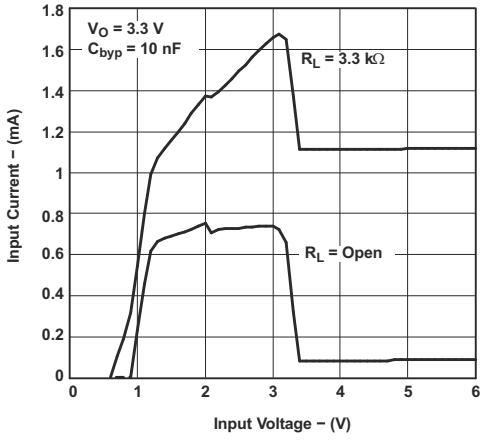


Figure 6-16. Input Current vs Input Voltage

6.6 Typical Characteristics (continued)

C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, and ON/$\overline{OFF}$ pin tied to V_{IN} (unless otherwise specified)

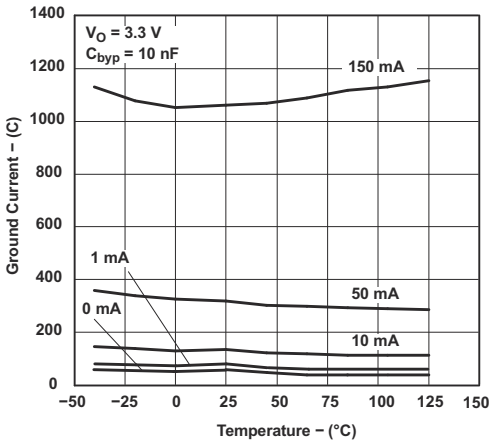


Figure 6-17. Ground-Pin Current vs Temperature

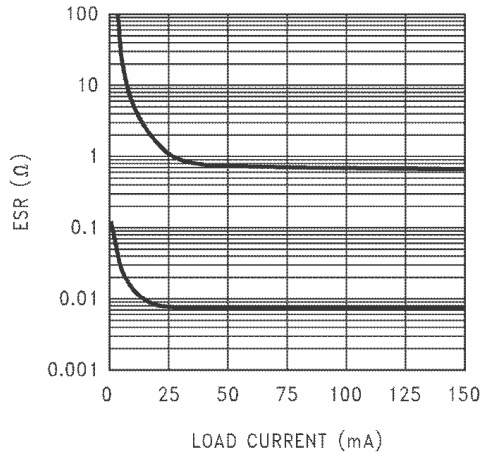


Figure 6-18. 2.2-µF Stable ESR Range for Output Voltage ≤ 2.3 V

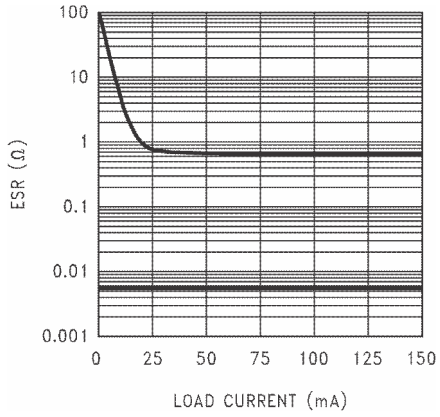


Figure 6-19. 4.7-µF Stable ESR Range for Output Voltage ≤ 2.3 V

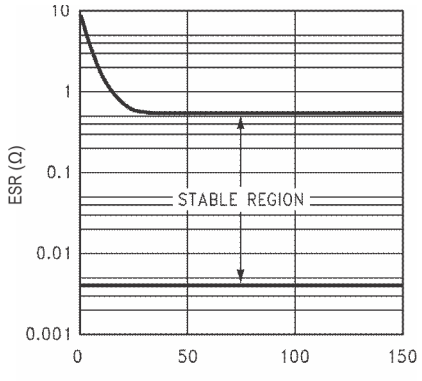


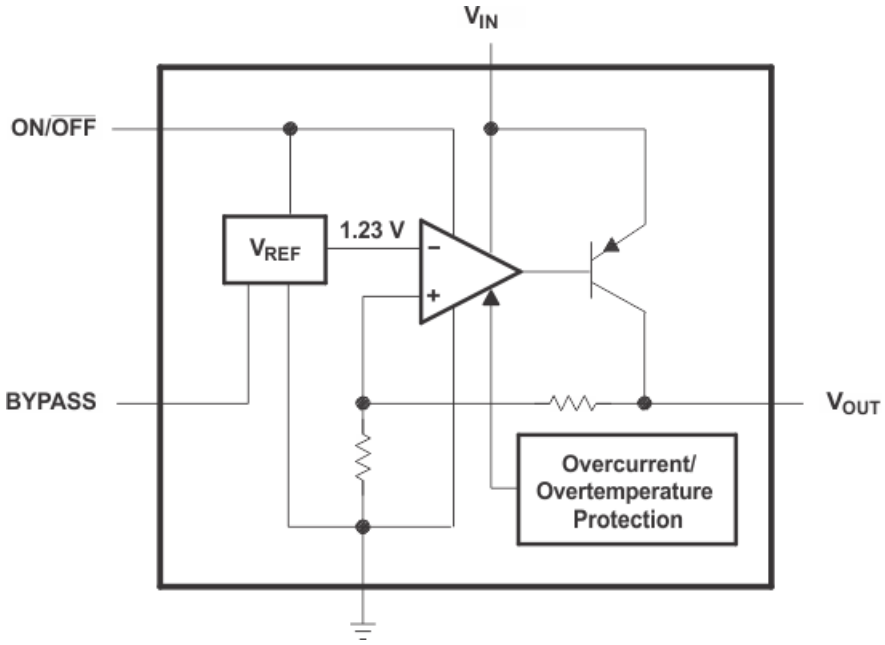
Figure 6-20. 2.2-µF, 3.3-µF Stable ESR Range for Output Voltage ≥ 2.5 V

7 Detailed Description

7.1 Overview

The LP2985 family of fixed-output, low-dropout regulators offers exceptional, cost-effective performance for both portable and nonportable applications. Available in voltages of 1.8 V, 2.5 V, 2.8 V, 2.9 V, 3 V, 3.1 V, 3.3 V, 5 V, and 10 V, the family has an output tolerance of 1% for the A version (1.5% for the non-A version) and is capable of delivering 150-mA continuous load current. Standard regulator features, such as overcurrent and overtemperature protection, are included.

7.2 Functional Block Diagram



7.3 Feature Description

The LP2985 has a host of features that makes the regulator an ideal candidate for a variety of portable applications:

- Low dropout: A PNP pass element allows a typical dropout of 280 mV at 150-mA load current and 7 mV at 1-mA load.
- Low quiescent current: The use of a vertical PNP process allows for quiescent currents that are considerably lower than those associated with traditional lateral PNP regulators.
- Shutdown: A shutdown feature is available, allowing the regulator to consume only 0.01 µA when the ON/$\overline{OFF}$ pin is pulled low.
- Low-ESR-capacitor friendly: The regulator is stable with low-ESR capacitors, allowing the use of small, inexpensive, ceramic capacitors in cost-sensitive applications.
- Low noise: A BYPASS pin allows for low-noise operation, with a typical output noise of 30 μV_{RMS}, with the use of a 10-nF bypass capacitor.
- Small packaging: For the most space-constrained needs, the regulator is available in the SOT-23 package.

7.4 Device Functional Modes

7.4.1 Normal Operation

In normal operation, the device will output a fixed voltage corresponding with the orderable part number. The device can deliver 150 mA of continuous load current.

7.4.2 Shutdown Mode

Set the ON/$\overline{OFF}$ pin low to shut down the device when V_{IN} is still present. If a shutdown mode is not needed, tie the pin to V_{IN}. For proper operation, do not leave ON/$\overline{OFF}$ unconnected, and apply a signal with a slew rate of ≥ 40 mV/µs.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Capacitors

8.1.1.1 Input Capacitor (C_{IN})

A minimum value of 1 µF (over the entire operating temperature range) is required at the input of the LP2985. In addition, this input capacitor must be located within 1 cm of the input pin and connected to a clean analog ground. There are no equivalent series resistance (ESR) requirements for this capacitor, and the capacitance can be increased without limit.

8.1.1.2 Output Capacitor (C_{OUT})

As an advantage over other regulators, the LP2985 permits the use of low-ESR capacitors at the output, including ceramic capacitors that can have an ESR as low as 5 mΩ. Tantalum and film capacitors also can be used if size and cost are not issues. The output capacitor must be located within 1 cm of the output pin and be returned to a clean analog ground.

As with other PNP LDOs, stability conditions require the output capacitor to have a minimum capacitance and an ESR that falls within a certain range.

- Minimum C_{OUT}: 2.2 µF (can be increased without limit to improve transient response stability margin)
- ESR range: see Figure 6-18 through Figure 6-20

Both the minimum capacitance and ESR requirement are critical to be met *over the entire operating temperature range*. Depending on the type of capacitors used, both these parameters can vary significantly with temperature (see the *Capacitor Characteristics* section).

8.1.1.3 Noise Bypass Capacitor (C_{BYPASS})

The LP2985 allows for low-noise performance with the use of a bypass capacitor that is connected to the internal band-gap reference via the BYPASS pin. This high-impedance band-gap circuitry is biased in the microampere range and, thus, cannot be loaded significantly, otherwise, its output (and, correspondingly, the output of the regulator) changes. Thus, for best output accuracy, dc leakage current through C_{BYPASS} must be minimized as much as possible and must never exceed 100 nA.

A 10-nF capacitor is recommended for C_{BYPASS}. Ceramic and film capacitors are well suited for this purpose.

8.1.1.4 Capacitor Characteristics

8.1.1.4.1 Ceramics

Ceramic capacitors are ideal choices for use on the output of the LP2985 for several reasons. For capacitances in the range of 2.2 µF to 4.7 µF, ceramic capacitors have the lowest cost and the lowest ESR, making them choice candidates for filtering high-frequency noise. For instance, a typical 2.2-µF ceramic capacitor has an ESR in the range of 10 mΩ to 20 mΩ and, thus, satisfies minimum ESR requirements of the regulator.

Ceramic capacitors have one major disadvantage that must be taken into account—a poor temperature coefficient, where the capacitance can vary significantly with temperature. For instance, a large-value ceramic capacitor (≥ 2.2 µF) can lose more than half of its capacitance as the temperature rises from 25°C to 85°C. Thus, a 2.2-µF capacitor at 25°C drops well below the minimum C_{OUT} required for stability, as ambient temperature rises. For this reason, select an output capacitor that maintains the minimum 2.2 µF required for

stability over the entire operating temperature range. There are some ceramic capacitors that can maintain a ±15% capacitance tolerance over temperature.

8.1.1.4.2 Tantalum

Tantalum capacitors can be used at the output of the LP2985, but there are significant disadvantages that can prohibit their use:

- In the 1-µF to 4.7-µF range, tantalum capacitors are more expensive than ceramics of the equivalent capacitance and voltage ratings.
- Tantalum capacitors have higher ESRs than their equivalent-sized ceramic counterparts. Thus, to meet the ESR requirements, a higher-capacitance tantalum may be required, at the expense of larger size and higher cost.
- The ESR of a tantalum capacitor increases as temperature drops, as much as double from +25°C to –40°C. Thus, ESR margins must be maintained over the temperature range to prevent regulator instability.

8.1.2 Reverse Input-Output Voltage

As shown in Figure 8-1, there is an inherent diode present across the PNP pass element of the LP2985.

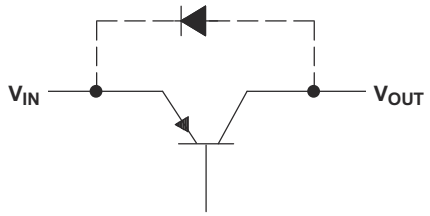


Figure 8-1. Inherent PNP Body Diode

With the anode connected to the output, this diode is reverse biased during normal operation, since the input voltage is higher than the output. However, if the output is pulled higher than the input for any reason, this diode is forward biased and can cause a parasitic silicon-controlled rectifier (SCR) to latch, resulting in high current flowing from the output to the input. Thus, to prevent possible damage to the regulator in any application where the output may be pulled above the input, or the input may be shorted to ground, connect an external Schottky diode between the output and input. With the anode on the output, this Schottky diode limits the reverse voltage across the output and input pins to approximately 0.3 V (as shown in Figure 8-2), preventing the regulator internal diode from forward biasing.

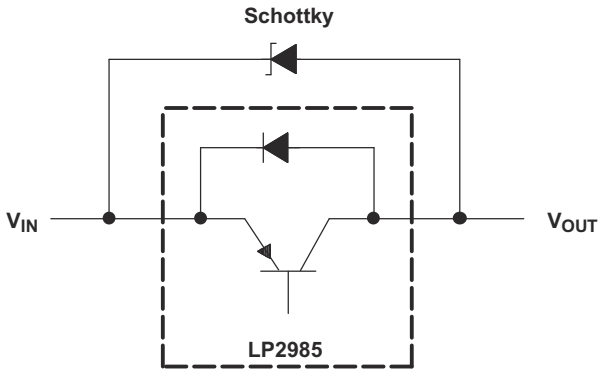


Figure 8-2. External Schottky Diode to Prevent Reverse Current Through the Device

8.2 Typical Application

Figure 8-3 shows the standard usage of the LP2985 as a low-dropout regulator.

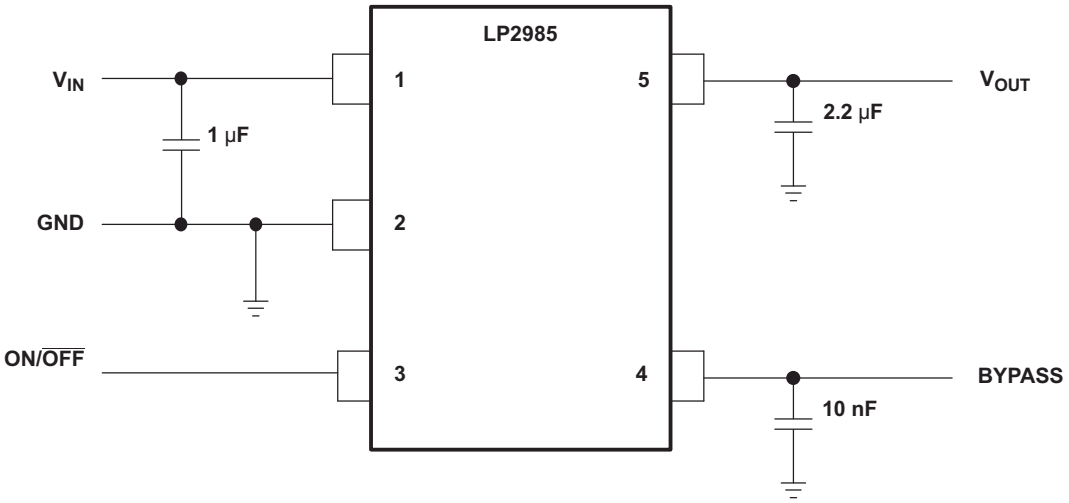


Figure 8-3. LP2985 Typical Application

8.2.1 Design Requirements

Minimum C_{OUT} value for stability (can be increased without limit for improved stability and transient response)

ON/$\overline{\text{OFF}}$ must be actively terminated. Connect to V_{IN} if shutdown feature is not used.

Optional BYPASS capacitor for low-noise operation.

8.2.2 Detailed Design Procedure

8.2.2.1 ON/$\overline{\text{OFF}}$ Operation

The LP2985 allows for a shutdown mode via the ON/$\overline{\text{OFF}}$ pin. Driving the pin LOW (≤ 0.3 V) turns the device OFF; conversely, a HIGH (≥ 1.6 V) turns the device ON. If the shutdown feature is not used, connect ON/$\overline{\text{OFF}}$ to the input to ensure that the regulator is on at all times. For proper operation, do not leave ON/$\overline{\text{OFF}}$ unconnected, and apply a signal with a slew rate of ≥ 40 mV/µs.

8.2.3 Application Curves

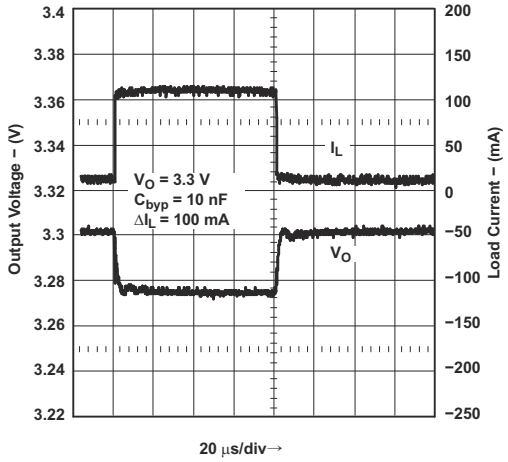


Figure 8-4. Load Transient Response

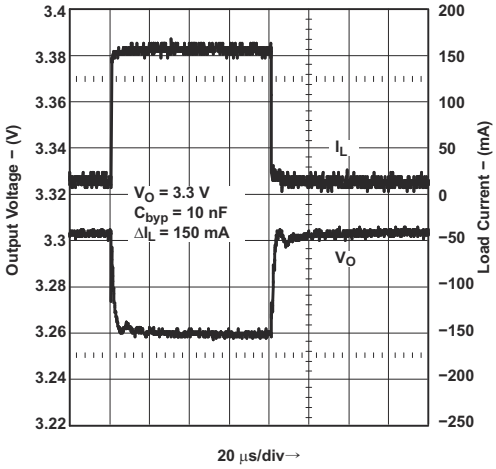


Figure 8-5. Load Transient Response

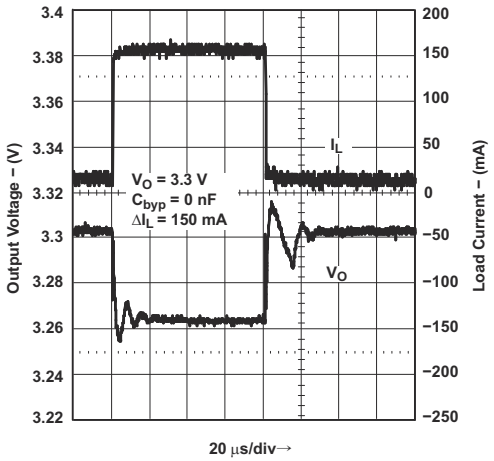


Figure 8-6. Load Transient Response

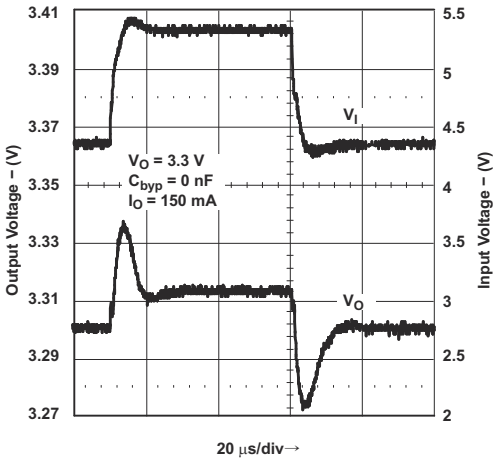


Figure 8-7. Line Transient Response

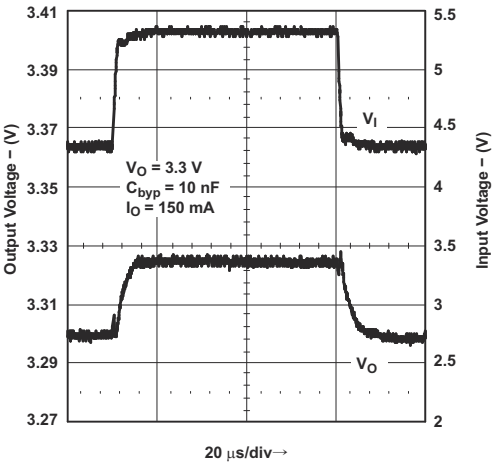


Figure 8-8. Line Transient Response

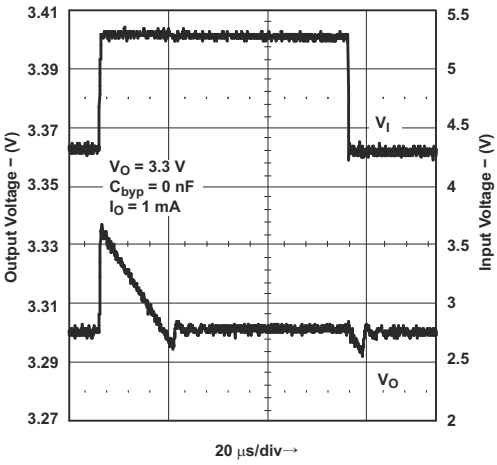


Figure 8-9. Line Transient Response

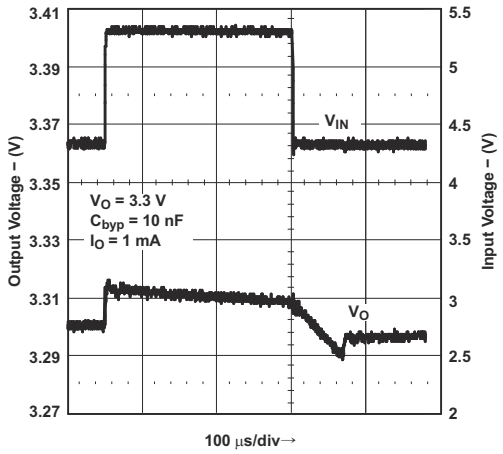


Figure 8-10. Line Transient Response

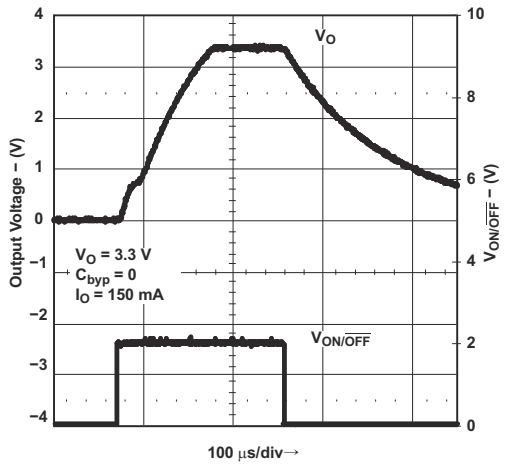


Figure 8-11. Turn-On Time

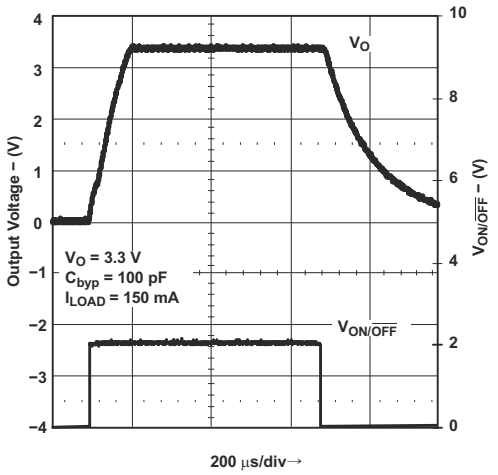


Figure 8-12. Turn-On Time

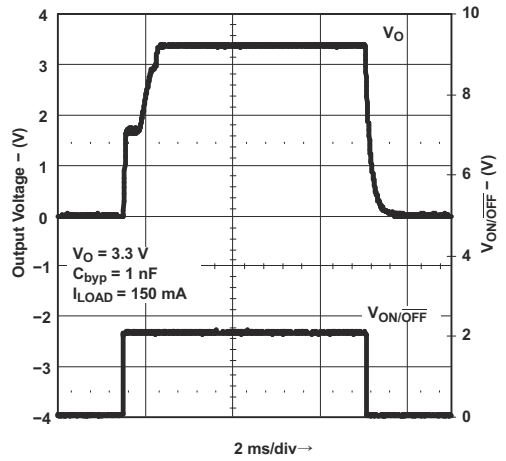


Figure 8-13. Turn-On Time

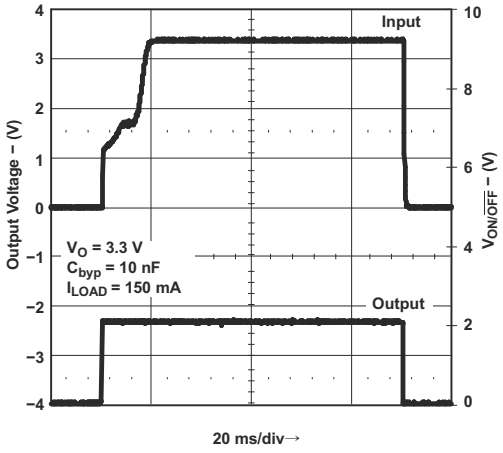


Figure 8-14. Turn-On Time

9 Power Supply Recommendations

A power supply can be used at the input voltage within the ranges given in the *Recommended Operating Conditions* table. Use bypass capacitors as described in the *Layout Guidelines* section.

10 Layout

10.1 Layout Guidelines

- Bypass the input pin to ground with a bypass-capacitor.
- The optimum placement of the bypass capacitor is closest to the V_{IN} of the device and GND of the system. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the V_{IN} pin, and the GND pin of the system.
- For operation at full-rated load, use wide trace lengths to eliminate IR drop and heat dissipation.

10.2 Layout Example

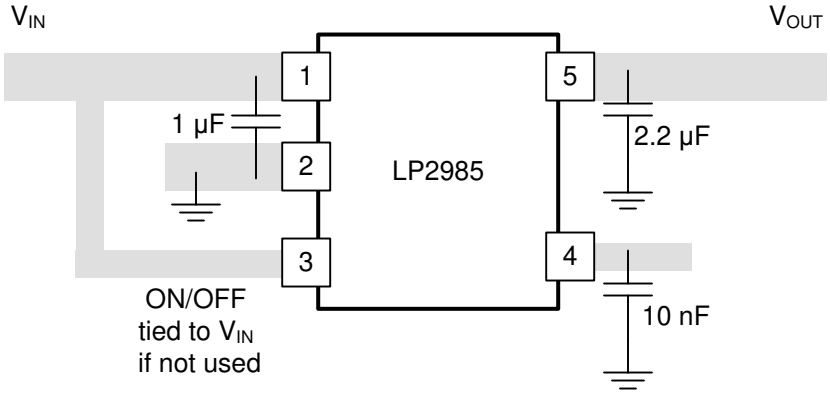


Figure 10-1. Layout Diagram

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2985-10DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LRCG	Samples
LP2985-10DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LRCG	Samples
LP2985-18DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPHG, LPHL)	Samples
LP2985-18DBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPHG	Samples
LP2985-18DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPHG	Samples
LP2985-18DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPHG, LPHL)	Samples
LP2985-18DBVTE4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPHG	Samples
LP2985-18DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPHG	Samples
LP2985-25DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPLG, LPLL)	Samples
LP2985-25DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPLG, LPLL)	Samples
LP2985-28DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPGG, LPGL)	Samples
LP2985-28DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPGG, LPGL)	Samples
LP2985-28DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPGG	Samples
LP2985-29DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPMG, LPML)	Samples
LP2985-30DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPNG, LPNL)	Samples
LP2985-30DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPNG, LPNL)	Samples
LP2985-30DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPNG, LPNL)	Samples
LP2985-30DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPNG, LPNL)	Samples
LP2985-33DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPFG, LPFL)	Samples
LP2985-33DBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPFG	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2985-33DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPFG	Samples
LP2985-33DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPFG, LPFL)	Samples
LP2985-33DBVTE4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPFG	Samples
LP2985-33DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPFG	Samples
LP2985-50DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPSG, LPSL)	Samples
LP2985-50DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPSG, LPSL)	Samples
LP2985-50DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPSG, LPSL)	Samples
LP2985-50DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPSG, LPSL)	Samples
LP2985A-10DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LRDG	Samples
LP2985A-10DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LRDG	Samples
LP2985A-18DBVJ	ACTIVE	SOT-23	DBV	5	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPTL	Samples
LP2985A-18DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPTG, LPTL)	Samples
LP2985A-18DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPTG	Samples
LP2985A-18DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPTG, LPTL)	Samples
LP2985A-25DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPUG, LPUL)	Samples
LP2985A-25DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPUG, LPUL)	Samples
LP2985A-25DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPUG, LPUL)	Samples
LP2985A-28DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPJG, LPJL)	Samples
LP2985A-28DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPJG, LPJL)	Samples
LP2985A-29DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPZG, LPZL)	Samples
LP2985A-30DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LRAG, LRAL)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2985A-30DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LRAG, LRAL)	Samples
LP2985A-33DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPKG, LPKL)	Samples
LP2985A-33DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPKG	Samples
LP2985A-33DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPKG, LPKL)	Samples
LP2985A-33DBVTE4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPKG	Samples
LP2985A-33DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPKG	Samples
LP2985A-50DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LR1G, LR1L)	Samples
LP2985A-50DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LR1G, LR1L)	Samples
LP2985A-50DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LR1G, LR1L)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

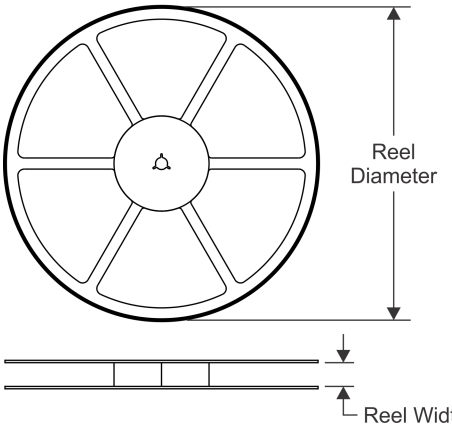
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

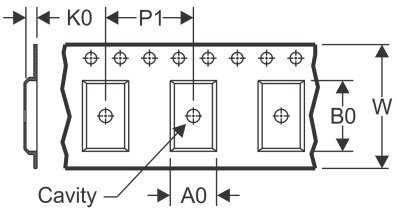
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

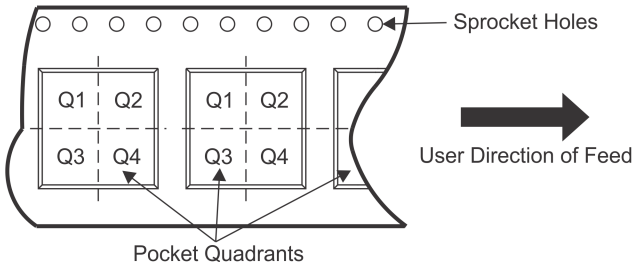


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

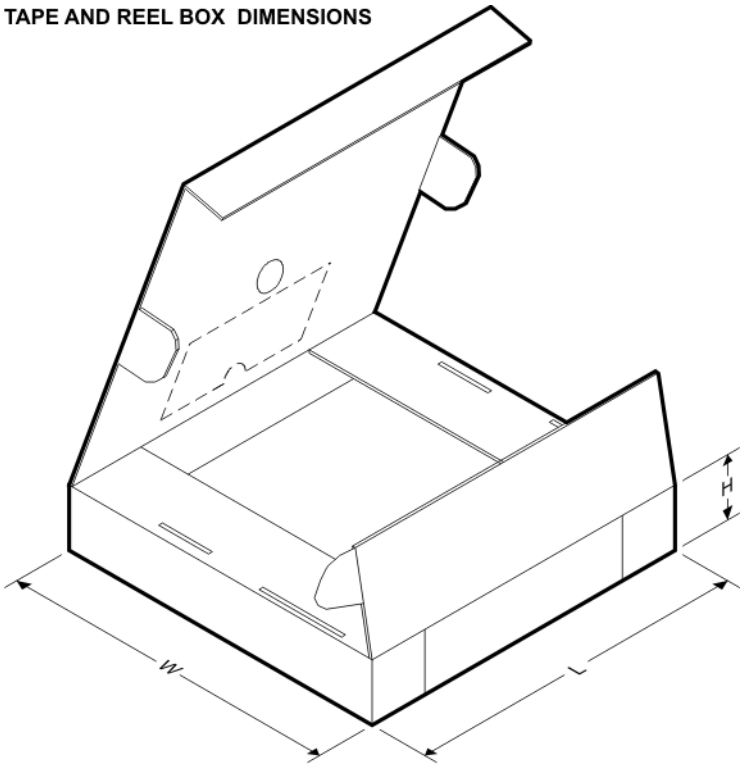


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2985-10DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985-10DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2985-18DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2985-18DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2985-18DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985-25DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2985-28DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985-28DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2985-29DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985-30DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2985-33DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2985-33DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985-33DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985-50DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985A-10DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985A-10DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2985A-18DBVJ	SOT-23	DBV	5	10000	330.0	8.4	3.17	3.23	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2985A-18DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985A-18DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985A-25DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985A-25DBVT	SOT-23	DBV	5	250	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
LP2985A-28DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985A-28DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
LP2985A-29DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985A-30DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985A-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2985A-33DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2985A-33DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985A-33DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2985A-50DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2985-10DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985-10DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
LP2985-18DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985-18DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0

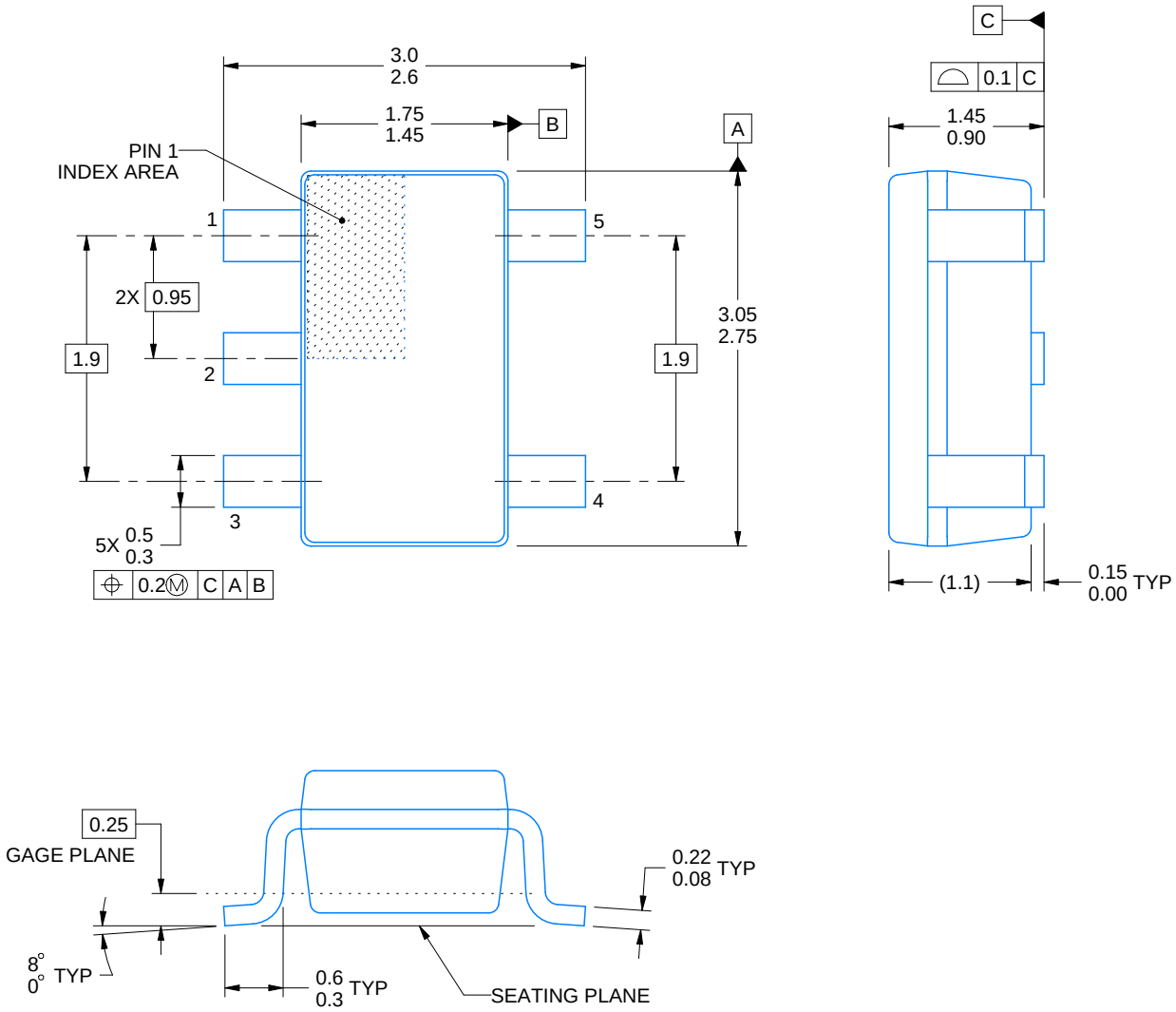
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2985-18DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
LP2985-25DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985-28DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985-28DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
LP2985-29DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985-30DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985-33DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985-33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
LP2985-33DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
LP2985-50DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985A-10DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985A-10DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
LP2985A-18DBVJ	SOT-23	DBV	5	10000	358.0	332.0	35.0
LP2985A-18DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985A-18DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985A-25DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985A-25DBVT	SOT-23	DBV	5	250	205.0	200.0	33.0
LP2985A-28DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985A-28DBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
LP2985A-29DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985A-30DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985A-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985A-33DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2985A-33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
LP2985A-33DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
LP2985A-50DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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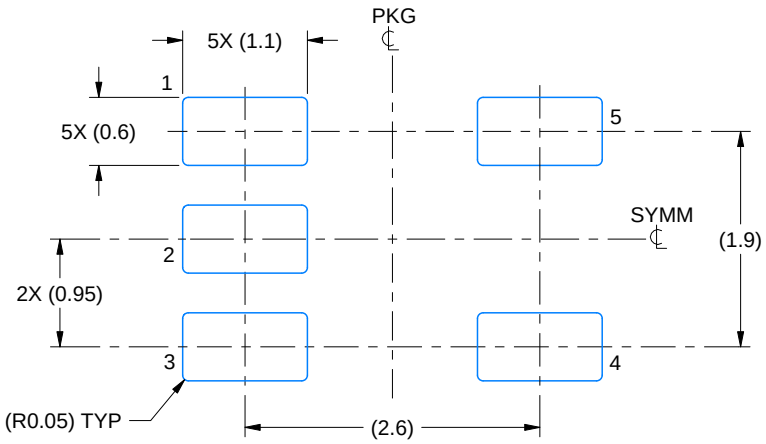
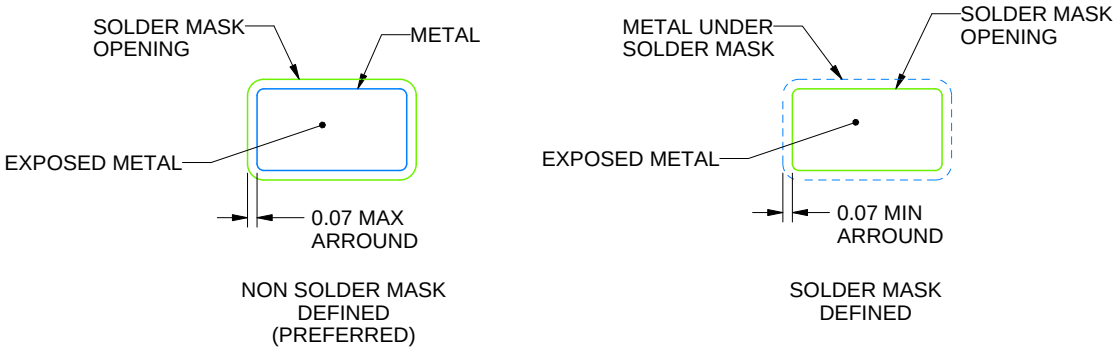
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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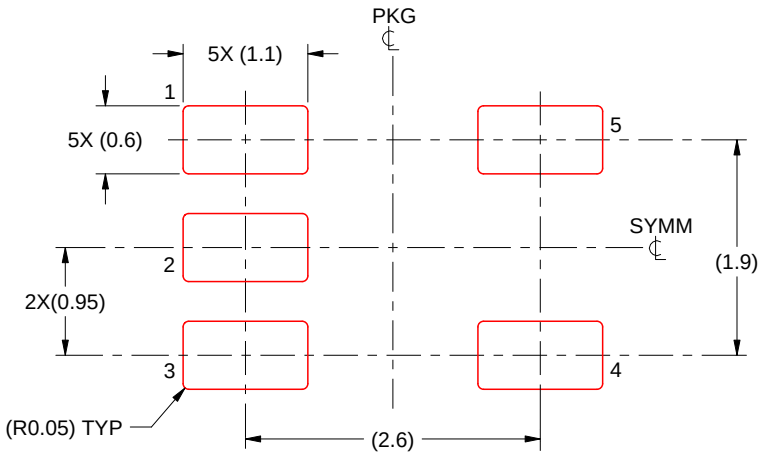
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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