

# SN74LV540A Octal Buffers/Drivers with 3-State Outputs

## 1 Features

- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 8.5 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  
 $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  
 $> 2.3$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 2000-V Charged-Device Model

## 2 Applications

- Tests and Measurements
- Industrial Transports
- Patient Monitoring
- Wireless Infrastructure
- Network Switches
- Automotive Infotainment

## 3 Description

The SN74LV540A device is an octal buffer/driver designed for 2-V to 5.5-V  $V_{CC}$  operation.

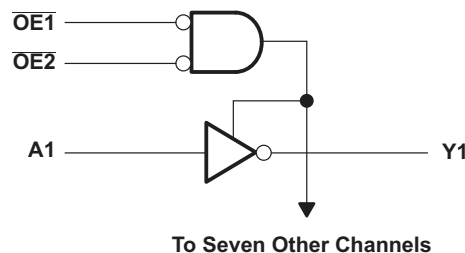
This device is ideal for driving bus lines or buffer memory address registers. It features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE    | BODY SIZE (NOM) |
|-------------|------------|-----------------|
| SN74LV540A  | VQFN (20)  | 4.50 x 3.50 mm  |
|             | SSOP (20)  | 7.50 x 5.30 mm  |
|             | TSSOP (20) | 6.50 x 4.40 mm  |
|             | TVSOP (20) | 5.00 x 4.40 mm  |
|             | SOIC (20)  | 12.80 x 7.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## 4 Simplified Schematic



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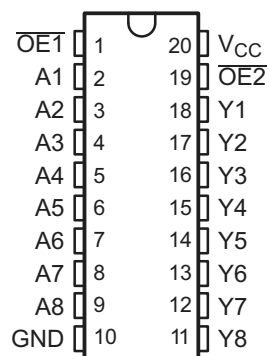
|                                                                               |          |                                                                  |           |
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## 5 Revision History

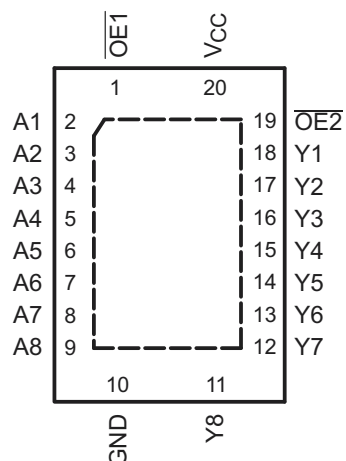
| Changes from Revision H (April 2005) to Revision I                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Page |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. .... | 1    |
| • Deleted <i>Ordering Information</i> table. ....                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 1    |
| • Changed MAX operating temperature to 125°C in <i>Recommended Operating Conditions</i> table. ....                                                                                                                                                                                                                                                                                                                                                                                                        | 5    |

## 6 Pin Configuration and Functions

**SN74LV540A . . . DB, DGV, DW, NS,  
OR PW PACKAGE  
(TOP VIEW)**



**SN74LV540A . . . RGY PACKAGE  
(TOP VIEW)**



### Pin Functions

| PIN |                  | TYPE | DESCRIPTION     |
|-----|------------------|------|-----------------|
| NO. | NAME             |      |                 |
| 1   | $\overline{OE1}$ | I    | Output Enable 1 |
| 2   | A1               | I    | A1 Input        |
| 3   | A2               | I    | A2 Input        |
| 4   | A3               | I    | A3 Input        |
| 5   | A4               | I    | A4 Input        |
| 6   | A5               | I    | A5 Input        |
| 7   | A6               | I    | A6 Input        |
| 8   | A7               | I    | A7 Input        |
| 9   | A8               | I    | A8 Input        |
| 10  | GND              | —    | Ground Pin      |
| 11  | Y8               | O    | Y8 Output       |
| 12  | Y7               | O    | Y7 Output       |
| 13  | Y6               | O    | Y6 Output       |
| 14  | Y5               | O    | Y5 Output       |
| 15  | Y4               | O    | Y4 Output       |
| 16  | Y3               | O    | Y3 Output       |
| 17  | Y2               | O    | Y2 Output       |
| 18  | Y1               | O    | Y1 Output       |
| 19  | $\overline{OE2}$ | I    | Output Enable 2 |
| 20  | V <sub>CC</sub>  | —    | Power Pin       |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|           |                                                                                             | MIN                   | MAX            | UNIT   |
|-----------|---------------------------------------------------------------------------------------------|-----------------------|----------------|--------|
| $V_{CC}$  | Supply voltage range                                                                        | –0.5                  | 7              | V      |
| $V_I$     | Input voltage range <sup>(2)</sup>                                                          | –0.5                  | 7              | V      |
| $V_O$     | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | –0.5                  | 7              | V      |
| $V_O$     | Output voltage range applied in the high or low state <sup>(2)(3)</sup>                     | –0.5                  | $V_{CC} + 0.5$ | V      |
| $I_{IK}$  | Input clamp current                                                                         | $V_I < 0$             |                | –20 mA |
| $I_{OK}$  | Output clamp current                                                                        | $V_O < 0$             |                | –50 mA |
| $I_O$     | Continuous output current                                                                   | $V_O = 0$ to $V_{CC}$ |                | ±35 mA |
|           | Continuous current through $V_{CC}$ or GND                                                  |                       |                | ±70 mA |
| $T_{stg}$ | Storage temperature range                                                                   | –65                   | 150            | °C     |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5-V maximum.

### 7.2 ESD Ratings

|             |                                                                                          | VALUE | UNIT |
|-------------|------------------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge                                                                  |       |      |
|             | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | 2000  | V    |
|             | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | 2000  |      |
|             | Machine Model (MM)                                                                       | 200   |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                    |                                  | SN74LV540A            |                       | UNIT |
|-----------------|------------------------------------|----------------------------------|-----------------------|-----------------------|------|
|                 |                                    |                                  | MIN                   | MAX                   |      |
| V <sub>CC</sub> | Supply voltage                     |                                  | 2                     | 5.5                   | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 2 V            | 1.5                   |                       | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.7 |                       |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.7 |                       |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.7 |                       |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 2 V            |                       | 0.5                   | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V |                       | V <sub>CC</sub> × 0.3 |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   |                       | V <sub>CC</sub> × 0.3 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V |                       | V <sub>CC</sub> × 0.3 |      |
| V <sub>I</sub>  | Input voltage                      |                                  | 0                     | 5.5                   | V    |
| V <sub>O</sub>  | Output voltage                     | High or low state                | 0                     | V <sub>CC</sub>       | V    |
|                 |                                    | 3-state                          | 0                     | 5.5                   |      |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 2 V            |                       | –50                   | μA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V |                       | –2                    | mA   |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   |                       | –8                    |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V |                       | –16                   |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 2 V            |                       | 50                    | μA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V |                       | 2                     | mA   |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   |                       | 8                     |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V |                       | 16                    |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 2.3 V to 2.7 V |                       | 200                   | ns/V |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   |                       | 100                   |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V |                       | 20                    |      |
| T <sub>A</sub>  | Operating free-air temperature     |                                  | –40                   | 125                   | °C   |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74LV540A |       |      |      |       |      | UNIT |
|-------------------------------|----------------------------------------------|------------|-------|------|------|-------|------|------|
|                               |                                              | DB         | DGV   | DW   | NS   | PW    | RGY  |      |
|                               |                                              | 20 PINS    |       |      |      |       |      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 96.0       | 116.1 | 79.8 | 77.1 | 102.8 | 35.1 | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 57.7       | 31.3  | 45.8 | 43.6 | 36.8  | 43.3 |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 51.2       | 57.6  | 47.4 | 44.6 | 53.8  | 12.9 |      |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 19.4       | 1.0   | 18.5 | 17.2 | 2.5   | 0.9  |      |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 50.8       | 56.9  | 47.0 | 44.2 | 53.3  | 12.9 |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | —          | —     | —    | —    | —     | 7.9  |      |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS                                             | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |     | –40°C to 85°C         |     | –40°C to 125°C        |     | UNIT |
|------------------|-------------------------------------------------------------|-----------------|-----------------------|-----|-----|-----------------------|-----|-----------------------|-----|------|
|                  |                                                             |                 | MIN                   | TYP | MAX | MIN                   | MAX | MIN                   | MAX |      |
| V <sub>OH</sub>  | I <sub>OH</sub> = –50 μA                                    | 2 V to 5.5 V    | V <sub>CC</sub> – 0.1 |     |     | V <sub>CC</sub> – 0.1 |     | V <sub>CC</sub> – 0.1 |     | V    |
|                  | I <sub>OH</sub> = –2 mA                                     | 2.3 V           | 2                     |     |     | 2                     |     | 2                     |     |      |
|                  | I <sub>OH</sub> = –8 mA                                     | 3 V             | 2.48                  |     |     | 2.48                  |     | 2.48                  |     |      |
|                  | I <sub>OH</sub> = –16 mA                                    | 4.5 V           | 3.8                   |     |     | 3.8                   |     | 3.8                   |     |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = 50 μA                                     | 2 V to 5.5 V    | 0.1                   |     |     | 0.1                   |     | 0.1                   |     | V    |
|                  | I <sub>OL</sub> = 2 mA                                      | 2.3 V           | 0.4                   |     |     | 0.4                   |     | 0.4                   |     |      |
|                  | I <sub>OL</sub> = 8 mA                                      | 3 V             | 0.44                  |     |     | 0.44                  |     | 0.44                  |     |      |
|                  | I <sub>OL</sub> = 16 mA                                     | 4.5 V           | 0.55                  |     |     | 0.55                  |     | 0.55                  |     |      |
| I <sub>I</sub>   | V <sub>I</sub> = 5.5 V or GND                               | 0 to 5.5 V      | ±1                    |     |     | ±1                    |     | ±1                    |     | μA   |
| I <sub>OZ</sub>  | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5.5 V           | ±5                    |     |     | ±5                    |     | ±5                    |     | μA   |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           | 20                    |     |     | 20                    |     | 20                    |     | μA   |
| I <sub>off</sub> | V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V               | 0               | 5                     |     |     | 5                     |     | 5                     |     | μA   |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 3.3 V           | 2.5                   |     |     |                       |     |                       |     | pF   |
|                  |                                                             | 5 V             | 2.5                   |     |     |                       |     |                       |     |      |

## 7.6 Switching Characteristics, V<sub>CC</sub> = 2.5 V ± 0.2 V

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| PARAMETER          | FROM (INPUT)           | TO (OUTPUT) | LOAD CAPACITANCE       | T <sub>A</sub> = 25°C |                     |     | –40°C to 85°C |      | –40°C to 125°C |      | UNIT |
|--------------------|------------------------|-------------|------------------------|-----------------------|---------------------|-----|---------------|------|----------------|------|------|
|                    |                        |             |                        | MIN                   | TYP                 | MAX | MIN           | MAX  | MIN            | MAX  |      |
| t <sub>pd</sub>    | A                      | Y           | C <sub>L</sub> = 15 pF | 5.6 <sup>(1)</sup>    | 12 <sup>(1)</sup>   |     | 1             | 14.5 | 1              | 16   | ns   |
| t <sub>en</sub>    | $\overline{\text{OE}}$ | Y           |                        | 7.8 <sup>(1)</sup>    | 17.4 <sup>(1)</sup> |     | 1             | 21   | 1              | 22.5 |      |
| t <sub>dis</sub>   | $\overline{\text{OE}}$ | Y           |                        | 5.7 <sup>(1)</sup>    | 16 <sup>(1)</sup>   |     | 1             | 19   | 1              | 20   |      |
| t <sub>pd</sub>    | A                      | Y           | C <sub>L</sub> = 50 pF | 7.9                   | 16.8                |     | 1             | 18.5 | 1              | 20   | ns   |
| t <sub>en</sub>    | $\overline{\text{OE}}$ | Y           |                        | 10.1                  | 22.2                |     | 1             | 25.5 | 1              | 27   |      |
| t <sub>dis</sub>   | $\overline{\text{OE}}$ | Y           |                        | 8.1                   | 22.3                |     | 1             | 25.5 | 1              | 26.5 |      |
| t <sub>sk(o)</sub> |                        |             |                        |                       |                     | 2   |               | 2    |                | 3    |      |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 7.7 Switching Characteristics, V<sub>CC</sub> = 3.3 V ± 0.3 V

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| PARAMETER          | FROM (INPUT)           | TO (OUTPUT) | LOAD CAPACITANCE       | T <sub>A</sub> = 25°C |                     |     | –40°C to 85°C |      | –40°C to 125°C |      | UNIT |
|--------------------|------------------------|-------------|------------------------|-----------------------|---------------------|-----|---------------|------|----------------|------|------|
|                    |                        |             |                        | MIN                   | TYP                 | MAX | MIN           | MAX  | MIN            | MAX  |      |
| t <sub>pd</sub>    | A                      | Y           | C <sub>L</sub> = 15 pF | 4.1 <sup>(1)</sup>    | 7 <sup>(1)</sup>    |     | 1             | 8.5  | 1              | 9.5  | ns   |
| t <sub>en</sub>    | $\overline{\text{OE}}$ | Y           |                        | 5.6 <sup>(1)</sup>    | 10.5 <sup>(1)</sup> |     | 1             | 12.5 | 1              | 14   |      |
| t <sub>dis</sub>   | $\overline{\text{OE}}$ | Y           |                        | 4.2 <sup>(1)</sup>    | 10.5 <sup>(1)</sup> |     | 1             | 12.5 | 1              | 13.5 |      |
| t <sub>pd</sub>    | A                      | Y           | C <sub>L</sub> = 50 pF | 5.8                   | 10.5                |     | 1             | 12   | 1              | 13   | ns   |
| t <sub>en</sub>    | $\overline{\text{OE}}$ | Y           |                        | 7.3                   | 14                  |     | 1             | 16   | 1              | 17.5 |      |
| t <sub>dis</sub>   | $\overline{\text{OE}}$ | Y           |                        | 5.8                   | 15.4                |     | 1             | 17.5 | 1              | 18.5 |      |
| t <sub>sk(o)</sub> |                        |             |                        |                       |                     | 1.5 |               | 1.5  |                | 2    |      |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 7.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER   | FROM<br>(INPUT)        | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |                    |                    | $-40^\circ\text{C to } 85^\circ\text{C}$ |      | $-40^\circ\text{C to } 125^\circ\text{C}$ |      | UNIT |
|-------------|------------------------|----------------|----------------------|--------------------------|--------------------|--------------------|------------------------------------------|------|-------------------------------------------|------|------|
|             |                        |                |                      | MIN                      | TYP                | MAX                | MIN                                      | MAX  | MIN                                       | MAX  |      |
| $t_{pd}$    | A                      | Y              | $C_L = 15\text{ pF}$ |                          | 3 <sup>(1)</sup>   | 5 <sup>(1)</sup>   | 1                                        | 6    | 1                                         | 7    | ns   |
| $t_{en}$    | $\overline{\text{OE}}$ | Y              |                      |                          | 4.1 <sup>(1)</sup> | 7.2 <sup>(1)</sup> | 1                                        | 8.5  | 1                                         |      |      |
| $t_{dis}$   | $\overline{\text{OE}}$ | Y              |                      |                          | 2.9 <sup>(1)</sup> | 7 <sup>(1)</sup>   | 1                                        | 8    | 1                                         | 9    |      |
| $t_{pd}$    | A                      | Y              | $C_L = 50\text{ pF}$ |                          | 4.2                | 7                  | 1                                        | 8    | 1                                         | 9    | ns   |
| $t_{en}$    | $\overline{\text{OE}}$ | Y              |                      |                          | 5.3                | 9.2                | 1                                        | 10.5 | 1                                         | 11.5 |      |
| $t_{dis}$   | $\overline{\text{OE}}$ | Y              |                      |                          | 3.5                | 8.8                | 1                                        | 10   | 1                                         | 11   |      |
| $t_{sk(o)}$ |                        |                |                      |                          |                    | 1                  |                                          | 1    |                                           | 1.5  |      |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 7.9 Noise Characteristics<sup>(1)</sup>

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER   |                                        | SN74LV540A |      |      | UNIT |
|-------------|----------------------------------------|------------|------|------|------|
|             |                                        | MIN        | TYP  | MAX  |      |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ |            | 0.5  | 0.8  | V    |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ |            | -0.3 | -0.8 | V    |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ |            | 3    |      | V    |
| $V_{IH(D)}$ | High-level dynamic input voltage       |            | 2.3  |      | V    |
| $V_{IL(D)}$ | Low-level dynamic input voltage        |            |      | 0.97 | V    |

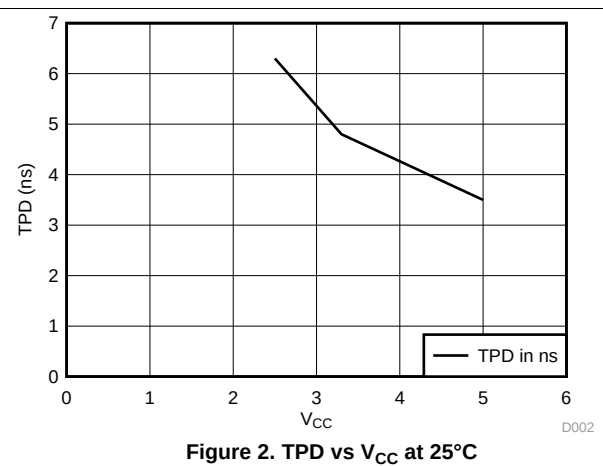
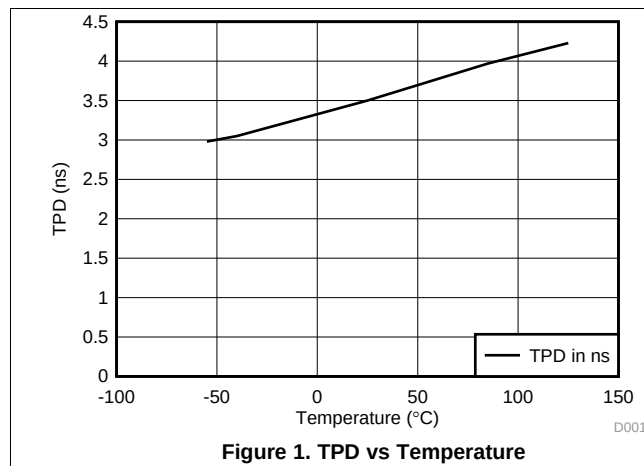
(1) Characteristics are for surface-mount packages only.

## 7.10 Operating Characteristics

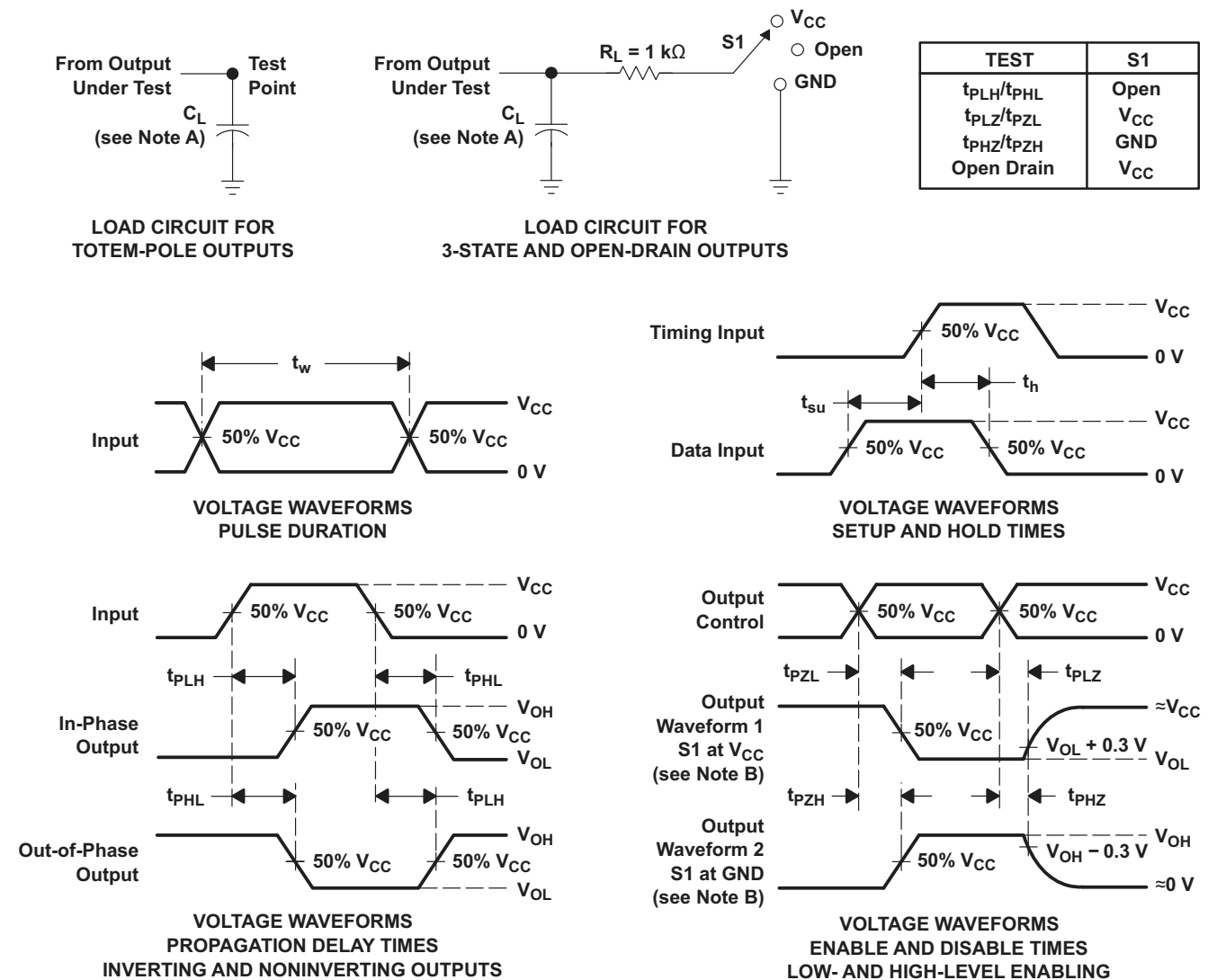
$T_A = 25^\circ\text{C}$

| PARAMETER |                               | TEST CONDITIONS |                                            | $V_{CC}$ | TYP | UNIT |
|-----------|-------------------------------|-----------------|--------------------------------------------|----------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | Outputs enabled | $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$ | 3.3 V    | 10  | pF   |
|           |                               | Outputs enabled |                                            | 5 V      | 11  |      |

## 7.11 Typical Characteristics



## 8 Parameter Measurement Information



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**



## 9 Detailed Description

### 9.1 Overview

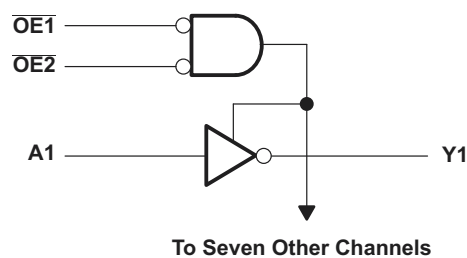
The SN74LV540A device is an octal buffer/driver designed for 2-V to 5.5-V  $V_{CC}$  operation.

This device is ideal for driving bus lines or buffer memory address registers. It features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that, if either output enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down-voltage translation
  - Inputs accept voltages to 5.5 V
- Slow edges reduce output ringing
- $I_{off}$  feature
  - Allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V

### 9.4 Device Functional Modes

**Table 1. Function Table  
(Each Buffer/Driver)**

| INPUTS           |                  |   | OUTPUT<br>Y |
|------------------|------------------|---|-------------|
| $\overline{OE1}$ | $\overline{OE2}$ | A |             |
| L                | L                | L | H           |
| L                | L                | H | L           |
| H                | X                | X | Z           |
| X                | H                | X | Z           |

## 10 Application and Implementation

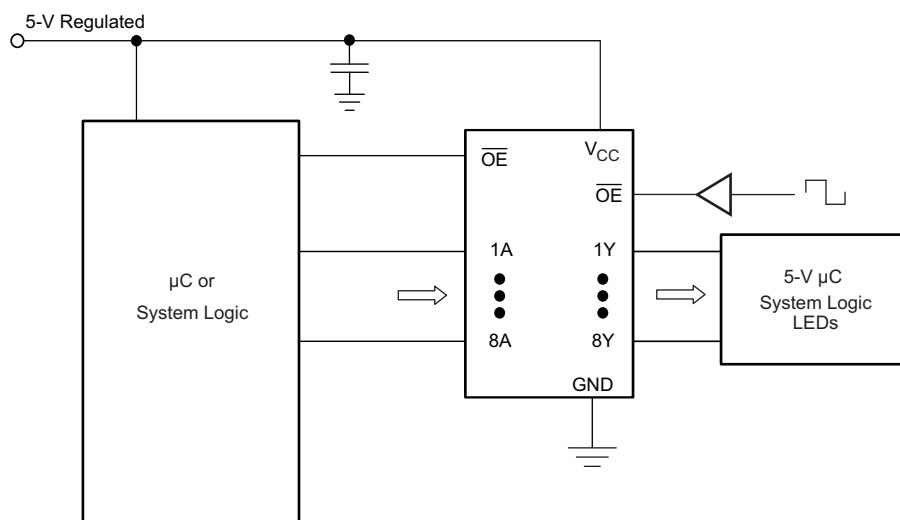
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The SN74LV540A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid  $V_{CC}$ . This feature makes it ideal for translating down to the  $V_{CC}$  level. [Figure 5](#) shows the reduction in ringing compared to higher drive parts such as AC.

### 10.2 Typical Application



**Figure 4. Typical Application Schematic**

#### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - For rise time and fall time specifications, see  $\Delta t/\Delta V$  in the [Recommended Operating Conditions](#) table.
  - For specified High and low levels, see  $V_{IH}$  and  $V_{IL}$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommend Output Conditions
  - Load currents should not exceed 35 mA per output and 70 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 10.2.3 Application Curves

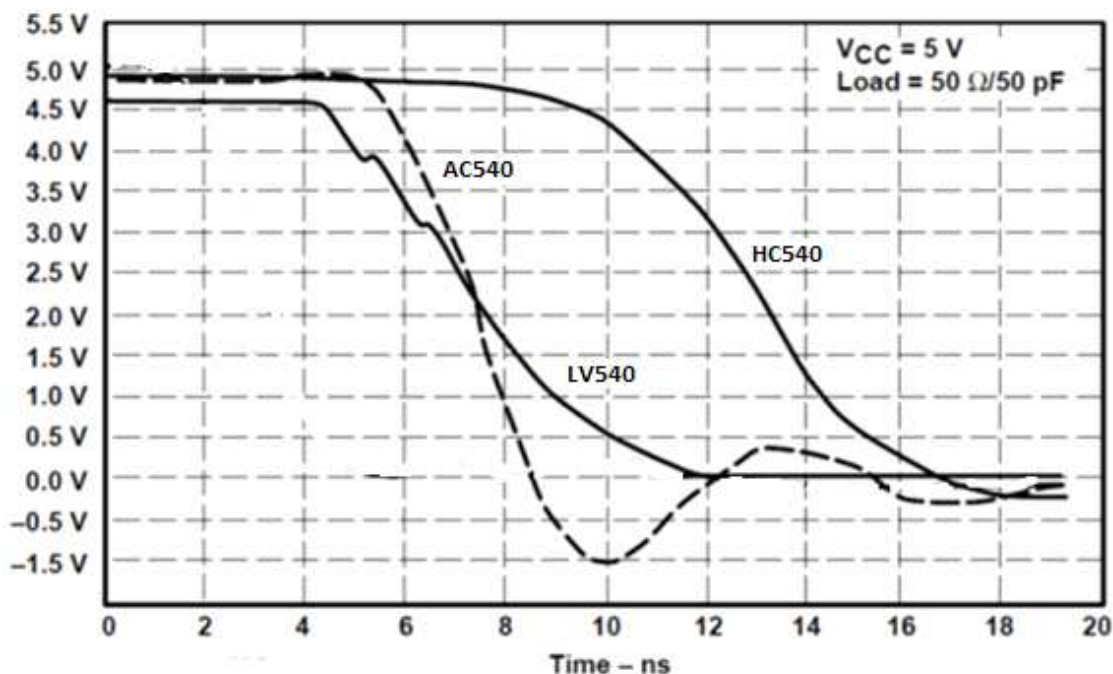


Figure 5. Switching Characteristics Comparison

## 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 6](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

### 12.2 Layout Example

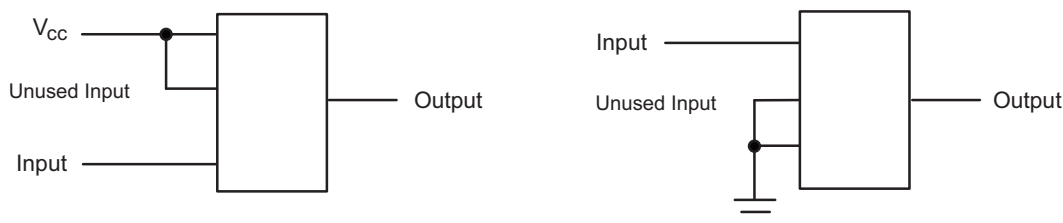


Figure 6. Layout Diagram

## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS      | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN74LV540A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 13.2 Trademarks

All trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LV540ADBR    | ACTIVE        | SSOP         | DB                 | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LV540A                  | <a href="#">Samples</a> |
| SN74LV540ADGVR   | ACTIVE        | TVSOP        | DGV                | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LV540A                  | <a href="#">Samples</a> |
| SN74LV540ADW     | ACTIVE        | SOIC         | DW                 | 20   | 25             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LV540A                  | <a href="#">Samples</a> |
| SN74LV540ADWR    | ACTIVE        | SOIC         | DW                 | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LV540A                  | <a href="#">Samples</a> |
| SN74LV540ANSR    | ACTIVE        | SO           | NS                 | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 74LV540A                | <a href="#">Samples</a> |
| SN74LV540ANSRE4  | ACTIVE        | SO           | NS                 | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 74LV540A                | <a href="#">Samples</a> |
| SN74LV540APW     | ACTIVE        | TSSOP        | PW                 | 20   | 70             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LV540A                  | <a href="#">Samples</a> |
| SN74LV540APWR    | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LV540A                  | <a href="#">Samples</a> |
| SN74LV540ARGYR   | ACTIVE        | VQFN         | RGY                | 20   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | LV540A                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

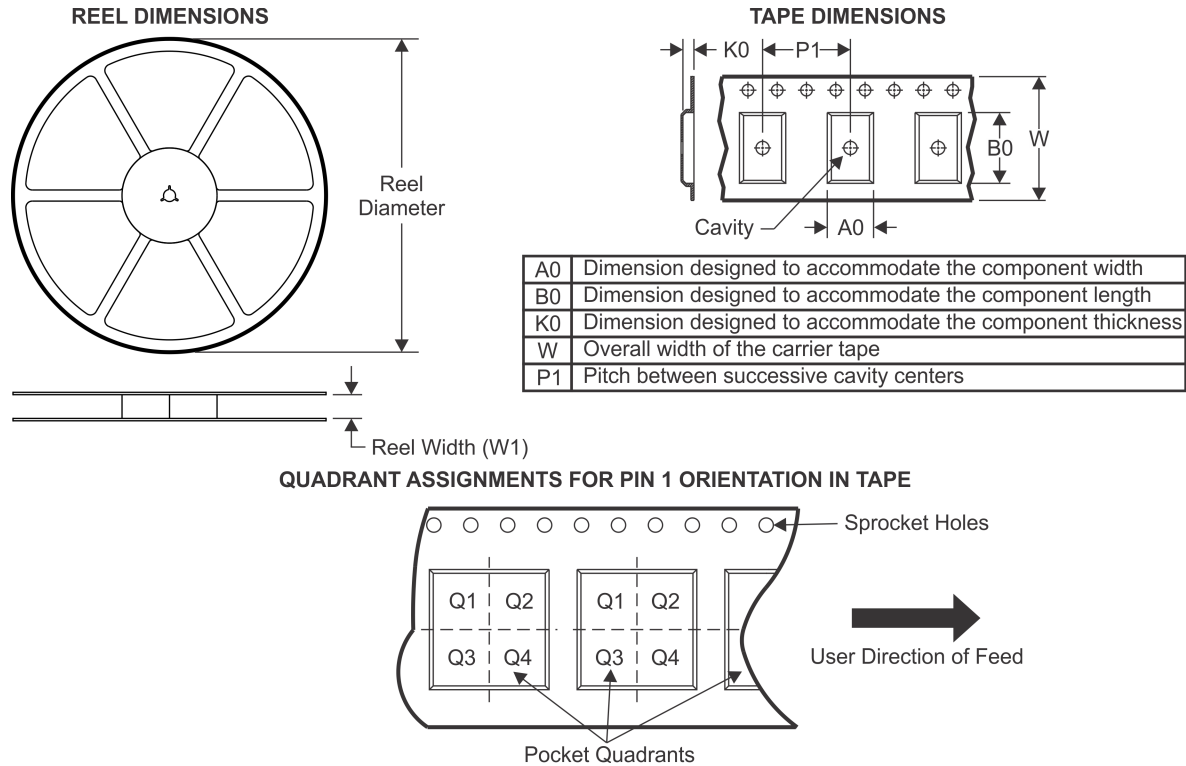
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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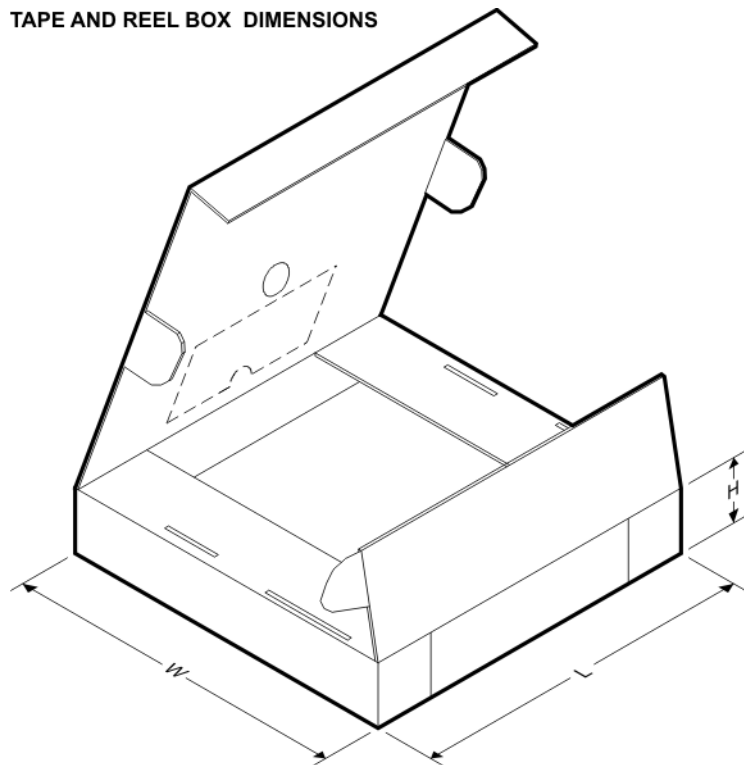
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV540ADBR  | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LV540ADGVR | TVSOP        | DGV             | 20   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV540ADWR  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LV540ANSR  | SO           | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74LV540APWR  | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74LV540ARGYR | VQFN         | RGY             | 20   | 3000 | 330.0              | 12.4               | 3.8     | 4.8     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

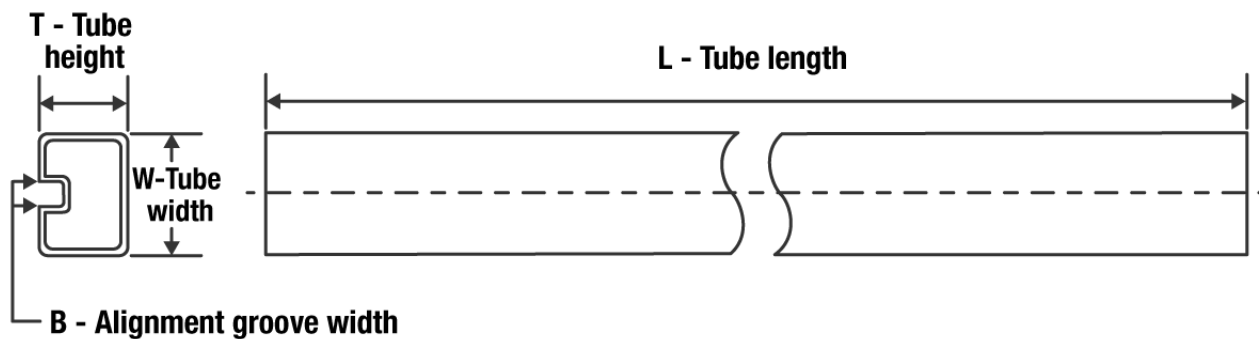


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV540ADBR  | SSOP         | DB              | 20   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74LV540ADGVR | TVSOP        | DGV             | 20   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74LV540ADWR  | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LV540ANSR  | SO           | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LV540APWR  | TSSOP        | PW              | 20   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74LV540ARGYR | VQFN         | RGY             | 20   | 3000 | 853.0       | 449.0      | 35.0        |



## TUBE



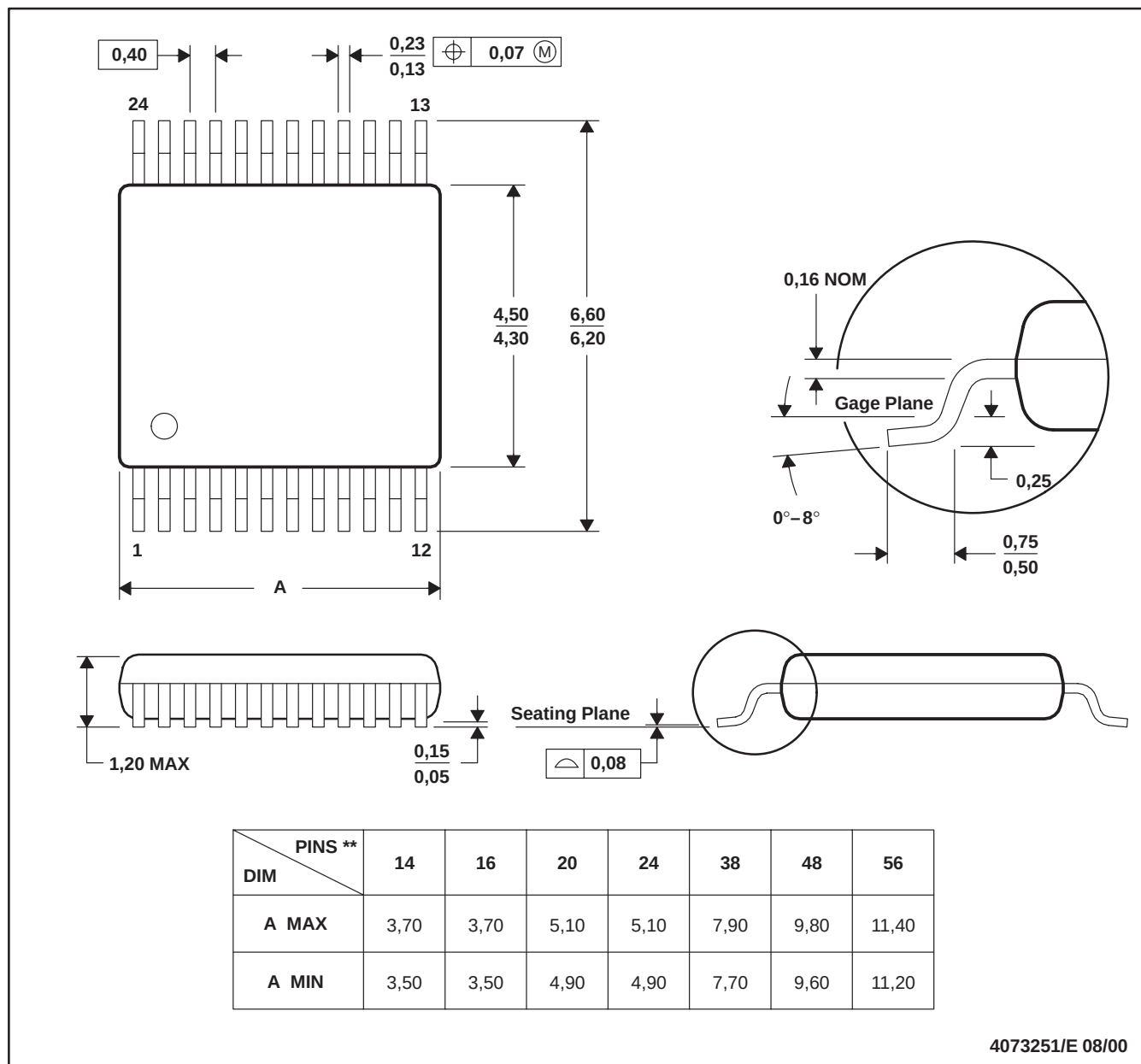
\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LV540ADW | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74LV540APW | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## GENERIC PACKAGE VIEW

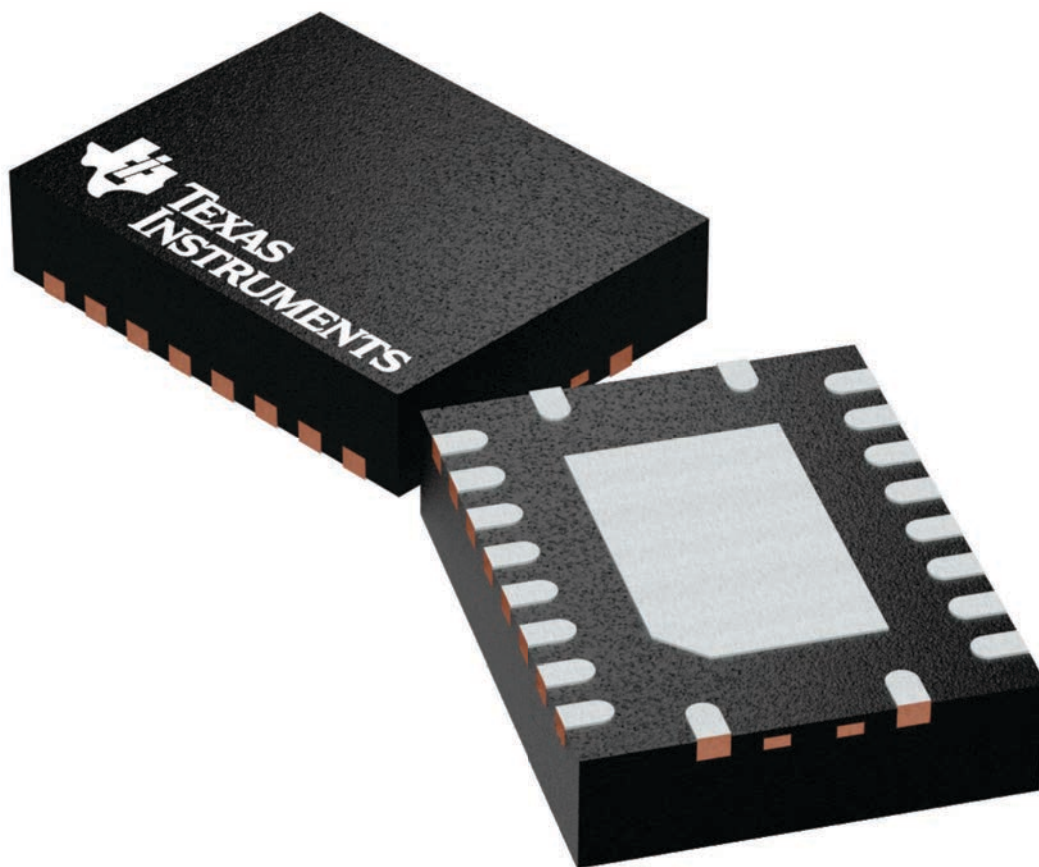
**RGY 20**

**VQFN - 1 mm max height**

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



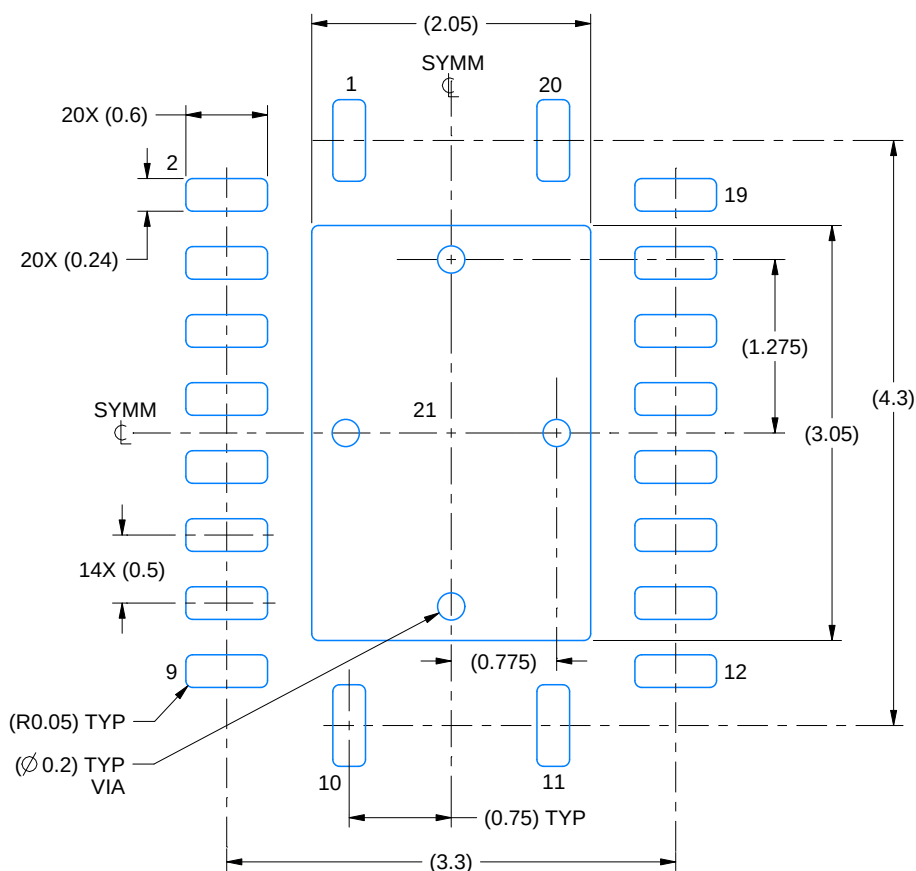
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

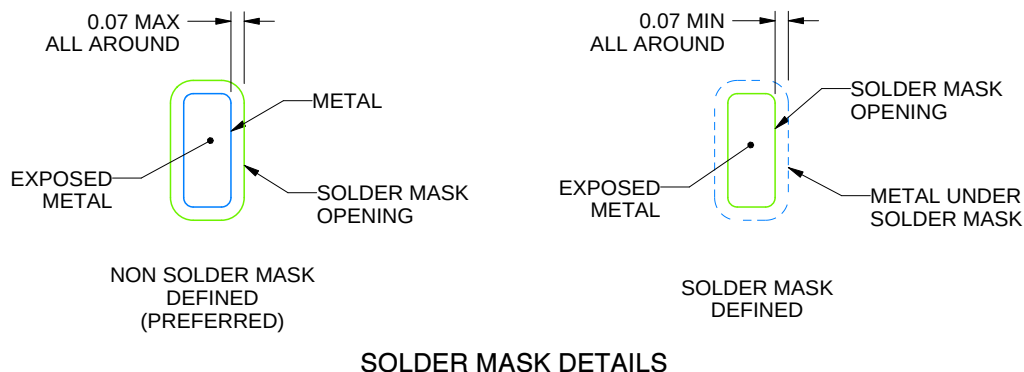
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

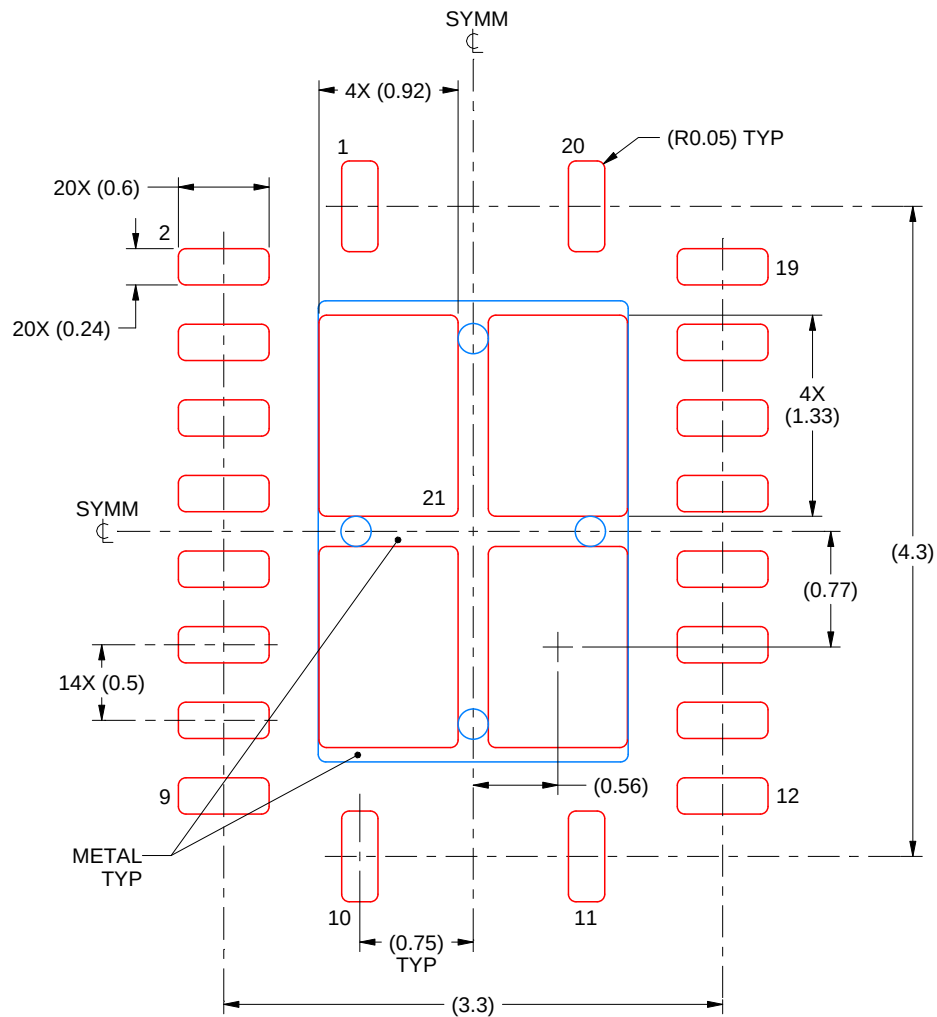
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



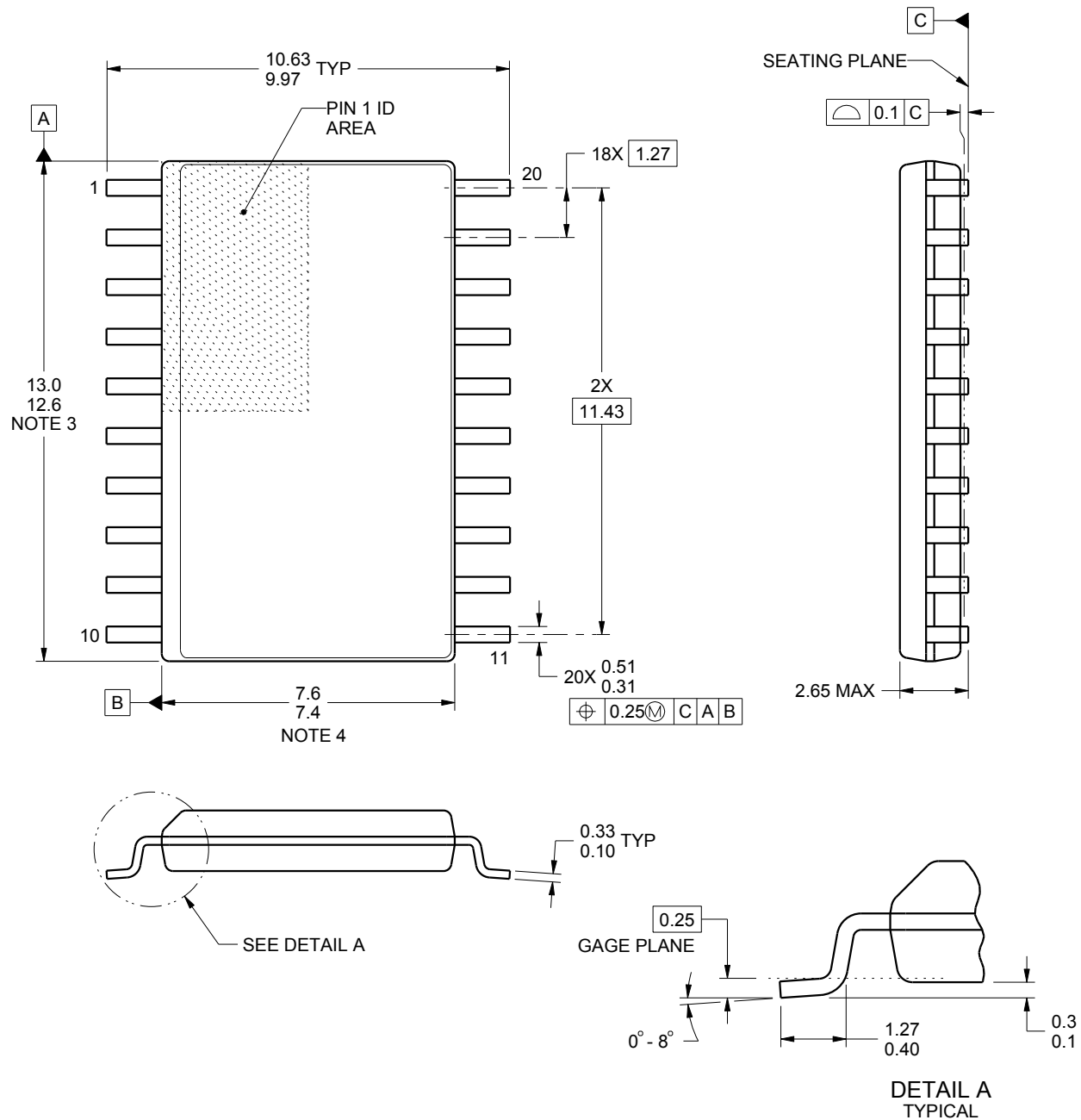
**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220724/A 05/2016

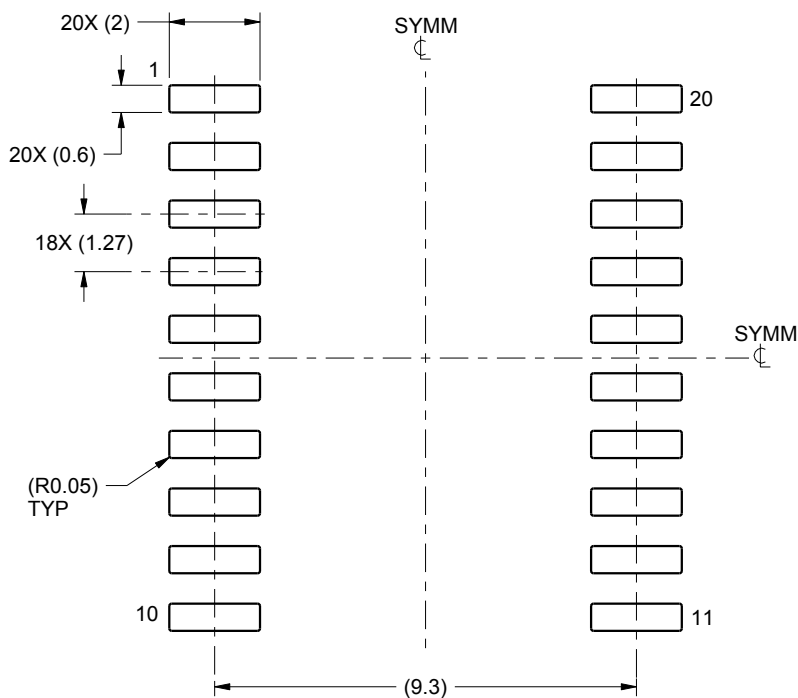
## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

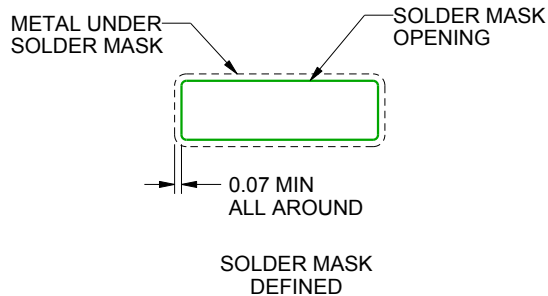
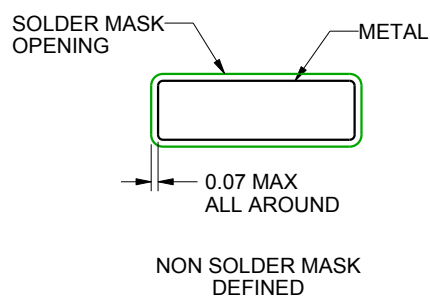
**DW0020A**

### SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



## SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

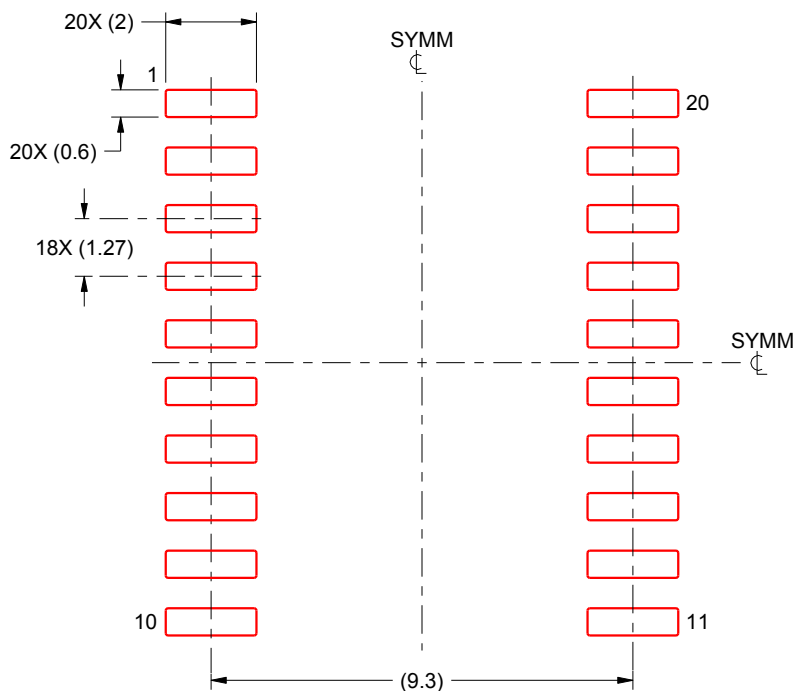


## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC

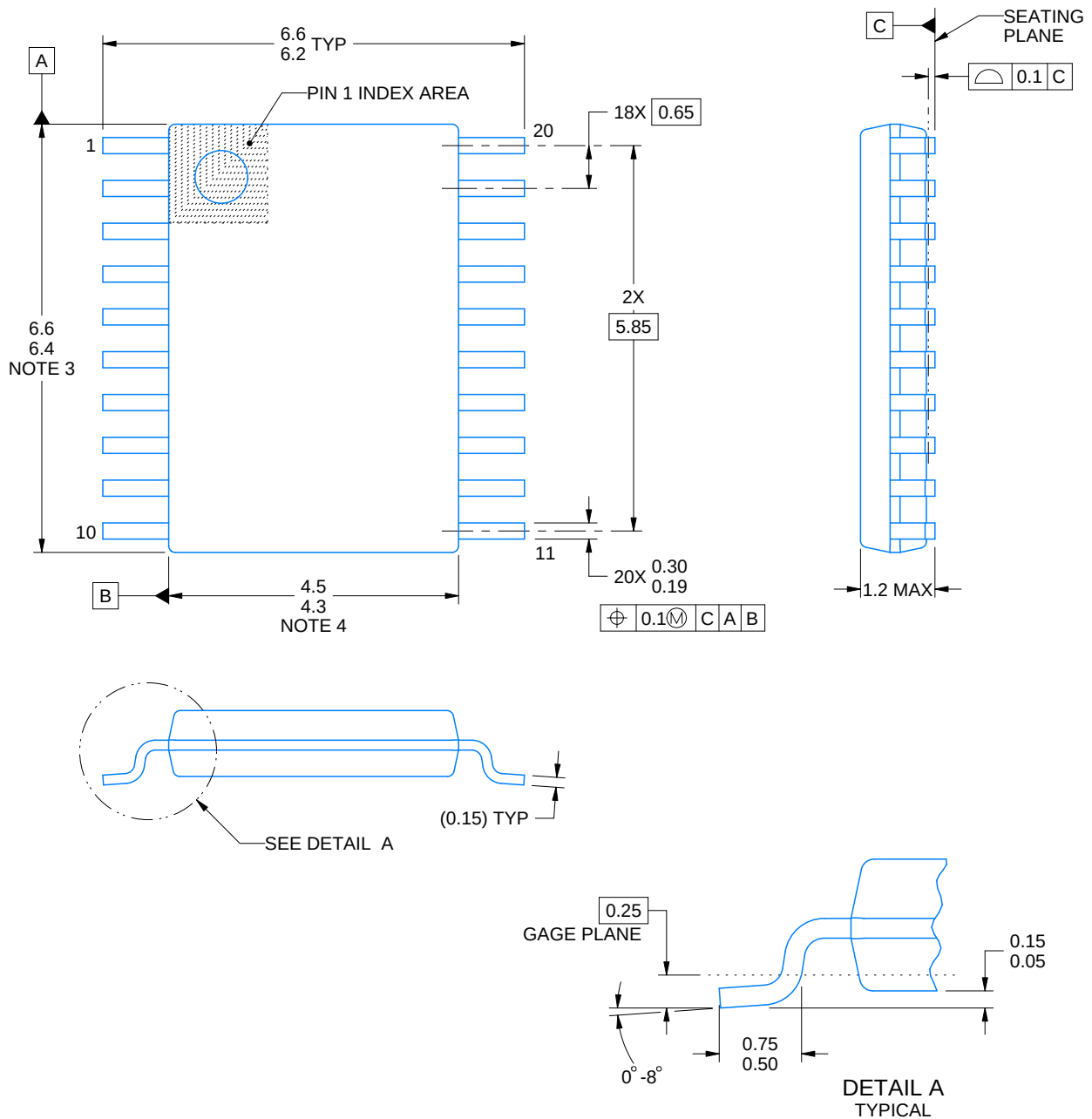
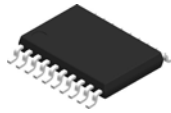


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220206/A 02/2017

## NOTES:

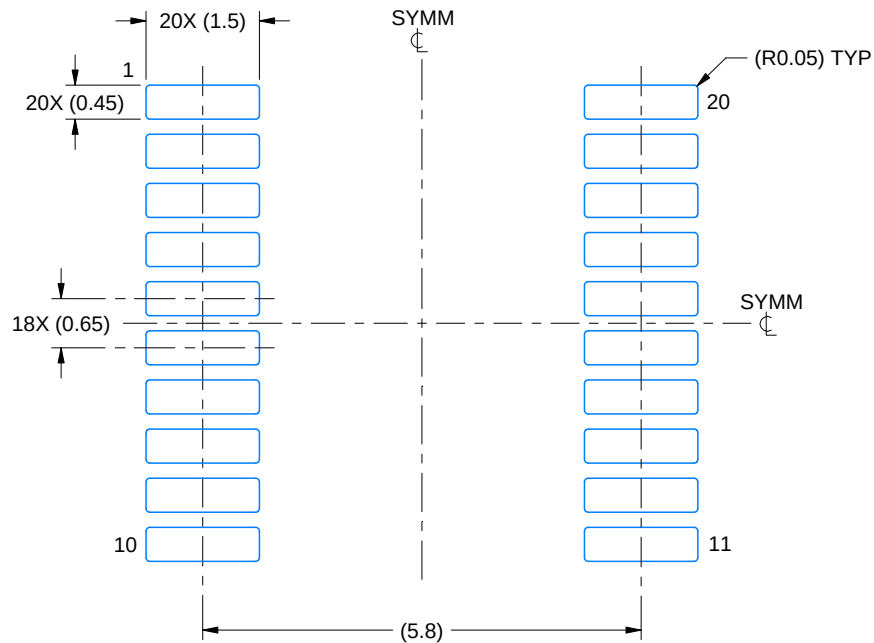
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

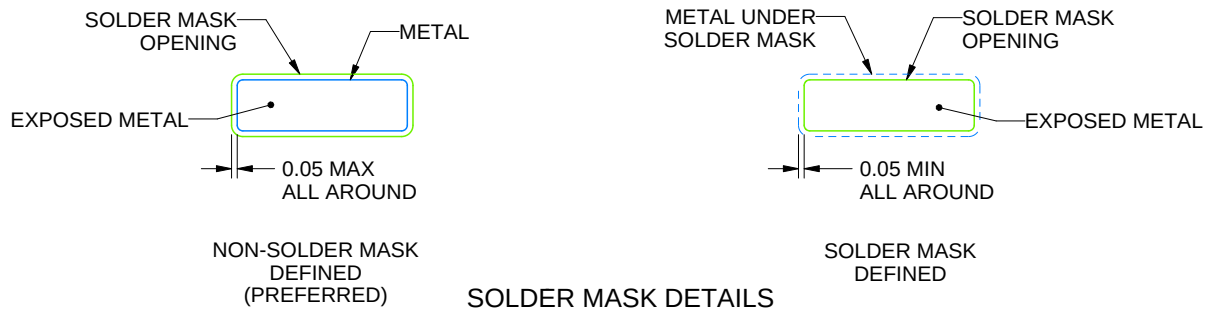
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

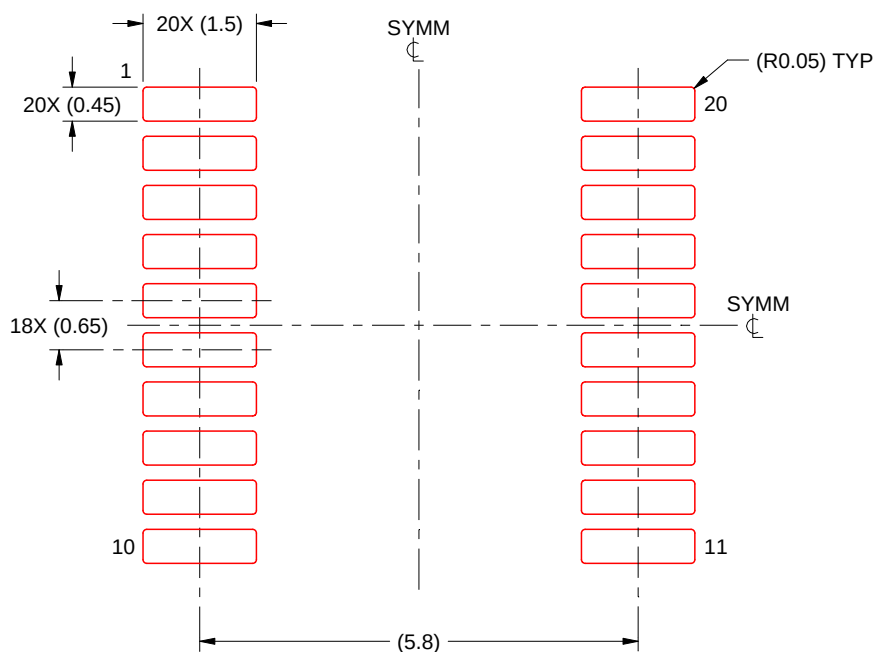
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

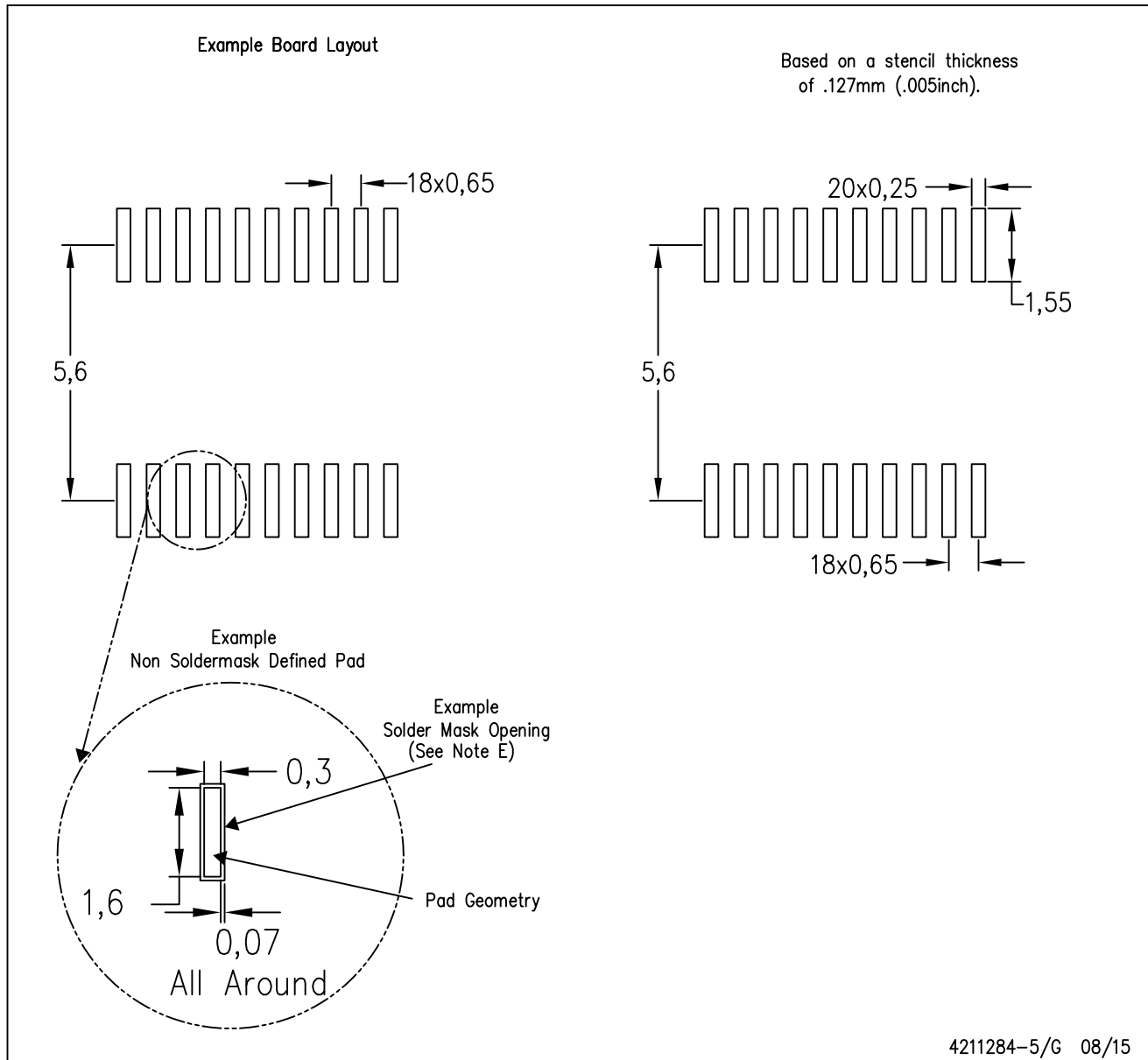
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

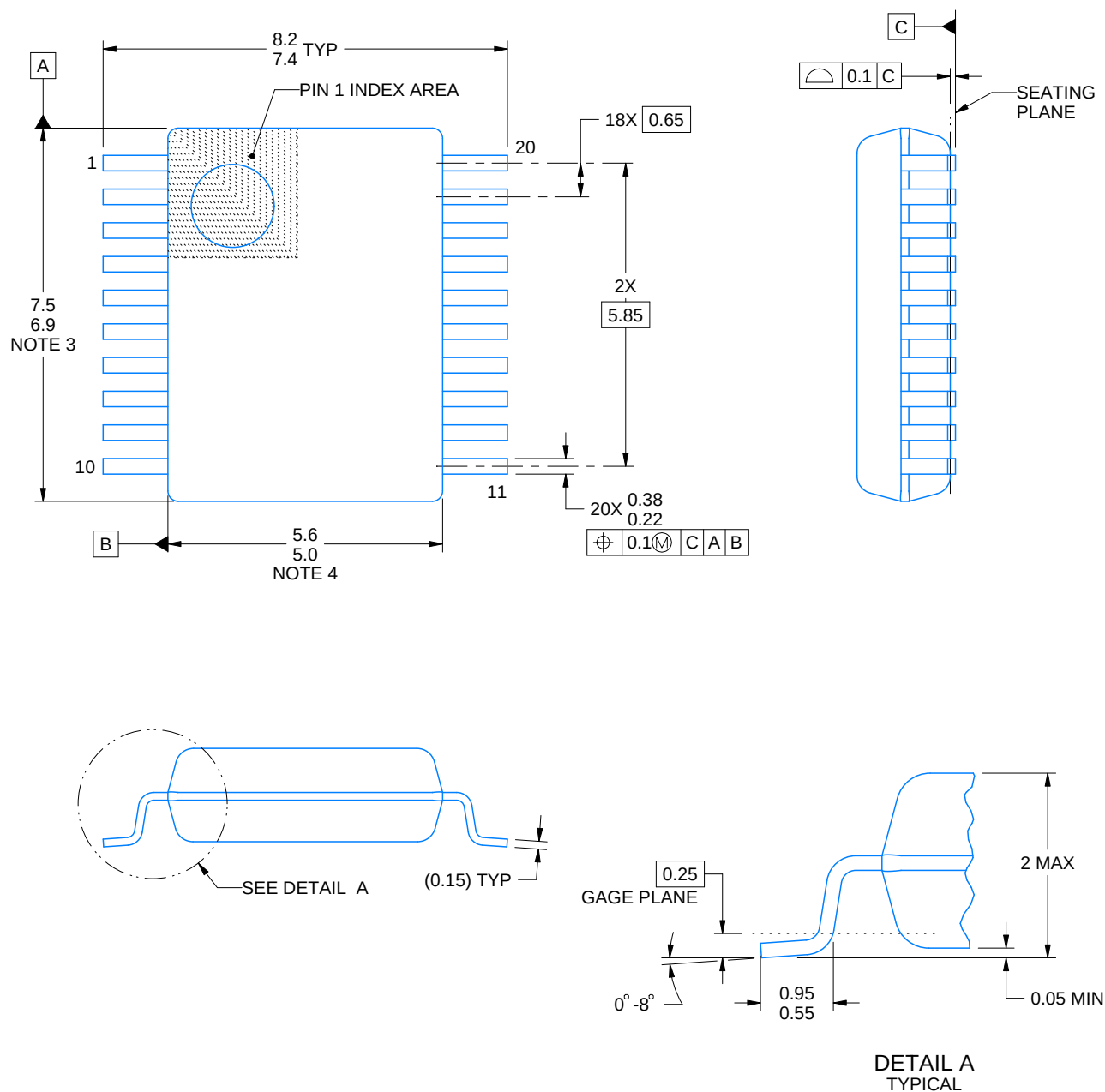


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## SSOP - 2 mm max height

## SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

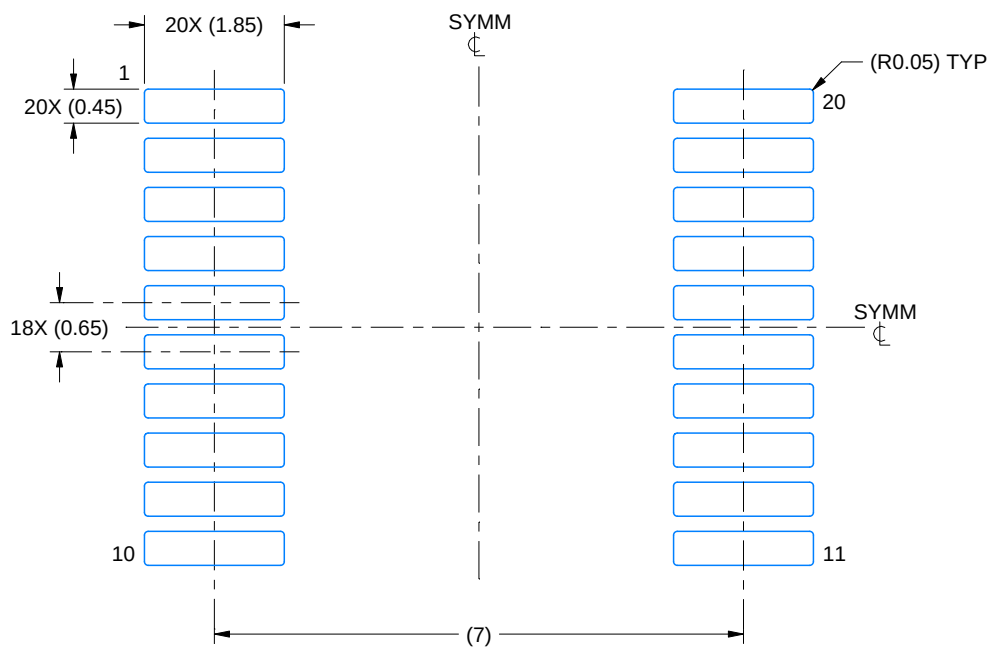
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

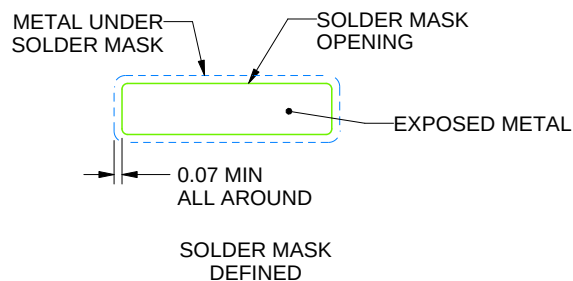
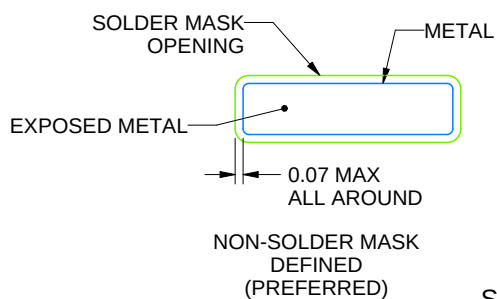
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

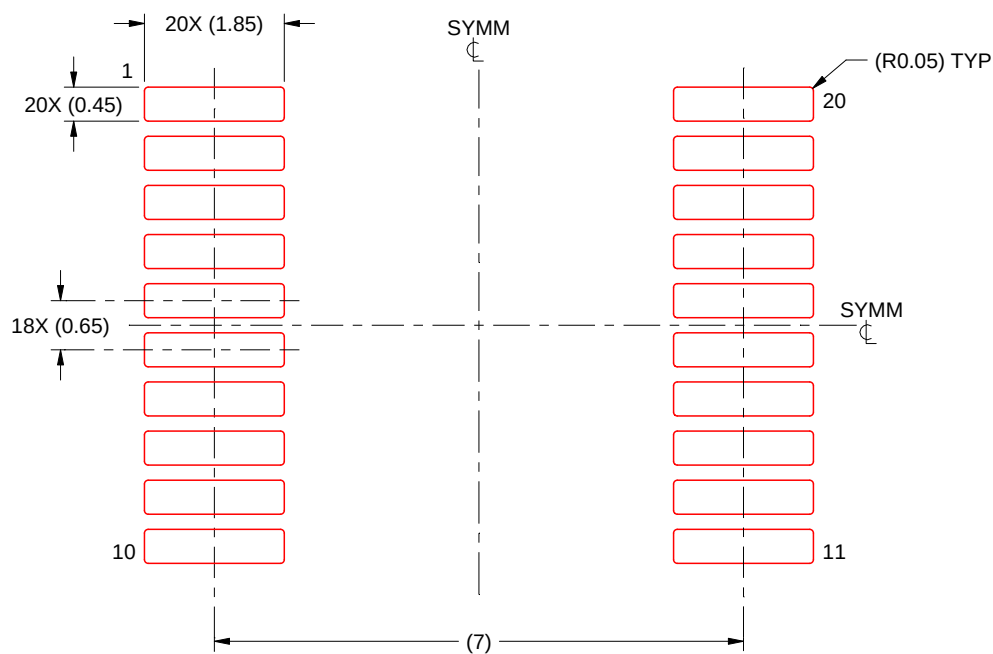
6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**DB0020A**

## SSOP - 2 mm max height

## SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

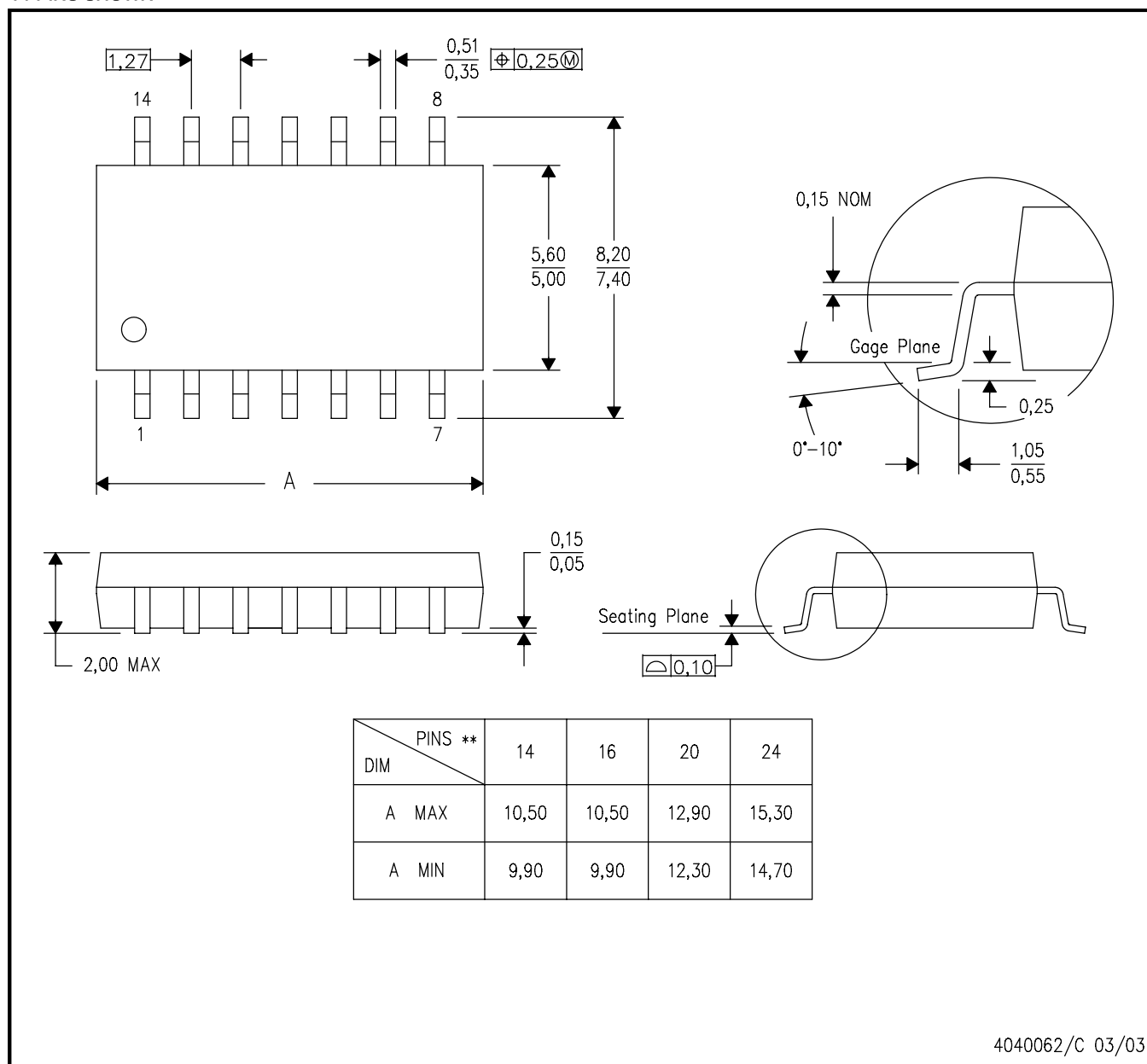


# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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