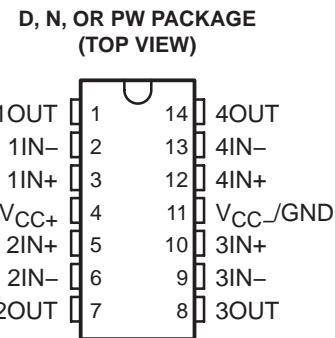


- Low Offset . . . 3 mV (Max) for A-Grade
- Wide Gain-Bandwidth Product . . . 4 MHz
- High Slew Rate . . . 13 V/μs
- Fast Settling Time . . . 1.1 μs to 0.1%
- Wide-Range Single-Supply Operation . . . 4 V to 36 V
- Wide Input Common-Mode Range Includes Ground (V_{CC-})
- Low Total Harmonic Distortion . . . 0.02%
- Large-Capacitance Drive Capability . . . 10,000 pF
- Output Short-Circuit Protection
- Alternative to MC33074/A and MC34074/A



description/ordering information

ORDERING INFORMATION

| T_A | $V_{IO\max}$ AT 25°C | PACKAGE [†] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|--|--------------------------|----------------------|--------------|--------------------------|---------------------|
| 0°C to 70°C | A-grade: 3 mV | PDIP (N) | Tube of 25 | TL3474ACN | TL3474ACN |
| | | SOIC (D) | Tube of 50 | TL3474ACD | |
| | | TSSOP (PW) | Reel of 2500 | TL3474ACDR | TL3474A |
| | | TSSOP (PW) | Tube of 90 | TL3474ACPW | |
| | Standard grade: 10 mV | TSSOP (PW) | Reel of 2000 | TL3474ACPWR | T3474A |
| | | PDIP (N) | Tube of 25 | TL3474CN | TL3474CN |
| | | SOIC (D) | Tube of 50 | TL3474CD | |
| | | TSSOP (PW) | Reel of 2500 | TL3474CDR | TL3474C |
| | | TSSOP (PW) | Tube of 90 | TL3474CPW | |
| | | TSSOP (PW) | Reel of 2000 | TL3474CPWR | TL3474 |
| -40°C to 105°C | A-grade: 3 mV | PDIP (N) | Tube of 25 | TL3474AIN | Z3474A |
| | | SOIC (D) | Tube of 50 | TL3474AID | |
| | | TSSOP (PW) | Reel of 2500 | TL3474AIDR | TL3474AI |
| | | TSSOP (PW) | Tube of 90 | TL3474AIPW | |
| | Standard grade: 10 mV | TSSOP (PW) | Reel of 2000 | TL3474AIPWR | Z3474A |
| | | PDIP (N) | Tube of 25 | TL3474IN | TL3474IN |
| | | SOIC (D) | Tube of 50 | TL3474ID | |
| | | TSSOP (PW) | Reel of 2500 | TL3474IDR | TL3474I |
| | | TSSOP (PW) | Tube of 90 | TL3474IPW | |
| | | TSSOP (PW) | Reel of 2000 | TL3474IPWR | Z3474 |

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

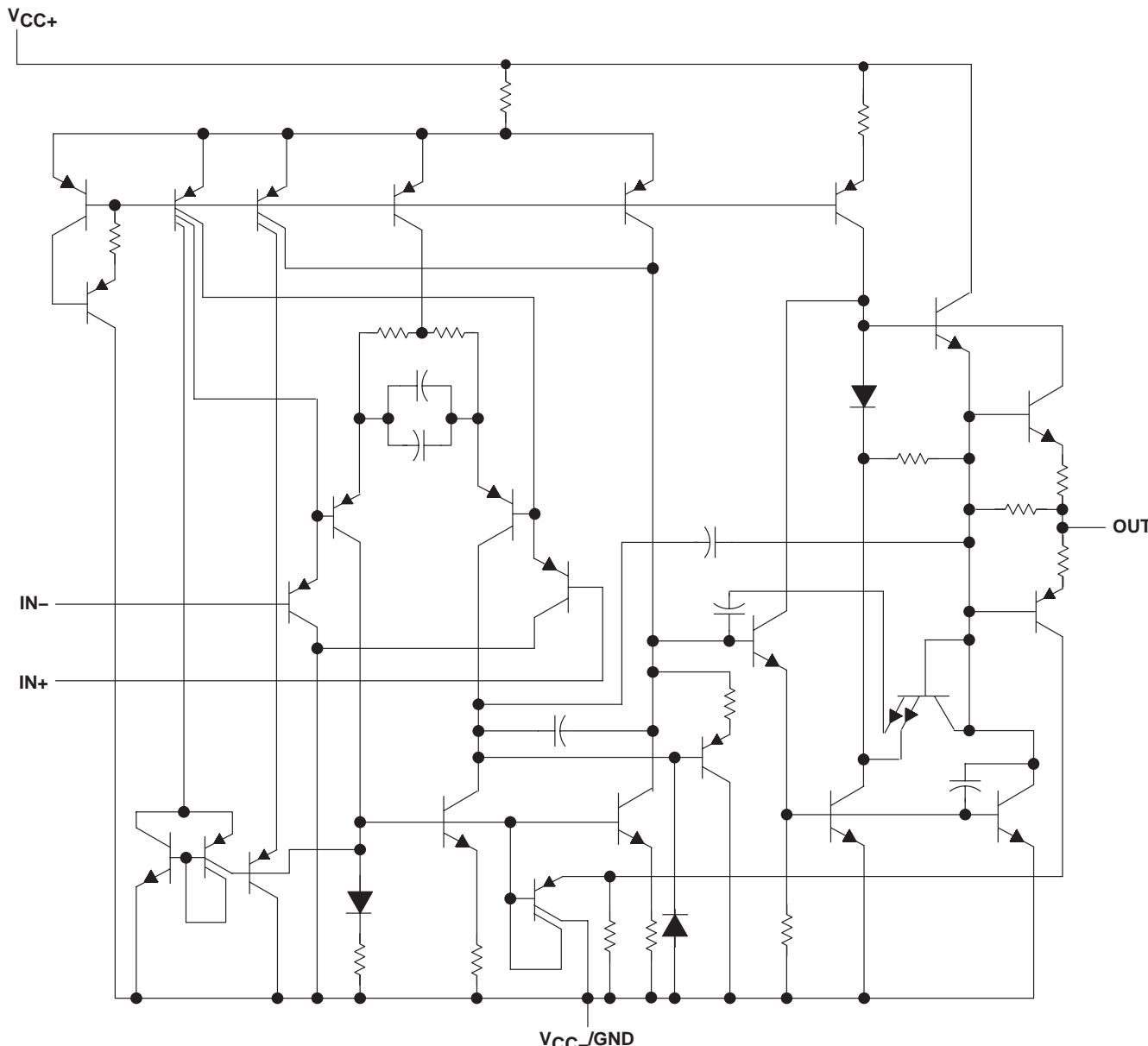
TL3474, TL3474A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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description/ordering information (continued)

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3474, TL3474A operational amplifiers. These devices offer 4 MHz of gain-bandwidth product, 13-V/ μ s slew rate, and fast settling time without the use of JFET device technology. Although the TL3474 and TL3474A can be operated from split supplies, they are particularly suited for single-supply operation because the common-mode input voltage range includes ground potential (V_{CC-}). With a Darlington transistor input stage, these devices exhibit high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. These low-cost amplifiers are an alternative to the MC34074/A and MC33074/A operational amplifiers.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage: V_{CC+} (see Note 1) | 18 V |
| V_{CC-} | -18 V |
| Differential input voltage, V_{ID} (see Note 2) | ±36 V |
| Input voltage, V_I (any input) | $V_{CC\pm}$ |
| Input current, I_I (each input) | ±1 mA |
| Output current, I_O | ±80 mA |
| Total current into V_{CC+} | 80 mA |
| Total current out of V_{CC-} | 80 mA |
| Duration of short-circuit current at (or below) 25°C (see Note 3) | Unlimited |
| Package thermal impedance, θ_{JA} (see Notes 4 and 5): D package | 86°C/W |
| N package | 80°C/W |
| PW package | 113°C/W |
| Operating virtual junction temperature, T_J | 150°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds | 260°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}/GND .
 2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive input current can flow when the input is less than $V_{CC-} - 0.3$ V.
 3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
 4. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

| | | MIN | MAX | UNIT |
|-------------|--------------------------------|------------------------|-----|------|
| $V_{CC\pm}$ | Supply voltage | 4 | 36 | V |
| V_{IC} | Common-mode input voltage | $V_{CC} = 5$ V | 0 | 2.8 |
| | | $V_{CC\pm} = \pm 15$ V | -15 | 12.8 |
| T_A | Operating free-air temperature | TL3474C, TL3474AC | 0 | 70 |
| | | TL3474I, TL3474AI | -40 | 105 |

TL3474, TL3474A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | TA | TL3474 | | | TL3474A | | | UNIT |
|---|---|-------------------------|-------------|-------|-------|---------|-------|-------|-------|
| | | | MIN | TYPT† | MAX | MIN | TYPT† | MAX | |
| V _{IO} Input offset voltage | V _{IC} = 0, V _O = 0, R _S = 50 Ω | V _{CC} = 5 V | 25°C | 1.5 | 10 | 1.5 | 3 | 3 | mV |
| | | V _{CC} = ±15 V | 25°C | 1.0 | 10 | 1.0 | 3 | 3 | |
| | | Full range‡ | | 12 | | | 5 | 5 | |
| αV _{IO} Temperature coefficient of input offset voltage | V _{IC} = 0, V _O = 0, R _S = 50 Ω | V _{CC} = ±15 V | Full range‡ | | 10 | | 10 | 10 | μV/°C |
| | | V _{CC} = ±15 V | 25°C | 6 | 75 | 6 | 75 | 75 | |
| I _{IO} Input offset current | V _{IC} = 0, V _O = 0, R _S = 50 Ω | V _{CC} = ±15 V | Full range‡ | | 300 | | 300 | 300 | nA |
| | | V _{CC} = ±15 V | 25°C | 100 | 500 | 100 | 500 | 500 | |
| I _{IB} Input bias current | V _{IC} = 0, V _O = 0, R _S = 50 Ω | V _{CC} = ±15 V | Full range‡ | | 700 | | 700 | 700 | nA |
| | | | 25°C | –15 | to | –15 | to | 12.8 | |
| V _{ICR} Common-mode input voltage range | R _S = 50 Ω | | Full range‡ | –15 | to | –15 | to | 12.8 | V |
| | | | 25°C | –15 | to | –15 | to | 12.8 | |
| V _{OH} High-level output voltage | V _{CC+} = 5 V, V _{CC–} = 0, R _L = 2 kΩ | | 25°C | 3.7 | 4 | 3.7 | 4 | 4 | V |
| | R _L = 10 kΩ | | 25°C | 13.6 | 14 | 13.6 | 14 | 14 | |
| | R _L = 2 kΩ | | Full range‡ | 13.4 | | 13.4 | | 13.4 | |
| V _{OL} Low-level output voltage | V _{CC+} = 5 V, V _{CC–} = 0, R _L = 2 kΩ | | 25°C | 0.1 | 0.3 | 0.1 | 0.3 | 0.3 | V |
| | R _L = 10 kΩ | | 25°C | –14.7 | –14.3 | –14.7 | –14.3 | –14.3 | |
| | R _L = 2 kΩ | | Full range‡ | | –13.5 | | –13.5 | –13.5 | |
| A _{VD} Large-signal differential voltage amplification | V _O = ±10 V, R _L = 2 kΩ | | 25°C | 25 | 100 | 25 | 100 | 100 | V/mV |
| | | | Full range‡ | 20 | | 20 | | 20 | |
| I _{OS} Short-circuit output current | Source: V _{ID} = 1 V, V _O = 0 | 25°C | –10 | –34 | | –10 | –34 | –34 | mA |
| | Sink: V _{ID} = –1 V, V _O = 0 | | 20 | 27 | | 20 | 27 | 27 | |
| CMRR Common-mode rejection ratio | V _{IC} = V _{ICR} (min), R _S = 50 Ω | 25°C | 65 | 97 | | 80 | 97 | 97 | dB |
| k _{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$) | V _{CC±} = ±13.5 V to ±16.5 V, R _S = 100 Ω | 25°C | 70 | 97 | | 70 | 97 | 97 | dB |
| I _{CC} Supply current (per channel) | V _O = 0, No load | 25°C | 3.5 | 4.5 | | 3.5 | 4.5 | 4.5 | mA |
| | | Full range‡ | 4.5 | 5.5 | | 4.5 | 5.5 | 5.5 | |
| | V _{CC+} = 5 V, V _O = 2.5 V, V _{CC–} = 0, No load | 25°C | 3.5 | 4.5 | | 3.5 | 4.5 | 4.5 | |

† All typical values are at $T_A = 25^\circ\text{C}$.

‡ Full range is 0°C to 70°C for the TL3474C, TL3474AC devices and –40°C to 105°C for the TL3474I, TL3474AI devices.

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operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TL3474 | | | TL3474A | | | UNIT |
|-------------|---|---|-----|------|---------|------|-----|------------------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR+ | Positive slew rate $V_I = -10$ V to 10 V, $R_L = 2 \text{ k}\Omega$, $C_L = 300 \text{ pF}$ | $A_V = 1$ | 8 | 10 | 8 | 10 | | $\text{V}/\mu\text{s}$ |
| SR- | Negative slew rate | $A_V = -1$ | | 13 | | 13 | | |
| t_s | Settling time $A_{VD} = -1$, 10-V step | To 0.1% | | 1.1 | | 1.1 | | μs |
| | | To 0.01% | | 2.2 | | 2.2 | | |
| V_n | Equivalent input noise voltage $f = 1$ kHz, | $R_S = 100 \Omega$ | | 49 | | 49 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| I_n | Equivalent input noise current | $f = 1$ kHz | | 0.22 | | 0.22 | | $\text{pA}/\sqrt{\text{Hz}}$ |
| THD | Total harmonic distortion $V_{O(PP)} = 2$ V to 20 V, $R_L = 2 \text{ k}\Omega$, $A_{VD} = 10$, $f = 10$ kHz | | | 0.02 | | 0.02 | | % |
| GBW | Gain-bandwidth product $f = 100$ kHz | | 3 | 4 | 3 | 4 | | MHz |
| BW | Power bandwidth $V_{O(PP)} = 20$ V, $R_L = 2 \text{ k}\Omega$, $A_{VD} = 1$, THD = 5.0% | | | 160 | | 160 | | kHz |
| ϕ_m | Phase margin $R_L = 2 \text{ k}\Omega$, $C_L = 0$ | $R_L = 2 \text{ k}\Omega$, $C_L = 0$ | | 70 | | 70 | | deg |
| | | $R_L = 2 \text{ k}\Omega$, $C_L = 300 \text{ pF}$ | | 50 | | 50 | | |
| Gain margin | $R_L = 2 \text{ k}\Omega$, $C_L = 0$ | $R_L = 2 \text{ k}\Omega$, $C_L = 0$ | | 12 | | 12 | | dB |
| | | $R_L = 2 \text{ k}\Omega$, $C_L = 300 \text{ pF}$ | | 4 | | 4 | | |
| r_i | Differential input resistance $V_{IC} = 0$ | | | 150 | | 150 | | $\text{M}\Omega$ |
| C_i | Input capacitance $V_{IC} = 0$ | | | 2.5 | | 2.5 | | pF |
| | Channel separation $f = 10$ kHz | | | 101 | | 101 | | dB |
| z_o | Open-loop output impedance $f = 1$ MHz, | $A_V = 1$ | | 20 | | 20 | | Ω |

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TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

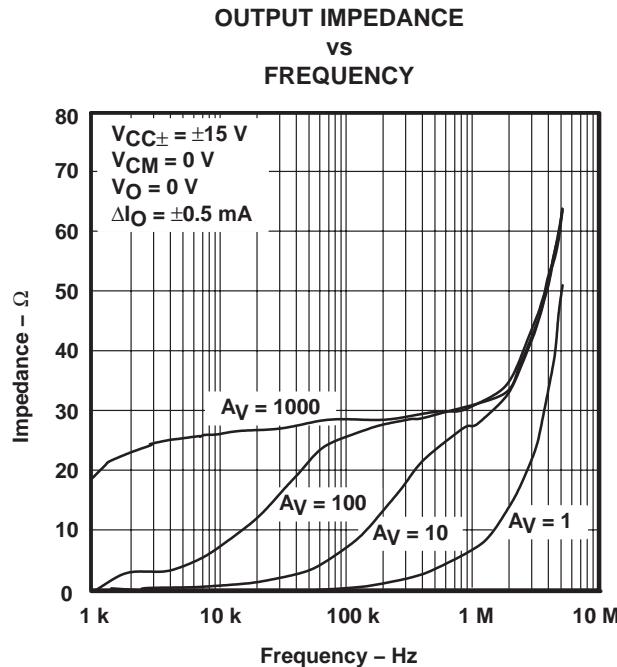


Figure 1

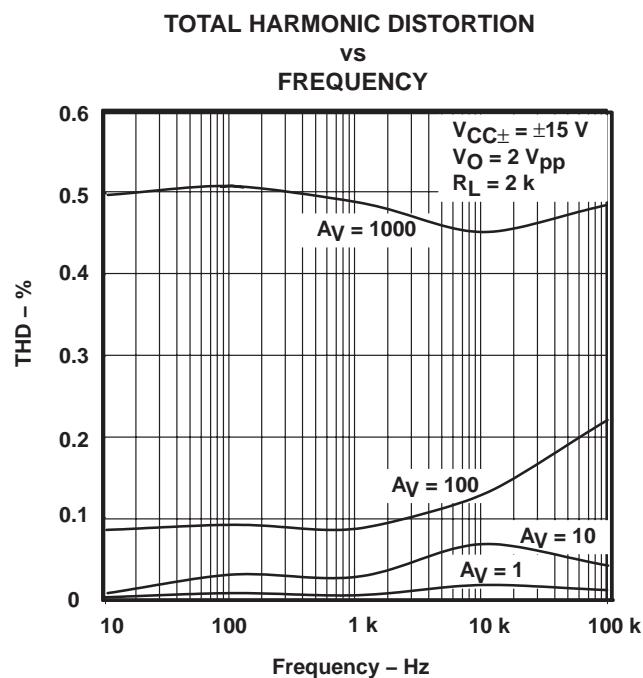


Figure 2

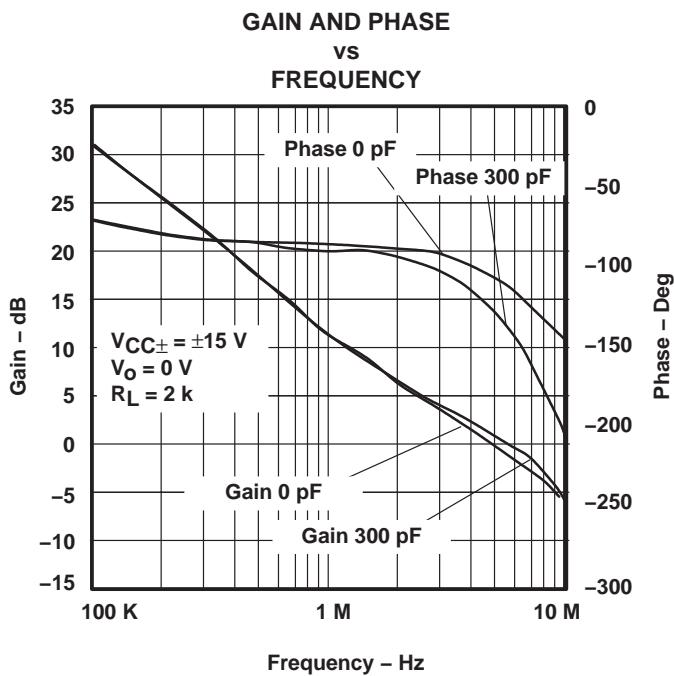


Figure 3

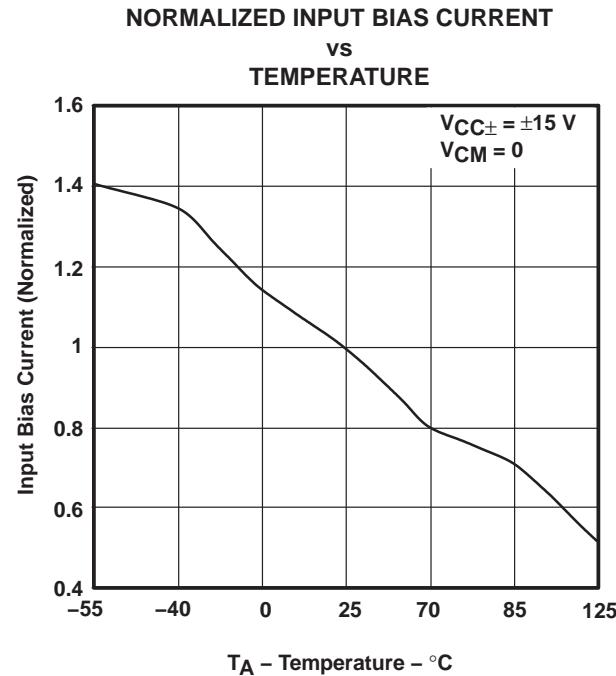


Figure 4

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

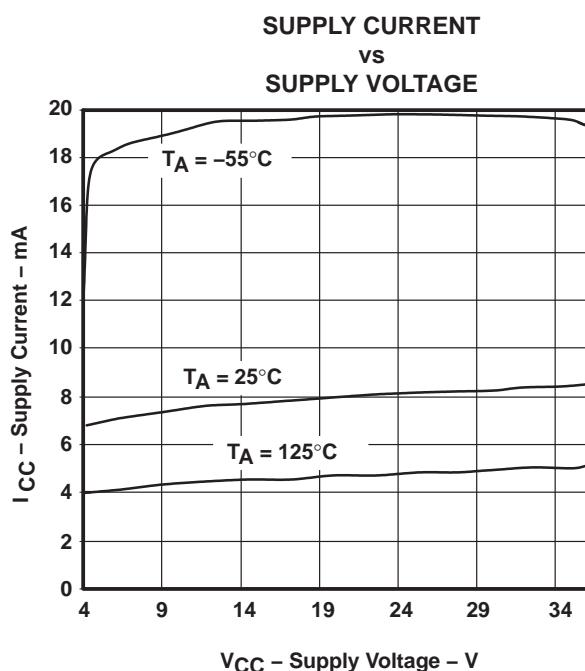


Figure 5

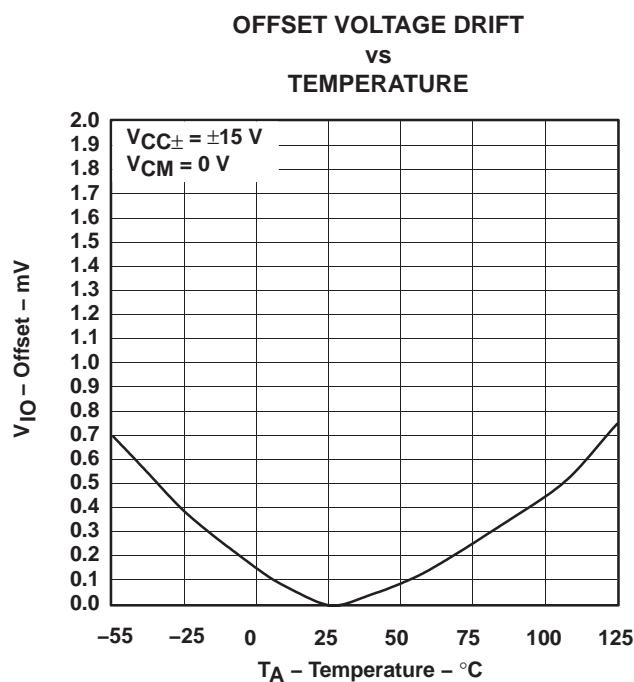


Figure 6

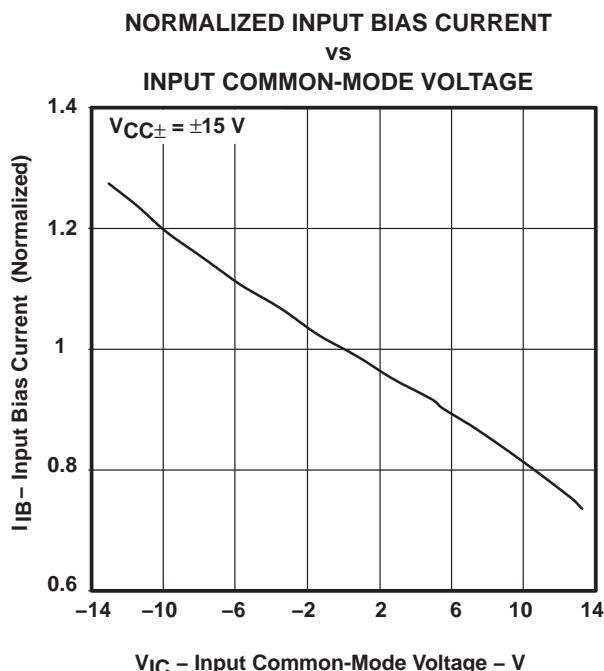


Figure 7

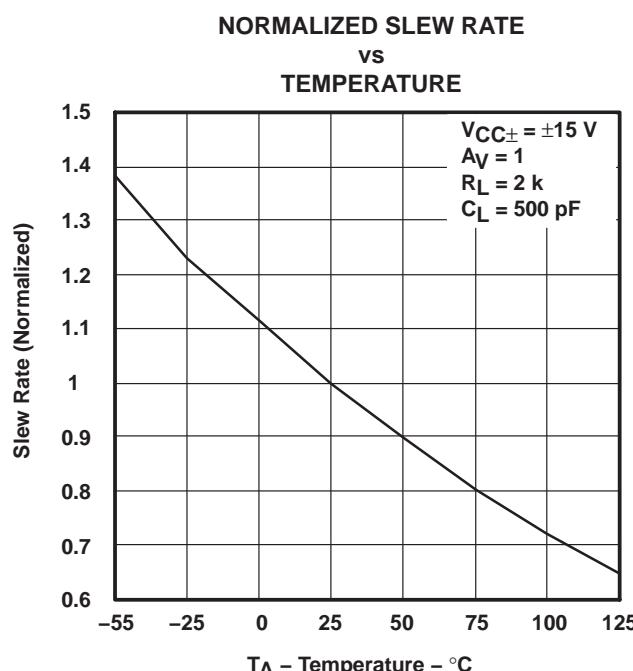


Figure 8

TL3474, TL3474A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

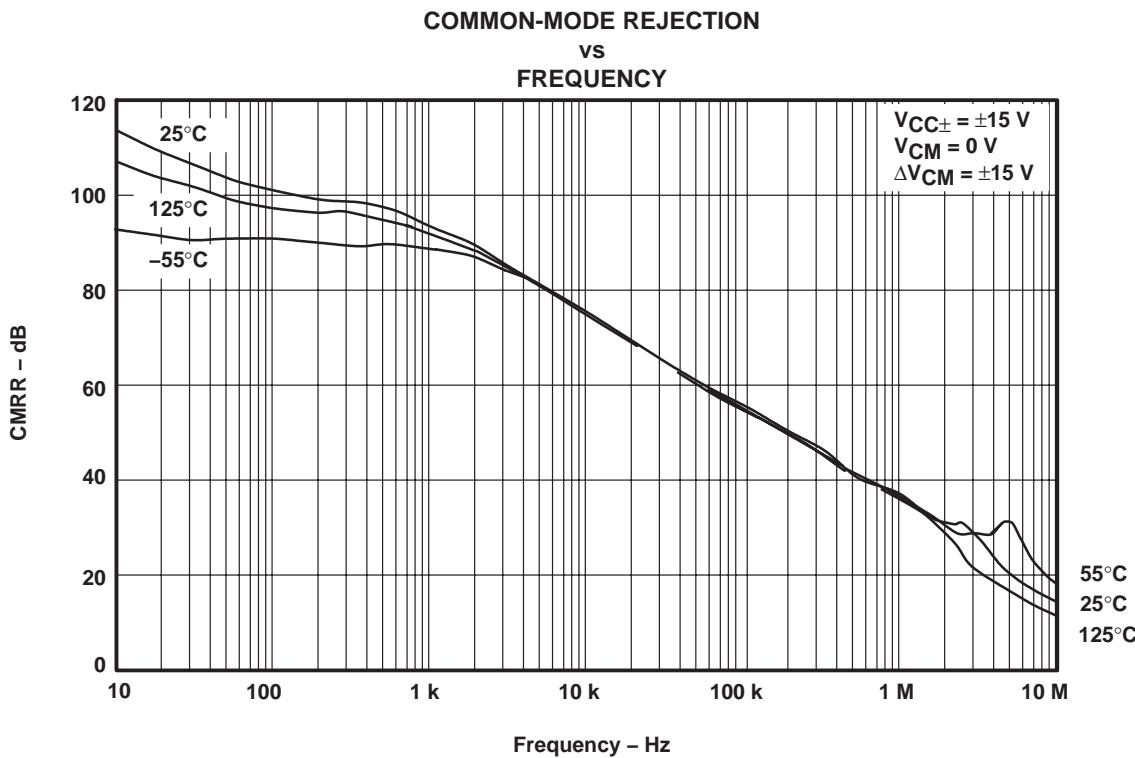


Figure 9

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| TL3474ACD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3474A | Samples |
| TL3474ACDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3474A | Samples |
| TL3474ACN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL3474ACN | Samples |
| TL3474ACPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T3474A | Samples |
| TL3474ACPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T3474A | Samples |
| TL3474AID | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | TL3474AI | Samples |
| TL3474AIDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | TL3474AI | Samples |
| TL3474AIDRE4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | TL3474AI | Samples |
| TL3474AIN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 105 | TL3474AIN | Samples |
| TL3474AIPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | Z3474A | Samples |
| TL3474AIPWE4 | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | Z3474A | Samples |
| TL3474AIPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | Z3474A | Samples |
| TL3474CD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3474C | Samples |
| TL3474CDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3474C | Samples |
| TL3474CN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL3474CN | Samples |
| TL3474CPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T3474 | Samples |
| TL3474CPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T3474 | Samples |
| TL3474ID | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | TL3474I | Samples |
| TL3474IDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | TL3474I | Samples |
| TL3474IN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 105 | TL3474IN | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| TL3474IPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | Z3474 | Samples |
| TL3474IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | Z3474 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

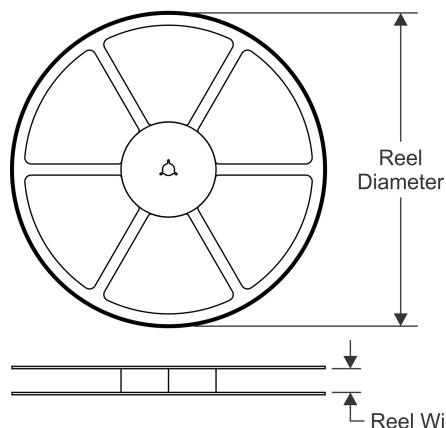
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

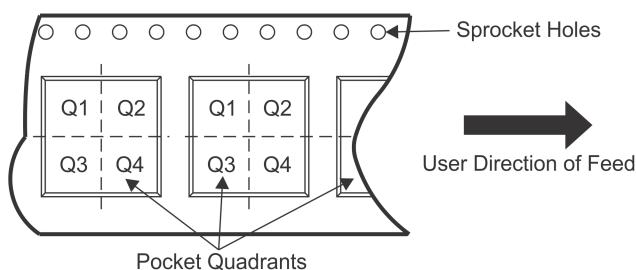
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


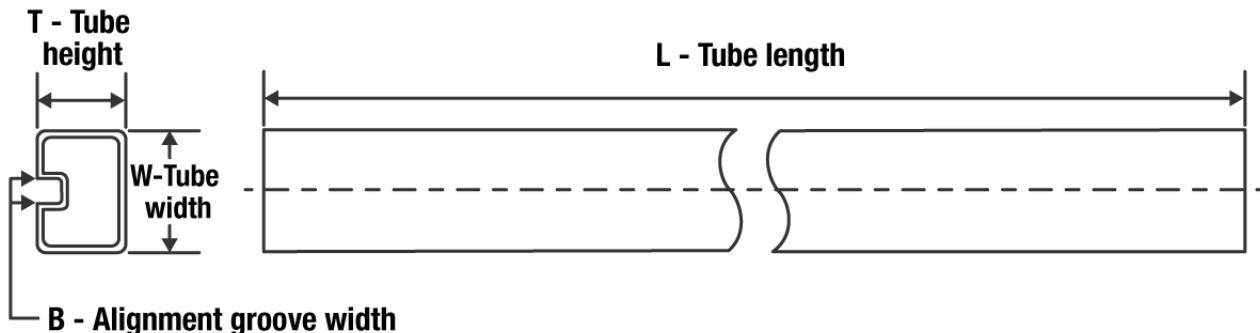
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL3474ACDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3474ACPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL3474AIDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3474AIPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL3474CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3474CPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL3474IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3474IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL3474ACDR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| TL3474ACPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| TL3474AIDR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| TL3474AIPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| TL3474CDR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| TL3474CPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| TL3474IDR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| TL3474IPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |

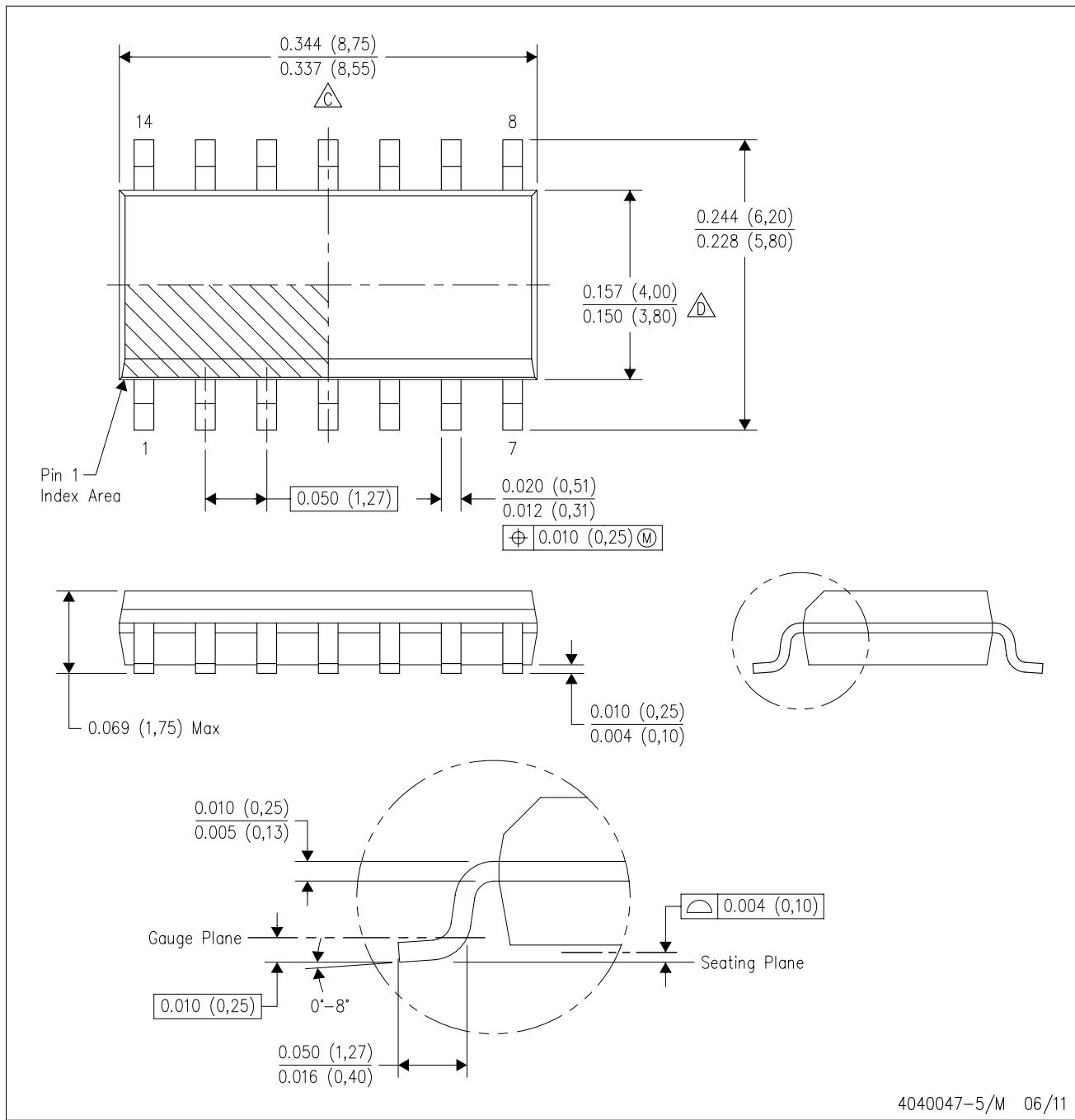
TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TL3474ACD | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| TL3474ACN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TL3474ACPW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| TL3474AID | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| TL3474AIN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TL3474AIPW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| TL3474AIPWE4 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| TL3474CD | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| TL3474CN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TL3474CPW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| TL3474ID | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| TL3474IN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TL3474IPW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

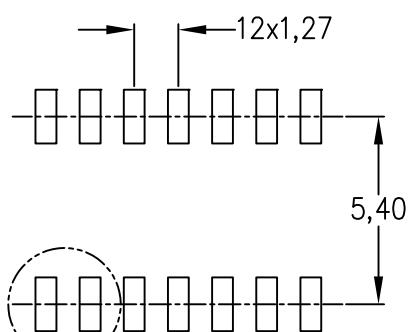
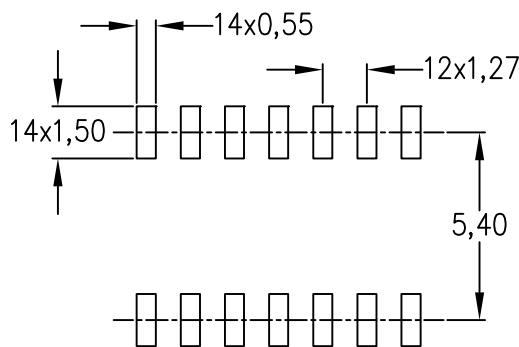
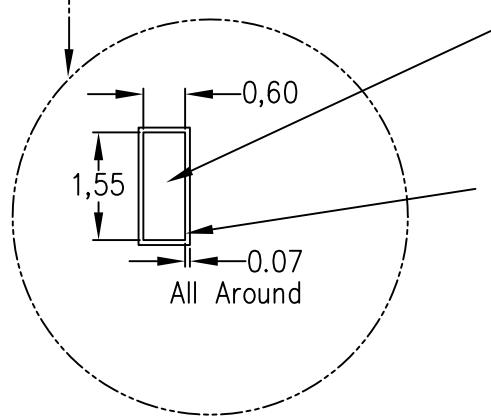
 Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

 Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

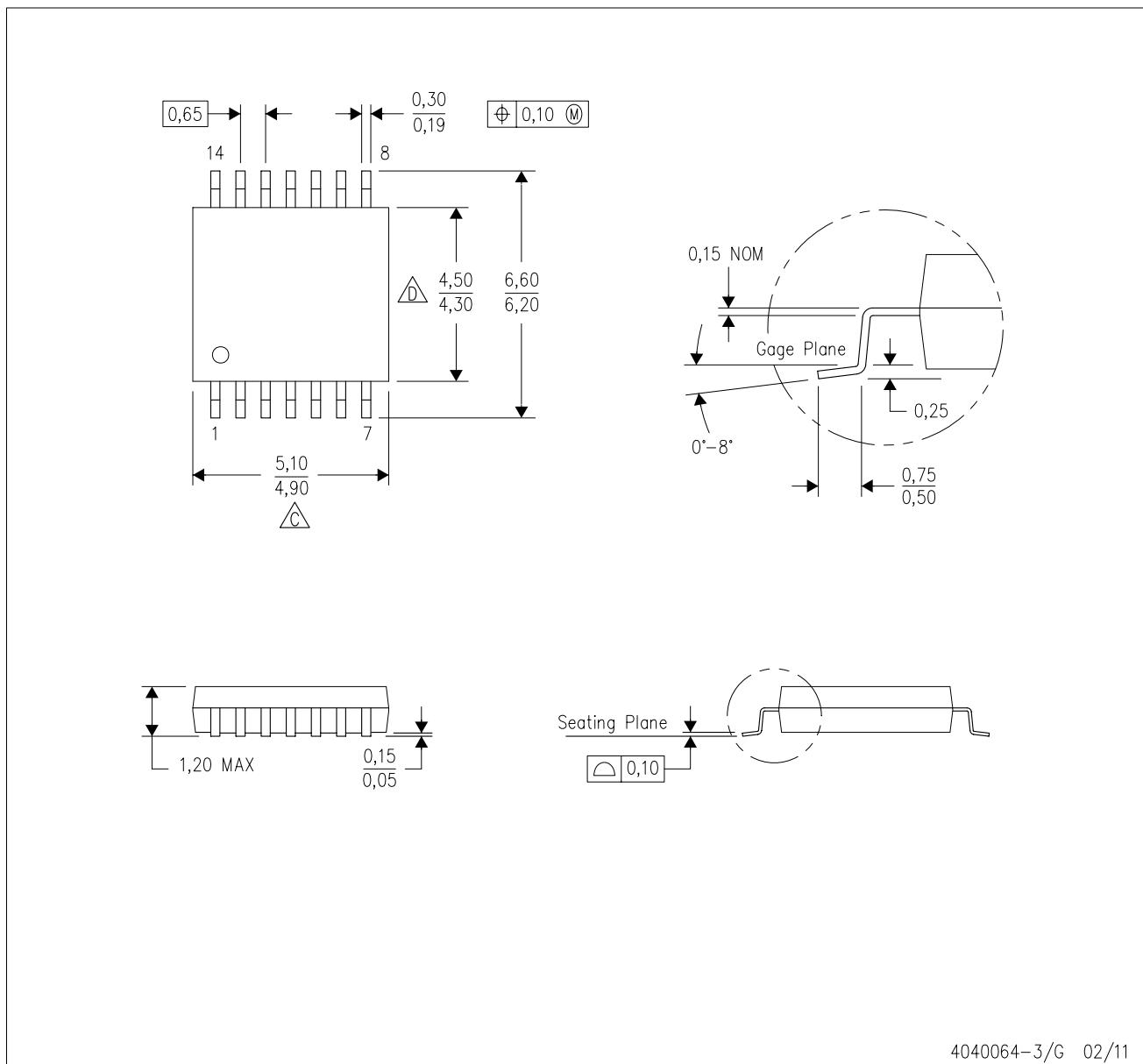
4211283-3/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

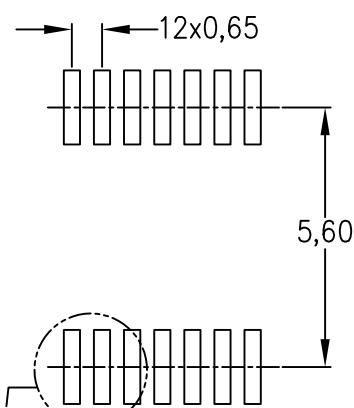
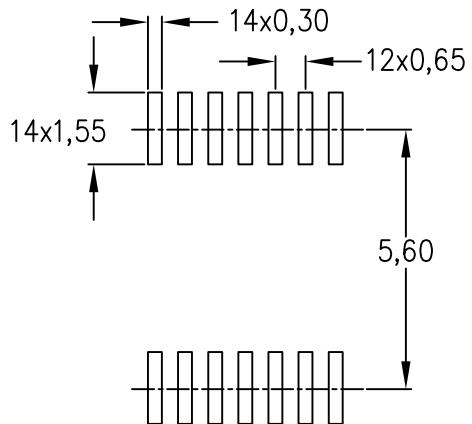
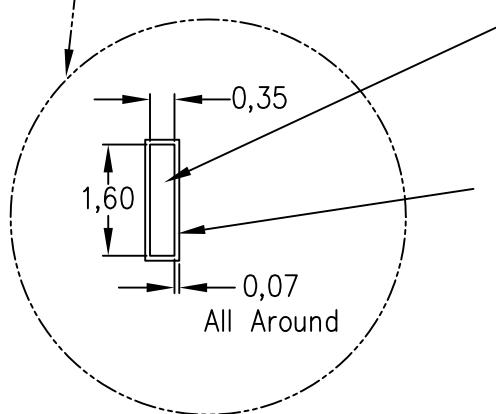
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211284-2/G 08/15

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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