

## ADS4449 四通道、14 位、250MSPS 低功耗 ADC

### 1 特性

- 四通道
- 14 位分辨率
- 最大采样数据速率：250MSPS
- 功率耗散：
  - 每通道 365mW
- 170MHz IF 上的频谱性能（典型值）：
  - SNR：69dBFS
  - SFDR：86dBc
- DDR LVDS 数字输出接口
- 内部抖动
- 封装：144 端子 NFBGA (10.00mm × 10.00mm)

### 2 应用

- 多载波 GSM 蜂窝基础设施基站
- 雷达和智能天线阵列
- 多载波多模式蜂窝基础设施基站
- 针对无线基础设施有源天线阵列
- 通信测试设备

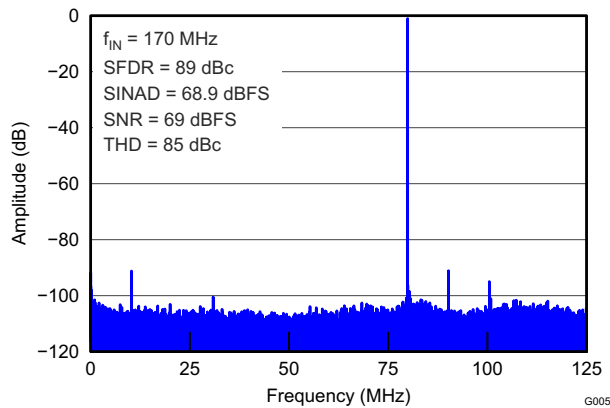
### 3 说明

ADS4449 是一款高线性、四通道、14 位、250MSPS 模数转换器 (ADC)。此器件针对低功耗和高无杂散动态范围 (SFDR) 而设计，具有低噪声性能以及在宽输入频率范围内出色的 SFDR。

#### 器件信息

| 器件型号    | 封装 <sup>(1)</sup> | 封装尺寸 (标称值)        |
|---------|-------------------|-------------------|
| ADS4449 | NFBGA (144)       | 10.00mm x 10.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



170MHz 输入频率的频谱



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| <b>Changes from Revision A (April 2013) to Revision B (November 2020)</b> | <b>Page</b> |
|---------------------------------------------------------------------------|-------------|
| • Added Low Sampling Rate mode to 表 8-2 .....                             | 24          |

| <b>Changes from Revision * (April 2013) to Revision A (January 2016)</b>                                                              | <b>Page</b> |
|---------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • 添加了 内部抖动特性要点.....                                                                                                                   | 1           |
| • 添加了 ESD 等级表、特性说明部分、器件功能模式部分、应用和实现部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分。.....                                                    | 1           |
| • 删除了封装和订购信息，因为这些数据在封装选项附录中重复.....                                                                                                    | 1           |
| • 从功能方框图中的配置寄存器块删除了 SNRB.....                                                                                                         | 1           |
| • Changed Clock Inputs, <i>Input clock sample rate</i> parameter minimum specification in Recommended Operating Conditions table..... | 5           |
| • Changed 表 8-1 .....                                                                                                                 | 23          |

## 5 Pin Configuration and Functions

|   | 1      | 2      | 3             | 4             | 5                | 6                | 7                | 8                | 9             | 10            | 11     | 12     |
|---|--------|--------|---------------|---------------|------------------|------------------|------------------|------------------|---------------|---------------|--------|--------|
| A | AVDD   | AVDD   | CINM          | CINP          | AVDD             | VCM              | VCM              | AVDD             | BINM          | BINP          | AVDD   | AVDD   |
| B | DINP   | AVSS   | AVDD          | AVDD          | AVSS             | AVDD33           | AVDD33           | AVSS             | AVDD          | AVDD          | AVSS   | AINM   |
| C | DINM   | AVSS   | AVSS          | AVSS          | AVSS             | CLKINM           | CLKINP           | AVSS             | AVSS          | AVSS          | AVSS   | AINP   |
| D | AVDD   | AVDD   | VCM           | AVSS          | AVSS             | AVSS             | AVSS             | AVSS             | AVSS          | VCM           | AVDD   | AVDD   |
| E | AVDD33 | AVDD33 | NC            | DRVSS         | DRVSS            | DRVSS            | DRVSS            | DRVSS            | DRVSS         | PDN           | AVDD33 | AVDD33 |
| F | DCD13M | DCD13P | DRVDD         | DRVSS         | DRVSS            | DRVSS            | DRVSS            | DRVSS            | DRVSS         | DRVDD         | DAB13P | DAB13M |
| G | DCD12M | DCD12P | NC            | NC            | NC               | RESET            | SCLK             | SDATA            | SEN           | SDOUT         | DAB12P | DAB12M |
| H | DCD11M | DCD11P | DCD6P         | DCD6M         | DRVDD            | DRVDD            | DRVDD            | DRVDD            | DAB6M         | DAB6P         | DAB11P | DAB11M |
| J | DCD10M | DCD10P | DCD5P         | DCD5M         | DCD2P            | DRVDD            | DRVDD            | DAB2M            | DAB5M         | DAB5P         | DAB10P | DAB10M |
| K | DCD9M  | DCD9P  | DCD4P         | DCD4M         | DCD2M            | DRVDD            | DRVDD            | DAB2P            | DAB4M         | DAB4P         | DAB9P  | DAB9M  |
| L | DCD8M  | DCD8P  | DCD3P         | DCD3M         | DCD1P            | DCD1M            | DAB1M            | DAB1P            | DAB3M         | DAB3P         | DAB8P  | DAB8M  |
| M | DCD7M  | DCD7P  | CLKOUT<br>CDP | CLKOUT<br>CDM | DCD0P/<br>OVRCDP | DCD0M/<br>OVRCDM | DAB0M/<br>OVRABM | DAB0P/<br>OVRABP | CLKOUT<br>ABM | CLKOUT<br>ABP | DAB7P  | DAB7M  |

图 5-1. ZCR Package, 144-Pin NFBGA, Top View

表 5-1. Pin Functions

| PIN                                                           |                                                                      | I/O | DESCRIPTION                                                                                 |
|---------------------------------------------------------------|----------------------------------------------------------------------|-----|---------------------------------------------------------------------------------------------|
| NAME                                                          | NO.                                                                  |     |                                                                                             |
| AINM                                                          | B12                                                                  | I   | Negative differential analog input for channel A                                            |
| AINP                                                          | C12                                                                  | I   | Positive differential analog input for channel A                                            |
| AVDD33                                                        | B6, B7, E1, E2, E11, E12                                             | I   | Analog 3.3-V power supply                                                                   |
| AVDD                                                          | A1, A2, A5, A8, A11, A12, B3, B4, B9, B10, D1, D2, D11, D12          | I   | Analog 1.9-V power supply                                                                   |
| AVSS                                                          | B2, B5, B8, B11, C2-C5, C8-C11, D4-D9                                | I   | Analog ground                                                                               |
| BINM                                                          | A9                                                                   | I   | Negative differential analog input for channel B                                            |
| BINP                                                          | A10                                                                  | I   | Positive differential analog input for channel B                                            |
| CINM                                                          | A3                                                                   | I   | Negative differential analog input for channel C                                            |
| CINP                                                          | A4                                                                   | I   | Positive differential analog input for channel C                                            |
| CLKINM                                                        | C6                                                                   | I   | Negative differential clock input                                                           |
| CLKINP                                                        | C7                                                                   | I   | Positive differential clock input                                                           |
| CLKOUTABM                                                     | M9                                                                   | O   | Negative differential LVDS clock output for channel A and B                                 |
| CLKOUTABP                                                     | M10                                                                  | O   | Positive differential LVDS clock output for channel A and B                                 |
| CLKOUTCDM                                                     | M4                                                                   | O   | Negative differential LVDS clock output for channels C and D                                |
| CLKOUTCDP                                                     | M3                                                                   | O   | Positive differential LVDS clock output for channels C and D                                |
| DAB[13:1]P, DAB0P/<br>OVRABP,<br>DAB[13:1]M, DAB0M/<br>OVRABM | F11, F12, G11, G12, H9-H12, J8-J12, K8-K12, L7-L12, M7, M8, M11, M12 | O   | DDR LVDS outputs for channels A and B.                                                      |
| DCD[13:1]P, DCD0P/<br>OVRCDP,<br>DCD[13:1]M, DCD0M/<br>OVRCDM | F1, F2, G1, G2, H1-H4, J1-J5, K1-K5, L1-L6, M1, M2, M5, M6           | O   | DDR LVDS outputs for channels C and D.                                                      |
| DINM                                                          | C1                                                                   | I   | Negative differential analog input for channel D                                            |
| DINP                                                          | B1                                                                   | I   | Positive differential analog input for channel D                                            |
| DRVDD                                                         | F3, F10, H5-H8, J6, J7, K6, K7                                       | I   | Digital 1.8-V power supply                                                                  |
| DRVSS                                                         | E4-E9, F4-F9                                                         | I   | Digital ground                                                                              |
| NC                                                            | E3, G3, G4, G5                                                       | -   | Do not connect                                                                              |
| PDN                                                           | E10                                                                  | I   | Power-down control; active high. Logic high is power down.                                  |
| RESET                                                         | G6                                                                   | I   | Hardware reset; active high                                                                 |
| SCLK                                                          | G7                                                                   | I   | Serial interface clock input                                                                |
| SDATA                                                         | G8                                                                   | I   | Serial interface data input                                                                 |
| SDOUT                                                         | G10                                                                  | O   | Serial interface data output                                                                |
| SEN                                                           | G9                                                                   | I   | Serial interface enable                                                                     |
| VCM                                                           | A6, A7, D3, D10                                                      | O   | Common-mode voltage for analog inputs. All VCM terminals are internally connected together. |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                    |                                    | MIN   | MAX                       | UNIT |
|------------------------------------|------------------------------------|-------|---------------------------|------|
| Supply voltage                     | AVDD33                             | – 0.3 | 3.6                       | V    |
|                                    | AVDD                               | – 0.3 | 2.1                       |      |
|                                    | DRVDD                              | – 0.3 | 2.1                       |      |
| Voltage between                    | AVSS and DRVSS                     | – 0.3 | 0.3                       | V    |
|                                    | AVDD and DRVDD                     | – 2.4 | 2.4                       |      |
|                                    | AVDD33 and DRVDD                   | – 2.4 | 3.9                       |      |
|                                    | AVDD33 and AVDD                    | – 2.4 | 3.9                       |      |
| Voltage applied to input terminals | XINP, XINM                         | – 0.3 | minimum (1.9, AVDD + 0.3) | V    |
|                                    | CLKP, CLKM <sup>(2)</sup>          | – 0.3 | minimum (1.9, AVDD + 0.3) |      |
|                                    | RESET, SCLK, SDATA, SEN, PDN       | – 0.3 | 3.9                       |      |
| Temperature                        | Operating free-air, T <sub>A</sub> | – 40  | 85                        | °C   |
|                                    | Operating junction, T <sub>J</sub> |       | 150                       |      |
|                                    | Storage, T <sub>stg</sub>          | – 65  | 150                       |      |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [§ 6.3](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) When AVDD is turned off, TI recommends switching off the input clock (or ensuring the voltage on CLKP and CLKM is less than | 0.3 V |). This recommendation prevents the ESD protection diodes at the clock input terminals from turning on.

### 6.2 ESD Ratings

|                                            |                                                                                | VALUE | UNIT |
|--------------------------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                                            | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                 |                                                                       | MIN                                              | NOM                     | MAX  | UNIT            |
|-----------------|-----------------------------------------------------------------------|--------------------------------------------------|-------------------------|------|-----------------|
| SUPPLIES        |                                                                       |                                                  |                         |      |                 |
| AVDD33          | Supply voltage                                                        | 3.15                                             | 3.3                     | 3.45 | V               |
| AVDD            |                                                                       | 1.8                                              | 1.9                     | 2    | V               |
| DRVDD           |                                                                       | 1.7                                              | 1.8                     | 2    | V               |
| ANALOG INPUTS   |                                                                       |                                                  |                         |      |                 |
|                 | Differential input voltage range                                      |                                                  | 2                       |      | V <sub>PP</sub> |
| V <sub>IC</sub> | Input common-mode voltage                                             |                                                  | V <sub>CM</sub> ± 0.025 |      | V               |
|                 | Analog input common-mode current (per input terminal of each channel) |                                                  | 1.5                     |      | µA/MSPS         |
|                 | VCM current capability                                                |                                                  | 5                       |      | mA              |
|                 | Maximum analog input frequency                                        | 2-V <sub>PP</sub> input amplitude <sup>(2)</sup> | 400                     |      | MHz             |
|                 |                                                                       | 1.4-V <sub>PP</sub> input amplitude              | 500                     |      |                 |
| CLOCK INPUTS    |                                                                       |                                                  |                         |      |                 |
|                 | Input clock sample rate <sup>(1)</sup>                                |                                                  | 10                      | 250  | MSPS            |

### 6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

|                                                                 |                                                                                         | MIN                          | NOM | MAX      | UNIT               |
|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|------------------------------|-----|----------|--------------------|
| Input clock amplitude differential<br>( $V_{CLKP} - V_{CLKM}$ ) | Sine wave, ac-coupled                                                                   | 0.2                          | 1.5 | $V_{PP}$ |                    |
|                                                                 | LVPECL, ac-coupled                                                                      |                              | 1.6 |          |                    |
|                                                                 | LVDS, ac-coupled                                                                        |                              | 0.7 |          |                    |
|                                                                 | LVC MOS, single-ended, ac-coupled                                                       |                              | 1.8 |          |                    |
| Input clock duty cycle                                          |                                                                                         | 40%                          | 50% | 60%      |                    |
| <b>DIGITAL OUTPUTS</b>                                          |                                                                                         |                              |     |          |                    |
| $C_{LOAD}$                                                      | Maximum external load capacitance from each output terminal to DRVSS (default strength) |                              | 3.3 |          | pF                 |
| $R_{LOAD}$                                                      | Differential load resistance between the LVDS output pairs (LVDS mode)                  |                              | 100 |          | $\Omega$           |
| <b>TEMPERATURE RANGE</b>                                        |                                                                                         |                              |     |          |                    |
| $T_A$                                                           | Operating free-air temperature                                                          | - 40                         |     | 85       | $^{\circ}\text{C}$ |
| $T_J$                                                           | Operating junction temperature                                                          | Recommended                  |     | 105      | $^{\circ}\text{C}$ |
|                                                                 |                                                                                         | Maximum rated <sup>(2)</sup> |     | 125      |                    |

(1) When input clock sample rate is below 200 MSPS Low Sample Rate Mode is required.

(2) Prolonged use at this junction temperature may increase the device failure-in-time (FIT) rate.

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | ADS4449     | UNIT                 |
|-------------------------------|----------------------------------------------|-------------|----------------------|
|                               |                                              | ZCR (NFBGA) |                      |
|                               |                                              | 144 PINS    |                      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 35.9        | $^{\circ}\text{C/W}$ |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 5.1         | $^{\circ}\text{C/W}$ |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 12.6        | $^{\circ}\text{C/W}$ |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 0.1         | $^{\circ}\text{C/W}$ |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 12.4        | $^{\circ}\text{C/W}$ |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | N/A         | $^{\circ}\text{C/W}$ |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

Typical values are at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , ADC clock frequency = 250 MHz, 50% clock duty cycle, AVDD33V = 3.3 V, AVDD = 1.9 V, DRVDD = 1.8 V, and -1-dBFS differential input, unless otherwise noted.

| PARAMETER                                                 |                                      |                                                    | TEST CONDITIONS                                   | MIN   | TYP | MAX             | UNITS |
|-----------------------------------------------------------|--------------------------------------|----------------------------------------------------|---------------------------------------------------|-------|-----|-----------------|-------|
| RESOLUTION                                                |                                      |                                                    |                                                   |       |     |                 |       |
| Default resolution                                        |                                      |                                                    |                                                   | 14    |     | Bits            |       |
| ANALOG INPUTS                                             |                                      |                                                    |                                                   |       |     |                 |       |
| Differential input full-scale                             |                                      |                                                    |                                                   | 2     |     | V <sub>PP</sub> |       |
| VCM                                                       | Common mode input voltage            |                                                    |                                                   | 1.15  |     | V               |       |
| R <sub>IN</sub>                                           | Input resistance, differential       |                                                    | At 170-MHz input frequency                        | 700   |     | Ω               |       |
| C <sub>IN</sub>                                           | Input capacitance, differential      |                                                    | At 170-MHz input frequency                        | 3.3   |     | pF              |       |
| Analog input bandwidth, 3 dB                              |                                      |                                                    | with a 50- Ω source driving the ADC analog inputs | 500   |     | MHz             |       |
| DYNAMIC ACCURACY                                          |                                      |                                                    |                                                   |       |     |                 |       |
| E <sub>O</sub>                                            | Offset error                         |                                                    | Specified across devices and channels             | - 15  | 15  |                 | mV    |
| E <sub>G</sub>                                            | Gain error <sup>(2)</sup>            | As a result of internal reference inaccuracy alone | Specified across devices and channels             | - 5   | 5   |                 | %FS   |
|                                                           |                                      | Of channel alone                                   | Specified across channels within a device         | ±0.2  |     |                 |       |
| Channel gain error temperature coefficient <sup>(2)</sup> |                                      |                                                    |                                                   | 0.001 |     | Δ %/°C          |       |
| POWER SUPPLY <sup>(1)</sup>                               |                                      |                                                    |                                                   |       |     |                 |       |
| I <sub>AVDD33</sub>                                       | Supply current                       | 3.3-V analog supply                                |                                                   | 51    |     | mA              |       |
| I <sub>AVDD</sub>                                         |                                      | 1.9-V analog supply                                |                                                   | 350   |     | mA              |       |
| I <sub>DRVDD</sub>                                        |                                      | 1.8-V digital supply                               |                                                   | 355   |     | mA              |       |
| P <sub>TOTAL</sub>                                        | Power dissipation                    | Total                                              |                                                   | 1.47  |     | 1.6             | W     |
| P <sub>DISS(standby)</sub>                                |                                      | Standby                                            |                                                   | 400   |     | mW              |       |
| P <sub>DISS(global)</sub>                                 |                                      | Global power-down                                  |                                                   | 6     |     | 52              | mW    |
| DYNAMIC AC CHARACTERISTICS                                |                                      |                                                    |                                                   |       |     |                 |       |
| SNR                                                       | Signal-to-noise ratio                | f <sub>IN</sub> = 40 MHz                           |                                                   | 71.1  |     | dBFS            |       |
|                                                           |                                      | f <sub>IN</sub> = 70 MHz                           |                                                   | 71    |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 140 MHz                          |                                                   | 69.5  |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 170 MHz                          | 67.5                                              | 69    |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 220 MHz                          |                                                   | 68.5  |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 307 MHz                          |                                                   | 67.5  |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 350 MHz                          |                                                   | 67    |     |                 |       |
| SINAD                                                     | Signal-to-noise and distortion ratio | f <sub>IN</sub> = 40 MHz                           |                                                   | 70.9  |     | dBFS            |       |
|                                                           |                                      | f <sub>IN</sub> = 70 MHz                           |                                                   | 70.8  |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 140 MHz                          |                                                   | 69.3  |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 170 MHz                          | 66.9                                              | 68.8  |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 220 MHz                          |                                                   | 68.3  |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 307 MHz                          |                                                   | 66.8  |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 350 MHz                          |                                                   | 66.3  |     |                 |       |
| SFDR                                                      | Spurious-free dynamic range          | f <sub>IN</sub> = 40 MHz                           |                                                   | 84    |     | dBc             |       |
|                                                           |                                      | f <sub>IN</sub> = 70 MHz                           |                                                   | 87    |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 140 MHz                          |                                                   | 85    |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 170 MHz                          | 78.5                                              | 86    |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 220 MHz                          |                                                   | 84    |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 307 MHz                          |                                                   | 78    |     |                 |       |
|                                                           |                                      | f <sub>IN</sub> = 350 MHz                          |                                                   | 77    |     |                 |       |

## 6.5 Electrical Characteristics (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , ADC clock frequency = 250 MHz, 50% clock duty cycle, AVDD33V = 3.3 V, AVDD = 1.9 V, DRVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

| PARAMETER |                                                     | TEST CONDITIONS                                                                        | MIN   | TYP  | MAX   | UNITS       |
|-----------|-----------------------------------------------------|----------------------------------------------------------------------------------------|-------|------|-------|-------------|
| THD       | Total harmonic distortion                           | $f_{\text{IN}} = 40\text{ MHz}$                                                        |       | 83   |       | dBc         |
|           |                                                     | $f_{\text{IN}} = 70\text{ MHz}$                                                        |       | 84   |       |             |
|           |                                                     | $f_{\text{IN}} = 140\text{ MHz}$                                                       |       | 82   |       |             |
|           |                                                     | $f_{\text{IN}} = 170\text{ MHz}$                                                       | 75    | 83   |       |             |
|           |                                                     | $f_{\text{IN}} = 220\text{ MHz}$                                                       |       | 82   |       |             |
|           |                                                     | $f_{\text{IN}} = 307\text{ MHz}$                                                       |       | 76   |       |             |
|           |                                                     | $f_{\text{IN}} = 350\text{ MHz}$                                                       |       | 75   |       |             |
| HD2       | Second-order harmonic distortion <sup>(3) (4)</sup> | $f_{\text{IN}} = 40\text{ MHz}$                                                        |       | 96   |       | dBc         |
|           |                                                     | $f_{\text{IN}} = 70\text{ MHz}$                                                        |       | 87   |       |             |
|           |                                                     | $f_{\text{IN}} = 140\text{ MHz}$                                                       |       | 86   |       |             |
|           |                                                     | $f_{\text{IN}} = 170\text{ MHz}$                                                       | 78.5  | 86   |       |             |
|           |                                                     | $f_{\text{IN}} = 220\text{ MHz}$                                                       |       | 84   |       |             |
|           |                                                     | $f_{\text{IN}} = 307\text{ MHz}$                                                       |       | 78   |       |             |
|           |                                                     | $f_{\text{IN}} = 350\text{ MHz}$                                                       |       | 77   |       |             |
| HD3       | Third-order harmonic distortion                     | $f_{\text{IN}} = 40\text{ MHz}$                                                        |       | 83   |       | dBc         |
|           |                                                     | $f_{\text{IN}} = 70\text{ MHz}$                                                        |       | 89   |       |             |
|           |                                                     | $f_{\text{IN}} = 140\text{ MHz}$                                                       |       | 85   |       |             |
|           |                                                     | $f_{\text{IN}} = 170\text{ MHz}$                                                       | 79.5  | 86   |       |             |
|           |                                                     | $f_{\text{IN}} = 220\text{ MHz}$                                                       |       | 85   |       |             |
|           |                                                     | $f_{\text{IN}} = 307\text{ MHz}$                                                       |       | 80   |       |             |
|           |                                                     | $f_{\text{IN}} = 350\text{ MHz}$                                                       |       | 78   |       |             |
|           | Worst spur<br>(non HD2, HD3)                        | $f_{\text{IN}} = 40\text{ MHz}$                                                        |       | 100  |       | dBc         |
|           |                                                     | $f_{\text{IN}} = 70\text{ MHz}$                                                        |       | 100  |       |             |
|           |                                                     | $f_{\text{IN}} = 140\text{ MHz}$                                                       |       | 95   |       |             |
|           |                                                     | $f_{\text{IN}} = 170\text{ MHz}$                                                       | 87    | 95   |       |             |
|           |                                                     | $f_{\text{IN}} = 220\text{ MHz}$                                                       |       | 95   |       |             |
|           |                                                     | $f_{\text{IN}} = 307\text{ MHz}$                                                       |       | 85   |       |             |
|           |                                                     | $f_{\text{IN}} = 350\text{ MHz}$                                                       |       | 85   |       |             |
| DNL       | Differential nonlinearity                           |                                                                                        | –0.95 | ±0.5 |       | LSBs        |
| INL       | Integral nonlinearity                               |                                                                                        |       | ±1.5 | ±5.25 | LSBs        |
|           | Input overload recovery                             | Recovery to within 1% (of final value) for 6-dB output overload with sine-wave input   |       | 1    |       | Clock cycle |
|           | Crosstalk                                           | with a full-scale, 220-MHz signal on aggressor channel and no signal on victim channel |       | 90   |       | dB          |
| PSRR      | AC power-supply rejection ratio                     | For 50-mV <sub>PP</sub> signal on AVDD supply                                          |       | < 30 |       | dB          |

- (1) A 185-MHz, full-scale, sine-wave input signal is applied to all four channels.
- (2) There are two sources of gain error: internal reference inaccuracy and channel gain error.
- (3) Phase and amplitude imbalances onboard must be minimized to obtain good performance.
- (4) The minimum value across temperature is ensured by bench characterization.



## 6.6 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD33 = 3.3 V, AVDD = 1.9 V, and DRVDD = 1.8 V, unless otherwise noted.

| PARAMETER                                                                                                                       |                                                       |                             | TEST CONDITIONS                                                                 | MIN         | TYP   | MAX   | UNIT |
|---------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|-----------------------------|---------------------------------------------------------------------------------|-------------|-------|-------|------|
| DIGITAL INPUTS <sup>(1)</sup> (RESET, SCLK, SDATA, SEN, PDN)                                                                    |                                                       |                             |                                                                                 |             |       |       |      |
| V <sub>IH</sub>                                                                                                                 | High-level input voltage                              |                             | All digital inputs support 1.8-V logic levels. SPI supports 3.3-V logic levels. | 1.25        |       |       | V    |
| V <sub>IL</sub>                                                                                                                 | Low-level input voltage                               |                             | All digital inputs support 1.8-V logic levels. SPI supports 3.3-V logic levels. |             |       | 0.45  | V    |
| I <sub>IH</sub>                                                                                                                 | High-level input current                              | RESET, SCLK, PDN terminals  | V <sub>HIGH</sub> = 1.8 V                                                       |             | 10    |       | μA   |
|                                                                                                                                 |                                                       | SEN <sup>(2)</sup> terminal | V <sub>HIGH</sub> = 1.8 V                                                       |             | 0     |       |      |
| I <sub>IL</sub>                                                                                                                 | Low-level input current                               | RESET, SCLK, PDN terminals  | V <sub>LOW</sub> = 0 V                                                          |             | 0     |       | μA   |
|                                                                                                                                 |                                                       | SEN terminal                | V <sub>LOW</sub> = 0 V                                                          |             | 10    |       |      |
| DIGITAL OUTPUTS (SDOUT)                                                                                                         |                                                       |                             |                                                                                 |             |       |       |      |
| V <sub>OH</sub>                                                                                                                 | High-level output voltage                             |                             |                                                                                 | DRVDD – 0.1 | DRVDD |       | V    |
| V <sub>OL</sub>                                                                                                                 | Low-level output voltage                              |                             |                                                                                 |             | 0     | 0.1   | V    |
| DIGITAL OUTPUTS, LVDS INTERFACE<br>(DAB[13:0]P, DAB[13:0]M, DCD[13:0]P, DCD[13:0]M, CLKOUTABP, CLKOUTABM, CLKOUTCDP, CLKOUTCDM) |                                                       |                             |                                                                                 |             |       |       |      |
| V <sub>ODH</sub>                                                                                                                | High-level output differential voltage <sup>(3)</sup> |                             | Standard-swing LVDS                                                             | 270         | 350   | 465   | mV   |
| V <sub>ODL</sub>                                                                                                                | Low-level output differential                         |                             | Standard-swing LVDS                                                             | – 465       | – 350 | – 270 | mV   |
| V <sub>OCM</sub>                                                                                                                | Output common-mode voltage                            |                             |                                                                                 |             | 1.05  |       | V    |

(1) RESET, SDATA, and SCLK have an internal 150-k $\Omega$  pull-down resistor.

(2) SEN has an internal 150-k $\Omega$  pull-up resistor to DRVDD.

(3) with an external 100- $\Omega$  termination.

## 6.7 Timing Requirements

Typical values are at 25°C, AVDD33 = 3.3 V, AVDD = 1.9 V, DRVDD = 1.8 V, sine-wave input clock, C<sub>LOAD</sub> = 3.3 pF<sup>(2)</sup>, and R<sub>LOAD</sub> = 100 Ω<sup>(3)</sup>, unless otherwise noted.

Minimum and maximum values are across the full temperature range of T<sub>MIN</sub> = –40°C to T<sub>MAX</sub> = 85°C.

|                                                |                                        | See Note <sup>(1)</sup>                                                                                               | MIN                                        | NOM  | MAX  | UNIT                |
|------------------------------------------------|----------------------------------------|-----------------------------------------------------------------------------------------------------------------------|--------------------------------------------|------|------|---------------------|
| t <sub>A</sub>                                 | Aperture delay                         |                                                                                                                       | 0.7                                        | 1.2  | 1.6  | ns                  |
|                                                | Aperture delay matching                | Between any two channels of the same device                                                                           | ±70                                        |      |      | ps                  |
|                                                | Variation of aperture delay            | Between two devices at the same temperature and DRVDD supply                                                          | ±150                                       |      |      | ps                  |
| t <sub>J</sub>                                 | Aperture jitter                        |                                                                                                                       | 140                                        |      |      | fs rms              |
|                                                | Wake up time                           | Time to valid data after coming out of global power down                                                              | 100                                        |      |      | μs                  |
|                                                |                                        | Time to valid data after coming out of channel power down                                                             | 10                                         |      |      |                     |
| ADC latency <sup>(4) (5)</sup>                 |                                        | Default latency in 14-bit mode                                                                                        | 10                                         |      |      | Output clock cycles |
|                                                |                                        | Digital gain enabled                                                                                                  | 13                                         |      |      |                     |
|                                                |                                        | Digital gain and offset correction enabled                                                                            | 14                                         |      |      |                     |
| OUTPUT TIMING <sup>(6)</sup>                   |                                        |                                                                                                                       |                                            |      |      |                     |
| t <sub>SU</sub>                                | Data setup time <sup>(7) (8) (9)</sup> | Data valid to CLKOUTxxP zero-crossing                                                                                 | 0.6                                        | 0.85 |      | ns                  |
| t <sub>H</sub>                                 | Data hold time <sup>(7) (8) (9)</sup>  | CLKOUTxxP zero-crossing to data becoming invalid                                                                      | 0.6                                        | 0.84 |      | ns                  |
|                                                | LVDS bit clock duty cycle              | Differential clock duty cycle (CLKOUTxxP – CLKOUTxxM)                                                                 | 50%                                        |      |      |                     |
| t <sub>PDI</sub>                               | Clock propagation delay <sup>(5)</sup> | Input clock falling edge cross-over to output clock falling edge cross-over, 184 MSPS ≤ sampling frequency ≤ 250 MSPS | 0.25 × t <sub>S</sub> + t <sub>delay</sub> |      |      | ns                  |
| t <sub>delay</sub>                             | Delay time                             | Input clock falling edge cross-over to output clock falling edge cross-over, 184 MSPS ≤ sampling frequency ≤ 250 MSPS | 6.9                                        | 8.65 | 10.5 | ns                  |
| t <sub>RISE</sub> ,<br>t <sub>FALL</sub>       | Data rise and fall time                | Rise time measured from – 100 mV to 100 mV                                                                            | 0.1                                        |      |      | ns                  |
| t <sub>CLKRISE</sub> ,<br>t <sub>CLKFALL</sub> | Output clock rise and fall time        | Rise time measured from – 100 mV to 100 mV                                                                            | 0.1                                        |      |      | ns                  |

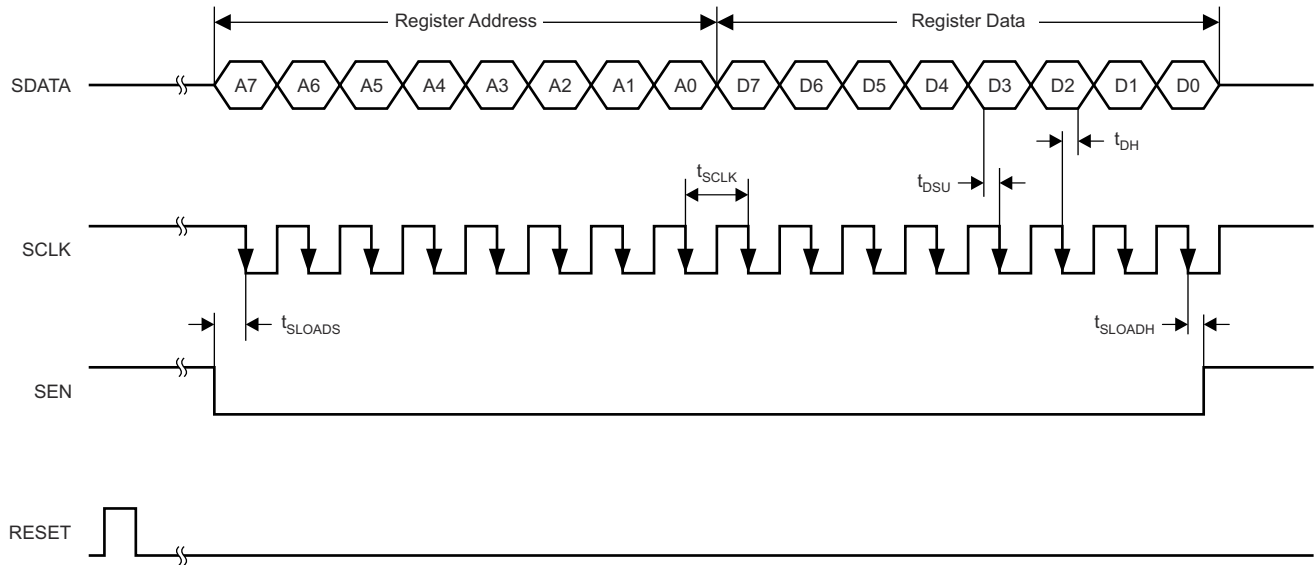
- (1) Timing parameters are ensured by design and characterization and are not tested in production.
- (2) C<sub>LOAD</sub> is the effective external single-ended load capacitance between each output terminal and ground.
- (3) R<sub>LOAD</sub> is the differential load resistance between the LVDS output pair.
- (4) ADC latency is given for channels B and D. For channels A and C, latency reduces by half of the output clock cycles.
- (5) Overall latency = ADC latency + t<sub>PDI</sub>.
- (6) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
- (7) Data valid refers to a logic high of 100 mV and a logic low of –100 mV.
- (8) Note that these numbers are taken with delayed output clocks by writing the following registers: **address A9h, value 02h; and address ACh, value 60h**. Refer to the section. By default after reset, minimum setup time and minimum hold times are 520 ps each.
- (9) The setup and hold times of a channel are measured with respect to the same channel output clock.

## 6.8 Timing Characteristics, Serial interface

| see 图 6-1           |                                                  | MIN  | NOM | MAX | UNIT |
|---------------------|--------------------------------------------------|------|-----|-----|------|
| f <sub>SCLK</sub>   | SCLK frequency (equal to 1 / t <sub>SCLK</sub> ) | > dc |     | 20  | MHz  |
| t <sub>SLOADS</sub> | SEN to SCLK setup time                           | 25   |     |     | ns   |
| t <sub>SLOADH</sub> | SCLK to SEN hold time                            | 25   |     |     | ns   |
| t <sub>DSU</sub>    | SDI setup time                                   | 25   |     |     | ns   |
| t <sub>DH</sub>     | SDI hold time                                    | 25   |     |     | ns   |

**表 6-1. LVDS Timings Across Lower Sampling Frequencies**

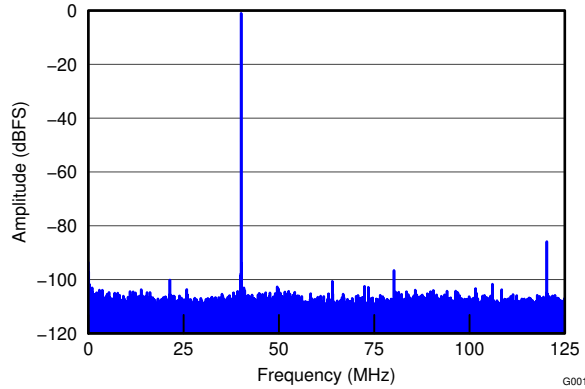
| SAMPLING FREQUENCY<br>(MSPS) | SETUP TIME (ns) |      |     | HOLD TIME (ns) |      |     |
|------------------------------|-----------------|------|-----|----------------|------|-----|
|                              | MIN             | TYP  | MAX | MIN            | TYP  | MAX |
| 210                          | 0.89            | 1.03 |     | 0.82           | 1.01 |     |
| 185                          | 1.06            | 1.21 |     | 0.95           | 1.15 |     |



**图 6-1. Serial Interface Timing**

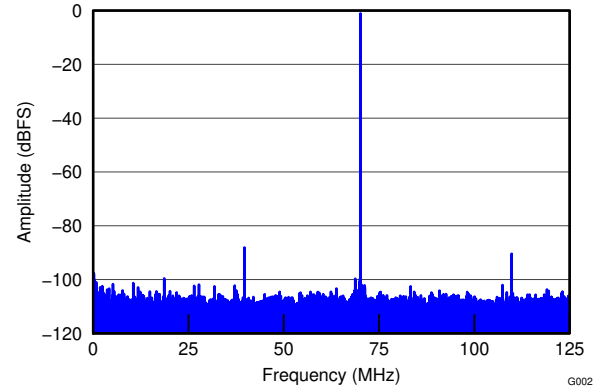
## 6.9 Typical Characteristics

At 25°C, AVDD = 1.9 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, rated sampling frequency, 0-dB gain, sine-wave input clock, 1.5-V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.



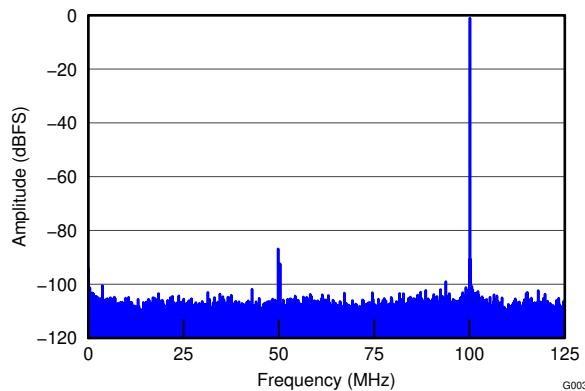
$f_{IN} = 40 \text{ MHz}$       SFDR = 84 dBc      SNR = 71.1 dBFS  
SINAD = 70.9 dBFS      THD = 84 dBc

图 6-2. FFT for 40-MHz Input Signal



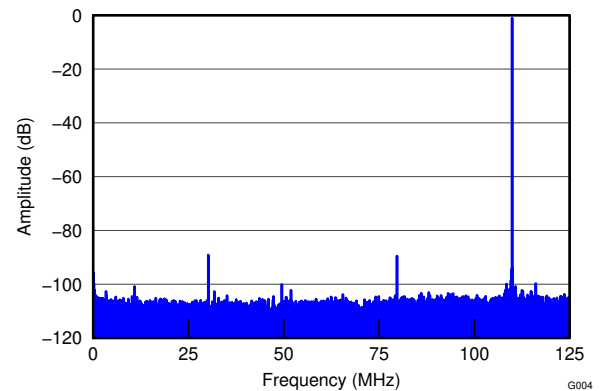
$f_{IN} = 70 \text{ MHz}$       SFDR = 87 dBc      SNR = 70.9 dBFS  
SINAD = 70.8 dBFS      THD = 84 dBc

图 6-3. FFT for 70-MHz Input Signal



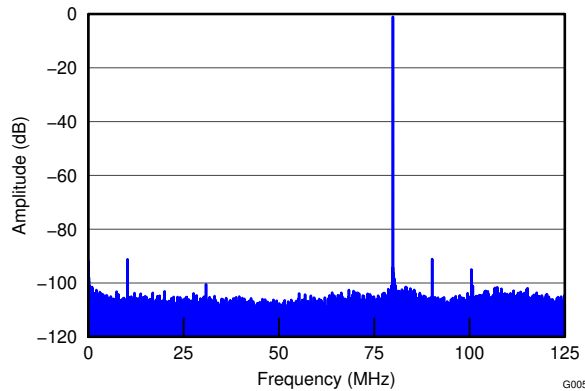
$f_{IN} = 100 \text{ MHz}$       SFDR = 85 dBc      SNR = 70.2 dBFS  
SINAD = 70.1 dBFS      THD = 84 dBc

图 6-4. FFT for 100-MHz Input Signal



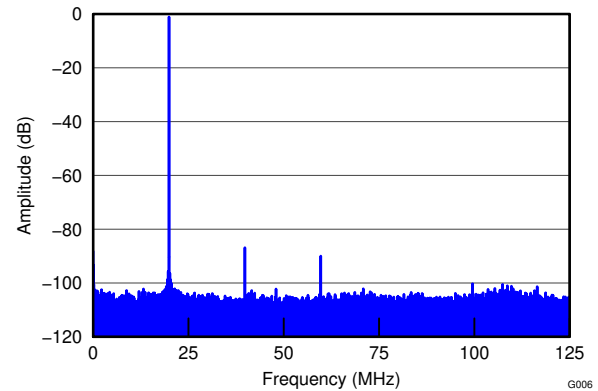
$f_{IN} = 140 \text{ MHz}$       SFDR = 87 dBc      SNR = 69.7 dBFS  
SINAD = 69.6 dBFS      THD = 84 dBc

图 6-5. FFT for 140-MHz Input Signal



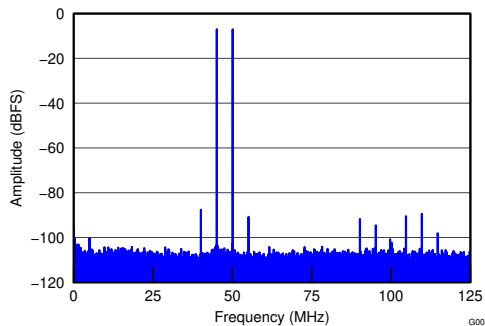
$f_{IN} = 170 \text{ MHz}$       SFDR = 89 dBc      SNR = 69 dBFS  
SINAD = 68.9 dBFS      THD = 85 dBc

图 6-6. FFT for 170-MHz Input Signal



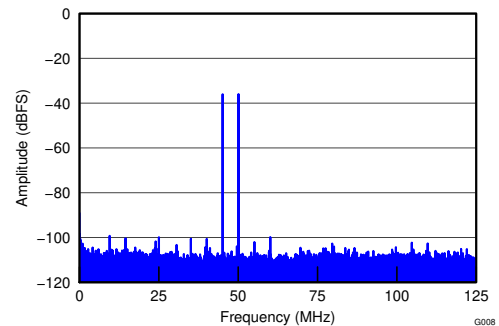
$f_{IN} = 230 \text{ MHz}$       SFDR = 86 dBc      SNR = 68.9 dBFS  
SINAD = 68.5 dBFS      THD = 84 dBc

图 6-7. FFT for 230-MHz Input Signal



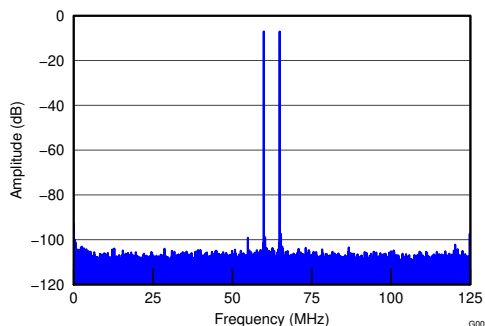
Each Tone at -7-dBFS Amplitude  
 $f_{IN1} = 45 \text{ MHz}$        $f_{IN2} = 50 \text{ MHz}$       SFDR = 92 dBFS  
2-Tone IMD = 87 dBFS

图 6-8. FFT for Two-Tone Input Signal



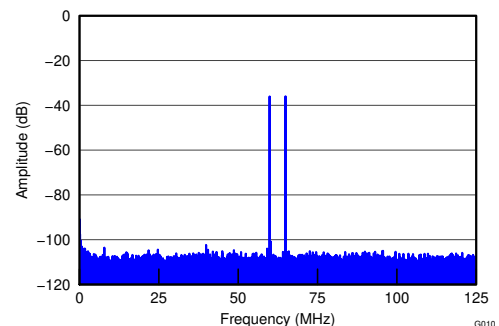
Each Tone at -36-dBFS Amplitude  
 $f_{IN1} = 45 \text{ MHz}$        $f_{IN2} = 50 \text{ MHz}$       SFDR = 99 dBFS  
2-Tone IMD = 99 dBFS

图 6-9. FFT for Two-Tone Input Signal



Each Tone at -7-dBFS Amplitude  
 $f_{IN1} = 185.1 \text{ MHz}$        $f_{IN2} = 190.1 \text{ MHz}$       SFDR = 102 dBFS  
2-Tone IMD = 97 dBFS

图 6-10. FFT for Two-Tone Input Signal



Each Tone at -36-dBFS Amplitude  
 $f_{IN1} = 185.1 \text{ MHz}$        $f_{IN2} = 190.1 \text{ MHz}$       SFDR = 100 dBFS  
2-Tone IMD = 101 dBFS

图 6-11. FFT for Two-Tone Input Signal

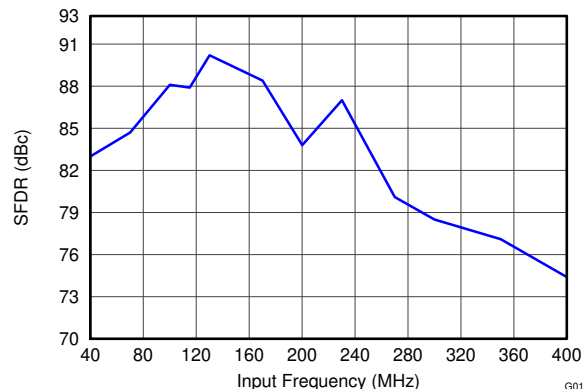
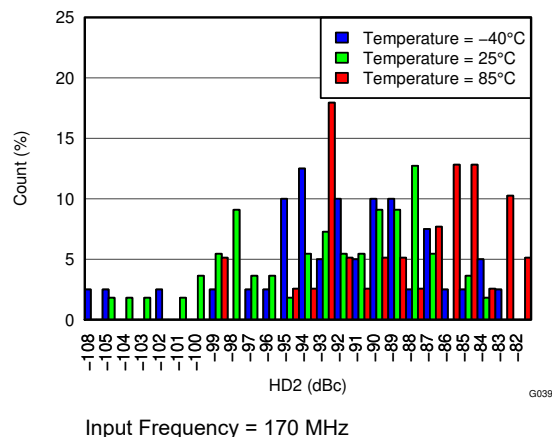


图 6-12. Spurious-Free Dynamic Range vs Input Frequency



Input Frequency = 170 MHz

图 6-13. HD2 Distribution over Multiple Devices

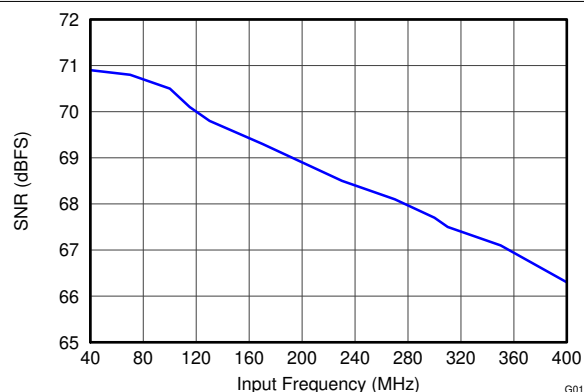


图 6-14. Signal-to-Noise Ratio vs Input Frequency

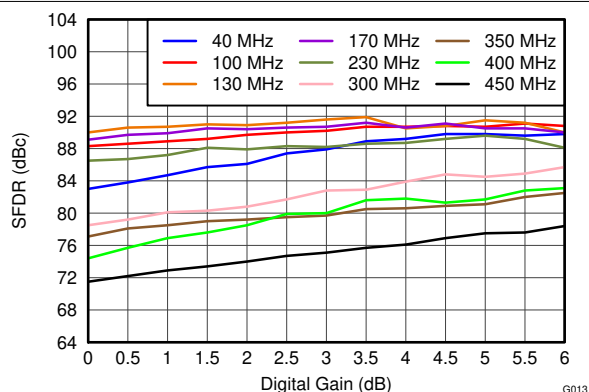


图 6-15. Spurious-Free Dynamic Range vs Digital Gain

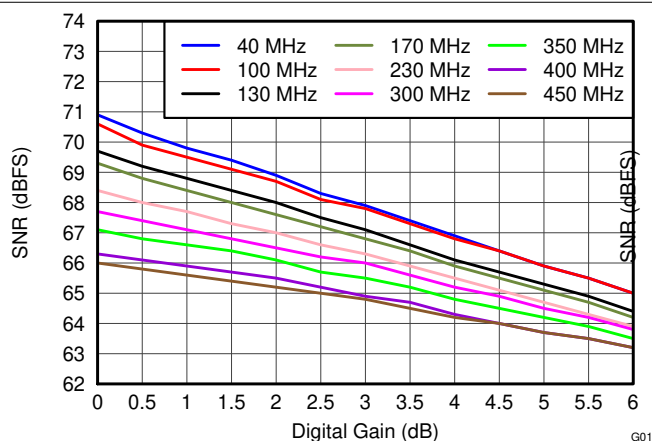


图 6-16. Signal-to-Noise Ratio vs Digital Gain

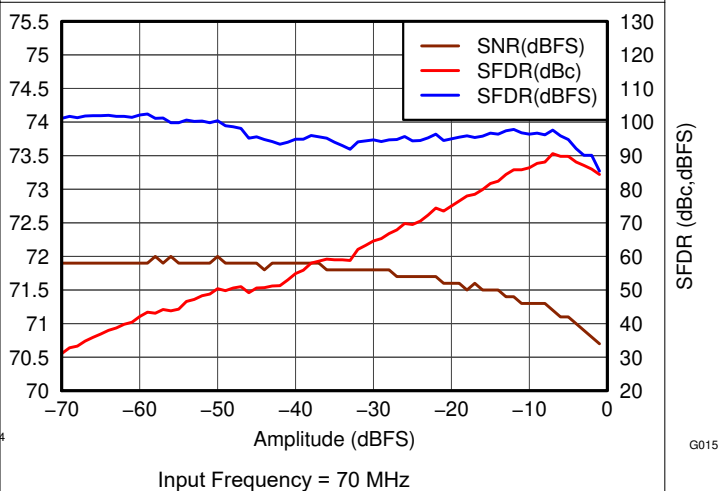


图 6-17. Performance vs Input Amplitude

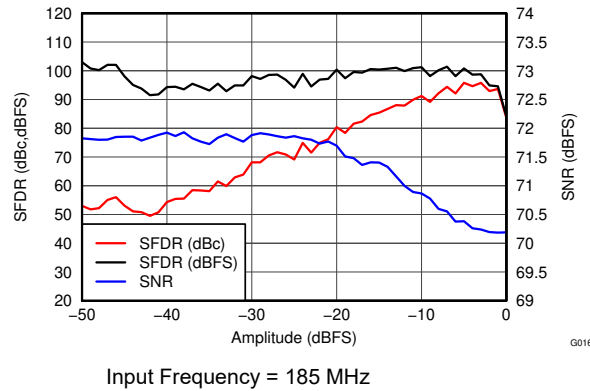


图 6-18. Performance vs Input Amplitude

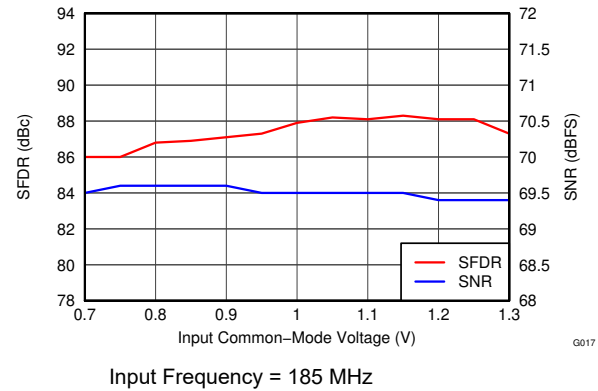


图 6-19. Performance vs Input Common-Mode Voltage

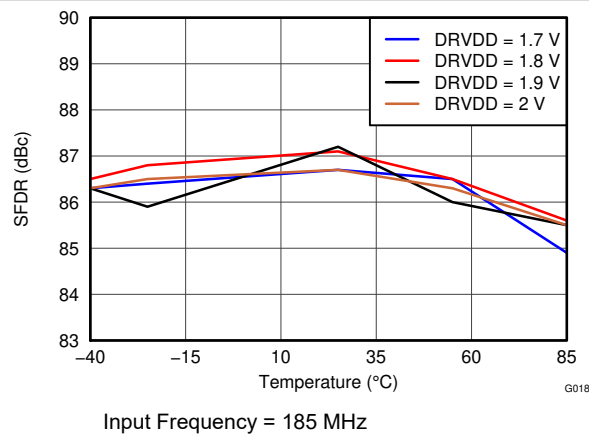


图 6-20. Spurious-Free Dynamic Range vs DRVDD Supply and Temperature

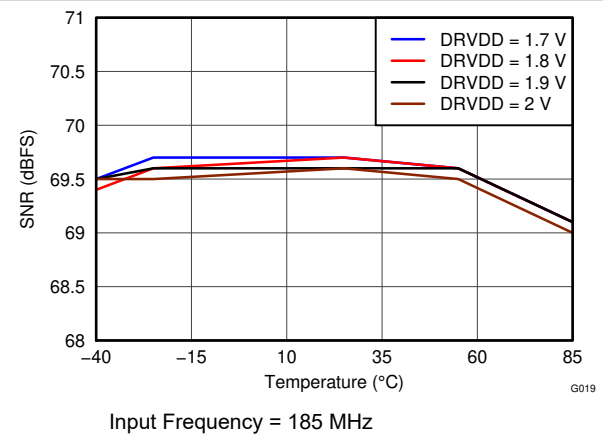


图 6-21. Signal-to-Noise Ratio vs DRVDD Supply and Temperature

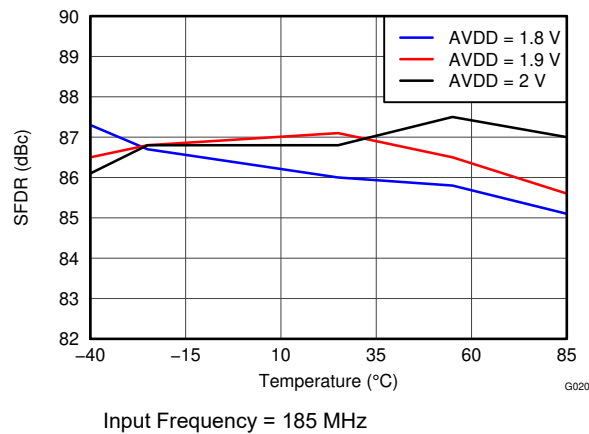


图 6-22. Spurious-Free Dynamic Range vs AVDD Supply and Temperature

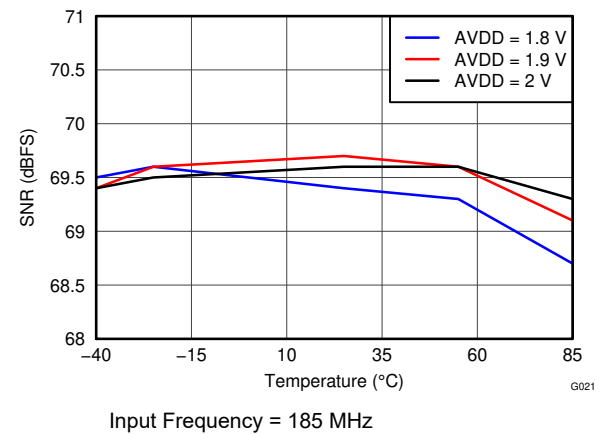


图 6-23. Signal-to-Noise Ratio vs AVDD Supply and Temperature

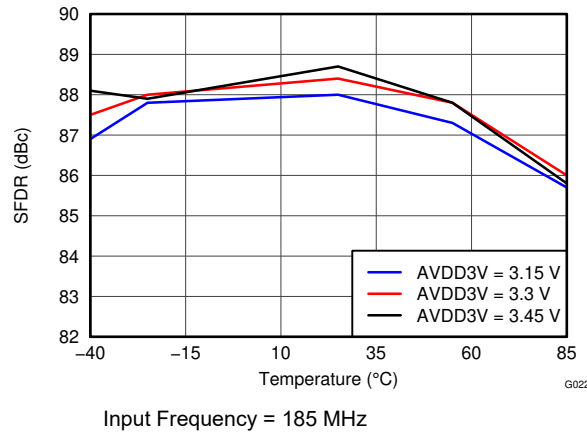


图 6-24. Spurious-Free Dynamic Range vs AVDD3V Supply and Temperature

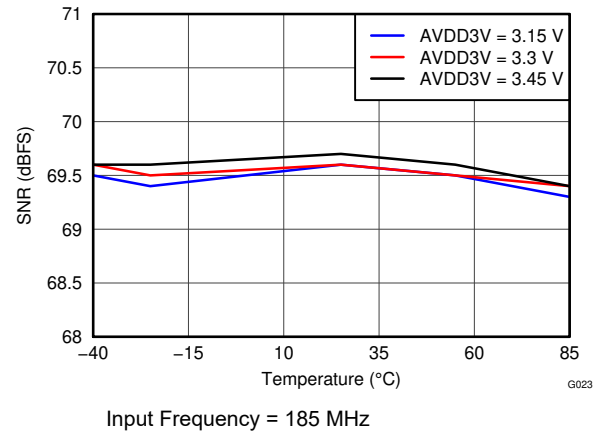


图 6-25. Signal-to-Noise Ratio vs AVDD3V Supply and Temperature

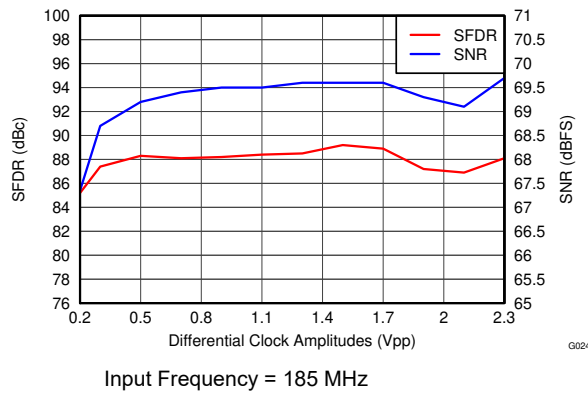


图 6-26. Performance vs Clock Amplitude

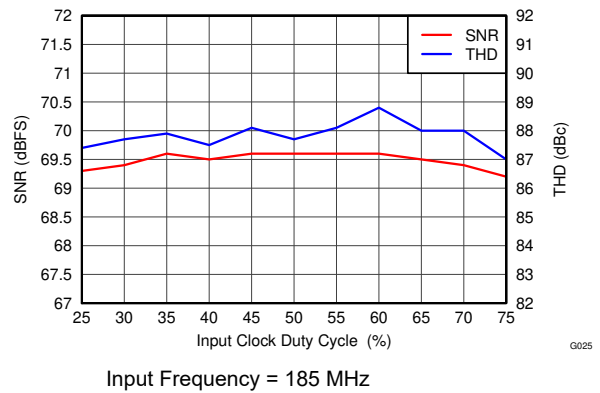


图 6-27. Performance vs Clock Duty Cycle

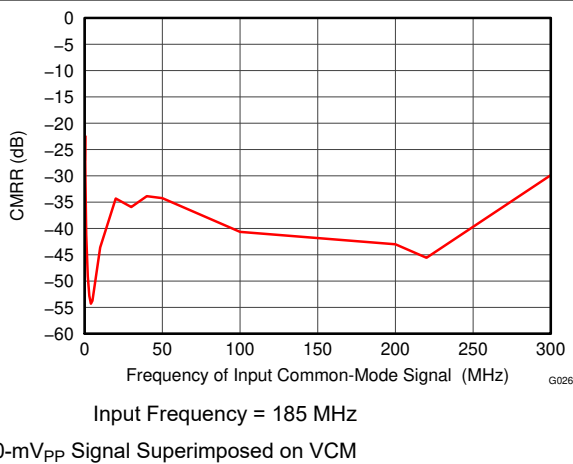


图 6-28. Common-Mode Rejection Ratio Spectrum

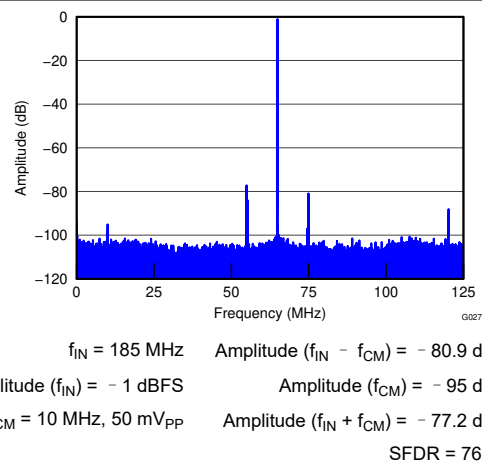
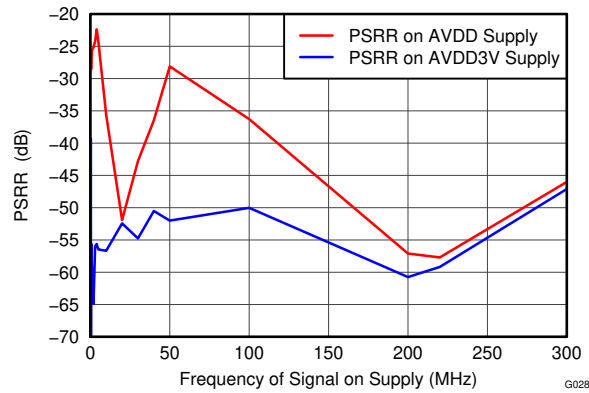


图 6-29. Common-Mode Rejection Ratio vs Test Signal Frequency

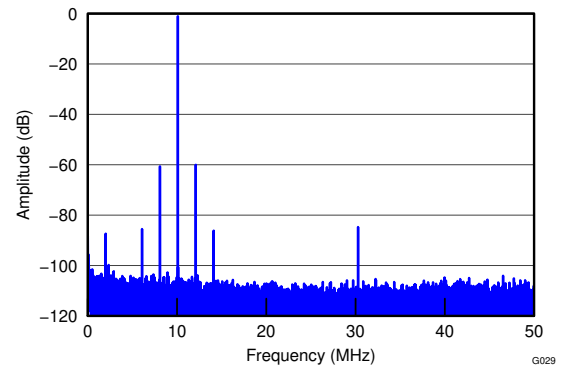




Input Frequency = 10 MHz

50-mV<sub>PP</sub> Signal Superimposed on Supply

**图 6-30. Power-Supply Rejection Ratio Spectrum for AVDD**

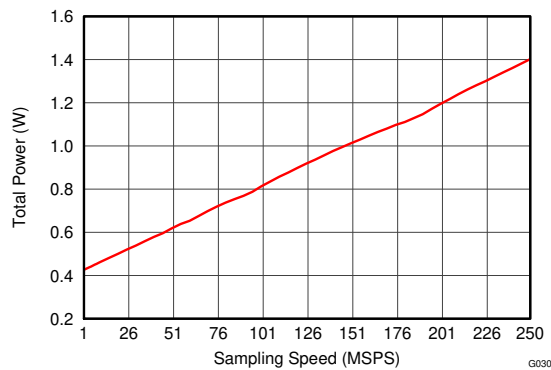


Amplitude ( $f_{IN}$ ) = -1 dBFS      Amplitude ( $f_{PSRR}$ ) = -87 dBFS

$f_{IN}$  = 10 MHz      Amplitude ( $f_{IN} + f_{PSRR}$ ) = -60.6 dBFS

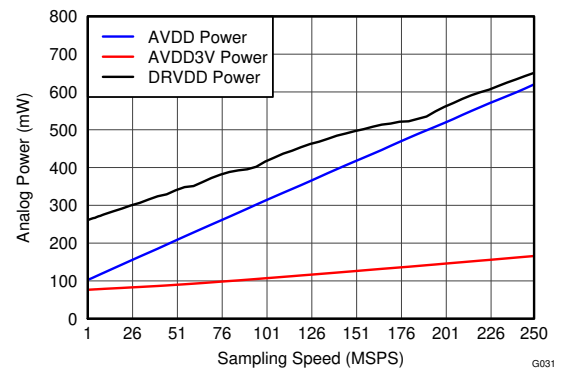
$f_{PSRR}$  = 2 MHz, 50 mV<sub>PP</sub>      Amplitude ( $f_{IN} - f_{PSRR}$ ) = -60 dBFS

**图 6-31. Power-Supply Rejection Ratio vs Test Signal Frequency**



Input Frequency = 185 MHz

**图 6-32. Total Power vs Sampling Frequency**



Input Frequency = 185 MHz

**图 6-33. Power Breakup vs Sampling Frequency**

## 6.10 Typical Characteristics: Contour

At 25°C, AVDD = 1.9 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, rated sampling frequency, 0-dB gain, sine-wave input clock,

1.5-V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

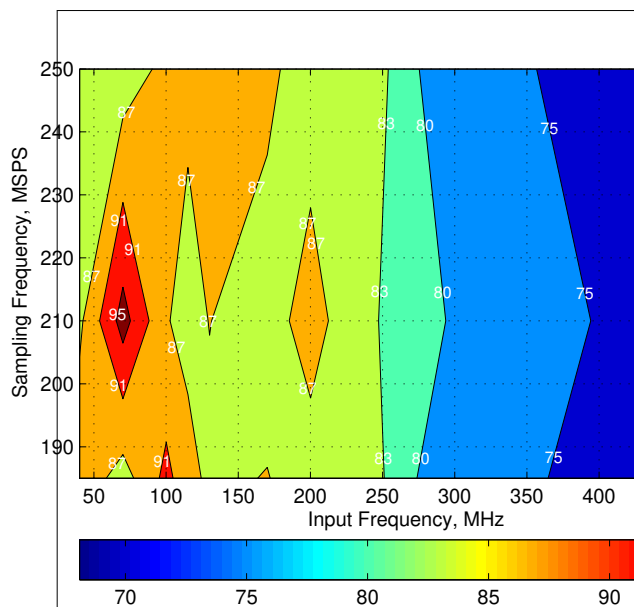


图 6-34. Spurious-Free Dynamic Range (0-dB Gain)

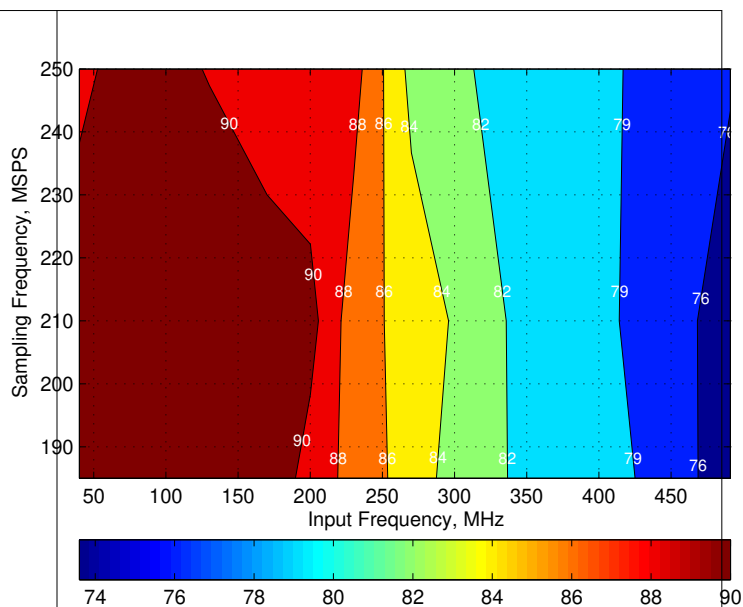


图 6-35. Spurious-Free Dynamic Range (6-dB Gain)

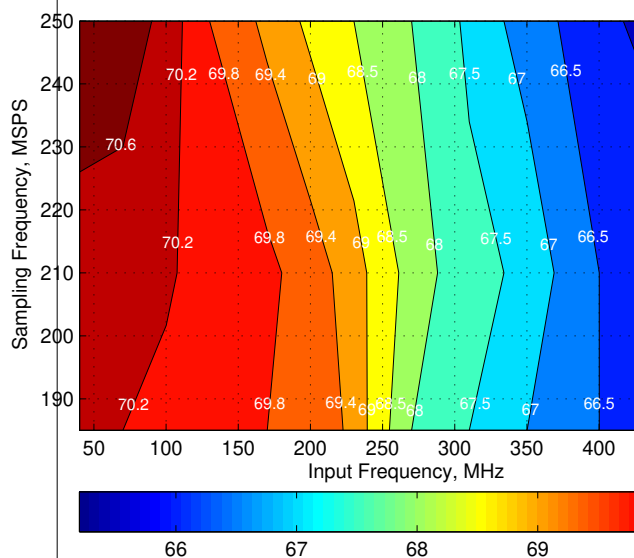


图 6-36. Signal-to-Noise Ratio (0-dB Gain)

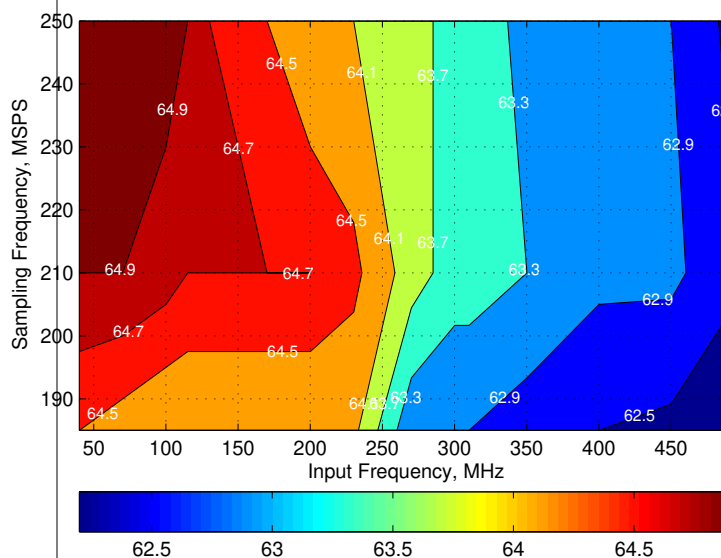


图 6-37. Signal-to-Noise Ratio (6-dB Gain)

## 7 Parameter Measurement Information

### 7.1 LVDS Output Timing

图 7-1 shows a timing diagram of the LVDS output voltage levels. 图 7-2 shows the latency described in the 节 6.7 table.

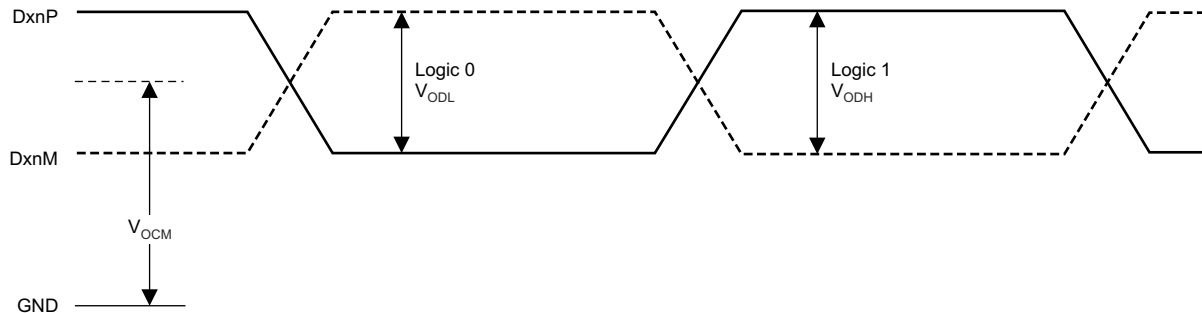


图 7-1. LVDS Output Voltage Levels

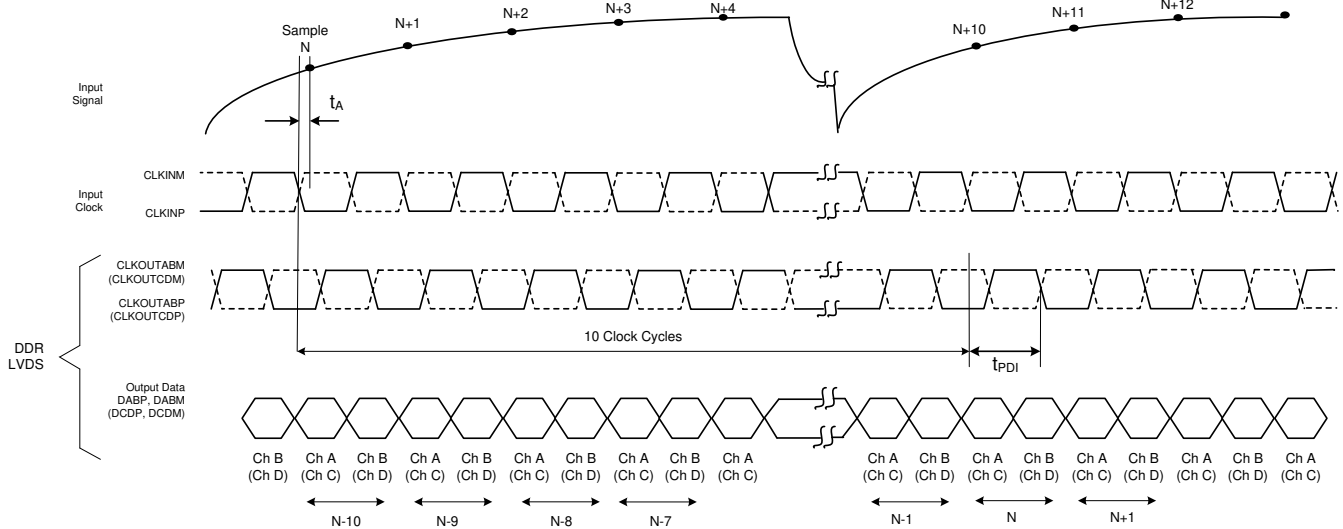


图 7-2. Latency Timing

All 14 data bits of one channel are included in the digital output interface at the same time, as shown in 图 7-3. Channel A and C data are output on the rising edge of the output clock while channels B and D are output on the falling edge of the output clock.

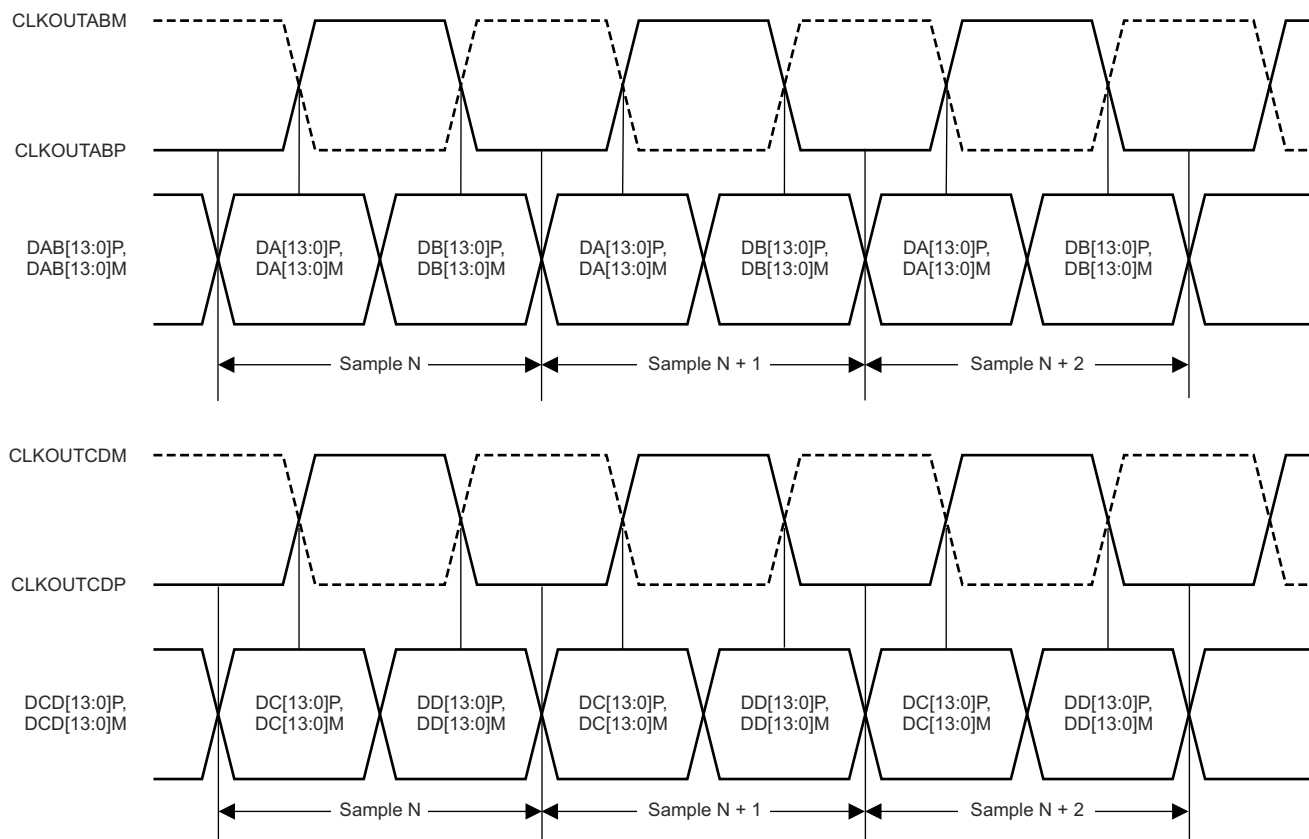


图 7-3. LVDS Output Interface Timing

## 8 Detailed Description

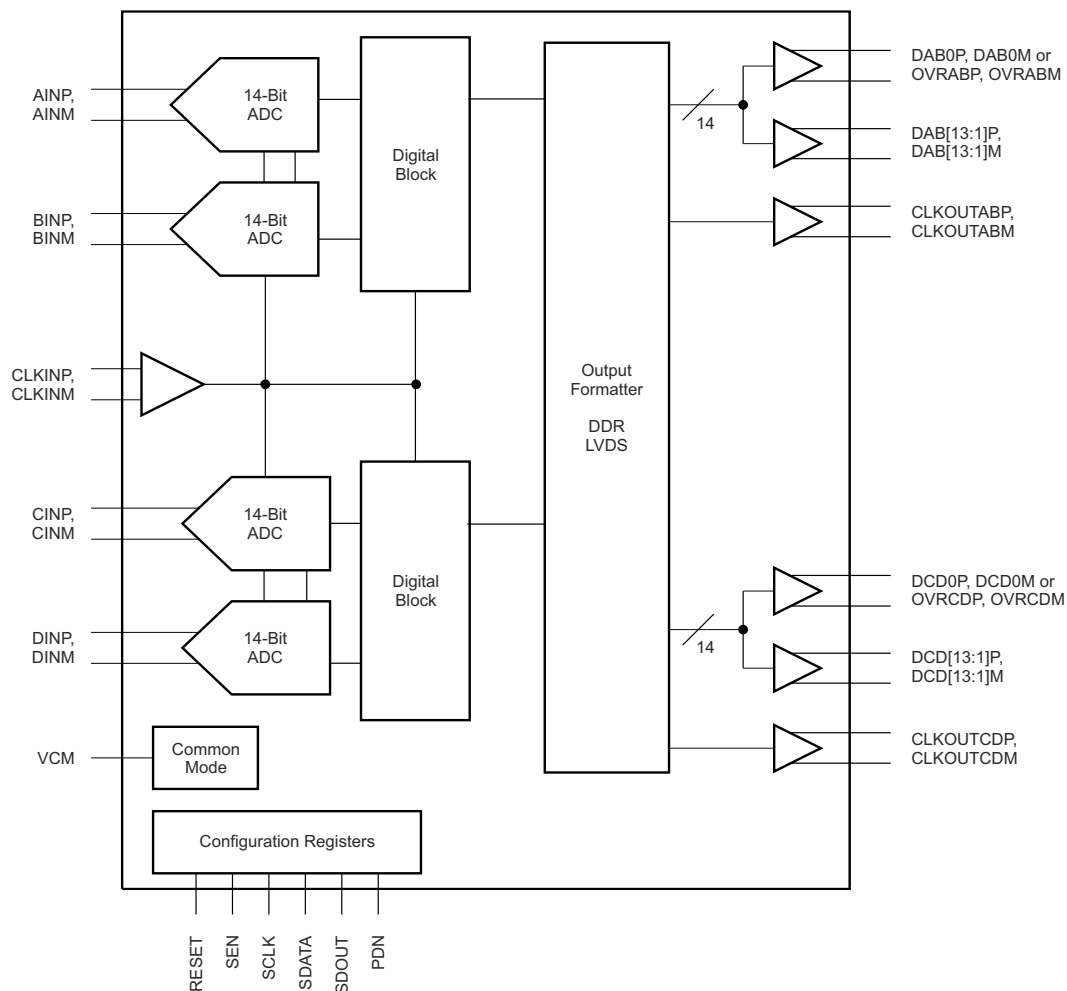
### 8.1 Overview

The ADS4449 belongs to TI's low-power family of quad-channel, 14-bit, analog-to-digital converters (ADCs). High performance is maintained while power is reduced for power-sensitive applications. In addition to its low power and high performance, the ADS4449 has a number of digital features and operating modes to enable design flexibility.

At every falling edge of the input clock, the analog input signal for each channel is sampled simultaneously. The sampled signal in each channel is converted by a pipeline of low-resolution stages. In each stage, the sampled-and-held signal is converted by a high-speed, low-resolution, flash sub-ADC. The difference (residue) between the stage input and quantized equivalent is gained and propagates to the next stage. At every clock, each subsequent stage resolves the sampled input with greater accuracy. The digital outputs from all stages are combined in a digital correction logic block and are digitally processed to create the final code, after a data latency of 10 clock cycles. The digital output is available in a double data rate (DDR) low-voltage differential signaling (LVDS) interface and is coded in binary two's complement format.

The ADS4449 can be configured with a serial programming interface (SPI), as described in the [§ 8.5.1](#) section. In addition, the device has control terminals that control power-down.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Overrange Indication (OVRxx)

After reset, all serial interface register "ALWAYS WRITE 1". Bits must be set to 1. Afterwards, 13-bit data are output on the Dxx13P, Dxx13M to Dxx1P, Dxx1M terminals and overrange information is output on the Dxx0P and Dxx0M terminals (where xx = channels A and B or channels C and D).

When the DIS OVR ON LSB bit is set to 1, 14-bit data are output on the Dxx13P, Dxx13M to Dxx0P, Dxx0M terminals without overrange information on the LSB bits.

The OVR timing diagram (13-bit data with OVR) is shown in 图 8-1. In 14-bit mode, OVR is disabled by setting the DIS OVR ON LSB bit to 1, as shown in 图 8-2.

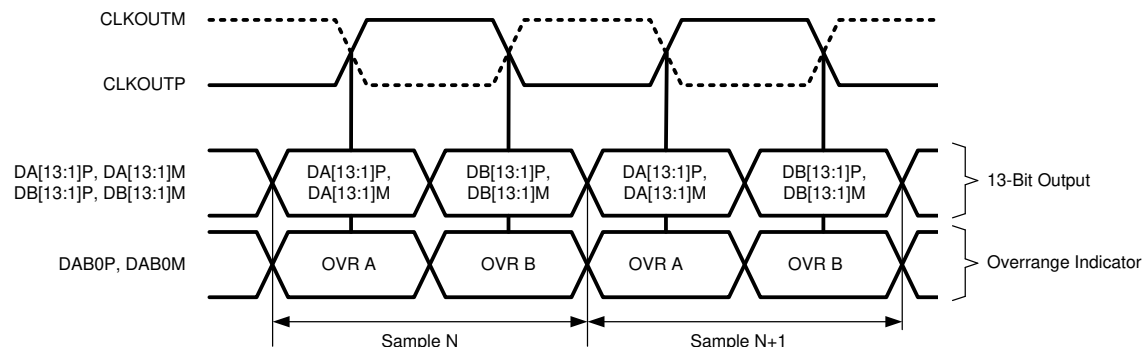


图 8-1. 13-Bit Data with OVR (Register Bits ALWAYS WRITE 1 = 1 and DIS OVR ON LSB = 0)

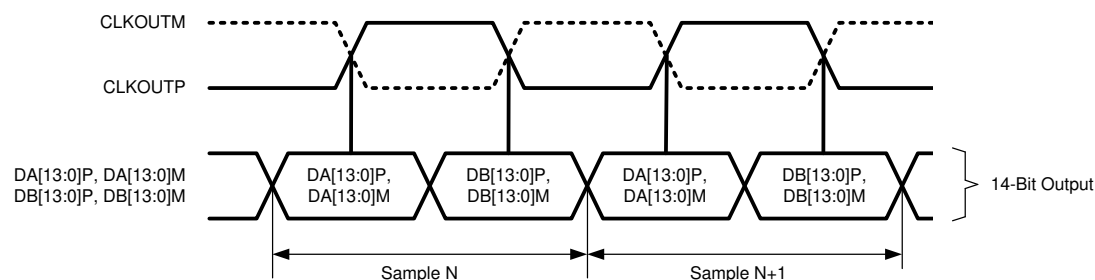


图 8-2. 14-Bit Mode (Register Bits ALWAYS WRITE 1 = 1 and DIS OVR ON LSB = 1)

Normal overrange indication (OVR) shows the event of the device digital output being saturated when the input signal exceeds the ADC full-scale range. Normal OVR has the same latency as digital output data. However, an overrange event can be indicated earlier (than normal latency) by using the fast OVR mode. The fast OVR mode (enabled by default) is triggered seven clock cycles after the overrange condition that occurred at the ADC input. The fast OVR thresholds are programmable with the FAST OVR THRESH PROG bits (refer to 表 8-3, register address C3h). At any time, either normal or fast OVR mode can be programmed on the Dxx0P and Dxx0M terminals.

### 8.3.2 Gain for SFDR and SNR Trade-Off

The device includes gain settings that can be used to obtain improved SFDR performance. The gain is programmable from 0 dB to 6 dB (in 0.5-dB steps) using the DIGITAL GAIN CH X register bits. For each gain setting, the analog input full-scale range scales proportionally, as shown in [表 8-1](#).

**表 8-1. Full-Scale Range Across Gains**

| GAIN (dB) | TYPE                | FULL-SCALE ( $V_{PP}$ ) |
|-----------|---------------------|-------------------------|
| 0         | Default after reset | 2                       |
| 0.5       | Fine, programmable  | 1.89                    |
| 1         | Fine, programmable  | 1.78                    |
| 1.5       | Fine, programmable  | 1.68                    |
| 2         | Fine, programmable  | 1.59                    |
| 2.5       | Fine, programmable  | 1.5                     |
| 3         | Fine, programmable  | 1.42                    |
| 3.5       | Fine, programmable  | 1.34                    |
| 4         | Fine, programmable  | 1.26                    |
| 4.5       | Fine, programmable  | 1.19                    |
| 5         | Fine, programmable  | 1.12                    |
| 5.5       | Fine, programmable  | 1.06                    |
| 6         | Fine, programmable  | 1                       |

SFDR improvement is achieved at the expense of SNR; for each gain setting, SNR degrades by approximately 0.5 dB to 1 dB. SNR degradation is diminished at high input frequencies. As a result, fine gain is very useful at high input frequencies because SFDR improvement is significant with marginal degradation in SNR. Therefore, fine gain can be used to trade-off between SFDR and SNR.

After a reset, the gain function is disabled. To use fine gain:

- First, program the DIGITAL ENABLE bits to enable digital functions.
- This setting enables the gain for all four channels and places the device in a 0-dB gain mode.
- For other gain settings, program the DIGITAL GAIN CH X register bits.

## 8.4 Device Functional Modes

### 8.4.1 Special Performance Modes

Best performance can be achieved by writing certain modes depending upon source impedance, band of operation and sampling speed. 表 8-2 summarizes the different these modes.

表 8-2. High-Performance Modes Summary

| SPECIAL MODES SUMMARY <sup>(1)</sup> |               |            |                                      |                                  |
|--------------------------------------|---------------|------------|--------------------------------------|----------------------------------|
| SPECIAL MODE NAME                    | ADDRESS (Hex) | DATA (Hex) | INPUT FREQUENCIES<br>(Up to 125 MHz) | INPUT FREQUENCIES<br>(> 125 MHz) |
| High-frequency mode                  | F1            | 20         | Not required                         | Must                             |
| High SNR mode <sup>(2)</sup>         | 58            | 20         | Optional                             | Optional                         |
|                                      | 70            | 20         | Optional                             | Optional                         |
|                                      | 88            | 20         | Optional                             | Optional                         |
|                                      | A0            | 20         | Optional                             | Optional                         |
| SPECIAL MODE NAME                    | ADDRESS (Hex) | DATA (Hex) | SAMPLING RATE (Up to<br>200 MSPS)    | SAMPLING RATE<br>(>200MHz)       |
| Low Sampling Rate mode               | 4A            | 1          | Must                                 | Not required                     |
|                                      | 62            | 1          | Must                                 | Not required                     |
|                                      | 7A            | 1          | Must                                 | Not required                     |
|                                      | 92            | 1          | Must                                 | Not required                     |

(1) See the 节 8.5.1 section for details.

(2) High SNR mode improves SNR typically by 1 dB at 170 MHz input frequency. See the 节 8.4.3 section.

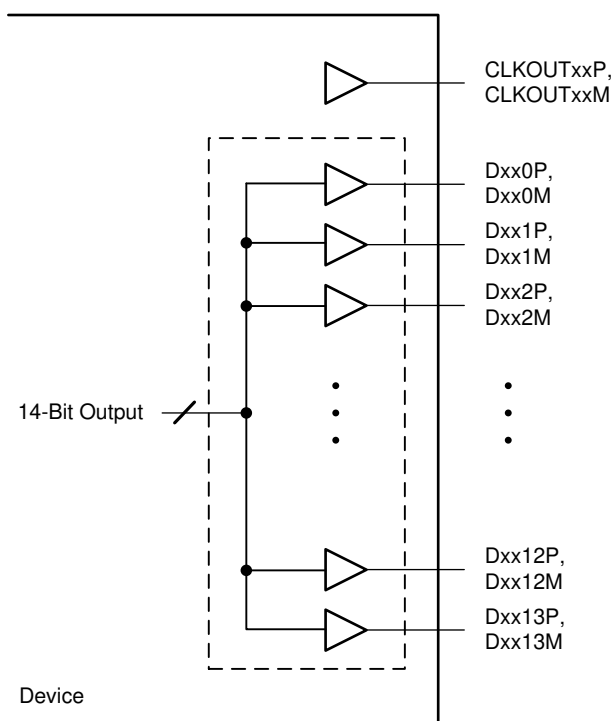
### 8.4.2 Digital Output Information

The device provides 14-bit digital data for each channel and two output clocks in LVDS mode. Output terminals are shared by a pair of channels that are accompanied by one dedicated output clock.

#### 8.4.2.1 DDR LVDS Outputs

In the LVDS interface mode, the data bits and clock are output using LVDS levels. The data bits of two channels are multiplexed and output on each LVDS differential pair of terminals; see 图 8-3 and 图 8-4.





NOTE: xx = channels A and B or C and D.

图 8-3. DDR LVDS Interface

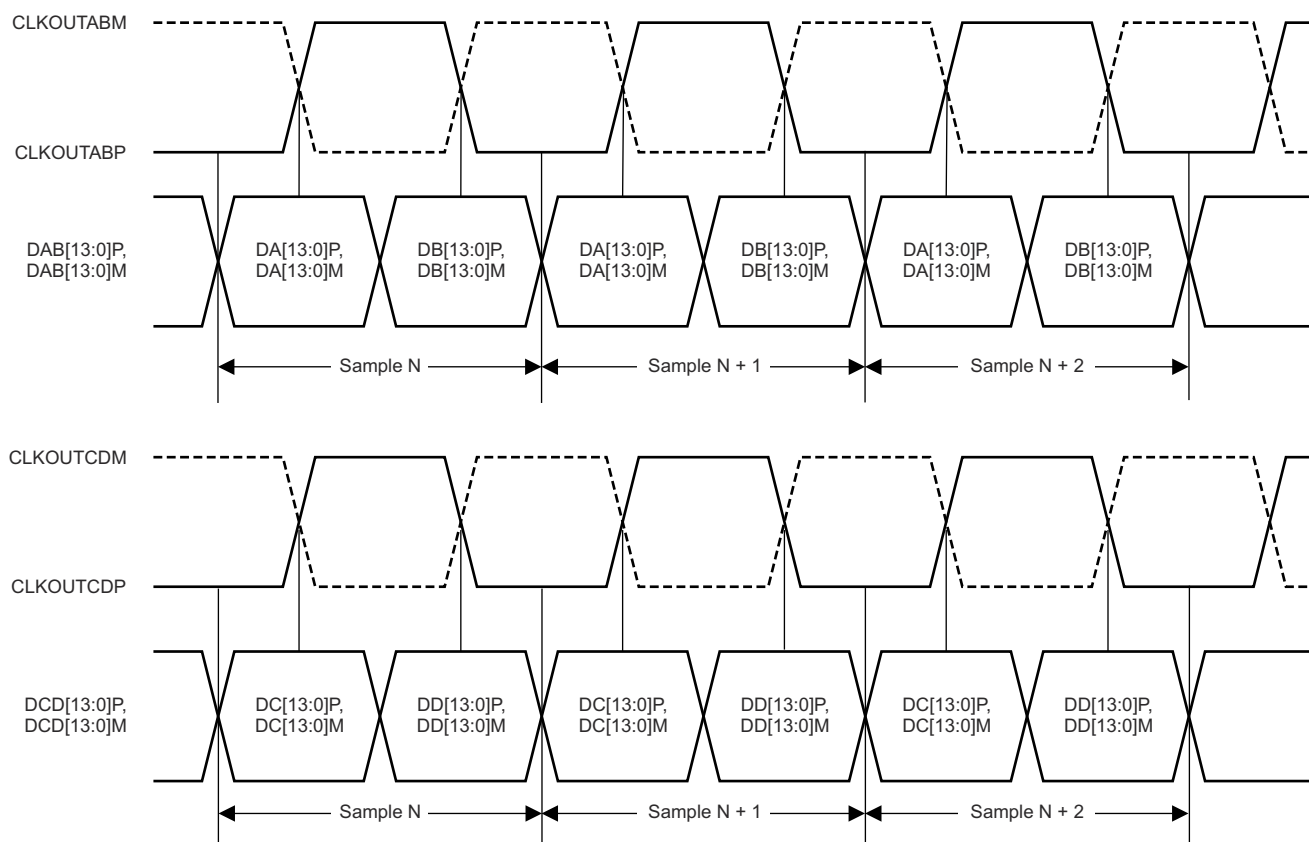


图 8-4. DDR LVDS Interface Timing Diagram

#### 8.4.2.1.1 LVDS Output Data and Clock Buffers

The equivalent circuit of each LVDS output buffer is shown in 图 8-5. After reset, the buffer presents an output impedance of  $100\ \Omega$  to match with the external  $100\text{-}\Omega$  termination.

The  $V_{\text{DIFF}}$  voltage is nominally 350 mV, resulting in an output swing of  $\pm 350\text{ mV}$  with  $100\text{-}\Omega$  external termination. The  $V_{\text{DIFF}}$  voltage is programmable using the LVDS SWING register bits (refer to 表 8-3, register address 01h). The buffer output impedance behaves similar to a source-side series termination. By absorbing reflections from the receiver end, the source-side termination helps improve signal integrity.

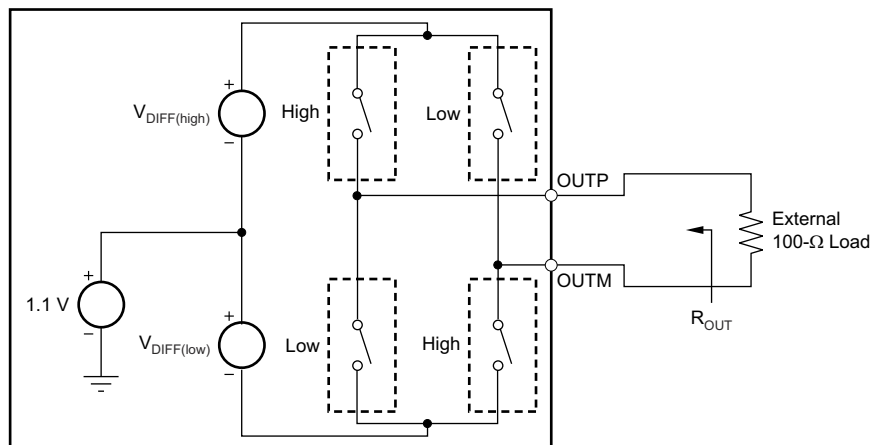


图 8-5. LVDS Buffer Equivalent Circuit

#### 8.4.2.1.2 Output Data Format

The device transmits data in binary two's complement format. In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 3FFh. For a negative input overdrive, the output code is 400h.

#### 8.4.3 Using High SNR Mode Register Settings

The HIGH SNR MODE register settings can be used to further improve the SNR. However, there is a trade off between improved SNR and degraded THD when these settings are used. These settings shut down the internal spectrum-cleaning algorithm, resulting in THD performance degradation. 图 8-6 and 图 8-7 show the effect of using HIGH SNR MODE. SNR improves by approximately 1 dB and THD degrades by 3 dB.

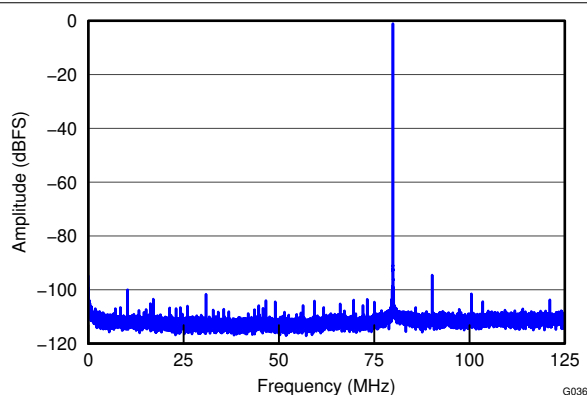


图 8-6. FFT (Default) at 170 MHz

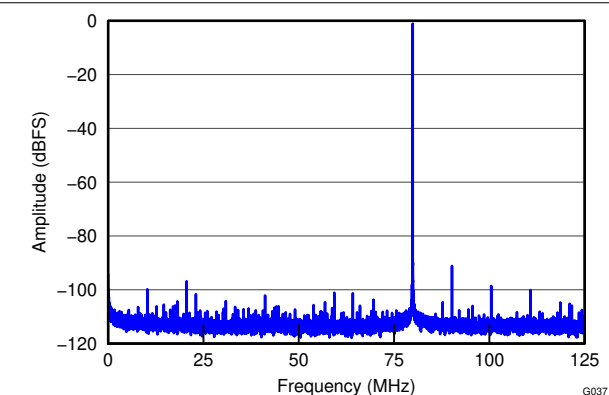


图 8-7. FFT with High SNR Mode at 170 MHz

图 8-8 shows SNR versus input frequency with and without these settings.

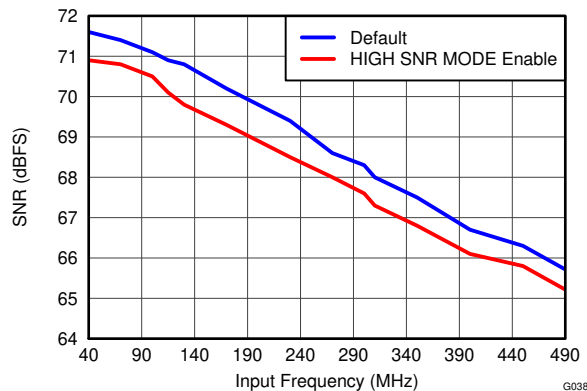


图 8-8. SNR vs Input Frequency with High SNR Mode

To obtain best performance, TI recommends keeping termination impedance between INP and INM low (for instance, at 50  $\Omega$  differential). This setting helps absorb the kickback noise component of the spectrum-cleaning algorithm. However, when higher termination impedances (such as 100  $\Omega$ ) are required, shutting down the spectrum-cleaning algorithm by using the HIGH SNR MODE register settings can be helpful.

#### 8.4.4 Input Common Mode

To ensure a low-noise, common-mode reference, the VCM terminal should be filtered with a 0.1- $\mu$ F, low-inductance capacitor connected to ground. The VCM terminal is designed to directly bias the ADC inputs (refer to 图 9-4 to 图 9-7).

Each ADC input terminal sinks a common-mode current of approximately 1.5  $\mu$ A per MSPS of clock frequency. When a differential amplifier is used to drive the ADC (with dc-coupling), ensure that the output common-mode of the amplifier is within the acceptable input common-mode range of the ADC inputs ( $V_{CM} \pm 25$  mV).

### 8.5 Programming

#### 8.5.1 Serial Interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface input data), and SDOUT (serial interface readback data) terminals. Serially shifting bits into the device is enabled when SEN is low. Serial data (SDATA) are latched at every SCLK falling edge when SEN is active (low). Serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can function with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

##### 8.5.1.1 Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

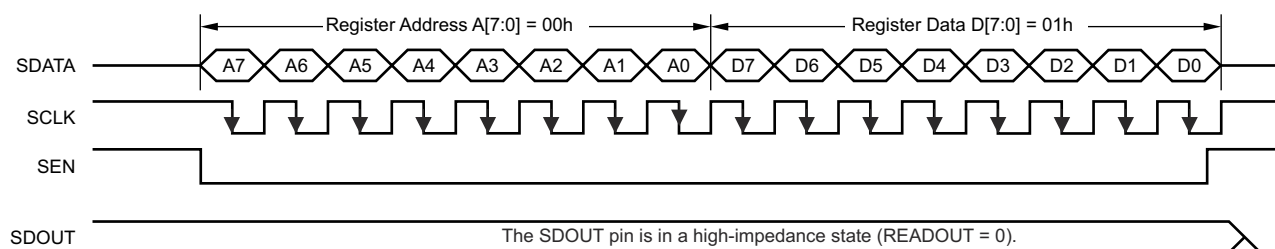
1. Either through a hardware reset by applying a high pulse on the RESET terminal (of widths greater than 10ns), as shown in 图 6-1; or
2. By applying a software reset. When using the serial interface, set the RESET bit (D1 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET terminal is kept low.

### 8.5.1.2 Serial Register Readout

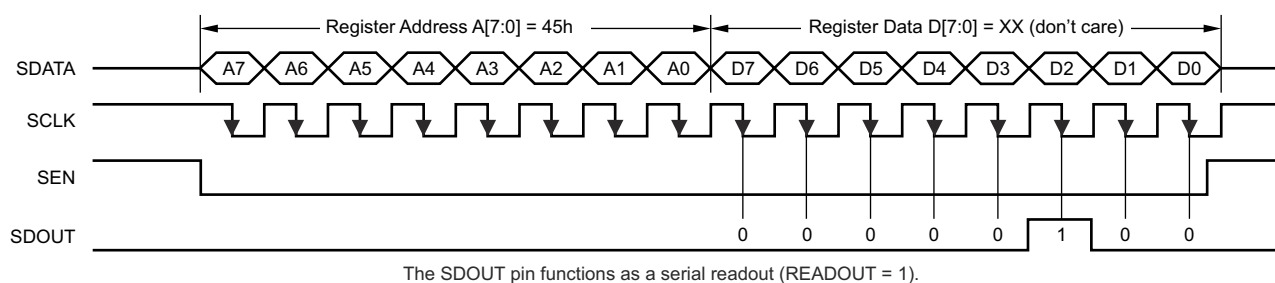
The device includes a mode where the contents of the internal registers can be read back, as shown in 图 8-9. This readback mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and ADC.

1. Set the READOUT register bit to 1. This setting disables any further writes to the registers except register address 00h.
2. Initiate a serial interface cycle specifying the address of the register (A[7:0]) whose content must be read.
3. The device outputs the contents (D[7:0]) of the selected register on the SDOUT terminal (terminal G10).
4. The external controller can latch the contents at the SCLK falling edge.
5. To enable register writes, reset the READOUT register bit to 0.

Note that the contents of register 00h cannot be read back because the register contains RESET and READOUT bits. When the READOUT bit is disabled, the SDOUT terminal is in a high-impedance state. If serial readout is not used, the SDOUT terminal must not be connected (must float).



a) Enable serial readout (READOUT = 1)



b) Read contents of Register 45h. This register is initialized with 04h.

图 8-9. Serial Readout Timing Diagram

SDOUT comes out at the SCLK rising edge with an approximate delay ( $t_{SD\_DELAY}$ ) of 8 ns, as shown in 图 8-10.

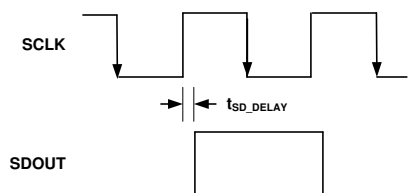


图 8-10. Sdout Delay Timing

## 8.6 Register Maps

表 8-3 summarizes the device registers.

**表 8-3. Register Map**

| REGISTER ADDRESS<br>A[7:0] (Hex) | REGISTER DATA        |                           |                      |                |                             |                        |          |                |
|----------------------------------|----------------------|---------------------------|----------------------|----------------|-----------------------------|------------------------|----------|----------------|
|                                  | D7                   | D6                        | D5                   | D4             | D3                          | D2                     | D1       | D0             |
| 00                               | 0                    | 0                         | 0                    | 0              | 0                           | 0                      | RESET    | READOUT        |
| 01                               | LVDS SWING           |                           |                      |                |                             |                        | 0        | 0              |
| 25                               | DIGITAL GAIN CH B    |                           |                      |                | DIGITAL GAIN BYPASS<br>CH B | TEST PATTERN CH B      |          |                |
| 2B                               | DIGITAL GAIN CH A    |                           |                      |                | DIGITAL GAIN BYPASS<br>CH A | TEST PATTERN CH A      |          |                |
| 31                               | DIGITAL GAIN CH D    |                           |                      |                | DIGITAL GAIN BYPASS<br>CH D | TEST PATTERN CH D      |          |                |
| 37                               | DIGITAL GAIN CH C    |                           |                      |                | DIGITAL GAIN BYPASS<br>CH C | TEST PATTERN CH C      |          |                |
| 3D                               | 0                    | 0                         | OFFSET CORR EN1      | 0              | 0                           | 0                      | 0        | 0              |
| 3F                               | 0                    | 0                         | CUSTOM PATTERN[13:8] |                |                             |                        |          |                |
| 40                               | CUSTOM PATTERN[7:0]  |                           |                      |                |                             |                        |          |                |
| 42                               | 0                    | 0                         | 0                    | 0              | DIGITAL ENABLE              | 0                      | 0        | 0              |
| 45                               | 0                    | 0                         | 0                    | DIS OVR ON LSB | SEL OVR                     | GLOBAL POWER DOWN      | 0        | CONFIG PDN PIN |
| 4A                               | 0                    | 0                         | 0                    | 0              | 0                           | 0                      | 0        | LSR MODE CH A  |
| 62                               | 0                    | 0                         | 0                    | 0              | 0                           | 0                      | 0        | LSR MODE CH B  |
| 7A                               | 0                    | 0                         | 0                    | 0              | 0                           | 0                      | 0        | LSR MODE CH D  |
| 92                               | 0                    | 0                         | 0                    | 0              | 0                           | 0                      | 0        | LSR MODE CH C  |
| A9                               | 0                    | 0                         | 0                    | 0              | CLOCKOUT DELAY PROG CH AB   |                        |          |                |
| AC                               | 0                    | CLOCKOUT DELAY PROG CH CD |                      |                |                             | 0                      | 0        | ALWAYS WRITE 1 |
| C3                               | FAST OVR THRESH PROG |                           |                      |                |                             |                        |          |                |
| C4                               | EN FAST OVR THRESH   | 0                         | 0                    | 0              | 0                           | 0                      | 0        | 0              |
| CF                               | 0                    | 0                         | 0                    | 0              | OFFSET CORR EN2             | 0                      | 0        | 0              |
| D6                               | ALWAYS WRITE 1       | 0                         | 0                    | 0              | 0                           | 0                      | 0        | 0              |
| D7                               | 0                    | 0                         | 0                    | 0              | ALWAYS WRITE 1              | ALWAYS WRITE 1         | 0        | 0              |
| F1                               | 0                    | 0                         | HIGH FREQ MODE       | 0              | 0                           | ENABLE LVDS SWING PROG |          |                |
| 58                               | 0                    | 0                         | HIGH SNR MODE CH A   | 0              | 0                           | 0                      | 0        | 0              |
| 59                               | ALWAYS WRITE 1       | 0                         | 0                    | 0              | 0                           | 0                      | 0        | 0              |
| 70                               | 0                    | 0                         | HIGH SNR MODE CH B   | 0              | 0                           | 0                      | 0        | 0              |
| 71                               | ALWAYS WRITE 1       | 0                         | 0                    | 0              | 0                           | 0                      | 0        | 0              |
| 88                               | 0                    | 0                         | HIGH SNR MODE CH D   | 0              | 0                           | 0                      | 0        | 0              |
| 89                               | ALWAYS WRITE 1       | 0                         | 0                    | 0              | 0                           | 0                      | 0        | 0              |
| A0                               | 0                    | 0                         | HIGH SNR MODE CH C   | 0              | 0                           | 0                      | 0        | 0              |
| A1                               | ALWAYS WRITE 1       | 0                         | 0                    | 0              | 0                           | 0                      | 0        | 0              |
| FE                               | 0                    | 0                         | 0                    | 0              | PDN CH D                    | PDN CH C               | PDN CH A | PDN CH B       |

## 8.6.1 Register Description

### 8.6.1.1 Register Address 00h (Default = 00h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0       |
|---|---|---|---|---|---|-------|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | RESET | READOUT |

**Bits 7-2** Always write 0

**Bit 1** RESET: Software reset applied

This bit resets all internal registers to the default values and self-clears to 0.

**Bit 0** READOUT: Serial readout

This bit sets the serial readout of the registers.

0 = Serial readout of registers disabled; the SDOOUT terminal is placed in a high-impedance state. (default)

1 = Serial readout enabled; the SDOOUT terminal functions as a serial data readout with CMOS logic levels running from the DRVDD supply.

### 8.6.1.2 Register Address 01h (Default = 00h)

| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|---|---|---|---|---|---|
| LVDS SWING |   |   |   |   |   | 0 | 0 |

**Bits 7-2** LVDS SWING: LVDS swing programmability

These bits program the LVDS swing only after the ENABLE LVDS SWING PROG bits are set to 11.

000000 = Default LVDS swing;  $\pm 350$  mV with an external 100- $\Omega$  termination (default)

011011 =  $\pm 420$ -mV LVDS swing with an external 100- $\Omega$  termination

110010 =  $\pm 470$ -mV LVDS swing with an external 100- $\Omega$  termination

010100 =  $\pm 560$ -mV LVDS swing with an external 100- $\Omega$  termination

001111 =  $\pm 160$ -mV LVDS swing with an external 100- $\Omega$  termination

**Bits 1-0** Always write 0

### 8.6.1.3 Register Address 25h (Default = 00h)

| 7                 | 6 | 5 | 4 | 3                           | 2                 | 1 | 0 |
|-------------------|---|---|---|-----------------------------|-------------------|---|---|
| DIGITAL GAIN CH B |   |   |   | DIGITAL GAIN<br>BYPASS CH B | TEST PATTERN CH B |   |   |

#### Bits 7-4

#### DIGITAL GAIN CH B: Channel B digital gain programmability

These bits set the digital gain programmability from 0 dB to 6 dB in 0.5-dB steps for channel B. Set the DIGITAL ENABLE bit to 1 beforehand to enable this feature.

0000 = 0-dB gain (default)  
 0001 = 0.5-dB gain  
 0010 = 1-dB gain  
 0011 = 1.5-dB gain  
 0100 = 2-dB gain  
 0101 = 2.5-dB gain  
 0110 = 3-dB gain  
 0111 = 3.5-dB gain  
 1000 = 4-dB gain  
 1001 = 4.5-dB gain  
 1010 = 5-dB gain  
 1011 = 5.5-dB gain  
 1100 = 6-dB gain

#### Bit 3

#### DIGITAL GAIN BYPASS CH B: Channel B digital gain bypass

0 = Normal operation (default)  
 1 = Digital gain feature for channel B is bypassed

#### Bits 2-0

#### TEST PATTERN CH B: Channel B test pattern programmability

These bits program the test pattern for channel B.

000 = Normal operation (default)  
 001 = Outputs all 0s  
 010 = Outputs all 1s  
 011 = Outputs toggle pattern

Output data ([D:0]) are an alternating sequence of 01010101010101 and 10101010101010.

100 = Outputs digital ramp

Output data increments by one 14-bit LSB every clock cycle from code 0 to code 16383

101 = Outputs custom pattern

To program a test pattern, use the CUSTOM PATTERN D[13:0] bits of registers 3Fh and 40h.

110 = Unused  
 111 = Unused

#### 8.6.1.4 Register Address 2bh (Default = 00h)

| 7                 | 6 | 5 | 4 | 3                        | 2                 | 1 | 0 |
|-------------------|---|---|---|--------------------------|-------------------|---|---|
| DIGITAL GAIN CH A |   |   |   | DIGITAL GAIN BYPASS CH A | TEST PATTERN CH A |   |   |

##### Bits 7-4

##### DIGITAL GAIN CH A: Channel A digital gain programmability

These bits set the digital gain programmability from 0 dB to 6 dB in 0.5-dB steps for channel A. Set the DIGITAL ENABLE bit to 1 beforehand to enable this feature.

0000 = 0-dB gain (default)  
 0001 = 0.5-dB gain  
 0010 = 1-dB gain  
 0011 = 1.5-dB gain  
 0100 = 2-dB gain  
 0101 = 2.5-dB gain  
 0110 = 3-dB gain  
 0111 = 3.5-dB gain  
 1000 = 4-dB gain  
 1001 = 4.5-dB gain  
 1010 = 5-dB gain  
 1011 = 5.5-dB gain  
 1100 = 6-dB gain

##### Bit 3

##### DIGITAL GAIN BYPASS CH A: Channel A digital gain bypass

0 = Normal operation (default)  
 1 = Digital gain feature for channel A is bypassed

##### Bits 2-0

##### TEST PATTERN CH A: Channel A test pattern programmability

These bits program the test pattern for channel A.

000 = Normal operation (default)  
 001 = Outputs all 0s  
 010 = Outputs all 1s  
 011 = Outputs toggle pattern

Output data ([D:0]) are an alternating sequence of 01010101010101 and 10101010101010.

100 = Outputs digital ramp

Output data increments by one 14-bit LSB every clock cycle from code 0 to code 16383

101 = Outputs custom pattern

To program a test pattern, use the CUSTOM PATTERN D[13:0] bits of registers 3Fh and 40h.

110 = Unused  
 111 = Unused



### 8.6.1.5 Register Address 31h (Default = 00h)

| 7                 | 6 | 5 | 4 | 3                           | 2                 | 1 | 0 |
|-------------------|---|---|---|-----------------------------|-------------------|---|---|
| DIGITAL GAIN CH D |   |   |   | DIGITAL GAIN<br>BYPASS CH D | TEST PATTERN CH D |   |   |

#### Bits 7-4

#### DIGITAL GAIN CH D: Channel D digital gain programmability

These bits set the digital gain programmability from 0 dB to 6 dB in 0.5-dB steps for channel D. Set the DIGITAL ENABLE bit to 1 beforehand to enable this feature.

0000 = 0-dB gain (default)  
 0001 = 0.5-dB gain  
 0010 = 1-dB gain  
 0011 = 1.5-dB gain  
 0100 = 2-dB gain  
 0101 = 2.5-dB gain  
 0110 = 3-dB gain  
 0111 = 3.5-dB gain  
 1000 = 4-dB gain  
 1001 = 4.5-dB gain  
 1010 = 5-dB gain  
 1011 = 5.5-dB gain  
 1100 = 6-dB gain

#### Bit 3

#### DIGITAL GAIN BYPASS CH D: Channel D digital gain bypass

0 = Normal operation (default)  
 1 = Digital gain feature for channel A is bypassed

#### Bits 2-0

#### TEST PATTERN CH D: Channel D test pattern programmability

These bits program the test pattern for channel D.

000 = Normal operation (default)  
 001 = Outputs all 0s  
 010 = Outputs all 1s  
 011 = Outputs toggle pattern

Output data ([D:0]) are an alternating sequence of 01010101010101 and 10101010101010.

100 = Outputs digital ramp

Output data increments by one 14-bit LSB every clock cycle from code 0 to code 16383

101 = Outputs custom pattern

To program test pattern, use the CUSTOM PATTERN D[13:0] bits of registers 3Fh and 40h.

110 = Unused  
 111 = Unused

### 8.6.1.6 Register Address 37h (Default = 00h)

| 7                 | 6 | 5 | 4 | 3                           | 2                 | 1 | 0 |
|-------------------|---|---|---|-----------------------------|-------------------|---|---|
| DIGITAL GAIN CH C |   |   |   | DIGITAL GAIN<br>BYPASS CH C | TEST PATTERN CH C |   |   |

#### Bits 7-4

#### DIGITAL GAIN CH C: Channel C digital gain programmability

These bits set the digital gain programmability from 0 dB to 6 dB in 0.5-dB steps for channel C. Set the DIGITAL ENABLE bit to 1 beforehand to enable this feature.

0000 = 0-dB gain (default)  
 0001 = 0.5-dB gain  
 0010 = 1-dB gain  
 0011 = 1.5-dB gain  
 0100 = 2-dB gain  
 0101 = 2.5-dB gain  
 0110 = 3-dB gain  
 0111 = 3.5-dB gain  
 1000 = 4-dB gain  
 1001 = 4.5-dB gain  
 1010 = 5-dB gain  
 1011 = 5.5-dB gain  
 1100 = 6-dB gain

#### Bit 3

#### DIGITAL GAIN BYPASS CH C: Channel C digital gain bypass

0 = Normal operation (default)  
 1 = Digital gain feature for channel A is bypassed

#### Bits 2-0

#### TEST PATTERN CH C: Channel C test pattern programmability

These bits program the test pattern for channel C.

000 = Normal operation (default)  
 001 = Outputs all 0s  
 010 = Outputs all 1s  
 011 = Outputs toggle pattern

Output data ([D:0]) are an alternating sequence of 01010101010101 and 10101010101010.

100 = Outputs digital ramp

Output data increments by one 14-bit LSB every clock cycle from code 0 to code 16383

101 = Outputs custom pattern

To program a test pattern, use the CUSTOM PATTERN D[13:0] bits of registers 3Fh and 40h.

110 = Unused  
 111 = Unused

### 8.6.1.7 Register Address 3dh (Default = 00h)

| 7 | 6 | 5               | 4 | 3 | 2 | 1 | 0 |
|---|---|-----------------|---|---|---|---|---|
| 0 | 0 | OFFSET CORR EN1 | 0 | 0 | 0 | 0 | 0 |

Bits 7-6

Always write 0

Bit 5

**OFFSET CORR EN1: Offset correction setting**

This bit enables the offset correction feature for all four channels after the DIGITAL ENABLE bit is set to '1,' correcting mid-code to 8191. In addition, write the OFFSET CORR EN2 bit (register CFh, value 08h) for proper operation of the offset correction feature.

0 = Offset correction disabled (default)

1 = Offset correction enabled

Bits 4-0

Always write 0

### 8.6.1.8 Register Address 3fh (Default = 00h)

| 7 | 6 | 5                  | 4                  | 3                  | 2                  | 1                 | 0                 |
|---|---|--------------------|--------------------|--------------------|--------------------|-------------------|-------------------|
| 0 | 0 | CUSTOM PATTERN D13 | CUSTOM PATTERN D12 | CUSTOM PATTERN D11 | CUSTOM PATTERN D10 | CUSTOM PATTERN D9 | CUSTOM PATTERN D8 |

Bits 7-6

Always write 0

Bits 5-0

**CUSTOM PATTERN D[13:8]**

Set the custom pattern using these bits for all four channels.

### 8.6.1.9 Register Address 40h (Default = 00h)

| 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| CUSTOM PATTERN D7 | CUSTOM PATTERN D6 | CUSTOM PATTERN D5 | CUSTOM PATTERN D4 | CUSTOM PATTERN D3 | CUSTOM PATTERN D2 | CUSTOM PATTERN D1 | CUSTOM PATTERN D0 |

Bits 7-0

**CUSTOM PATTERN D[7:0]**

Set the custom pattern using these bits for all four channels.

### 8.6.1.10 Register Address 42h (Default = 00h)

| 7 | 6 | 5 | 4 | 3              | 2 | 1 | 0 |
|---|---|---|---|----------------|---|---|---|
| 0 | 0 | 0 | 0 | DIGITAL ENABLE | 0 | 0 | 0 |

Bits 7-4

Always write 0

Bit 3

**DIGITAL ENABLE**

1 = Digital gain and offset correction features disabled

1 = Digital gain and offset correction features enabled

Bits 2-0

Always write 0

**8.6.1.11 Register Address 45h (Default = 00h)**

| 7 | 6 | 5 | 4                 | 3       | 2                    | 1 | 0                 |
|---|---|---|-------------------|---------|----------------------|---|-------------------|
| 0 | 0 | 0 | DIS OVR ON<br>LSB | SEL OVR | GLOBAL<br>POWER DOWN | 0 | CONFIG PDN<br>PIN |

**Bits 7-5****Always write 0****Bit 4****DIS OVR ON LSB**

0 = Effective ADC resolution is 13 bits (the LSB of a 14-bit output is OVR) (default)  
 1 = ADC resolution is 14 bits

**Bit 3****SEL OVR: OVR selection**

0 = Fast OVR selected (default)  
 1 = Normal OVR selected. See the [§ 8.3.1](#) section for details.

**Bit 2****GLOBAL POWER DOWN**

0 = Normal operation (default)  
 1 = Global power down. All ADC channels, internal references, and output buffers are powered down. Wakeup time from this mode is slow (100  $\mu$ s).

**Bit 1****Always write 0****Bit 0****CONFIG PDN PIN**

Use this bit to configure PDN terminal.  
 0 = The PDN terminal functions as a standby terminal. All channels are put in standby. Wake-up time from standby mode is fast (10  $\mu$ s). (default)  
 1 = The PDN terminal functions as a global power-down terminal. All ADC channels, internal references, and output buffers are powered down. Wake-up time from global power mode is slow (100  $\mu$ s).

**8.6.1.12 Register Address 4ah (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|---|---|---|---|---|---|---|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | LSR CH A |

**Bits 7-1****Always write 0****Bit 0****LSR CH A**

Use this bit to put Channel A into Low Sampling Rate Mode when sampling at a rate below 200MSPS.

**8.6.1.13 Register Address 62h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|---|---|---|---|---|---|---|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | LSR CH B |

**Bits 7-1****Always write 0****Bit 0****LSR CH B: Enables Low Sampling Rate Mode for channel B**

Use this bit to put Channel B into Low Sampling Rate Mode when sampling at a rate below 200MSPS.

**8.6.1.14 Register Address 7ah (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|---|---|---|---|---|---|---|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | LSR CH D |

**Bits 7-1****Always write 0****Bit 0****LSR CH D: Enables Low Sampling Rate Mode for channel D**

Use this bit to put Channel D into Low Sampling Rate Mode when sampling at a rate below 200MSPS.

### 8.6.1.15 Register Address 92h (Default = 00h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|---|---|---|---|---|---|---|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | LSR CH C |

**Bits 7-1**

**Always write 0**

**Bit 0**

**LSR CH C: Enables Low Sampling Rate Mode for channel C**

Use this bit to put Channel C into Low Sampling Rate Mode when sampling at a rate below 200MSPS.

### 8.6.1.16 Register Address A9h (Default = 00h)

| 7 | 6 | 5 | 4 | 3                         | 2 | 1 | 0 |
|---|---|---|---|---------------------------|---|---|---|
| 0 | 0 | 0 | 0 | CLOCKOUT DELAY PROG CH AB |   |   |   |

**Bits 7-4**

**Always write 0**

**Bits 3-0**

**CLOCKOUT DELAY PROG CH AB**

These bits program the clock out delay for channels A and B, see 表 8-4.

### 8.6.1.17 Register Address Ach (Default = 00h)

| 7 | 6                         | 5 | 4 | 3 | 2 | 1 | 0                 |
|---|---------------------------|---|---|---|---|---|-------------------|
| 0 | CLOCKOUT DELAY PROG CH CD |   |   |   | 0 | 0 | ALWAYS<br>WRITE 1 |

**Bit 7** Always write 0

**Bits 6-4** CLOCKOUT DELAY PROG CH CD

These bits program the clock out delay for channels C and D, as shown in 表 8-4 .

**Bits 2-1** Always write 0

**Bit 0** Always write 1

This bit is set to 0 by default. User **must** set it to 1 after reset or power-up.

**表 8-4. Clockout Delay Programmability For All Channels**

| CLOCKOUT DELAY PROG CHxx | DELAY (ps)  |
|--------------------------|-------------|
| 0000 (default)           | 0 (default) |
| 0001                     | – 30        |
| 0010                     | 70          |
| 0011                     | 30          |
| 0100                     | – 150       |
| 0101                     | – 180       |
| 0110                     | – 70        |
| 0111                     | – 110       |
| 1000                     | 270         |
| 1001                     | 230         |
| 1010                     | 340         |
| 1011                     | 300         |
| 1100                     | 140         |
| 1101                     | 110         |
| 1110                     | 200         |
| 1111                     | 170         |

### 8.6.1.18 Register Address C3h (Default = 00h)

| 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------|---|---|---|---|---|---|---|
| FAST OVR THRESH PROG |   |   |   |   |   |   |   |

**Bits 7-0** FAST OVR THRESH PROG

The device has a fast OVR mode that indicates an overload condition at the ADC input. The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the FAST OVR THRESH PROG bits.

FAST OVR is triggered seven output clock cycles after the overload condition occurs. To enable the FAST OVR programmability, enable the EN FAST OVR THRESH register bit. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESH PROG bits] / 255).

After reset, when EN FAST OVR THRESH PROG is set, the default value of the FAST OVR THRESH PROG bits is 230 (decimal).

#### 8.6.1.19 Register Address C4h (Default = 00h)

| 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|---|---|---|---|---|---|---|
| EN FAST OVR THRESH | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7

**EN FAST OVR THRESH**

This bit enables the device to be programmed to select the fast OVR threshold.

Bits 6-0

**Always write 0**

#### 8.6.1.20 Register Address Cfh (Default = 00h)

| 7 | 6 | 5 | 4 | 3               | 2 | 1 | 0 |
|---|---|---|---|-----------------|---|---|---|
| 0 | 0 | 0 | 0 | OFFSET CORR EN2 | 0 | 0 | 0 |

Bits 7-4

**Always write 0**

Bit 3

**OFFSET CORR EN2**

This bit must be set to '1' when the OFFSET CORR EN1 bit is selected.

Bits 2-0

**Always write 0**

#### 8.6.1.21 Register Address D6h (Default = 00h)

| 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|---|---|---|---|
| ALWAYS WRITE 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7

**Always write 1**

This bit is set to 0 by default. User **must** set it to 1 after reset or power-up.

Bits 6-0

**Always write 0**

#### 8.6.1.22 Register Address D7h (Default = 00h)

| 7 | 6 | 5 | 4 | 3              | 2              | 1 | 0 |
|---|---|---|---|----------------|----------------|---|---|
| 0 | 0 | 0 | 0 | ALWAYS WRITE 1 | ALWAYS WRITE 1 | 0 | 0 |

Bits 7-4

**Always write 0**

Bits 3-2

**Always write 1**

This bit is set to 0 by default. User **must** set it to 1 after reset or power-up.

Bits 1-0

**Always write 0**

**8.6.1.23 Register Address F1h (Default = 00h)**

| 7 | 6 | 5                 | 4 | 3 | 2                      | 1 | 0 |
|---|---|-------------------|---|---|------------------------|---|---|
| 0 | 0 | HIGH FREQ<br>MODE | 0 | 0 | ENABLE LVDS SWING PROG |   |   |

**Bits 7-6****Always write 0****Bit 5****HIGH FREQ MODE**

0 = Default (default)

1 = Use for input frequencies &gt; 125 MHz

**Bits 4-3****Always write 0****Bits 2-0****ENABLE LVDS SWING PROG**

This bit enables the LVDS swing control with the LVDS SWING bits.

00 = LVDS swing control disabled (default)

01 = Do not use

10 = Do not use

11 = LVDS swing control enabled

**8.6.1.24 Register Address 58h (Default = 00h)**

| 7 | 6 | 5                     | 4 | 3 | 2 | 1 | 0 |
|---|---|-----------------------|---|---|---|---|---|
| 0 | 0 | HIGH SNR<br>MODE CH A | 0 | 0 | 0 | 0 | 0 |

**Bits 7-6****Always write 0****Bit 5****HIGH SNR MODE CH A**See the [§ 8.4.3](#) section.**Bits 4-0****Always write 0****8.6.1.25 Register Address 59h (Default = 00h)**

| 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|---|---|---|---|---|---|---|
| ALWAYS<br>WRITE 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7****Always write 1**This bit is set to 0 by default. User **must** set it to 1 after reset or power-up.**Bits 6-0****Always write 0**



#### 8.6.1.26 Register Address 70h (Default = 00h)

| 7 | 6 | 5                     | 4 | 3 | 2 | 1 | 0 |
|---|---|-----------------------|---|---|---|---|---|
| 0 | 0 | HIGH SNR<br>MODE CH B | 0 | 0 | 0 | 0 | 0 |

Bits 7-6

Always write 0

Bit 5

HIGH SNR MODE CH B

See the [§ 8.4.3](#) section.

Bits 4-0

Always write 0

#### 8.6.1.27 Register Address 71h (Default = 00h)

| 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|---|---|---|---|---|---|---|
| ALWAYS<br>WRITE 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7

Always write 1

This bit is set to 0 by default. User **must** set it to 1 after reset or power-up.

Bits 6-0

Always write 0

#### 8.6.1.28 Register Address 88h (Default = 00h)

| 7 | 6 | 5                     | 4 | 3 | 2 | 1 | 0 |
|---|---|-----------------------|---|---|---|---|---|
| 0 | 0 | HIGH SNR<br>MODE CH D | 0 | 0 | 0 | 0 | 0 |

Bits 7-6

Always write 0

Bit 5

HIGH SNR MODE CH D

See the [§ 8.4.3](#) section.

Bits 4-0

Always write 0

#### 8.6.1.29 Register Address 89h (Default = 00h)

| 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|---|---|---|---|---|---|---|
| ALWAYS<br>WRITE 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7

Always write 1

This bit is set to 0 by default. User **must** set it to 1 after reset or power-up.

Bits 6-0

Always write 0

**8.6.1.30 Register Address A0h (Default = 00h)**

| 7 | 6 | 5                     | 4 | 3 | 2 | 1 | 0 |
|---|---|-----------------------|---|---|---|---|---|
| 0 | 0 | HIGH SNR<br>MODE CH C | 0 | 0 | 0 | 0 | 0 |

**Bits 7-6****Always write 0****Bit 5****HIGH SNR MODE CH C**

See the § 8.4.3 section.

**Bits 4-0****Always write 0****8.6.1.31 Register Address A1h (Default = 00h)**

| 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|---|---|---|---|---|---|---|
| ALWAYS<br>WRITE 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7****Always write 1**This bit is set to 0 by default. User **must** set it to 1 after reset or power-up.**Bits 6-0****Always write 0****8.6.1.32 Register Address Feh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3        | 2        | 1        | 0        |
|---|---|---|---|----------|----------|----------|----------|
| 0 | 0 | 0 | 0 | PDN CH D | PDN CH C | PDN CH A | PDN CH B |

**Bits 7-4****Always write 0****Bit 3****PDN CH D: Power-down channel D**

Channel D is powered down.

**Bit 2****PDN CH C: Power-down channel C**

Channel C is powered down.

**Bit 1****PDN CH B: Power-down channel B**

Channel B is powered down.

**Bit 0****PDN CH A: Power-down channel A**

Channel A is powered down.

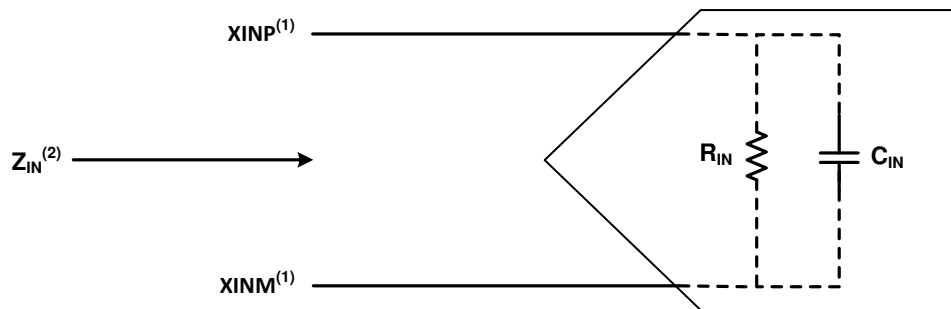
## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

Typical applications involving transformer-coupled circuits are discussed in this section. Transformers (such as ADT1-1WT or WBC1-1) can be used up to 250 MHz to achieve good phase and amplitude balances at ADC inputs. While designing the dc driving circuits, the ADC input impedance must be considered. 图 9-1 shows that ADC input impedance is represented by parallel combination of resistance and capacitance.



- A. X = A, B, C, or D.  
B.  $Z_{IN} = R_{IN} \parallel (1 / j \omega C_{IN})$ .

图 9-1. ADC Equivalent Input Impedance

图 9-2 and 图 9-3 show how input impedance ( $Z_{IN} = R_{IN} \parallel C_{IN}$ ) varies over input frequency.

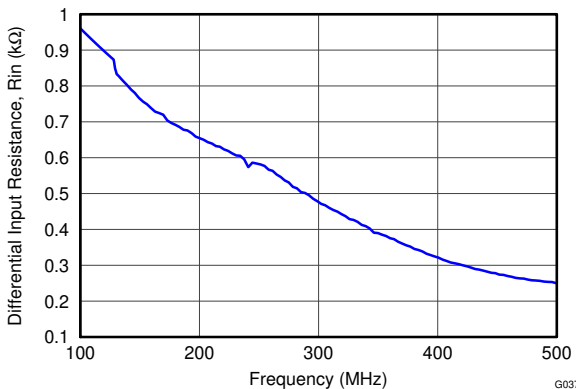


图 9-2. ADC Analog Input Resistance ( $R_{IN}$ ) vs Frequency

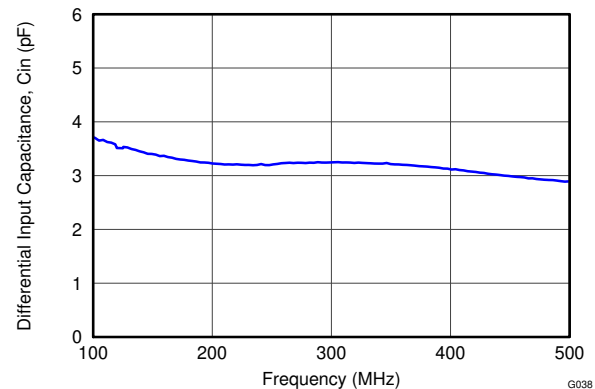


图 9-3. ADC Analog Input Capacitance ( $C_{IN}$ ) vs Frequency

### 9.2 Typical Application

Depending on the input frequency, sampling rate, and input amplitude, one of these metrics plays a dominant part in limiting performance. At very high input frequencies, SFDR is determined largely by the device sampling circuit nonlinearity. At low input amplitudes, the quantizer nonlinearity typically limits performance. Glitches are caused by opening and closing the sampling switches. The driving circuit should present a low source impedance to absorb these glitches, otherwise these glitches may limit performance. A low impedance path between the analog input terminals and VCM is required from the common-mode switching currents perspective

as well. This impedance can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM). The device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the sampling glitches inside the device itself. The R-C component values are also optimized to support high input bandwidth (up to 500 MHz). However, using an external R-LC-R filter as a part of drive circuit can improve glitch filtering, thus further resulting in better performance. In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched source impedance. In doing so, the ADC input impedance (shown in 图 9-2 and 图 9-3) must be considered.

### 9.2.1 Design Requirements

For optimum performance, the analog inputs must be driven differentially. An optional 5-Ω to 15-Ω resistor in-series with each input pin can be kept to damp out ringing caused by package parasitic. The drive circuit may have to be designed to minimize the impact of kick-back noise generated by sampling switches opening and closing inside the ADC, as well as ensuring low insertion loss over the desired frequency range and matched impedance to the source.

### 9.2.2 Detailed Design Procedure

Two example driving circuits with a 50-Ω source impedance are shown in 图 9-4 and 图 9-5. The driving circuit in 图 9-4 is optimized for input frequencies in the second Nyquist zone (centered at 185 MHz), whereas the circuit in 图 9-5 is optimized for input frequencies in third Nyquist zone (centered at 310 MHz).

Note that both drive circuits are terminated by 50 Ω near the ADC side. This termination is accomplished with a 25-Ω resistor from each input to the 1.15-V common-mode (VCM) from the device. This architecture allows the analog inputs to be biased around the required common-mode voltage.

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals.

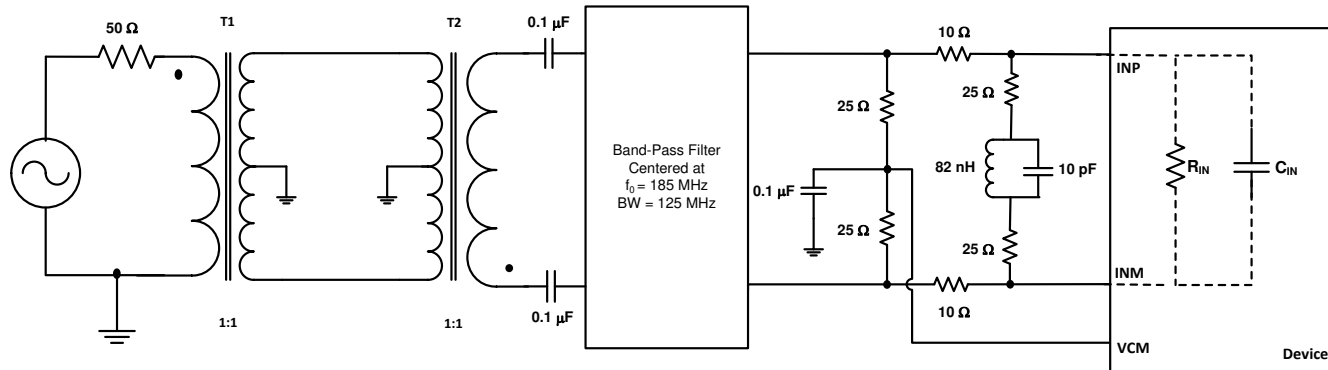


图 9-4. Driving Circuit for a 50-Ω Source Impedance and Input Frequencies in the Second Nyquist Zone

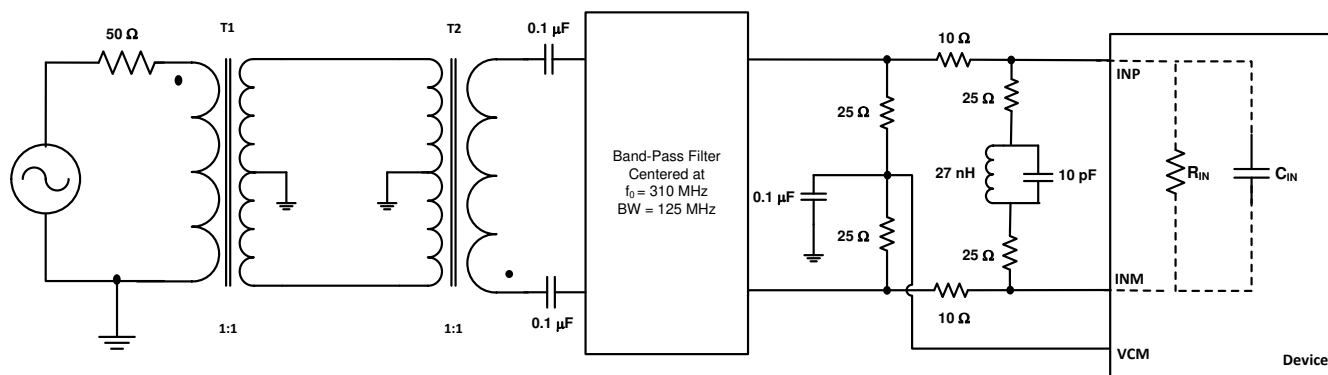


图 9-5. Driving Circuit for a 50-Ω Source Impedance and Input Frequencies in the Third Nyquist Zone

TI recommends terminating the drive circuit by a 50- $\Omega$  (or lower) impedance near the ADC for best performance. However, in some applications higher impedances be required to terminate the drive circuit. Two example driving circuits with 100- $\Omega$  differential termination are shown in 图 9-6 and 图 9-7. In these example circuits, the 1:2 transformer (T1) is used to transform the 50- $\Omega$  source impedance into a differential 100  $\Omega$  at the input of the band-pass filter. In 图 9-6, the parallel combination of two 68- $\Omega$  resistors and one 120-nH inductor and two 100- $\Omega$  resistors is used (100  $\Omega$  is the effective impedance in pass-band) for better performance.

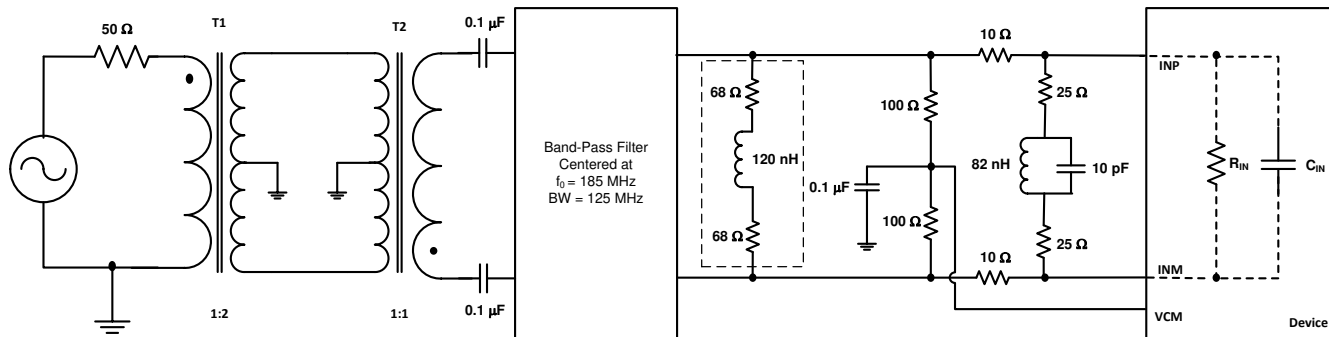


图 9-6. Driving Circuit for a 100- $\Omega$  Source Impedance and Input Frequencies in the Second Nyquist Zone

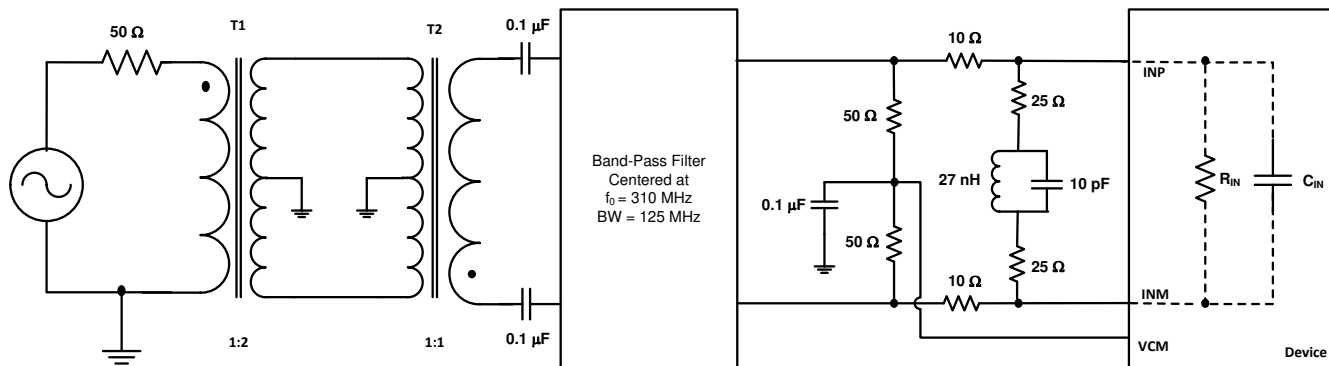


图 9-7. Driving Circuit for a 100- $\Omega$  Source Impedance and Input Frequencies in the Third Nyquist Zone

### 9.2.3 Application Curves

Figure 10 and Figure 11 below show performance obtained at 170-MHz and 230-MHz input frequencies respectively using appropriate driving circuit.

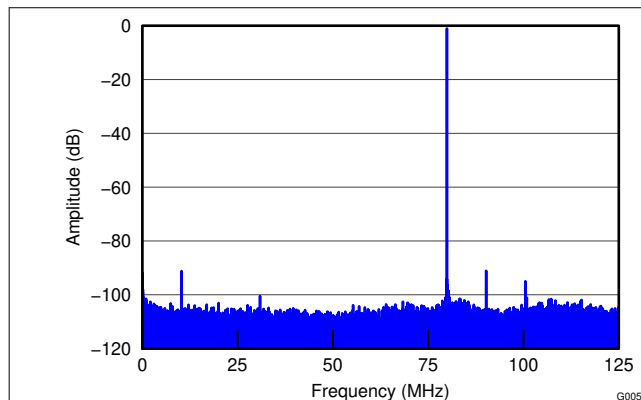


图 9-8. FFT For 170-MHz Input Signal

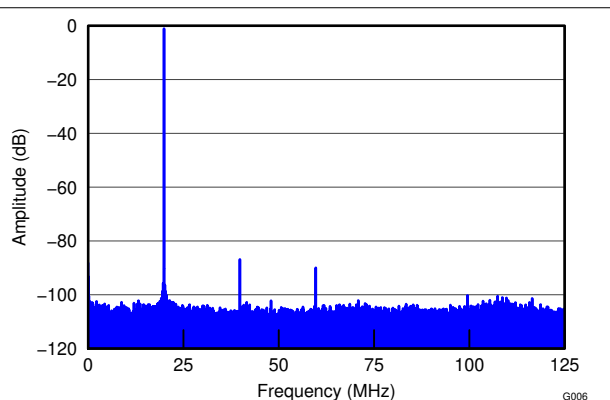


图 9-9. FFT For 230MHz Input Signal

### 9.2.4 Enabling 14-Bit Resolution

By default after reset, the device outputs 11-bit data on the Dxx13P, Dxx13M and Dxx3P, Dxx3M terminals and OVR information on the Dxx0P, Dxx0M terminals. When the ALWAYS WRITE 1 bits are set, the ADC outputs 13-bit data on the Dxx13P, Dxx13M and Dxx1P, Dxx1M terminals and OVR information on the Dxx0P, Dxx0M terminals. To enable 14-bit resolution, the DIS OVR ON LSB register bit must be set to 1 as indicated in 表 9-1.

**表 9-1. ADC Configuration**

| ADC TERMINAL NAMES | DATA ON ADC TERMINALS                                      |                                                            |                                           |
|--------------------|------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------|
|                    | AFTER RESET                                                | ALWAYS WRITE 1 = 1                                         | ALWAYS WRITE 1 = 1<br>DIS OVR ON LSB = 1  |
| Dxx13              | D13                                                        | D13                                                        | D13                                       |
| —                  | —                                                          | —                                                          | —                                         |
| Dxx3               | D3                                                         | D3                                                         | D3                                        |
| Dxx2               | Logic 0                                                    | D2                                                         | D2                                        |
| Dxx1               | Logic 1                                                    | D1                                                         | D1                                        |
| Dxx0               | OVR                                                        | OVR                                                        | D0                                        |
| Comments           | 11-bit data (D[13:3]) and OVR come on ADC output terminals | 13-bit data (D[13:1]) and OVR come on ADC output terminals | 14-bit data comes on ADC output terminals |

### 9.2.5 Analog Input

The analog input consists of a switched-capacitor-based differential sample-and-hold architecture. This differential topology results in very good ac performance even for high input frequencies at high sampling rates.

The INP and INM terminals must be externally biased around a common-mode voltage of 1.15 V, available on the VCM terminal. For a full-scale differential input, each input terminal (INP, INM) must swing symmetrically between  $V_{CM} + 0.5\text{ V}$  and  $V_{CM} - 0.5\text{ V}$ , resulting in a  $2\text{-}V_{PP}$  differential input swing.

The input sampling circuit has a high 3-dB bandwidth that extends up to 500 MHz when a  $50\text{-}\Omega$  source drives the ADC analog inputs.

### 9.2.6 Drive Circuit Requirements

This configuration improves the common-mode noise immunity and even-order harmonic rejection. A  $5\text{-}\Omega$  to  $15\text{-}\Omega$  resistor in series with each input terminal is recommended to damp out ringing caused by package parasitics.

Glitches are caused by opening and closing the sampling switches. The driving circuit should present a low source impedance to absorb these glitches, otherwise these glitches may limit performance. A low impedance path between the analog input terminals and VCM is required from the common-mode switching currents perspective as well. This impedance can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

The device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the sampling glitches inside the device itself. The R-C component values are also optimized to support high input bandwidth (up to 500 MHz). However, using an external R-LC-R filter (refer to 图 9-4, 图 9-5, 图 9-6, 图 9-7, and 图 9-10) improves glitch filtering, thus further resulting in better performance.

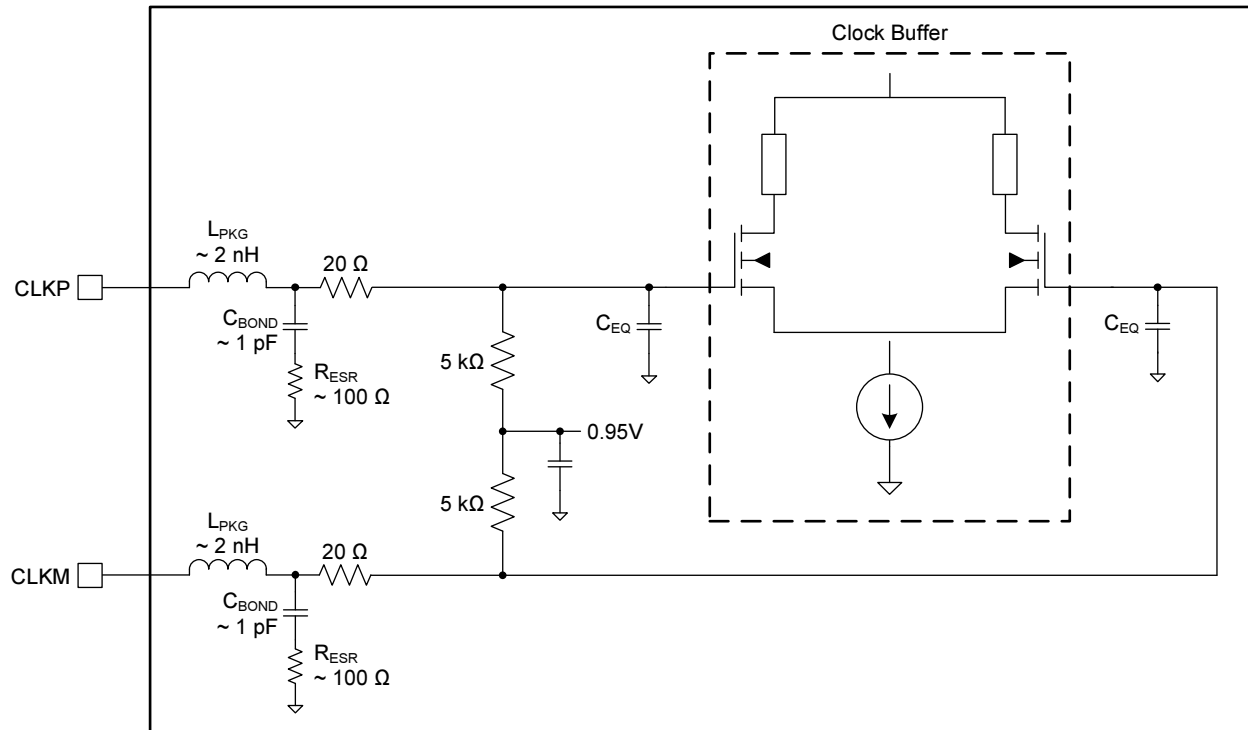
In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched source impedance. In doing so, the ADC input impedance must be considered. 图 9-1, 图 9-2, and 图 9-3 show the impedance ( $Z_{IN} = R_{IN} \parallel C_{IN}$ ) at the ADC input terminals.

Spurious-free dynamic range (SFDR) performance can be limited because of several reasons (such as the effect of sampling glitches, sampling circuit nonlinearity, and quantizer nonlinearity that follows the sampling circuit). Depending on the input frequency, sampling rate, and input amplitude, one of these metrics plays a dominant part in limiting performance. At very high input frequencies, SFDR is determined largely by the device sampling circuit nonlinearity. At low input amplitudes, the quantizer nonlinearity typically limits performance.

### 9.2.7 Clock Input

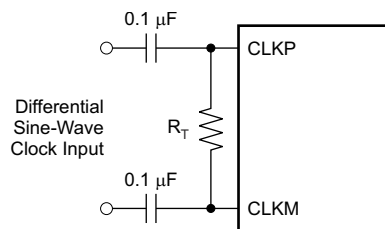
The device clock inputs can be driven differentially with a sine, LVPECL, or LVDS source with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 0.95 V using internal 5-k $\Omega$  resistors, as shown in 图 9-10. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL, LVDS, and LVCMOS clock sources (see 图 9-11, 图 9-12, and 图 9-13).

For best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. TI recommends keeping the differential voltage between clock inputs less than 1.8 V<sub>PP</sub> to obtain best performance. A clock source with very low jitter is recommended for high input frequency sampling. Band-pass filtering of the clock source can help reduce the effects of jitter. With a non-50% duty cycle clock input, performance does not change.



NOTE:  $C_{EQ}$  is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

图 9-10. Internal Clock Buffer



A.  $R_T$  is the termination resistor (optional).

图 9-11. Differential Sine-Wave Clock Driving Circuit

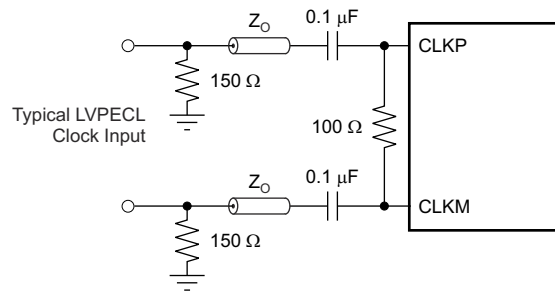


图 9-12. LVPECL Clock Driving Circuit

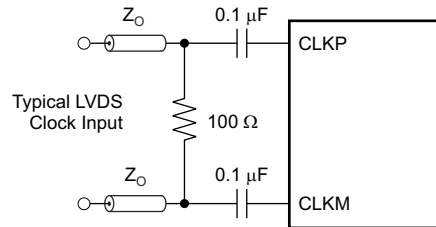


图 9-13. LVDS Clock Driving Circuit

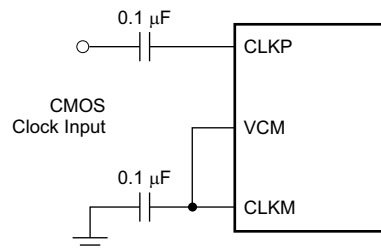


图 9-14. Typical LVCMOS Clock Driving Circuit

## 10 Power Supply Recommendations

The device requires a 1.8-V nominal supply for AVDD and DVDD. There are no specific sequence power-supply requirements during device power-up. AVDD and DVDD can power up in any order.



## 11 Layout

### 11.1 Layout Guidelines

The ADS4449 EVM layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in 图 11-1. Some important points to remember during laying out the board are:

- Analog inputs are located on opposite sides of the device pin out to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs should exit the pin out in opposite directions, as shown in the reference layout of Figure 66 as much as possible.
- In the device pin out, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of Figure 66 as much as possible.
- Digital outputs should be kept away from the analog inputs. When these digital outputs exit the pin out, the digital output traces should not be kept parallel to the analog input traces because this configuration may result in coupling from digital outputs to analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] should be matched in length to avoid skew among outputs.
- At each power-supply pin (AVDD and DVDD), a 0.1- $\mu$ F decoupling capacitor should be kept close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10- $\mu$ F, 1- $\mu$ F, and 0.1- $\mu$ F capacitors can be kept close to the supply source.

### 11.2 Layout Example

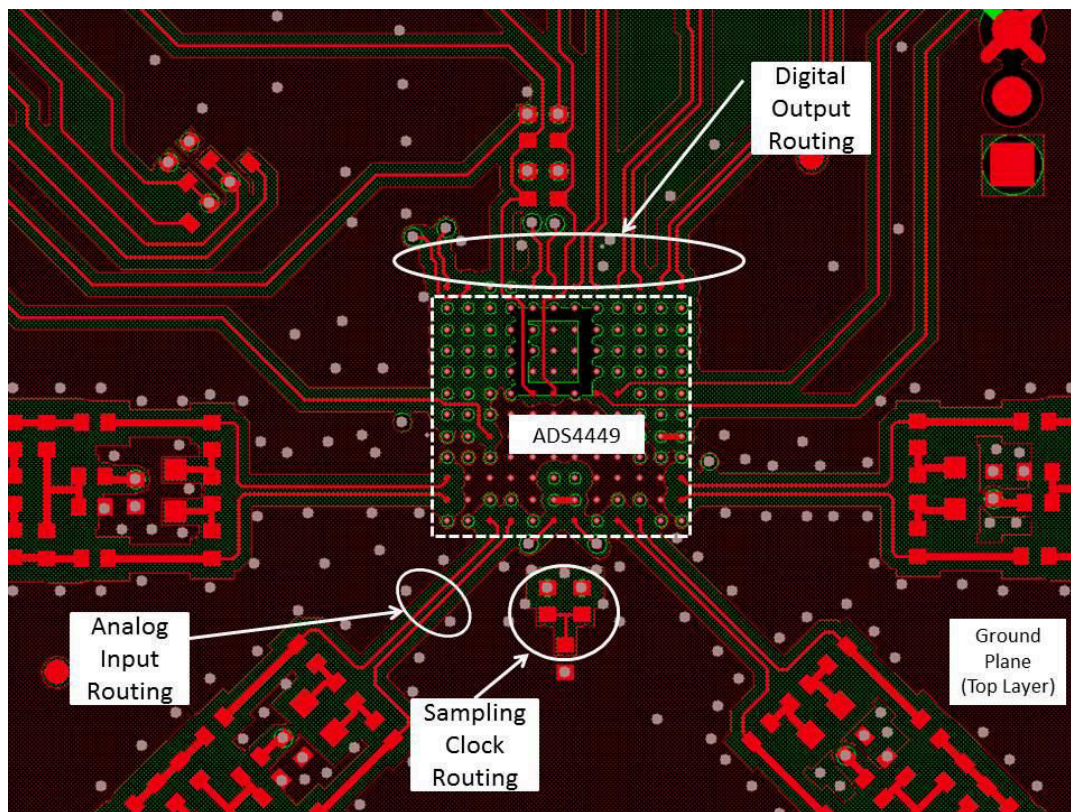


图 11-1. ADS4449 Layout

## 12 Device and Documentation Support

### 12.1 Device Nomenclature

|                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Analog Bandwidth</b>                 | The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Aperture Delay</b>                   | The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as an aperture delay variation (channel-to-channel).                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <b>Aperture Uncertainty (Jitter)</b>    | The sample-to-sample variation in aperture delay.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <b>Clock Pulse Width and Duty Cycle</b> | The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <b>Maximum Conversion Rate</b>          | The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate, unless otherwise noted.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <b>Minimum Conversion Rate</b>          | The minimum sampling rate at which the ADC functions.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <b>Differential Nonlinearity (DNL)</b>  | An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSBs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <b>Integral Nonlinearity (INL)</b>      | INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function, measured in units of LSBs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| <b>Gain Error</b>                       | <p>Gain error is the deviation of the ADC actual input full-scale range from the ideal value. Gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as <math>E_{GREF}</math> and <math>E_{GCHAN}</math>.</p> <p>To a first-order approximation, the total gain error of <math>E_{TOTAL}</math> is approximately <math>E_{GREF} + E_{GCHAN}</math>.</p> <p>For example, if <math>E_{TOTAL} = \pm 0.5\%</math>, the full-scale input varies from <math>(1 - 0.5 / 100) \times f_{S\ ideal}</math> to <math>(1 + 0.5 / 100) \times f_{S\ ideal}</math>.</p> |
| <b>Offset Error</b>                     | Offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>Temperature Drift</b>                | The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from $T_{MIN}$ to $T_{MAX}$ . The coefficient is calculated by dividing the maximum deviation of the parameter across the $T_{MIN}$ to $T_{MAX}$ range by the difference of $T_{MAX} - T_{MIN}$ .                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>Signal-to-Noise Ratio (SNR)</b>      | SNR is the ratio of the power of the fundamental ( $P_S$ ) to the noise floor power ( $P_N$ ), excluding the power at dc and the first nine harmonics.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

$$SNR = 10 \log_{10} \frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

### Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental ( $P_S$ ) to the power of all other spectral components, including noise ( $P_N$ ) and distortion ( $P_D$ ) but excluding dc.

$$\text{SINAD} = 10\text{Log}^{10} \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

## 12.2 Documentation Support

### 12.2.1 Related Documentation

For related documentation see the following:

- *ADS4449 User Guide*, [SLAU485](#)
- *Design Considerations for Avoiding Timing Errors during High-Speed ADC, LVDS Data Interface with FPGA*, [SLAA592](#)
- *Why Oversample when Undersampling can do the Job?*, [SLAA594](#)

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.5 Trademarks

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### 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| ADS4449IZCR      | ACTIVE        | NFBGA        | ZCR                | 144  | 184            | RoHS & Green    | SNAGCU                               | Level-3-260C-168 HR  | -40 to 85    | ADS4449I                | <a href="#">Samples</a> |
| ADS4449IZCRR     | ACTIVE        | NFBGA        | ZCR                | 144  | 1000           | RoHS & Green    | SNAGCU                               | Level-3-260C-168 HR  | -40 to 85    | ADS4449I                | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

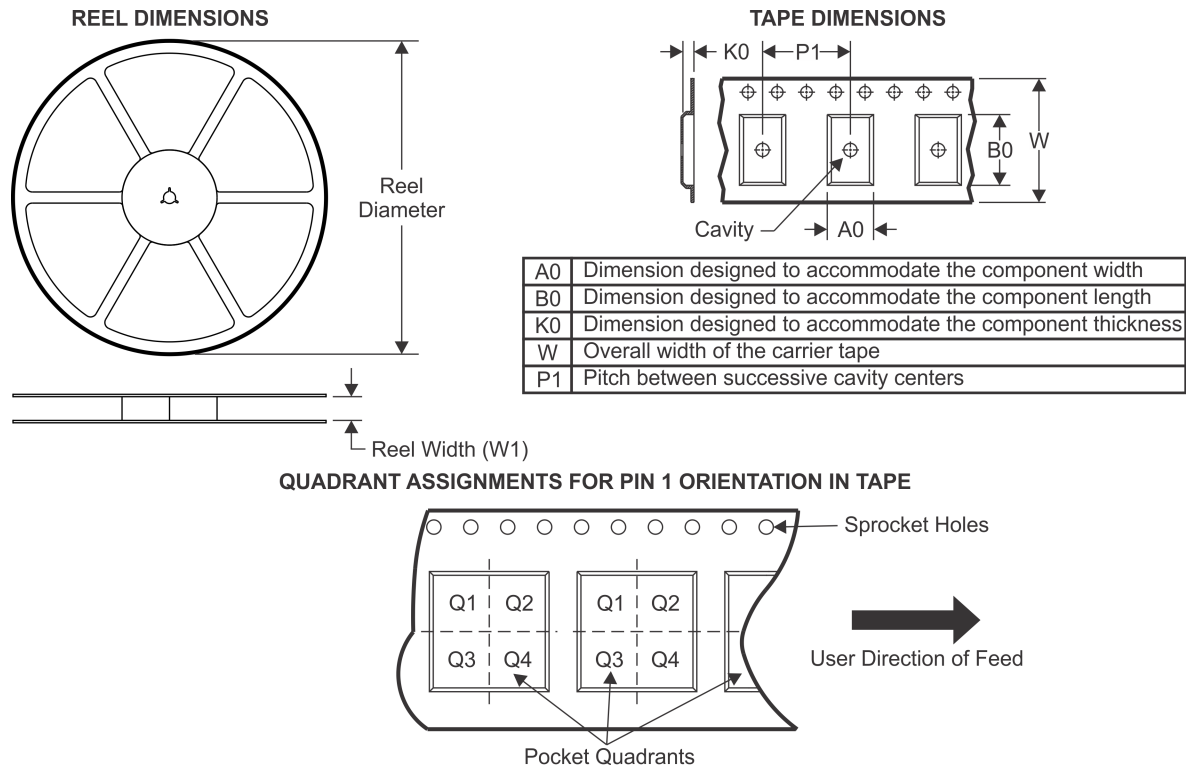
<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

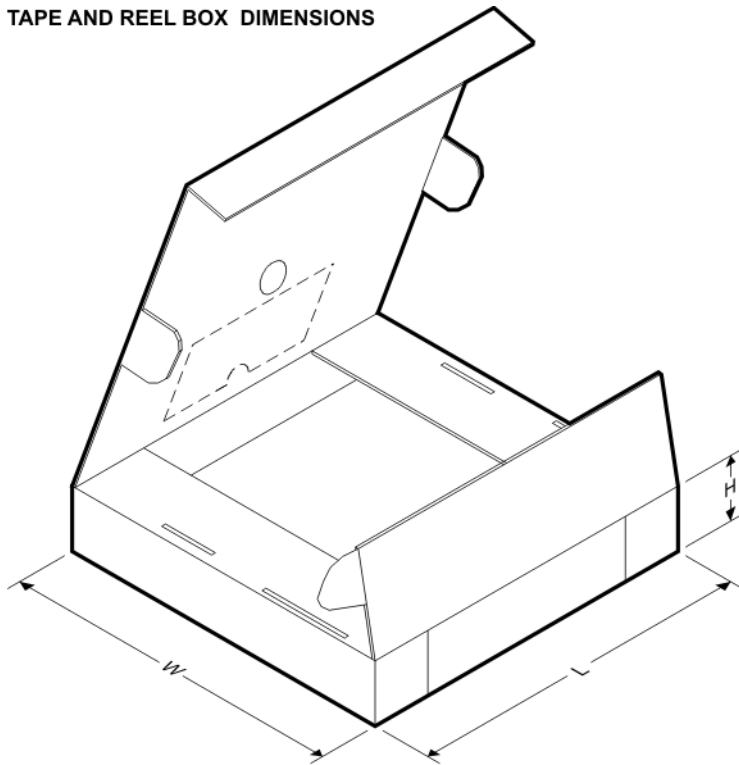


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS4449IZCRR | NFBGA        | ZCR             | 144  | 1000 | 330.0              | 24.4               | 10.25   | 10.25   | 2.25    | 16.0    | 24.0   | Q1            |



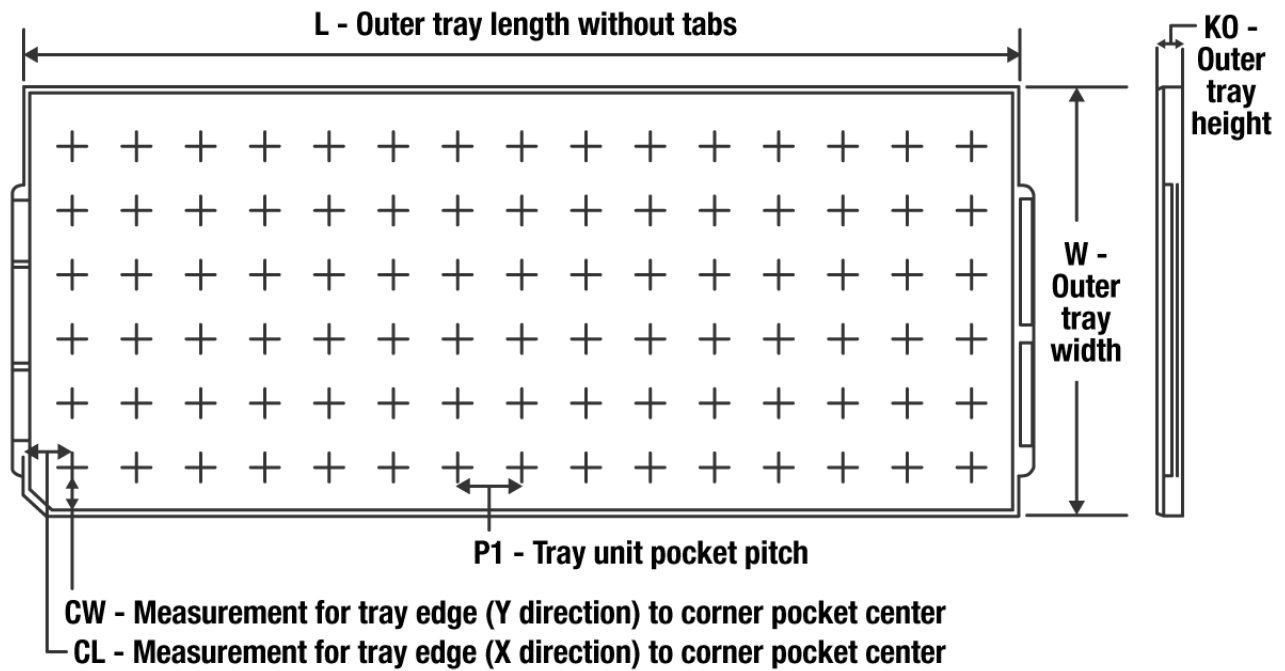
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS4449IZCRR | NFBGA        | ZCR             | 144  | 1000 | 350.0       | 350.0      | 43.0        |

## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|-------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| ADS4449IZCR | ZCR          | NFBGA        | 144  | 184 | 8 x 23            | 150                  | 315    | 135.9  | 7620    | 13.4    | 10.1    | 19.65   |

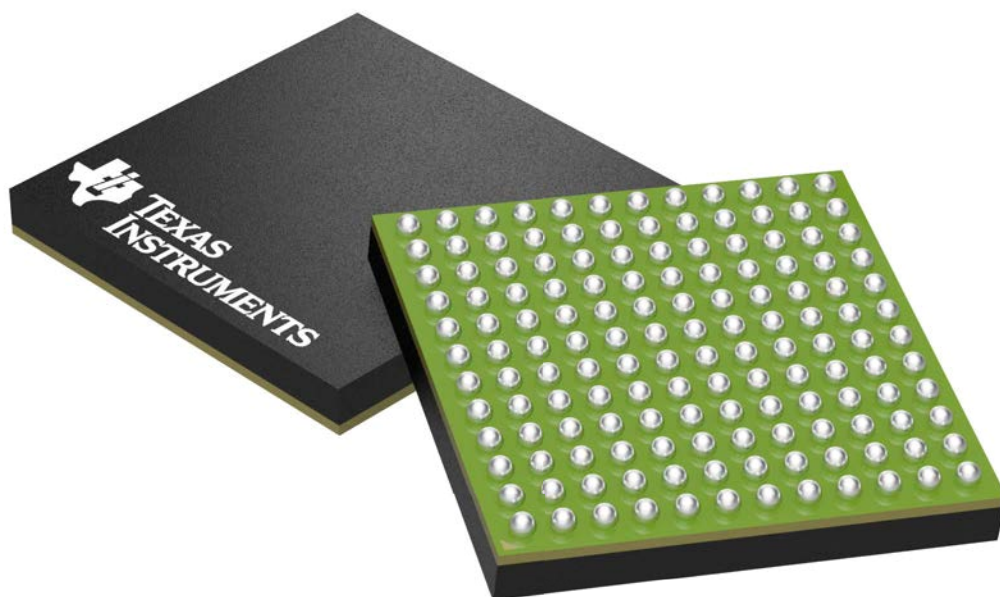


**ZCR 144**

**NFBGA - 1.5 mm max height**

10 x 10 mm, 0.8 mm pitch

PLASTIC BALL GRID ARRAY



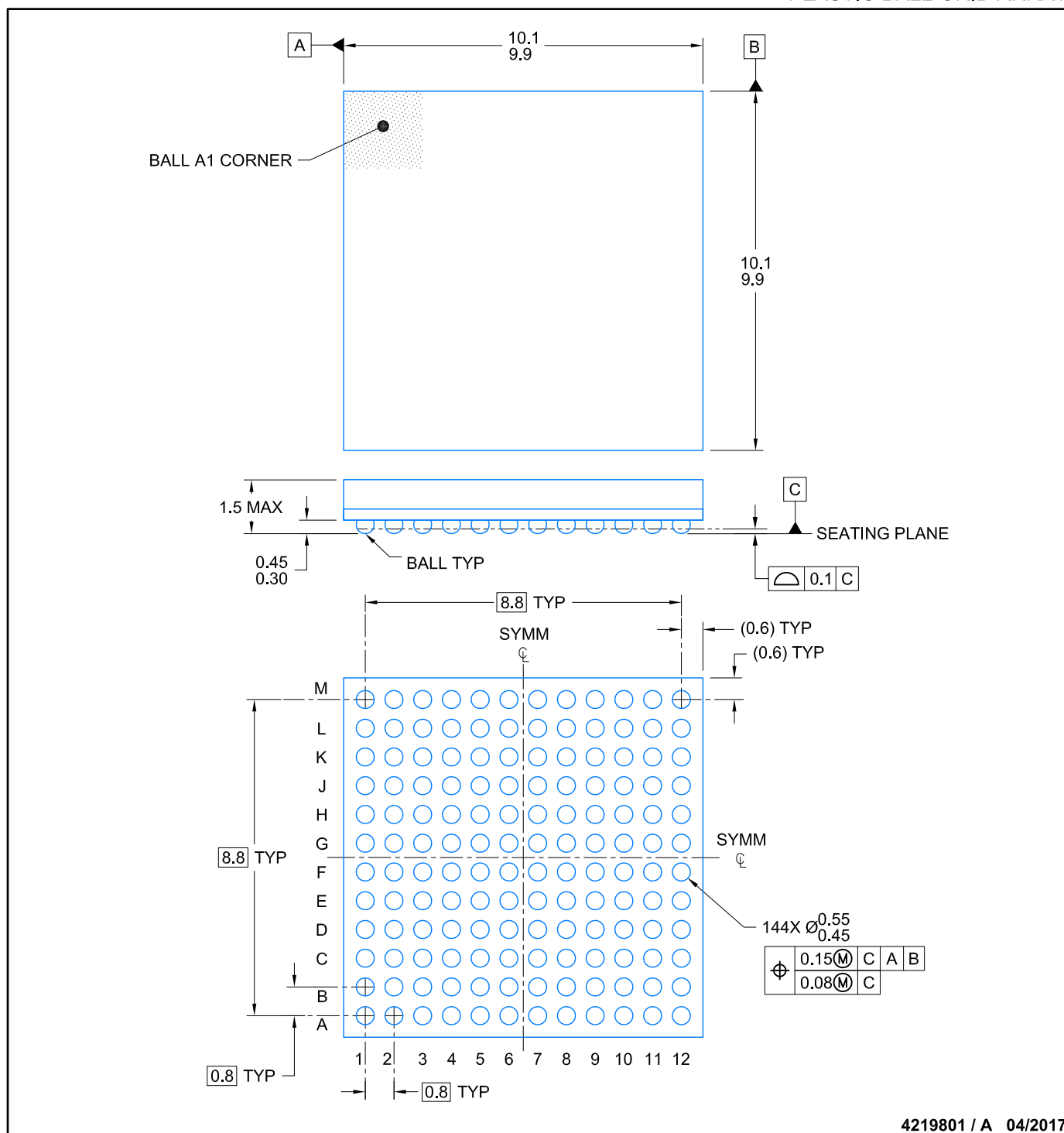
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

## PACKAGE OUTLINE

### NFBGA - 1.5 mm max height

## NFBGA - 1.5 mm max height

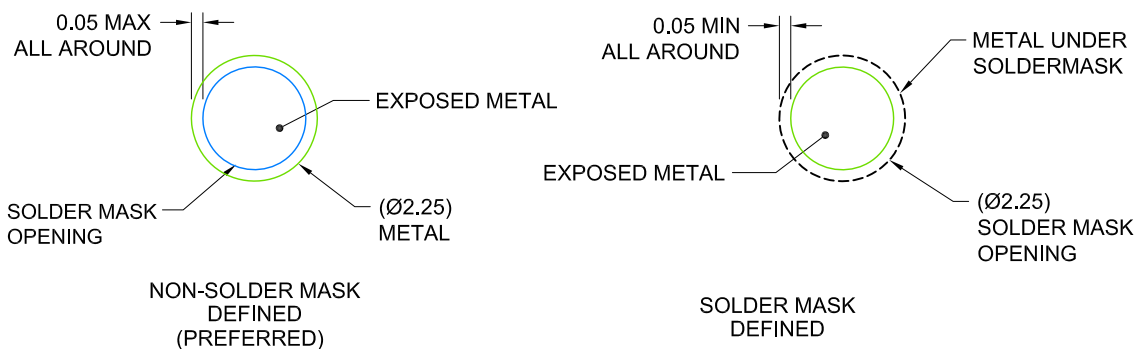
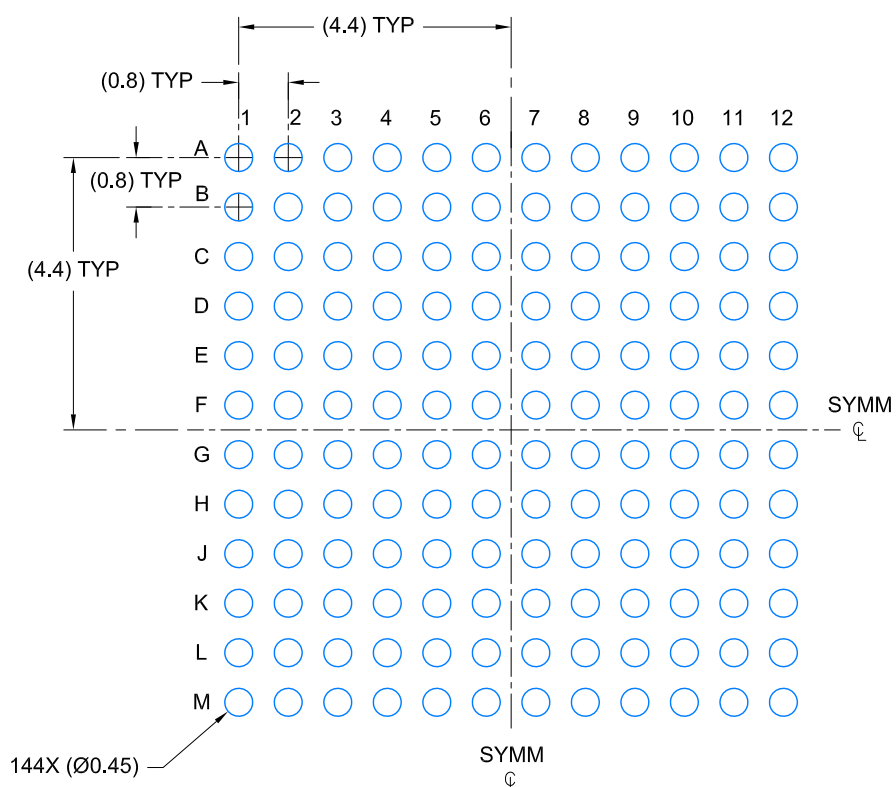
## PLASTIC BALL GRID ARRAY



4219801 / A 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



4219801 / A 04/2017

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

## NFBGA - 1.5 mm max height

Technical drawing of a square with rounded corners. The square has a side length of 0.45, indicated by a dimension line on the left. The corners are rounded with a radius of R0.05, indicated by a dimension line at the bottom right. The drawing is labeled "METAL" and "(R0.05) TYP".

4219801 / A 04/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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