
QUAD CHANNEL, 12-BIT, 125-MSPS ADC WITH SERIAL LVDS INTERFACE

FEATURES

- **Maximum Sample Rate: 125 MSPS**
- **12-Bit Resolution with No Missing Codes**
- **1.65-W Total Power**
- **Simultaneous Sample and Hold**
- **70.3 dBFS SNR at $F_{in} = 50$ MHz**
- **83 dBc SFDR at $F_{in} = 50$ MHz, 0 dB Gain**
- **79 dBc SFDR at $F_{in} = 170$ MHz, 3.5 dB Gain**
- **3.5 dB Coarse Gain and up to 6 dB Programmable Fine Gain for SFDR/SNR Trade-Off**
- **Serialized LVDS Outputs with Programmable Internal Termination Option**
- **Supports Sine, LVCMOS, LVPECL, LVDS Clock Inputs and Amplitude Down to 400 mV_{pp} Differential**
- **Internal Reference with External Reference Support**
- **No External Decoupling Required for References**
- **3.3-V Analog and Digital Supply**
- **64 QFN Package (9 mm × 9 mm)**
- **Pin Compatible 14-Bit Family (ADS644X - [SLAS532](#))**

APPLICATIONS

- **Base-Station IF Receivers**
- **Diversity Receivers**
- **Medical Imaging**
- **Test Equipment**

DESCRIPTION

The ADS6425 is a high performance 12-bit, 125-MSPS quad channel ADC. Serial LVDS data outputs reduce the number of interface lines, resulting in a compact 64-pin QFN package (9 mm × 9 mm) that allows for high system integration density. The device includes a 3.5 dB coarse gain option that can be used to improve SFDR performance with little degradation in SNR. In addition to the coarse gain, fine gain options also exist, programmable in 1dB steps up to 6dB.

The output interface is 2-wire, where each ADC's data is serialized and output over two LVDS pairs. This makes it possible to halve the serial data rate (compared to a 1-wire interface) and restrict it to less than 1Gbps easing receiver design. The ADS6425 also includes the traditional 1-wire interface that can be used at lower sampling frequencies.

An internal phase locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock. The bit clock is used to serialize the 12-bit data from each channel. In addition to the serial data streams, the frame and bit clocks are also transmitted as LVDS outputs. The LVDS output buffers have features such as programmable LVDS currents, current doubling modes, and internal termination options. These can be used to widen eye-openings and improve signal integrity, easing capture by the receiver.

The ADC channel outputs can be transmitted either as MSB or LSB first and 2s complement or straight binary.

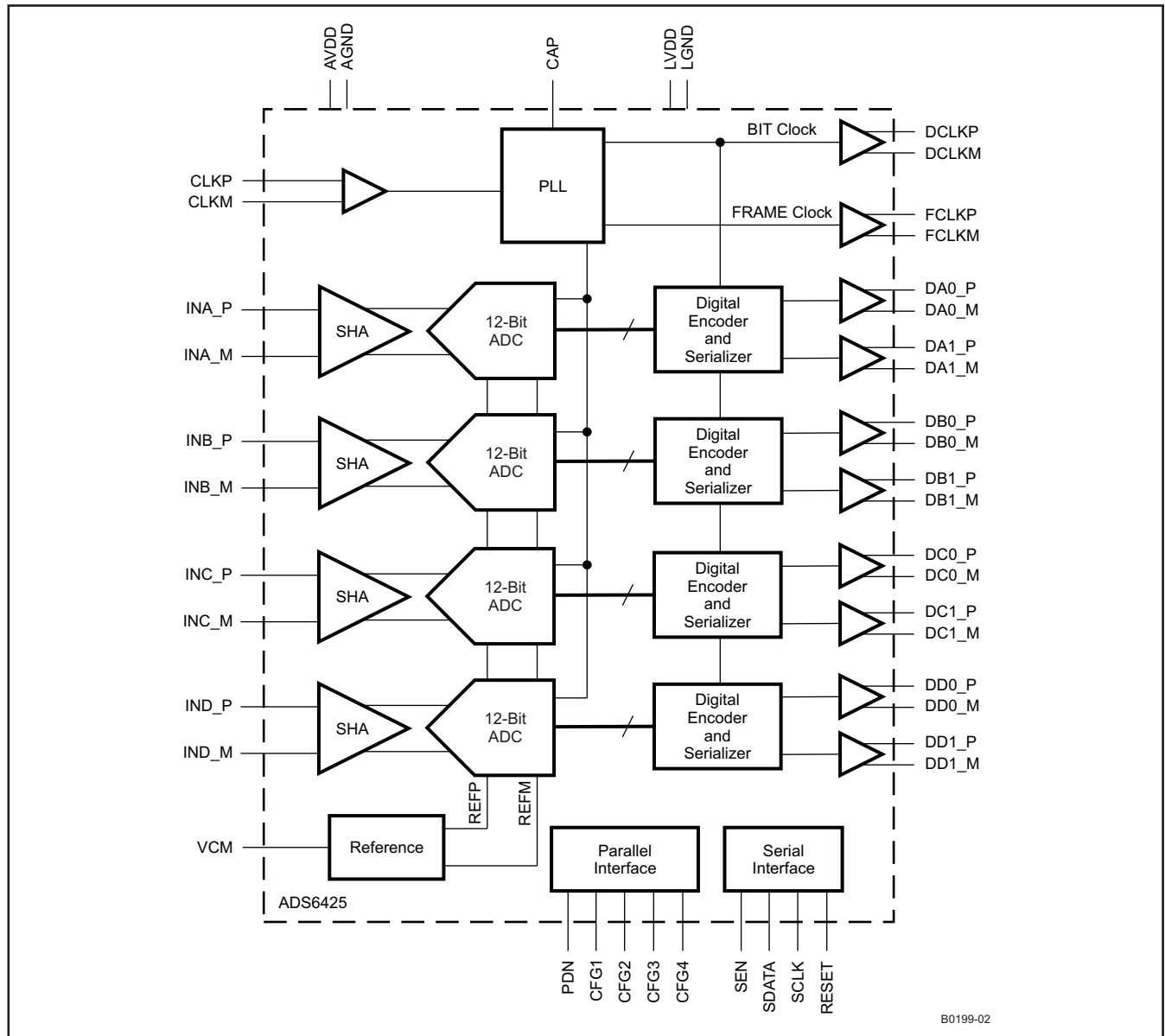
The ADS6425 has internal references, but can also support an external reference mode. The device is specified over the industrial temperature range (–40°C to 85°C).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



PACKAGE/ORDERING INFORMATION⁽¹⁾

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---------|-----------------------|--------------------|-----------------------------|-----------------|-----------------|---------------------------|
| ADS6425 | QFN-64 ⁽²⁾ | RGC | -40°C to 85°C | AZ6425 | ADS6425IRGCT | 250, Tape/reel |
| | | | | | ADS6425IRGCR | 2000, Tape/reel |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) For thermal pad size on the package, see the mechanical drawings at the end of this data sheet. $\theta_{JA} = 23.17\text{ }^{\circ}\text{C/W}$ (0 LFM air flow), $\theta_{JC} = 22.1\text{ }^{\circ}\text{C/W}$ when used with 2 oz. copper trace and pad soldered directly to a JEDEC standard four layer 3 in. x 3 in. PCB.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | | VALUE | UNIT |
|------------------|--|--------------------------------------|------|
| AVDD | Supply voltage range | –0.3 to 3.9 | V |
| LVDD | Supply voltage range | –0.3 to 3.9 | V |
| | Voltage between AGND and DGND | –0.3 to 0.3 | V |
| | Voltage between AVDD to LVDD | –0.3 to 3.3 | V |
| | Voltage applied to external pin, VCM | –0.3 to 2.0 | V |
| | Voltage applied to analog input pins | –0.3V to minimum (3.6, AVDD + 0.3V) | V |
| T _A | Operating free-air temperature range | –40 to 85 | °C |
| T _J | Operating junction temperature range | 125 | °C |
| T _{stg} | Storage temperature range | –65 to 150 | °C |
| | Lead temperature 1,6 mm (1/16") from the case for 10 seconds | 220 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|------------------------|---|------------------------------|-------------|------|-----------------|
| SUPPLIES | | | | | |
| AVDD | Analog supply voltage | 3.0 | 3.3 | 3.6 | V |
| LVDD | LVDS Buffer supply voltage | 3.0 | 3.3 | 3.6 | V |
| ANALOG INPUTS | | | | | |
| | Differential input voltage range | | 2 | | V _{pp} |
| | Input common-mode voltage | | 1.5 ±0.1 | | V |
| | Voltage applied on VCM in external reference mode | 1.45 | 1.50 | 1.55 | V |
| CLOCK INPUT | | | | | |
| | Input clock sample rate | 5 | | 125 | MSPS |
| | Input clock amplitude differential (V _{CLKP} – V _{CLKM}) | Sine wave, ac-coupled | 0.4 | 1.5 | V _{pp} |
| | | LVPECL, ac-coupled | ± 0.8 | | |
| | | LVDS, ac-coupled | ± 0.35 | | |
| | | LVC MOS, ac-coupled | 3.3 | | |
| | Input Clock duty cycle | 35% | 50% | 65% | |
| DIGITAL OUTPUTS | | | | | |
| C _{LOAD} | Maximum external load capacitance from each output pin to DGND | Without internal termination | 5 | | pF |
| | | With internal termination | 10 | | |
| R _{LOAD} | Differential load resistance (external) between the LVDS output pairs | 100 | | | Ω |
| T _A | Operating free-air temperature | –40 | | 85 | °C |

ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, min and max values are across the full temperature range $T_{MIN} = -40^{\circ}C$ to $T_{MAX} = 85^{\circ}C$, $AVDD = LVDD = 3.3V$, sampling rate = 125MSPS, 50% clock duty cycle, -1dBFS differential analog input, internal reference mode (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|--|--|------|---------|-----|----------------------|
| RESOLUTION | | | | 12 | | Bits |
| ANALOG INPUT | | | | | | |
| | Differential input voltage range | | | 2.0 | | V_{pp} |
| | Differential input capacitance | | | 7 | | pF |
| | Analog input bandwidth | | | 500 | | MHz |
| | Analog input common mode current (per input pin of each ADC) | | | 155 | | μA |
| REFERENCE VOLTAGES | | | | | | |
| VREFB | Internal reference bottom voltage | | | 1.0 | | V |
| VREFT | Internal reference top voltage | | | 2.0 | | V |
| VCM | Common mode output voltage | | | 1.5 | | V |
| | VCM Output current capability | | | ± 4 | | mA |
| DC ACCURACY | | | | | | |
| | No missing codes | | | Assured | | |
| E_O | Offset error | | -15 | ± 2 | +15 | mV |
| | Offset error temperature coefficient | | | 0.05 | | mV/ $^{\circ}C$ |
| | Offset error temperature coefficient, channel-channel | | | | | |
| | Internal reference error (VREFT-VREFB) | | -15 | ± 5 | 15 | mV |
| | Internal reference error temperature coefficient | | | 0.25 | | mV/ $^{\circ}C$ |
| E_G | Gain error ⁽¹⁾ | Does not include gain error caused due to internal reference error | -1 | 0.3 | +1 | % FS |
| | Gain error temperature coefficient | | | 0.005 | | $\Delta\%/^{\circ}C$ |
| | Gain error temperature coefficient, channel-channel | | | | | |
| DNL | Differential nonlinearity | | -0.9 | 0.5 | 2.0 | LSB |
| INL | Integral nonlinearity | | -2.5 | 1.0 | 2.5 | LSB |
| PSRR | DC Power supply rejection ratio | | | -0.5 | | mV/V |
| POWER SUPPLY | | | | | | |
| I_{CC} | Total supply current | | | 502 | | mA |
| I_{AVDD} | Analog supply current | | | 412 | | mA |
| I_{LVDD} | LVDS supply current | | | 90 | | mA |
| | Total power | | | 1.65 | 1.8 | W |
| | Power down | Input clock running | | 77 | 150 | mW |

(1) This is specified by design and characterization. It is not tested in production.

ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, min and max values are across the full temperature range $T_{MIN} = -40^{\circ}\text{C}$ to $T_{MAX} = 85^{\circ}\text{C}$, $AVDD = LVDD = 3.3\text{V}$, sampling rate = 125MSPS, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------------------------|--------------------------------------|----------------------------|--------------------|------|-------|-----|------|
| DYNAMIC AC CHARACTERISTICS | | | | | | | |
| SNR | Signal to noise ratio | Fin = 10 MHz | | | 70.9 | | dBFS |
| | | Fin = 50 MHz | | 67.5 | 70.5 | | |
| | | Fin = 100 MHz | | | 69.9 | | |
| | | Fin = 170 MHz | 0 dB Gain | | 68.5 | | |
| | | | 3.5 dB Coarse gain | | 68.1 | | |
| | | Fin = 230 MHz | 0 dB Gain | | 67.4 | | |
| 3.5 dB Coarse gain | | | 67.1 | | | | |
| SINAD | Signal to noise and distortion ratio | Fin = 10 MHz | | | 70.7 | | dBFS |
| | | Fin = 50 MHz | | 67 | 70 | | |
| | | Fin = 100 MHz | | | 69.7 | | |
| | | Fin = 170 MHz | 0 dB Gain | | 66.9 | | |
| | | | 3.5 dB Coarse gain | | 67.4 | | |
| | | Fin = 230 MHz | 0 dB Gain | | 66 | | |
| 3.5 dB Coarse gain | | | 66.5 | | | | |
| RMS Output noise | | Inputs tied to common-mode | | | 0.407 | | LSB |
| SFDR | Spurious free dynamic range | Fin = 10 MHz | | | 90 | | dBc |
| | | Fin = 50 MHz | | 73 | 83 | | |
| | | Fin = 100 MHz | | | 87 | | |
| | | Fin = 170 MHz | 0 dB Gain | | 75 | | |
| | | | 3.5 dB Coarse gain | | 79 | | |
| | | Fin = 230 MHz | 0 dB Gain | | 74 | | |
| 3.5 dB Coarse gain | | | 78 | | | | |
| HD2 | Second harmonic | Fin = 10 MHz | | | 93 | | dBc |
| | | Fin = 50 MHz | | 73 | 91 | | |
| | | Fin = 100 MHz | | | 90 | | |
| | | Fin = 170 MHz | 0 dB Gain | | 85 | | |
| | | | 3.5 dB Coarse gain | | 88 | | |
| | | Fin = 230 MHz | 0 dB Gain | | 82 | | |
| 3.5 dB Coarse gain | | | 85 | | | | |
| HD3 | Third harmonic | Fin = 10 MHz | | | 90 | | dBc |
| | | Fin = 50 MHz | | 73 | 83 | | |
| | | Fin = 100 MHz | | | 87 | | |
| | | Fin = 170 MHz | 0 dB Gain | | 75 | | |
| | | | 3.5 dB Coarse gain | | 79 | | |
| | | Fin = 230 MHz | 0 dB Gain | | 74 | | |
| 3.5 dB Coarse gain | | | 78 | | | | |
| | Worst harmonic (other than HD2, HD3) | Fin = 10 MHz | | | 95 | | dBc |
| | | Fin = 50 MHz | | | 94 | | |
| | | Fin = 100 MHz | | | 91 | | |
| | | Fin = 170 MHz | | | 88 | | |
| | | Fin = 230 MHz | | | 86 | | |

ELECTRICAL CHARACTERISTICS (continued)

Typical values are at 25°C, min and max values are across the full temperature range $T_{MIN} = -40^{\circ}C$ to $T_{MAX} = 85^{\circ}C$, $AVDD = LVDD = 3.3V$, sampling rate = 125MSPS, 50% clock duty cycle, -1dBFS differential analog input, internal reference mode (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|-------------------------------------|--|------|------|-----|------|
| THD | Total harmonic distortion | Fin = 10 MHz | | 88 | | dBc |
| | | Fin = 50 MHz | 70 | 81 | | |
| | | Fin = 100 MHz | | 84 | | |
| | | Fin = 170 MHz | | 73 | | |
| | | Fin = 230 MHz | | 72 | | |
| ENOB | Effective number of bits | Fin = 50 MHz | 10.8 | 11.4 | | Bits |
| IMD | Two-tone intermodulation distortion | F1= 46.09 MHz, F2 = 50.09 MHz | | 90 | | dBFS |
| | | F1= 185.09 MHz, F2 = 190.09 MHz | | 82 | | |
| Cross-talk | Cross-talk | Near channel, Frequency of interfering signal = 10 MHz | | 92 | | dBFS |
| | | Far channel, Frequency of interfering signal = 10 MHz | | 105 | | |

DIGITAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1 $AVDD = LVDD = 3.3V$, $I_O = 3.5mA$, $R_{LOAD} = 100\Omega^{(1)}$.

All LVDS specifications are characterized, but not tested at production.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|-----------------------------|--|------|------|---------|
| DIGITAL INPUTS | | | | | |
| High-level input voltage | | 2.4 | | | V |
| Low-level input voltage | | | | 0.8 | V |
| High-level input current | | | 10 | | μA |
| Low-level input current | | | 10 | | μA |
| Input capacitance | | | 4 | | pF |
| DIGITAL OUTPUTS | | | | | |
| High-level output voltage | | | 1375 | | mV |
| Low-level output voltage | | | 1025 | | mV |
| V _{OD} | Output differential voltage | 250 | 350 | 450 | mV |
| V _{OS} | Output offset voltage | Common-mode voltage of OUTP and OUTM | | 1200 | mV |
| | Output capacitance | Output capacitance inside the device, from either output to ground | | 2 | pF |

(1) I_O refers to the LVDS buffer current setting, R_{LOAD} is the external differential load resistance between the LVDS output pair

TIMING SPECIFICATIONS⁽¹⁾

Typical values are at 25°C, min and max values are across the full temperature range $T_{MIN} = -40^{\circ}\text{C}$ to $T_{MAX} = 85^{\circ}\text{C}$, $AVDD = LVDD = 3.3\text{ V}$, sampling frequency = 125 MSPS, sine wave input clock, 1.5 V_{PP} clock amplitude, $C_L = 5\text{ pF}$ ⁽²⁾, $I_O = 3.5\text{ mA}$, $R_L = 100\ \Omega$ ⁽³⁾, no internal termination, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|------|-----|-----|---------------|
| t_J Aperture jitter | Uncertainty in the sampling instant | | 250 | | fs rms |
| Interface: 2-wire, DDR bit clock, 12x serialization⁽⁴⁾ | | | | | |
| t_{su} Data setup time ^{(5) (6)} | Measured from zero crossing of data transitions to zero crossing of bit clock | 0.4 | 0.6 | | ns |
| t_h Data hold time ^{(5) (6)} | Measured from zero crossing of bit clock to zero crossing of data transitions | 0.5 | 0.7 | | ns |
| t_{su} Frame setup time | Measured from zero-cross of frame clock rising edge to zero-cross of bit clock rising edge | 0.4 | 0.6 | | ns |
| t_h Frame hold time | Measured from zero-cross of bit clock falling edge to zero-cross of frame clock falling edge | 0.5 | 0.7 | | ns |
| t_{pd_clk} Clock propagation delay ⁽⁴⁾ | Input clock rising edge cross-over to frame clock rising edge cross-over | 3.6 | 4.4 | 5.2 | ns |
| | Bit clock cycle-cycle jitter ⁽⁶⁾ | | 350 | | ps pp |
| | Frame clock cycle-cycle jitter ⁽⁶⁾ | | 75 | | ps pp |
| Below specifications apply for $5\text{ MSPS} \leq F_s \leq 125\text{ MSPS}$ and all interface options. | | | | | |
| t_A Aperture delay | Delay from rising edge of input clock to the actual sampling instant | 1 | 2 | 3 | ns |
| | Aperture delay variation, channel-channel | -250 | | 250 | ps |
| | ADC Latency ⁽⁷⁾ | | 12 | | Clock cycles |
| Wake up time | Time to valid data after coming out of global power down | | | 100 | μs |
| | Time to valid data after input clock is re-started | | | 100 | μs |
| | Time to valid data after coming out of channel standby | | | 200 | clock cycles |
| t_{RISE} Data rise time | Data rise time measured from -100 mV to $+100\text{ mV}$ | 50 | 100 | 200 | ps |
| t_{FALL} Data fall time | Data fall time measured from $+100\text{ mV}$ to -100 mV | 50 | 100 | 200 | ps |
| t_{RISE} Bit clock and frame clock rise time | Rise time measured from -100mV to $+100\text{mV}$ | 50 | 100 | 200 | ps |
| t_{FALL} Bit clock and frame clock fall time | Fall time measured from $+100\text{mV}$ to -100mV | 50 | 100 | 200 | ps |
| | LVDS Bit clock duty cycle | 45% | 50% | 55% | |
| | LVDS Frame clock duty cycle | 47% | 50% | 53% | |

- (1) Timing parameters are ensured by design and characterization and not tested in production.
- (2) C_L is the external single-ended load capacitance between each output pin and ground.
- (3) I_O refers to the LVDS buffer current setting; R_L is the external differential load resistance between the LVDS output pair.
- (4) Refer to [Output Timings](#) in application section for timings at lower sampling frequencies and other interface options.
- (5) Timing parameters are measured at the end of a 2 inch pcb trace (100- Ω characteristic impedance) terminated by R_L and C_L .
- (6) Setup and hold time specifications take into account the effect of jitter on the output data and clock.
- (7) Note that the total latency = ADC latency + internal serializer latency. The serializer latency depends on the interface option selected as shown in [Table 25](#)

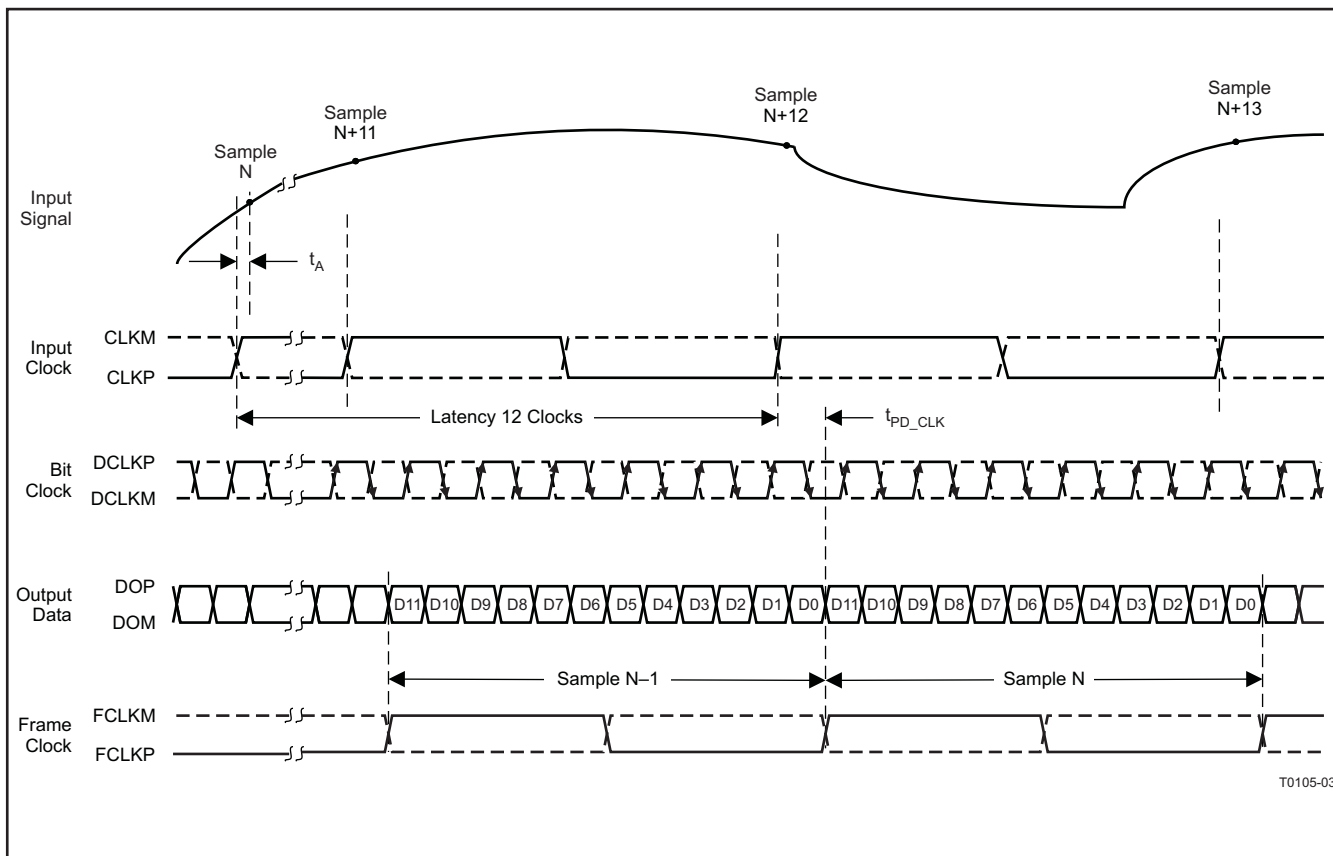


Figure 1. Latency

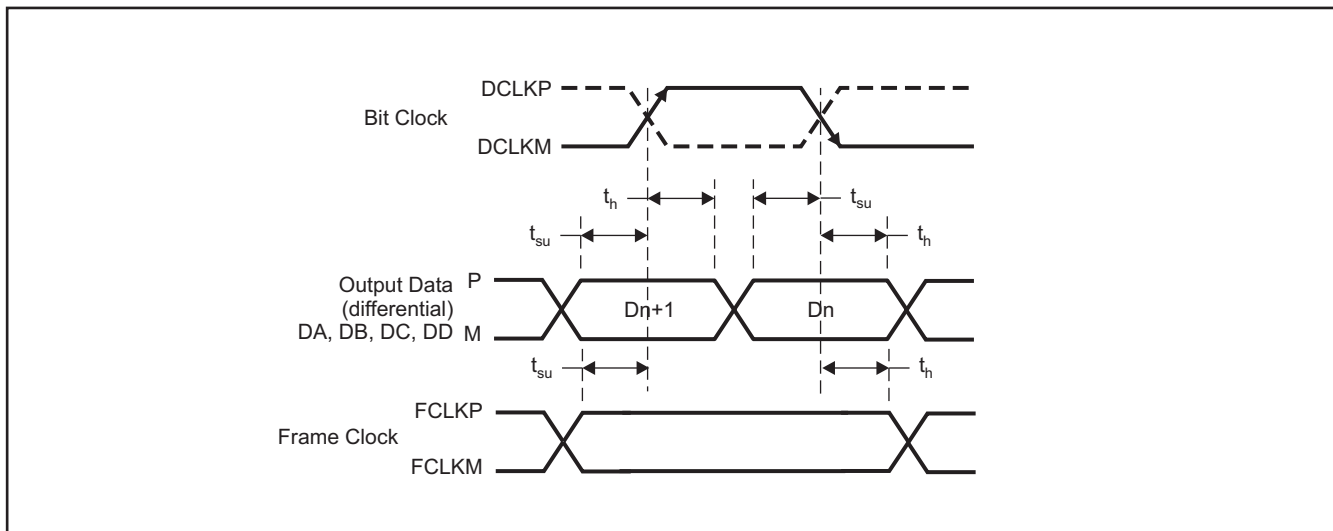


Figure 2. LVDS Timings

DEVICE PROGRAMMING MODES

The ADS6425 offers flexibility with several programmable features that are easily configured.

The device can be configured independently using either parallel interface control or serial interface programming.

In addition, the device supports a third configuration mode, where both the parallel interface and the serial control registers are used. In this mode, the priority between the parallel and serial interfaces is determined by a priority table ([Table 2](#)). If this additional level of flexibility is not required, the user can select either the serial interface programming or the parallel interface control.

USING PARALLEL INTERFACE CONTROL ONLY

To control the device using parallel interface, keep RESET tied to **high** (LVDD). Pins CFG1, CFG2, CFG3, CFG4, PDN, SEN, SCLK, and SDATA are used to directly control certain functions of the ADC. After power-up, the device will automatically get configured as per the parallel pin voltage settings ([Table 3](#) to [Table 6](#)) and no reset is required. In this mode, SEN, SCLK, and SDATA function as parallel interface control pins.

Frequently used functions are controlled in this mode—output data interface and format, power down modes, coarse gain and internal/external reference. The parallel pins can be configured using a simple resistor string (with 10% tolerance resistors) as illustrated in [Figure 3](#).

[Table 1](#) briefly describes the modes controlled by the parallel pins.

Table 1. Parallel Pin Definition

| PIN | CONTROL FUNCTIONS |
|-------------|--|
| SEN | Coarse gain and internal/external reference. |
| SCLK, SDATA | Sync, deskew patterns and global power down. |
| PDN | Dedicated pin for global power down |
| CFG1 | 1-Wire/2-wire and DDR/SDR bit clock |
| CFG2 | 12x/14x Serialization and SDR bit clock capture edge |
| CFG3 | Reserved function. Tie CFG3 to Ground. |
| CFG4 | MSB/LSB First and data format. |

USING SERIAL INTERFACE PROGRAMMING ONLY

In this mode, SEN, SDATA, and SCLK function as serial interface pins and are used to access the internal registers of ADC. The registers must first be reset to their default values either by applying a pulse on RESET pin or by a **high** setting on the <RST> bit (in register). After reset, the RESET pin must be kept **low**.

The [Serial Interface](#) section describes the register programming and register reset in more detail.

Since the parallel pins (CFG1-4 and PDN) are not used in this mode, they must be tied to ground. The register override bit <OVRD> - D10 in register 0x0D has to be set **high** to disable the control of parallel interface pins in this serial interface control ONLY mode.

USING BOTH THE SERIAL INTERFACE AND PARALLEL CONTROLS

For increased flexibility, a combination of serial interface registers and parallel pin controls (CFG1-4 and PDN) can also be used to configure the device.

The parallel interface control pins CFG1 to CFG4 and PDN are available. After power-up, the device will automatically get configured as per the parallel pin voltage settings ([Table 3](#) to [Table 9](#)) and no reset is required. A simple resistor string can be used as illustrated in [Figure 3](#).

SEN, SDATA, and SCLK function as serial interface pins and are used to access the internal registers of ADC. The registers must first be reset to their default values either by applying a pulse on RESET pin or by a **high** setting on the <RST> bit (in register). After reset, the RESET pin must be kept **low**.

The [Serial Interface](#) section describes the register programming and register reset in more detail.

Since some functions are controlled using both the parallel pins and serial registers, the priority between the two is determined by a priority table ([Table 2](#)).

Table 2. Priority Between Parallel Pins and Serial Registers

| PIN | FUNCTIONS SUPPORTED | PRIORITY |
|--------------|--|--|
| CFG1 to CFG4 | As described in Table 6 to Table 9 | Register bits can control the modes ONLY if the <OVRD> bit is high . If the <OVRD> bit is LOW, then the control voltage on these parallel pins determines the function as per Tables |
| PDN | Global Power Down | D0 bit in register 0x00 controls global power down ONLY if PDN pin is LOW. If PDN is high , device is in global power down mode. |
| SEN | Serial Interface Enable | 3.5 dB coarse gain setting is controlled by bit D5 in register 0x0D ONLY if the <OVRD> bit is high . Else, it is in default setting of 0 dB coarse gain. Internal/External reference setting is determined by bit D5 in register 0x00. |
| SCLK, SDATA | Serial Interface Clock and Serial Interface Data | Bits D5-D7 in register 0x0A control the SYNC and DESKEW output patterns. Power down is determined by bit D0 in 0x00 register. |

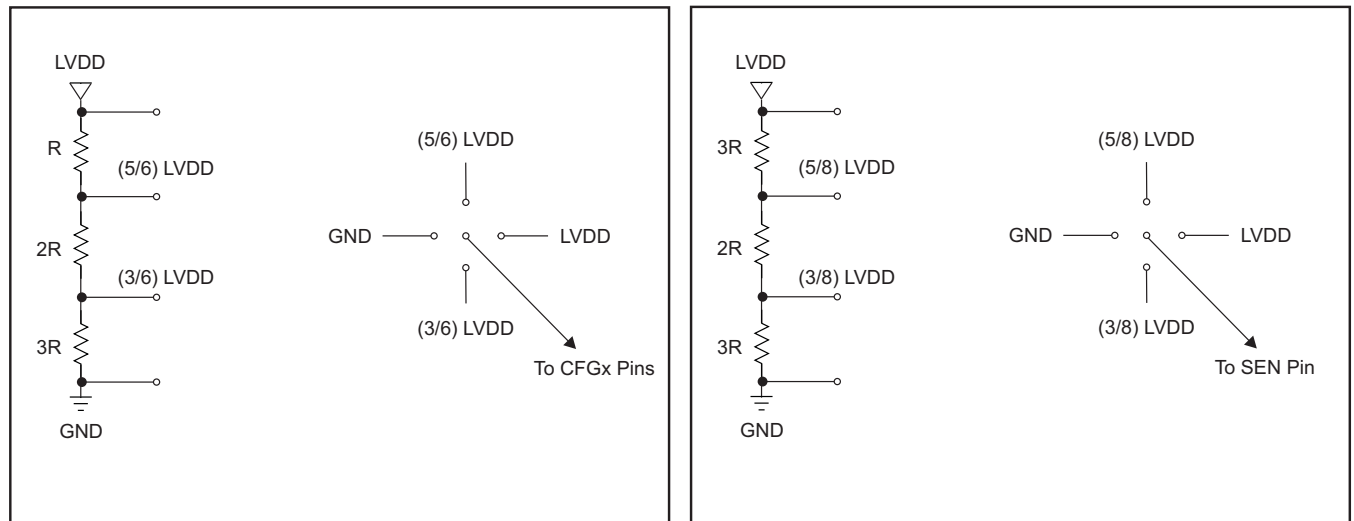


Figure 3. Simple Scheme to Configure Parallel Pins

DESCRIPTION OF PARALLEL PINS
Table 3. SCLK, SDATA Control Pins

| SCLK | SDATA | DESCRIPTION |
|------|-------|--|
| LOW | LOW | NORMAL conversion. |
| LOW | HIGH | SYNC - ADC outputs sync pattern on all channels. This pattern can be used by the receiver to align the deserialized data to the frame boundary. See Capture Test Patterns for details. |
| HIGH | LOW | POWER DOWN –Global power down, all channels of the ADC are powered down, including internal references, PLL and output buffers. |
| HIGH | HIGH | DESKEW - ADC outputs deskew pattern on all channels. This pattern can be used by the receiver to ensure deserializer uses the right clock edge. See Capture Test Patterns for details. |

Table 4. SEN Control Pin

| SEN | DESCRIPTION |
|-----------|---|
| 0 | External reference and 0 dB coarse gain (full-scale = 2V pp) |
| (3/8)LVDD | External reference and 3.5 dB coarse gain (full-scale = 1.34V pp) |
| (5/8)LVDD | Internal reference and 3.5 dB coarse gain (full-scale = 1.34V pp) |
| LVDD | Internal reference and 0 dB coarse gain (full-scale = 2V pp) |

Independent of the programming mode used, after power-up the parallel pins PDN, CFG1 to CFG4 will automatically configure the device as per the voltage applied ([Table 5](#) to [Table 9](#)).

Table 5. PDN Control Pin

| PDN | DESCRIPTION |
|------|-------------------|
| 0 | Normal operation |
| AVDD | Power down global |

Table 6. CFG1 Control Pin

| CFG1 | DESCRIPTION |
|-----------------------|------------------------------------|
| 0 (default) +200mV | DDR Bit clock and 1-wire interface |
| (3/6)LVDD ±200mV | Not used |
| (5/6)LVDD ±200mV | SDR Bit clock and 2-wire interface |
| LVDD - 200mV | DDR Bit clock and 2-wire interface |

Table 7. CFG2 Control Pin

| CFG2 | DESCRIPTION |
|-----------------------|--|
| 0 (default) +200mV | 12x Serialization and capture at falling edge of bit clock (only with SDR bit clock) |
| (3/6)LVDD ±200mV | 14x Serialization and capture at falling edge of bit clock (only with SDR bit clock) |
| (5/6)LVDD ±200mV | 14x Serialization and capture at rising edge of bit clock (only with SDR bit clock) |
| LVDD - 200mV | 12x Serialization and capture at rising edge of bit clock (only with SDR bit clock) |

Table 8. CFG3 Control Pin

| CFG3 | RESERVED - TIE TO GROUND |
|------|--------------------------|
| | |

Table 9. CFG4 Control Pin

| CFG4 | DESCRIPTION |
|-----------------------|-----------------------------|
| 0 (default) +200mV | MSB First and 2s complement |
| (3/6)LVDD ±200mV | MSB First and Offset binary |
| (5/6)LVDD ±200mV | LSB First and Offset binary |
| LVDD - 200mV | LSB First and 2s complement |

SERIAL INTERFACE

The ADC has a serial interface formed by pins SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data) and RESET. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiple of 16-bit words within a single active SEN pulse. The interface can work with SCLK frequency from 20 MHz down to very low speeds (few hertz) and even with non-50% duty cycle SCLK.

The first 5-bits of the 16-bit word are the address of the register while the next 11 bits are the register data.

Register Reset

After power-up, the internal registers **must** be reset to their default values. This can be done in one of two ways:

1. Either by applying a high-going pulse on RESET (of width greater than 10ns) **OR**
2. By applying software reset. Using the serial interface, set the <RST> bit in register 0x00 to **high** – this resets the registers to their default values and then self-resets the <RST> bit to LOW.

When RESET pin is not used, it must be tied to LOW.

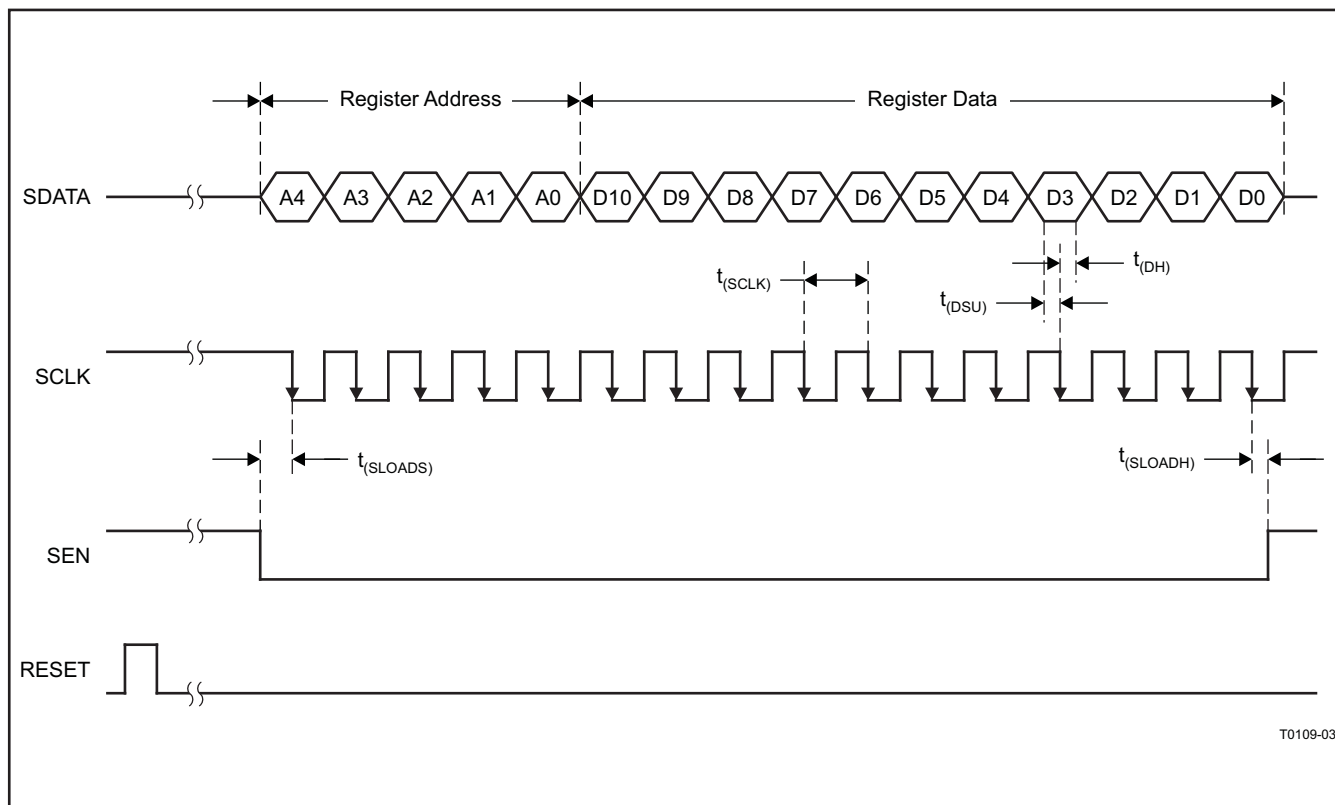


Figure 4. Serial Interface Timing

T0109-03

SERIAL INTERFACE TIMING CHARACTERISTICS

Typical values at 25°C, min and max values across the full temperature range $T_{MIN} = -40^{\circ}C$ to $T_{MAX} = 85^{\circ}C$, $AVDD = LVDD = 3.3V$, unless otherwise noted.

| PARAMETER | | MIN | TYP | MAX | UNIT |
|--------------|---|------|-----|-----|------|
| f_{SCLK} | SCLK Frequency, $f_{SCLK} = 1/t_{SCLK}$ | > dc | | 20 | MHz |
| t_{SLOADS} | SEN to SCLK Setup time | | 25 | | ns |
| t_{SLOADH} | SCLK to SEN Hold time | | 25 | | ns |
| t_{DSU} | SDATA Setup time | | 25 | | ns |
| t_{DH} | SDATA Hold time | | 25 | | ns |
| | Time taken for register write to take effect after 16th SCLK falling edge | | 100 | | ns |

RESET TIMING

Typical values at 25°C, min and max values across the full temperature range $T_{MIN} = -40^{\circ}C$ to $T_{MAX} = 85^{\circ}C$, $AVDD = LVDD = 3.3V$, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|-----|-----|-----|------|
| t_1 | Power-on delay time Delay from power-up of AVDD and LVDD to RESET pulse active | 5 | | | ms |
| t_2 | Reset pulse width Pulse width of active RESET signal | 10 | | | ns |
| t_3 | Register write delay time Delay from RESET disable to SEN active | 25 | | | ns |
| t_{PO} | Power-up delay time Delay from power-up of AVDD and LVDD to output stable | | 6.5 | | ms |

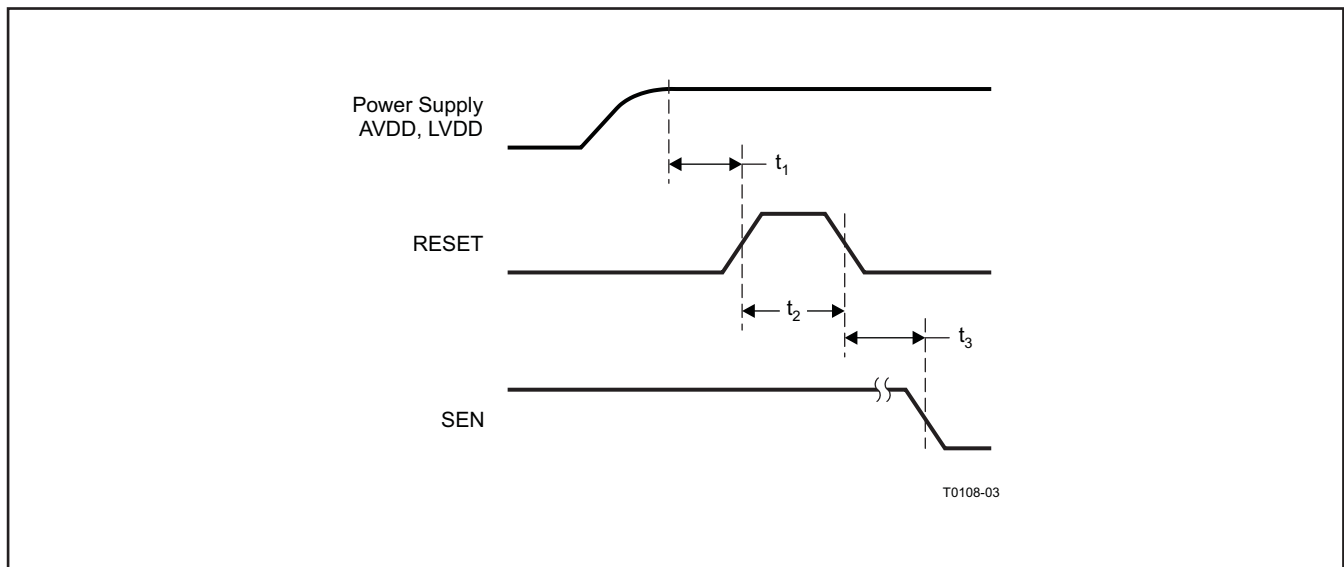


Figure 5. Reset Timing

SERIAL REGISTER MAP
Table 10. Summary of Functions Supported By Serial Interface

| REGISTER ADDRESS | REGISTER FUNCTIONS ⁽¹⁾⁽²⁾⁽³⁾ | | | | | | | | | | | |
|------------------|---|--|----|-----------------------------|---|---|--|---------------------------------|----------------------------------|--------------------------------------|----------------------------------|---|
| | A4 - A0 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00 | <RST> S/W RESET | 0 | 0 | 0 | 0 | 0 | <REF> INTERNAL OR EXTERNAL | <PDN CHD> POWER DOWN CH D | <PDN CHC> POWER DOWN CHC | <PDN CHB> POWER DOWN CH B | <PDN CHA> POWER DOWN CH A | <PDN GLOBAL> GLOBAL POWER DOWN |
| 04 | 0 | 0 | 0 | 0 | <CLKIN GAIN> INPUT CLOCK BUFFER GAIN CONTROL | | | | | | 0 | 0 |
| 0A | 0 | <DF> DATA FORMAT 2S COMP OR STRAIGHT BINARY | 0 | <PATTERNS> TEST PATTERNS | | | | 0 | 0 | 0 | 0 | 0 |
| 0B | <CUSTOM A> CUSTOM PATTERN (LOWER 11 BITS) | | | | | | | | | | | |
| 0C | <FINE GAIN> FINE GAIN CONTROL (1dB to 6 dB) | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | <CUSTOM B> CUSTOM PATTERN (MSB BIT) |
| 0D | <OVRD> OVERRIDE BIT | 0 | 0 | BYTE-WISE OR BIT-WISE | MSB OR LSB FIRST | <COARSE GAIN> COURSE GAIN ENABLE | FALLING OR RISING BIT CLOCK CAPTURE EDGE | 0 | 12-BIT OR 14-BIT SERIALIZE | DDR OR SDR BIT CLOCK | 1-WIRE OR 2-WIRE INTERFACE | |
| 10 | <TERM CLK> LVDS INTERNAL TERMINATION BIT AND WORD CLOCKS | | | | | <LVDS CURR> LVDS CURRENT SETTINGS | | | | <CURR DOUBLE> LVDS CURRENT DOUBLE | | |
| 11 | WORD-WISE CONTROL | 0 | 0 | 0 | 0 | <TERM DATA> LVDS INTERNAL TERMINATION - DATA OUTPUTS | | | | | | |

- (1) The unused bits in each register (shown by blank cells in above table) must be programmed as 0.
- (2) Multiple functions in a register can be programmed in a single write operation.
- (3) After a hardware or software reset, all register bits are cleared to 0.

DESCRIPTION OF SERIAL REGISTERS

Table 11. Serial Register A⁽¹⁾

| REGISTER ADDRESS | BITS | | | | | | | | | | | |
|------------------|--------------------|-----|----|----|----|----|-------------------------------------|---------------------------------|--------------------------------|---------------------------------|---------------------------------|----------------------------------|
| | A4 - A0 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00 | <RST> S/W RESET | 0 | 0 | 0 | 0 | 0 | <REF> INTERNAL OR EXTERNAL | <PDN CHD> POWER DOWN CH D | <PDN CHC> POWER DOWN CHC | <PDN CHB> POWER DOWN CH B | <PDN CHA> POWER DOWN CH A | <PDN> GLOBAL POWER DOWN |

(1) After a hardware or software reset, all register bits are cleared to 0.

| D0 - D4 | | Power down modes |
|----------------|--|--|
| D0 | | <PDN GLOBAL> |
| 0 | | Normal operation |
| 1 | | Global power down, including all channels ADCs, internal references, internal PLL and output buffers |
| D1 | | <PDN CHA> |
| 0 | | CH A Powered up |
| 1 | | CH A ADC Powered down |
| D2 | | <PDN CHB> |
| 0 | | CH B Powered up |
| 1 | | CH B ADC Powered down |
| D3 | | <PDN CHC> |
| 0 | | CH C Powered up |
| 1 | | CH C ADC Powered down |
| D4 | | <PDN CHD> |
| 0 | | CH D Powered up |
| 1 | | CH D ADC Powered down |
| D5 | | <REF> Reference |
| 0 | | Internal reference enabled |
| 1 | | External reference enabled |
| D10 | | <RST> |
| 1 | | Software reset applied – resets all internal registers and self-clears to 0 |

Table 12. Serial Register B⁽¹⁾

| REGISTER ADDRESS | BITS | | | | | | | | | | | |
|------------------|---------|-----|----|----|---|----|----|----|----|----|----|----|
| | A4 - A0 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 04 | 0 | 0 | 0 | 0 | <CLKIN GAIN> INPUT CLOCK BUFFER GAIN CONTROL | | | | | | 0 | 0 |

(1) After a hardware or software reset, all register bits are cleared to 0.

D6 - D2 <CLKIN GAIN> [Input clock buffer gain control](#)

| | |
|-------|----------------------------------|
| 11000 | Gain 0, minimum gain |
| 00000 | Gain 1, default gain after reset |
| 01100 | Gain 2 |
| 01010 | Gain 3 |
| 01001 | Gain 4 |
| 01000 | Gain 5, maximum gain |

Table 13. Serial Register C⁽¹⁾

| REGISTER ADDRESS | BITS | | | | | | | | | | | |
|------------------|---------|--|----|-----------------------------|----|----|----|----|----|----|----|----|
| | A4 - A0 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00 | 0 | <DF> DATA DORMAT 2S COMP OR STRAIGHT BINARY | 0 | <PATTERNS> TEST PATTERNS | | | | 0 | 0 | 0 | 0 | 0 |

(1) After a hardware or software reset, all register bits are cleared to 0.

D7 - D5 <PATTERNS> [Capture test patterns](#)

| | |
|-----|--|
| 000 | Normal ADC operation |
| 001 | Output all zeros |
| 010 | Output all ones |
| 011 | Output toggle pattern |
| 100 | Unused |
| 101 | Output custom pattern (contents of CUSTOM pattern registers 0x0B and 0x0C) |
| 110 | Output DESKEW pattern (serial stream of 1010..) |
| 111 | Output SYNC pattern |

D9 <DF> Data format selection

| | |
|---|------------------------|
| 0 | 2s Complement format |
| 1 | Straight binary format |

Table 14. Serial Register D⁽¹⁾

| REGISTER ADDRESS | BITS | | | | | | | | | | |
|------------------|--|----|----|----|----|----|----|----|----|----|----|
| A4 - A0 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0B | <CUSTOM A> CUSTOM PATTERN (LOWER 11 BITS) | | | | | | | | | | |

(1) After a hardware or software reset, all register bits are cleared to 0.

D10 - D0 <CUSTOM A> Lower 11 bits of custom pattern <D10>...<D0>

Table 15. Serial Register E⁽¹⁾

| REGISTER ADDRESS | BITS | | | | | | | | | | |
|------------------|---|----|----|----|----|----|----|----|----|----|--|
| A4 - A0 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0C | <FINE GAIN> FINE GAIN CONTROL (1 dB to 6 dB) | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | <CUSTOM B> CUSTOM PATTERN (MSB BIT) |

(1) After a hardware or software reset, all register bits are cleared to 0.

D4 - D0 <CUSTOM B> MSB bit of custom pattern <D11>

D10-D8 <FINE GAIN> [Fine gain control](#)

| | |
|-----|--|
| 000 | 0 dB Gain (full-scale range = 2.00 V _{PP}) |
| 001 | 1 dB Gain (full-scale range = 1.78 V _{PP}) |
| 010 | 2 dB Gain (full-scale range = 1.59 V _{PP}) |
| 011 | 3 dB Gain (full-scale range = 1.42 V _{PP}) |
| 100 | 4 dB Gain (full-scale range = 1.26 V _{PP}) |
| 101 | 5 dB Gain (full-scale range = 1.12 V _{PP}) |
| 110 | 6 dB Gain (full-scale range = 1.00 V _{PP}) |

Table 16. Serial Register F⁽¹⁾

| REGISTER ADDRESS | BITS | | | | | | | | | | |
|------------------|--------------------------|----|----|-----------------------------|---------------------|--|--|----|----------------------------------|----------------------------|----------------------------------|
| A4 - A0 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0D | <OVRD> OVER-RIDE BITE | 0 | 0 | BYTE-WISE OR BIT-WISE | MSB OR LSB FIRST | <COARSE GAIN> COARSE GAIN ENABLE | FALLING OR RISING BIT CLOCK CAPTURE EDGE | 0 | 14-BIT OR 16-BIT SERIALIZE | DDR OR SDR BIT CLOCK | 1-WIRE OR 2-WIRE INTERFACE |

(1) After a hardware or software reset, all register bits are cleared to 0.

D0 **Interface selection**

| | |
|---|------------------|
| 0 | 1 Wire interface |
| 1 | 2 Wire interface |

D1 **Bit clock selection** (only in 2-wire interface)

| | |
|---|---------------|
| 0 | DDR Bit clock |
| 1 | SDR Bit clock |

D2 **Serialization selection**

| | |
|---|-------------------|
| 0 | 12x Serialization |
| 1 | 14x Serialization |

| | |
|------------|--|
| D4 | Bit clock capture edge (only when SDR bit clock is selected, D1 = 1) |
| 0 | Capture data with falling edge of bit clock |
| 1 | Capture data with rising edge of bit clock |
| D5 | <COARSE GAIN> Coarse gain control |
| 0 | 0 dB coarse gain |
| 1 | 3.5dB coarse gain (full-scale range = 1.34 V _{PP}) |
| D6 | MSB or LSB first selection |
| 0 | MSB First |
| 1 | LSB First |
| D7 | Byte/bit wise outputs (only when 2-wire is selected) |
| 0 | Byte wise |
| 1 | Bit wise |
| D10 | <OVRD> Over-ride bit. All the functions in register 0x0D can also be controlled using the parallel control pins. By setting bit <OVRD> = 1, the contents of register 0x0D will over-ride the settings of the parallel pins. |
| 0 | Disable over-ride |
| 1 | Enable over-ride |

Table 17. Serial Register G⁽¹⁾

| REGISTER ADDRESS | BITS | | | | | | | | | | |
|------------------|---|-----|----|----|----|--------------------------------------|----|----|----|--------------------------------------|----|
| | A4 - A0 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 |
| 10 | <TERM CLK> LVDS INTERNAL TERMINATION BIT AND WORD CLOCKS | | | | | <LVDS CURR> LVDS CURRENT SETTINGS | | | | <LVDS DOUBLE> LVDS CURRENT DOUBLE | |

(1) After a hardware or software reset, all register bits are cleared to 0.

| | |
|--------------|---|
| D0 | <CURR DOUBLE> LVDS current double for data outputs |
| 0 | Nominal LVDS current, as set by <D5...D2> |
| 1 | Double the nominal value |
| D1 | <CURR DOUBLE> LVDS current double for bit and word clock outputs |
| 0 | Nominal LVDS current, as set by <D5...D2> |
| 1 | Double the nominal value |
| D3-D2 | <LVDS CURR> LVDS current setting for data outputs |
| 00 | 3.5 mA |
| 01 | 4 mA |
| 10 | 2.5 mA |
| 11 | 3 mA |
| D5-D4 | <LVDS CURR> LVDS current setting for bit and word clock outputs |
| 00 | 3.5 mA |
| 01 | 4 mA |

10 2.5 mA
 11 3 mA

D10-D6 <TERM CLK> LVDS internal termination for bit and word clock outputs

00000 No internal termination
 00001 166 Ω
 00010 200 Ω
 00100 250 Ω
 01000 333 Ω
 10000 500 Ω

Any combination of above bits can also be programmed, resulting in a parallel combination of the selected values. For example, 00101 is the parallel combination of 166||250 = 100 Ω

00101 100 Ω

Table 18. Serial Register H⁽¹⁾

| REGISTER ADDRESS | BITS | | | | | | | | | | | |
|------------------|-------------------|-----|----|----|----|----|---|----|----|----|----|----|
| | A4 - A0 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 11 | WORD-WISE CONTROL | | 0 | 0 | 0 | 0 | <TERM DATA> LVDS INTERNAL TERMINATION - DATA OUTPUTS | | | | | |

(1) After a hardware or software reset, all register bits are cleared to 0.

D4-D0 <TERM DATA> LVDS internal termination for data outputs

00000 No internal termination
 00001 166 Ω
 00010 200 Ω
 00100 250 Ω
 01000 333 Ω
 10000 500 Ω

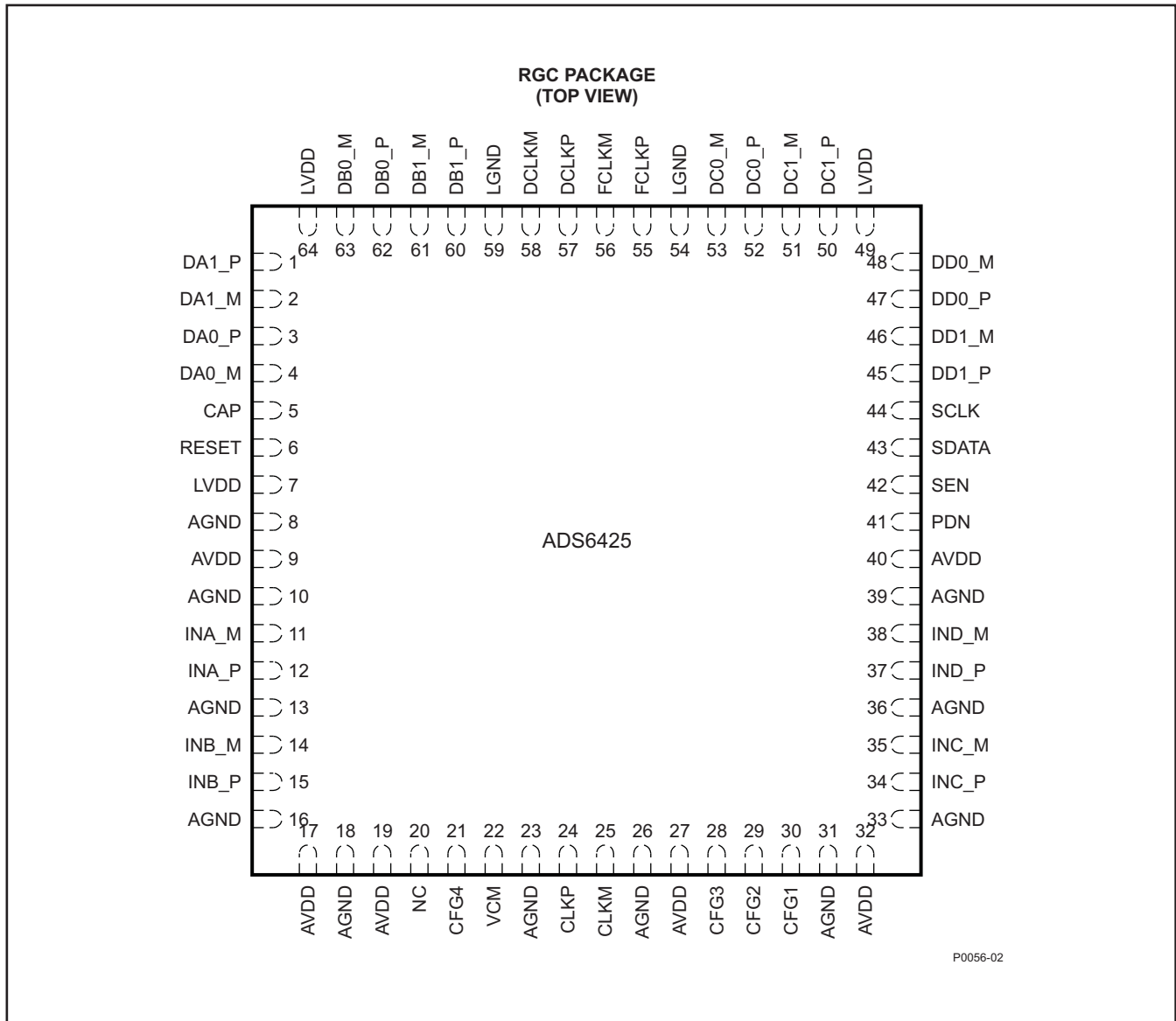
Any combination of above bits can also be programmed, resulting in a parallel combination of the selected values. For example, 00101 is the parallel combination of 166||250 = 100 Ω

00101 100 Ω

D10-D9 Only when 2-wire interface is selected

00 Byte-wise or bit-wise output, 1x frame clock
 11 Word-wise output enabled, 0.5x frame clock
 01,10 Do not use

PIN CONFIGURATION (2-WIRE INTERFACE)



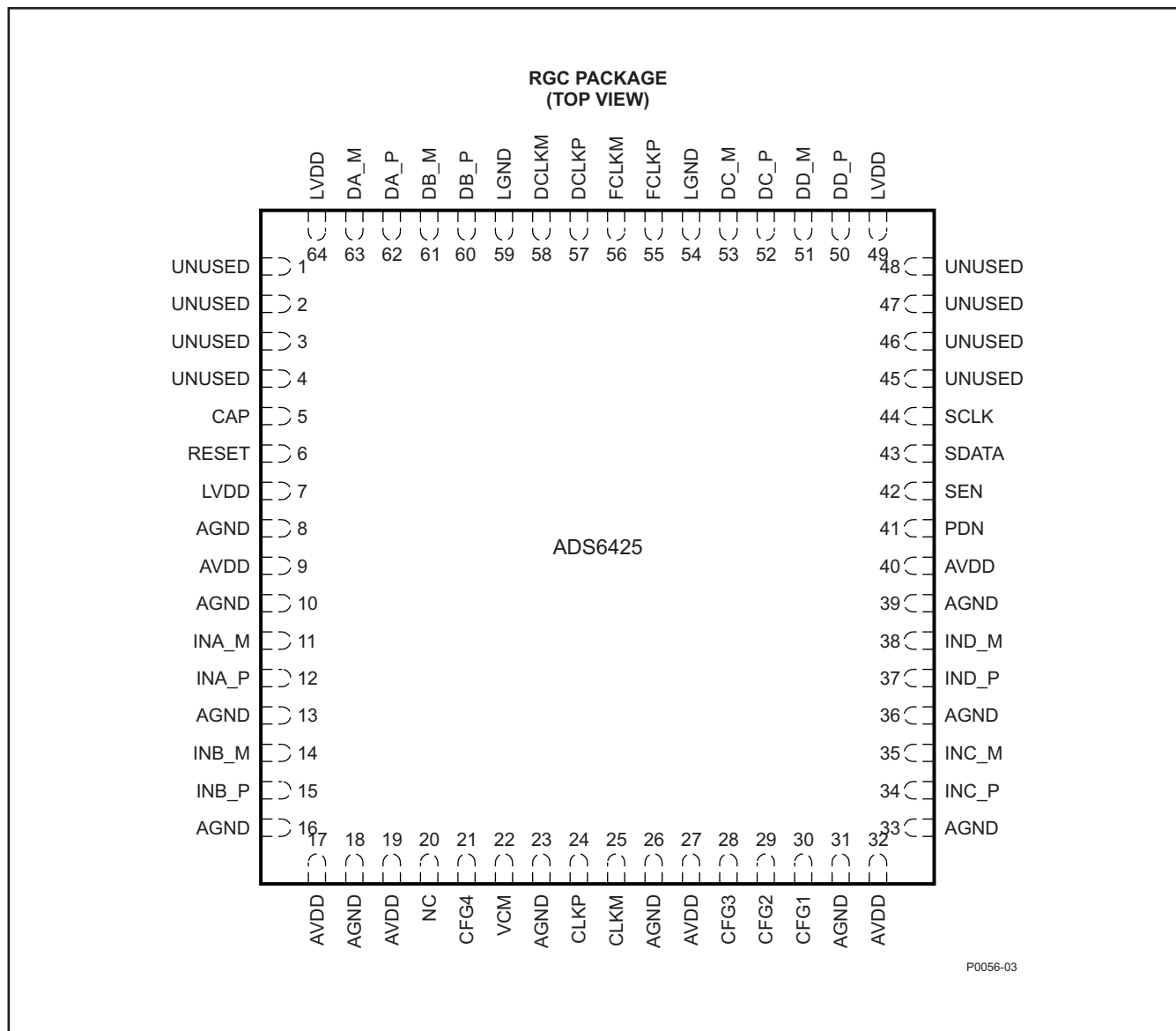
PIN ASSIGNMENTS (2-WIRE INTERFACE)

| PINS | | I/O | NO. OF PINS | DESCRIPTION |
|-------------------------------|---|-----|-------------|---|
| NAME | NO. | | | |
| SUPPLY AND GROUND PINS | | | | |
| AVDD | 9,17,19,27,32,40, | | 6 | Analog power supply |
| AGND | 8,10,13,16,18,23,26, 31,33 36,39, | | 11 | Analog ground |
| LVDD | 7,49,64 | | 3 | Digital power supply |
| LGND | 54,59 | | 2 | Digital ground |
| INPUT PINS | | | | |
| CLKP, CLKM | 24,25 | I | 2 | Differential input clock pair |
| INA_P, INA_M | 12,11 | I | 2 | Differential input signal pair, channel A. If unused, the pins should be tied to VCM and not floated. |

PIN ASSIGNMENTS (2-WIRE INTERFACE) (continued)

| PINS | | I/O | NO. OF PINS | DESCRIPTION |
|--------------------|-------|-----|-------------|---|
| NAME | NO. | | | |
| INB_P, INB_M | 15,14 | I | 2 | Differential input signal pair, channel B. If unused, the pins should be tied to VCM and not floated. |
| INC_P, INC_M | 34,35 | I | 2 | Differential input signal pair, channel C. If unused, the pins should be tied to VCM and not floated. |
| IND_P, IND_M | 37,38 | I | 2 | Differential input signal pair, channel D. If unused, the pins should be tied to VCM and not floated. |
| CAP | 5 | | 1 | Connect 2nF capacitor from pin to ground |
| SCLK | 44 | I | 1 | This pin functions as serial interface clock input when RESET is low. When RESET is high , it controls DESKEW, SYNC and global POWER DOWN modes (along with SDATA). See Table 3 for description. This pin has an internal pull-down resistor. |
| SDATA | 43 | I | 1 | This pin functions as serial interface data input when RESET is low. When RESET is high , it controls DESKEW, SYNC and global POWER DOWN modes (along with SCLK). See Table 3 for description. This pin has an internal pull-down resistor. |
| SEN | 42 | I | 1 | This pin functions as serial interface enable input when RESET is low. When RESET is high , it controls coarse gain and internal/external reference modes. See Table 4 for description. This pin has an internal pull-up resistor. |
| RESET | 6 | I | 1 | Serial interface reset input. When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset option. Refer to the Serial Interface section. In parallel interface mode, tie RESET permanently high . (SCLK, SDATA and SEN function as parallel control pins in this mode). The pin has an internal pull-down resistor to ground. |
| PDN | 41 | I | 1 | Global power down control pin. |
| CFG1 | 30 | I | 1 | Parallel input pin. It controls 1-wire or 2-wire interface and DDR or SDR bit clock selection. See Table 6 for description. Tie to AVDD for 2-wire interface with DDR bit clock. |
| CFG2 | 29 | I | 1 | Parallel input pin. It controls 12x or 14x serialization and SDR bit clock capture edge. See Table 7 for description. For 12x serialization with DDR bit clock, tie to ground or AVDD. |
| CFG3 | 28 | I | 1 | RESERVED pin - Tie to ground. |
| CFG4 | 21 | I | 1 | Parallel input pin. It controls data format and MSB or LSB first modes. See Table 9 for description. |
| VCM | 22 | I/O | 1 | Internal reference mode – common-mode voltage output External reference mode – reference input. The voltage forced on this pin sets the internal reference. |
| OUTPUT PINS | | | | |
| DA0_P,DA0_M | 3,4 | O | 2 | Channel A differential LVDS data output pair, wire 0 |
| DA1_P,DA1_M | 1,2 | O | 2 | Channel A differential LVDS data output pair, wire 1 |
| DB0_P,DB0_M | 62,63 | O | 2 | Channel B differential LVDS data output pair, wire 0 |
| DB1_P,DB1_M | 60,61 | O | 2 | Channel B differential LVDS data output pair, wire 1 |
| DC0_P,DC0_M | 52,53 | O | 2 | Channel C differential LVDS data output pair, wire 0 |
| DC1_P,DC1_M | 50,51 | O | 2 | Channel C differential LVDS data output pair, wire 1 |
| DD0_P,DD0_M | 47,48 | O | 2 | Channel D differential LVDS data output pair, wire 0 |
| DD1_P,DD1_M | 45,46 | O | 2 | Channel D differential LVDS data output pair, wire 1 |
| DCLKP,DCLKM | 57,58 | O | 2 | Differential bit clock output pair |
| FCLKP,FCLKM | 55,56 | O | 2 | Differential frame clock output pair |
| NC | 20 | | 1 | Do Not Connect |

PIN CONFIGURATION (1-WIRE INTERFACE)



PIN ASSIGNMENTS (1-WIRE INTERFACE)

| PINS | | I/O | NO. OF PINS | DESCRIPTION |
|-------------------------------|---|-----|-------------|---|
| NAME | NO. | | | |
| SUPPLY AND GROUND PINS | | | | |
| AVDD | 9,17,19,27,32,40, | | 6 | Analog power supply |
| AGND | 8,10,13,16,18,23,26, 31,33 36,39, | | 11 | Analog ground |
| LVDD | 7,49,64 | | 3 | Digital power supply |
| LGND | 54,59 | | 2 | Digital ground |
| INPUT PINS | | | | |
| CLKP, CLKM | 24,25 | I | 2 | Differential input clock pair |
| INA_P, INA_M | 12,11 | I | 2 | Differential input signal pair, channel A. If unused, the pins should be tied to VCM and not floated. |

PIN ASSIGNMENTS (1-WIRE INTERFACE) (continued)

| PINS | | I/O | NO. OF PINS | DESCRIPTION |
|--------------------|-----------|-----|-------------|---|
| NAME | NO. | | | |
| INB_P, INB_M | 15,14 | I | 2 | Differential input signal pair, channel B. If unused, the pins should be tied to VCM and not floated. |
| INC_P, INC_M | 34,35 | I | 2 | Differential input signal pair, channel C. If unused, the pins should be tied to VCM and not floated. |
| IND_P, IND_M | 37,38 | I | 2 | Differential input signal pair, channel D. If unused, the pins should be tied to VCM and not floated. |
| CAP | 5 | | 1 | Connect 2nF capacitance from pin to ground |
| SCLK | 44 | I | 1 | This pin functions as serial interface clock input when RESET is low . When RESET is high , it controls DESKEW, SYNC and global POWER DOWN modes (along with SDATA). See Table 3 for description. This pin has an internal pull-down resistor. |
| SDATA | 43 | I | 1 | This pin functions as serial interface data input when RESET is low . When RESET is high , it controls DESKEW, SYNC and global POWER DOWN modes (along with SCLK). See Table 3 for description. This pin has an internal pull-down resistor. |
| SEN | 42 | I | 1 | This pin functions as serial interface enable input when RESET is low . When RESET is high , it controls coarse gain and internal/external reference modes. See Table 4 for description. This pin has an internal pull-up resistor. |
| RESET | 6 | I | 1 | Serial interface reset input. When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset option. Refer to the Serial Interface section. In parallel interface mode, tie RESET permanently high . (SCLK, SDATA and SEN function as parallel control pins in this mode). The pin has an internal pull-down resistor to ground. |
| PDN | 41 | I | 1 | Global power down control pin. |
| CFG1 | 30 | I | 1 | Parallel input pin. It controls 1-wire or 2-wire interface and DDR or SDR bit clock selection. See Table 6 for description. Tie to ground for 1-wire interface with DDR bit clock. |
| CFG2 | 29 | I | 1 | Parallel input pin. It controls 12x or 14x serialization and SDR bit clock capture edge. See Table 7 for description. For 12x serialization with DDR bit clock, tie to ground or AVDD. |
| CFG3 | 28 | I | 1 | RESERVED pin - Tie to ground . |
| CFG4 | 21 | I | 1 | Parallel input pin. It controls data format and MSB or LSB first modes. See Table 9 for description. |
| VCM | 22 | I/O | 1 | Internal reference mode – common-mode voltage output External reference mode – reference input. The voltage forced on this pin sets the internal reference. |
| OUTPUT PINS | | | | |
| DA_P,DA_M | 62,63 | O | 2 | Channel A differential LVDS data output pair |
| DB_P,DB_M | 60,61 | O | 2 | Channel B differential LVDS data output pair |
| DC_P,DC_M | 52,53 | O | 2 | Channel C differential LVDS data output pair |
| DD_P,DD_M | 50,51 | O | 2 | Channel D differential LVDS data output pair |
| DCLKP,DCLKM | 57,58 | O | 2 | Differential bit clock output pair |
| FCLKP,FCLKM | 55,56 | O | 2 | Differential frame clock output pair |
| UNUSED | 1-4,45-48 | | 8 | These pins are unused in the 1-wire interface. Do not connect |
| NC | 20 | | 1 | Do not connect |

TYPICAL CHARACTERISTICS

All plots are at 25°C, AVDD = LVDD = 3.3 V, sampling frequency = 125 MSPS, sine wave input clock, 1.5 V_{pp} differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, 32K point FFT (unless otherwise noted)

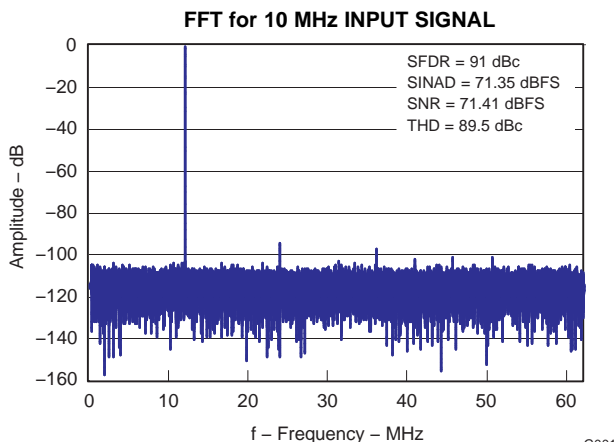


Figure 6.

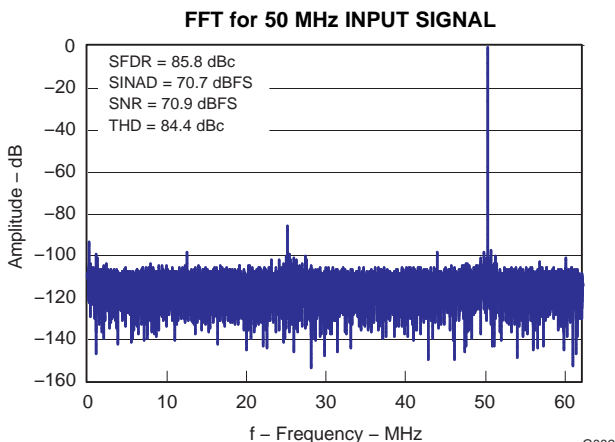


Figure 7.

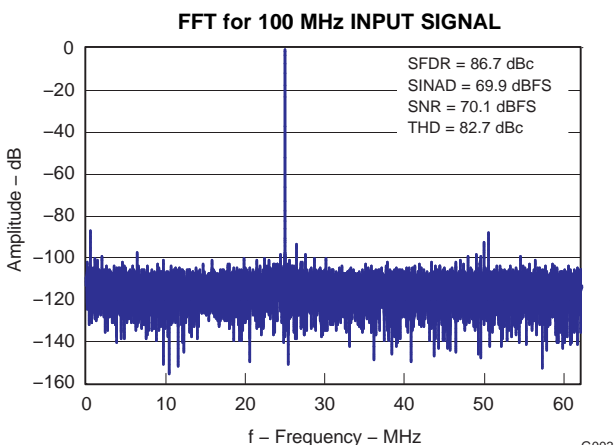


Figure 8.

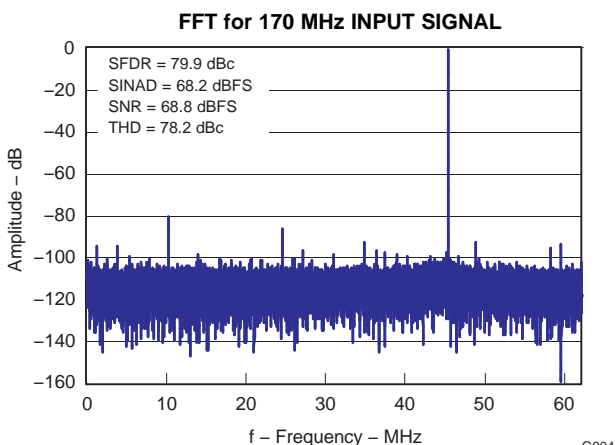


Figure 9.

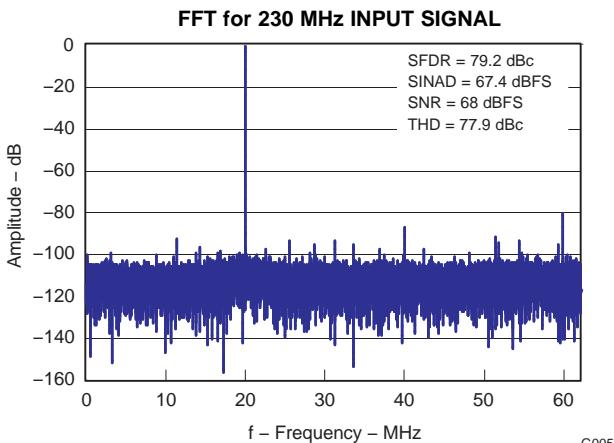


Figure 10.

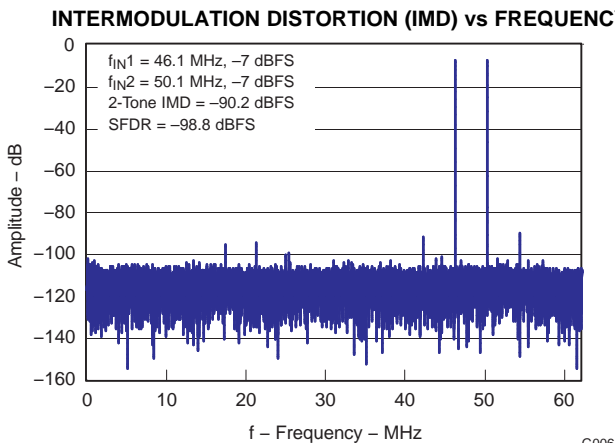


Figure 11.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = LVDD = 3.3 V, sampling frequency = 125 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, 32K point FFT (unless otherwise noted)

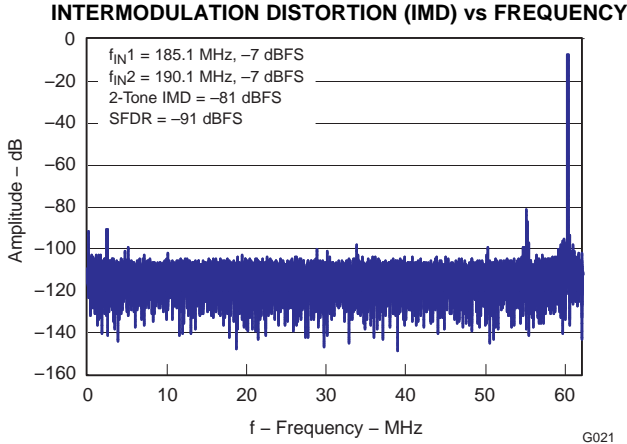


Figure 12.

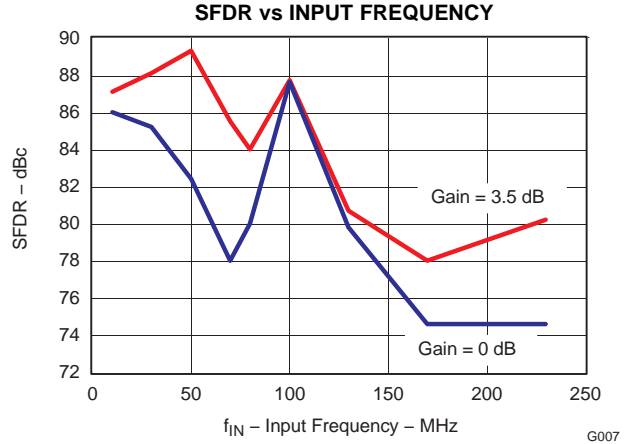


Figure 13.

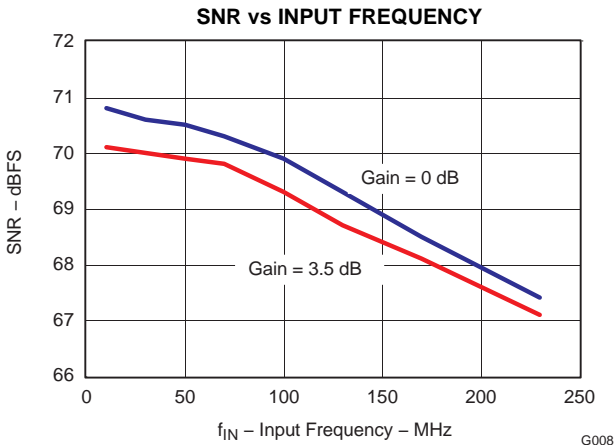


Figure 14.

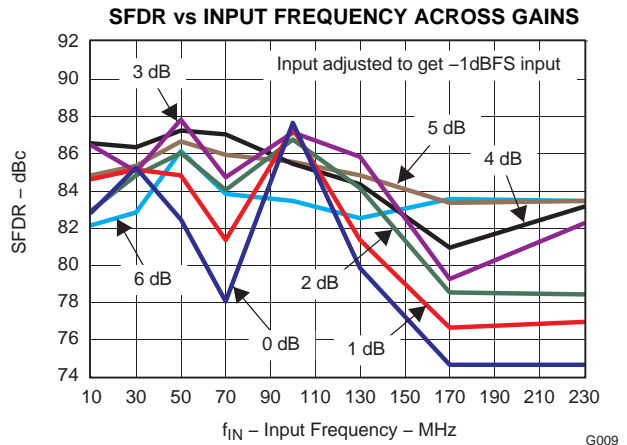


Figure 15.

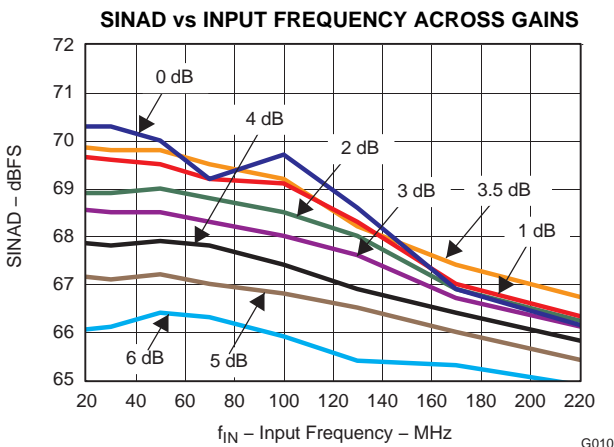


Figure 16.

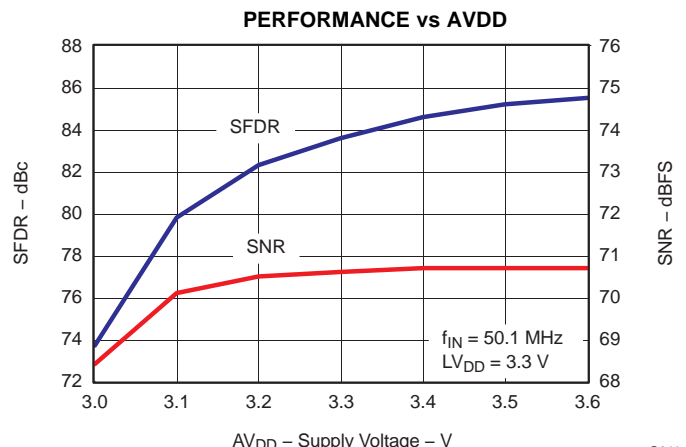


Figure 17.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = LVDD = 3.3 V, sampling frequency = 125 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, 32K point FFT (unless otherwise noted)

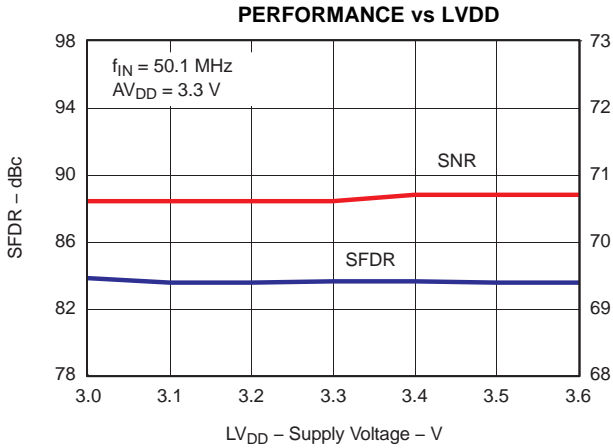


Figure 18.

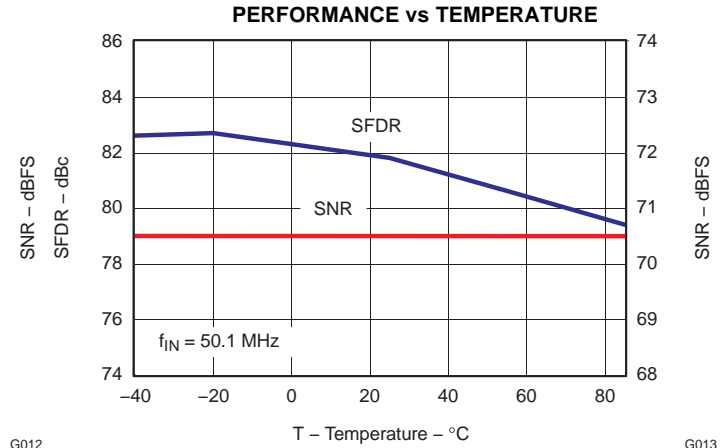


Figure 19.

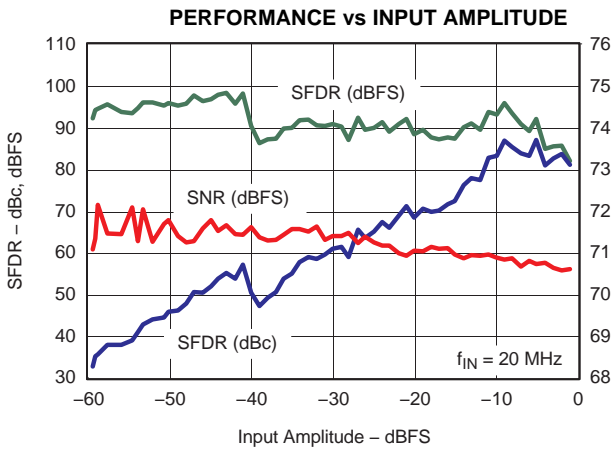


Figure 20.

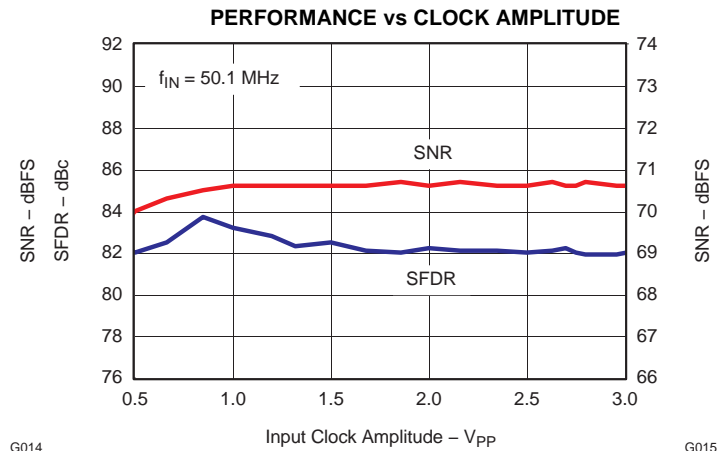


Figure 21.

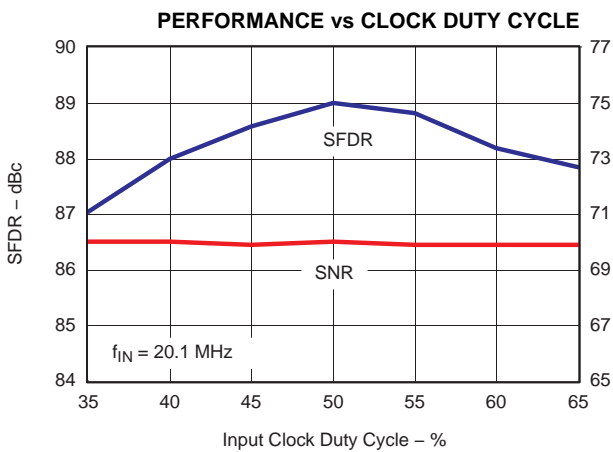


Figure 22.

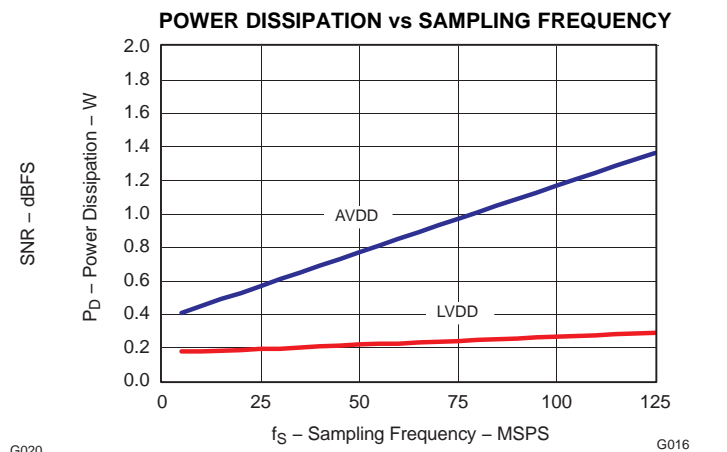
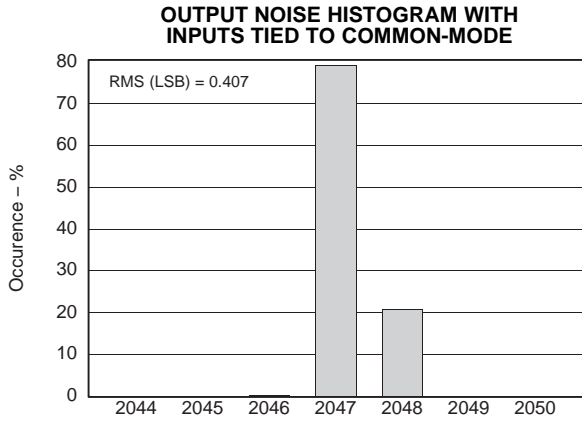


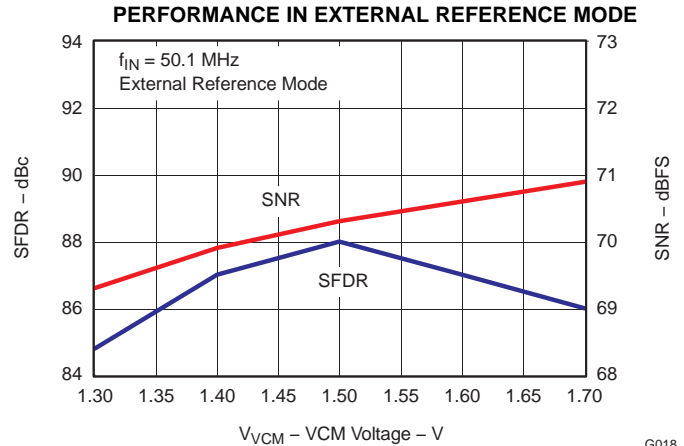
Figure 23.

TYPICAL CHARACTERISTICS (continued)

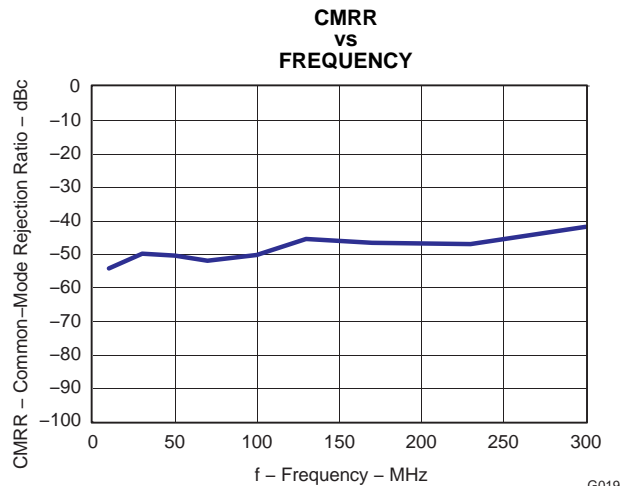
All plots are at 25°C, AVDD = LVDD = 3.3 V, sampling frequency = 125 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, 32K point FFT (unless otherwise noted)



Output Code G017
Figure 24.



V_{VCM} – VCM Voltage – V G018
Figure 25.



f – Frequency – MHz G019
Figure 26.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = LVDD = 3.3 V, sampling frequency = 125 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, 32K point FFT (unless otherwise noted)

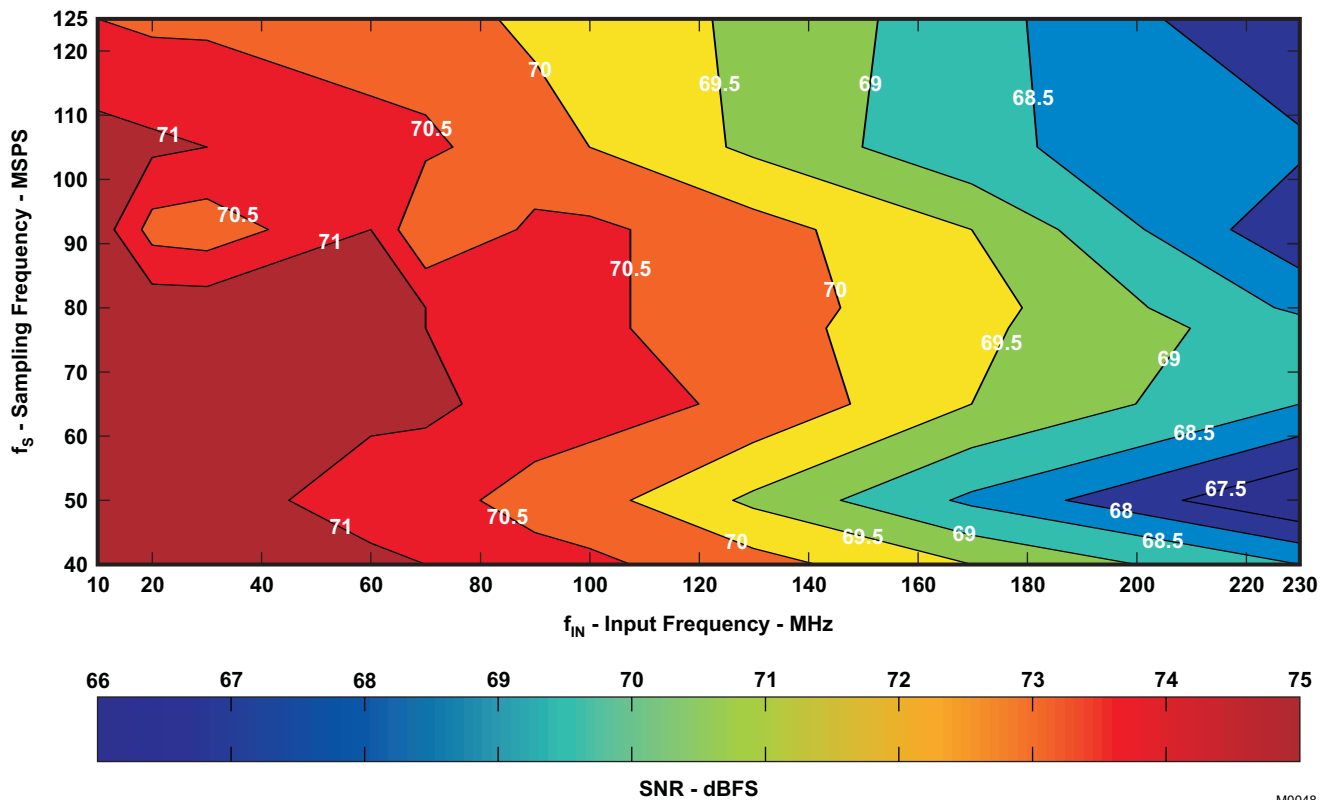
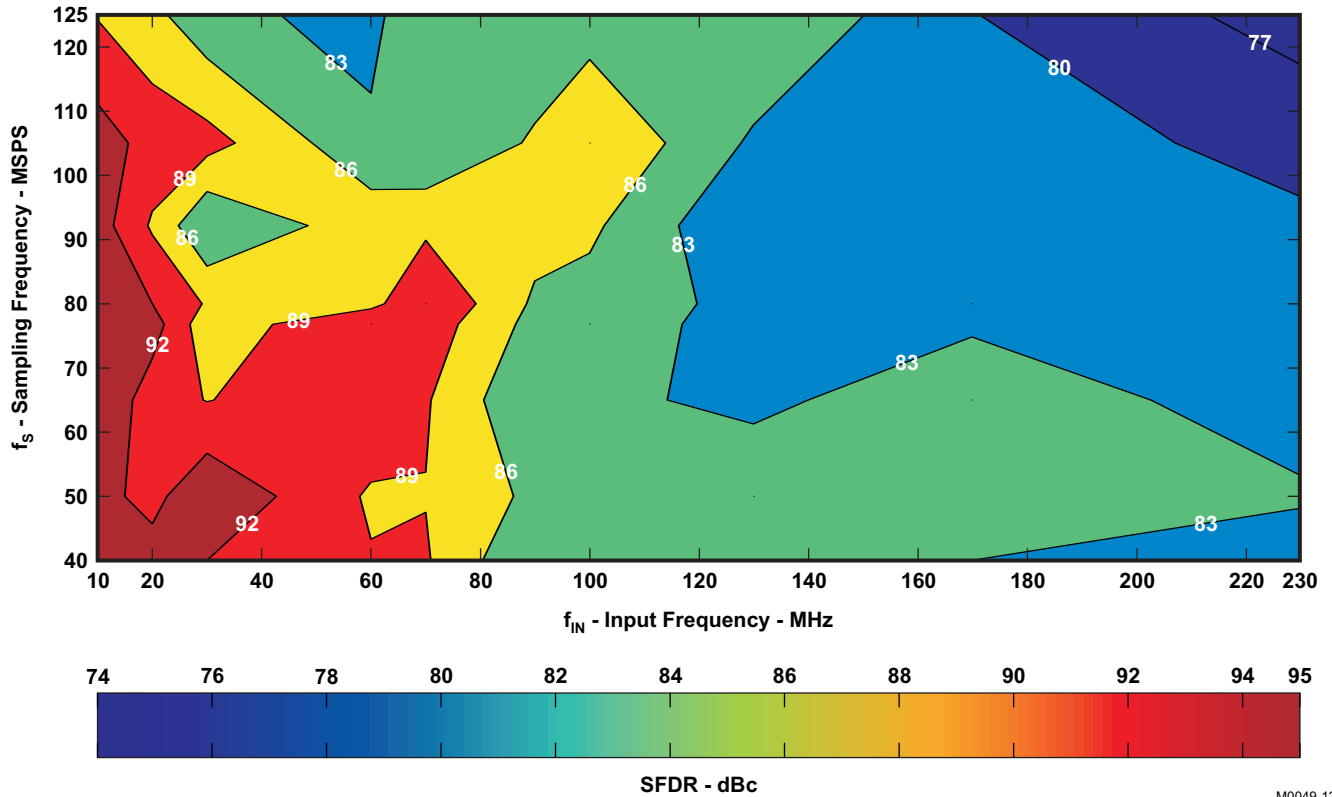


Figure 27. SNR Contour

M0048-12

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = LVDD = 3.3 V, sampling frequency = 125 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, 32K point FFT (unless otherwise noted)



M0049-12

Figure 28. SFDR Contour

APPLICATION INFORMATION

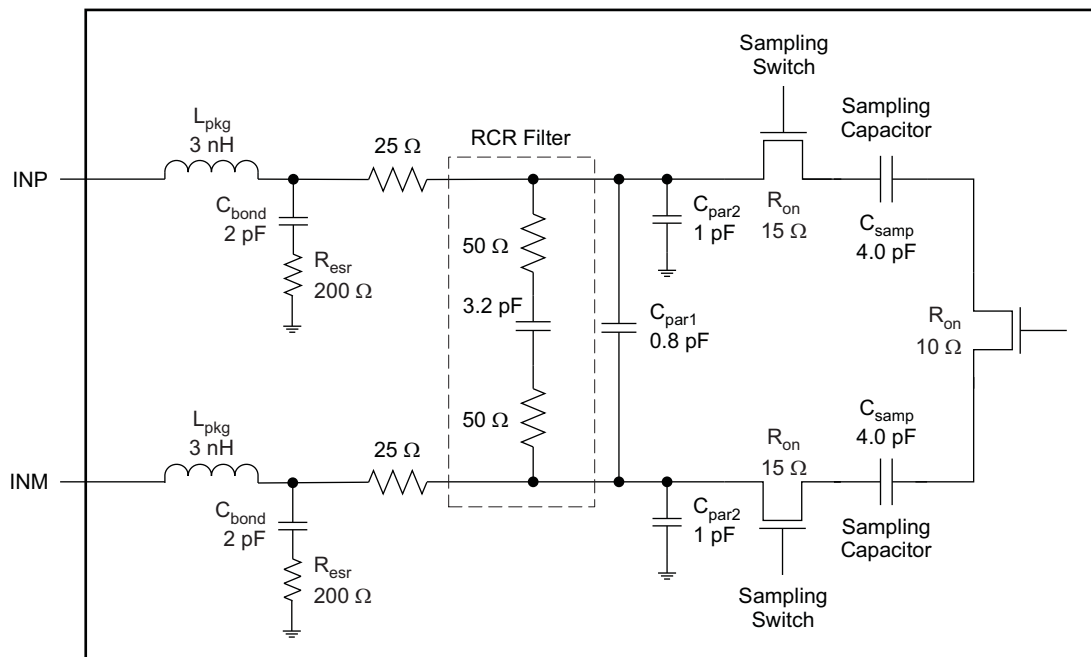
THEORY OF OPERATION

The ADS6425 is a quad channel, 12-bit, 125-MSPS, pipeline ADC, based on switched capacitor architecture in CMOS technology.

The conversion is initiated simultaneously by all the four channels at the rising edge of the external input clock. After the input signals are captured by the sample and hold circuit of each channel, the samples are sequentially converted by a series of low resolution stages. The stage outputs are combined in a digital correction logic block to form the final 12-bit word with a latency of 12 clock cycles. The 12-bit word of each channel is serialized and output as LVDS levels. In addition to the data streams, a bit clock and a frame clock are also output. The frame clock is aligned with the 12-bit word boundary.

ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture, shown in Figure 29. This differential topology results in very good AC performance even for high input frequencies. The INP and INM pins have to be externally biased around a common-mode voltage of 1.5 V, available on VCM pin 13. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between $V_{CM} + 0.5\text{ V}$ and $V_{CM} - 0.5\text{ V}$, resulting in a $2\text{-}V_{pp}$ differential input swing. The maximum swing is determined by the internal reference voltages REFP (2.0V nominal) and REFM (1.0 V, nominal). The sampling circuit has a 3 dB bandwidth that extends up to 500 MHz (Figure 30, shown by the transfer function from the analog input pins to the voltage across the sampling capacitors TF_ADC).



S0237-01

Figure 29. Input Sampling Circuit

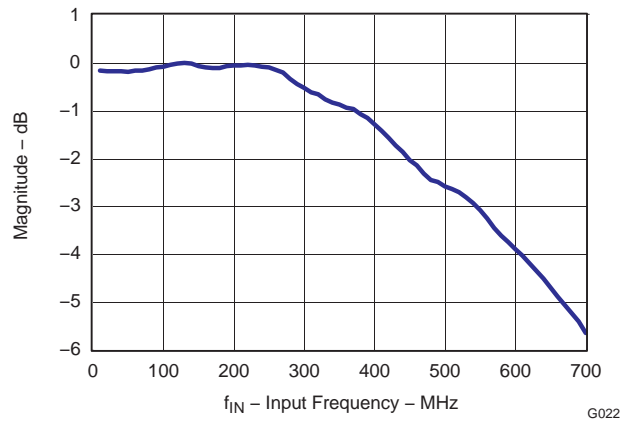


Figure 30. Analog Input Bandwidth (represented by magnitude of TF_ADC, see Figure 31)

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection.

A 5-Ω resistor in series with each input pin is recommended to damp out ringing caused by the package parasitics. It is also necessary to present low impedance (< 50 Ω) for the common mode switching currents. For example, this is achieved by using two resistors from each input terminated to the common mode voltage (VCM).

Using RF-Transformer Based Drive Circuits

Figure 31 shows a configuration using a single 1:1 turns ratio transformer (for example, WBC1-1) that can be used for low input frequencies up to 100MHz.

The single-ended signal is fed to the primary winding of the RF transformer. The transformer is terminated on the secondary side. Putting the termination on the secondary side helps to shield the kickbacks caused by the sampling circuit from the RF transformer’s leakage inductances. The termination is accomplished by two resistors connected in series, with the center point connected to the 1.5 V common mode (VCM pin). The value of the termination resistors (connected to common mode) has to be low (< 100 Ω) to provide a low-impedance path for the ADC common-mode switching current.

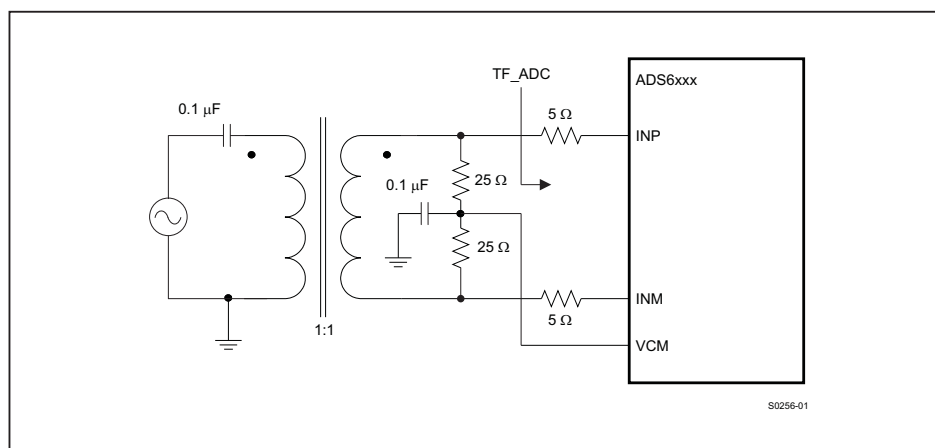


Figure 31. Single Transformer Drive Circuit

At high input frequencies, the mismatch in the transformer parasitic capacitance (between the windings) results

in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch, and good performance is obtained for high frequency input signals. Figure 32 shows an example using two transformers (Coilcraft WBC1-1). An additional termination resistor pair (enclosed within the shaded box in Figure 32) may be required between the two transformers to improve the balance between the P and M sides. The center point of this termination must be connected to ground.

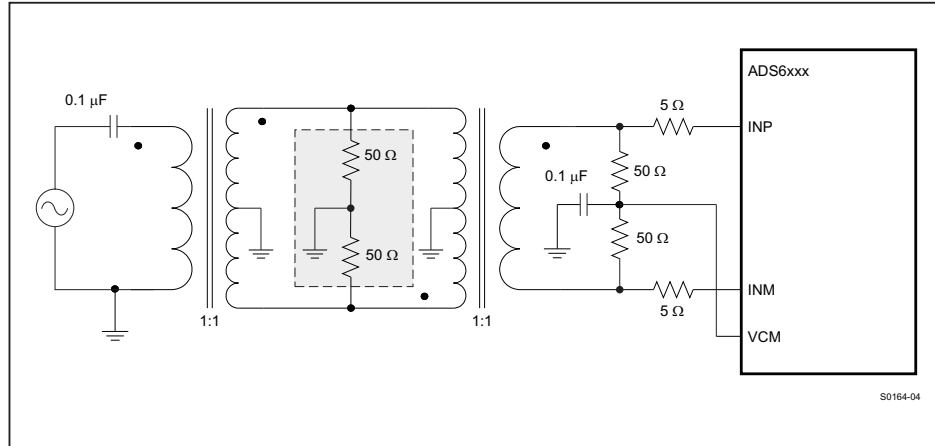


Figure 32. Two Transformer Drive Circuit

INPUT COMMON MODE

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1- μ F low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. The input stage of the ADC sinks a common-mode current in the order of 155 μ A at 125 MSPS (per input pin). Equation 1 describes the dependency of the common-mode current and the sampling frequency.

$$\frac{155 \mu\text{A} \times F_s}{125 \text{ MSPS}} \quad (1)$$

This equation helps to design the output capability and impedance of the CM driving circuit accordingly.

REFERENCE

The ADS6425 has built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the on-chip integration of the requisite reference capacitors eliminates the need for external decoupling. The full-scale input range of the converter can be controlled in the external reference mode as explained below. The internal or external reference modes can be selected by programming the register bit <REF> (Table 11).

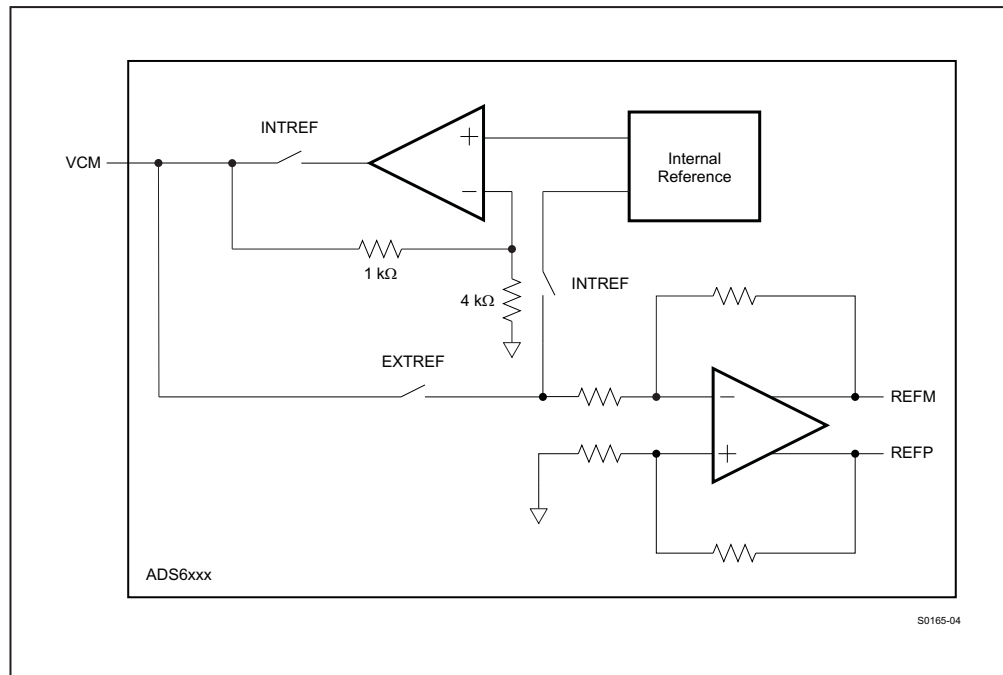


Figure 33. Reference Section

Internal Reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. Common-mode voltage (1.5 V nominal) is output on VCM pin, which can be used to externally bias the analog input pins.

External Reference

When the device is in external reference mode, the VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained by 1.33 internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by [Equation 2](#).

$$\text{Full-scale differential input pp} = (\text{Voltage forced on VCM}) \times 1.33 \quad (2)$$

In this mode, the range of voltage applied on VCM pin should be 1.45 to 1.55V. The 1.5-V common-mode voltage to bias the input pins has to be generated externally.

COARSE GAIN AND PROGRAMMABLE FINE GAIN

The ADS6425 includes gain settings that can be used to get improved SFDR performance (compared to 0 dB gain mode). The gain settings are 3.5 dB coarse gain and programmable fine gain from 0 dB to 6 dB. For each gain setting, the analog input full-scale range scales proportionally, as shown in [Table 19](#).

The coarse gain is a fixed setting of 3.5 dB and is designed to improve SFDR with little degradation in SNR (as seen in [Figure 13](#) and [Figure 14](#)). The fine gain is programmable in 1 dB steps from 0 to 6 dB. With the fine gain also, SFDR improvement is achieved, but at the expense of SNR (there will be about 1dB SNR degradation for every 1dB of fine gain).

So, the fine gain can be used to trade-off between SFDR and SNR. The coarse gain makes it possible to get best SFDR but without losing SNR significantly. At high input frequencies, the gains are especially useful as the SFDR improvement is significant with marginal degradation in SINAD.

The gains can be programmed using the register bits **<COARSE GAIN>** ([Table 16](#)) and **<FINE GAIN>** ([Table 15](#)). Note that the default gain after reset is 0 dB.

Table 19. Full-Scale Range Across Gains

| GAIN, dB | TYPE | FULL-SCALE, V _{pp} |
|----------|-----------------------------|-----------------------------|
| 0 | Default (after reset) | 2 |
| 3.5 | Coarse setting (fixed) | 1.34 |
| 1 | Fine setting (programmable) | 1.78 |
| 2 | | 1.59 |
| 3 | | 1.42 |
| 4 | | 1.26 |
| 5 | | 1.12 |
| 6 | | 1.00 |

CLOCK INPUT

The ADS6425 clock inputs can be driven differentially (SINE, LVPECL or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors as shown in Figure 34. This allows using transformer-coupled drive circuits for sine wave clock or ac-coupling for LVPECL, LVDS clock sources (see Figure 35 and Figure 37).

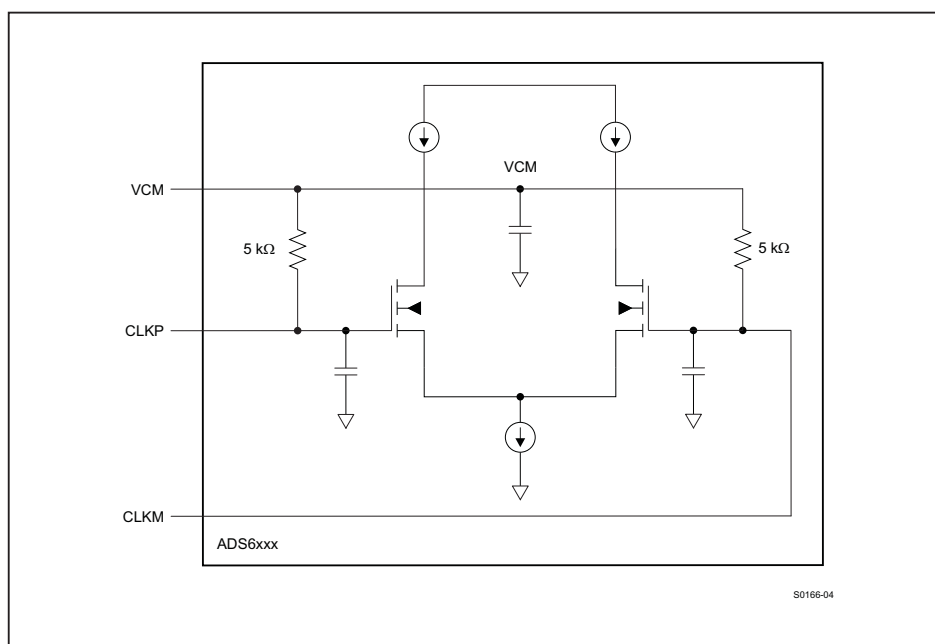


Figure 34. Internal Clock Buffer

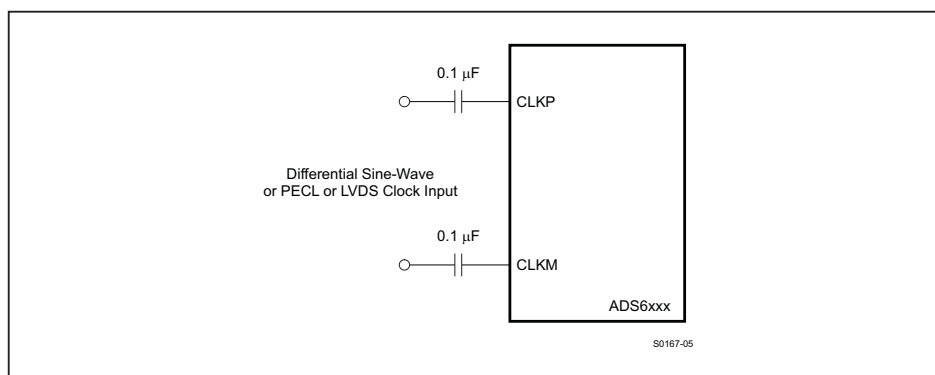


Figure 35. Differential Clock Driving Circuit

Figure 36 shows a typical scheme using PECL clock drive from a CDCM7005 clock driver. SNR performance with this scheme is comparable with that of a low jitter sine wave clock source.

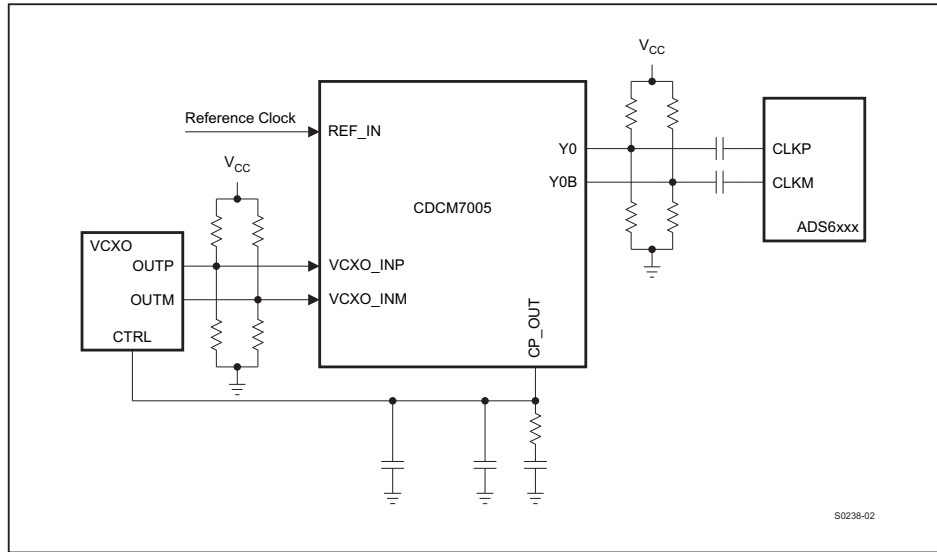


Figure 36. PECL Clock Drive Using CDCM7005

Single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM (pin) connected to ground with a 0.1-μF capacitor, as shown in Figure 37.

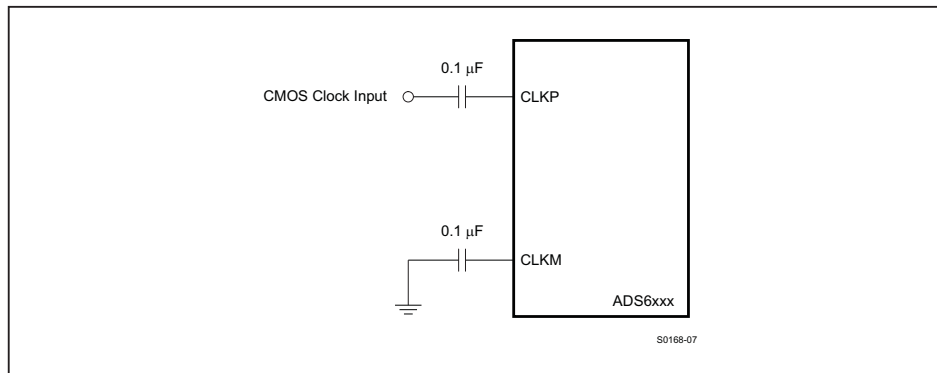


Figure 37. Single-Ended Clock Driving Circuit

For best performance, the clock inputs have to be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input.

CLOCK BUFFER GAIN

When using a sinusoidal clock input, the noise contributed by clock jitter improves as the clock amplitude is increased. Hence, it is recommended to use large clock amplitude. As shown by Figure 21, use clock amplitude greater than 1V pp to avoid performance degradation.

In addition, the clock buffer has programmable gain to amplify the input clock to support very low clock amplitude. The gain can be set by programming the register bits <CLKIN GAIN> (Table 12) and increases monotonically from Gain 0 to Gain 5 settings. Table 20 shows the minimum clock amplitude supported for each gain setting.

Table 20. Minimum Clock Amplitude Across Gains

| CLOCK BUFFER GAIN | MINIMUM CLOCK AMPLITUDE SUPPORTED, mV (pp differential) |
|-----------------------|---|
| Gain 0 (minimum gain) | 800 |
| Gain 1 (default gain) | 400 |
| Gain 2 | 300 |
| Gain 3 | 200 |
| Gain 4 | 150 |
| Gain 5 (highest gain) | 100 |

POWER DOWN MODES

The ADS6425 has three power down modes – global power down, channel standby and input clock stop.

Global Power Down

This is a global power down mode in which almost the entire chip is powered down, including the four ADCs, internal references, PLL and LVDS buffers. As a result, the total power dissipation falls to about 77 mW typical (with input clock running). This mode can be initiated by setting the register bit **<PDN GLOBAL>** (Table 11). The output data and clock buffers are in high impedance state.

The wake-up time from this mode to data becoming valid in normal mode is 100 μ s.

Channel Standby

In this mode, only the ADC of each channel is powered down and this helps to get very fast wake-up times. Each of the four ADCs can be powered down independently using the register bits **<PDN CH>** (Table 11). The analog power dissipation varies from 1115 mW (only one channel in standby) to 245 mW (all four channels in standby). The output LVDS buffers remain powered up.

The wake-up time from this mode to data becoming valid in normal mode is 200 clock cycles.

Input Clock Stop

The converter enters this mode:

- If the input clock frequency falls below 1 MSPS or
- If the input clock amplitude is less than 400 mV (pp, differential with default clock buffer gain setting) at any sampling frequency.

All ADCs and LVDS buffers are powered down and the power dissipation is about 235 mW. The wake-up time from this mode to data becoming valid in normal mode is 100 μ s.

Table 21. Power Down Modes Summary

| POWER DOWN MODE | AVDD POWER (mW) | LVDD POWER (mW) | WAKE UP TIME |
|-----------------------|-----------------|-----------------|--------------|
| In power-up | 1360 | 297 | – |
| Global power down | 65 | 12 | 100 μ s |
| 1 Channel in standby | 1115 | 297 | 200 Clocks |
| 2 Channels in standby | 825 | 297 | 200 Clocks |
| 3 Channels in standby | 532 | 297 | 200 Clocks |
| 4 Channels in standby | 245 | 297 | 200 Clocks |
| Input clock stop | 200 | 35 | 100 μ s |

POWER SUPPLY SEQUENCING

During power-up, the AVDD and LVDD supplies can come up in any sequence. The two supplies are separated inside the device. Externally, they can be driven from separate supplies or from a single supply.

DIGITAL OUTPUT INTERFACE

The ADS6425 offers several flexible output options making it easy to interface to an ASIC or an FPGA. These options can be easily programmed using either parallel pins and/or the serial interface.

The output interface options are:

- 1-wire, 1x frame clock, 12x and 14x serialization with DDR bit clock
- 2-wire, 1x frame clock, 12x serialization, with DDR and SDR bit clock, byte wise/bit wise/word wise
- 2-wire, 1x word clock, 14x serialization, with SDR bit clock, byte wise/bit wise/word wise
- 2-wire, (0.5 x) frame clock, 14x serialization, with DDR bit clock, byte wise/bit wise/word wise.

The maximum sampling frequency, bit clock frequency and output data rate will vary depending on the interface options selected (refer to Table 12).

Table 22. Maximum Recommended Sampling Frequency for Different Output Interface Options

| INTERFACE OPTIONS | | | MAXIMUM RECOMMENDED SAMPLING FREQUENCY, MSPS | BIT CLOCK FREQUENCY, MHZ | FRAME CLOCK FREQUENCY, MHZ | SERIAL DATA RATE, Mbps |
|-------------------|---------------|-------------------|--|--------------------------|----------------------------|------------------------|
| 1-Wire | DDR Bit clock | 12x Serialization | 65 | 390 | 65 | 780 |
| | | 14x Serialization | 65 | 455 | 65 | 910 |
| 2-Wire | DDR Bit clock | 12x Serialization | 125 | 375 | 125 | 750 |
| | | 14x Serialization | 125 | 437.5 | 62.5 | 875 |
| 2-Wire | SDR Bit clock | 12x Serialization | 65 | 390 | 65 | 390 |
| | | 14x Serialization | 65 | 455 | 65 | 455 |

Each interface option is described in detail below.

1-WIRE INTERFACE - 12x AND 14x SERIALIZATION WITH DDR BIT CLOCK

Here the device outputs the data of each ADC serially on a single LVDS pair (1-wire). The data is available at the rising and falling edges of the bit clock (DDR bit clock). The ADC outputs a new word at the rising edge of every frame clock, starting with the MSB. Optionally, it can also be programmed to output the LSB first. The data rate is 12 x Sample frequency (12x serialization) and 14 x Sample frequency (14x serialization).

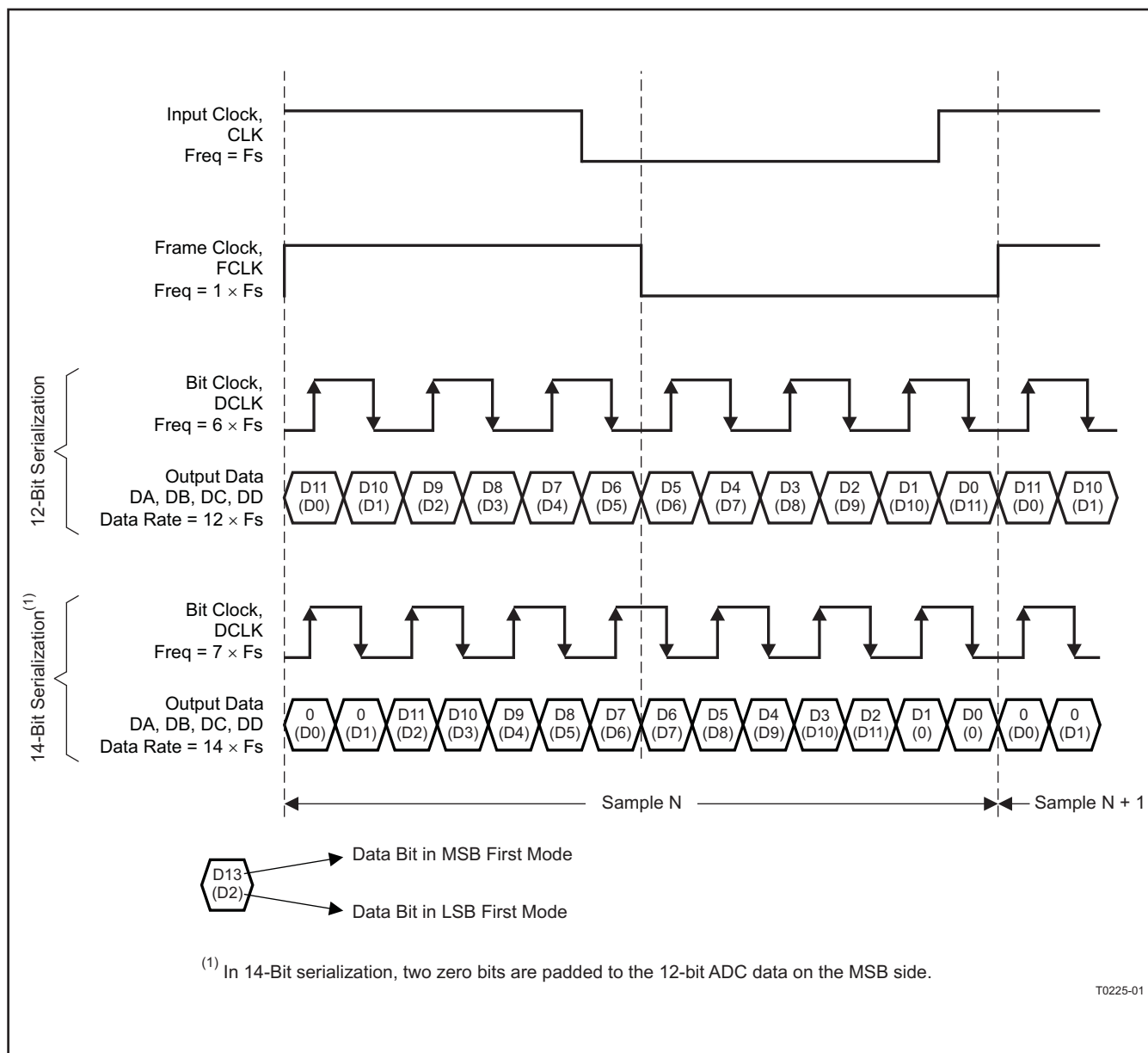
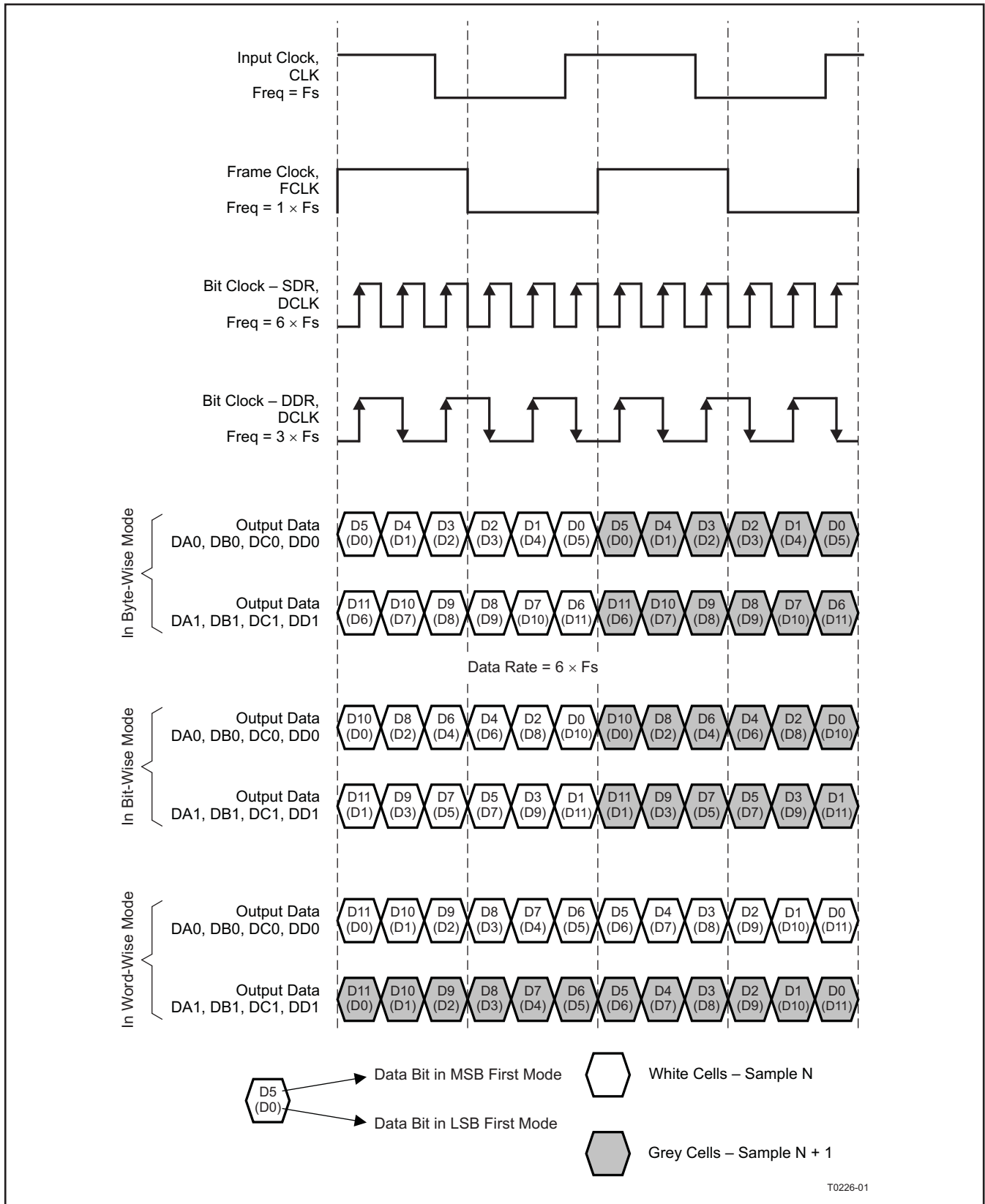


Figure 38. 1-Wire Interface

2-WIRE INTERFACE - 12x SERIALIZATION WITH DDR/SDR BIT CLOCK

The 2-wire interface is recommended for sampling frequencies above 65 MSPS. The device outputs the data of each ADC serially on two LVDS pairs (2-wire). The data rate is $6 \times$ Sample frequency since 6 bits are sent on each wire every clock cycle. The data is available along with DDR bit clock or optionally with SDR bit clock. Each ADC sample is sent over the 2 wires as byte-wise or bit-wise or word-wise.



A. In the byte-wise and bit-wise modes, the frame clock frequency is $1 \times F_s$. In the word-wise mode, the frame clock frequency is $0.5 \times F_s$.

Figure 39. 2-Wire Interface 12× Serialization

2-WIRE INTERFACE - 14× SERIALIZATION

In 14× serialization, two zero bits are padded to the 12-bit ADC data on the MSB side and the combined 14-bit data is serialized and output over two LVDS pairs. A frame clock at 1× sample frequency is also available with an SDR bit clock. With DDR bit clock option, the frame clock frequency is 0.5× sample frequency. The output data rate will be 7 × Sample frequency as 7 data bits are output every clock cycle on each wire. Each ADC sample is sent over the 2 wires as byte-wise or bit-wise or word-wise.

Using the 14× serialization makes it possible to upgrade to a 14-bit ADC in the 64xx family in the future seamlessly, without requiring any modification to the receiver capture logic design.

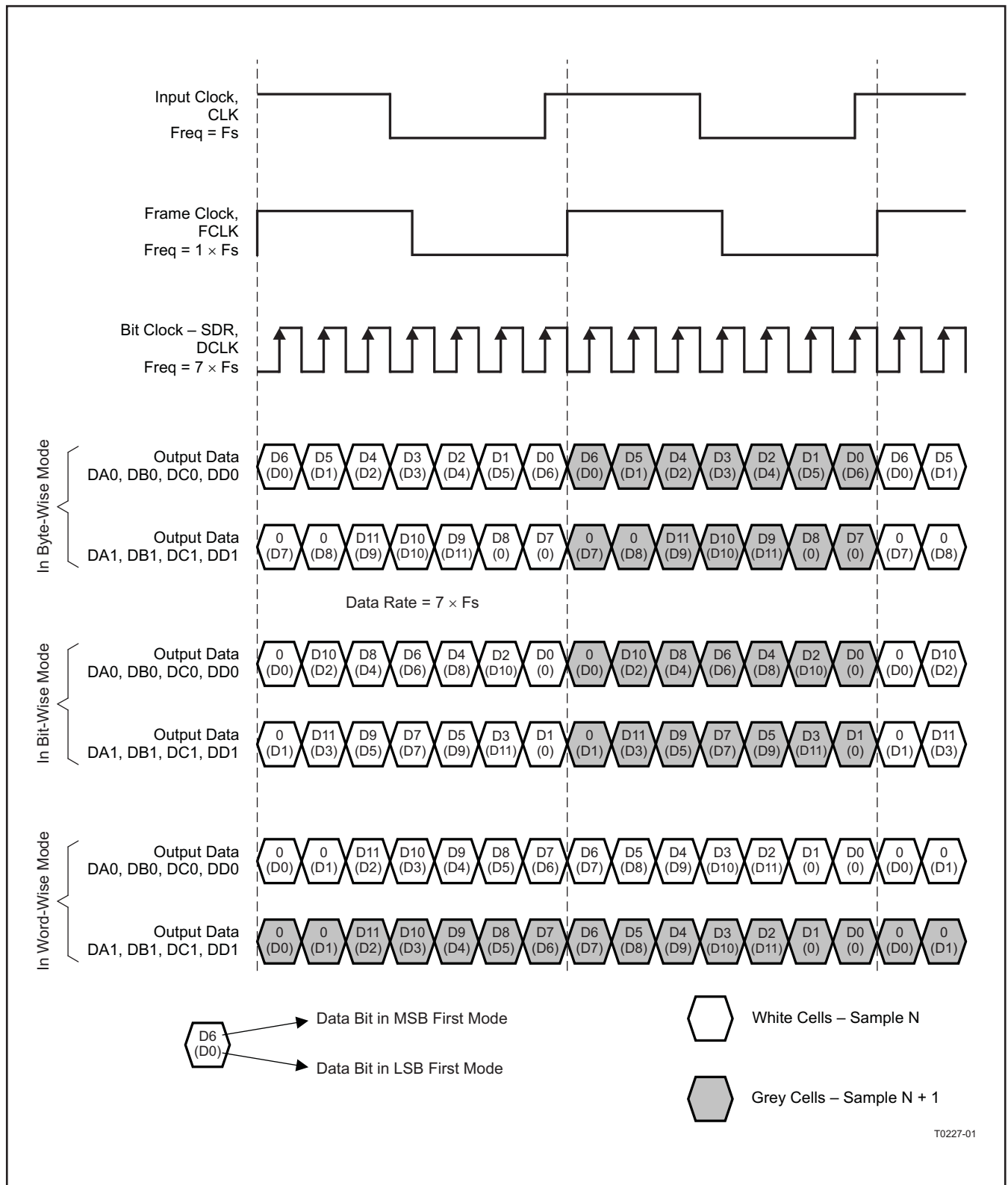


Figure 40. 2-Wire Interface 14x Serialization - SDR Bit Clock

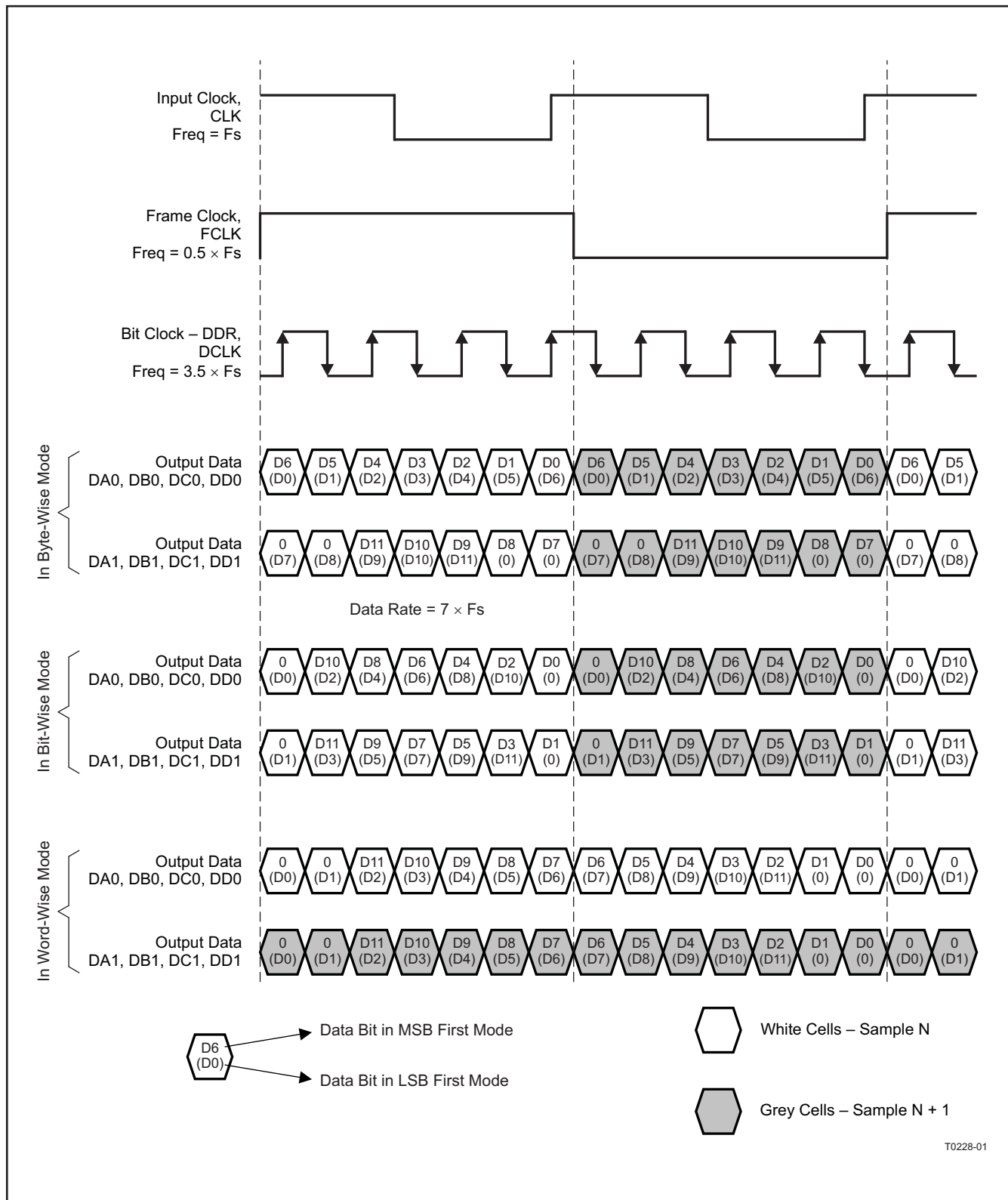


Figure 41. 2-Wire Interface 14x Serialization - DDR Bit Clock

OUTPUT BIT ORDER

In the 2-wire interface, three types of bit order are supported - byte-wise, bit-wise and word-wise.

Byte-wise: Each 12-bit sample is split across the 2 wires. Wires DA0, DB0, DC0 and DD0 carry the 6 LSB bits (D5-D0) and wires DA1, DB1, DC1 and DD1 carry the 6 MSB bits.

Bit-wise: Each 12-bit sample is split across the 2 wires. Wires DA0, DB0, DC0 and DD0 carry the 6 even bits (D0,D2,D4..) and wires DA1, DB1, DC1 and DD1 carry the 6 odd bits (D1,D3,D5...).

Word-wise: In this case, all 12-bits of a sample are sent over a single wire. Successive samples are sent over the 2 wires. For example sample N is sent on wires DA0, DB0, DC0 and DD0, while sample N+1 is sent over wires DA1, DB1, DC1 and DD1. The frame clock frequency is 0.5x sampling frequency, with the rising edge aligned with the start of each word.

MSB/LSB FIRST

By default after reset, the 12-bit ADC data is output serially with the MSB first (D11,D10,...D1,D0). The data can be output LSB first also by programming the register bit **<MSB_LSB_First>**. In the 2-wire mode, the bit order in each wire is flipped in the LSB first mode.

OUTPUT DATA FORMATS

Two output data formats are supported – 2s complement (default after reset) and offset binary. They can be selected using the serial interface register bit **<DF>**. In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 0xFFF in offset binary output format, and 0x7FF in 2s complement output format. For a negative input overdrive, the output code is 0x000 in offset binary output format and 0x800 in 2s complement output format.

LVDS CURRENT CONTROL

The default LVDS buffer current is 3.5 mA. With an external 100-Ω termination resistance, this develops ±350-mV logic levels at the receiver. The LVDS buffer currents can also be programmed to 2.5 mA, 3.0 mA and 4.5 mA using the register bits **<LVDS_CURR>**. In addition, there exists a current double mode, where the LVDS nominal current is doubled (register bits **<CURR_DOUBLE>**, [Table 17](#)).

LVDS INTERNAL TERMINATION

An internal termination option is available (using the serial interface), by which the LVDS buffers are differentially terminated inside the device. Five termination resistances are available – 166, 200, 250, 333, and 500 Ω (nominal with ±20% variation). Any combination of these terminations can be programmed; the effective termination will be the parallel combination of the selected resistances. The terminations can be programmed separately for the clock and data buffers (bits **<TERM_CLK>** and **<TERM_DATA>**, [Table 18](#)).

The internal termination helps to absorb any reflections from the receiver end, improving the signal integrity. This makes it possible to drive up to 10 pF of load capacitance, compared to only 5 pF without the internal termination. [Figure 42](#) and [Figure 43](#) show the eye diagram with 5 pF and 10 pF load capacitors (connected from each output pin to ground).

With 100-Ω internal and 100-Ω external termination, the voltage swing at the receiver end will be halved (compared to no internal termination). The voltage swing can be restored by using the LVDS current double mode (bits **<CURR_DOUBLE>**, [Table 17](#)).

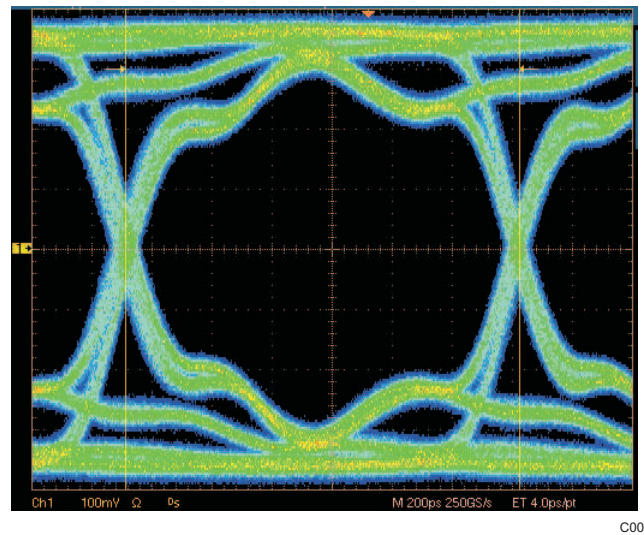


Figure 42. LVDS Data Eye Diagram with 5-pF Load Capacitance (No Internal Termination)

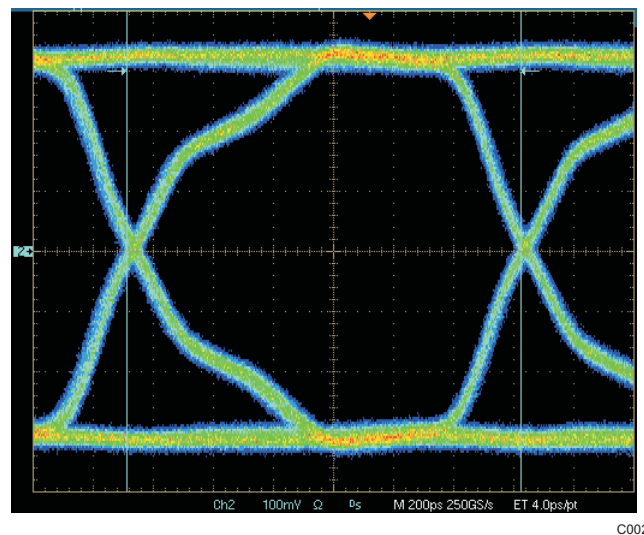


Figure 43. LVDS Data Eye Diagram with 10-pF Load Capacitance (100 Ω Internal Termination)

CAPTURE TEST PATTERNS

The ADS6425 outputs the bit clock (DCLK), positioned nearly at the center of the data transitions. It is recommended to route the bit clock, frame clock and output data lines with minimum relative skew on the PCB. This ensures sufficient setup/hold times for a reliable capture by the receiver.

The DESKEW is a 1010... or 0101... pattern output on the serial data lines that can be used to verify if the receiver capture clock edge is positioned correctly. This may be useful in case there is some skew between DCLK and serial data inside the receiver. Once deserialized, it is required to ensure that the parallel data is aligned to the frame boundary. The SYNC test pattern can be used for this. For example, in the 1-wire interface, the SYNC pattern is 6 '1's followed by 6 '0's (from MSB to LSB). This information can be used by the receiver logic to shift the deserialized data till it matches the SYNC pattern.

In addition to DESKEW and SYNC, the ADS6425 includes other test patterns to verify correctness of the capture by the receiver such as all zeros, all ones and toggle. These patterns are output on all four channel data lines simultaneously. Some patterns like custom and sync are affected by the type of interface selected, serialization and bit order.

Table 23. Test Patterns

| PATTERN | DESCRIPTION |
|-----------|--|
| All zeros | Outputs logic low. |
| All ones | Outputs logic high. |
| Toggle | Outputs toggle pattern - <D11-D0> alternates between 1010101010 and 0101010101 every clock cycle. |
| Custom | Outputs a 12-bit custom pattern. The 12-bit custom pattern can be specified into two serial interface registers. In the 2-wire interface, each code is sent over the 2 wires depending on the serialization and bit order. |
| Sync | Outputs a sync pattern. |
| Deskew | Outputs deskew pattern. Either <D11-D0> = 1010101010 OR <D11-D0> = 0101010101 every clock cycle. |

Table 24. SYNC Pattern

| INTERFACE OPTION | SERIALIZATION | SYNC PATTERN ON EACH WIRE |
|------------------|---------------|-------------------------------|
| 1-Wire | 12 X | MSB-111111000000-LSB |
| | 14 X | MSB-11111110000000-LSB |
| 2-Wire | 12 X | MSB-111000-LSB |
| | 14 X | MSB-1111000-LSB |

OUTPUT TIMINGS AT LOWER SAMPLING FREQUENCIES

Setup, hold and other timing parameters are specified across sampling frequencies and for each type of output interface in the tables below.

Table 26 to Table 29: Typical values are at 25°C, min and max values are across the full temperature range $T_{MIN} = -40^{\circ}C$ to $T_{MAX} = 85^{\circ}C$, $AVDD = LVDD = 3.3 V$, $C_L = 5 pF$, $I_O = 3.5 mA$, $R_L = 100 \Omega$, no internal termination, unless otherwise noted.

Timing parameters are ensured by design and characterization and not tested in production.

$T_s = 1 / \text{Sampling frequency} = 1/F_s$

Table 25. Clock Propagation Delay and Serializer Latency for Different Interface Options

| INTERFACE | SERIALIZATION | CLOCK PROPAGATION DELAY, t_{pd_clk} | SERIALIZER LATENCY ⁽¹⁾ clock cycles |
|---------------------------|---------------|--|---|
| 1-Wire with DDR bit clock | 12X | $t_{pd_clk} = 0.5xT_s + t_{delay}$ | 0 |
| | 14X | $t_{pd_clk} = 0.428xT_s + t_{delay}$ | |
| 2-Wire with DDR bit clock | 12X | $t_{pd_clk} = t_{delay}$ | 1 |
| 2-Wire with SDR bit clock | | $t_{pd_clk} = 0.5xT_s + t_{delay}$ | 0 |
| 2-Wire with DDR bit clock | 14X | $t_{pd_clk} = 0.857xT_s + t_{delay}$ | 2 (when $t_{pd_clk} \geq T_s$) |
| 2-Wire with SDR bit clock | | | 1 (when $t_{pd_clk} < T_s$) |
| 2-Wire with SDR bit clock | | $t_{pd_clk} = 0.428xT_s + t_{delay}$ | 0 |

(1) Note that the total latency = ADC latency + serializer latency. The ADC latency is 12 clocks.

Table 26. Timings for 1-Wire Interface

| SERIALIZATION | SAMPLING FREQUENCY MSPS | DATA SETUP TIME, t_{su} ns | | | DATA HOLD TIME, t_h ns | | | t_{delay} ns | | |
|---------------|-------------------------------|---------------------------------|------|-----|-----------------------------|-----|-----|----------------------------|-----|-----|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |
| 12x | 65 | 0.4 | 0.6 | | 0.5 | 0.7 | | $F_s \geq 40 \text{ MSPS}$ | | |
| | 40 | 0.8 | 1.0 | | 0.9 | 1.1 | | 3 | 4 | 5 |
| | 20 | 1.6 | 2.0 | | 1.8 | 2.2 | | $F_s < 40 \text{ MSPS}$ | | |
| | 10 | 3.5 | 4.0 | | 3.5 | 4.2 | | 3 | 4.5 | 6 |
| 14x | 65 | 0.3 | 0.5 | | 0.4 | 0.6 | | $F_s \geq 40 \text{ MSPS}$ | | |
| | 40 | 0.65 | 0.85 | | 0.7 | 0.9 | | 3 | 4 | 5 |
| | 20 | 1.3 | 1.65 | | 1.6 | 1.9 | | $F_s < 40 \text{ MSPS}$ | | |
| | 10 | 3.2 | 3.5 | | 3.2 | 3.6 | | 3 | 4.5 | 6 |

Table 27. Timings for 2-Wire Interface, DDR Bit Clock

| SERIALIZATION | SAMPLING FREQUENCY MSPS | DATA SETUP TIME, t_{su} ns | | | DATA HOLD TIME, t_h ns | | | t_{delay} ns | | |
|---------------|-------------------------------|---------------------------------|------|-----|-----------------------------|------|-----|----------------------------|-----|-----|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |
| 12x | 105 | 0.55 | 0.75 | | 0.6 | 0.8 | | $F_s \geq 45 \text{ MSPS}$ | | |
| | 92 | 0.65 | 0.85 | | 0.7 | 0.9 | | 3.4 | 4.4 | 5.4 |
| | 80 | 0.8 | 1.0 | | 0.8 | 1.05 | | $F_s < 45 \text{ MSPS}$ | | |
| | 40 | 1.7 | 2.0 | | 1.1 | 2.1 | | 3.7 | 5.2 | 6.7 |
| 14x | 105 | 0.45 | 0.65 | | 0.5 | 0.7 | | $F_s \geq 45 \text{ MSPS}$ | | |
| | 92 | 0.55 | 0.75 | | 0.6 | 0.8 | | 3 | 4 | 5 |
| | 80 | 0.65 | 0.85 | | 0.7 | 0.9 | | $F_s < 45 \text{ MSPS}$ | | |
| | 65 | 0.8 | 1.1 | | 0.8 | 1.1 | | $F_s < 45 \text{ MSPS}$ | | |
| | 40 | 1.4 | 1.7 | | 1.5 | 1.9 | | 3 | 4.5 | 6 |

Table 28. Timings for 2-Wire Interface, SDR Bit Clock

| SERIALIZATION | SAMPLING FREQUENCY MSPS | DATA SETUP TIME, t_{su} ns | | | DATA HOLD TIME, t_h ns | | | t_{delay} ns | | |
|---------------|----------------------------|---------------------------------|-----|-----|-----------------------------|-----|-----|-------------------|--------------------|-----|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |
| 12x | 65 | 1.0 | 1.2 | | 1.1 | 1.3 | | 3.4 | $F_s \geq 40$ MSPS | |
| | 40 | 1.8 | 2.0 | | 1.9 | 2.1 | | | 4.4 | 5.4 |
| | 20 | 3.9 | 4.1 | | 3.8 | 4.1 | | $F_s < 40$ MSPS | | |
| | 10 | 8.2 | 8.4 | | 7.8 | 8.2 | | 3.7 | 5.2 | 6.7 |
| 14x | 65 | 0.8 | 1.0 | | 1.0 | 1.2 | | 3.4 | $F_s \geq 40$ MSPS | |
| | 40 | 1.5 | 1.7 | | 1.6 | 1.8 | | | 4.4 | 5.4 |
| | 20 | 3.4 | 3.6 | | 3.3 | 3.5 | | $F_s < 40$ MSPS | | |
| | 10 | 6.9 | 7.2 | | 6.6 | 6.9 | | 3.7 | 5.2 | 6.7 |

Table 29. Output Jitter (applies to all interface options)

| SAMPLING FREQUENCY MSPS | BIT CLOCK JITTER, CYCLE-CYCLE ps, peak-peak | | | FRAME CLOCK JITTER, CYCLE-CYCLE ps, peak-peak | | |
|----------------------------|--|-----|-----|--|-----|-----|
| | MIN | TYP | MAX | MIN | TYP | MAX |
| ≥ 65 | | 350 | | | 75 | |

DEFINITION OF SPECIFICATIONS

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

Offset Error – The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX} . It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX}-T_{MIN}$.

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at DC and the first nine harmonics.

$$SNR = 10\text{Log}_{10} \frac{P_S}{P_N} \quad (3)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10\text{Log}_{10} \frac{P_S}{P_N + P_D} \quad (4)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB) – The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (5)$$

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$THD = 10\text{Log}_{10} \frac{P_S}{P_D} \quad (6)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion – IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1-f_2$ or $2f_2-f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

DC Power Supply Rejection Ratio (DC PSRR) – The DC PSRR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

AC Power Supply Rejection Ratio (AC PSRR) – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{sup} is the change in supply voltage and ΔV_{out} is the resultant change of the ADC output code (referred to the input), then

$$PSRR = 20\text{Log}_{10} \frac{\Delta V_{out}}{\Delta V_{sup}}, \text{ expressed in dBc} \quad (7)$$

Voltage Overload Recovery – The number of clock cycles taken to recover to less than 1% error for a 6 dB overload on the analog inputs. A 6 dBFS sine wave input at Nyquist frequency is used as the test stimulus.

Common Mode Rejection Ratio (CMRR) – CMRR is the measure of rejection of variations in the analog input common-mode by the ADC. If ΔV_{cm_in} is the change in the common-mode voltage of the input pins and ΔV_{out} is the resultant change of the ADC output code (referred to the input), then

$$CMRR = 20\text{Log}_{10} \frac{\Delta V_{out}}{\Delta V_{cm_in}}, \text{ expressed in dBc} \quad (8)$$

| Changes from Revision A (October 2007) to Revision B | Page |
|--|-------------|
| • Added Frame setup time to timing specifications | 7 |
| • Added Frame hold time to timing specifications | 7 |
| • Changed Figure 2 | 8 |
| • Added (with 10% tolerance resistors) to USING PARALLEL INTERFACE CONTROL ONLY section..... | 9 |
| • Changed Figure 3 | 10 |
| • Added voltage values to Table 6 | 11 |
| • Added voltage values to Table 7 | 11 |
| • Added voltage values to Table 9 | 12 |
| • Added note to Table 10 | 15 |
| • Added 32K point FFT to typical characteristics conditions | 25 |
| • Added 32K point FFT to typical characteristics conditions | 26 |
| • Added 32K point FFT to typical characteristics conditions | 27 |
| • Added 32K point FFT to typical characteristics conditions | 28 |
| • Added 32K point FFT to typical characteristics conditions | 29 |
| • Added 32K point FFT to typical characteristics conditions | 30 |
| • Changed Gain 4 to Gain 5 in CLOCK BUFFER GAIN section..... | 36 |
| • Added Gain 5 to Table 20 | 37 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| ADS6425IRGCT | ACTIVE | VQFN | RGC | 64 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ6425 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

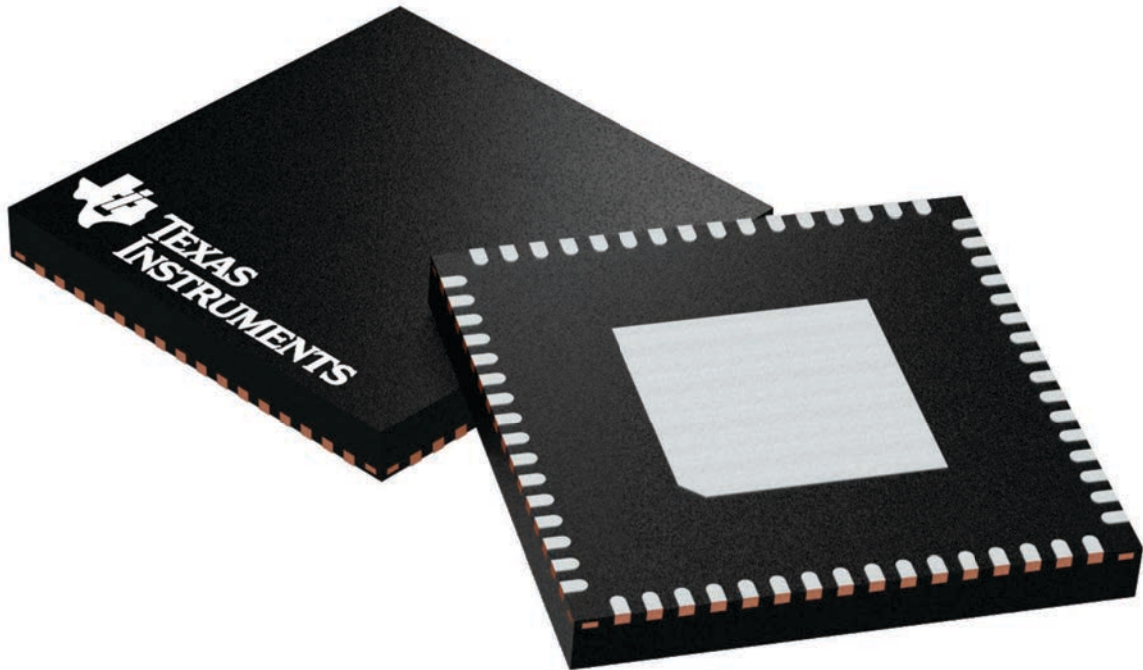
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

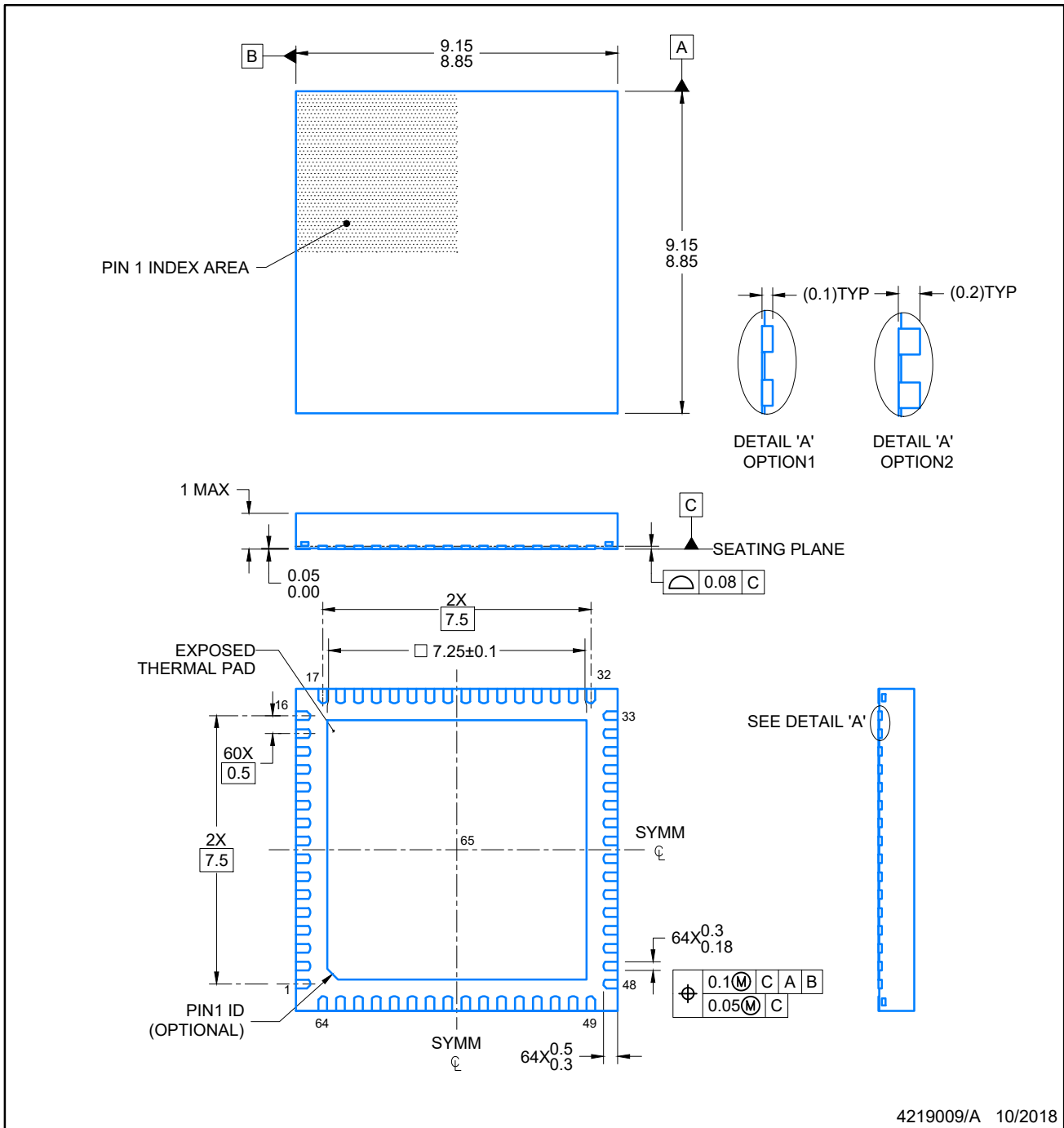
9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



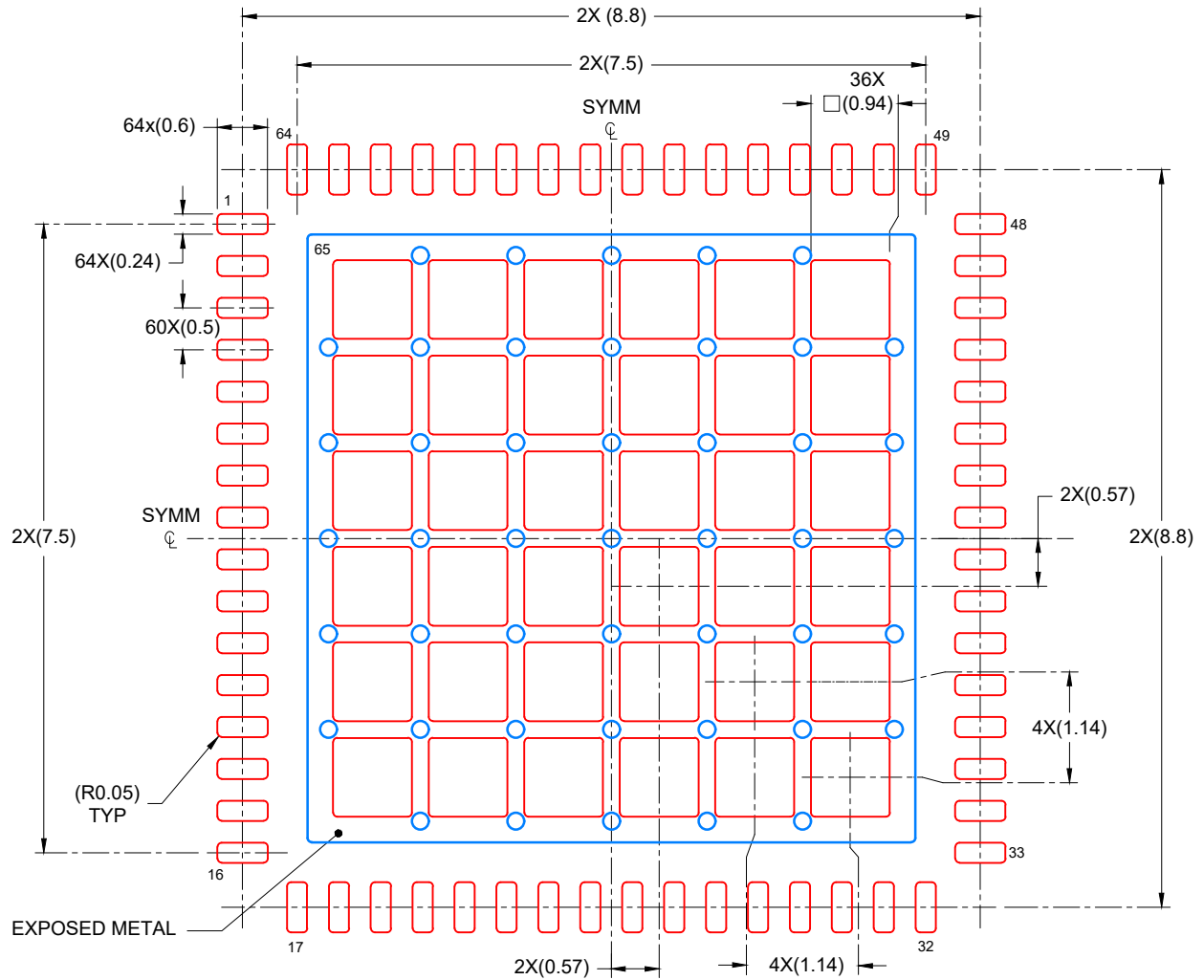
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224597/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 60% PRINTED COVERAGE BY AREA
 SCALE: 12X

4219009/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated