LM22673/-Q1 42V、3A SIMPLE SWITCHER® 特性 降压稳压器

1 特性

- 宽输入电压范围：4.5V 至 42V
- 内部补偿电压模式控制
- 在使用低等效串联电阻 (ESR) 陶瓷电容器时保持稳定
- 120mΩ N 通道金属氧化物半导体场效应晶体管 (MOSFET) PFM 封装
- 100mΩ N 通道 MOSFET 小外形尺寸 (SO) PowerPAD 封装
- 输出电压选项：
  -ADJ（输出电压最低为 1.285V）
  -5.0（输出电压固定为 5V）
- ±1.5% 反馈基准精度
- 开关频率为 500kHz
- –40°C 至 125°C 的运行结温范围
- 可调节软启动
- 可调节限流
- 集成引导加载二极管
- 完全 Webench®启用
- LM22673-Q1 是一款汽车级产品，符合 AEC-Q100 1 级标准（运行结温范围为 –40°C 至 +125°C）
- SO PowerPAD（外露垫）
- PFM（外露垫）

2 应用

- 工业控制
- 电信和数据通信系统
- 嵌入式系统
- 转换自 24V、12V 和 5V 标准输入电源轨

3 说明

LM22673 开关稳压器使用最少的外部组件来提供执行高效高压降压稳压器所需的全部功能。 这款稳压器易于使用，且集成了一个 42V N 沟道金属氧化物半导体场效应晶体管 (MOSFET) 开关，可提供高达 3A 的负载电流。 并且特有出色的线路和负载调节以及高效率 (> 90%)。 电压模式控制提供较短的最小接通时间，从而实现了输入和输出电压间的最宽比率。 内部环路补偿意味着用户无需承担计算环路补偿组件的枯燥工作。 这款稳压器提供 5V 固定输出和可调输出电压两种选项。 500kHz 的开关频率使得小型外部组件的使用成为可能并可实现良好的瞬态响应。 通过选择一个单个外部电容器可提供一个可调软启动特性。 此外，使用一个单个外部电阻器可在 200kHz 至 1MHz 的范围内对频率进行调节。 LM22673 器件还内置有热关断和限流功能，可防止器件发生意外过载。

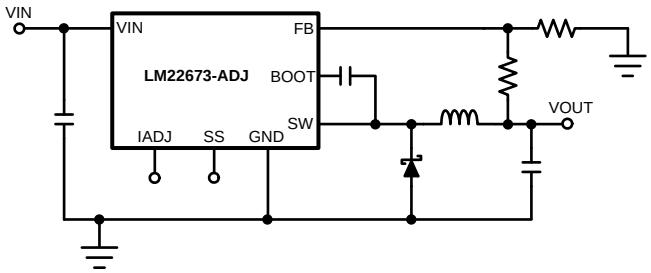
LM22673 器件是德州仪器 (TI) 的成员 SIMPLE SWITCHER® 系列产品。 SIMPLE SWITCHER® 概念使用最少量的外部组件和德州仪器 (TI) WEBENCH® 设计工具提供一套易于使用的完整设计。 为了简化设计，TI 的 WEBENCH® 工具包含诸如外部组件计算、电气模拟、散热模拟以及内置电路板等特性。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LM22673，LM22673-Q1	HSOP (8)	4.89mm x 3.90mm
	TO-263	10.16mm x 9.85mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化应用电路原理图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

Changes from Revision N (April 2013) to Revision O **Page**

- 已添加 *引脚配置和功能部分，处理额定值表，热性能信息表，特性描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分* ... 1
- Deleted *Inverting Regulator Application* ... 13

Changes from Revision M (April 2013) to Revision N **Page**

- 已更改 国家格式至 TI 格式 ... 1

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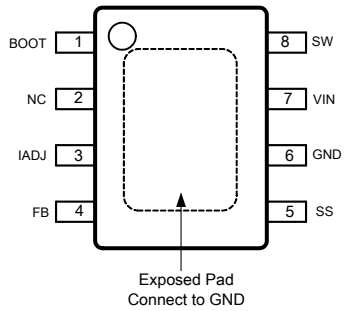
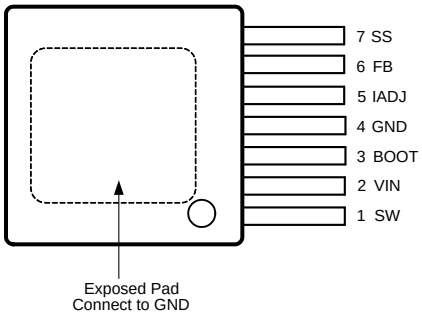
5 Pin Configuration and Functions

8-Pin
HSOP
Top View



7-Pin
PFM
Top View



Pin Functions

PIN			TYPE	DESCRIPTION	APPLICATION INFORMATION
NAME	SO PowerPAD	PFM			
BOOT	1	3	I	Bootstrap input	Provides the gate voltage for the high side NFET.
NC	2	—	—	Not Connected	Pin is not electrically connected inside the chip. Pin does function as thermal conductor.
IADJ	3	5	I	Current limit adjust input pin	A resistor attached between this pin and GND can be used to set the current limit threshold. Pin can be left floating and internal setting will be default.
FB	4	6	I	Feedback input	Feedback input to regulator.
SS	5	7		Soft-Start pin	Used to increase soft-start time. See *Soft-Start* section of data sheet.
GND	6	4	—	Ground input to regulator; system common	System ground pin.
VIN	7	2	I	Input voltage	Supply input to the regulator.
SW	8	1	O	Switch output	Switching output of regulator.
EP	EP	EP	—	Exposed Pad	Connect to ground. Provides thermal connection to PCB. See *Thermal Considerations*.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VIN to GND		43	V
SS, IADJ Pin Voltage	–0.5	7	V
SW to GND(1)	–5	V_{IN}	V
Boot Pin Voltage		V_{SW} + 7	V
FB Pin Voltage	–0.5	7	V
Power Dissipation	Internally Limited		
Junction Temperature		150	°C
For soldering specifications, refer to Application Report *Absolute Maximum Ratings for Soldering* (SNOA549).			

(1) The absolute maximum specification of the 'SW to GND' applies to dc voltage. An extended negative voltage limit of –10 V applies to a pulse of up to 50 ns.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2	2	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Handling Ratings: LM22673-Q1

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	–2	2	kV

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Supply Voltage	4.5	42	V
	Junction Temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC(1)		LM22673		UNIT
		DDA	NDR	
		8 PINS	7 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60	22	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

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6.6 Electrical Characteristics

Typical values represent the most likely parametric norm at $T_A = T_J = 25°C$, and are provided for reference purposes only. Unless otherwise specified: $V_{IN} = 12$ V.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
LM22673-5.0						
V_{FB}	Feedback Voltage	V_{IN} = 8 V to 42 V	4.925	5.0	5.075	V
		V_{IN} = 8 V to 42 V, –40°C ≤ T_J ≤ 125°C	4.9		5.1	
LM22673-ADJ						
V_{FB}	Feedback Voltage	V_{IN} = 4.7 V to 42 V	1.266	1.285	1.304	V
		V_{IN} = 4.7 V to 42 V, –40°C ≤ T_J ≤ 125°C	1.259		1.311	
ALL OUTPUT VOLTAGE VERSIONS						
I_Q	Quiescent Current	V_{FB} = 5 V		3.4		mA
		V_{FB} = 5 V, –40°C ≤ T_J ≤ 125°C			6	
V_{ADJ}	Current Limit Adjust Voltage			0.8		V
		–40°C ≤ T_J ≤ 125°C	0.65		0.9	
I_{CL}	Current Limit		3.4	4.2	5.3	A
		–40°C ≤ T_J ≤ 125°C	3.35		5.5	
$R_{DS(ON)}$	Switch On-Resistance	PFM Package		0.12	0.16	Ω
		PFM Package, –40°C ≤ T_J ≤ 125°C			0.22	
		SO PowerPAD Package		0.10	0.16	
		SO PowerPAD Package, –40°C ≤ T_J ≤ 125°C			0.20	
f_O	Oscillator Frequency			500		kHz
		–40°C ≤ T_J ≤ 125°C	400		600	
T_{OFFMIN}	Minimum Off-time			200		ns
		–40°C ≤ T_J ≤ 125°C	100		300	
T_{ONMIN}	Minimum On-time			100		ns
I_{BIAS}	Feedback Bias Current	V_{FB} = 1.3 V (ADJ Version Only)		230		nA
I_{SS}	Soft-start Current	EN Input = 0 V		50		µA
		EN Input = 0 V, –40°C ≤ T_J ≤ 125°C	30		70	
T_{SD}	Thermal Shutdown Threshold			150		°C

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Typical values represent most likely parametric norms at the conditions specified and are not ensured.

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6.7 Typical Characteristics

V_{in} = 12 V, T_J = 25°C (unless otherwise specified)

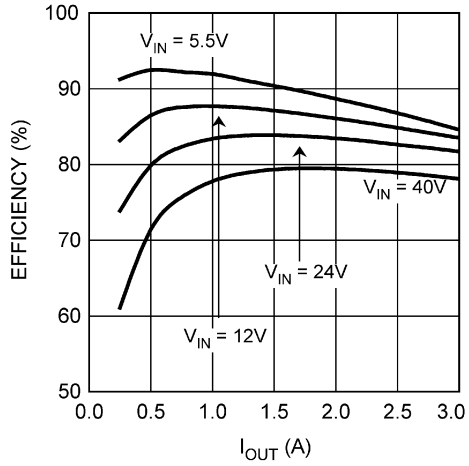

Figure 1. Efficiency vs I_{OUT} and V_{IN} V_{OUT} = 3.3 V

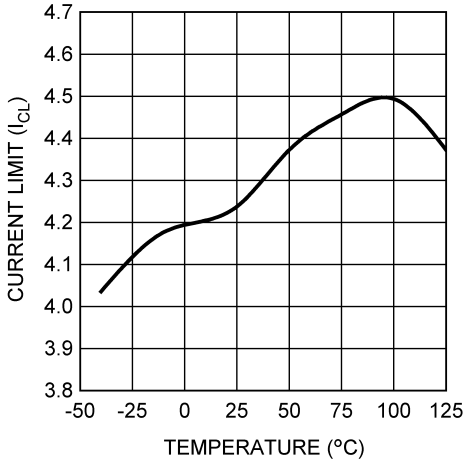

Figure 2. Current Limit vs Temperature

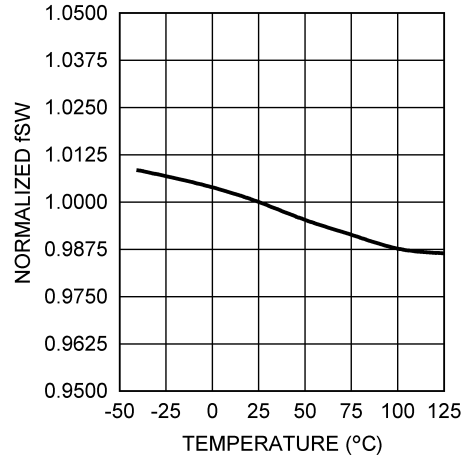

Figure 3. Normalized Switching Frequency vs Temperature

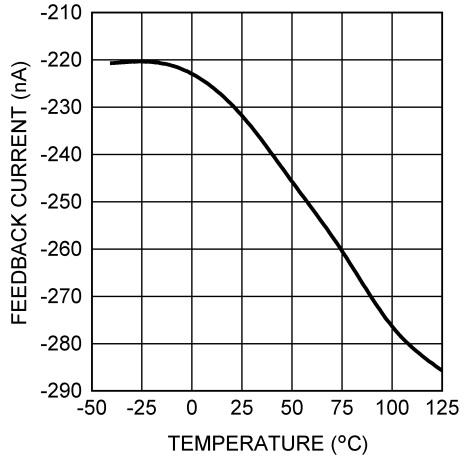

Figure 4. Feedback Bias Current vs Temperature

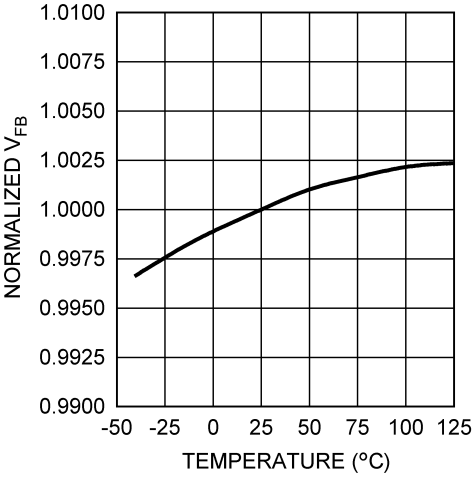

Figure 5. Normalized Feedback Voltage vs Temperature

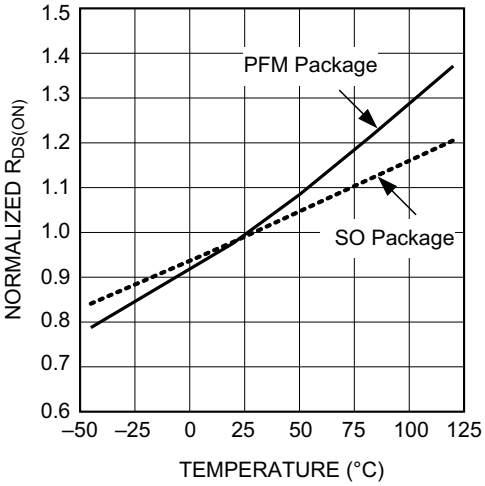

Figure 6. Normalized $R_{DS(ON)}$ vs Temperature

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Typical Characteristics (continued)

V_{in} = 12 V, T_J = 25°C (unless otherwise specified)

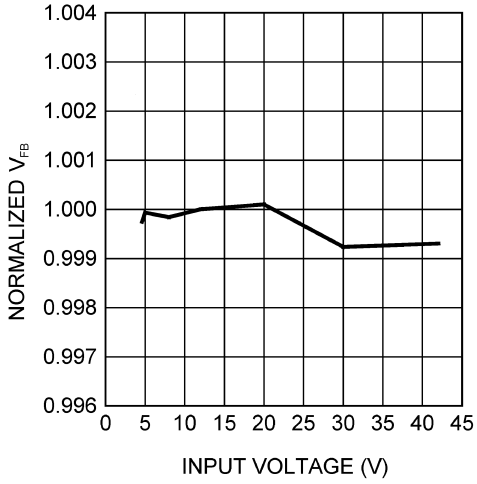

Figure 7. Normalized Feedback Voltage vs Input Voltage

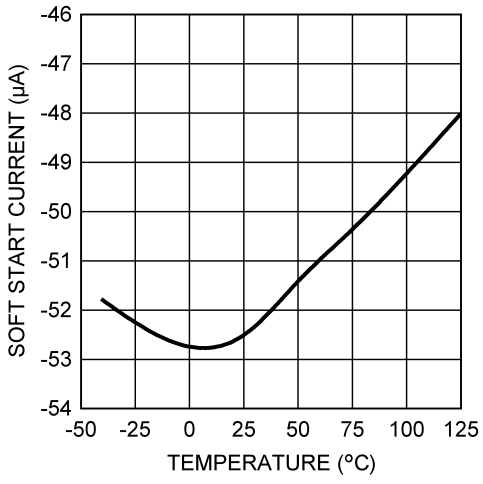

Figure 8. Soft-Start Current vs Temperature

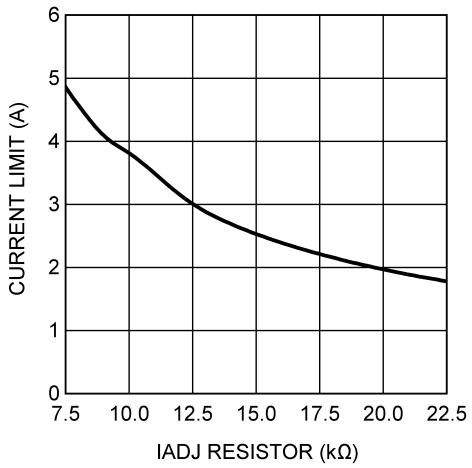

Figure 9. Current Limit vs IADJ Resistor

7 Detailed Description

7.1 Overview

The LM22673 device incorporates a voltage mode constant frequency PWM architecture. In addition, input voltage feedforward is used to stabilize the loop gain against variations in input voltage. This allows the loop compensation to be optimized for transient performance. The power MOSFET, in conjunction with the diode, produce a rectangular waveform at the switch pin, that swings from about zero volts to VIN. The inductor and output capacitor average this waveform to become the regulator output voltage. By adjusting the duty cycle of this waveform, the output voltage can be controlled. The error amplifier compares the output voltage with the internal reference and adjusts the duty cycle to regulate the output at the desired value.

The internal loop compensation of the -ADJ option is optimized for outputs of 5V and below. If an output voltage of 5V or greater is required, the -5.0 option can be used with an external voltage divider. The minimum output voltage is equal to the reference voltage, that is, 1.285 V (typ).

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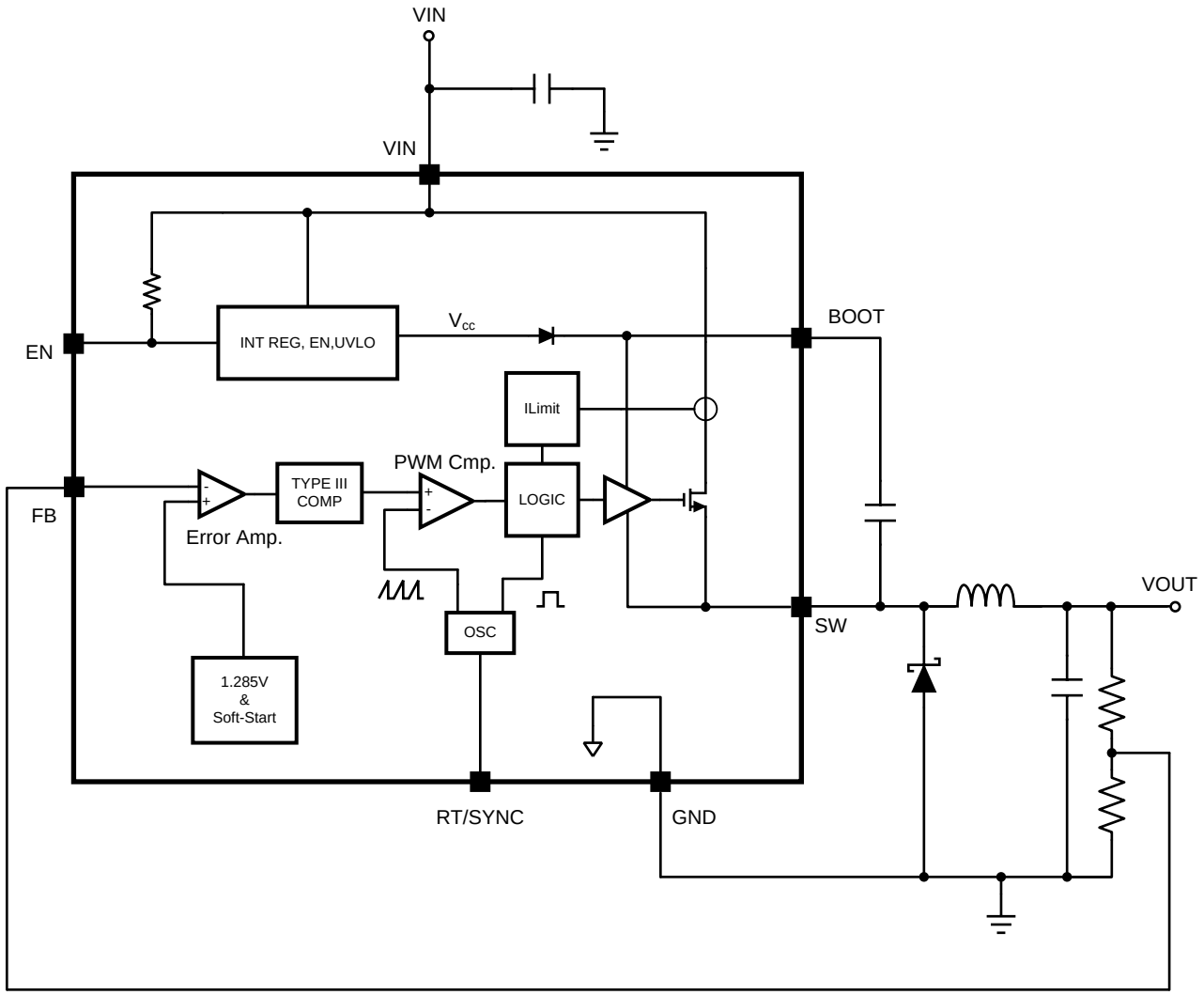
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 UVLO

The LM22673 also incorporates an input undervoltage lock-out (UVLO) feature. This prevents the regulator from turning on when the input voltage is not great enough to properly bias the internal circuitry. The rising threshold is 4.3 V (typ) while the falling threshold is 3.9 V (typ).

7.3.2 Soft-Start

The soft-start feature allows the regulator to gradually reach steady-state operation, thus reducing start-up stresses. The internal soft-start feature brings the output voltage up in about 500 µs. This time can be extended by using an external capacitor connected to the SS pin. Values in the range of 100 nF to 1 µF are recommended. The approximate soft-start time can be estimated from Equation 1.

$$T_{SS} \approx 26 \times 10^{3} \cdot C_{SS} \quad (1)$$

Soft-start is reset any time the part is shut down or a thermal overload event occurs.

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Feature Description (continued)

7.3.3 Boot-Strap Supply

The LM22673 incorporates a floating high-side gate driver to control the power MOSFET. The supply for this driver is the external boot-strap capacitor connected between the BOOT pin and SW. A good quality 10 nF ceramic capacitor must be connected to these pins with short, wide PCB traces. One reason the regulator imposes a minimum off-time is to ensure that this capacitor recharges every switching cycle. A minimum load of about 5 mA is required to fully recharge the boot-strap capacitor in the minimum off-time. Some of this load can be provided by the output voltage divider, if used.

7.3.4 Internal Compensation

The LM22673 has internal loop compensation designed to provide a stable regulator over a wide range of external power stage components. The internal compensation of the -ADJ option is optimized for output voltages below 5 V. If an output voltage of 5 V or greater is needed, the -5.0 option with an external resistor divider can be used.

Ensuring stability of a design with a specific power stage (inductor and output capacitor) can be tricky. The LM22673 stability can be verified using the WEBENCH Designer online circuit simulation tool. A quick start spreadsheet can also be downloaded from the online product folder.

The complete transfer function for the regulator loop is found by combining the compensation and power stage transfer functions. The LM22673 has internal type III loop compensation, as detailed in Figure 10. This is the approximate "straight line" function from the FB pin to the input of the PWM modulator. The power stage transfer function consists of a dc gain and a second order pole created by the inductor and output capacitor(s). Due to the input voltage feedforward employed in the LM22673, the power stage dc gain is fixed at 20 dB. The second order pole is characterized by its resonant frequency and its quality factor (Q). For a first pass design, the product of inductance and output capacitance should conform to Equation 2.

$$L \cdot C_{out} \approx 1.1 \times 10^{-9} \tag{2}$$

Alternatively, this pole should be placed between 1.5 kHz and 15 kHz and is given by Equation 3.

$$F_o = \frac{1}{2\pi \cdot \sqrt{L \cdot C_{out}}} \tag{3}$$

The Q factor depends on the parasitic resistance of the power stage components and is not typically in the control of the designer. Of course, loop compensation is only one consideration when selecting power stage components (see the *Applications and Implementation* section for more details).

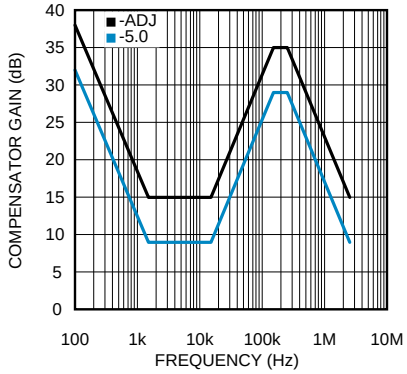

Figure 10. Compensator Gain

In general, hand calculations or simulations can only aid in selecting good power stage components. Good design practice dictates that load and line transient testing should be done to verify the stability of the application. Also, Bode plot measurements should be made to determine stability margins. *AN-1889 How to Measure the Loop Transfer Function of Power Supplies* (SNVA364) shows how to perform a loop transfer function measurement with only an oscilloscope and function generator.

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7.4 Device Functional Modes

7.4.1 Current Limit

The LM22673 has current limiting to prevent the switch current from exceeding safe values during an accidental overload on the output. This peak current limit is found in the *Electrical Characteristics* table under the heading of I_{CL}. The maximum load current that can be provided, before current limit is reached, is determined from Equation 4.

$$I_{out}|_{max} \approx I_{CL} - \frac{(V_{in} - V_{out})}{2 \cdot L \cdot F_{sw}} \cdot \frac{V_{out}}{V_{in}} \quad (4)$$

Where:

L is the value of the power inductor.

When the LM22673 enters current limit, the output voltage will drop and the peak inductor current will be fixed at I_{CL} at the end of each cycle. The switching frequency will remain constant while the duty cycle drops. The load current will not remain constant, but will depend on the severity of the overload and the output voltage.

For very severe overloads ("short-circuit"), the regulator changes to a low frequency current foldback mode of operation. The frequency foldback is about 1/5 of the nominal switching frequency. This will occur when the current limit trips before the minimum on-time has elapsed. This mode of operation is used to prevent inductor current "run-away", and is associated with very low output voltages when in overload. Equation 5 can be used to determine what level of output voltage will cause the part to change to low frequency current foldback.

$$V_x \leq V_{in} \cdot F_{sw} \cdot T_{on} \cdot 1.8 \quad (5)$$

Where:

F_{sw} is the normal switching frequency.

V_{in} is the maximum for the application.

If the overload drives the output voltage to less than or equal to V_x, the part will enter current foldback mode. If a given application can drive the output voltage to ≤ V_x, during an overload, then a second criterion must be checked. Equation 6 gives the maximum input voltage, when in this mode, before damage occurs.

$$V_{in} \leq \frac{V_{sc} + 0.4}{T_{on} \cdot F_{sw} \cdot 0.36} \quad (6)$$

Where:

V_{sc} is the value of output voltage during the overload.

f_{sw} is the normal switching frequency.

NOTE

If the input voltage should exceed this value, while in foldback mode, the regulator and/or the diode may be damaged.

It is important to note that the voltages in Equation 4 through Equation 6 are measured at the inductor. Normal trace and wiring resistance will cause the voltage at the inductor to be higher than that at a remote load. Therefore, even if the load is shorted with zero volts across its terminals, the inductor will still see a finite voltage. It is this value that should be used for V_x and V_{sc} in the calculations. In order to return from foldback mode, the load must be reduced to a value much lower than that required to initiate foldback. This load "hysteresis" is a normal aspect of any type of current limit foldback associated with voltage regulators.

The safe operating area, when in short circuit mode, is shown in Figure 11. Operating points below and to the right of the curve represent safe operation.

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Device Functional Modes (continued)

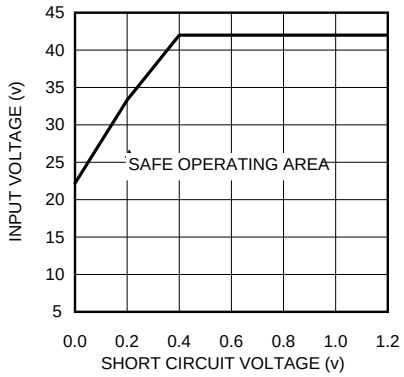

Figure 11. SOA

7.4.2 Current-Limit Adjustment

A key feature of the LM22673 is the ability to adjust the peak switch current limit. This can be useful when the full current capability of the regulator is not required for a given application. A smaller current limit may allow the use of power components with lower current ratings, thus saving space and reducing cost. A single resistor between the IADJ pin and ground controls the current limit in accordance with Figure 12. The current limit mode is set during start-up of the regulator. When V_{IN} is applied, a weak pullup is connected to the IADJ pin and, after approximately 100 µs, the voltage on the pin is checked against a threshold of about 0.8V. With the IADJ pin open, the voltage floats above this threshold, and the current limit is set to the default value of 4.2A (typ). With a resistor present, an internal reference holds the pin voltage at 0.8 V; the resulting current sets the current limit. The accuracy of the adjusted current limit will be slightly worse than that of the default value, that is, +35% / –25% is to be expected. Resistor values should not exceed the limits shown in Figure 12.

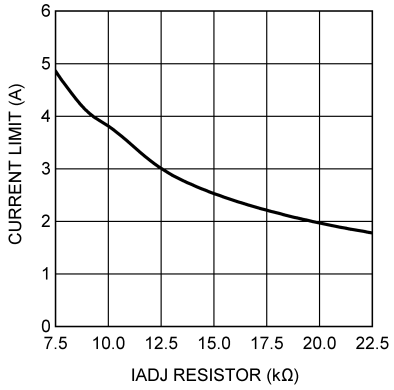

Figure 12. Current Limit vs IADJ Resistor

7.4.3 Thermal Protection

Internal thermal shutdown circuitry protects the LM22673 should the maximum junction temperature be exceeded. This protection is activated at about 150°C, with the result that the regulator will shutdown until the temperature drops below about 135°C.

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Device Functional Modes (continued)

7.4.4 Duty-Cycle Limits

Ideally the regulator would control the duty cycle over the full range of zero to one. However due to inherent delays in the circuitry, there are limits on both the maximum and minimum duty cycles that can be reliably controlled. This in turn places limits on the maximum and minimum input and output voltages that can be converted by the LM22673. A minimum on-time is imposed by the regulator in order to correctly measure the switch current during a current limit event. A minimum off-time is imposed in order the re-charge the bootstrap capacitor. Equation 7 can be used to determine the approximate maximum input voltage for a given output voltage.

$$V_{in}|_{max} \approx \frac{V_{out} + 0.4}{T_{on} \cdot F_{sw} \cdot 1.8} \tag{7}$$

Where:

F_{sw} is the switching frequency.

T_{ON} is the minimum on-time.

Both parameters are found in the *Electrical Characteristics* table.

Nominal values should be used. The worst case is lowest output voltage. If this input voltage is exceeded, the regulator will skip cycles, effectively lowering the switching frequency. The consequences of this are higher output voltage ripple and a degradation of the output voltage accuracy.

The second limitation is the maximum duty cycle before the output voltage will "dropout" of regulation. Equation 8 can be used to approximate the minimum input voltage before dropout occurs.

$$V_{in}|_{min} \approx \frac{V_{out} + 0.4 + I_{out} \cdot R_L}{1 - T_{off} \cdot F_{sw} \cdot 1.8} + I_{out} \cdot R_{dson} \tag{8}$$

Where:

The values of T_{OFF} and $R_{DS(ON)}$ are found in the *Electrical Characteristics* table.

The worst case here is largest load. In this equation, R_L is the dc inductor resistance. Of course, the lowest input voltage to the regulator must not be less than 4.5 V (typ).

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8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM22673 device is a step down dc-to-dc regulator. It is typically used to convert a higher dc voltage to a lower dc voltage with a maximum output current of 3 A. *Detailed Design Procedure* can be used to select components for the LM22673 device. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH® software utilizes iterative design procedure and accesses comprehensive databases of components. Go to WEBENCH Designer for more details. This section presents a simplified discussion of the design process.

8.1.1 Output Voltage Divider Selection

For output voltages between about 1.285 V and 5 V, the -ADJ option should be used, with an appropriate voltage divider as shown in Figure 13. Equation 9 can be used to calculate the resistor values of this divider.

$$R_{FBT} = \left[\frac{V_{out}}{1.285} - 1\right] \cdot R_{FBB} \tag{9}$$

A good value for R_{FBB} is 1 kΩ. This will help to provide some of the minimum load current requirement and reduce susceptibility to noise pick-up. The top of R_{FBT} should be connected directly to the output capacitor or to the load for remote sensing. If the divider is connected to the load, a local high-frequency bypass should be provided at that location.

For output voltages of 5 V, the -5.0 option should be used. In this case no divider is needed and the FB pin is connected to the output. The approximate values of the internal voltage divider are as follows: 7.38 kΩ from the FB pin to the input of the error amplifier and 2.55 kΩ from there to ground.

Both the -ADJ and -5.0 options can be used for output voltages greater than 5 V, by using the correct output divider. As mentioned in the *Internal Compensation* section, the -5.0 option is optimized for output voltages of 5 V. However, for output voltages greater than 5 V, this option may provide better loop bandwidth than the -ADJ option, in some applications. If the -5.0 option is to be used at output voltages greater than 5 V, Equation 10 should be used to determine the resistor values in the output divider.

$$R_{FBT} = \frac{R_{FBB} \cdot (V_{out} - 5)}{5 + R_{FBB} \cdot 5 \times 10^{-4}} \tag{10}$$

A value of R_{FBB} of about 1 kΩ is a good first choice.

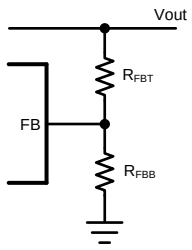

Figure 13. Resistive Feedback Divider

A maximum value of 10 kΩ is recommended for the sum of R_{FBB} and R_{FBT} to maintain good output voltage accuracy for the -ADJ option. A maximum of 2 kΩ is recommended for the -5.0 option. For the -5.0 option, the total internal divider resistance is typically 9.93 kΩ.

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Application Information (continued)

In all cases the output voltage divider should be placed as close as possible to the FB pin of the LM22673, because this is a high impedance input and is susceptible to noise pick-up.

8.1.2 Power Diode

A Schottky-type power diode is required for all LM22673 applications. Ultra-fast diodes are not recommended and may result in damage to the IC due to reverse recovery current transients. The near ideal reverse recovery characteristics and low forward voltage drop of Schottky diodes are particularly important for high input voltage and low output voltage applications common to the LM22673. The reverse breakdown rating of the diode should be selected for the maximum V_{IN}, plus some safety margin. A good rule of thumb is to select a diode with a reverse voltage rating of 1.3 times the maximum input voltage.

Select a diode with an average current rating at least equal to the maximum load current that will be seen in the application.

8.2 Typical Application

8.2.1 Typical Buck Regulator Application

Figure 14 shows an example of converting an input voltage range of 5.5 V to 42 V, to an output of 3.3 V at 3 A.

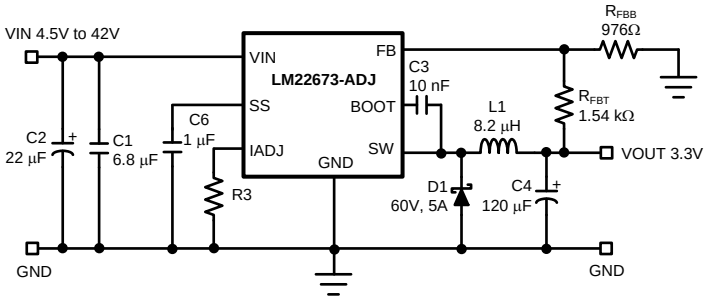

Figure 14. Typical Buck Regulator Application

8.2.1.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (VIN)	5.5 to 42 V
Output Voltage (VOUT)	3.3 V
R_{FBT}	Calculated based on R_{FBB} and V_{REF} of 1.285 V.
R_{FBB}	1 kΩ to 10 kΩ
I_{OUT}	3 A

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 External Components

The following guidelines should be used when designing a step-down (buck) converter with the LM22673.

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8.2.1.2.2 Inductor

The inductor value is determined based on the load current, ripple current, and the minimum and maximum input voltages. To keep the application in continuous conduction mode (CCM), the maximum ripple current, I_{RIPPLE} , should be less than twice the minimum load current.

The general rule of keeping the inductor current peak-to-peak ripple around 30% of the nominal output current is a good compromise between excessive output voltage ripple and excessive component size and cost. Using this value of ripple current, the value of inductor, L, is calculated using Equation 11.

$$L = \frac{(V_{in} - V_{out}) \cdot V_{out}}{0.3 \cdot I_{out} \cdot F_{sw} \cdot V_{in}} \tag{11}$$

Where:

F_{sw} is the switching frequency.

V_{in} should be taken at its maximum value, for the given application.

The formula in Equation 11 provides a guide to select the value of the inductor L; the nearest standard value will then be used in the circuit.

Once the inductor is selected, the actual ripple current can be determined by Equation 12.

$$\Delta I = \frac{(V_{in} - V_{out}) \cdot V_{out}}{L \cdot F_{sw} \cdot V_{in}} \tag{12}$$

Increasing the inductance will generally slow down the transient response but reduce the output voltage ripple. Reducing the inductance will generally improve the transient response but increase the output voltage ripple.

The inductor must be rated for the peak current, I_{PK}, in a given application, to prevent saturation. During normal loading conditions, the peak current is equal to the load current plus 1/2 of the inductor ripple current.

During an overload condition, as well as during certain load transients, the controller may trip current limit. In this case the peak inductor current is given by I_{CL}, found in the *Electrical Characteristics* table. Good design practice requires that the inductor rating be adequate for this overload condition.

NOTE

If the inductor is not rated for the maximum expected current, it can saturate resulting in damage to the LM22673 and/or the power diode.

This consideration highlights the value of the current limit adjust feature of the LM22673.

8.2.1.2.3 Input Capacitor

The input capacitor selection is based on both input voltage ripple and RMS current. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the regulator current during switch on-time. Low ESR ceramic capacitors are preferred. Larger values of input capacitance are desirable to reduce voltage ripple and noise on the input supply. This noise may find its way into other circuitry, sharing the same input supply, unless adequate bypassing is provided. A very approximate formula for determining the input voltage ripple is shown in Equation 13.

$$V_{ri} \approx \frac{I_{out}}{4 \cdot F_{sw} \cdot C_{in}} \tag{13}$$

Where:

V_{ri} is the peak-to-peak ripple voltage at the switching frequency.

Another concern is the RMS current passing through this capacitor. Equation 14 gives an approximation to this current.

$$I_{rms} \approx \frac{I_{out}}{2} \tag{14}$$

The capacitor must be rated for at least this level of RMS current at the switching frequency.

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All ceramic capacitors have large voltage coefficients, in addition to normal tolerances and temperature coefficients. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum capacitance up to the desired value. This may also help with RMS current constraints by sharing the current among several capacitors. Many times it is desirable to use an electrolytic capacitor on the input, in parallel with the ceramics. The moderate ESR of this capacitor can help to damp any ringing on the input supply caused by long power leads. This method can also help to reduce voltage spikes that may exceed the maximum input voltage rating of the LM22673.

It is good practice to include a high frequency bypass capacitor as close as possible to the LM22673. This small case size, low ESR, ceramic capacitor should be connected directly to the VIN and GND pins with the shortest possible PCB traces. Values in the range of 0.47 µF to 1 µF are appropriate. This capacitor helps to provide a low impedance supply to sensitive internal circuitry. It also helps to suppress any fast noise spikes on the input supply that may lead to increased EMI.

8.2.1.2.4 Output Capacitor

The output capacitor is responsible for filtering the output voltage and supplying load current during transients. Capacitor selection depends on application conditions as well as ripple and transient requirements. Best performance is achieved with a parallel combination of ceramic capacitors and a low ESR SP™ or POSCAP™ type. Very low ESR capacitors such as ceramics reduce the output ripple and noise spikes, while higher value electrolytics or polymers provide large bulk capacitance to supply transients. Assuming very low ESR, Equation 15 gives an approximation to the output voltage ripple.

$$V_{ro} \approx \frac{(V_{in} - V_{out}) \cdot V_{out}}{8 \cdot V_{in}} \cdot \frac{1}{F_{sw}^2 \cdot L \cdot C_{out}} \tag{15}$$

Typically, a total value of 100 µF, or greater, is recommended for output capacitance.

In applications with V_{out} less than 3.3 V, it is critical that low ESR output capacitors are selected. This will limit potential output voltage overshoots as the input voltage falls below the device normal operating range.

8.2.1.2.5 Boot-Strap Capacitor

The bootstrap capacitor between the BOOT pin and the SW pin supplies the gate current to turn on the N-channel MOSFET. The recommended value of this capacitor is 10 nF and should be a good quality, low ESR ceramic capacitor. In some cases it may be desirable to slow down the turn-on of the internal power MOSFET, in order to reduce EMI. This can be done by placing a small resistor in series with the C_{boot} capacitor. Resistors in the range of 10 Ω to 50 Ω can be used. This technique should only be used when absolutely necessary, because it will increase switching losses and thereby reduce efficiency.

8.2.1.3 Application Curve

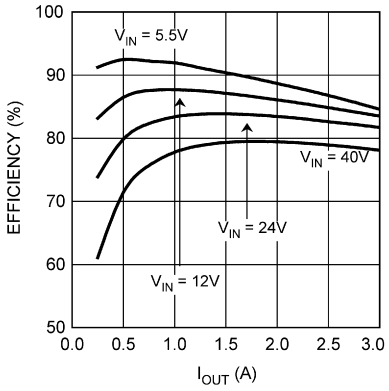

Figure 15. Efficiency vs I_{OUT} and V_{IN}
V_{OUT} = 3.3 V

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9 Power Supply Recommendations

The LM22673 device is designed to operate from an input voltage supply range between 4.5 V and 42 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LM22673 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LM22673, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47 µF or 100 µF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

Board layout is critical for the proper operation of switching power supplies. First, the ground plane area must be sufficient for thermal dissipation purposes. Second, appropriate guidelines must be followed to reduce the effects of switching noise. Switch mode converters are very fast switching devices. In such cases, the rapid increase of input current combined with the parasitic trace inductance generates unwanted L di/dt noise spikes. The magnitude of this noise tends to increase as the output current increases. This noise may turn into electromagnetic interference (EMI) and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise.

The most important layout rule is to keep the ac current loops as small as possible. Figure 16 shows the current flow in a buck converter. The top schematic shows a dotted line which represents the current flow during the FET switch on-state. The middle schematic shows the current flow during the FET switch off-state.

The bottom schematic shows the currents referred to as ac currents. These ac currents are the most critical because they are changing in a very short time period. The dotted lines of the bottom schematic are the traces to keep as short and wide as possible. This will also yield a small loop area reducing the loop inductance. To avoid functional problems due to layout, review the PCB layout example. Best results are achieved if the placement of the LM22673, the bypass capacitor, R_{FFB}, R_{FBT}, the Schottky diode and the inductor are placed as shown in the example. In the layout shown, R1 = R_{FBB} and R2 = R_{FBT}. It is also recommended to use 2 oz copper boards or heavier to help thermal dissipation and to reduce the parasitic inductances of board traces. See *AN-1229 SIMPLE SWITCHER ® PCB Layout Guidelines* (SNVA054) for more information.

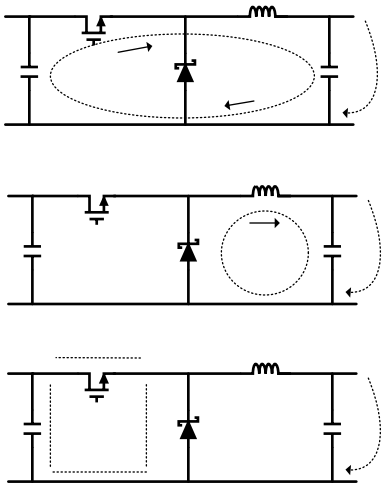

Figure 16. Current Flow in a Buck Application

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10.2 Layout Examples

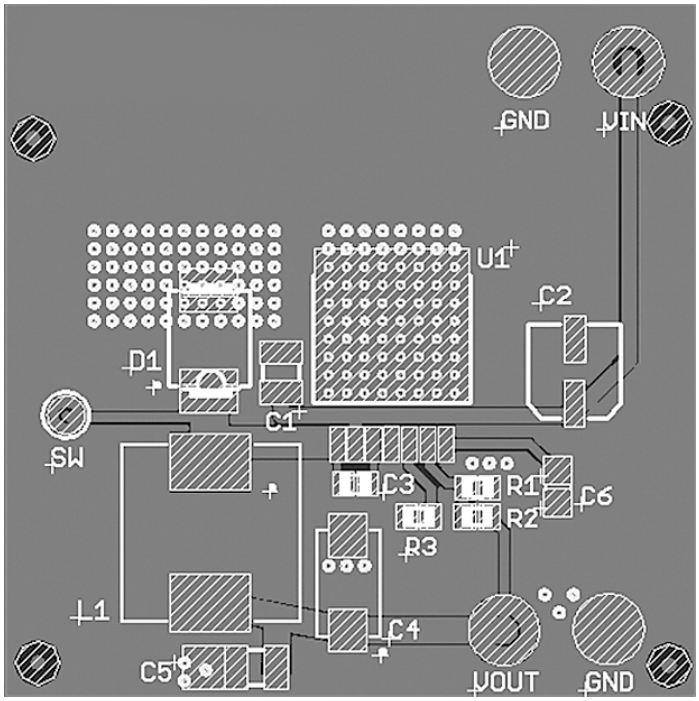

Figure 17. PCB Layout Example for PFM Package

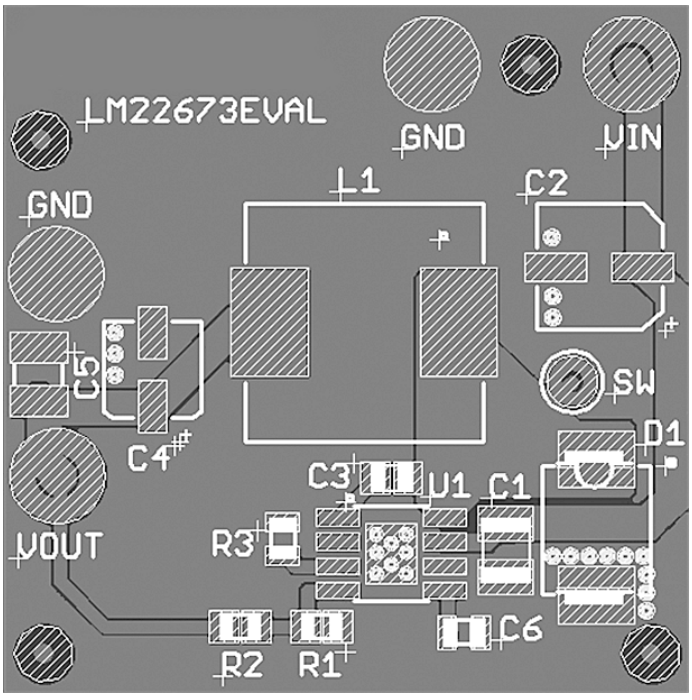

Figure 18. PCB Layout Example for SO PowerPAD Package

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10.3 Thermal Considerations

The components with the highest power dissipation are the power diode and the power MOSFET internal to the LM22673 regulator. The easiest method to determine the power dissipation within the LM22673 is to measure the total conversion losses then subtract the power losses in the diode and inductor. The total conversion loss is the difference between the input power and the output power. An approximation for the power diode loss is shown in Equation 16.

$$P_D = I_{out} \cdot V_D \cdot \left[1 - \frac{V_{out}}{V_{in}}\right] \quad (16)$$

Where:

V_D is the diode voltage drop.

An approximation for the inductor power is determined by Equation 17.

$$P_L = I_{out}^2 \cdot R_L \cdot 1.1 \quad (17)$$

Where:

R_L is the dc resistance of the inductor.

The 1.1 factor is an approximation for the ac losses.

The regulator has an exposed thermal pad to aid power dissipation. Adding multiple vias under the device to the ground plane will greatly reduce the regulator junction temperature. Selecting a diode with an exposed pad will also aid the power dissipation of the diode. The most significant variables that affect the power dissipation of the regulator are output current, input voltage and operating frequency. The power dissipated while operating near the maximum output current and maximum input voltage can be appreciable. The junction-to-ambient thermal resistance of the LM22673 will vary with the application. The most significant variables are the area of copper in the PC board, the number of vias under the IC exposed pad and the amount of forced air cooling provided. A large continuos ground plane on the top or bottom PCB layer will provide the most effective heat dissipation. The integrity of the solder connection from the IC exposed pad to the PC board is critical. Excessive voids will greatly diminish the thermal dissipation capacity. The junction-to-ambient thermal resistance of the LM22673 SO PowerPAD package, and the PFM package, are specified in the *Electrical Characteristics* table. See *AN-2020 Thermal Design By Insight, Not Hindsight* (SNVA419) for more information.

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11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

- *AN-2020《富于洞见的热设计》*（文献编号：SNVA419）
- *AN-1229《SIMPLE SWITCHER? PCB 布局指南》*（文献编号：SNVA054）
- *《AN-1894 LM22673 评估板》*（文献编号：SNVA367）
- *AN-1889《如何测量电源的环路传递函数》*（文献编号：SNVA364）
- *《AN-1797 TO-263 薄型封装》*（文献编号：SNVA328）

11.2 相关链接

下面的表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，以及样片或购买的快速访问。

表 **1.** 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
LM22673	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LM22673-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 商标

SIMPLE SWITCHER, WEBENCH are registered trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM22673MR-5.0/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L22673 5.0	Samples
LM22673MR-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L22673 ADJ	Samples
LM22673MRE-5.0/NOPB	ACTIVE	SO PowerPAD	DDA	8	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L22673 5.0	Samples
LM22673MRE-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L22673 ADJ	Samples
LM22673MRX-5.0/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L22673 5.0	Samples
LM22673MRX-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L22673 ADJ	Samples
LM22673QMR-5.0/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L22673 Q-5.0	Samples
LM22673QMR-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L22673 QADJ	Samples
LM22673QMRE-5.0/NOPB	ACTIVE	SO PowerPAD	DDA	8	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L22673 Q-5.0	Samples
LM22673QMRE-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L22673 QADJ	Samples
LM22673QMRX-5.0/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L22673 Q-5.0	Samples
LM22673QMRX-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L22673 QADJ	Samples
LM22673QTJ-5.0/NOPB	ACTIVE	TO-263	NDR	7	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM22673 QTJ-5.0	Samples
LM22673QTJ-ADJ/NOPB	ACTIVE	TO-263	NDR	7	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM22673 QTJ-ADJ	Samples
LM22673QTJE-5.0/NOPB	ACTIVE	TO-263	NDR	7	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM22673 QTJ-5.0	Samples
LM22673QTJE-ADJ/NOPB	ACTIVE	TO-263	NDR	7	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM22673 QTJ-ADJ	Samples
LM22673TJ-5.0/NOPB	ACTIVE	TO-263	NDR	7	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM22673	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										TJ-5.0	
LM22673TJ-ADJ/NOPB	ACTIVE	TO-263	NDR	7	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM22673 TJ-ADJ	Samples
LM22673TJE-5.0/NOPB	ACTIVE	TO-263	NDR	7	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM22673 TJ-5.0	Samples
LM22673TJE-ADJ/NOPB	ACTIVE	TO-263	NDR	7	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM22673 TJ-ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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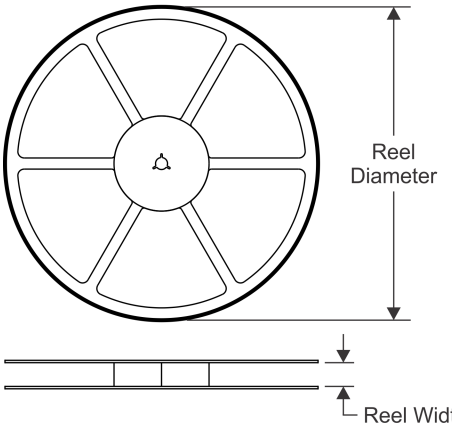
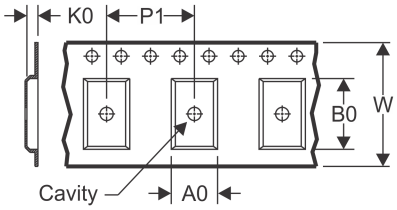
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

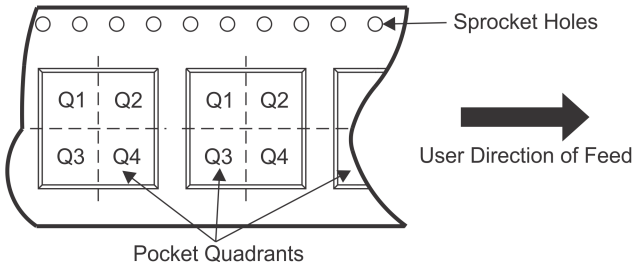


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

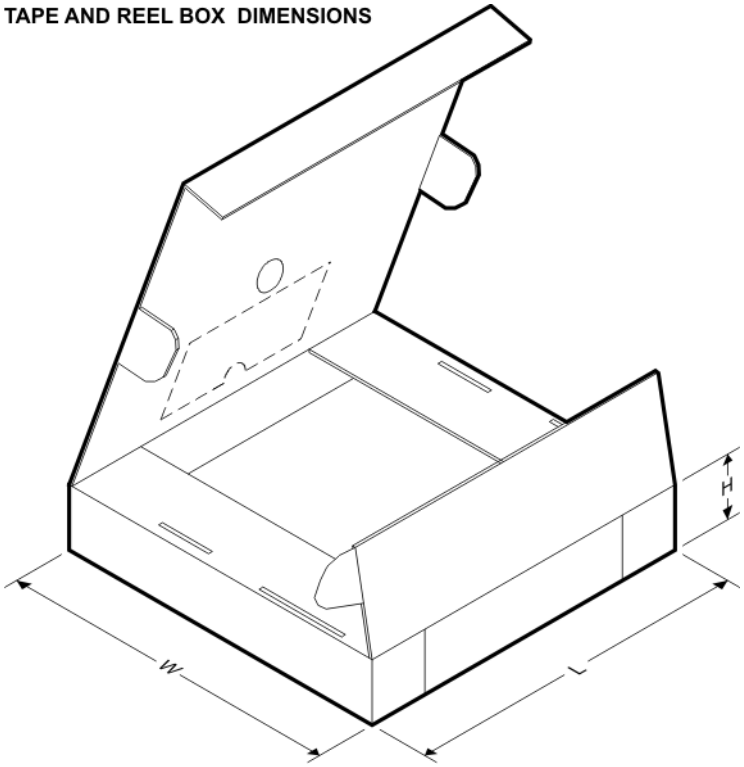


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM22673MRE-5.0/NOPB	SO Power PAD	DDA	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM22673MRE-ADJ/NOPB	SO Power PAD	DDA	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM22673MRX-5.0/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM22673MRX-ADJ/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM22673QMRE-5.0/NOPB	SO Power PAD	DDA	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM22673QMRE-ADJ/NOPB	SO Power PAD	DDA	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM22673QMRX-5.0/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM22673QMRX-ADJ/NOP	SO	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
B	Power PAD											
LM22673QTJ-5.0/NOPB	TO-263	NDR	7	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22673QTJ-ADJ/NOPB	TO-263	NDR	7	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22673QTJE-5.0/NOPB	TO-263	NDR	7	250	178.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22673QTJE-ADJ/NOPB	TO-263	NDR	7	250	178.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22673TJ-5.0/NOPB	TO-263	NDR	7	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22673TJ-ADJ/NOPB	TO-263	NDR	7	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22673TJE-5.0/NOPB	TO-263	NDR	7	250	178.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22673TJE-ADJ/NOPB	TO-263	NDR	7	250	178.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

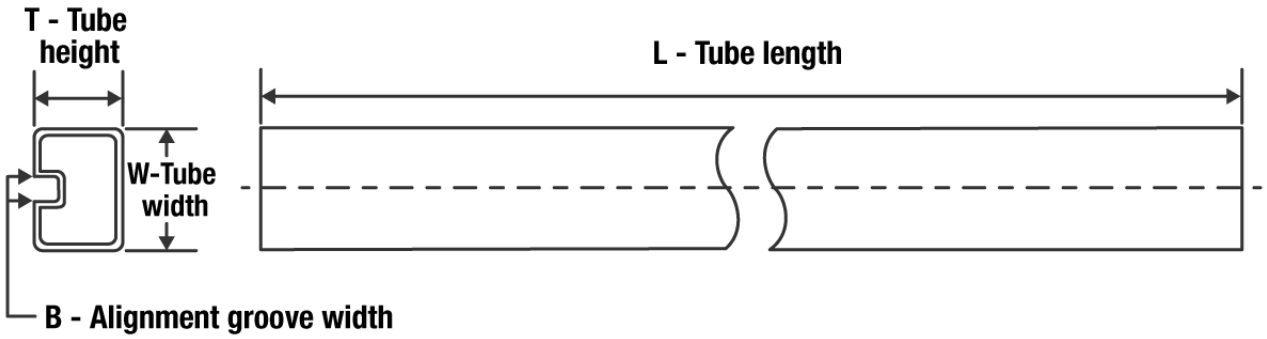


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM22673MRE-5.0/NOPB	SO PowerPAD	DDA	8	250	208.0	191.0	35.0
LM22673MRE-ADJ/NOPB	SO PowerPAD	DDA	8	250	208.0	191.0	35.0
LM22673MRX-5.0/NOPB	SO PowerPAD	DDA	8	2500	853.0	449.0	35.0
LM22673MRX-ADJ/NOPB	SO PowerPAD	DDA	8	2500	853.0	449.0	35.0
LM22673QMRE-5.0/NOPB	SO PowerPAD	DDA	8	250	208.0	191.0	35.0
LM22673QMRE-ADJ/NOPB	SO PowerPAD	DDA	8	250	208.0	191.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM22673QMRX-5.0/NOPB	SO PowerPAD	DDA	8	2500	853.0	449.0	35.0
LM22673QMRX-ADJ/NOPB	SO PowerPAD	DDA	8	2500	853.0	449.0	35.0
LM22673QTJ-5.0/NOPB	TO-263	NDR	7	1000	367.0	367.0	35.0
LM22673QTJ-ADJ/NOPB	TO-263	NDR	7	1000	367.0	367.0	35.0
LM22673QTJE-5.0/NOPB	TO-263	NDR	7	250	210.0	185.0	35.0
LM22673QTJE-ADJ/NOPB	TO-263	NDR	7	250	210.0	185.0	35.0
LM22673TJ-5.0/NOPB	TO-263	NDR	7	1000	367.0	367.0	35.0
LM22673TJ-ADJ/NOPB	TO-263	NDR	7	1000	367.0	367.0	35.0
LM22673TJE-5.0/NOPB	TO-263	NDR	7	250	210.0	185.0	35.0
LM22673TJE-ADJ/NOPB	TO-263	NDR	7	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

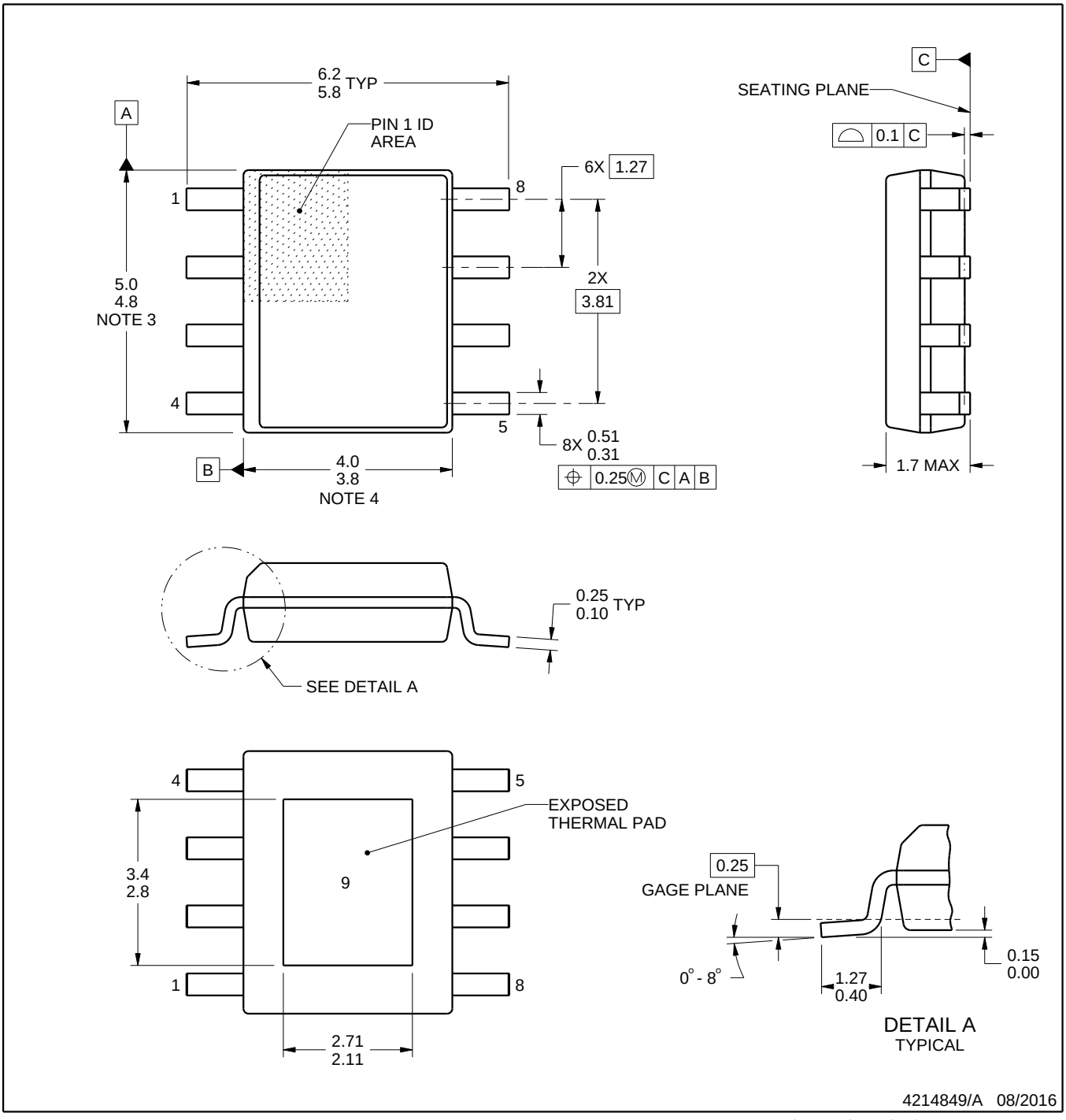
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM22673MR-5.0/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LM22673MR-ADJ/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LM22673MR-ADJ/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LM22673QMR-5.0/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LM22673QMR-ADJ/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

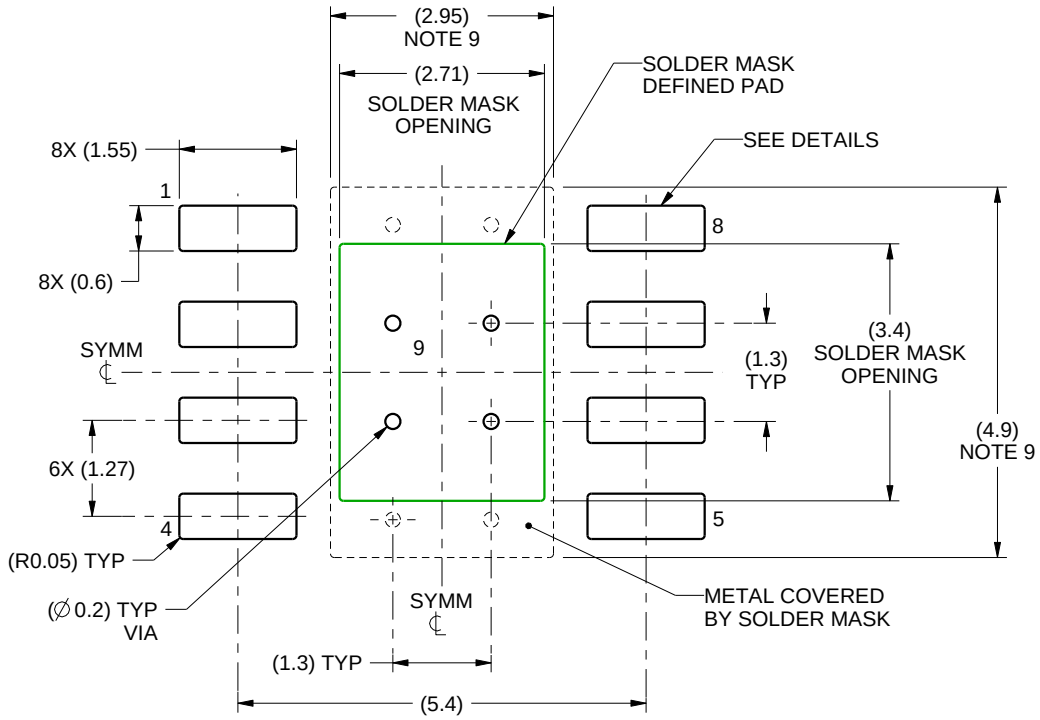
PLASTIC SMALL OUTLINE



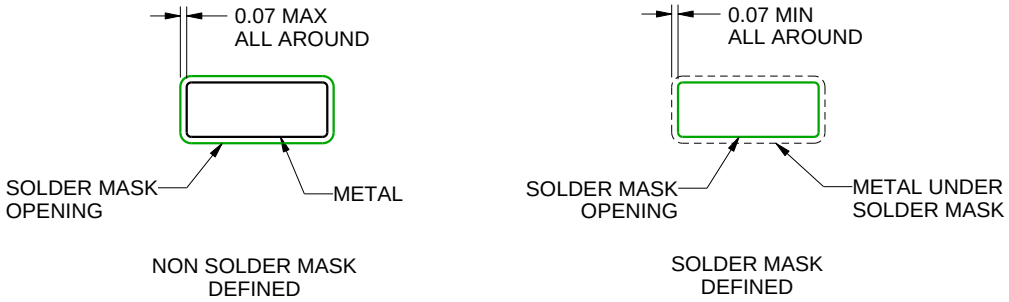
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

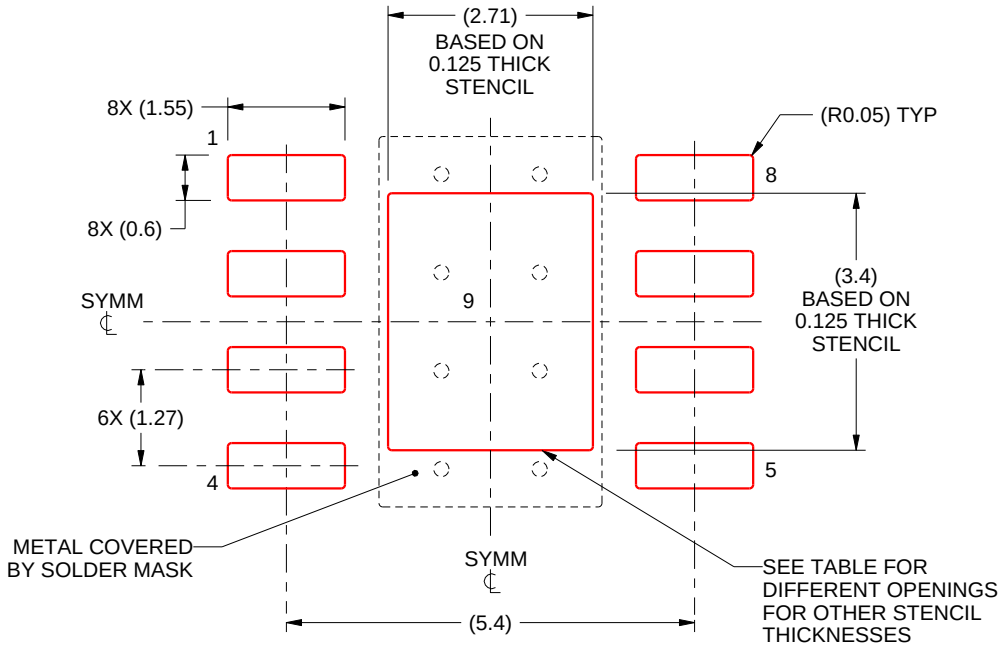
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

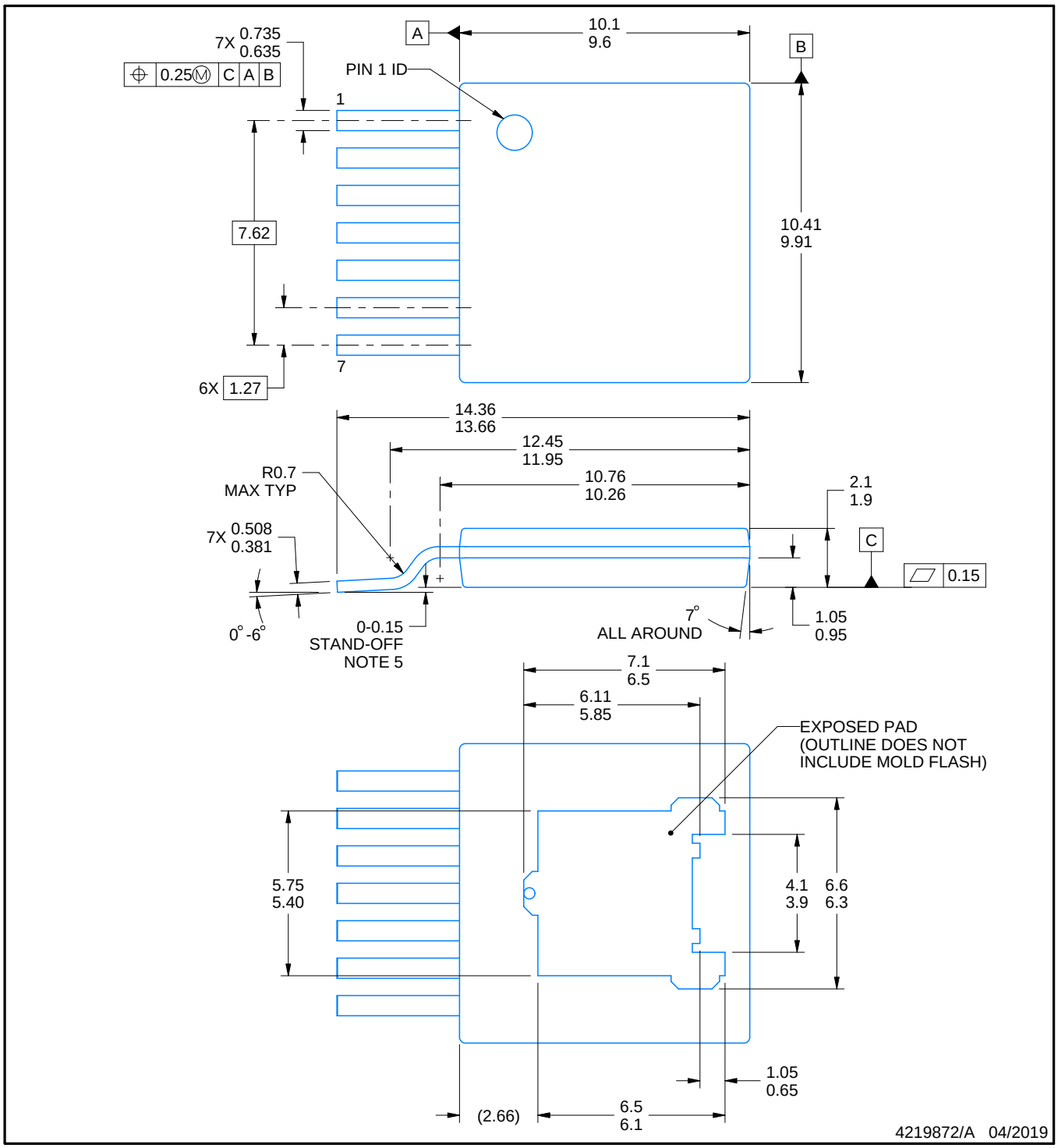
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

NDR0007A

TO-263 - 2.25 mm max height

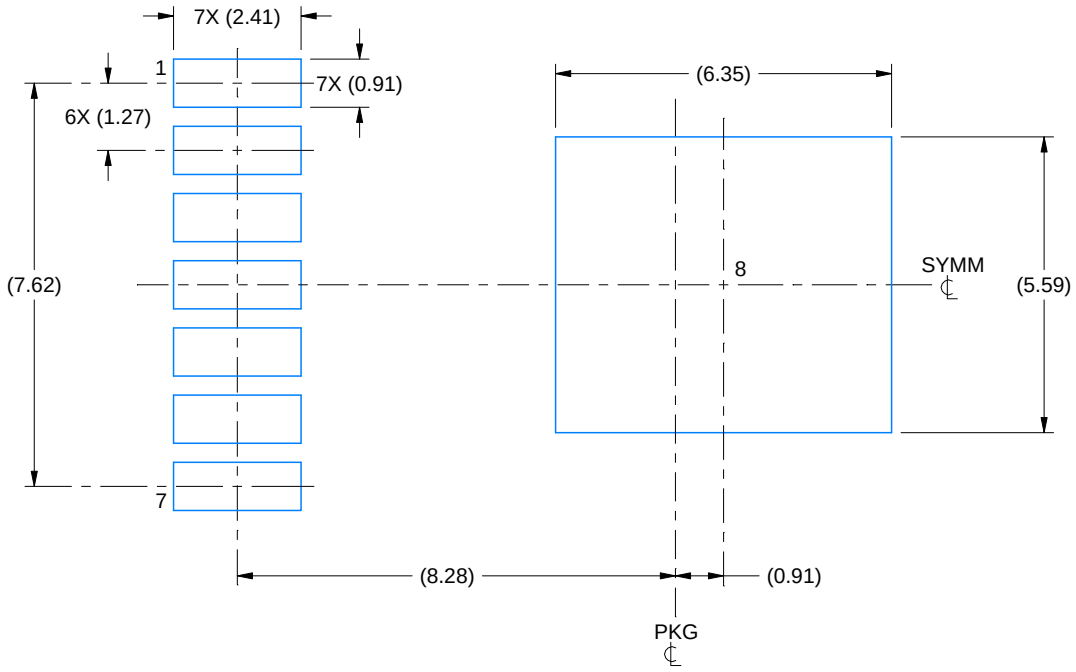
TO-263

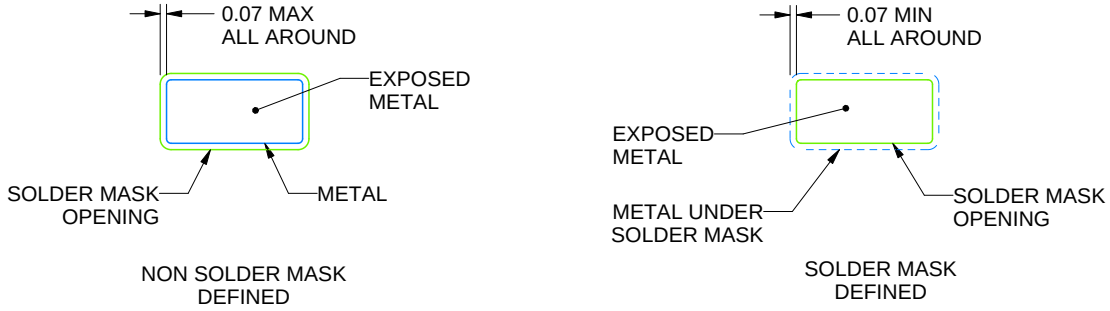


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.
4. Reference JEDEC registration TO-279B.
5. Under all conditions, leads must not be above Datum C

TO-263



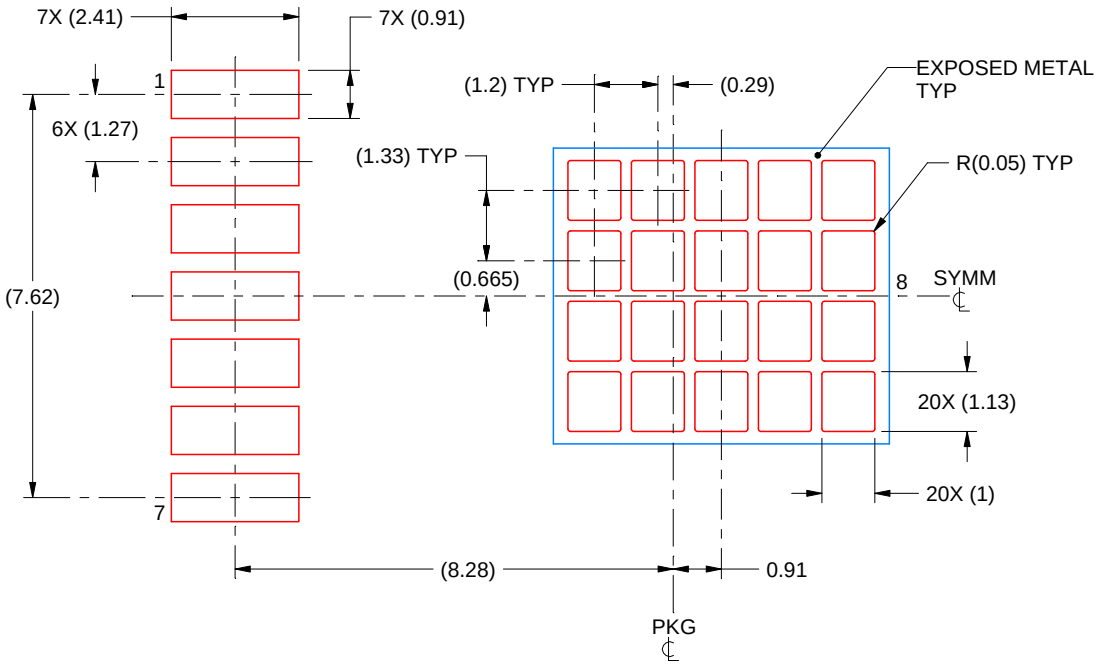


SOLDER MASK DETAILS

4219872/A 04/2019

NOTES: (continued)

6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
7. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
64% PRINTED SOLDER COVERAGE BY AREA
SCALE:7X

4219872/A 04/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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