ISO71xxCC 4242V$_{PK}$ 小封装低功耗三通道和四通道数字隔离器

1 特性

- 最大信号传输速率： 50Mbps（5V 电源）
- 具有集成噪声滤波器的稳健耐用设计
- 缺省输出低选项（后缀 F）
- 低功耗，每通道 I_{CC} 典型值（3.3V 电源）：
  - ISO7131：1Mbps 时为 1.5mA，25Mbps 时为 2.6mA
  - ISO7140：1Mbps 时为 1mA，25Mbps 时为 2.3mA
  - ISO7141：1Mbps 时为 1.3mA，25Mbps 时为 2.6mA
- 低传播延迟：典型值 23ns（3.3V 电源）
- 宽温度范围：-40℃ 至 125°C
- 50kV/μs 瞬态抗扰度，典型值
- 采用 SiO_2 隔离格栅，使用寿命长
- 可由 2.7V、3.3V 和 5V 电源及逻辑电平供电
- 小型四分之一尺寸小外形封装 (QSOP)-16 封装
- 安全及管理批准
  - 符合 UL 1577 的长达 1 分钟的 2500V$_{RMS}$ 隔离
  - 符合 DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 的 4242V$_{PK}$ 隔离，566V$_{PK}$ 工作电压
  - CSA 组件接受通知 5A，IEC 60950-1 和 IEC 61010-1 终端设备标准
  - 符合 GB 4943.1-2011 的 CQC 认证

2 应用范围

- 通用隔离
  - 工业现场总线 (Fieldbus)
    - Profibus 现场总线
    - Modbus™
    - DeviceNet 数据总线
  - RS-232，RS-485
  - 串行外设接口

3 说明

ISO7131、ISO7140 和 ISO7141 器件提供符合 UL 标准的长达 1 分钟的 2500 V_{RMS} 电流隔离，以及符合 VDE 标准的 4242 V_{PK}。 ISO7131 有三个通道，其中两个为正向通道，一个为反向通道。 ISO7140 和 ISO7141 均为四通道隔离器；ISO7140 有四个正向通道，而 ISO7141 有三个正向通道和一个反向通道。 这些器件在由 5V 电源和 3.3V/2.7V 电源供电时，分别可提供 50Mbps 和 40Mbps 的最大数据传输速率，并且输入上带有集成滤波器，适用于易受噪声干扰的应用。后缀 F 表示缺省输出状态为低电平；否则，缺省输出状态为高电平（请见表 3）。

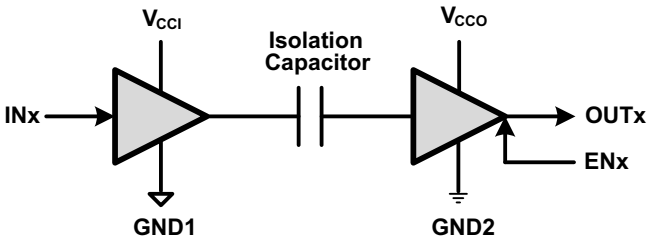
每个隔离通道的逻辑输入和输出缓冲器均由二氧化硅 (SiO_2) 绝缘隔栅分离开来。 与隔离式电源一起使用时，这些器件可防止数据总线或者其它电路上的噪声电流进入本地接地并且干扰或损坏敏感电路。 这些器件具有晶体管晶体管逻辑电路 (TTL) 输入阈值，并且可由 2.7V、3.3V 和 5V 电压供电运行。 通过 2.7V 或 3.3V 电源供电时，所有输入均可耐受 5V 电压。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ISO7131CC	SSOP (16)	4.90mm × 3.90mm
ISO7140CC		
ISO7140FCC		
ISO7141CC		
ISO7141FCC		

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (September 2013) to Revision F **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定表*，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分部分 ... 1
- VDE 标准更改为 DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ... 1

Changes from Revision D (August 2013) to Revision E **Page**

- 将符合 UL 1577 的长达 1 分钟的 2500V_{RMS} 隔离从（审批正在审理中）更改为（已通过审批） ... 1
- Added note1 to the AVAILABLE OPTIONS table ... 17
- Changed 图 15 ... 18
- Changed From: Basic Insulation To: Basic Insulation, Altitude ≤ 5000m, Tropical Climate, 250 VRMS maximum working voltage in the Regulatory Information table ... 19
- Changed File number: E181974 (approval pending) To: File number: E181974 in the Regulatory Information table ... 19
- Changed the title of 图 21, 图 22, and 图 23 to include "PRBS 2^{16} - 1" ... 23

Changes from Revision C (July 2013) to Revision D **Page**

- 添加了安全列表项“GB 4943.1-2011 和 GB 8898:2011 CQC 认证（审批正在审理中）” ... 1
- Added 图 2 ... 12
- Deleted "Product Preview" From the AVAILABLE OPTIONS table ... 17
- Changed the REGULATORY INFORMATION, added column for CQC ... 19

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Changes from Revision B (June 2013) to Revision C **Page**

- 将特性从：ISO7140：1Mbps 时待定 (TBD)，25Mbps 时 TBD 改为：ISO7140：1Mbps 时为 1mA，25Mbps 时为 2.3mA 1
- 在说明中添加了文本：“当由一个 2.7V 或者 3.3V 电源供电时，所有输入均可耐受 5V 电压。” 1
- 删除了产品状态表 1
- 更改了安全和管理批准 1
- Changed the ABSOLUTE MAXIMUM RATINGS table 5
- Changed the SWITCHING CHARACTERISTICS table, Input glitch rejection time. 7
- Changed the SWITCHING CHARACTERISTICS table, Input glitch rejection time. 8
- Changed the SWITCHING CHARACTERISTICS table, Input glitch rejection time. 8
- Changed ISO7140 in the SUPPLY CURRENT table From: TBD To: values 9
- Changed ISO7140 in the SUPPLY CURRENT table From: TBD To: values 10
- Changed ISO7140 in the SUPPLY CURRENT table From: TBD To: values 11
- Changed 图 1 X-axis scale 12
- Changed the AVAILABLE OPTIONS table 17

Changes from Revision A (June 2013) to Revision B **Page**

- 将器件 ISO7141CC 从：产品预览改为：在产品状态表中发布 1

Changes from Original (April 2013) to Revision A **Page**

- 更改了简化电路原理图，添加了接地符号 1
- Changed the SWITCHING CHARACTERISTICS table, Input glitch rejection time. Values by device. 7
- Changed the SWITCHING CHARACTERISTICS table, Input glitch rejection time. Values by device. 8
- Changed the SWITCHING CHARACTERISTICS table, Input glitch rejection time. Values by device. 8
- Added 图 3 12

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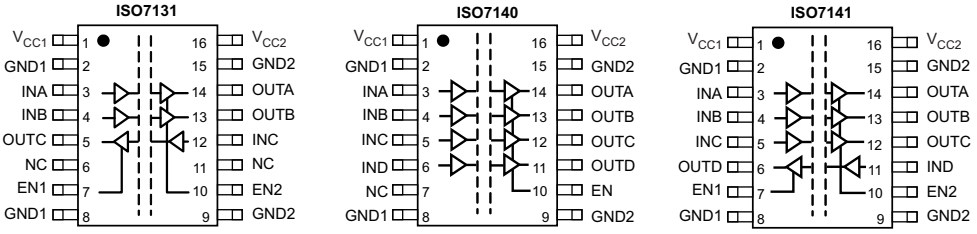
5 Pin Configuration and Functions

16-Pin
SSOP Package
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	ISO7131	ISO7140	ISO7141		
EN	—	10	—	I	Output enable. All output pins are enabled when EN is high or disconnected and disabled when EN is low.
EN1	7	—	7	I	Output enable 1. Output pins on side-1 are enabled when EN1 is high or disconnected and disabled when EN1 is low.
EN2	10	—	10	I	Output enable 2. Output pins on side-2 are enabled when EN2 is high or disconnected and disabled when EN2 is low.
GND1	2,8	2,8	2,8	—	Ground connection for V_{CC1}
GND2	9,15	9,15	9,15	—	Ground connection for V_{CC2}
INA	3	3	3	I	Input, channel A
INB	4	4	4	I	Input, channel B
INC	12	5	5	I	Input, channel C
IND	—	6	11	I	Input, channel D
NC	6,11	7	—	—	No Connect pins are floating with no internal connection
OUTA	14	14	14	O	Output, channel A
OUTB	13	13	13	O	Output, channel B
OUTC	5	12	12	O	Output, channel C
OUTD	—	11	6	O	Output, channel D
V_{CC1}	1	1	1	—	Power supply, V_{CC1}
V_{CC2}	16	16	16	—	Power supply, V_{CC2}

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6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage(2)	–0.5	6	V
INx, ENx, OUTx	Voltage	–0.5	V_{CC}+ 0.5(3)	V
I_O	Output current	–15	15	mA
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	2.7		5.5	V
I_{OH}	High-level output current (V_{CC} ≥ 3.0 V)	–4			mA
	High-level output current (V_{CC} < 3.0 V)	–2			
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	0		0.8	
t_{ui}	Input pulse duration (V_{CC} ≥ 4.5V)	20			ns
t_{ui}	Input pulse duration (V_{CC} < 4.5V)	25			
1 / t_{ui}	Signaling rate (V_{CC} ≥ 4.5V)	0		50	Mbps
1 / t_{ui}	Signaling rate (V_{CC} < 4.5V)	0		40	
T_A	Ambient temperature	–40	25	125	°C
T_J	Junction temperature	–40		136	

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6.4 Thermal Information

THERMAL METRIC(1)		ISO7131, ISO714x DBQ 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	104.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	57.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Power Dissipation Ratings

		TEST CONDITIONS	VALUE	UNIT
P_D	Device power dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF Input a 25-MHz, 50% duty cycle square wave	150	mW

6.6 Electrical Characteristics: V_{CC1} and V_{CC2} at 5 V ±10%

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see 图 10	V_{CCO} (1) – 0.5	4.8		V
		I_{OH} = –20 µA; see 图 10	V_{CCO} (1) – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see 图 10		0.2	0.4	V
		I_{OL} = 20 µA; see 图 10		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			450		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see 图 13	25	75		kV/µs

(1) V_{CCO} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

6.7 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V ±10%

V_{CC1} and V_{CC2} at 3.3 V ±10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see 图 10	V_{CCO} (1) – 0.5	3		V
		I_{OH} = –20 µA; see 图 10	V_{CCO} (1) – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see 图 10		0.2	0.4	V
		I_{OL} = 20 µA; see 图 10		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			425		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see 图 13	25	50		kV/µs

(1) V_{CCO} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

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6.8 Electrical Characteristics: V_{CC1} and V_{CC2} at 2.7 V

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see 图 10	V_{CCO} (1) – 0.3	2.5		V
		I_{OH} = –20 μA; see 图 10	V_{CCO} (1) – 0.1	2.7		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see 图 10		0.2	0.4	V
		I_{OL} = 20 μA; see 图 10		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			350		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			μA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see 图 13	25	50		kV/μs

(1) V_{CCO} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

6.9 Switching Characteristics: V_{CC1} and V_{CC2} at 5 V ±10%

V_{CC1} and V_{CC2} at 5 V ±10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 10	12	19	35	ns
PWD (1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$				3	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction channels			2	ns
		Opposite-direction channels			4	
$t_{sk(pp)}$ (3)	Part-to-part skew time				12	ns
t_r	Output signal rise time	See 图 10		2		ns
t_f	Output signal fall time			2		ns
t_{PHZ}, t_{PLZ}	Disable propagation delay, high/low-to-high impedance output	See 图 11		6	10	ns
t_{PZH}, t_{PZL}	Enable propagation delay, high impedance-to-high/low output			5	10	ns
t_{fs}	Fail-safe output delay time from input data or power loss	See 图 12		9.5		μs
t_{GR}	Input glitch rejection time			11		ns

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals, and loads.

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6.10 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3 V ±10%

V_{CC1} and V_{CC2} at 3.3 V ±10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 10	15	23	45	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				3	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			2	ns
		Opposite-direction Channels			4	
$t_{sk(pp)}$ (3)	Part-to-part skew time				19	ns
t_r	Output signal rise time	See 图 10		2.5		ns
t_f	Output signal fall time			2.5		ns
t_{PHZ}, t_{PLZ}	Disable propagation delay, from high/low to high-impedance output	See 图 11		6.5	15	ns
t_{PZH}, t_{PZL}	Enable propagation delay, from high-impedance to high/low output			6.5	15	ns
t_{fs}	Fail-safe output delay time from input data or power loss	See 图 12		8		µs
t_{GR}	Input glitch rejection time			12.5		ns

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.11 Switching Characteristics: V_{CC1} and V_{CC2} at 2.7 V

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 10	15	27	50	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				3	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			2	ns
		Opposite-direction Channels			4	
$t_{sk(pp)}$ (3)	Part-to-part skew time				22	ns
t_r	Output signal rise time	See 图 10		3		ns
t_f	Output signal fall time			3		ns
t_{PHZ}, t_{PLZ}	Disable propagation delay, from high/low to high-impedance output	See 图 11		9	15	ns
t_{PZH}, t_{PZL}	Enable propagation delay, from high-impedance to high/low output			9	15	ns
t_{fs}	Fail-safe output delay time from input data or power loss	See 图 12		8.5		µs
t_{GR}	Input glitch rejection time			14		ns

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals, and loads.

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6.12 Supply Current: V_{CC1} and V_{CC2} at 5 V ±10%

V_{CC1} and V_{CC2} at 5 V ±10% (over recommended operating conditions unless otherwise noted.)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7131						
I_{CC1}	Disable	EN1 = EN2 = 0 V		2.2	3.7	mA
I_{CC2}				3.7	5	
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V AC signal: All channels switching with square-wave clock input; C_L = 15 pF		2.2	3.7	mA
I_{CC2}				3.7	5	
I_{CC1}	10 Mbps			3.4	4.8	
I_{CC2}				4.9	6.6	
I_{CC1}	25 Mbps			4.9	6.6	
I_{CC2}				6.8	9	
I_{CC1}	50 Mbps			7.1	10	
I_{CC2}				10.5	13	
ISO7140						
I_{CC1}	Disable	EN = 0 V		0.6	1.2	mA
I_{CC2}				4.6	7	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.6	1.3	mA
I_{CC2}				4.8	7	
I_{CC1}	10 Mbps			1.4	2.2	
I_{CC2}				6.9	9.2	
I_{CC1}	25 Mbps			2.7	3.9	
I_{CC2}				10.3	13.5	
I_{CC1}	50 Mbps			4.7	6.5	
I_{CC2}				15.6	21	
ISO7141						
I_{CC1}	Disable	EN1 = EN2 = 0V		2.5	4.2	mA
I_{CC2}				4.2	7	
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V, AC signal: All channels switching with square wave clock input; C_L = 15 pF		2.5	4.2	mA
I_{CC2}				4.2	7	
I_{CC1}	10 Mbps			3.8	5.3	
I_{CC2}				6.2	9.6	
I_{CC1}	25 Mbps			5.6	7.5	
I_{CC2}				9.2	13	
I_{CC1}	50 Mbps			8.4	11.2	
I_{CC2}				14	18.5	

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6.13 Supply Current: V_{CC1} and V_{CC2} at 3.3 V ±10%

V_{CC1} and V_{CC2} at 3.3 V ±10% (over recommended operating conditions unless otherwise noted.)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7131						
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.9	2.7	mA
I_{CC2}				2.6	3.8	
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V AC signal: All channels switching with square-wave clock input; C_L = 15 pF		1.9	2.7	mA
I_{CC2}				2.6	3.8	
I_{CC1}	10 Mbps			2.4	3.5	
I_{CC2}				3.5	4.7	
I_{CC1}	25 Mbps			3.2	4.6	
I_{CC2}				4.7	6.2	
I_{CC1}	40 Mbps			5	7	
I_{CC2}				7	9	
ISO7140						
I_{CC1}	Disable	EN = 0 V		0.3	0.7	mA
I_{CC2}				3.6	5.2	
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V, AC signal: All channels switching with square-wave clock input; C_L = 15 pF		0.4	0.8	mA
I_{CC2}				3.7	5.3	
I_{CC1}	10 Mbps			0.9	1.4	
I_{CC2}				5.1	6.8	
I_{CC1}	25 Mbps			1.7	2.4	
I_{CC2}				7.3	10	
I_{CC1}	40 Mbps			2.4	3.7	
I_{CC2}				9.4	13	
ISO7141						
I_{CC1}	Disable	EN1 = EN2 = 0 V		2	3.1	mA
I_{CC2}				3.2	4.9	
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V, AC signal: All channels switching with square-wave clock input; C_L = 15 pF		2	3.1	mA
I_{CC2}				3.2	4.9	
I_{CC1}	10 Mbps			2.8	3.8	
I_{CC2}				4.5	6.1	
I_{CC1}	25 Mbps			4	5.2	
I_{CC2}				6.4	8.3	
I_{CC1}	40 Mbps			5	8	
I_{CC2}				8.2	11.6	

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6.14 Supply Current: V_{CC1} and V_{CC2} at 2.7 V

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted.)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7131						
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.2	2.4	mA
I_{CC2}				2.3	3.3	
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V AC signal: All channels switching with square-wave clock input; C_L = 15 pF		1.2	2.4	mA
I_{CC2}				2.3	3.3	
I_{CC1}	10 Mbps			2.1	3	
I_{CC2}				2.9	4	
I_{CC1}	25 Mbps			3	3.8	
I_{CC2}				4	5.2	
I_{CC1}	40 Mbps			4.2	5.3	
I_{CC2}				5.8	7	
ISO7140						
I_{CC1}	Disable	EN = 0 V		0.2	0.4	mA
I_{CC2}				3.2	4.7	
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V, AC signal: All channels switching with square-wave clock input; C_L = 15 pF		0.2	0.5	mA
I_{CC2}				3.4	4.8	
I_{CC1}	10 Mbps			0.6	1	
I_{CC2}				4.5	6.3	
I_{CC1}	25 Mbps			1.2	1.8	
I_{CC2}				6.2	8	
I_{CC1}	40 Mbps			1.8	2.6	
I_{CC2}				8	11	
ISO7141						
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.6	2.6	mA
I_{CC2}				2.8	4.1	
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V, AC signal: All channels switching with square-wave clock input; C_L = 15 pF		1.6	2.6	mA
I_{CC2}				2.8	4.1	
I_{CC1}	10 Mbps			2.3	3.2	
I_{CC2}				3.8	5	
I_{CC1}	25 Mbps			3.3	4.2	
I_{CC2}				5.4	6.8	
I_{CC1}	40 Mbps			4.3	5.8	
I_{CC2}				6.9	9.2	

6.15 Typical Characteristics

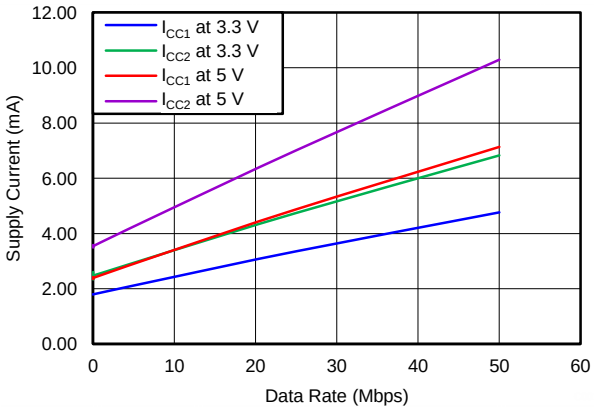

图 1. ISO7131 Supply Current for All Channels vs Data Rate

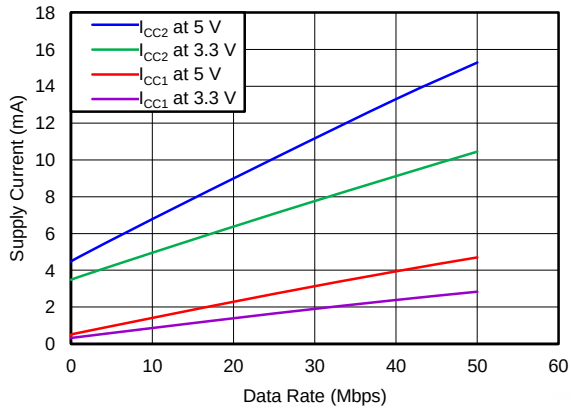

图 2. ISO7140 Supply Current for All Channels vs Data Rate

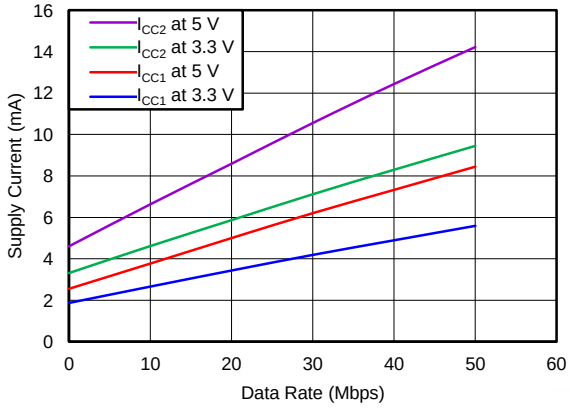

图 3. ISO7141 Supply Current for All Channels vs Data Rate

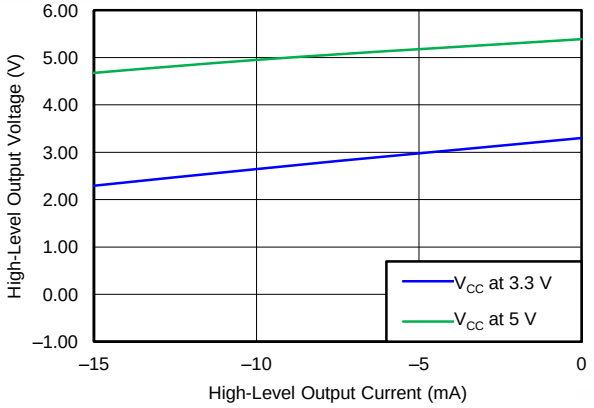

图 4. High-Level Output Voltage vs High-Level Output Current

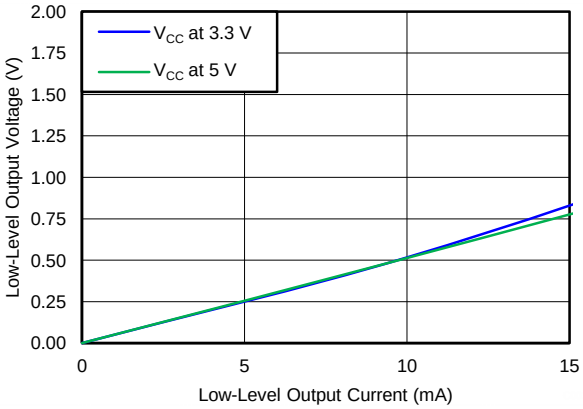

图 5. Low-Level Output Voltage vs Low-Level Output Current

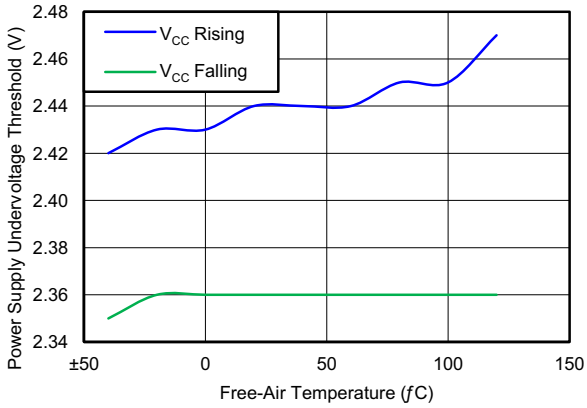

图 6. V_{CC} Undervoltage Threshold vs Free-Air Temperature

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Typical Characteristics (接下页)

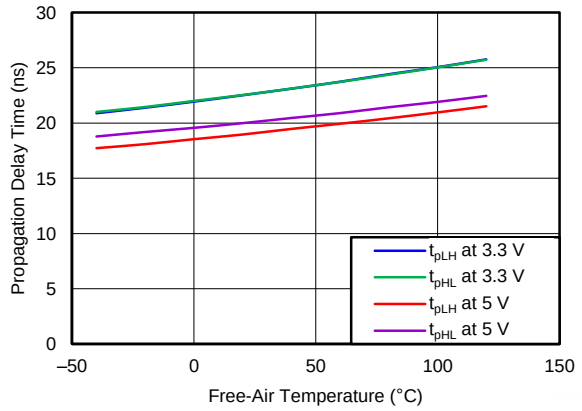


图 7. Propagation Delay Time vs Free-Air Temperature

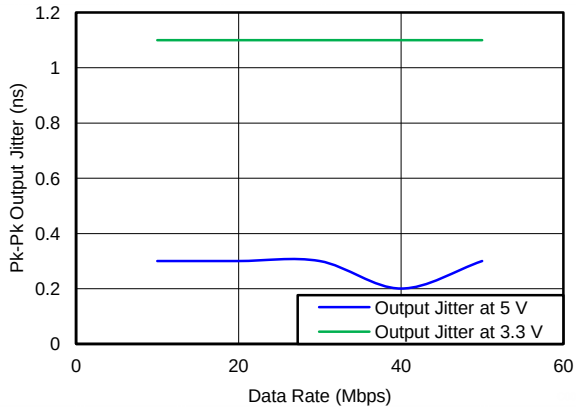


图 8. Output Jitter vs Data Rate

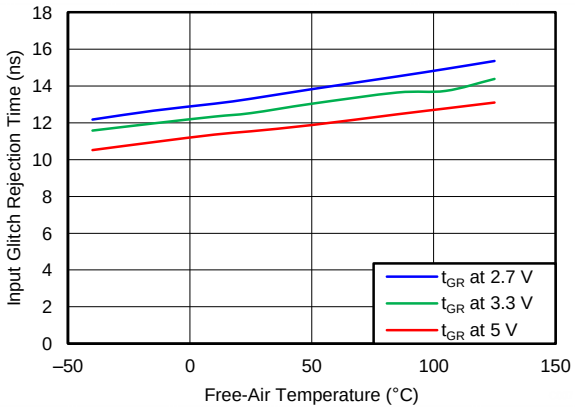
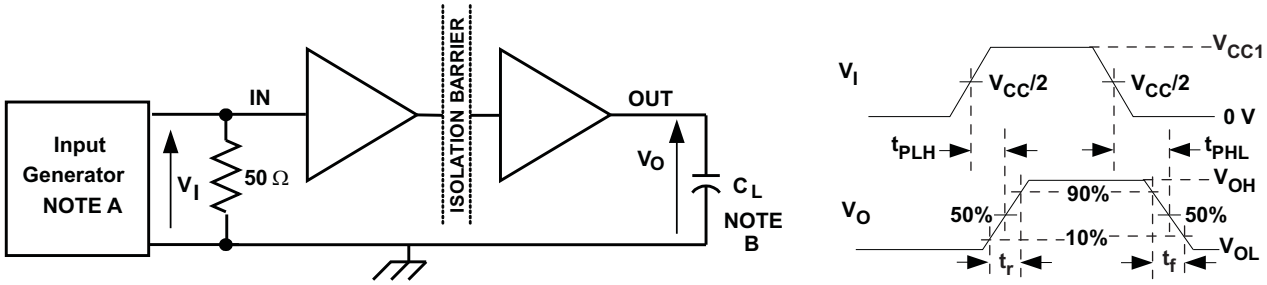


图 9. Input Glitch Rejection vs Free-Air Temperature

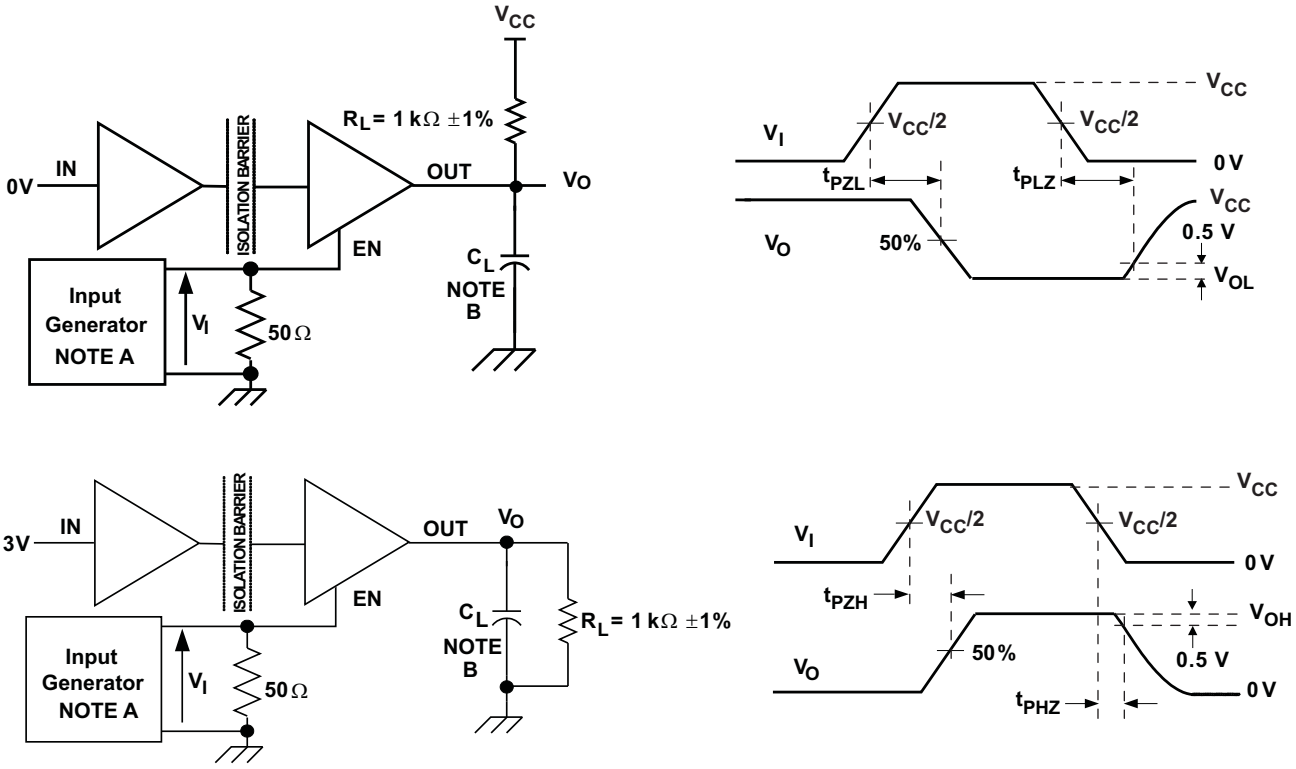
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, a 50-Ω resistor is required to terminate the input-generator signal. It is not needed in an actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

图 10. Switching-Characteristics Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

图 11. Enable/Disable Propagation Delay-Time Test Circuit and Waveform

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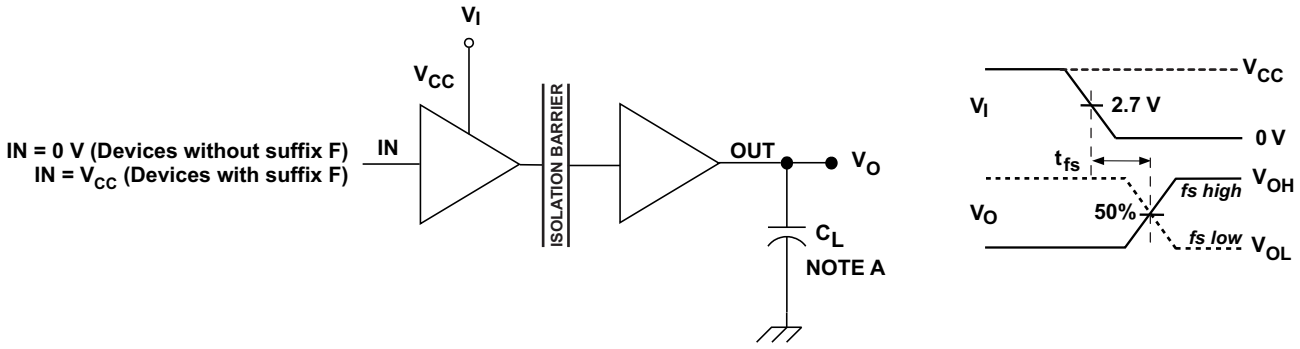
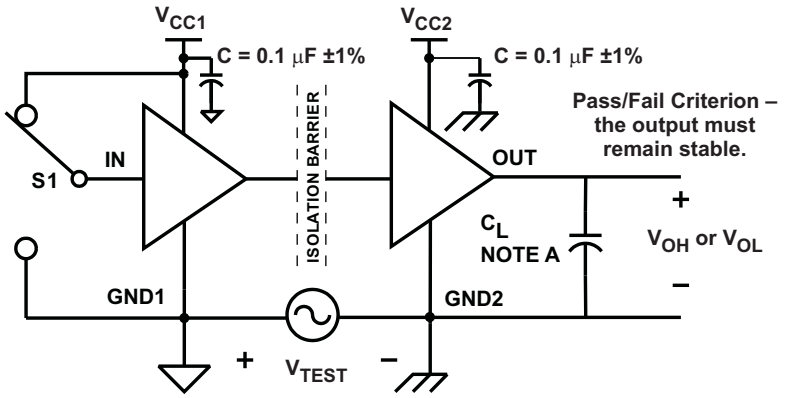
Parameter Measurement Information (接下页)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

图 12. Failsafe Delay-Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

图 13. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The isolator in 图 14 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 150 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single-ended input signal entering the HF-channel is split into a differential signal through the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.2 Functional Block Diagram

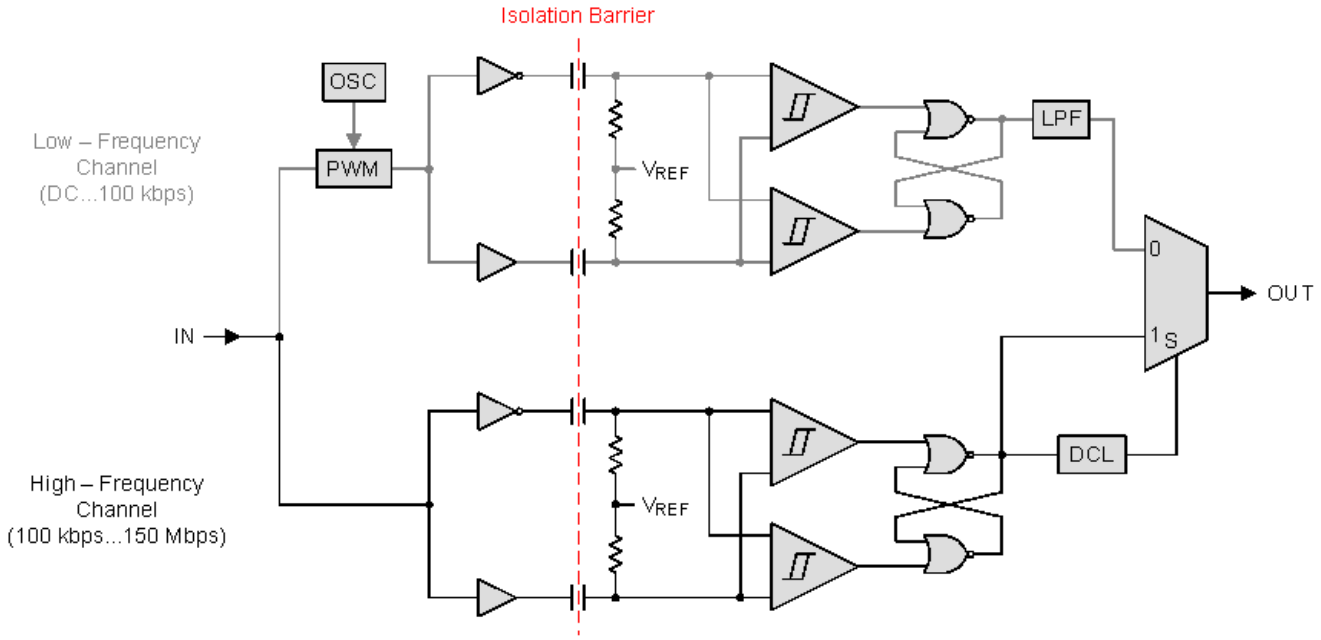


图 14. Conceptual Block Diagram of a Digital Capacitive Isolator

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8.3 Feature Description

表 1. Product Features

PRODUCT	RATED ISOLATION	INPUT THRESHOLD	DEFAULT OUTPUT	MAX DATA RATE and INPUT FILTER	CHANNEL DIRECTION
ISO7131CC	4242 V_{PK} (1)	1.5-V TTL (CMOS compatible)	High	50 Mbps, with noise filter integrated	2 forward, 1 reverse
ISO7140CC					4 forward, 0 reverse
ISO7140FCC			Low		
ISO7141CC			High		3 forward, 1 reverse
ISO7141FCC			Low		

(1) See *Regulatory Information* for detailed Isolation Ratings.

8.3.1 Insulation and Safety-Related Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IOTM}	Maximum transient overvoltage per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12				4242	V_{PK}
V_{IORM}	Maximum working voltage per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12				566	V_{PK}
V_{ISO}	Isolation Voltage per UL 1577	$V_{TEST} = V_{ISO}$, t = 60 sec (qualification)			2500	V_{RMS}
		$V_{TEST} = 1.2 * V_{ISO}$, t = 1 sec (100% production)			3000	
V_{PR}	Input-to-output test voltage per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 s, Partial discharge < 5 pC			679	V_{PK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.6, t = 10 s, Partial discharge < 5 pC			906	
		Method b1, 100% production test, $V_{PR} = V_{IORM}$ x 1.875, t = 1 s, Partial discharge < 5 pC			1061	
L(I01)	Minimum air gap (clearance)	Shortest terminal to terminal distance through air	3.7			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal to terminal distance across the package surface	3.7			mm
	Minimum internal gap (internal clearance)	Distance through the insulation	0.014			mm
	Pollution degree			2		
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1	≥400			V
R_{IO} (1)	Isolation Resistance, Input to Output	V_{IO} = 500 V, T_A = 25°C		$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ T_A max		$>10^{11}$		
C_{IO} (1)	Barrier capacitance, input to output	V_I = 0.4 sin (2πft), f = 1 MHz		2.3		pF
C_I (2)	Input capacitance	$V_I = V_{CC}/2$ + 0.4 sin (2πft), f = 1 MHz, V_{CC} = 5 V		2.8		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

注

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit-board (PCB) do not reduce this distance.

Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and/or ribs on a PCB are used to help increase these specifications.

表 2. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic Isolation Group	Material Group	II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I–IV
	Rated mains voltage ≤ 300 V_{RMS}	I–III
	Rated mains voltage ≤ 400 V_{RMS}	I–II

8.3.1.1 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DBQ-16	$R_{\theta JA}$ = 104.5°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			217	mA
			$R_{\theta JA}$ = 104.5°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			332	
			$R_{\theta JA}$ = 104.5°C/W, V_I = 2.7V, T_J = 150°C, T_A = 25°C			443	
T_S	Maximum case temperature					150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings*(1) table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

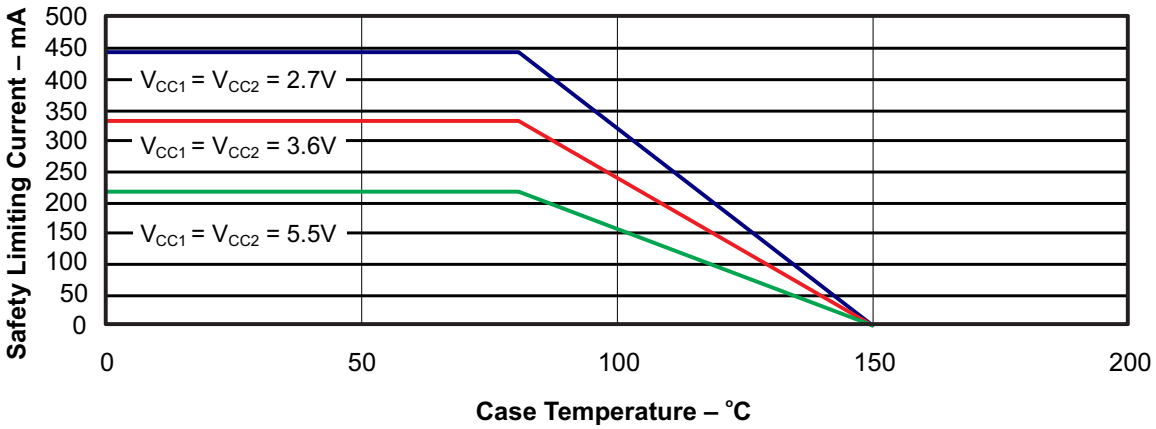

图 15. DBQ-16 θ_{JC} Thermal Derating Curve

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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8.3.1.2 Regulatory Information

VDE	UL	CSA	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1	Recognized under UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 61010-1	Certified according to GB 4943.1-2011
Basic Insulation Maximum Transient Overvoltage, 4242 V_{PK} Maximum Working Voltage, 566 V_{PK}	Single protection, 2500 V_{RMS} (1)	Reinforced Insulation per CSA 60950-1-03 and IEC 60950-1 (2nd Ed.), 185 V_{RMS} maximum working voltage Basic Insulation per CSA 60950-1-03 and IEC 60950-1 (2nd Ed.), 370 V_{RMS} maximum working voltage Reinforced Insulation per CSA 61010-1-12 and IEC 61010-1 (3rd Edition), 150 V_{RMS} maximum working voltage Basic Insulation per CSA 61010-1-12 and IEC 61010-1 (3rd Edition), 300 V_{RMS} maximum working voltage	Basic Insulation, Altitude ≤ 5000m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40016131	File number: E181974	Master contract number: 220991	Certificate number: CQC14001109540

(1) Production tested ≥ 3000 Vrms for 1 second in accordance with UL 1577.

8.4 Device Functional Modes

表 3. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	
				ISO71xxCC	ISO71xxFCC
PU	PU	H	H or open	H	H
		L	H or open	L	L
		X	L	Z	Z
		Open	H or open	H	L
PD	PU	X	H or open	H	L
PD	PU	X	L	Z	Z
PU	PD	X	X	Undetermined	Undetermined

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered Up (V_{CC} ≥ 2.7 V); PD = Powered Down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance

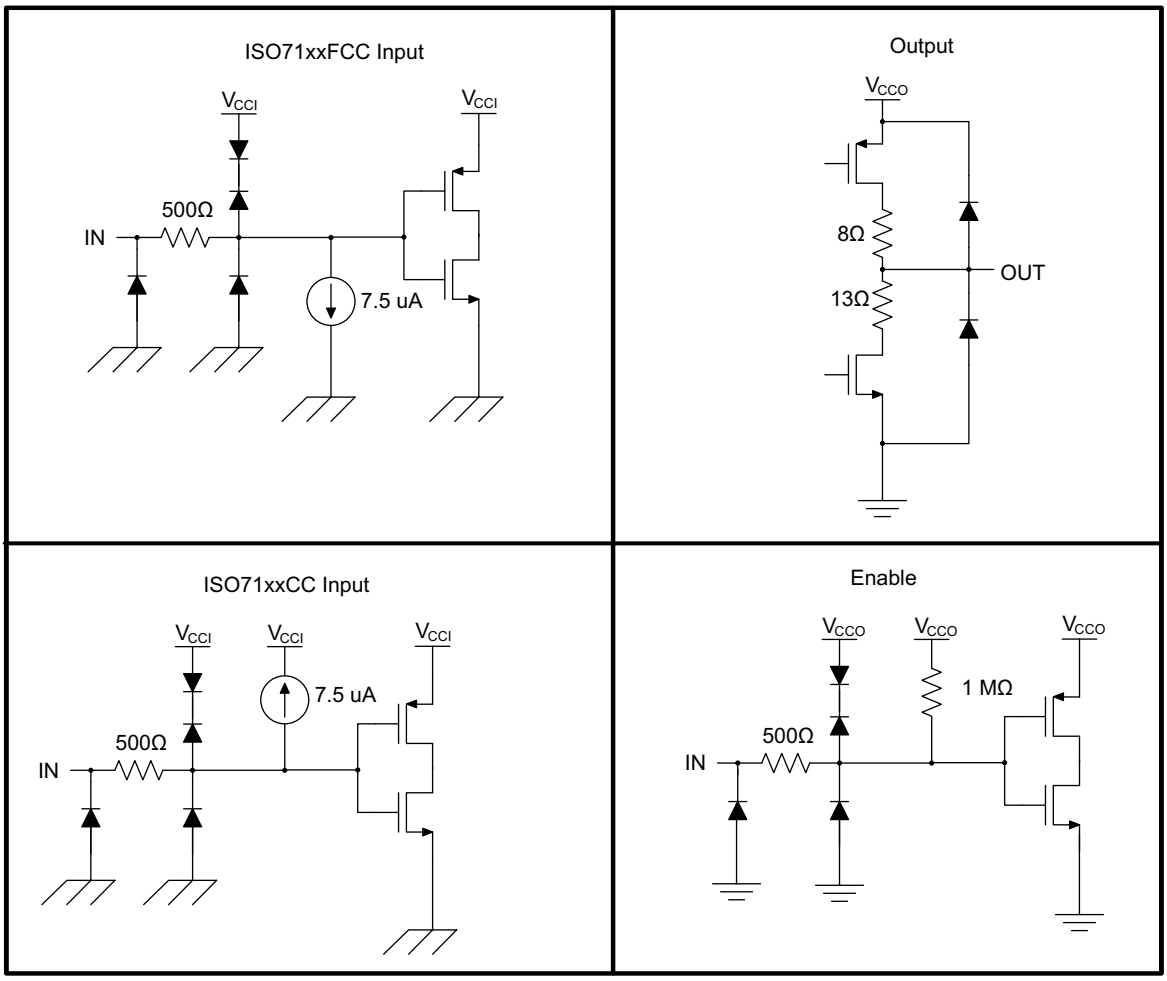

图 16. Device I/O Schematics

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

ISO71xx use single-ended TTL-logic switching technology. Its supply voltage range is from 3 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to note that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Applications

9.2.1 Isolated Data Acquisition System for Process Control

ISO71xx combined with TI's precision analog-to-digital converter and mixed signal micro-controller can create an advanced isolated data acquisition system as shown in 图 17.

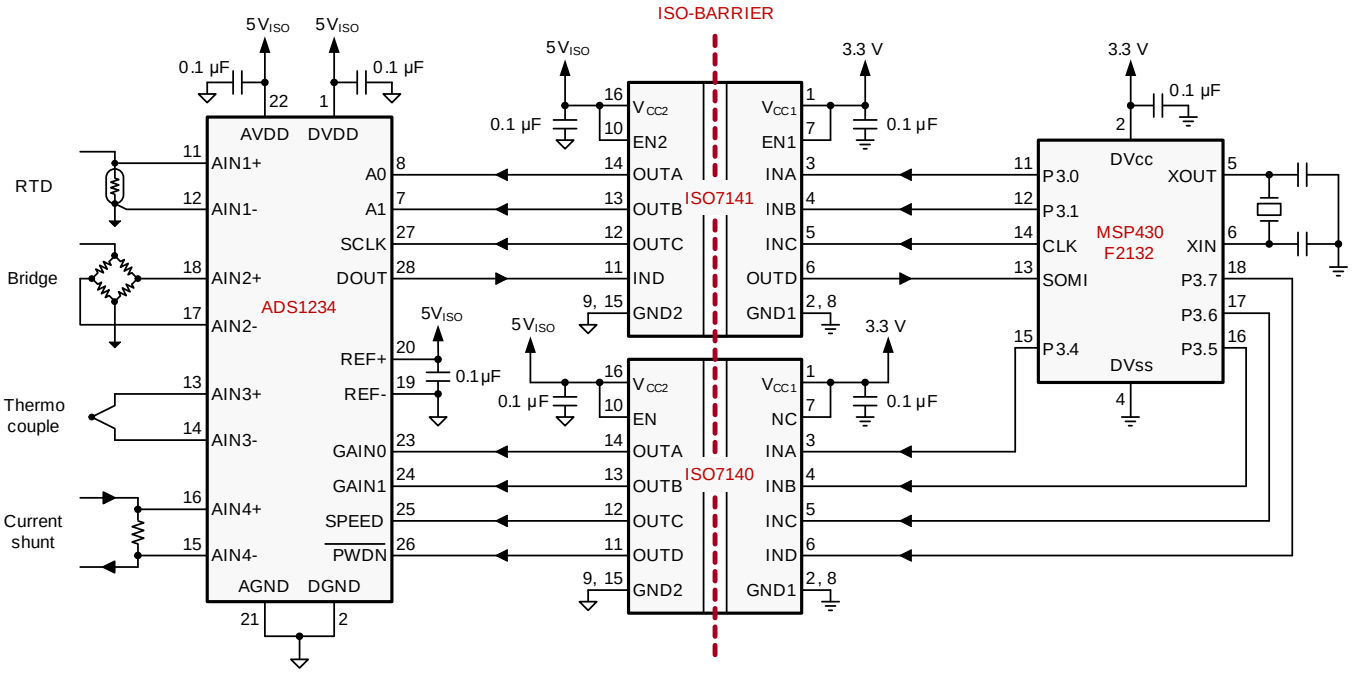

图 17. Isolated Data Acquisition System for Process Control

Typical Applications (接下页)

9.2.1.1 Design Requirements

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, ISO71xx only needs two external bypass capacitors to operate.

9.2.1.2 Detailed Design Procedure

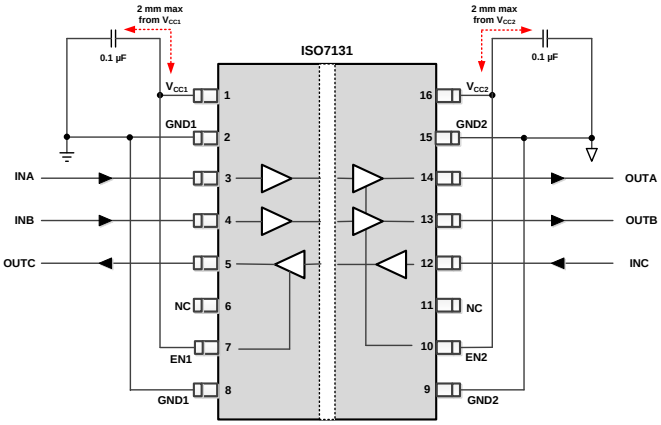

图 18. Typical ISO7131 Circuit Hook-up

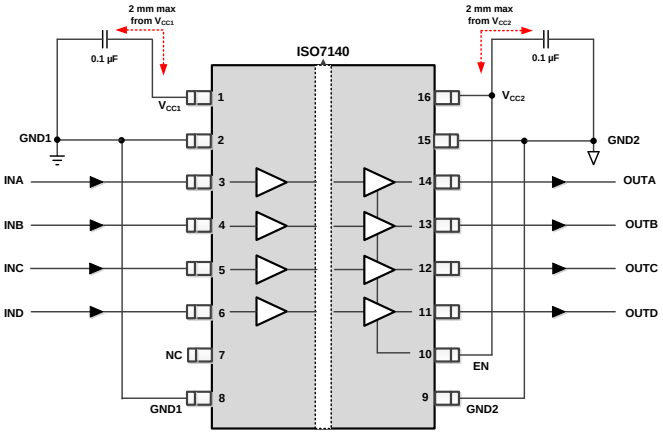

图 19. Typical ISO7140 Circuit Hook-up

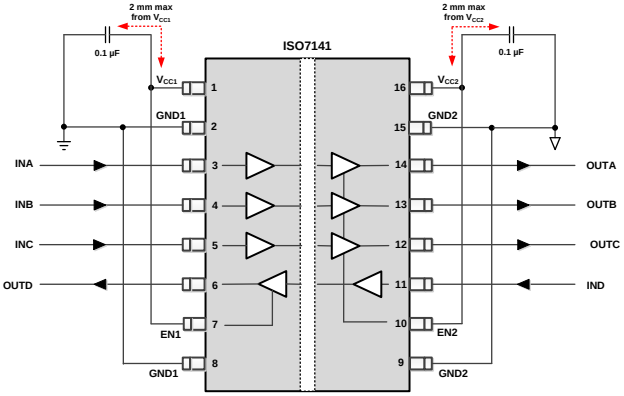

图 20. Typical ISO7141 Circuit Hook-up

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Typical Applications (接下页)

9.2.1.3 Application Curves

Typical eye diagrams of ISO71xx (see 图 21, 图 22, and 图 23) indicate low jitter and wide open eye at the maximum data rate.

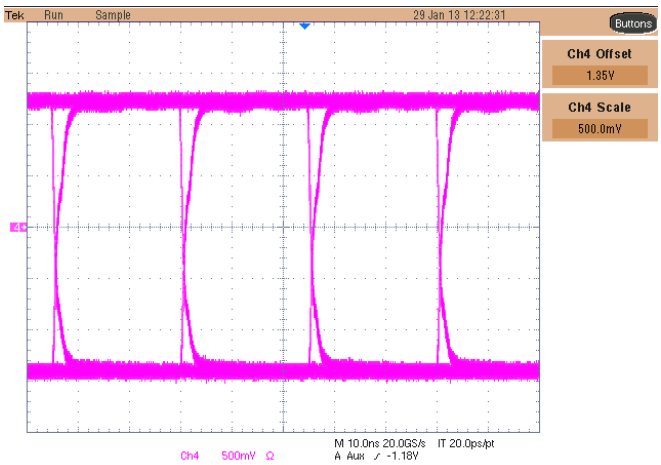

图 21. Typical Eye Diagram at 40 MBPS, PRBS 2^{16} - 1, 2.7-V Operation

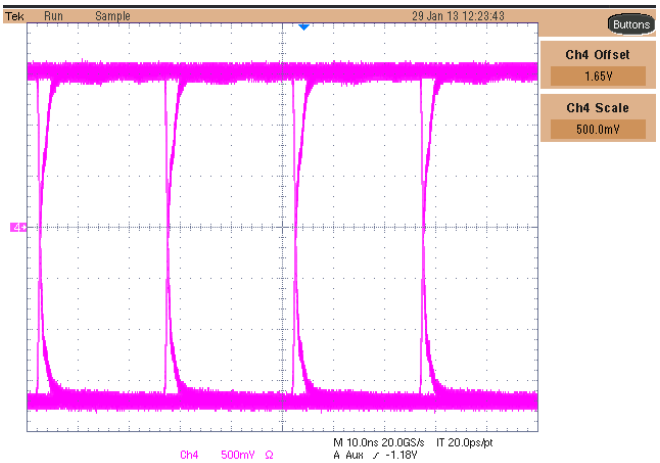

图 22. Typical Eye Diagram at 40 MBPS, PRBS 2^{16} - 1, 3.3-V Operation

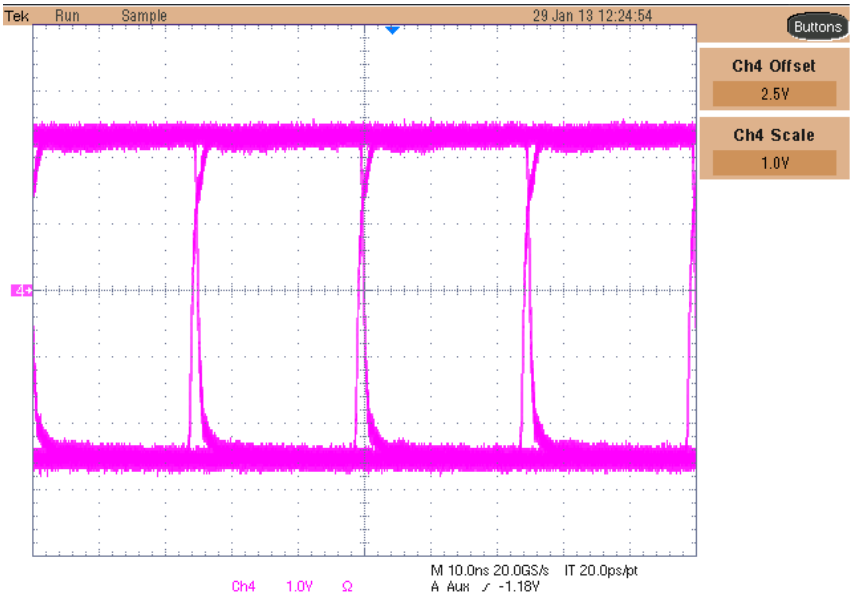

图 23. Typical Eye Diagram at 50 MBPS, PRBS 2^{16} - 1, 5-V Operation

Typical Applications (接下页)

9.2.2 Isolated RS-485 Interface

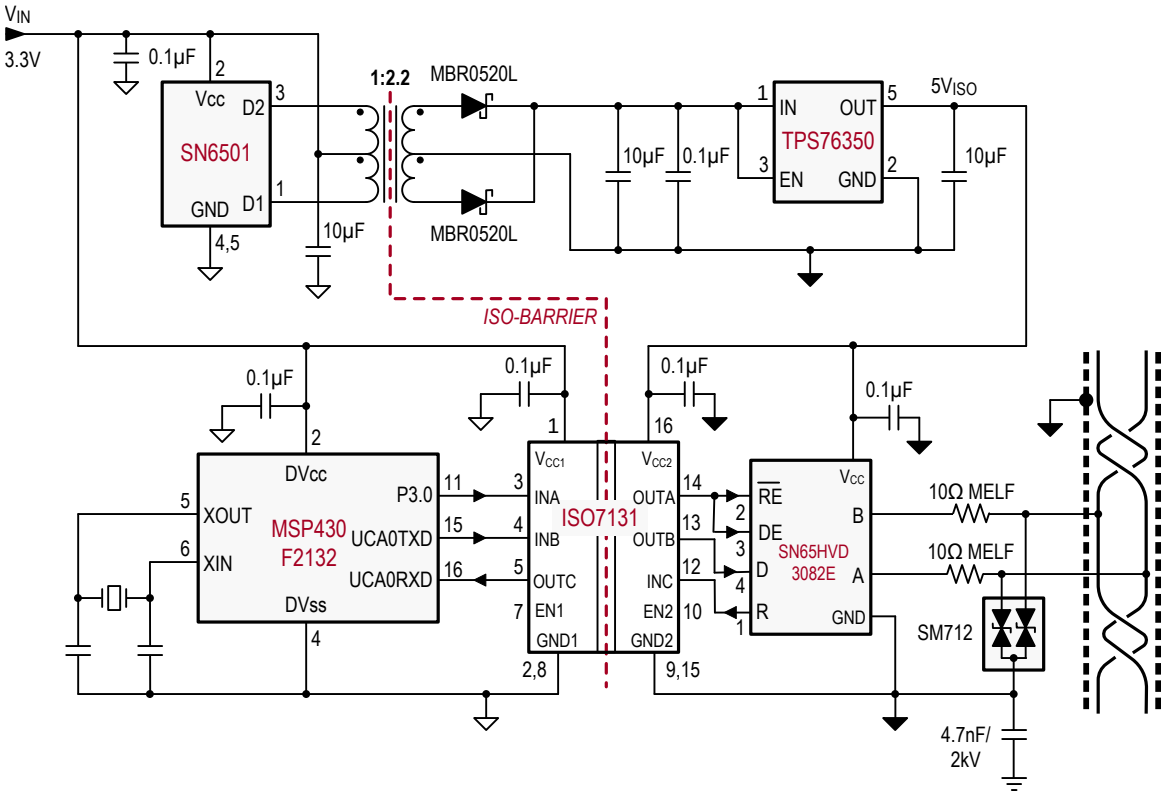

图 24. Isolated RS-485 Interface

9.2.2.1 Design Requirements

See previous *Design Requirements*.

9.2.2.2 Detailed Design Procedure

See previous *Detailed Design Procedure*.

9.2.2.3 Application Curves

See previous *Application Curves*.

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10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as TI's SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 图 25). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

11.2 Layout Example

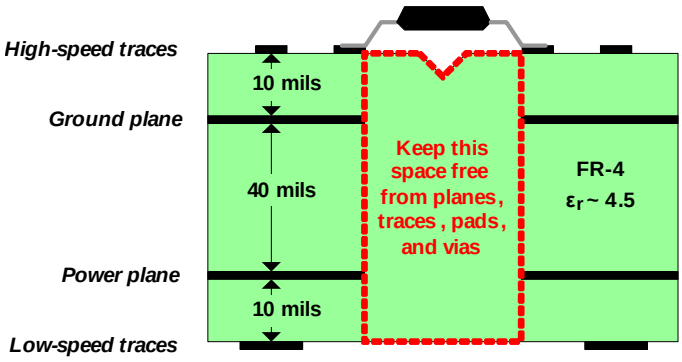

图 25. Recommended Layer Stack

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

- SLLA284，*《数字隔离器设计指南》*
- SLLSEA0，*《用于隔离电源的变压器驱动器》*

12.2 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 4. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
ISO7131CC	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7140CC	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7140FCC	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7141CC	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7141FCC	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 商标

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12.4 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

SLLA353 - *《隔离相关术语》*。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7131CCDBQ	ACTIVE	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7131CC	Samples
ISO7131CCDBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7131CC	Samples
ISO7140CCDBQ	ACTIVE	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7140CC	Samples
ISO7140CCDBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7140CC	Samples
ISO7140FCCDBQ	ACTIVE	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7140FC	Samples
ISO7140FCCDBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7140FC	Samples
ISO7141CCDBQ	ACTIVE	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7141CC	Samples
ISO7141CCDBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7141CC	Samples
ISO7141FCCDBQ	ACTIVE	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7141FC	Samples
ISO7141FCCDBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7141FC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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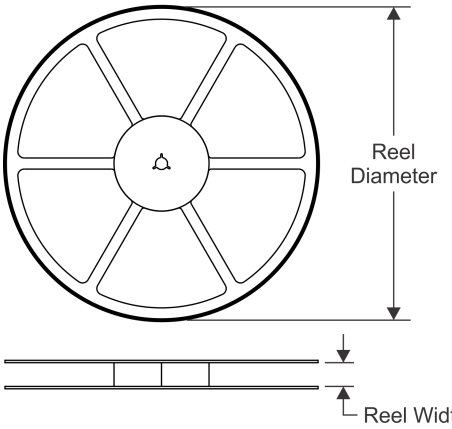
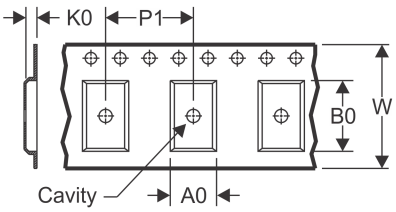
TAPE AND REEL INFORMATION

REEL DIMENSIONS

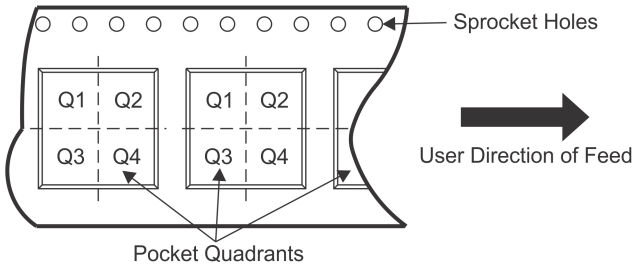


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

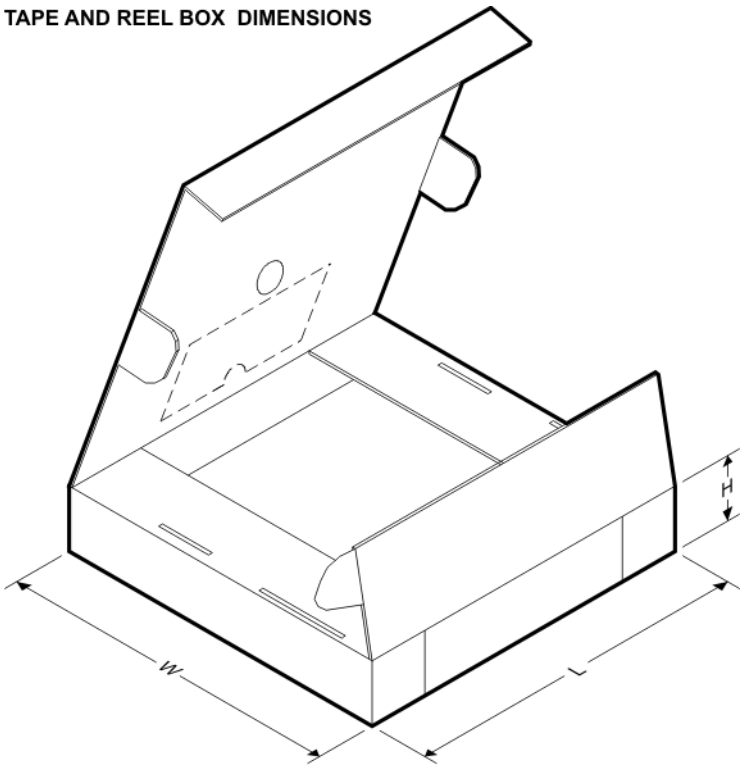
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7131CCDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7140CCDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7140FCCDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7141CCDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7141FCCDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

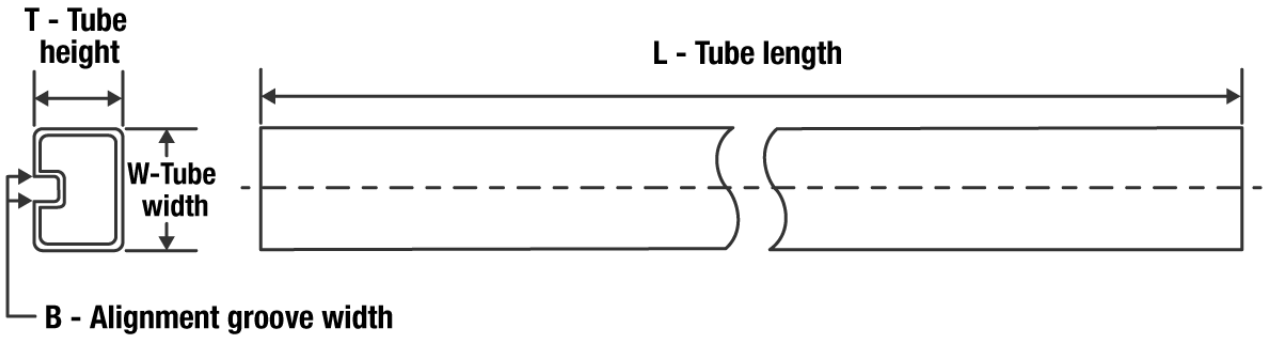
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

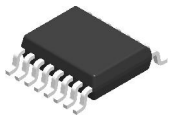
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7131CCDBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7140CCDBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7140FCCDBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7141CCDBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7141FCCDBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7131CCDBQ	DBQ	SSOP	16	75	505.46	6.76	3810	4
ISO7140CCDBQ	DBQ	SSOP	16	75	505.46	6.76	3810	4
ISO7140FCCDBQ	DBQ	SSOP	16	75	505.46	6.76	3810	4
ISO7141CCDBQ	DBQ	SSOP	16	75	505.46	6.76	3810	4
ISO7141FCCDBQ	DBQ	SSOP	16	75	505.46	6.76	3810	4

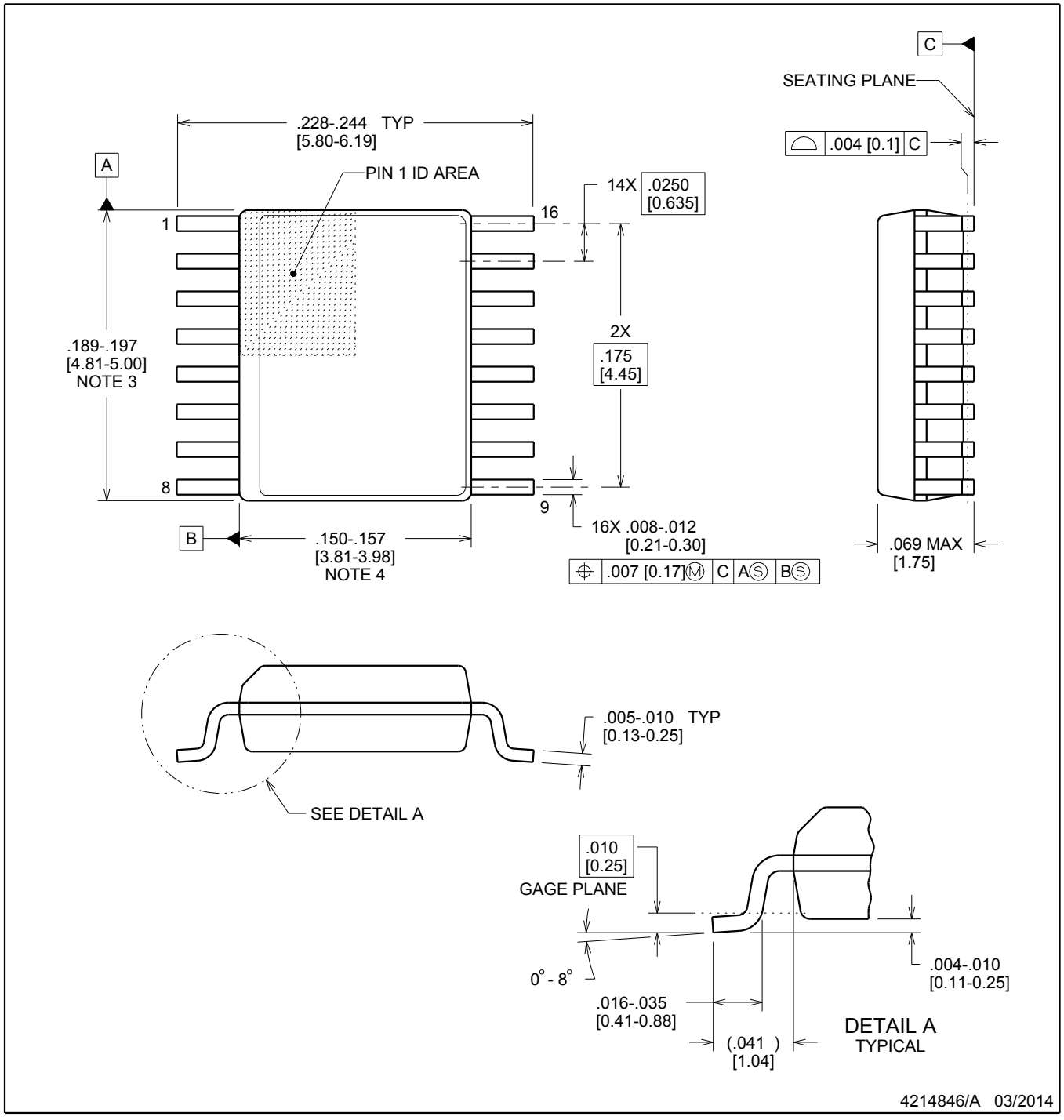


PACKAGE OUTLINE

DBQ0016A

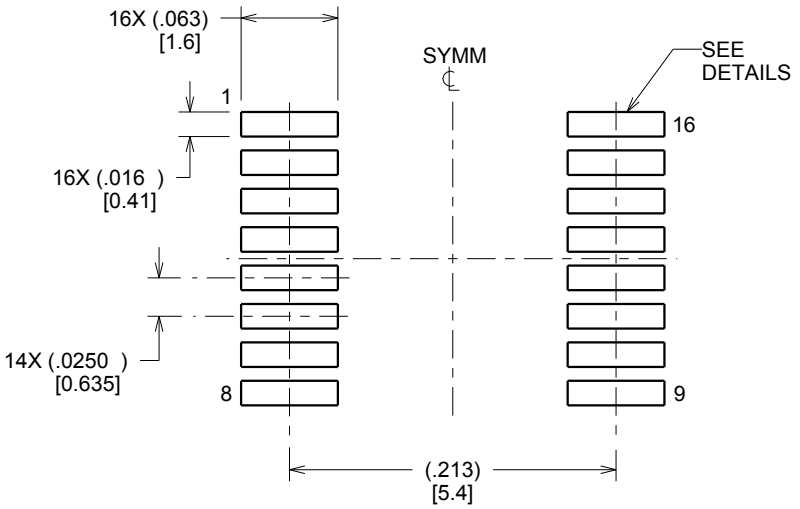
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

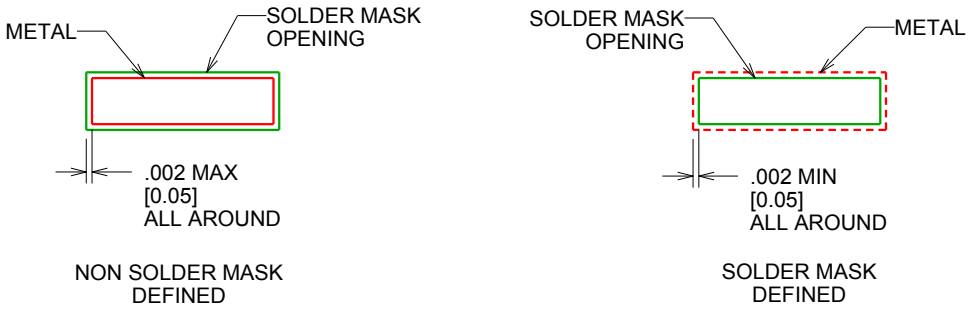


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

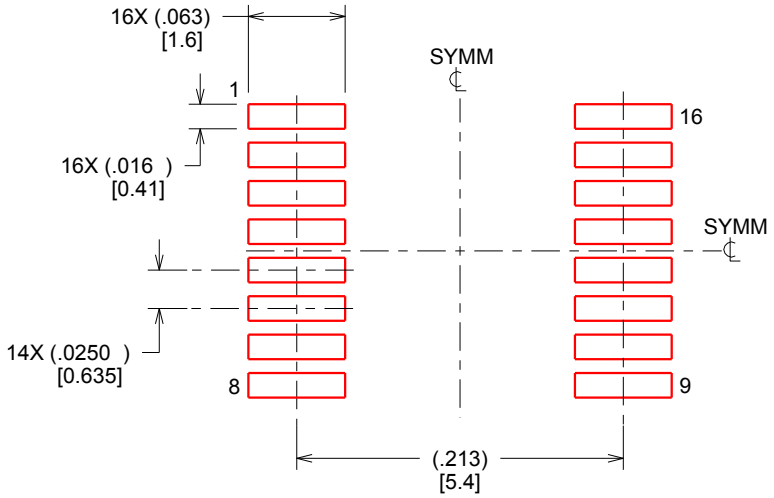
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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