AMC1300B-Q1 精密、±250mV 输入、增强型隔离放大器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1: – 40 ° C 至 125 ° C 、 T_A
- ±250mV 输入电压范围，针对使用分流电阻器测量电流进行了优化
- 固定增益：8.2
- 低直流误差：
  - 失调电压误差：±0.2mV（最大值）
  - 温漂±0.9μV/°C（最大值）
  - 增益误差：±0.3%（最大值）
  - 增益漂移：±30ppm/°C（最大值）
  - 非线性度：0.03%（最大值）
- 高侧和低侧以 3.3V 或 5V 电压运行
- 失效防护输出
- 高 CMTI：100kV/μs（最小值）
- 低 EMI，符合 CISPR-11 和 CISPR-25 标准
- 安全相关认证：
  - 7071-V_{PK} 增强型隔离，符合 DIN VDE V 0884-11：2017-01
  - 符合 UL1577 标准且长达 1 分钟的 5000V_{RMS} 隔离

2 应用

- 基于分流电阻器的电流感应，可用于：
  - HEV/EV 充电桩
  - HEV/EV 车载充电器 (OBC)
  - HEV/EV 直流/直流转换器
  - HEV/EV 牵引逆变器

3 说明

AMC1300B-Q1 是一款隔离式精密放大器，此放大器的输出与输入电路由抗电磁干扰性能极强的隔离栅隔开。该隔离栅经认证可提供高达 5kV_{RMS} 的增强型电隔离，符合 VDE V 0884-11 和 UL1577 标准，并且可支持最高 1.5kV_{RMS} 的工作电压。

该隔离栅可将系统中以不同共模电压电平运行的各器件隔开，并保护电压较低的器件免受高电压冲击。

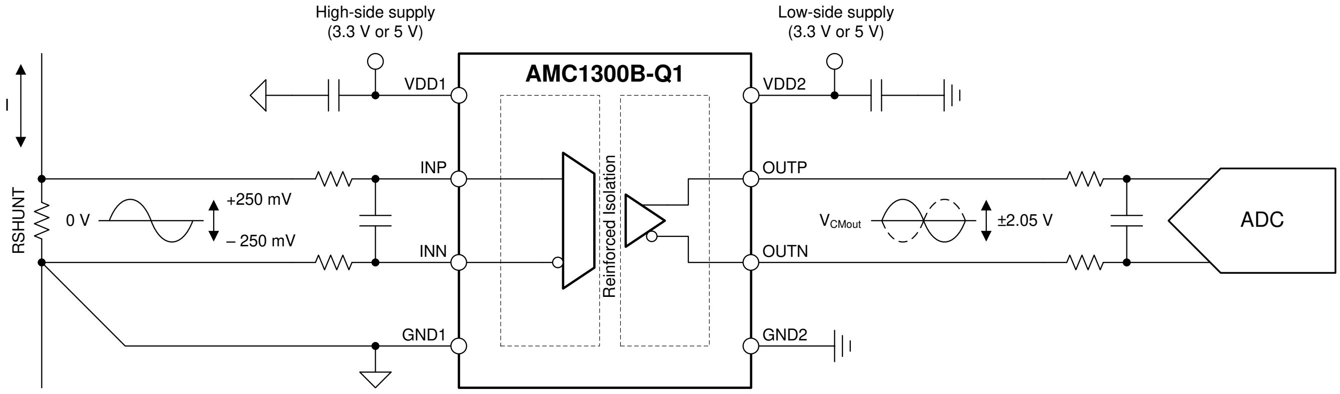
AMC1300B-Q1 的输入针对直接连接低阻抗分流电阻器或其他具有低信号电平的低阻抗电压源的情况进行了优化。出色的直流精度和低温漂支持在 –40°C 至 +125°C 的整个汽车温度范围内，在 PFC 级、直流/直流转换器、牵引逆变器和 OBC 中进行精确的电流控制。

集成的无分流器和无高侧电源检测功能可简化系统级设计和诊断。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
AMC1300B-Q1	SOIC (8)	5.85mm × 7.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用

English Data Sheet: SBASA40

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (April 2020) to Revision A (January 2021) — Page

- 1
- Changed CLR from ⩾8.5 mm to ⩾9 mm 6
- Changed TCV_{OS} from ±3 μV/°C to ±0.9 μV/°C 8
- Changed TCE_G from ±50 ppm/°C to ±30 ppm/°C 8
- Changed $VDD1_{UV}$ from 1.75 V (min) / 2.53 V (typ) / 2.7 V (max) to 2.4 V (min) / 2.6 V (typ) / 2.8 V (max) 8

5 Pin Configuration and Functions

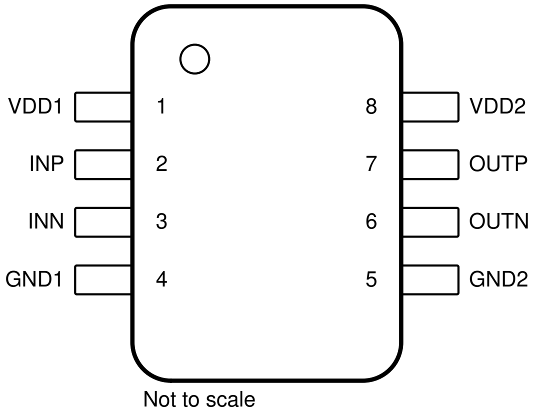


图 5-1. DWV Package, 8-Pin SOIC, Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply.(1)
2	INP	Analog input	Noninverting analog input. Either INP or INN must have a DC current path to GND1 to define the common-mode input voltage.(2)
3	INN	Analog input	Inverting analog input. Either INP or INN must have a DC current path to GND1 to define the common-mode input voltage.(2)
4	GND1	High-side ground	High-side analog ground.
5	GND2	Low-side ground	Low-side analog ground.
6	OUTN	Analog output	Inverting analog output.
7	OUTP	Analog output	Noninverting analog output.
8	VDD2	Low-side power	Low-side power supply.(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
(2) See the *Layout* section for details.

6 Specifications

6.1 Absolute Maximum Ratings

see(1)

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	–0.3	6.5	V
	Low-side VDD2 to GND2	–0.3	6.5	
Analog input voltage	INP, INN	GND1 – 6	VDD1 + 0.5	V
Output voltage	OUTP, OUTN	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* table. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1), HBM ESD classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification Level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-side power supply	VDD1 to GND1	3	5	5.5	V
	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} - V_{INN}$		±320		mV
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{INP} - V_{INN}$	–250		250	mV
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN}) / 2$ to GND1	–0.16		VDD1 – 2.1	V
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		AMC1300B-Q1	UNIT
		DWV (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	99	mW
P_{D1}	Maximum power dissipation (high-side)	VDD1 = 3.6 V	31	mW
		VDD1 = 5.5 V	54	
P_{D2}	Maximum power dissipation (low-side)	VDD2 = 3.6 V	26	mW
		VDD2 = 5.5 V	45	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	$\geq$ 9	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	$\geq$ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	$\geq$ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	$\geq$ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage $\leq$ 600 V_{RMS}	I-IV	
		Rated mains voltage $\leq$ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11 (VDE V 0884-11): 2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2121	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V_{RMS}
		At DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7071	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	8485	
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroups 2 and 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	$\leq$ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	$\leq$ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	$\leq$ 5	
C_{IO}	Barrier capacitance, input to output(5)	$V_{IO} = 0.5\ V_{PP}$ at 1 MHz	~1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V at 100°C $\leq T_A \leq$ 125°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000\ V_{RMS}$ or 7071 V_{DC}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	Certificate number: E181974

6.8 Safety Limiting Values

Safety limiting[1] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 85.4°C/W, VDDx = 5.5 V, T_J = 150°C, T_A = 25°C			266	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 85.4°C/W, VDDx = 3.6 V, T_J = 150°C, T_A = 25°C			407	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 85.4°C/W, T_J = 150°C, T_A = 25°C			1464	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

6.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = –250 mV to +250 mV, and INN = GND1; typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{CMov}	Common-mode overvoltage detection level	$(V_{INP} + V_{INN})$ / 2 to GND1	VDD1 – 2			V
	Hysteresis of common-mode overvoltage detection level			60		mV
V_{OS}	Input offset voltage(1)	Initial, at T_A = 25°C, INP = INN = GND1	–0.2	±0.01	0.2	mV
TCV_{OS}	Input offset drift(1)		–0.9	±0.1	0.9	μV/°C
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min} \leqslant V_{CM} \leqslant V_{CM\ max}$		–100		dB
		f_{IN} = 10 kHz, $V_{CM\ min} \leqslant V_{CM} \leqslant V_{CM\ max}$		–98		
R_{IN}	Single-ended input resistance	INN = GND1		19		kΩ
R_{IND}	Differential input resistance			22		kΩ
I_{IB}	Input bias current	INP = INN = GND1; $I_{IB} = (I_{IBP} + I_{IBN}) / 2$	–41	–30	–24	μA
I_{IO}	Input offset current	$I_{IO} = I_{IBP} – I_{IBN}$; INP = INN = GND1		±5		nA
C_{IN}	Single-ended input capacitance	INN = GND1, f_{IN} = 275 kHz		2		pF
C_{IND}	Differential input capacitance	f_{IN} = 275 kHz		1		pF
ANALOG OUTPUT						
	Nominal gain			8.2		
E_G	Gain error(1)	at T_A = 25°C	–0.3%	±0.04%	0.3%	
TCE_G	Gain drift(1)		–30	±5	30	ppm/°C
	Nonlinearity(1)		–0.03%	±0.01%	0.03%	
THD	Total harmonic distortion	f_{IN} = 10 kHz		–85		dB
	Output noise	INP = INN = GND1, f_{IN} = 0 Hz, BW = 100 kHz brickwall filter		230		μV_{RMS}
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, BW = 10 kHz	81.5	85		dB
		f_{IN} = 10 kHz, BW = 100 kHz		72		
PSRR	Power-supply rejection ratio(2)	PSRR vs VDD1, at DC		–103		dB
		PSRR vs VDD1, 100-mV and 10-kHz ripple		–96		
		PSRR vs VDD2, at DC		–106		
		PSRR vs VDD2, 100-mV and 10-kHz ripple		–86		
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{CLIPout}$	Clipping differential output voltage	$V_{OUT} = (V_{OUTP} – V_{OUTN})$; $\lvert V_{IN}\rvert = \lvert V_{INP} – V_{INN}\rvert > \lvert V_{Clipping}\rvert$	–2.52	±2.49	2.52	V
$V_{Failsafe}$	Failsafe differential output voltage	$V_{CM} \geqslant V_{CMov}$, or VDD1 missing	–2.63	–2.57	–2.53	V
BW	Output bandwidth		250	310		kHz
R_{OUT}	Output resistance	On OUTP or OUTN		< 0.2		Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, INN = INP = GND1, outputs shorted to either GND2 or VDD2		14		mA
CMTI	Common-mode transient immunity	$\lvert GND1 – GND2\rvert$ = 1 kV	100	150		kV/μs

6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = –250 mV to +250 mV, and INN = GND1; typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
$VDD1_{UV}$	VDD1 undervoltage detection threshold voltage	VDD1 falling	2.4	2.6	2.8	V
IDD1	High-side supply current	$3.0\ V \leqslant VDD1 \leqslant 3.6\ V$		6.3	8.5	mA
		$4.5\ V \leqslant VDD1 \leqslant 5.5\ V$		7.2	9.8	
IDD2	Low-side supply current	$3.0\ V \leqslant VDD2 \leqslant 3.6\ V$		5.3	7.2	mA
		$4.5\ V \leqslant VDD2 \leqslant 5.5\ V$		5.9	8.1	

(1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
(2) This parameter is input referred.

6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.3		μs
t_f	Output signal fall time			1.3		μs
	V_{INx} to V_{OUTx} signal delay (50% - 10%)	Unfiltered output		1	1.5	μs
	V_{INx} to V_{OUTx} signal delay (50% - 50%)	Unfiltered output		1.6	2.1	μs
	V_{INx} to V_{OUTx} signal delay (50% - 90%)	Unfiltered output		2.5	3	μs
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 $\geqslant$ 3.0 V, to V_{OUTP}, V_{OUTN} valid, 0.1% settling		500		μs

6.11 Timing Diagram

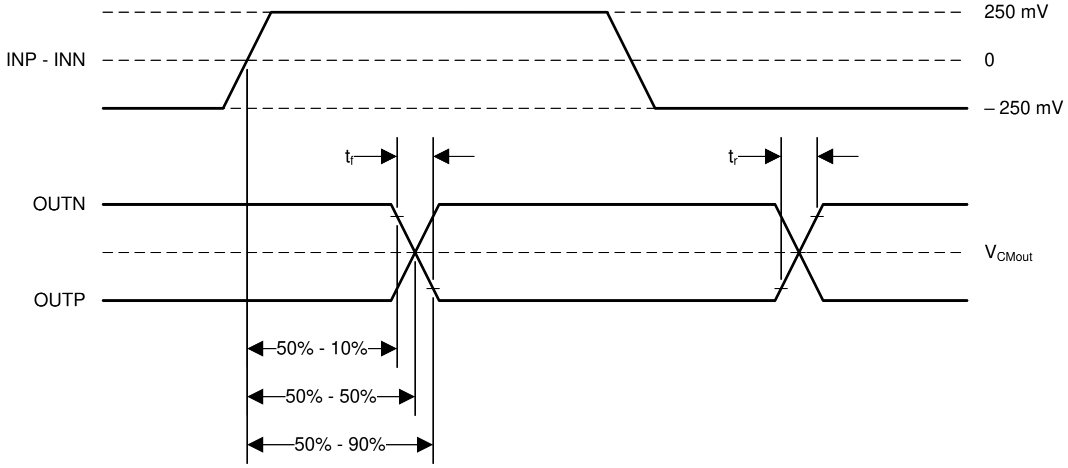


图 6-1. Rise, Fall, and Delay Time Definition

6.12 Insulation Characteristics Curves

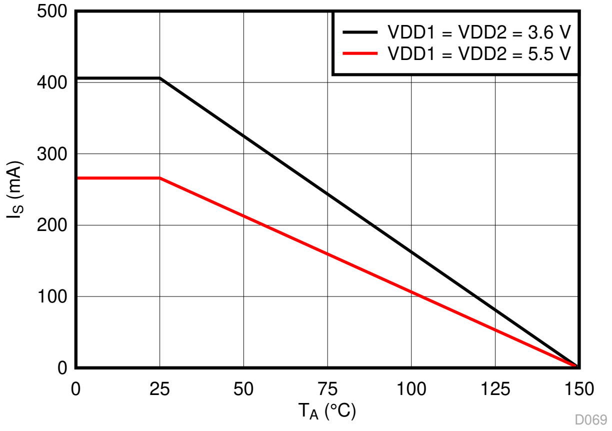


图 6-2. Thermal Derating Curve for Safety-Limiting Current per VDE

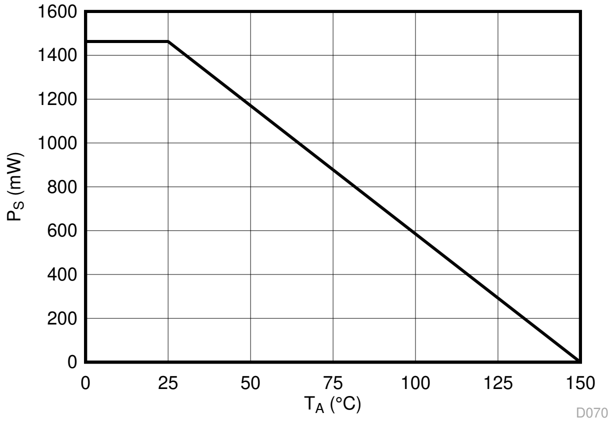
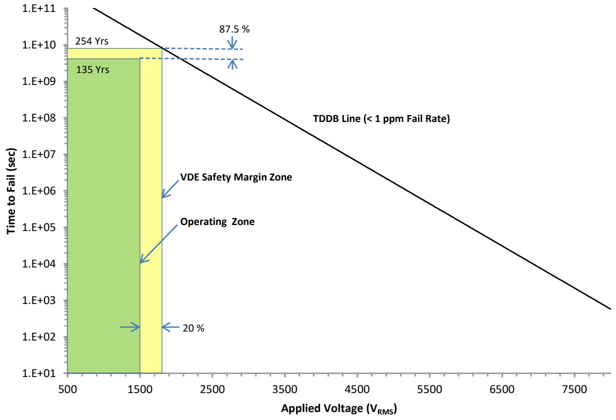


图 6-3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz, isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 year

图 6-4. Reinforced Isolation Capacitor Lifetime Projection

6.13 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, INP = –250 mV to 250 mV, INN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

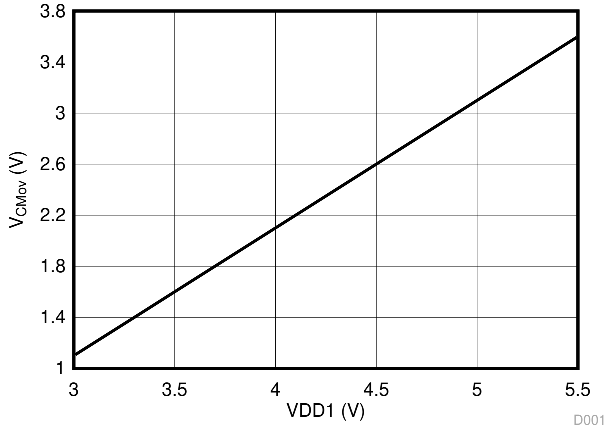


图 6-5. Common-Mode Overvoltage Detection Level vs High-Side Supply Voltage

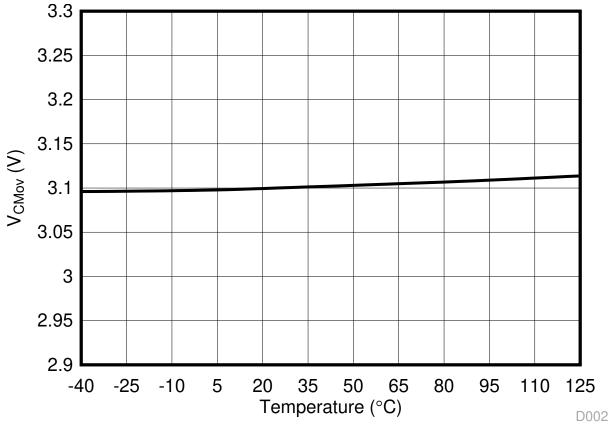


图 6-6. Common-Mode Overvoltage Detection Level vs Temperature

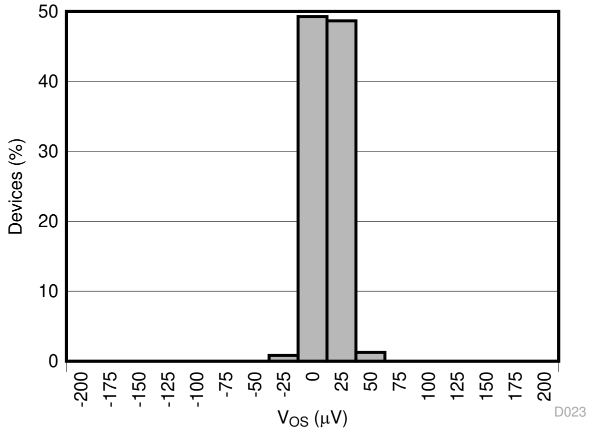


图 6-7. Input Offset Voltage Histogram

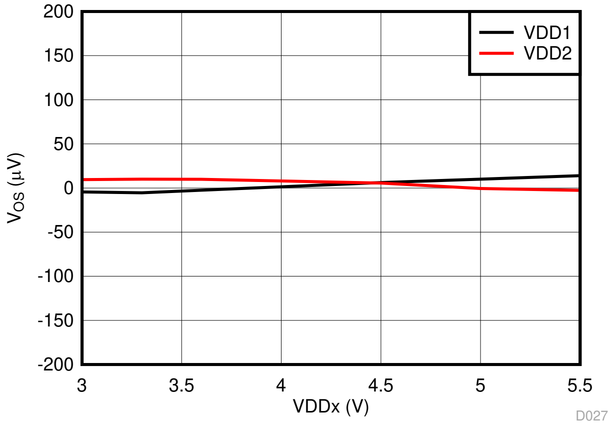


图 6-8. Input Offset Voltage vs Supply Voltage

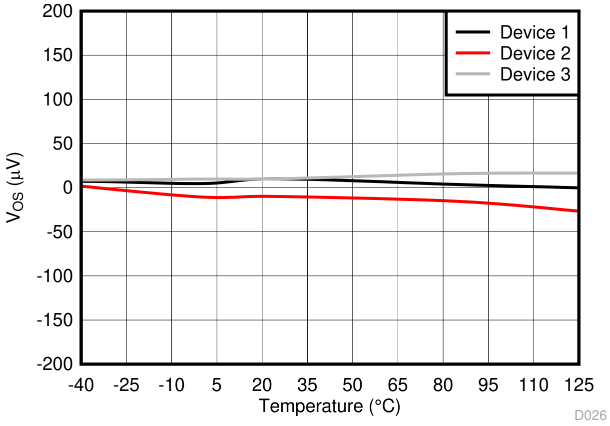


图 6-9. Input Offset Voltage vs Temperature

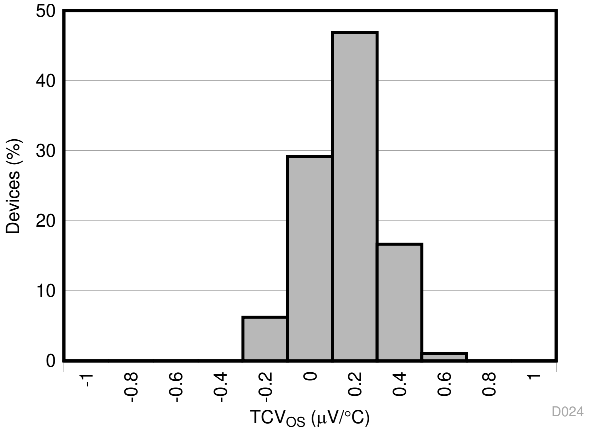


图 6-10. Input Offset Drift Histogram

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = –250 mV to 250 mV, INN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

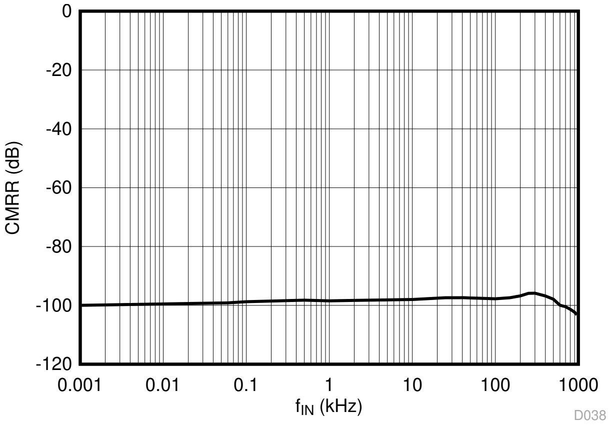


图 6-11. Common-Mode Rejection Ratio vs Input Frequency

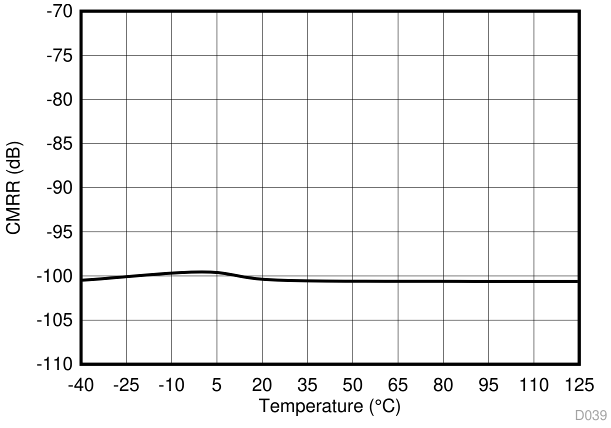


图 6-12. Common-Mode Rejection Ratio vs Temperature

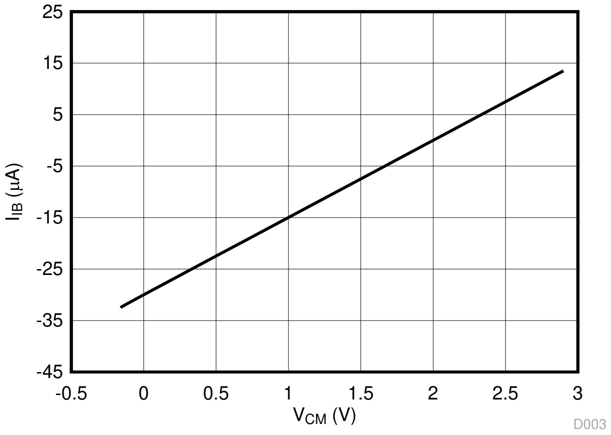


图 6-13. Input Bias Current vs Common-Mode Input Voltage

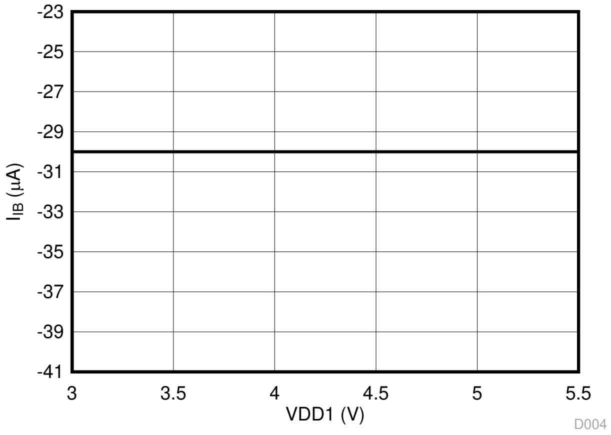


图 6-14. Input Bias Current vs High-Side Supply Voltage

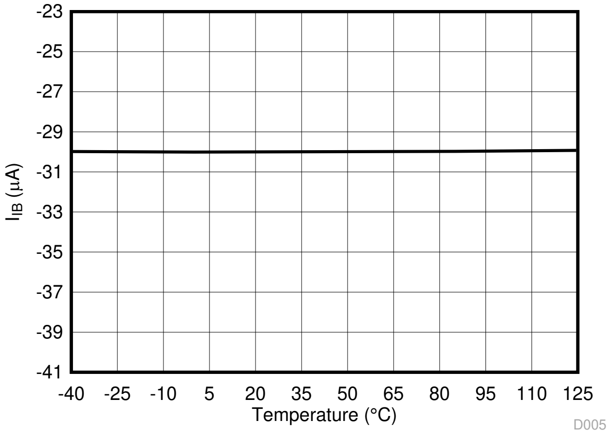


图 6-15. Input Bias Current vs Temperature

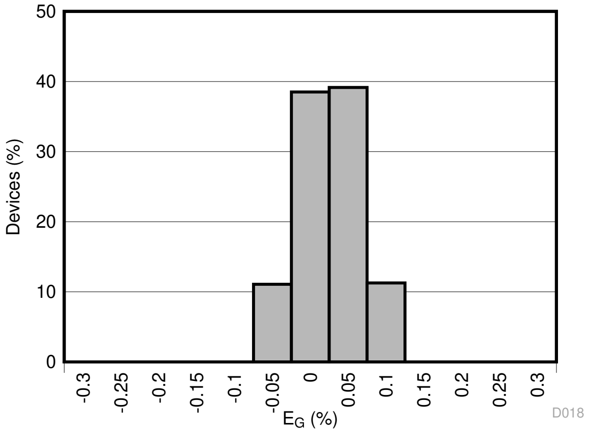


图 6-16. Gain Error Histogram

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = –250 mV to 250 mV, INN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

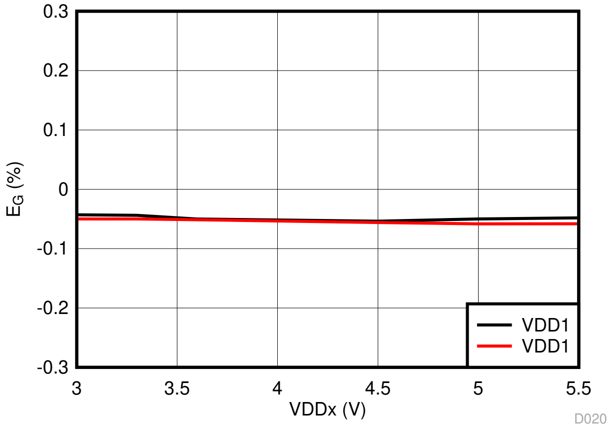


图 6-17. Gain Error vs Supply Voltage

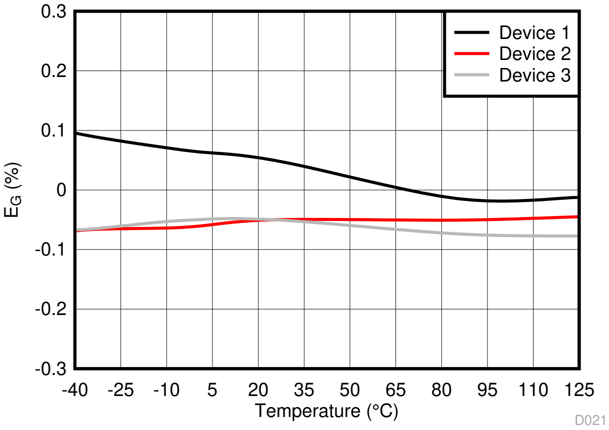


图 6-18. Gain Error vs Temperature

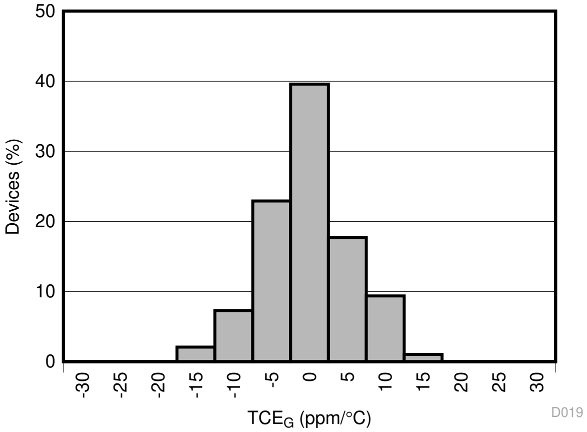


图 6-19. Gain Error Drift Histogram

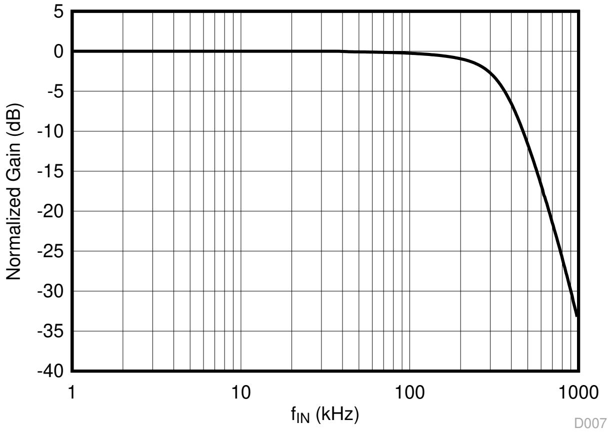


图 6-20. Normalized Gain vs Input Frequency

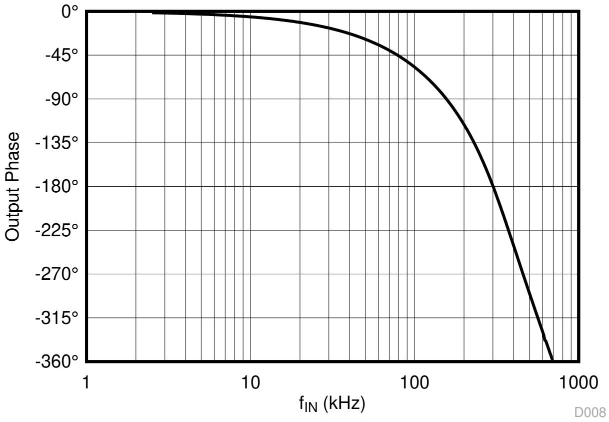


图 6-21. Output Phase vs Input Frequency

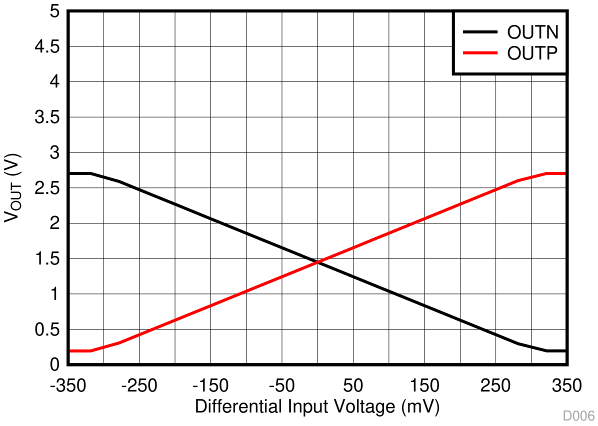


图 6-22. Output Voltage vs Input Voltage

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = –250 mV to 250 mV, INN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

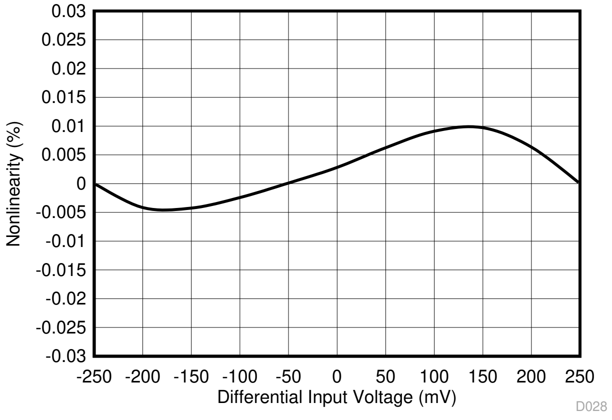


图 6-23. Nonlinearity vs Input Voltage

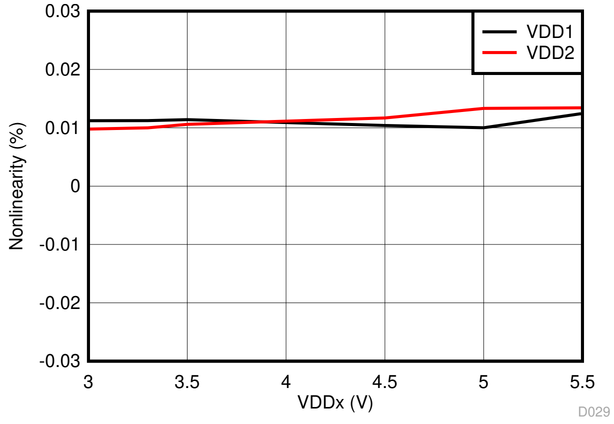


图 6-24. Nonlinearity vs Supply Voltage

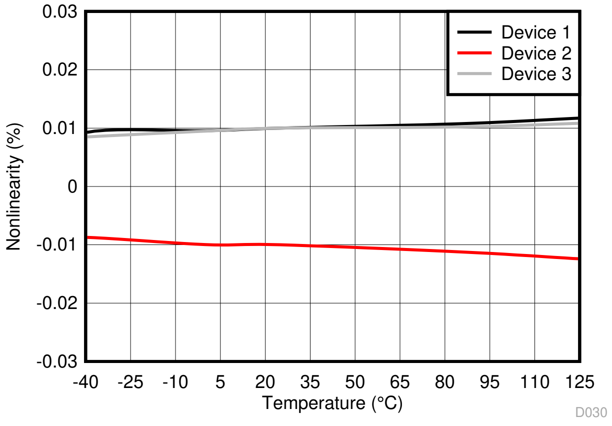


图 6-25. Nonlinearity vs Temperature

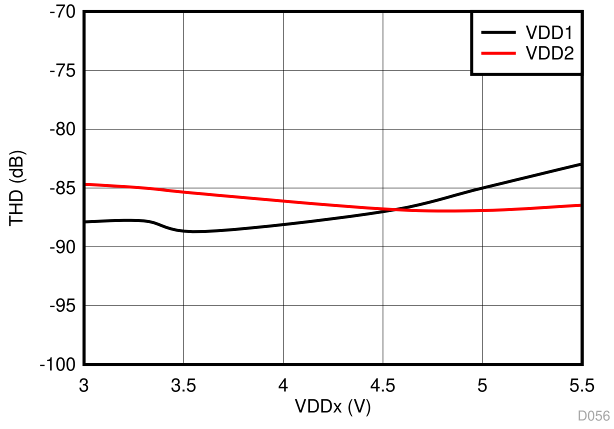


图 6-26. Total Harmonic Distortion vs Supply Voltage

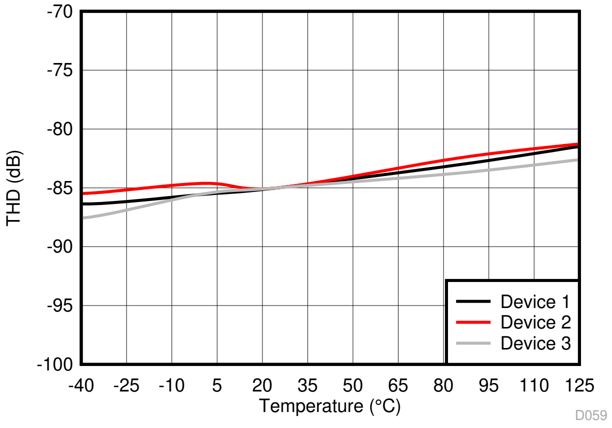


图 6-27. Total Harmonic Distortion vs Temperature

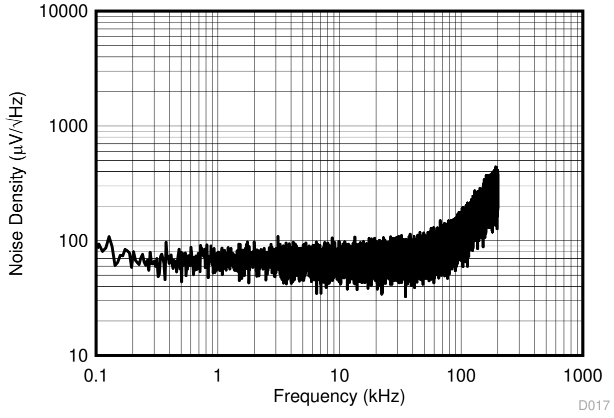


图 6-28. Input-Referred Noise Density vs Frequency

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = –250 mV to 250 mV, INN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

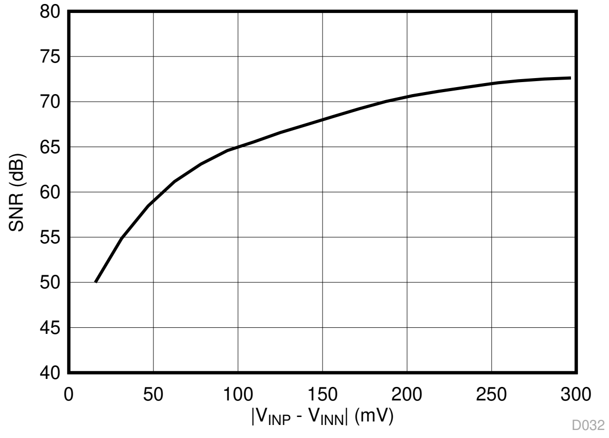


图 6-29. Signal-to-Noise Ratio vs Input Voltage

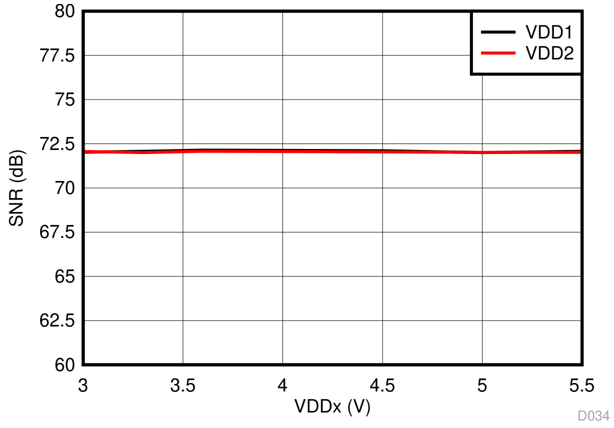


图 6-30. Signal-to-Noise Ratio vs Supply Voltage

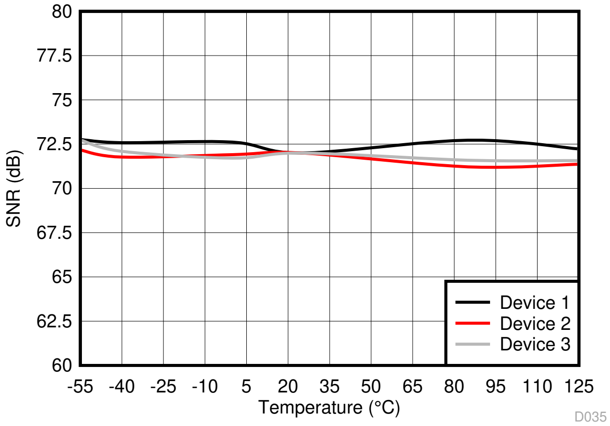


图 6-31. Signal-to-Noise Ratio vs Temperature

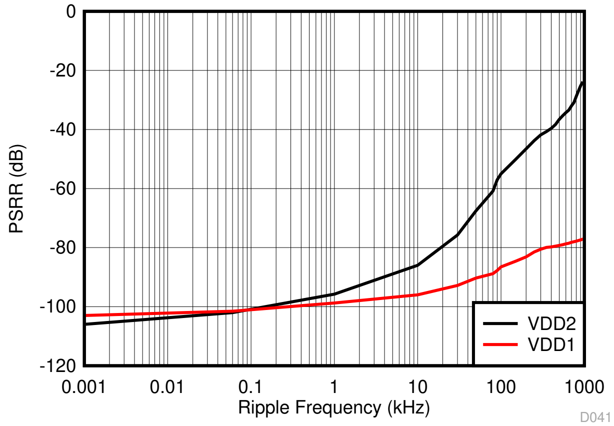


图 6-32. Power-Supply Rejection Ratio vs Ripple Frequency

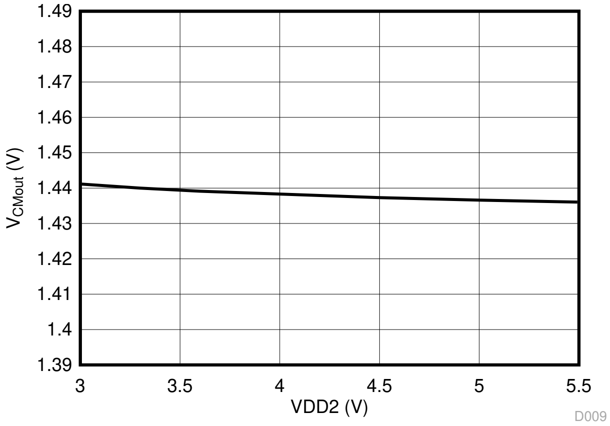


图 6-33. Output Common-Mode Voltage vs Low-Side Supply Voltage

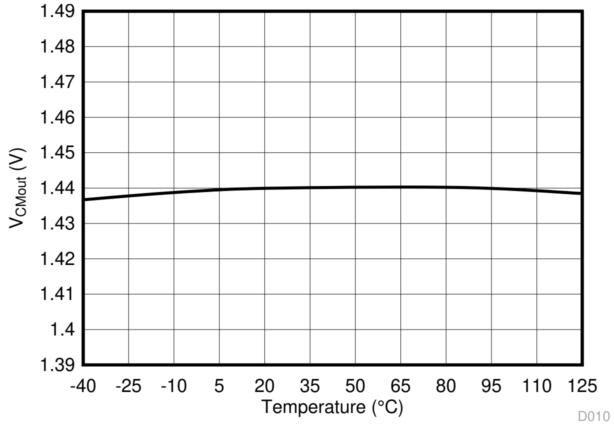


图 6-34. Output Common-Mode Voltage vs Temperature

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = –250 mV to 250 mV, INN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

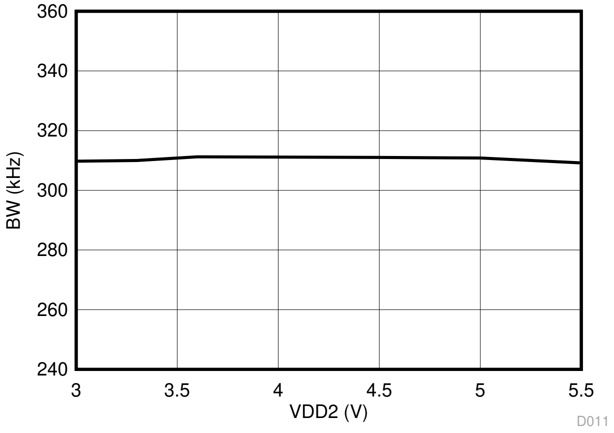


图 6-35. Output Bandwidth vs Low-Side Supply Voltage

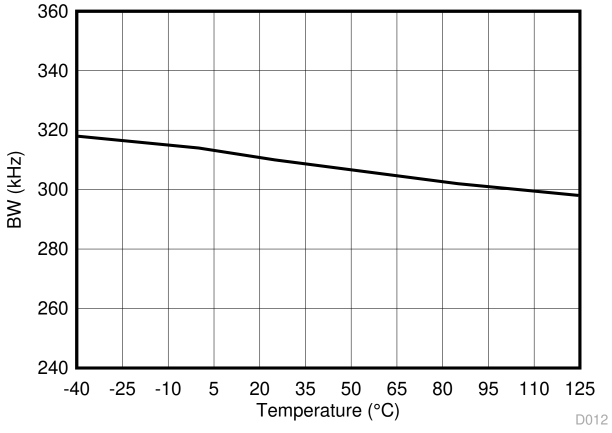


图 6-36. Output Bandwidth vs Temperature

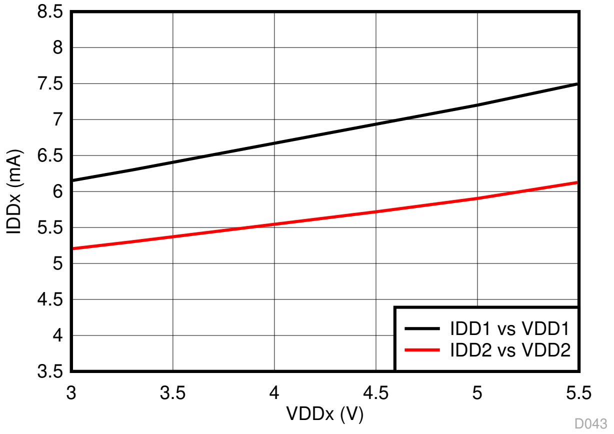


图 6-37. Supply Current vs Supply Voltage

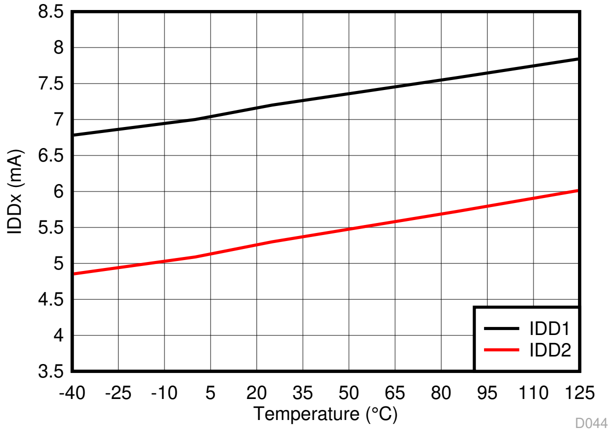


图 6-38. Supply Current vs Temperature

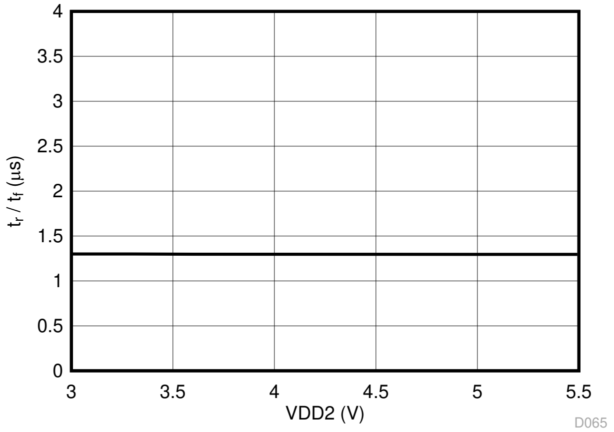


图 6-39. Output Rise and Fall Time vs Low-Side Supply

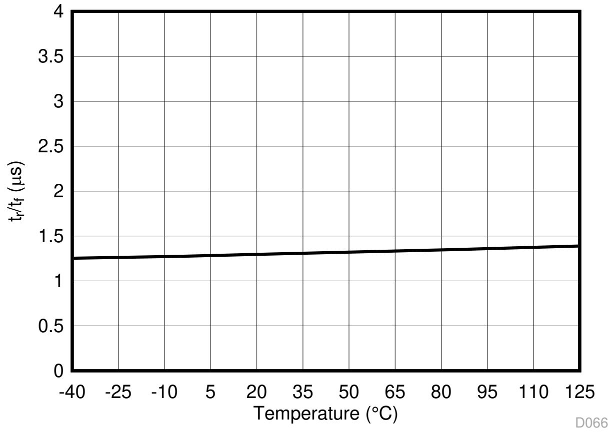


图 6-40. Output Rise and Fall Time vs Temperature

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = –250 mV to 250 mV, INN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

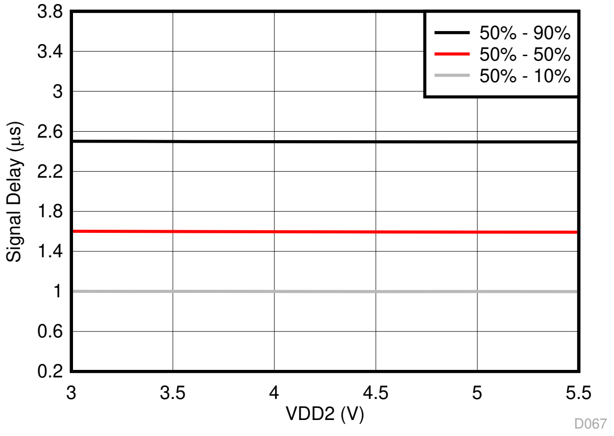


图 6-41. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

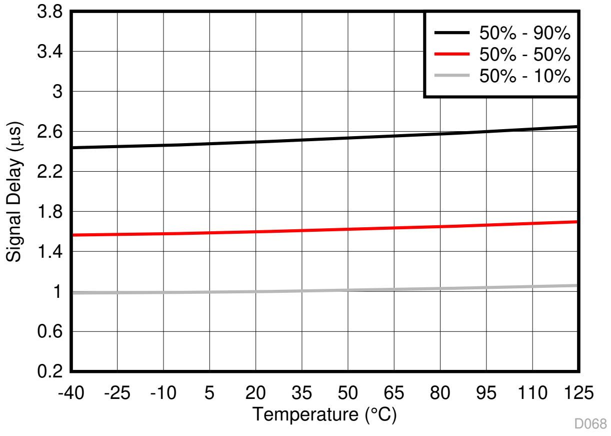


图 6-42. V_{IN} to V_{OUT} Signal Delay vs Temperature

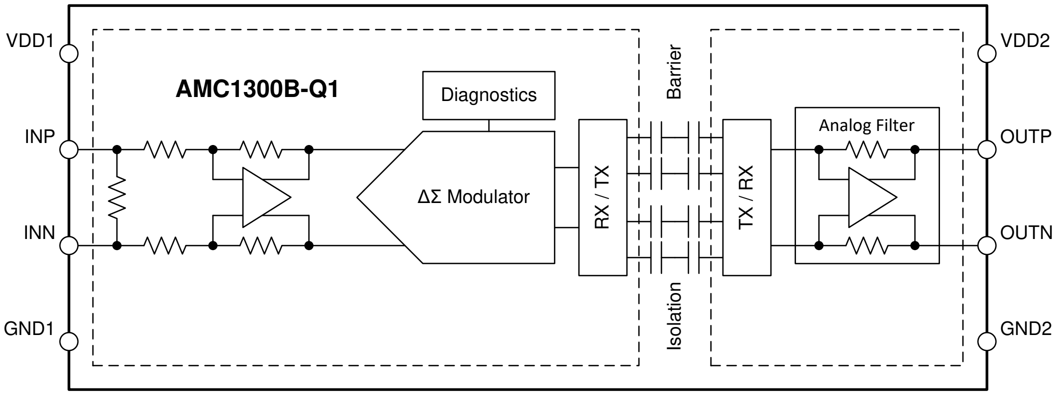
7 Detailed Description

7.1 Overview

The AMC1300B-Q1 is a fully differential, precision, isolated amplifier. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins that is proportional to the input signal.

The SiO_2-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report. The digital modulation used in the AMC1300B-Q1 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and common-mode transient immunity.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The differential amplifier input stage of the AMC1300B-Q1 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of R_{IND}. The modulator converts the analog input signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signals INP and INN. First, if the input voltages V_{INP} or V_{INN} exceed the range specified in the *Absolute Maximum Ratings* table, the input currents must be limited to the absolute maximum value, because the electrostatic discharge (ESD) protection turns on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within the linear full-scale range (V_{FSR}) and within the common-mode input voltage range (V_{CM}) as specified in the *Recommended Operating Conditions* table.

7.3.2 Isolation Channel Signal Transmission

The AMC1300B-Q1 uses an on-off keying (OOK) modulation scheme, as shown in 图 7-1, to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1300B-Q1 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the 4th-order analog filter. The AMC1300B-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

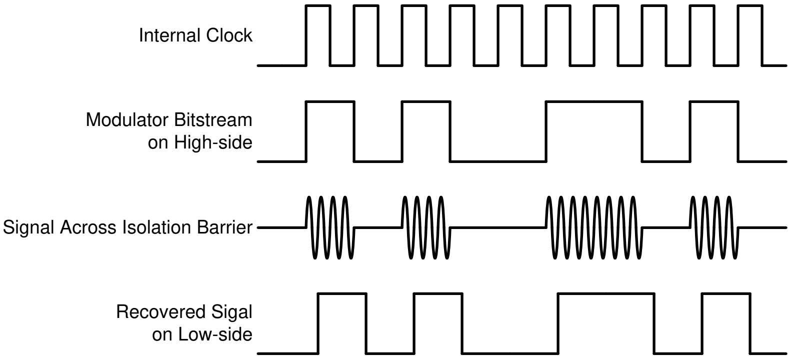


图 7-1. OOK-Based Modulation Scheme

7.3.3 Analog Output

The AMC1300B-Q1 offers a differential analog output comprised of the OUTP and OUTN pins. For differential input voltages (V_{INP} – V_{INN}) in the range from –250 mV to 250 mV, the device provides a linear response with a nominal gain of 8.2. For example, for a differential input voltage of 250 mV, the differential output voltage (V_{OUTP} – V_{OUTN}) is 2.05 V. At zero input (INP shorted to INN), both pins output the same common-mode output voltage V_{CMout}, as specified in the *Electrical Characteristics* table. For absolute differential input voltages greater than 250 mV but less than 320 mV, the differential output voltage continues to increase in magnitude but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in 图 7-2, if the differential input voltage exceeds the $V_{Clipping}$ value.

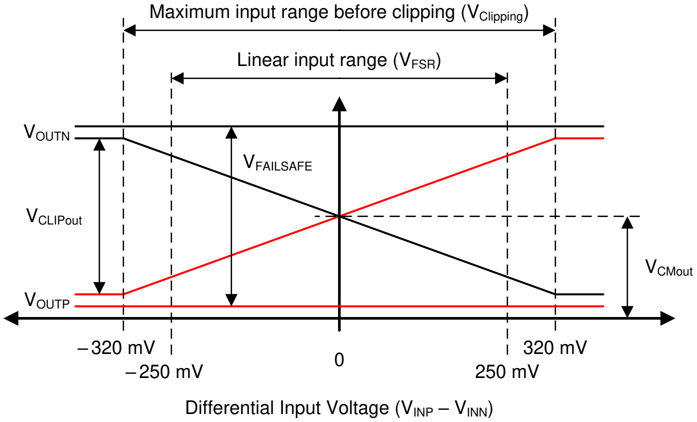


图 7-2. Output Behavior of the AMC1300B-Q1

The AMC1300B-Q1 offers a failsafe feature that simplifies diagnostics on system level. 图 7-2 shows the failsafe mode, in which the AMC1300B-Q1 outputs a negative differential output voltage that does not occur under normal operating conditions. The failsafe output is active in two cases:

- When the high-side supply is missing or below the $VDD1_{UV}$ threshold
- When the common-mode input voltage, that is $V_{CM} = (V_{INP} + V_{INN}) / 2$, exceeds the common-mode overvoltage detection level V_{CMov}

Use the maximum $V_{FAILSAFE}$ voltage specified in the *Electrical Characteristics* table as a reference value for failsafe detection on system level.

7.4 Device Functional Modes

The AMC1300B-Q1 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the *Recommended Operating Conditions* table.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The low analog input voltage range, excellent accuracy, and low temperature drift make the AMC1300B-Q1 a high-performance solution for automotive applications where shunt-based current sensing in the presence of high common-mode voltage levels is required.

8.2 Typical Application

The AMC1300B-Q1 is ideally suited for shunt-based current sensing applications where accurate current monitoring is required in the presence of high common-mode voltages.

图 8-1 shows the AMC1300B-Q1 in a typical application. The load current flowing through an external shunt resistor RSHUNT produces a voltage drop that is sensed by the AMC1300B-Q1. The AMC1300B-Q1 digitizes the analog input signal on the high-side, transfers the data across the isolation barrier to the low-side, reconstructs the analog signal, and presents that signal as a differential voltage on the output pins.

The differential input, differential output, and the high common-mode transient immunity (CMTI) of the AMC1300B-Q1 ensure reliable and accurate operation even in high-noise environments.

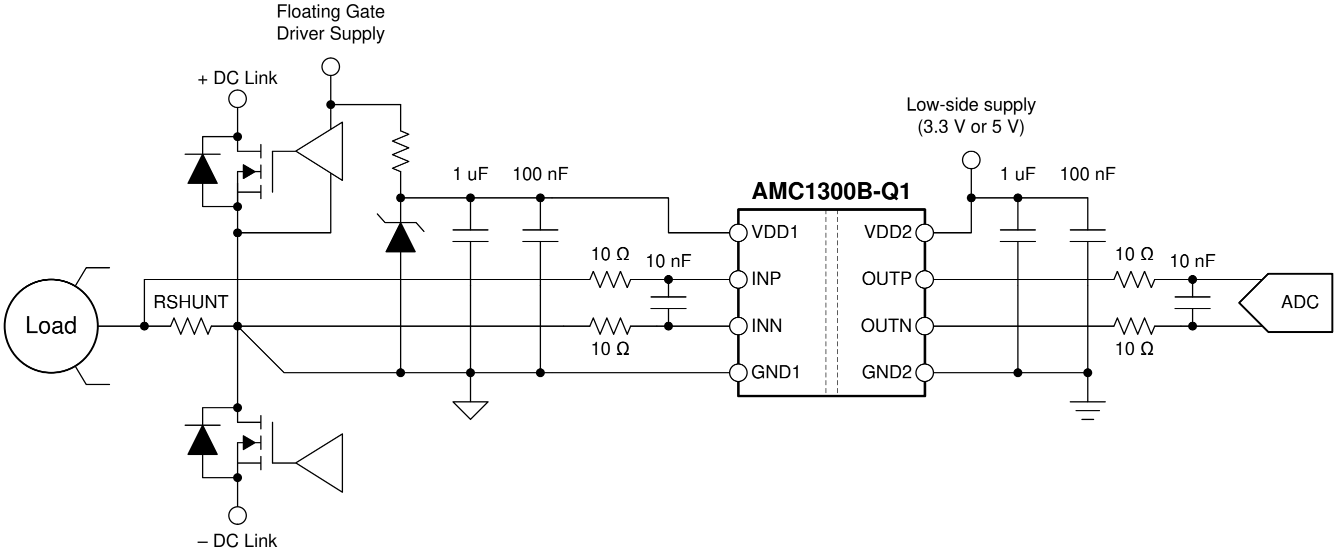


图 8-1. Using the AMC1300B-Q1 for Current Sensing in a Typical Application

8.2.1 Design Requirements

表 8-1 lists the parameters for this typical application.

表 8-1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across RSHUNT for a linear response	±250 mV (maximum)
Signal delay (50% V_{IN} to 90% OUTP, OUTN)	3 µs (maximum)

8.2.2 Detailed Design Procedure

In 图 8-1, the high-side power supply (VDD1) for the AMC1300B-Q1 is derived from the floating power supply of the upper gate driver.

The floating ground reference (GND1) is derived from the end of the shunt resistor that is connected to the negative input of the AMC1300B-Q1 (INN). If a four-pin shunt is used, the inputs of the AMC1300B-Q1 are connected to the inner leads and GND1 is connected to the outer lead on the INN-side of the shunt. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device. See the *Layout* section for more details.

8.2.2.1 Shunt Resistor Sizing

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times RSHUNT$.

Consider the following two restrictions when selecting the value of the shunt resistor, RSHUNT:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range for a linear response: $|V_{SHUNT}| \leqslant |V_{FSR}|$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \leqslant |V_{Clipping}|$

8.2.2.2 Input Filter Design

TI recommends placing an RC-filter in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the ΔΣ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

For most applications, the structure shown in 图 8-2 achieves excellent performance.

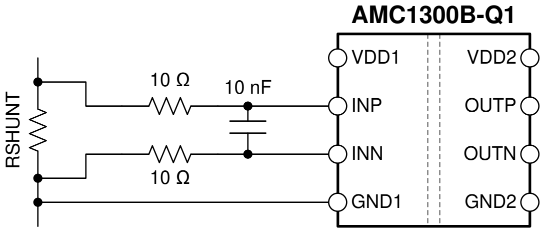


图 8-2. Differential Input Filter

8.2.2.3 Differential to Single-Ended Output Conversion

图 8-3 shows an example of a TLVx313-Q1-based signal conversion and filter circuit for systems using single-ended-input ADCs to convert the analog output voltage into digital. With R1 = R2 = R3 = R4, the output voltage equals (V_{OUTP} – V_{OUTN}) + V_{REF}. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system. For most applications, R1 = R2 = R3 = R4 = 3.3 kΩ and C1 = C2 = 330 pF yields good performance.

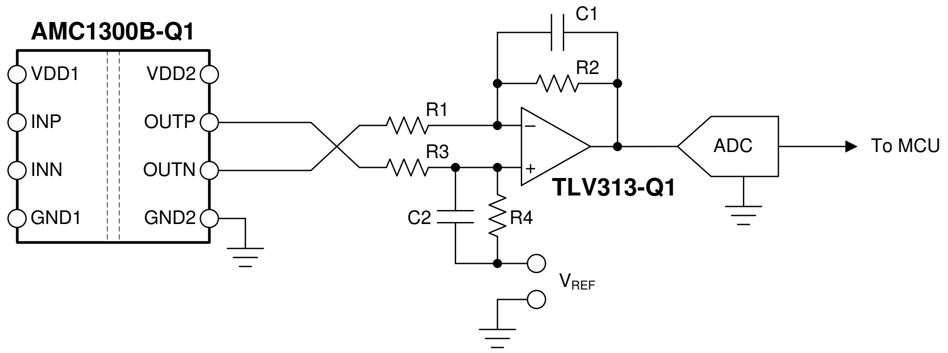


图 8-3. Connecting the AMC1300B-Q1 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guides, available for download at www.ti.com.

8.2.3 Application Curves

One important aspect of power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, a low delay caused by the isolated amplifier is required. 图 8-4 shows the typical full-scale step response of the AMC1300B-Q1.

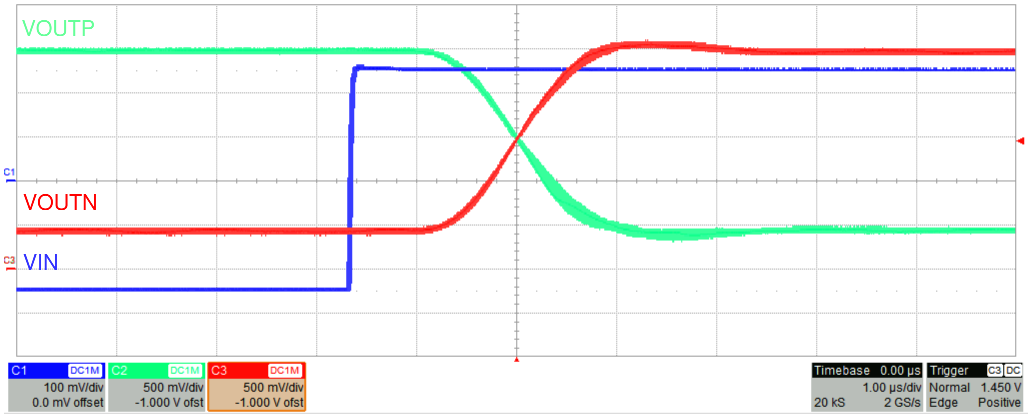


图 8-4. Step Response of the AMC1300B-Q1

8.3 What to Do and What Not to Do

Do not leave the inputs of the AMC1300B-Q1 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current may drive the inputs to a positive value that exceeds the operating common-mode input voltage and the device outputs the failsafe voltage as described in the *Analog Output* section.

Connect the high-side ground (GND1) to INN, either by a hard short or through a resistive path. A DC current path between INN and GND1 is required to define the input common-mode voltage. Take care not to exceed the input common-mode range as specified in the *Recommended Operating Conditions* table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device. See the *Layout* section for more details.

9 Power Supply Recommendations

The AMC1300B-Q1 does not require any specific power up sequencing. The high-side power-supply (VDD1) is decoupled with a low-ESR 100-nF capacitor (C1) parallel to a low-ESR 1-µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR 100-nF capacitor (C3) parallel to a low-ESR 1-µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible.

The ground reference for the high-side (GND1) is derived from the end of the shunt resistor, which is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace (as shown in 图 9-1) to make this connection instead of shorting GND1 to INN directly at the device input. If a four-terminal shunt is used, the device inputs are connected to the inner leads and GND1 is connected to the outer lead on the INN-side of the shunt.

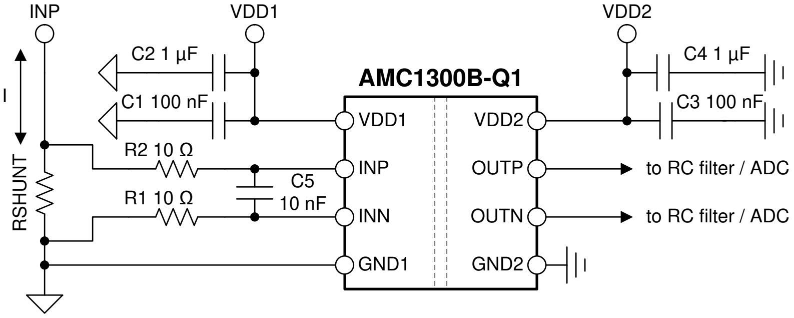


图 9-1. Decoupling of the AMC1300B-Q1

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCCs) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

10 Layout

10.1 Layout Guidelines

图 10-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1300B-Q1 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1300B-Q1 and keep the layout of both connections symmetrical.

10.2 Layout Example

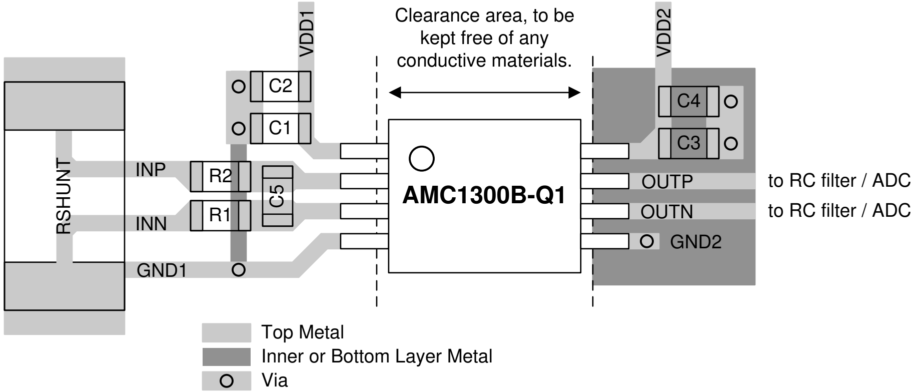


图 10-1. Recommended Layout of the AMC1300B-Q1

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *TLVx313-Q1 Low-Power, Rail-to-Rail In/Out, 750-µV Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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11.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1300BQDWVRQ1	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	MC1300BQ	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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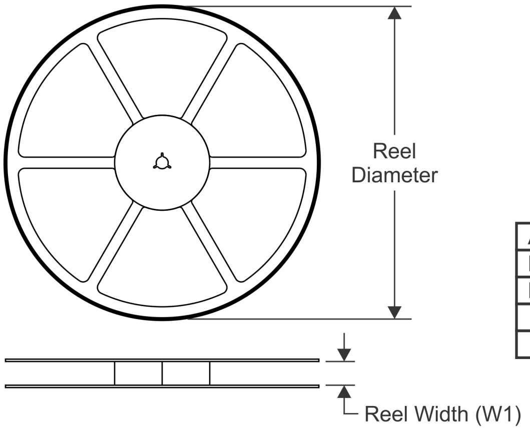
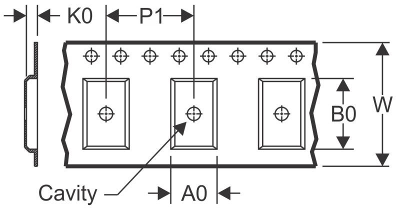
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

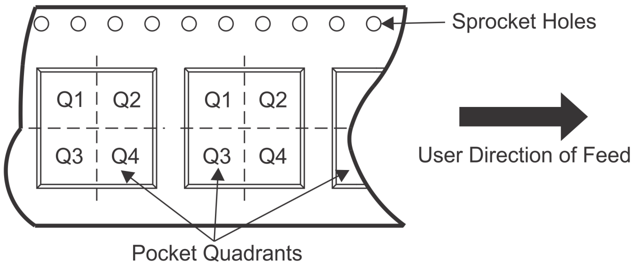


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

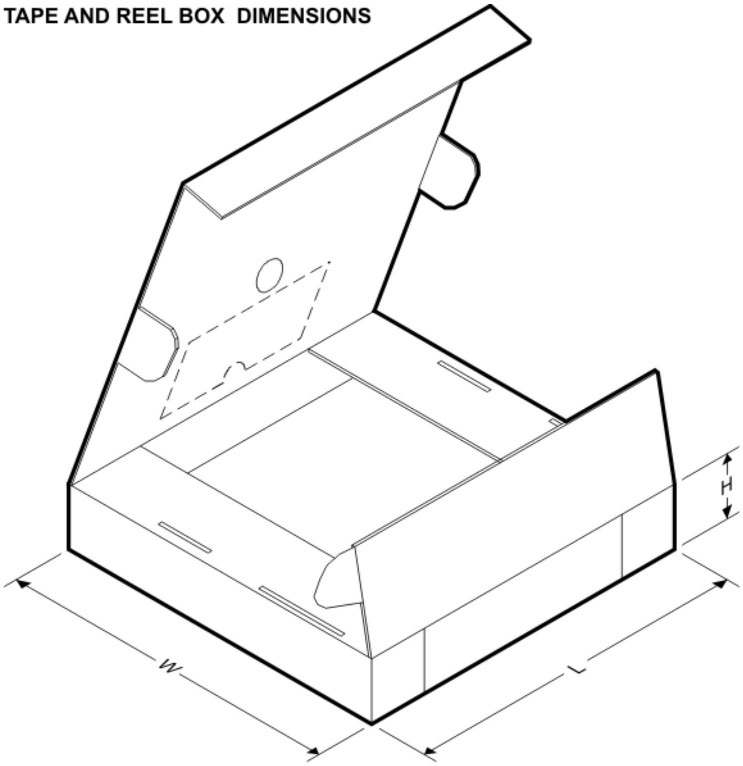
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

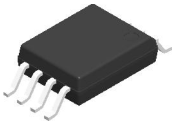
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1300BQDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

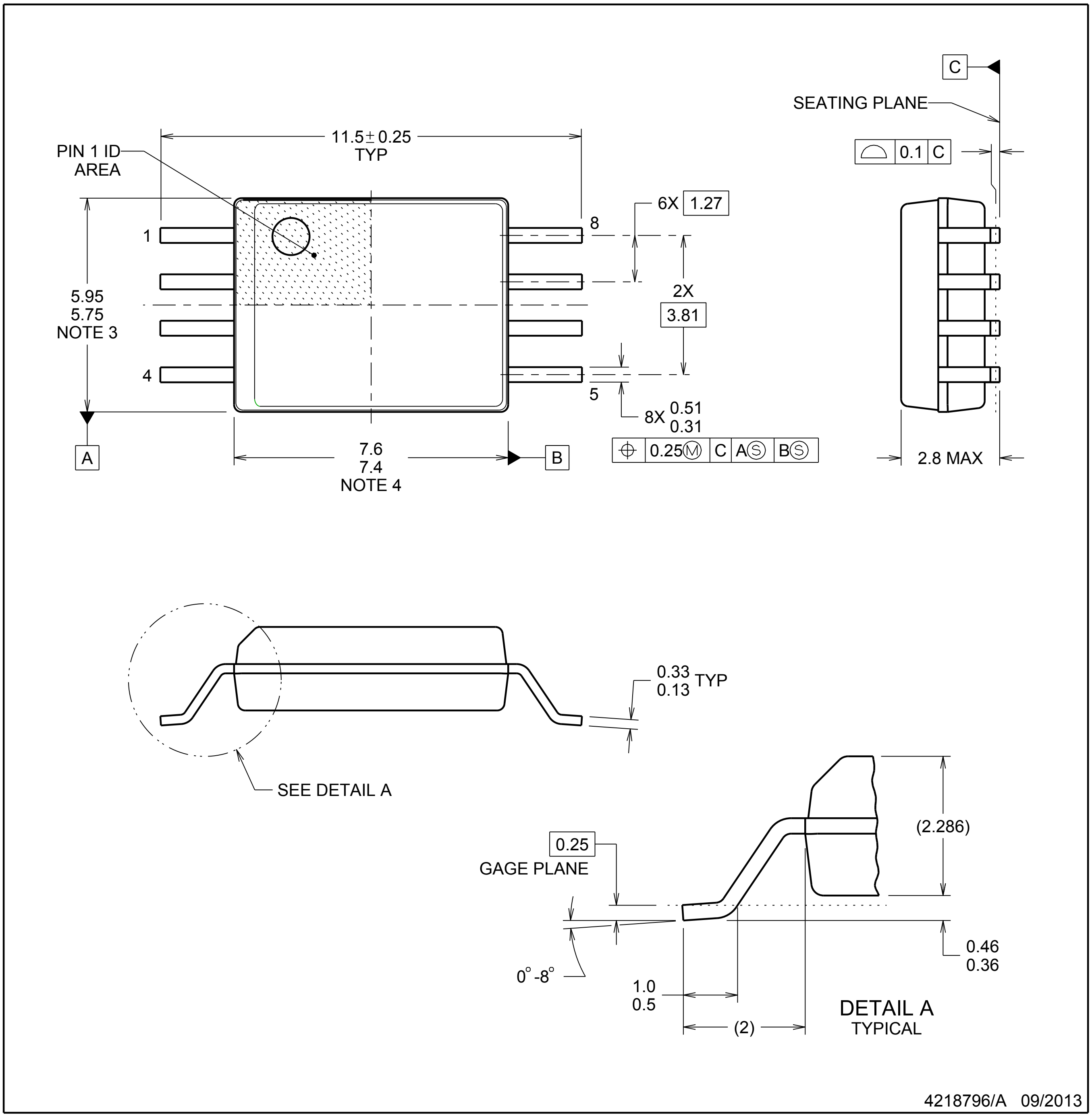
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1300BQDWVRQ1	SOIC	DWV	8	1000	350.0	350.0	43.0



DWV0008A

SOIC - 2.8 mm max height

SOIC



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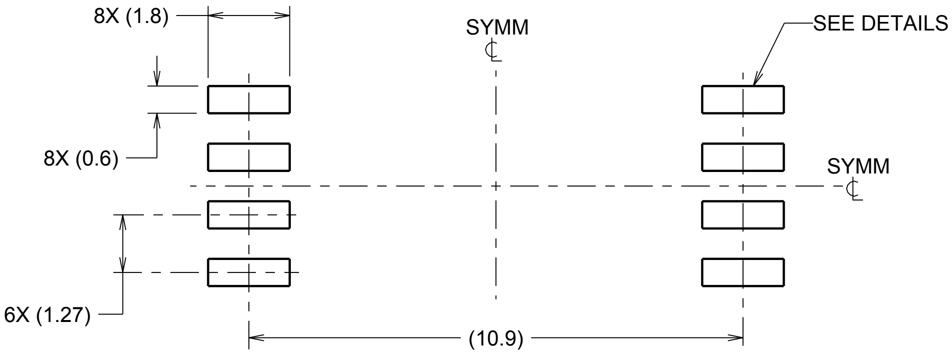
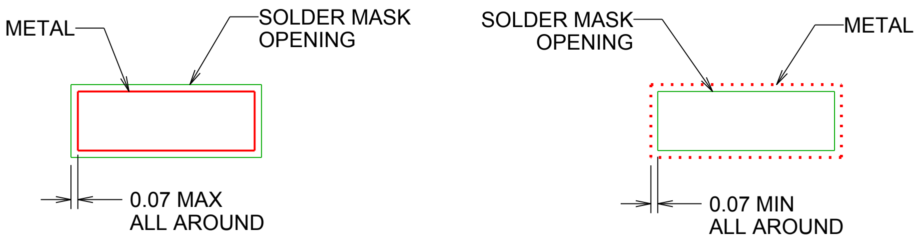
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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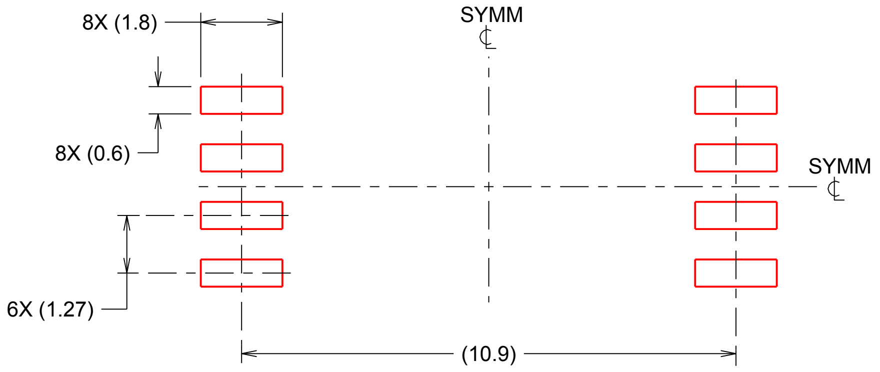
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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