AMC1100 全差动隔离放大器

1 特性

- 针对分流电阻器进行优化的 ±250mV 输入电压范围
- 超低的非线性度：5V 时最大为 0.075%
- 低失调电压误差：1.5mV（最大值）
- 低噪声：3.1mV_{RMS}（典型值）
- 低高侧电源电流：
  5V 时的最大值为 8mA
- 输入带宽：60kHz（最小值）
- 固定增益：8（精度为 0.5%）
- 高共模抑制比：108dB
- 低侧运行：3.3V
- 安全相关认证：
  - 符合 DIN VDE V 0884-11: 2017-01 标准的 4250V_{PK} 基础型隔离
  - 符合 UL1577 标准且长达 1 分钟的 3005V_{RMS} 隔离
  - 符合 CAN/CSA No. 5A 组件验收服务通知和 DIN EN 61010-1 标准
  - 工作电压：1200V_{PEAK}
  - 瞬态抗扰度：2.5kV/µs（最小值）
- 可在扩展工业温度范围内正常工作

2 应用

基于分流电阻器的电流感应，可用于：

- 电表
- 串式逆变器
- 功率测量 或

3 说明

AMC1100 是一款高精度隔离放大器，通过具有高磁场抗扰度的二氧化硅 (SiO_2) 隔栅隔离输出与输入电路。根据 DIN VDE V 0884-11: 2017-01 和 UL1577 标准，该隔离栅经认证可提供高达 4250V_{PEAK} 的电隔离。当与隔离电源配合使用时，此器件可防止高共模电压线路上的噪声电流流入本地接地并干扰或损坏敏感电路。

AMC1100 输入进行了优化，可以直接连接到分流电阻器或其他低电压电平信号源。凭借该器件的出色性能，可在电能计量应用中实现精确的电流和电压 测量。输出信号共模电压被自动调节至 3V 或者 5V 低侧电源。

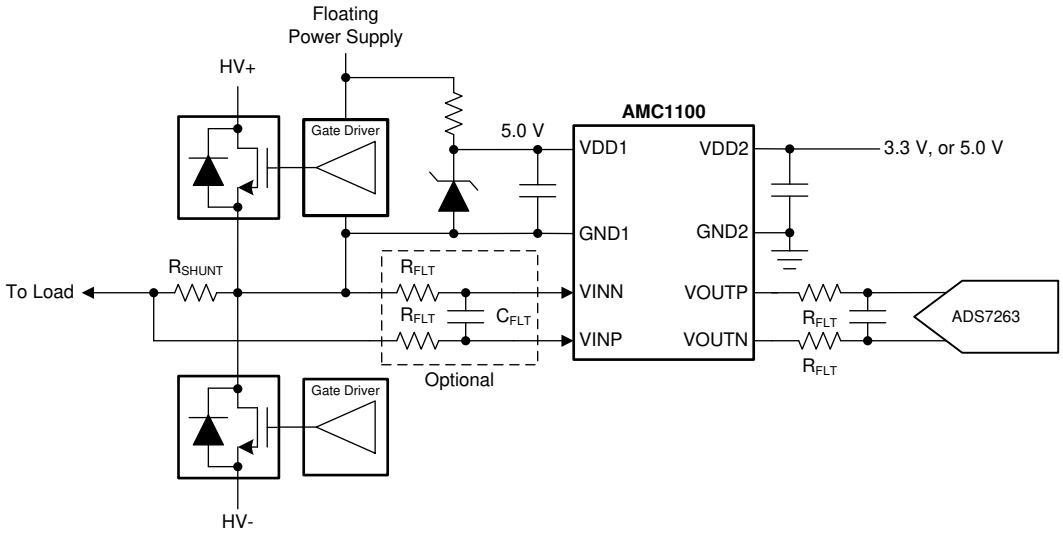
AMC1100 在扩展工业温度范围（–40°C 至 +105°C）内完全额定运行，并且采用 SMD 型宽体小外形集成电路 (SOIC)-8 (DWV) 封装以及 gullwing-8 (DUB) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
AMC1100	SOP (8)	9.50mm × 6.57mm
	SOIC (8)	5.85mm × 7.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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4 修订历史记录

Changes from Revision A (December 2014) to Revision B **Page**

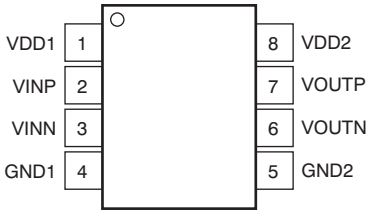
- 已更改 根据 ISO 标准更改了*安全相关认证* 特性 项目中的认证详细信息 ... 1
- 已删除 删除了 特性 项目符号中的寿命典型值 ... 1
- 已更改 *更改了"应用"*部分以包含终端设备链接 ... 1
- 已更改 将 *IEC60747-5-2* 更改为 *DIN VDE V 0884-11: 2017-01*（位于*说明* 部分） ... 1
- 已更改 更改了第 1 页的图并添加了标题 ... 1
- Added *Power Ratings* table ... 4
- Changed *Insulation Specifications* table per ISO standard ... 5
- Added DWV-package related details in *Insulation Specifications* table ... 5
- Changed *Safety-Related Certification* table per ISO standard ... 6
- Changed *Safety Limiting Values* table per ISO standard ... 6
- Deleted VDD1 and VDD2 from *Electrical Characteristics* table (repeated in *Recommended Operating Conditions* table) ... 7
- Added *Insulation Characteristics Curves* section ... 8
- Changed *Zener Diode Based High-Side Supply* figure ... 21

Changes from Original (April 2012) to Revision A **Page**

- 更改了格式，以符合最新的数据表标准 ... 1
- 添加了 *ESD 额定值* 表和*特性* *说明*、*器件功能模式*、*应用和实施*、*电源相关建议*、*布局*、*器件和文档支持* 以及*机械、封装和可订购信息* 部分 ... 1
- 在文档中添加了 DWV 封装 ... 1
- Deleted *Package and Ordering Information* section ... 3

5 Pin Configuration and Functions

DUB and DWV Packages
SOP-8 and SOIC-8
(Top View)



Pin Descriptions

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
GND1	4	Power	High-side analog ground
GND2	5	Power	Low-side analog ground
VDD1	1	Power	High-side power supply
VDD2	8	Power	Low-side power supply
VINN	3	Analog input	Inverting analog input
VINP	2	Analog input	Noninverting analog input
VOUTN	6	Analog output	Inverting analog output
VOUTP	7	Analog output	Noninverting analog output

6 Specifications

6.1 Absolute Maximum Ratings

see(1)

	MIN	MAX	UNIT
Supply voltage, VDD1 to GND1 or VDD2 to GND2	–0.5	6	V
Analog input voltage at VINP, VINN	GND1 – 0.5	VDD1 + 0.5	V
Input current to any pin except supply pins		±10	mA
Maximum junction temperature, T_J Max		150	°C
Storage temperature range, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating ambient temperature range	–40		105	°C
VDD1	High-side power supply	4.5	5.0	5.5	V
VDD2	Low-side power supply	2.7	5.0	5.5	V

6.4 Thermal Information

THERMAL METRIC(1)		AMC1100		UNIT
		DUB (SOP)	DWV (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.1	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.6	49.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.8	56.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.2	16.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.4	55.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V			82.5	mW
		VDD1 = 5.5 V, VDD2 = 3.6 V			65.6	
P_{D1}	Maximum power dissipation (high-side supply)	VDD1 = 5.5 V			44.0	mW
P_{D2}	Maximum power dissipation (low-side supply)	VDD2 = 5.5 V			38.5	mW
		VDD2 = 3.6 V			21.6	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air, DUB package	≥ 7	mm
		Shortest pin-to-pin distance through air, DWV package	≥ 8.5	
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface, DUB package	≥ 7	mm
		Shortest pin-to-pin distance across the package surface, DWV package	≥ 8.5	
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the insulation	≥ 0.014	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112, DUB package	≥ 400	V
		DIN EN 60112 (VDE 0303-11); IEC 60112, DWV package	≥ 600	
	Material group	According to IEC 60664-1, DUB package	II	
		According to IEC 60664-1, DWV package	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
DIN VDE V 0884-11: 2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At ac voltage (bipolar)	1200	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At ac voltage (sine wave)	849	V_{RMS}
		At dc voltage	1200	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	4250	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	5100	
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.3 \times V_{IOSM} = 6000\ V_{PK}$ (qualification)	4615	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroup 2 / 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM} = 1440\ V_{PK}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.3 \times V_{IORM} = 1560\ V_{PK}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.5 \times V_{IORM} = 1800\ V_{PK}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.5 V_{PP} at 1 MHz	1.2	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_A < 85°C	> 10^{12}	Ω
		V_{IO} = 500 V at 85°C < T_A < 105°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 3005 V_{RMS} or 4250 V_{DC}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 3606 V_{RMS}, t = 1 s (100% production test)	3005	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL	CSA
Certified according to DIN VDE V 0884-11: 2017-01 and DIN EN 61010-1 (VDE 0411-1) : 2011-07	Recognized under 1577 component recognition program	Recognized under CSA component acceptance NO 5 program, IEC 60950-1, and IEC 61010-1
Basic insulation	Single protection	Basic insulation
Certificate number: 40047657	File number: E181974	Certificate number: 2643952

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DUB package, $R_{\theta JA}$ = 75.1°C/W, T_J = 150°C, T_A = 25°C, VDD1 = VDD2 = 5.5 V, see Figure 1			302	mA
		DWV package, $R_{\theta JA}$ =102.8°C/W, T_J = 150°C, T_A = 25°C, VDD1 = VDD2 = 5.5 V, see Figure 1			221	
P_S	Safety input, output, or total power(1)	DUB package, $R_{\theta JA}$ = 75.1°C/W, T_J = 150°C, T_A = 25°C, see Figure 2			1664	mW
		DWV package, $R_{\theta JA}$ = 102.8°C/W, T_J = 150°C, T_A = 25°C, see Figure 2			1216	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD1_{max} + I_S \times VDD2_{max}$, where $VDD1_{max}$ is the maximum high-side supply voltage and $VDD2_{max}$ is the maximum low-side supply voltage.

6.9 Electrical Characteristics

All minimum and maximum specifications are at T_A = –40°C to +105°C and are within the specified voltage range, unless otherwise noted. Typical values are at T_A = +25°C, VDD1 = 5 V, and VDD2 = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
	Maximum input voltage before clipping	VINP – VINN		±320		mV
	Differential input voltage	VINP – VINN	–250		250	mV
V_{CM}	Common-mode operating range		–0.16		VDD1	V
V_{OS}	Input offset voltage		–1.5	±0.2	1.5	mV
TCV_{OS}	Input offset thermal drift		–10	±1.5	10	µV/K
CMRR	Common-mode rejection ratio	V_{IN} from 0 V to 5 V at 0 Hz		108		dB
		V_{IN} from 0 V to 5 V at 50 kHz		95		dB
C_{IN}	Input capacitance to GND1	VINP or VINN		3		pF
C_{IND}	Differential input capacitance			3.6		pF
R_{IN}	Differential input resistance			28		kΩ
	Small-signal bandwidth		60	100		kHz
OUTPUT						
	Nominal gain			8		
G_{ERR}	Gain error	Initial, at T_A = +25°C	–0.5%	±0.05%	0.5%	
			–1%	±0.05%	1%	
TCG_{ERR}	Gain error thermal drift			±56		ppm/K
	Nonlinearity	4.5 V ≤ VDD2 ≤ 5.5 V	–0.075%	±0.015%	0.075%	
		2.7 V ≤ VDD2 ≤ 3.6 V	–0.1%	±0.023%	0.1%	
	Nonlinearity thermal drift			2.4		ppm/K
	Output noise	VINP = VINN = 0 V		3.1		mV_{RMS}
PSRR	Power-supply rejection ratio	vs VDD1, 10-kHz ripple		80		dB
		vs VDD2, 10-kHz ripple		61		dB
	Rise-and-fall time	0.5-V step, 10% to 90%		3.66	6.6	µs
	V_{IN} to V_{OUT} signal delay	0.5-V step, 50% to 10%, unfiltered output		1.6	3.3	µs
		0.5-V step, 50% to 50%, unfiltered output		3.15	5.6	µs
		0.5-V step, 50% to 90%, unfiltered output		5.26	9.9	µs
CMTI	Common-mode transient immunity	V_{CM} = 1 kV	2.5	3.75		kV/µs
	Output common-mode voltage	2.7 V ≤ VDD2 ≤ 3.6 V	1.15	1.29	1.45	V
		4.5 V ≤ VDD2 ≤ 5.5 V	2.4	2.55	2.7	V
	Short-circuit current			20		mA
R_{OUT}	Output resistance			2.5		Ω
POWER SUPPLY						
I_{DD1}	High-side supply current			5.4	8	mA
I_{DD2}	Low-side supply current	2.7 V < VDD2 < 3.6 V		3.8	6	mA
		4.5 V < VDD2 < 5.5 V		4.4	7	mA
P_{DD1}	High-side power dissipation			27.0	44.0	mW
P_{DD2}	Low-side power dissipation	2.7 V < VDD2 < 3.6 V		11.4	21.6	mW
		4.5 V < VDD2 < 5.5 V		22.0	38.5	mW

6.10 Insulation Characteristics Curves

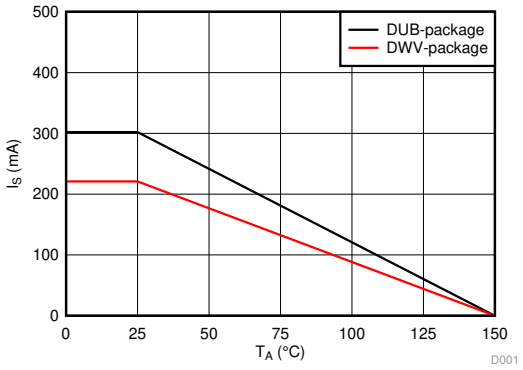


Figure 1. Thermal Derating Curve for Safety-Limiting Current per VDE

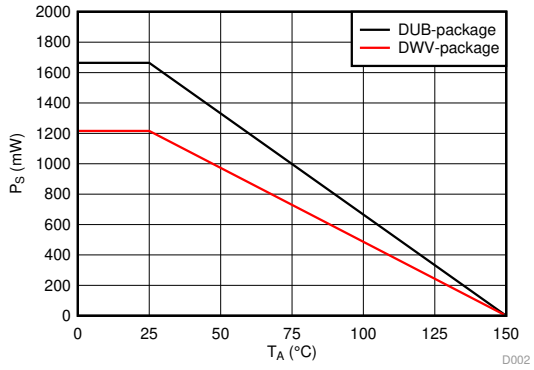


Figure 2. Thermal Derating Curve for Safety-Limiting Power per VDE

6.11 Typical Characteristics

At VDD1 = VDD2 = 5 V, VINP = –250 mV to +250 mV, and VINN = 0 V, unless otherwise noted.

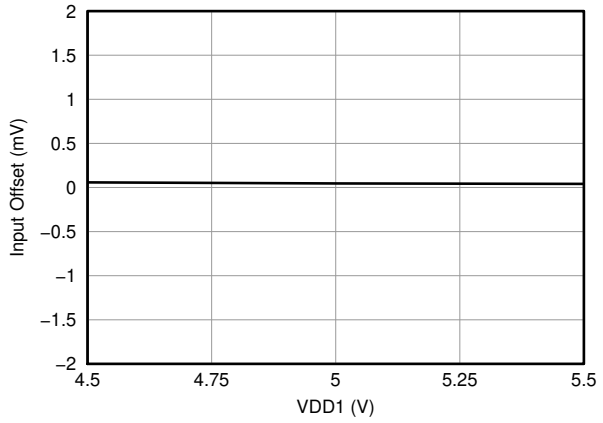


Figure 3. Input Offset vs High-Side Supply Voltage

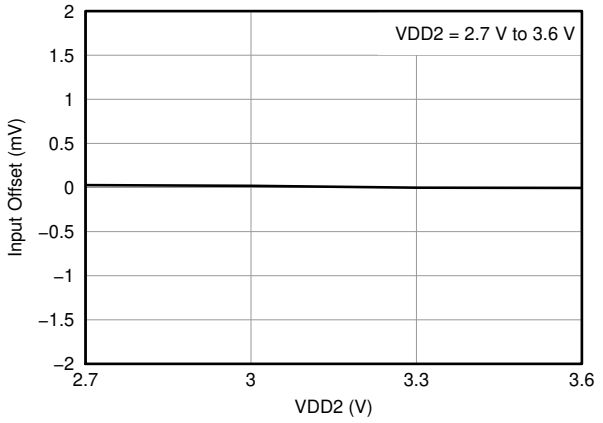


Figure 4. Input Offset vs Low-Side Supply Voltage

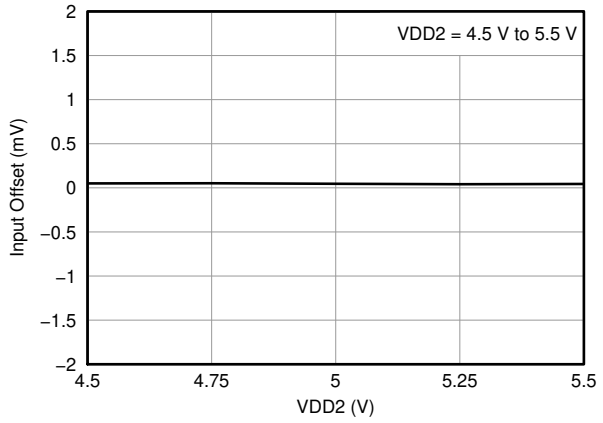


Figure 5. Input Offset vs Low-Side Supply Voltage

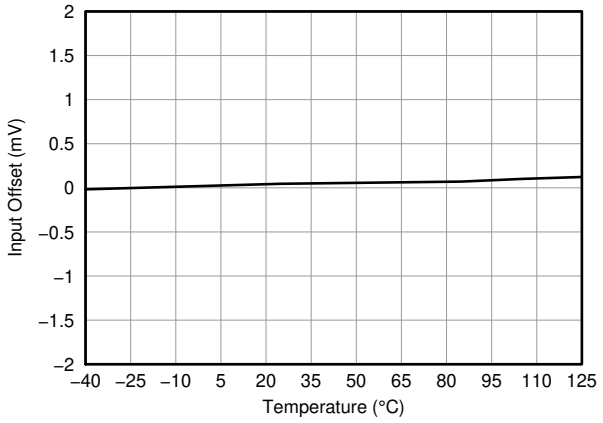


Figure 6. Input Offset vs Temperature

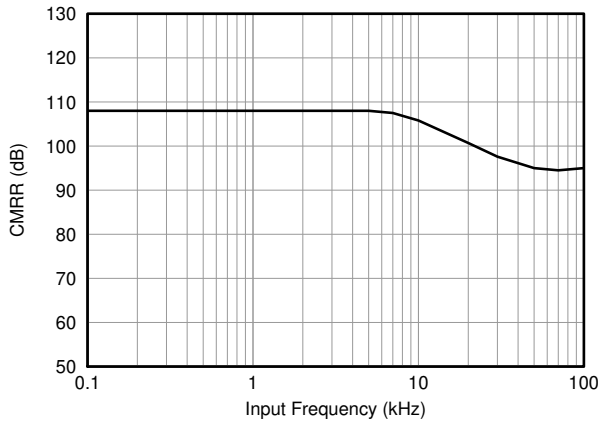


Figure 7. Common-Mode Rejection Ratio vs Input Frequency

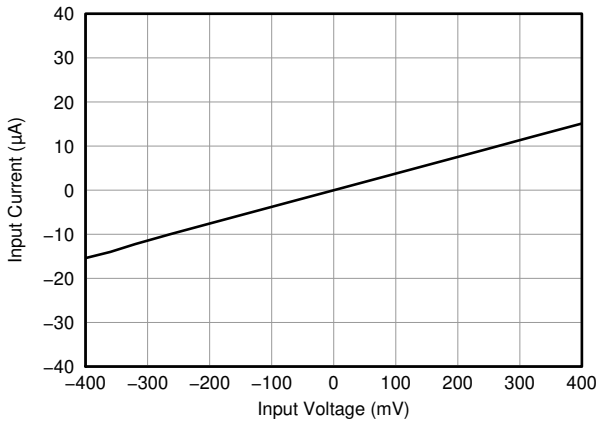


Figure 8. Input Current vs Input Voltage

Typical Characteristics (continued)

At VDD1 = VDD2 = 5 V, VINP = –250 mV to +250 mV, and VINN = 0 V, unless otherwise noted.

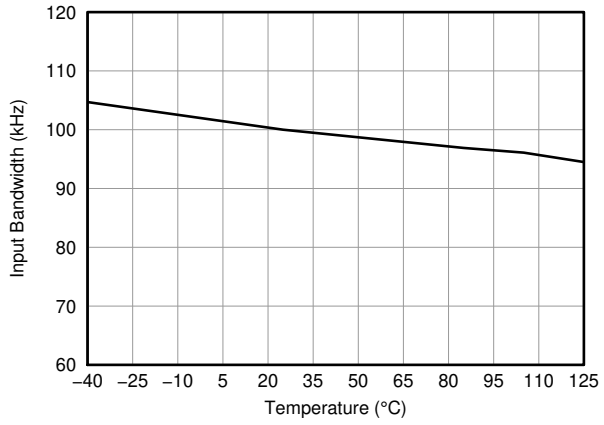


Figure 9. Input Bandwidth vs Temperature

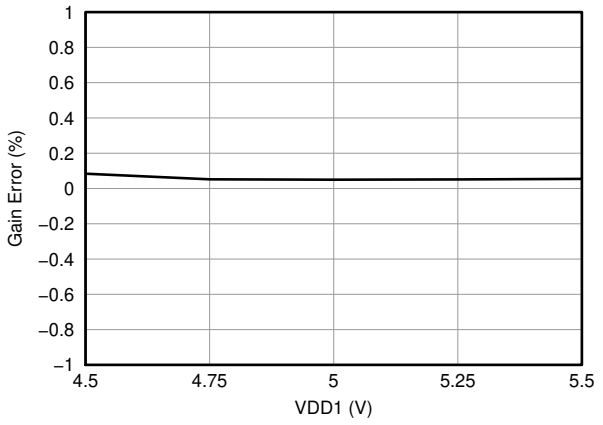


Figure 10. Gain Error vs High-Side Supply Voltage

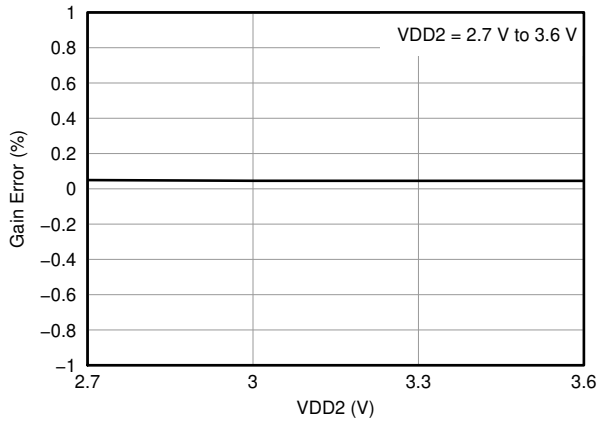


Figure 11. Gain Error vs Low-Side Supply Voltage

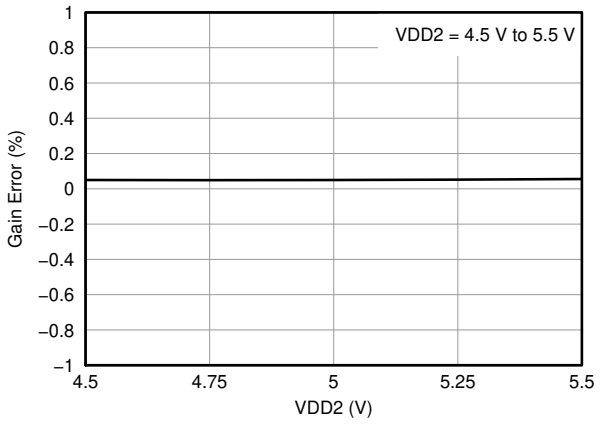


Figure 12. Gain Error vs Low-Side Supply Voltage

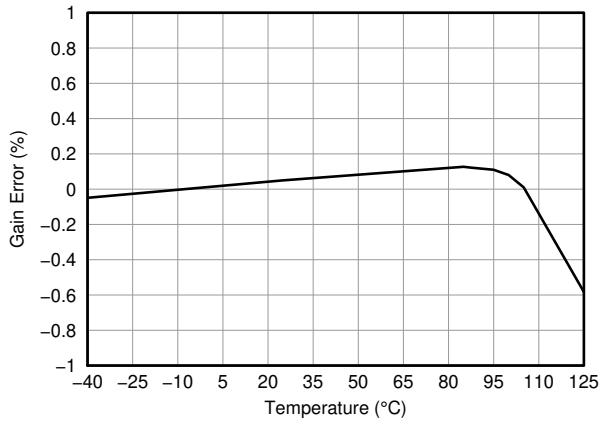


Figure 13. Gain Error vs Temperature

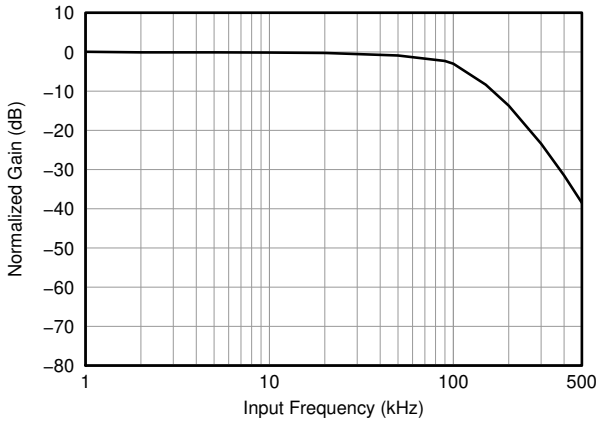


Figure 14. Normalized Gain vs Input Frequency

Typical Characteristics (continued)

At VDD1 = VDD2 = 5 V, VINP = –250 mV to +250 mV, and VINN = 0 V, unless otherwise noted.

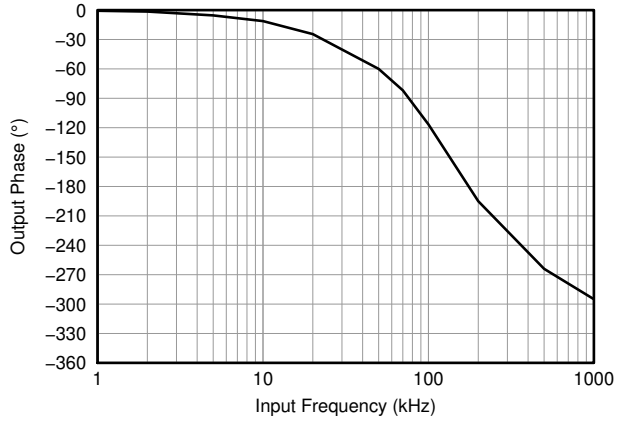


Figure 15. Output Phase vs Input Frequency

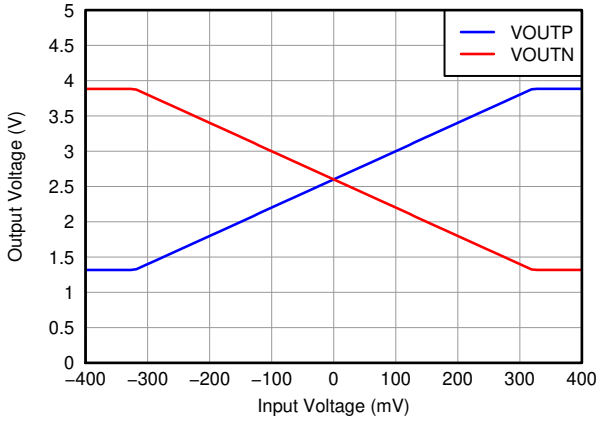


Figure 16. Output Voltage vs Input Voltage

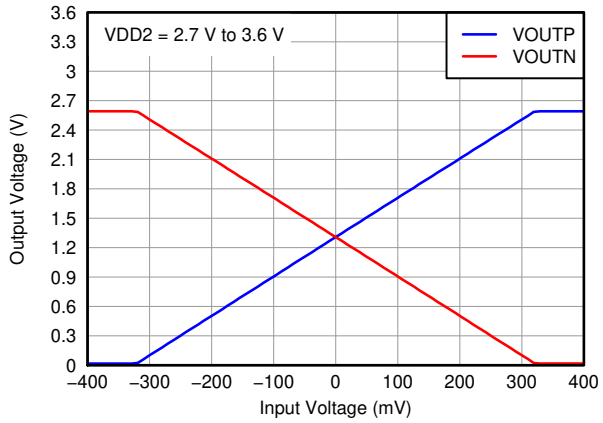


Figure 17. Output Voltage vs Input Voltage

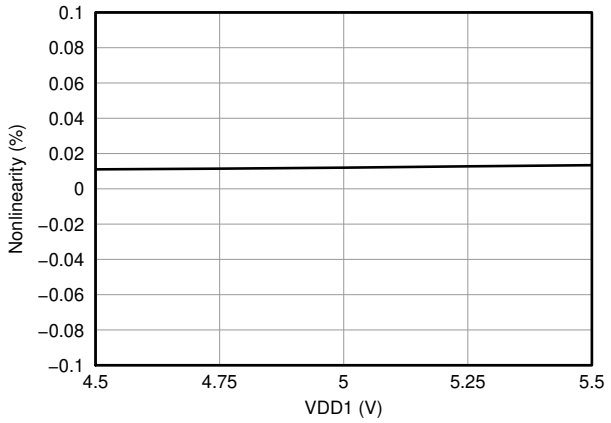


Figure 18. Nonlinearity vs High-Side Supply Voltage

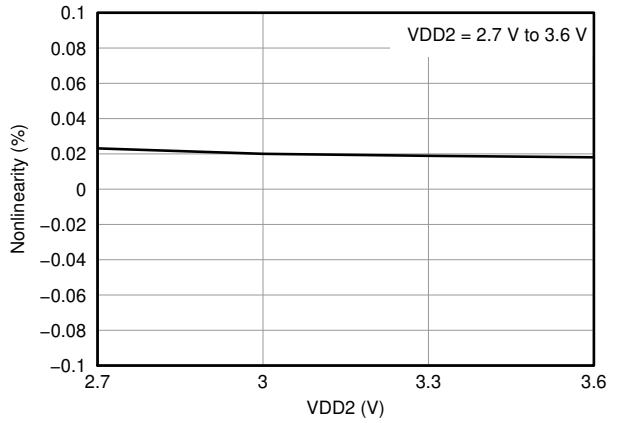


Figure 19. Nonlinearity vs Low-Side Supply Voltage

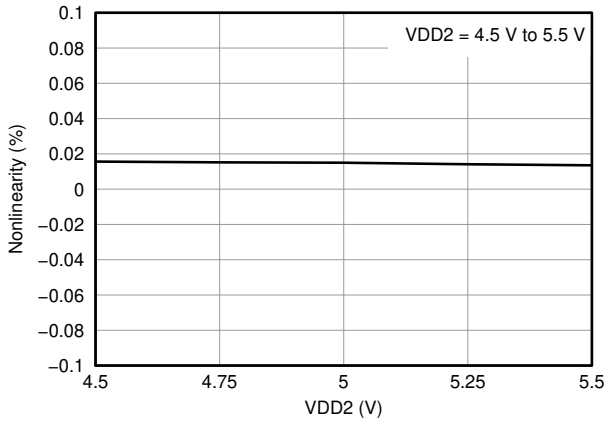


Figure 20. Nonlinearity vs Low-Side Supply Voltage

Typical Characteristics (continued)

At VDD1 = VDD2 = 5 V, VINP = –250 mV to +250 mV, and VINN = 0 V, unless otherwise noted.

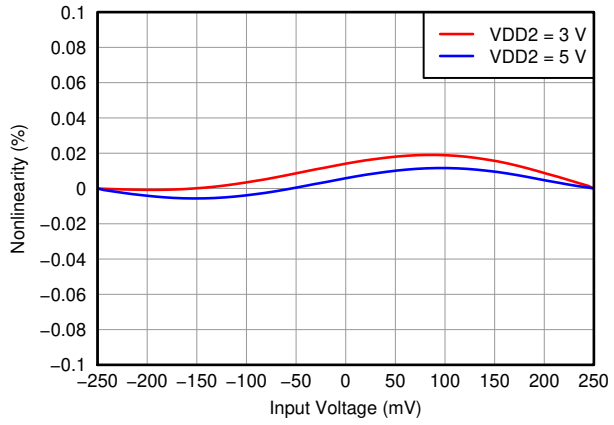


Figure 21. Nonlinearity vs Input Voltage

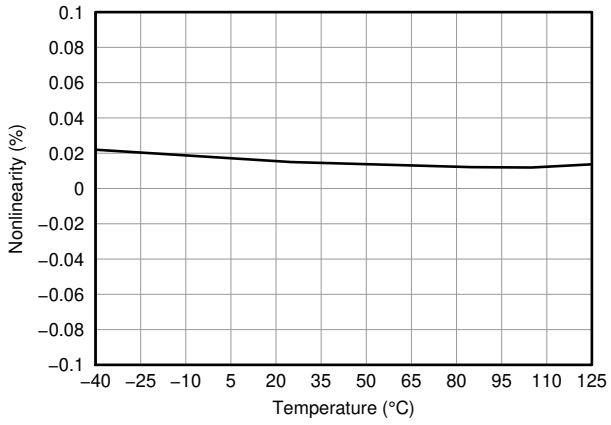


Figure 22. Nonlinearity vs Temperature

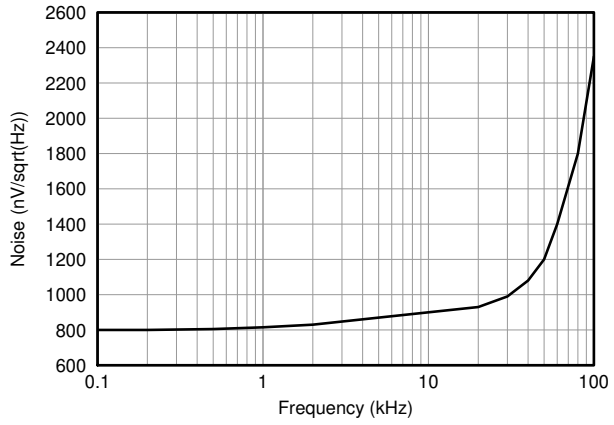


Figure 23. Output Noise Density vs Frequency

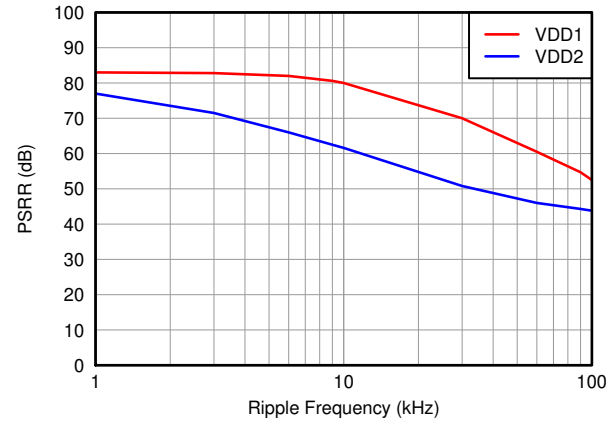


Figure 24. Power-Supply Rejection Ratio vs Ripple Frequency

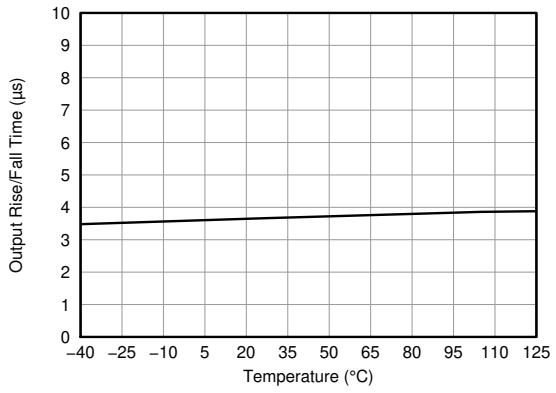


Figure 25. Output Rise and Fall Time vs Temperature

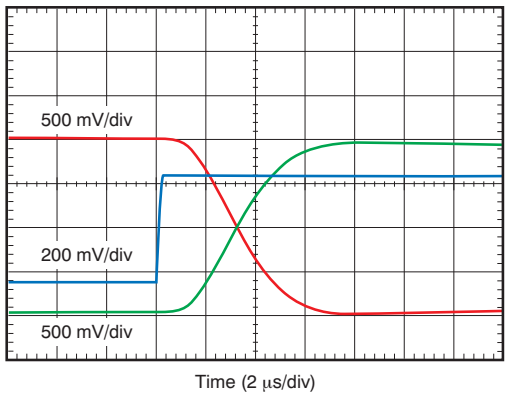


Figure 26. Full-Scale Step Response

Typical Characteristics (continued)

At VDD1 = VDD2 = 5 V, VINP = –250 mV to +250 mV, and VINN = 0 V, unless otherwise noted.

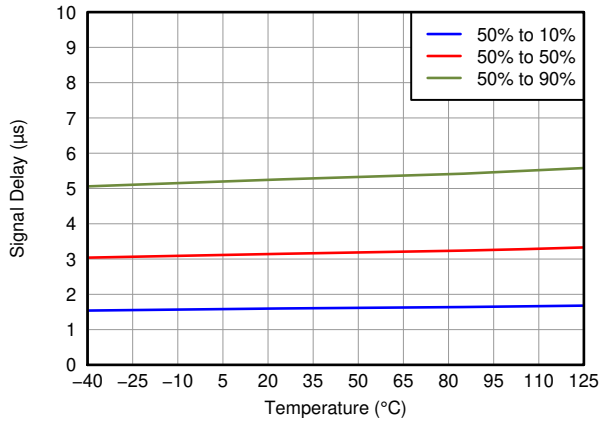


Figure 27. Output Signal Delay Time vs Temperature

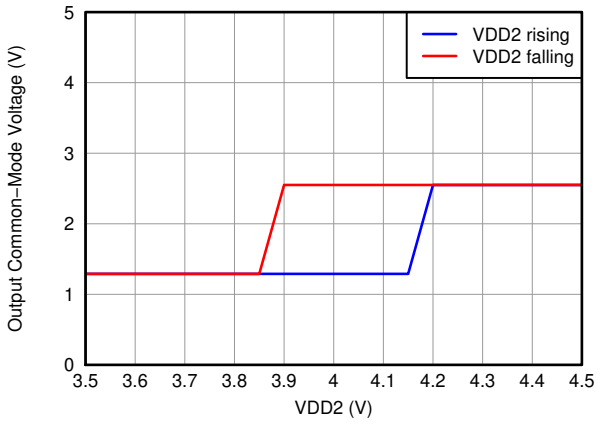


Figure 28. Output Common-Mode Voltage vs Low-Side Supply Voltage

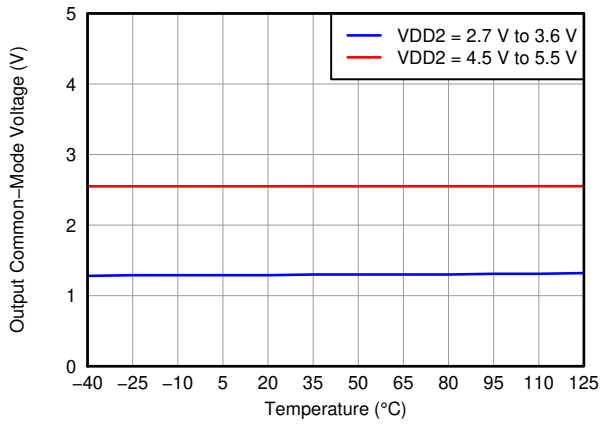


Figure 29. Output Common-Mode Voltage vs Temperature

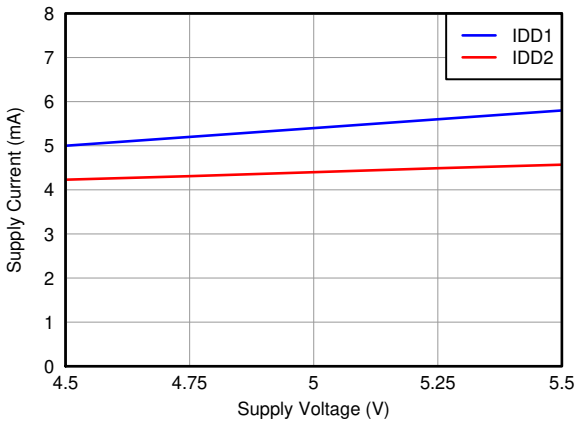


Figure 30. Supply Current vs Supply Voltage

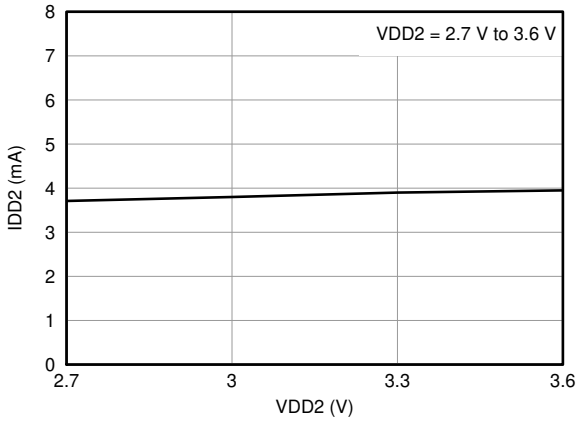


Figure 31. Low-Side Supply Current vs Low-Side Supply Voltage

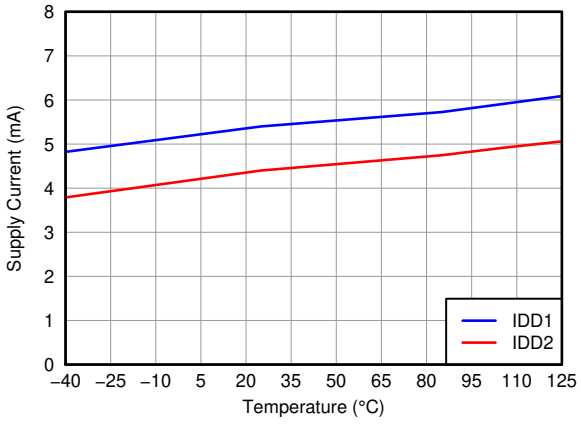


Figure 32. Supply Current vs Temperature

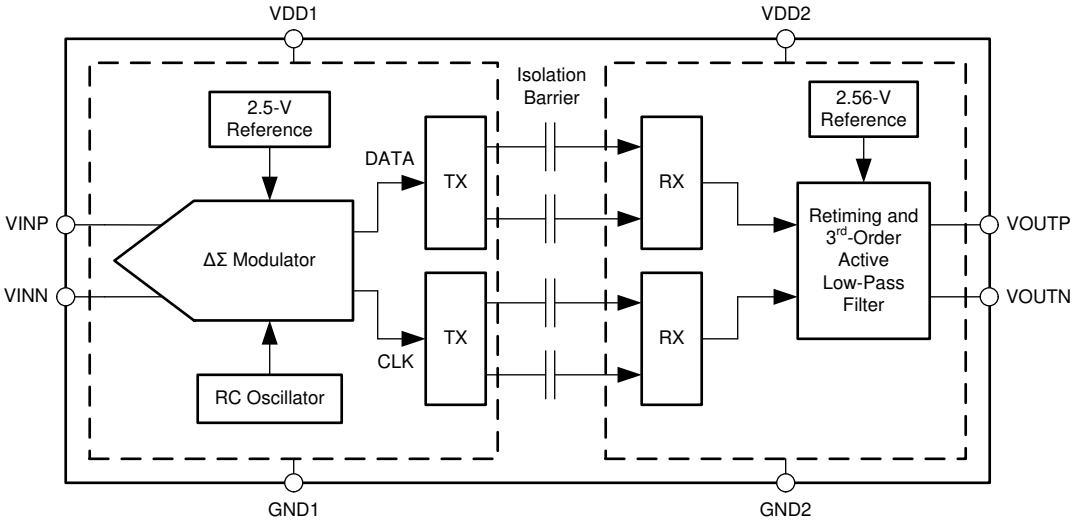
7 Detailed Description

7.1 Overview

The AMC1100 consists of a delta-sigma modulator input stage including an internal reference and clock generator. The output of the modulator and clock signal are differentially transmitted over the integrated capacitive isolation barrier that separates the high- and low-voltage domains. The received bitstream and clock signals are synchronized and processed by a third-order analog filter with a nominal gain of 8 on the low-side and presented as a differential output of the device, as shown in the *Functional Block Diagram* section.

The SiO_2-based capacitive isolation barrier supports a high level of magnetic field immunity, as described in application report SLLA181, *ISO72x Digital Isolator Magnetic-Field Immunity* (available for download at www.ti.com).

7.2 Functional Block Diagram



7.3 Feature Description

The differential analog input of the AMC1100 is a switched-capacitor circuit based on a second-order modulator stage that digitizes the input signal into a 1-bit output stream. The device compares the differential input signal (V_{IN} = VINP – VINN) against the internal reference of 2.5 V using internal capacitors that are continuously charged and discharged with a typical frequency of 10 MHz. With the S1 switches closed, C_{IND} charges to the voltage difference across VINP and VINN. For the discharge phase, both S1 switches open first and then both S2 switches close. C_{IND} discharges to approximately GND1 + 0.8 V during this phase. Figure 33 shows the simplified equivalent input circuitry.

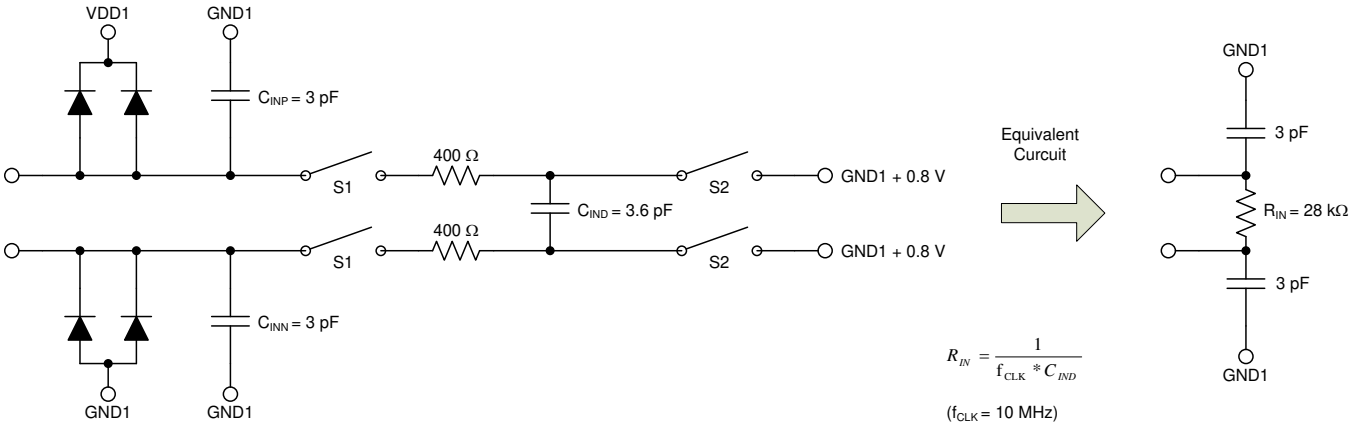


Figure 33. Equivalent Input Circuit

The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. However, there are two restrictions on the analog input signals, VINP and VINN. If the input voltage exceeds the range GND1 – 0.5 V to VDD1 + 0.5 V, the input current must be limited to 10 mA to protect the implemented input protection diodes from damage. In addition, the device linearity and noise performance are ensured only when the differential analog input voltage remains within ±250 mV.

7.4 Device Functional Modes

The AMC1100 is powered on when the supplies are connected. The device is operated off a 5-V nominal supply on the high-side. The potential of the ground reference GND1 can be floating, which is usually the case in shunt-based current-measurement applications. TI recommends tying one side of the shunt to the GND1 pin of the AMC1100 to maintain the operating common-mode range requirements of the device.

The low-side of the AMC1100 can be powered from a supply source with a nominal voltage of 3.0 V, 3.3 V, or 5.0 V. When operated at 5 V, the common-mode voltage of the output stage is set to 2.55 V nominal; in both other cases, the common-mode voltage is automatically set to 1.29 V.

Although usually applied in shunt-based current-sensing circuits, the AMC1100 can also be used for isolated voltage measurement applications, as shown in a simplified way in Figure 34. In such applications, usually a resistor divider (R_1 and R_2 in Figure 34) is used to match the relatively small input voltage range of the AMC1100. R_2 and the AMC1100 input resistance (R_{IN}) also create a resistance divider that results in additional gain error. With the assumption that R_1 and R_{IN} have a considerably higher value than R_2, the resulting total gain error can be estimated using Equation 1:

$$G_{ERRTOT} = G_{ERR} + \frac{R_2}{R_{IN}} \quad (1)$$

where:

- G_{ERR} = device gain error.

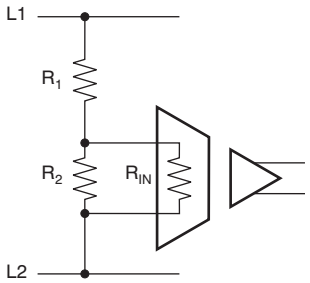


Figure 34. Voltage Measurement Application

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The AMC1100 offers unique linearity, high input common-mode rejection, and low dc errors and drift. These features make the AMC1100 a robust, high-performance isolation amplifier for industrial applications where users and subsystems must be protected from high voltage potentials.

8.2 Typical Applications

8.2.1 The AMC1100 in Frequency Inverters

A typical operation for the AMC1100 is isolated current and voltage measurement in frequency inverter applications (such as industrial motor drives, photovoltaic inverters, or uninterruptible power supplies), as conceptually shown in Figure 35. Depending on the end application, only two or three phase currents are being sensed.

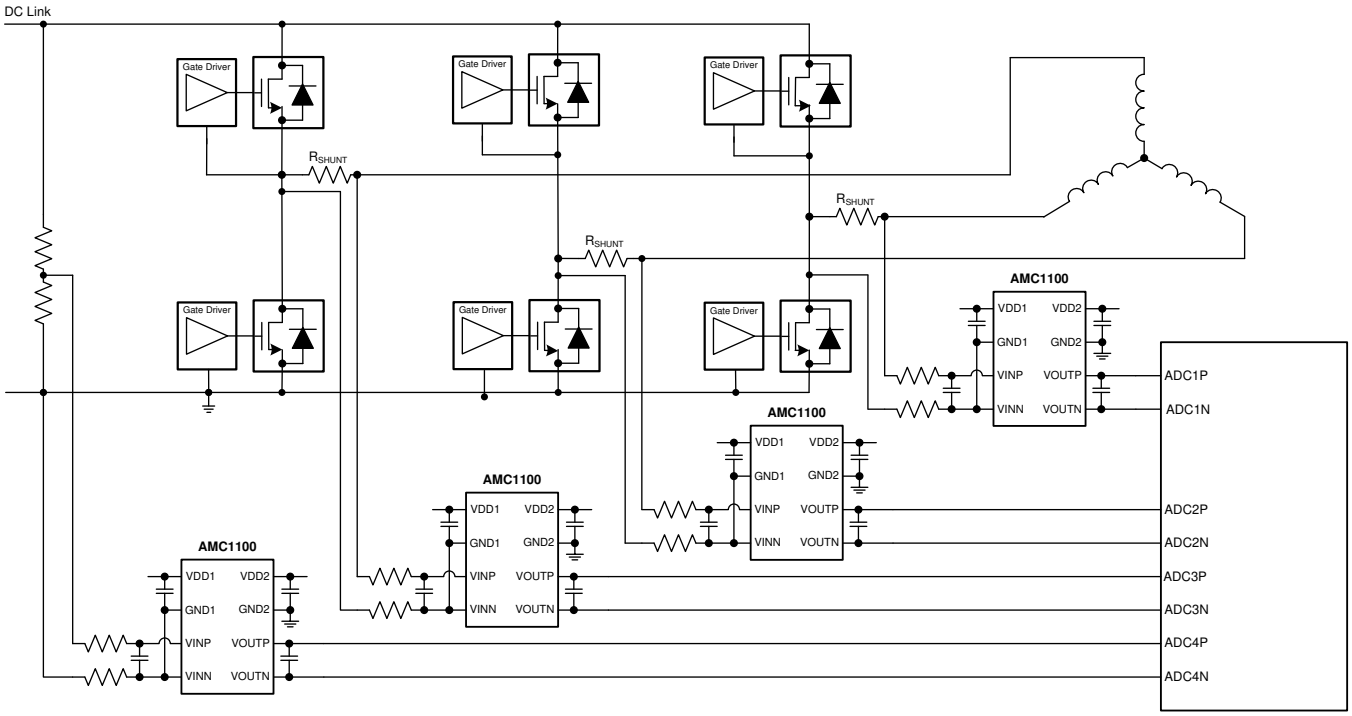


Figure 35. Isolated Current and Voltage Sensing in Frequency Inverters

8.2.1.1 Design Requirements

Current measurement through the phase of a motor power line is done via the shunt resistor R_{SHUNT} (in a two-terminal shunt); see Figure 36. For better performance, the differential signal is filtered using RC filters (components R_2, R_3, and C_2). Optionally, C_3 and C_4 can be used to reduce charge dumping from the inputs. In this case, care must be taken when choosing the quality of these capacitors; mismatch in values of these capacitors leads to a common-mode error at the modulator input. Using NP0 capacitors is recommended, if necessary.

Typical Applications (continued)

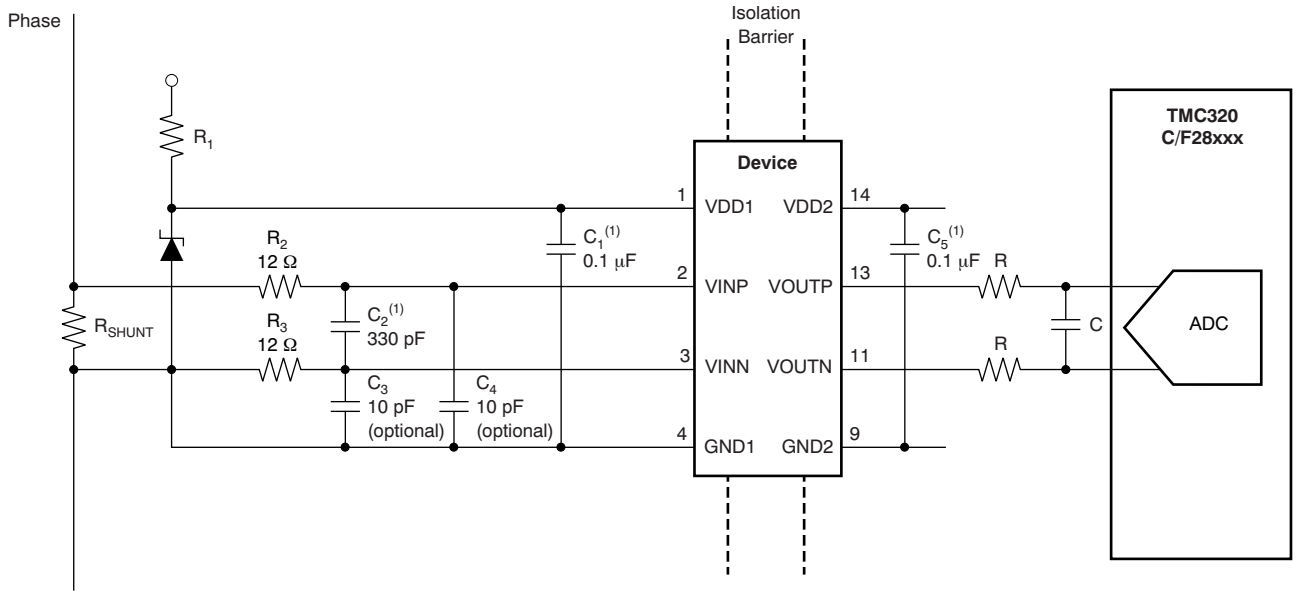


Figure 36. Shunt-Based Current Sensing with the AMC1100

The isolated voltage measurement can be performed as described in the *Device Functional Modes* section.

8.2.1.2 Detailed Design Procedure

The floating ground reference (GND1) is derived from the end of the shunt resistor, which is connected to the negative input of the AMC1100 (VINN). If a four-terminal shunt is used, the inputs of the AMC1100 are connected to the inner leads and GND1 is connected to one of the outer shunt leads. The differential input of the AMC1100 ensures accurate operation even in noisy environments.

The differential output of the AMC1100 can either directly drive an analog-to-digital converter (ADC) input or can be further filtered before being processed by the ADC.

8.2.1.3 Application Curve

In frequency inverter applications the power switches must be protected in case of an overcurrent condition. To allow fast powering off of the system, low delay caused by the isolation amplifier is required. Figure 37 shows the typical full-scale step response of the AMC1100.

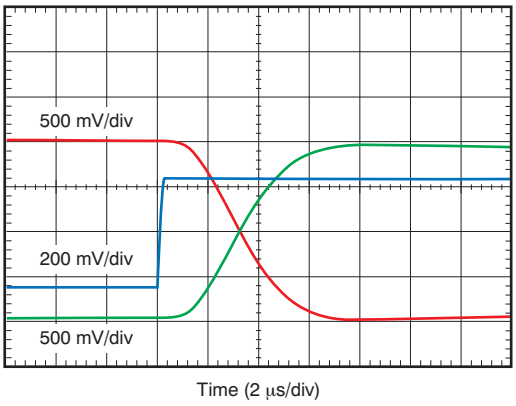


Figure 37. Typical Step Response of the AMC1100

Typical Applications (continued)

8.2.2 The AMC1100 in Energy Metering

Resulting from its immunity to magnetic fields, the AMC1100 can be used for shunt-based current sensing in smart electricity meter (e-meter) designs, as shown in Figure 38. Three AMC1100 devices are used for isolated current sensing. For voltage sensing, resistive dividers are usually used to reduce the common-mode voltage to levels that allow non-isolated measurement.

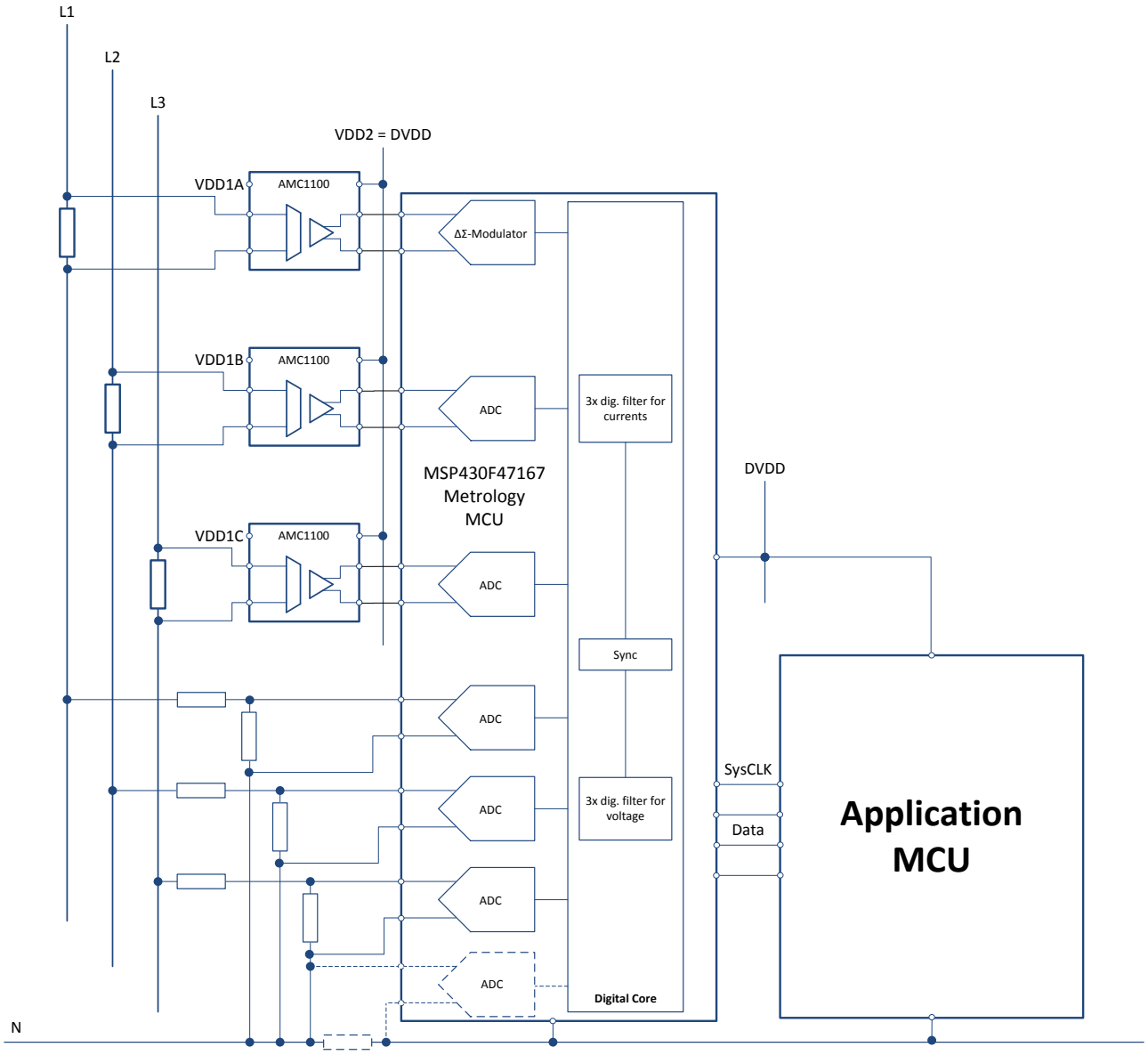


Figure 38. The AMC1100 in an E-Meter Application

8.2.2.1 Design Requirements

For best performance, an RC low-pass filter can be used in front of the AMC1100. Further improvement can be achieved by filtering the output signal of the device. In both cases, the values of the resistors and the capacitors must be tailored to the bandwidth requirements of the system.

Typical Applications (continued)

The analog output of the device is converted to the digital domain using the on-chip analog-to-digital converters (ADCs) of a suitable metrology microcontroller. The architecture of the MSP430F471x7 family of ultra-low power microcontrollers is tailored for this kind of applications. The MSP430F471x7 offers up to seven ADCs for simultaneous sampling: six of which are used for the three phase currents and voltages whereas the seventh channel can be used for additional voltage sensing of the neutral line for applications that require anti-tampering measures.

8.2.2.2 Detailed Design Procedure

The high-side supply for the AMC1100 can be derived from the phase voltage using a capacitive-drop power supply (cap-drop), as shown in Figure 39 and described in the application report SLAA552, *AMC1100: Replacement of Input Main Sensing Transformer in Inverters with Isolate Amplifier*.

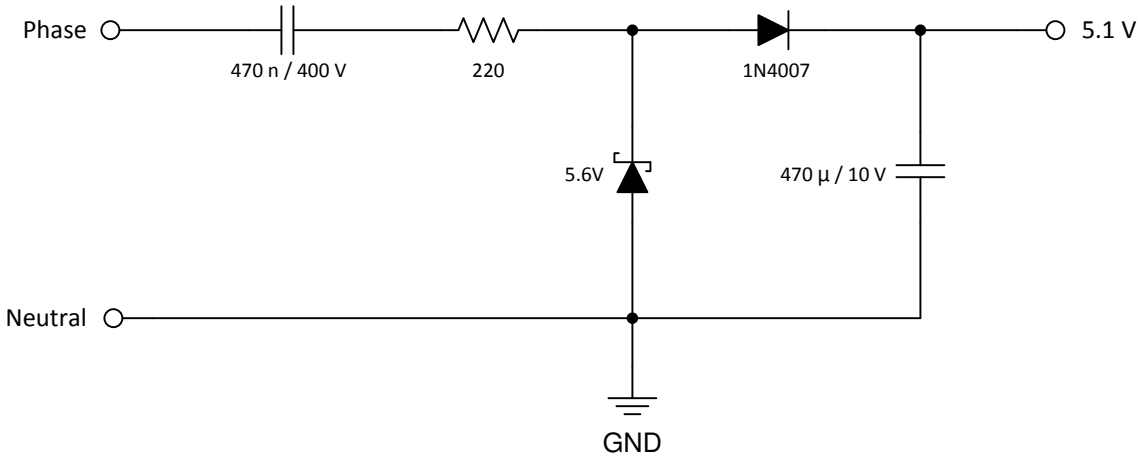


Figure 39. Cap-Drop High-Side Power Supply for the AMC1100

Alternatively, the high-side power supply for each AMC1100 can also be derived from the low-side supply using the SN6501 to drive a transformer, as proven by the TI reference design TIPD121, *Isolated Current Sensing Reference Design Solution, 5A, 2kV*.

8.2.2.3 Application Curve

One of the key parameters of an e-meter is its noise performance, which is mainly influenced by the performance of the ADC and the current sensor. When using a shunt-based approach, the sensor front-end consists of the actual shunt resistor and the isolated amplifier. Figure 40 shows the typical output noise density of the AMC1100 as a basis for overall performance estimations.

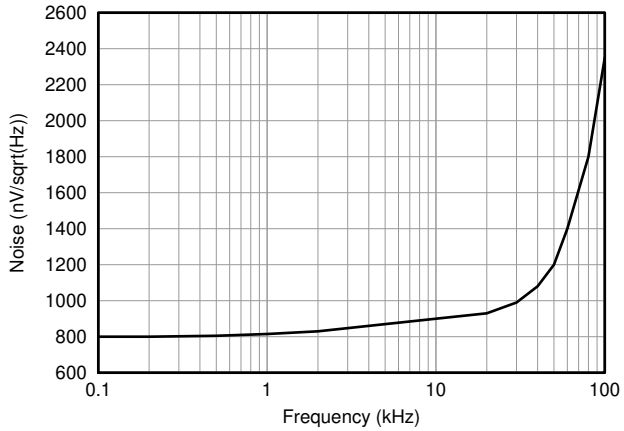


Figure 40. Output Noise Density of the AMC1100

9 Power Supply Recommendations

In a typical frequency inverter application, the high-side power supply for the AMC1100 (VDD1) is derived from the system supply, as shown in Figure 41. For lowest cost, a Zener diode can be used to limit the voltage to 5 V ± 10%. A 0.1-µF decoupling capacitor is recommended for filtering this power-supply path. Place this capacitor (C_1) as close as possible to the VDD1 pin for best performance. If better filtering is required, an additional 1-µF to 10-µF capacitor can be used.

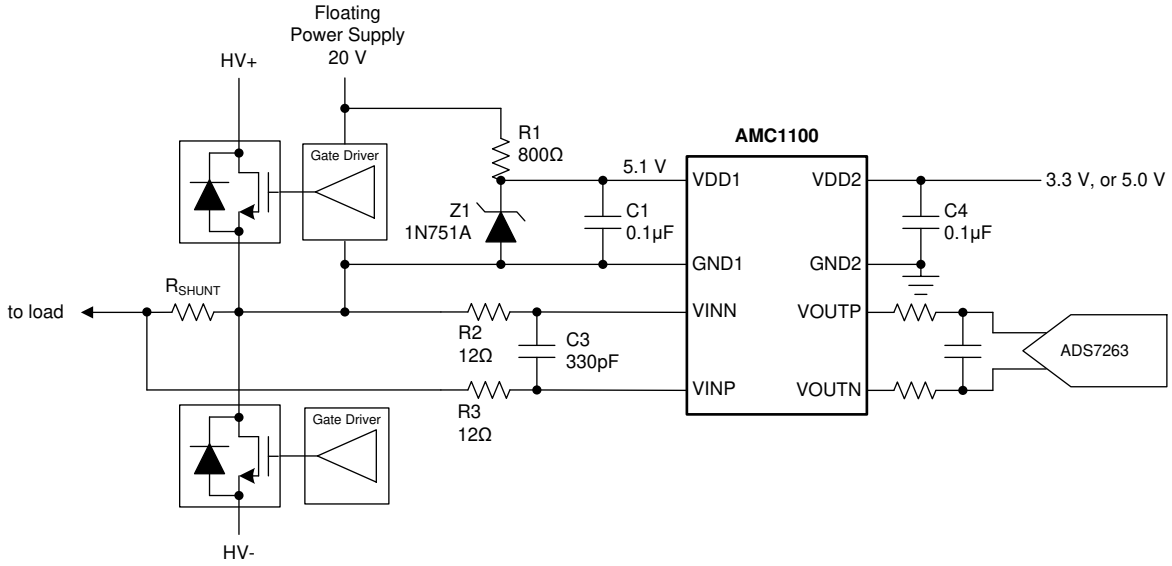


Figure 41. Zener Diode Based High-Side Supply

For higher power efficiency and better performance, a buck converter can be used; an example of such an approach is based on the LM5017. A reference design including performance test results and layout documentation can be downloaded at PMP9480, *Isolated Bias Supplies + Isolated Amplifier Combo for Line Voltage or Current Measurement*.

10 Layout

10.1 Layout Guidelines

A layout recommendation showing the critical placement of the decoupling capacitors that be placed as close as possible to the AMC1100 while maintaining a differential routing of the input signals is shown in Figure 42.

To maintain the isolation barrier and the common-mode transient immunity (CMTI) of the device, keep the distance between the high-side ground (GND1) and the low-side ground (GND2) at a maximum; that is, the entire area underneath the device must be kept free of any conducting materials.

10.2 Layout Example

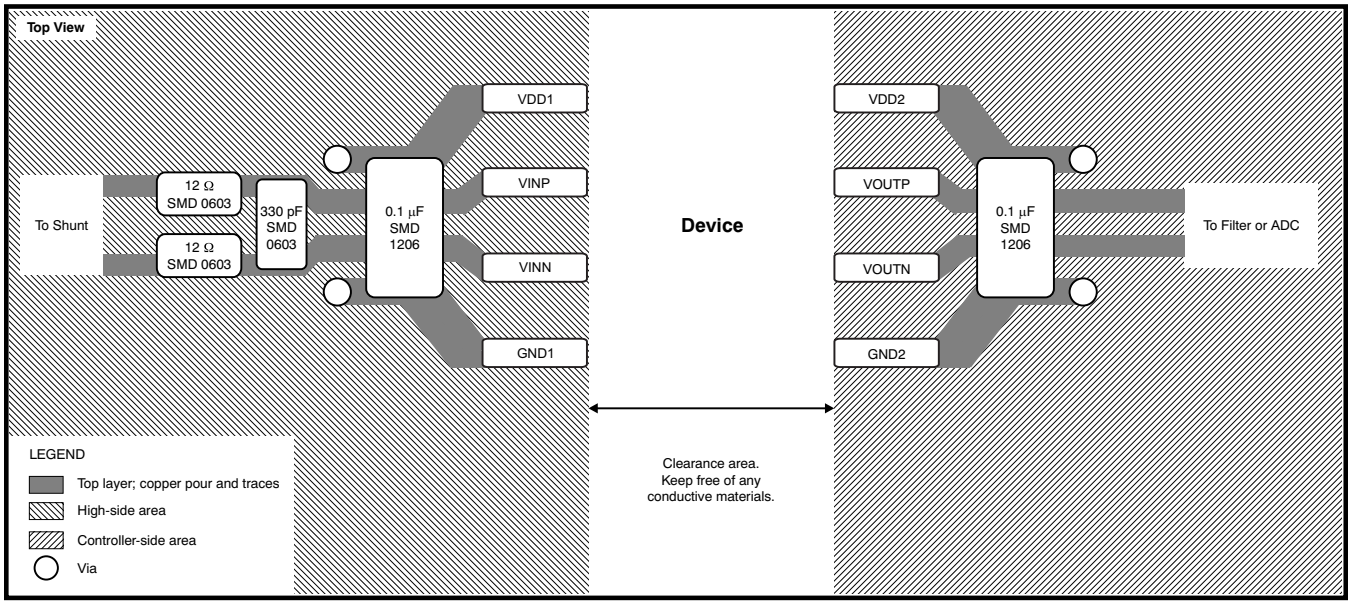


Figure 42. Example Layout

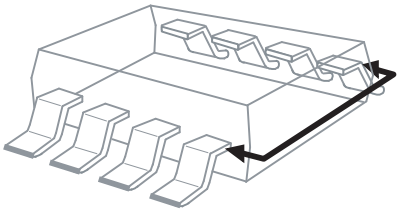
11 器件和文档支持

11.1 器件支持

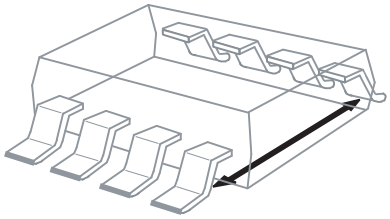
11.1.1 器件命名规则

11.1.1.1 隔离相关术语

爬电距离：沿绝缘材料表面测得的两个输入到输出导电引线间的最短路径。最短距离路径在器件封装体的末端附近位置。



电气间隙：两个输入到输出导电引线间测得的最短空间（视线）距离。



输入到输出势垒电容：所有连在一起的输入端子与所有连在一起的输出端子之间的总电容。

输入到输出势垒电阻：所有连在一起的输入端子与所有连在一起的输出端子之间的总电阻。

初级电路：此类电路为内部电路，直接与外部电源或其它为初级电路供电的等效电源相连。

次级电路：此类电路并不直接与主电源相连，而是由单独的隔离电源供电。

相对电痕指数 (CTI)：CTI 是一个用于电气绝缘材料的指数。该指数被定义为标准测试期间因漏电起痕导致故障的电压数值。在漏电起痕过程中，绝缘表面或靠近绝缘表面的位置上会发生放电，进而在绝缘材料表面或内部产生局部受损的部分导电路径。绝缘材料的 CTI 值越高，最短爬电距离越小。

绝缘击穿通常发生在绝缘材料内部或表面上，也可能在两处同时发生。导致表面损伤的原因可能是：飞弧现象或者因局部小火花所导致的绝缘表面逐渐老化。这类火花是绝缘材料上的导电污染物表面膜形成断点所导致。这种断点会对泄漏电流产生影响，进而在中断位置产生过电压，并生成电火花。这些火花通常会导致绝缘材料碳化，致使不同电位点之间形成碳轨迹。这一过程称为*漏电起痕*。

11.1.1.1.1 绝缘：

工作绝缘 - 设备正常运行所需的绝缘。

基本绝缘 — 针对电击现象提供基本保护的绝缘。

辅助绝缘 — 除基本绝缘外可应用的独立绝缘，可确保在基本绝缘出现故障时提供防电击保护。

双重绝缘 — 同时具有基本绝缘和辅助绝缘的绝缘。

强化绝缘 — 防电击保护等级等效于双重绝缘的单一绝缘系统。

11.1.1.1.2 污染等级：

污染等级 1 — 无污染或仅存在干燥的非导电性污染。此污染等级对器件性能没有任何影响。

污染等级 2 — 通常仅存在非导电性污染。不过，应预料到可能会因为凝露而出现暂时的导电性。

污染等级 3 — 存在导电污染或者由于凝露的作用而变成导电性污染的干燥非导电性污染。将会出现凝露。

污染等级 4 — 由于导电性粉尘、雨水或其它潮湿状况而导致的持久导电性污染。

器件支持 (接下页)

11.1.1.1.3 安装类别：

过电压类别 — 本节旨在通过确定可能出现的瞬态过电压并根据 IEC 60664 标准指定的四个不同等级来进行绝缘协调。

I. 信号级：特殊设备或设备零部件。
II. 现场级：便携式设备等
III. 配电级：固定式安装。
IV. 一次侧电源级：架空线、电缆系统。

各类别的瞬态过电压要低于上述类别。

11.2 文档支持

11.2.1 相关文档

德州仪器 (TI)，*《ISO72x 系列数字隔离器高压使用寿命》* 应用报告

德州仪器 (TI)，*《ISO72x 数字隔离器磁场抗扰度》* 应用报告

德州仪器 (TI)，*《AMC1100：使用隔离放大器替换逆变器中的输入主感应变压器》* 应用报告

德州仪器 (TI)，*《5A、2kV 隔离式电流感应参考设计解决方案》* 参考指南

德州仪器 (TI)，*《用于线路电压或电流测量的 PMP9480 隔离式偏置电源 + 隔离式放大器组合》*

德州仪器 (TI)，*《TPS6212x 15V、75mA 高效降压转换器》* 数据表

德州仪器 (TI)，*《MSP430F471xx 混合信号微控制器》* 数据表

德州仪器 (TI)，*《SN6501 用于隔离式电源的变压器驱动器》*数据表

德州仪器 (TI)，*《LM5017 100V、600mA 恒定导通时间同步降压稳压器》* 数据表

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 商标

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11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1100DUB	ACTIVE	SOP	DUB	8	50	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 105	AMC1100	Samples
AMC1100DUBR	ACTIVE	SOP	DUB	8	350	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC1100	Samples
AMC1100DWV	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	AMC1100	Samples
AMC1100DWVR	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	AMC1100	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

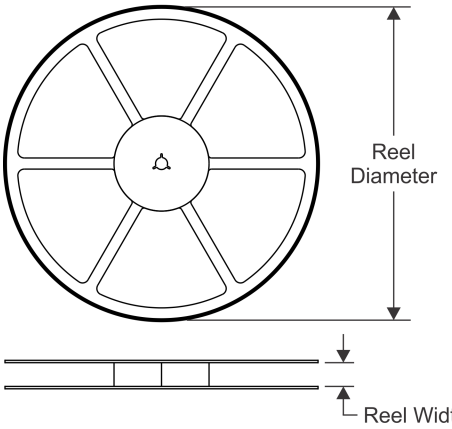
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

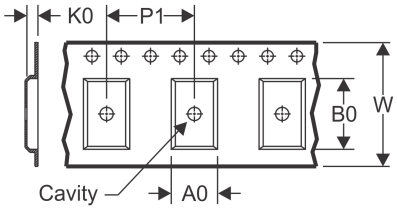
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

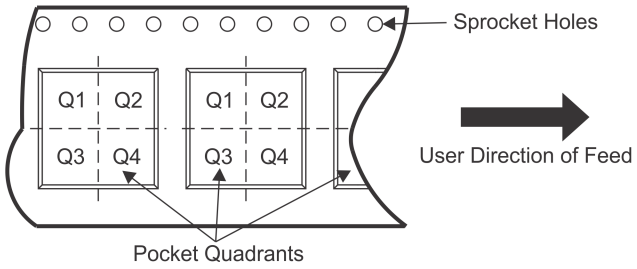


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

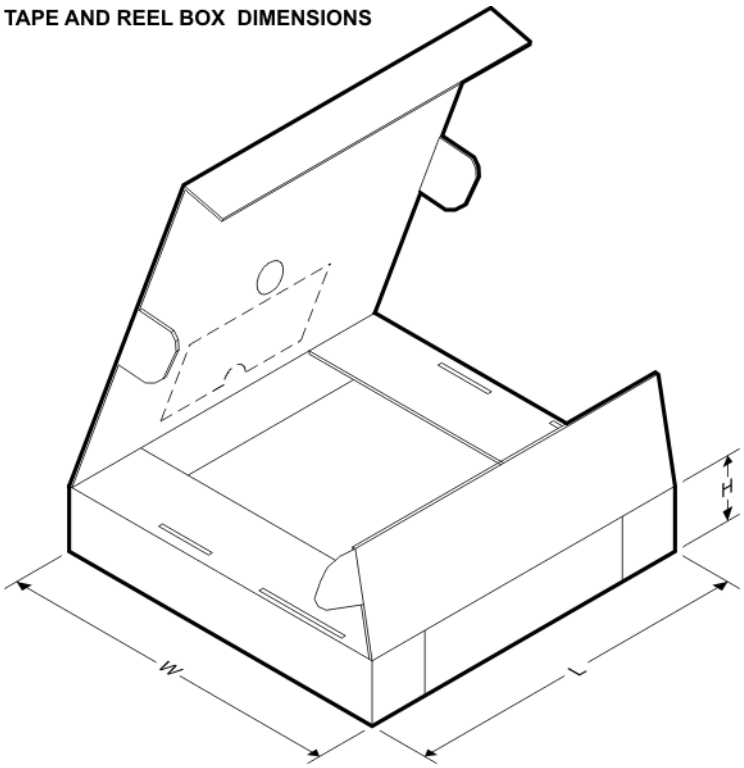
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1100DUBR	SOP	DUB	8	350	330.0	24.4	10.9	10.01	5.85	16.0	24.0	Q1
AMC1100DUBR	SOP	DUB	8	350	330.0	24.4	13.1	9.75	6.0	16.0	24.0	Q1
AMC1100DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

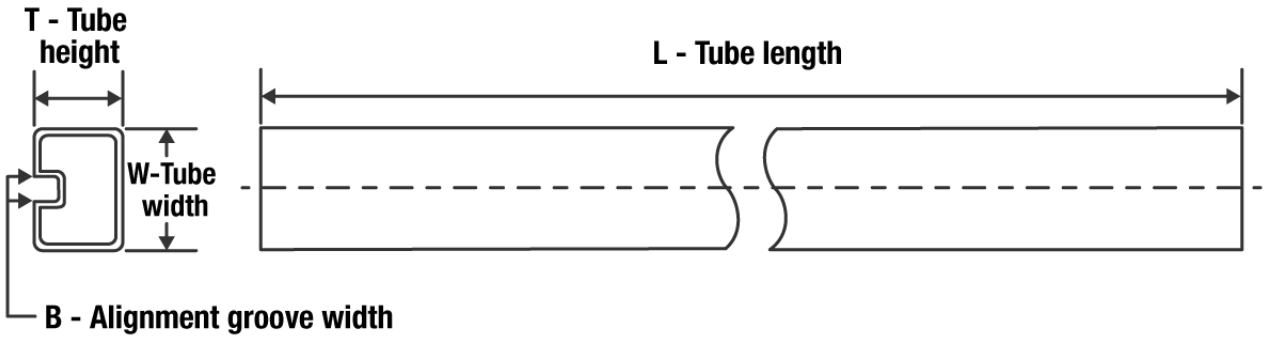
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1100DUBR	SOP	DUB	8	350	346.0	346.0	29.0
AMC1100DUBR	SOP	DUB	8	350	367.0	367.0	45.0
AMC1100DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0

TUBE



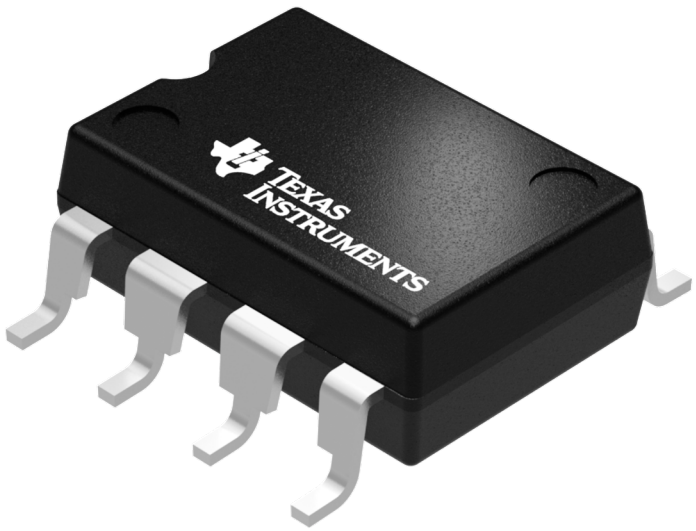
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AMC1100DUB	DUB	SOP	8	50	532.13	13	7300	6.6
AMC1100DUB	DUB	SOP	8	50	532.13	13.51	7.36	6.91
AMC1100DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6

GENERIC PACKAGE VIEW

DUB 8 SOP - 4.85 mm max height

SMALL OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

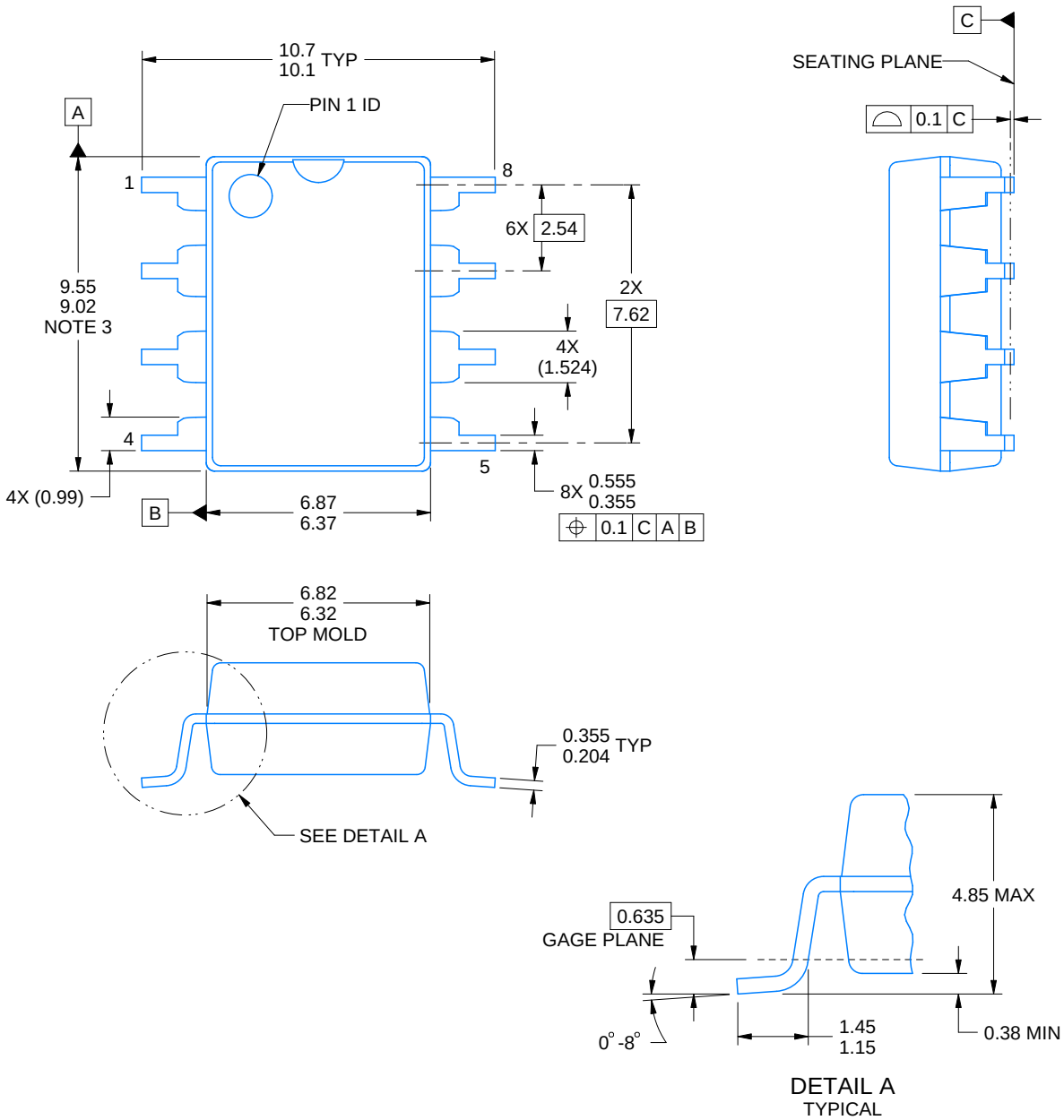
4207614/E

PACKAGE OUTLINE

DUB0008A

SOP - 4.85 mm max height

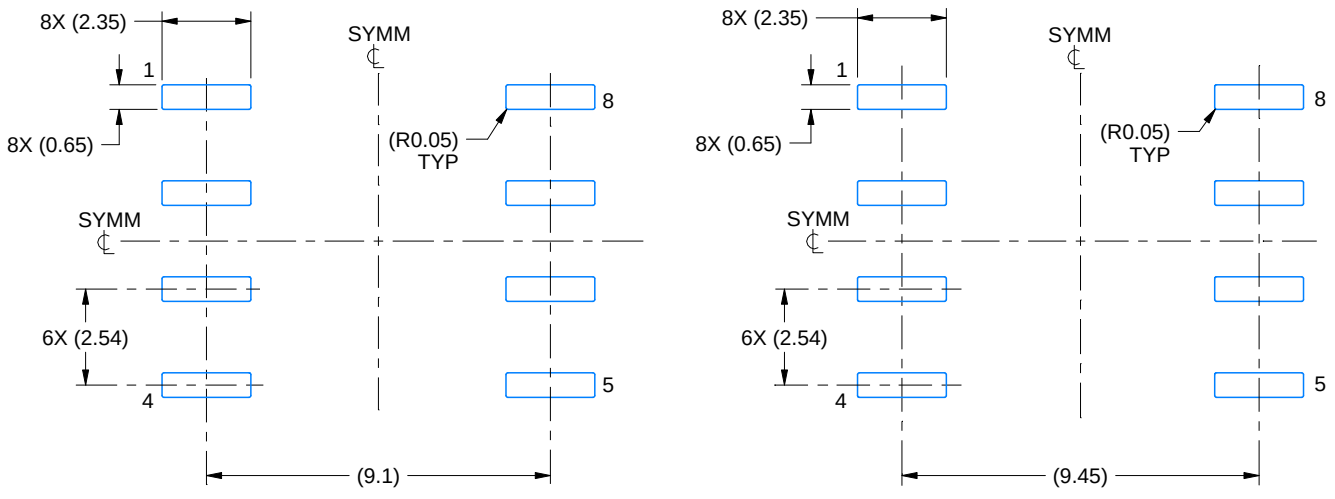
SMALL OUTLINE PACKAGE



4222355/G 04/2019

NOTES:

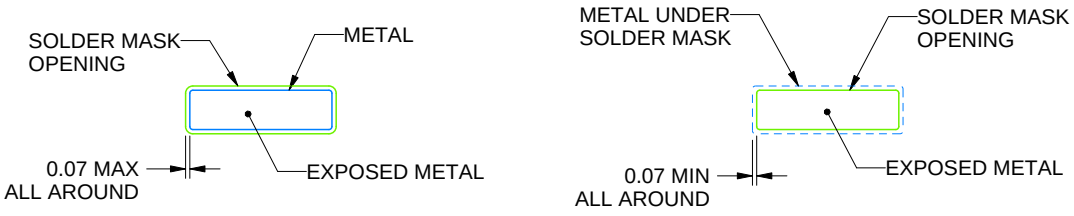
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.254 mm per side.



IPC-7351 NOMINAL
6.75 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
7.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLES
EXPOSED METAL SHOWN
SCALE:5X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4222355/G 04/2019

NOTES: (continued)

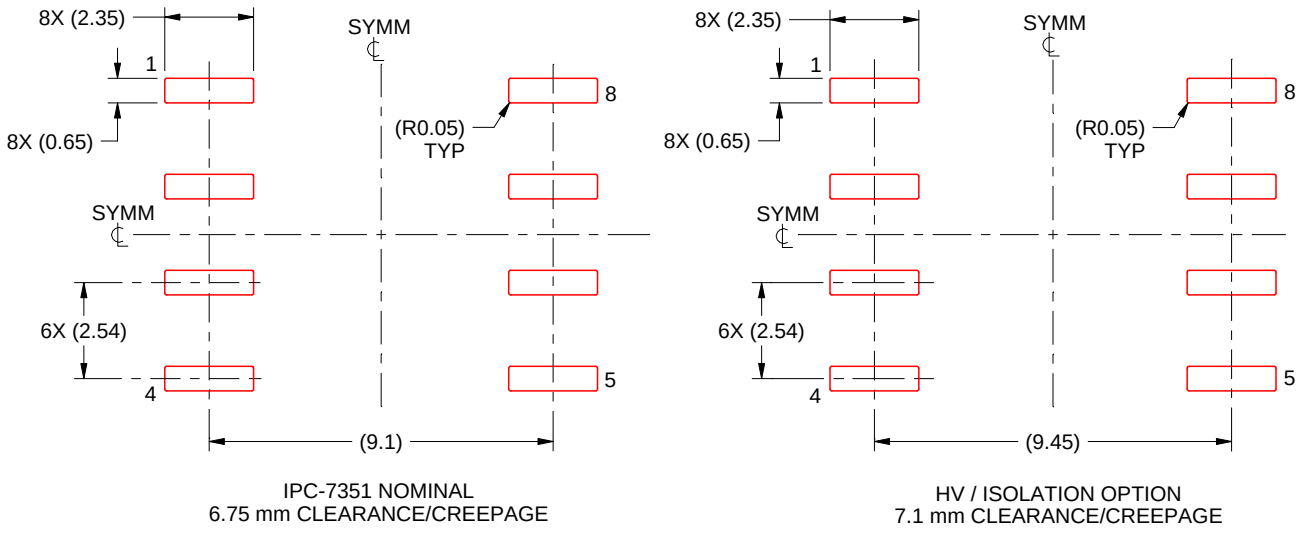
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DUB0008A

SOP - 4.85 mm max height

SMALL OUTLINE PACKAGE



IPC-7351 NOMINAL
6.75 mm CLEARANCE/CREEPAGE

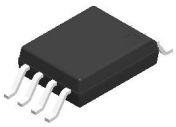
HV / ISOLATION OPTION
7.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:5X

4222355/G 04/2019

NOTES: (continued)

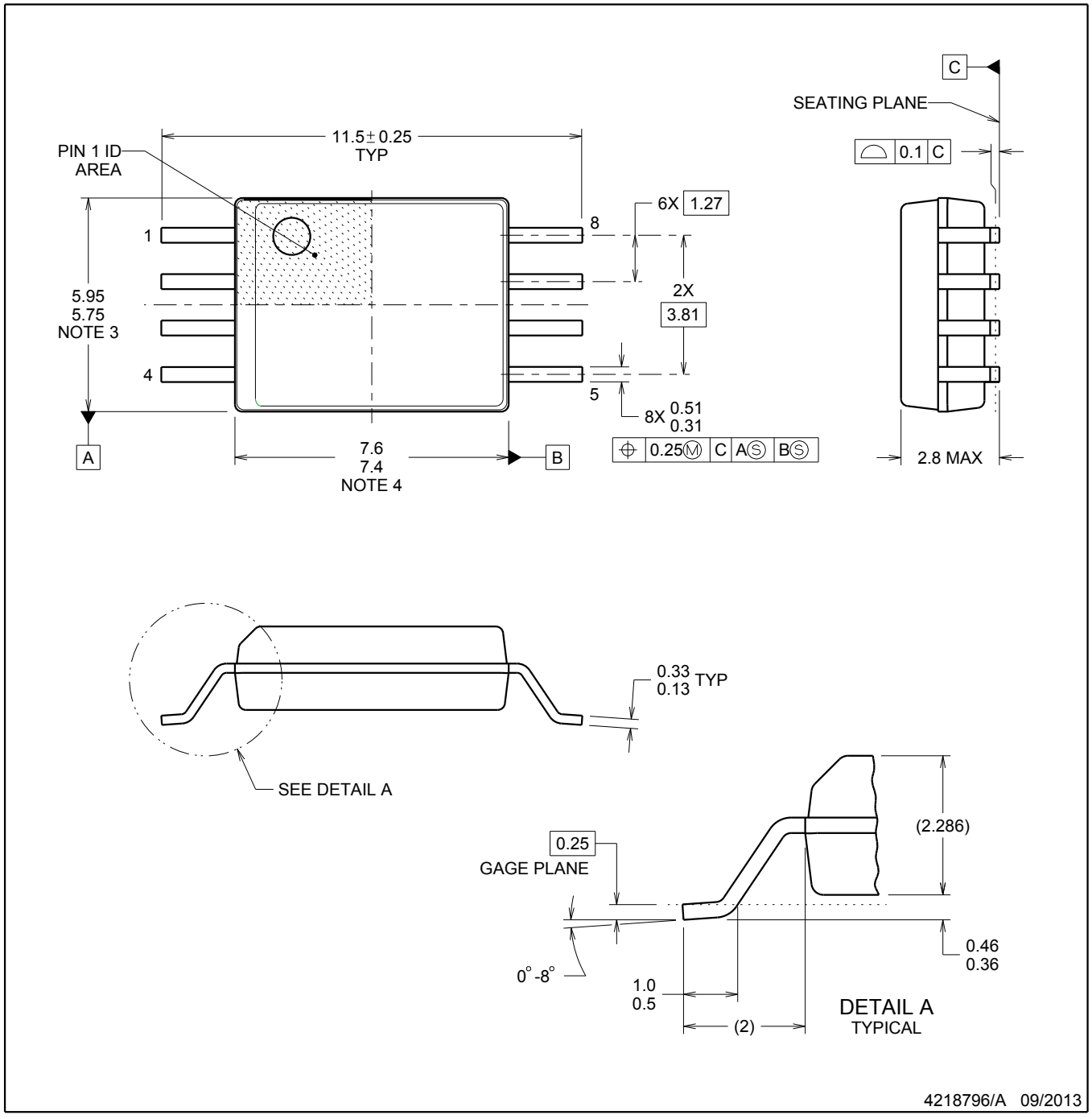
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



DWV0008A

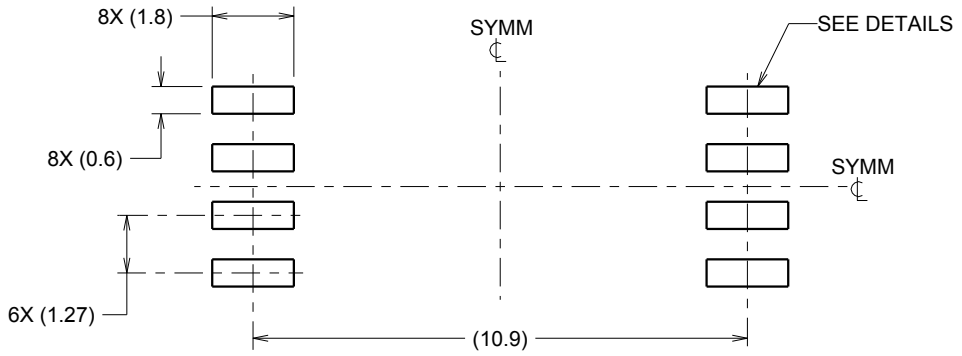
SOIC - 2.8 mm max height

SOIC

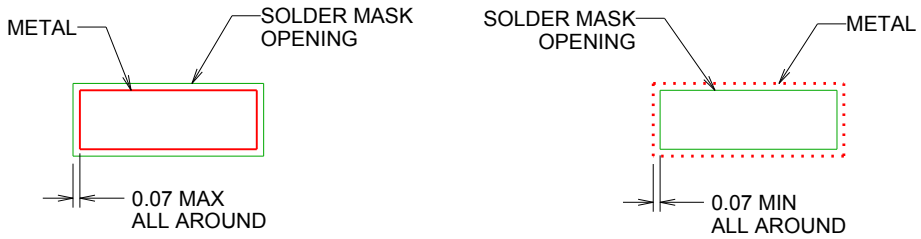


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

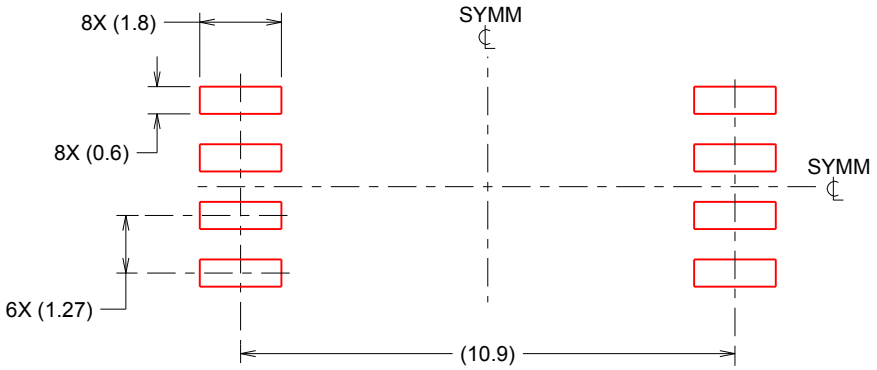
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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