TEXAS INSTRUMENTS
BQ2961, BQ2962
ZHCSE10N – NOVEMBER 2013 – REVISED JUNE 2021

适用于 2 节、3 节和 4 节串联锂离子电池且具有稳压输出电源的 BQ296xxx 过压保护器

1 特性

- 2 节、3 节和 4 节串联电池过压保护 (OVP)
- 固定延迟计时器，用于触发 FET 驱动输出（3s、4s、5.5s 或 6.5s 四种选项）
- 出厂设定的 OVP 阈值（阈值电压范围为 3.85V 至 4.6V）
- 输出选项：高电平有效
- 高精度过压保护：±10mV
- 具有自禁能和/或外部使能/禁能控制功能的稳压电源输出
  - 选项：3.3V、2.5V 和 1.8V (BQ2961)
  - 选项：3.3V、3.15V、3.0V (BQ2962)
- 低功耗 I_{CC} ~ 4μA ($V_{CELL(ALL)} < V_{PROTECT}$)
- 禁用稳压输出时具有超低功耗，I_{CC} 约为 1.2μA
- 每个电池输入的低泄漏电流<100nA
- 小型封装引脚尺寸
  - 8 引脚 WSON (2mm × 2mm)

2 应用

- 笔记本电脑
- 超极本
- 医疗
- UPS 备用电池

3 说明

BQ296xxx 系列是一款高精度、低功耗过压保护器，具有适用于锂离子电池组应用的 2mA 稳压输出电源。

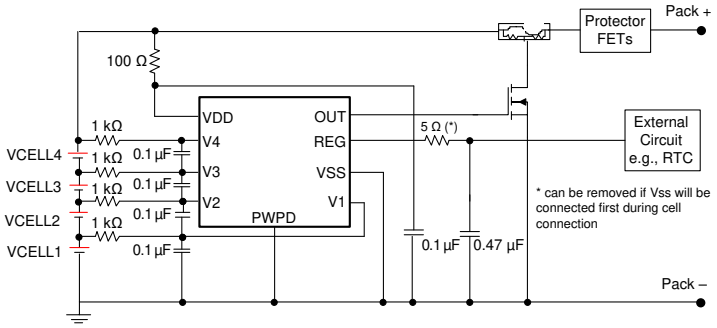
该器件可为 2-4 节串联电池组中的每节电池单独监视过压情况。当检测到任意电池上存在过压状态时，即会启动内部固定延迟计时器。延迟计时器到期后，输出引脚将被触发进入活动状态以指示发生过压情况。

稳压输出电源最高可提供 2mA（最大值）输出电流，以驱动始终接通的电路，例如实时时钟 (RTC) 振荡器。BQ296xxx 系列具有自禁能功能，能够在任意一节电池的电压低于特定阈值时关闭稳压输出，从而防止电池电量耗尽；该器件还可通过外部控制对稳压输出进行启能或禁能。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
BQ2961	WSON (8)	2.00mm × 2.00mm
BQ2962		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision M (June 2021) to Revision N (June 2021) **Page**

- Added the BQ296227 and BQ296233 PRODUCT PREVIEW devices to the *Device Comparison Table* 3

Changes from Revision L (February 2020) to Revision M (June 2021) **Page**

- Added the BQ296115 device to the *Device Comparison Table* 3

Changes from Revision K (February 2020) to Revision L (February 2021) **Page**

- 删除了整个数据表中的 BQ2960 引用..... 1
- Added the BQ296116 device to the *Device Comparison Table* 3

Changes from Revision J (December 2019) to Revision K (February 2020) **Page**

- Added the BQ296229, BQ296230, BQ296231, and BQ296232 devices to the *Device Comparison Table* 3

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5 Device Comparison Table

表 5-1. BQ2961 Device Options

BQ2961	OVP (V)	OVP DELAY (s)	UV (V)	LDO (V)
BQ296100	4.35	6.5	2.5	3.3
BQ296103	4.50	6.5	2.5	3.3
BQ296106	4.45	6.5	2.8	3.3
BQ296107	4.50	6.5	2.8	3.3
BQ296111	4.45	4.0	2.5	3.3
BQ296112	4.50	3.0	2.5	3.3
BQ296113	4.35	3.0	2.5	3.3
BQ296114	4.50	4.0	2.5	3.3
BQ296115(1)	4.25	6.5	2.0	2.5
BQ296116(2)	4.50	6.5	2.5	1.8
BQ2961	3.85 V – 4.60 V (50-mV step)	3.0, 4.0, 5.5, 6.5	2.0 V – 2.8 V (50-mV step)	1.8, 2.5, 3.3

(1) PRODUCT PREVIEW only
(2) PRODUCT PREVIEW. Contact TI for more information.

表 5-2. BQ2962 Device Options

BQ2962	OVP (V)	OVP DELAY (s)	UV (V)	LDO (V)
BQ296202	4.45	6.5	2.5	3.3
BQ296203	4.50	6.5	2.5	3.3
BQ296212	4.50	3.0	2.5	3.3
BQ296213	4.35	3.0	2.5	3.3
BQ296215	4.50	6.5	2.5	3.0
BQ296216	4.55	6.5	2.5	3.0
BQ296217	4.55	6.5	2.8	3.3
BQ296221	4.55	6.5	2.5	3.3
BQ296222	4.50	6.5	3.0	3.0
BQ296223	4.50	6.5	2.5	3.3
BQ296224	4.50	6.5	2.5	3.0
BQ296226	4.5	6.5	2.8	3.3
BQ296227(1)	4.55	6.5	2.8	3.3
BQ296228	4.55	6.5	2.5	3.0
bq296229	4.60	6.5	2.5	3.0
BQ296230	4.35	6.5	3.0	3.0
BQ296231	4.60	6.5	2.5	3.3
BQ296232	4.55	6.5	3.0	3.0
BQ296233(1)	4.45	6.5	2.5	3.3
BQ2962	3.85 V – 4.60 V (50-mV step)	3.0, 4.0, 5.5, 6.5	2.0 V – 2.8 V (50-mV step)	3, 3.15, 3.3

(1) PRODUCT PREVIEW only

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6 Pin Configuration and Functions

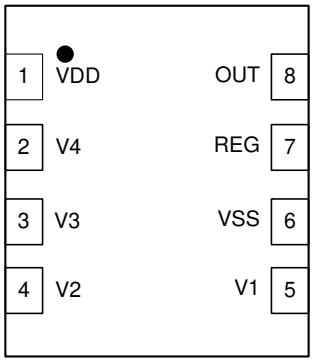


图 6-1. 2-Series to 4-Series BQ2961 (Top View)

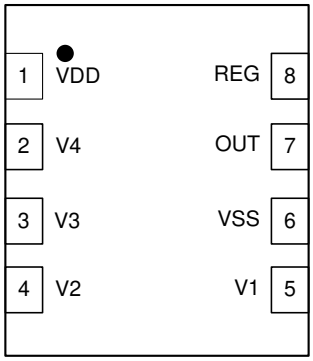


图 6-2. 2-Series to 4-Series BQ2962 (Top View)

表 6-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	BQ2961	BQ2962		
OUT	8	7	OA	Analog output drive for an overvoltage fault signal; CMOS output high or open-drain active low
PWPD	9	9	P	TI recommends connecting the exposed pad to VSS on PCB.
REG	7	8	OA	Regulated supply output. Requires an external ceramic capacitor for stability
REG_EN	—	—	IA	Regulated supply output enable. A "high" to enable REG output and "low" to disable REG output
V1	5	5	IA	Sense input for positive voltage of the lowest cell from the bottom of the stack
V2	4	4	IA	Sense input for positive voltage of the second cell from the bottom of the stack
V3	3	3	IA	Sense input for positive voltage of the third cell from the bottom of the stack
V4	2	2	IA	Sense input for positive voltage of the fourth cell from the bottom of the stack
VDD	1	1	P	Power supply input
VSS	6	6	P	Electrically connected to integrated circuit ground and negative terminal of the lowest cell in the stack

(1) IA = Analog input, OA = Analog Output, P = Power connection

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	VDD – VSS	–0.3	30	V
Input voltage	V4 – V3, V3 – V2, V2 – V1, V1 – VSS	–0.3	30	
	REG – VSS	–0.3	3.6	
	REG_EN – VSS	–0.3	28	
Output voltage	OUT – VSS	–0.3	30	
Continuous total power dissipation, P_{TOT}		See 节 7.4.		
Lead temperature (soldering, 10 s), T_{SOLDER}		300	300	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Procedures*. Exposure to absolute-maximum – rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (1)	Supply voltage, V_{DD} (1)	3		20	V
	Supply voltage, V_{DD} with REG output on	4			
Input voltage range	V_n – V_{n-1}, V1 – VSS	0		5	V
	REG_EN	0		15	V
Operating ambient temperature range, T_A		–40		110	°C

(1) See 节 9.2.

7.4 Thermal Information

THERMAL METRIC(1)		BQ296xxx DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	72	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	10	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

Typical values stated where T_A = 25°C and VDD = 14.4 V, MIN/MAX values stated where T_A = –40°C to +110°C, and V_{DD} = 3 V to 15 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Voltage Protection Thresholds							
V_{OV}	$V_{(PROTECT)}$ Overvoltage Detection	R_{IN} = 1 kΩ		Applicable Voltage: 3.85 V to 4.6 V in 50-mV steps			V
V_{HYS}	OV Detection Hysteresis			250	300	400	mV
V_{OA}	OV Detection Accuracy	T_A = 25°C		–10		10	mV
$V_{OADRIFT}$	OV Detection Accuracy Across Temperature	T_A = –40°C		–40		40	mV
		T_A = 0°C		–20		20	mV
		T_A = 60°C		–24		24	mV
		T_A = 110°C		–54		54	mV
		T_A = 110°C		–54		54	mV
Supply and Leakage Current							
I_{DD}	Supply Current with REG on	(V_n – V_{n-1}) = 2 V to 4.15 V, n = 1 to 4, VDD = top V_n voltage ($V1$ – V_{SS}) > V_{UVREG} , I_{REG} = 0 mA,	T_A = 0°C to 60°C		4	6	µA
			T_A = –40°C to 110°C			8	µA
I_{DD}	Supply Current with REG off	(V_n – V_{n-1}) = 2 V to 4.15 V, n = 1 to 4, VDD = top V_n voltage ($V1$ – V_{SS}) < V_{UVREG}	T_A = 0°C to 60°C		1	2	µA
			T_A = –40°C to 110°C			4	µA
I_{IN}	Input Current at V_x Pins	(V_n – V_{n-1}) = ($V1$ – V_{SS}) = 3.8 V, VDD = top V_n voltage, T_A = 25°C		–0.1		0.1	µA
Output Drive OUT, CMOS Active High							
V_{OUT}	Output Drive Voltage, Active High	(V_n – V_{n-1}) or ($V1$ – V_{SS}) > V_{OV}, I_{OH} = 100 µA, VDD = top V_n voltage		6	7	8	V
		If three of four cells are short circuited, only one cell remains powered and > V_{OV}, VDD = V_n (the remaining cell voltage), I_{OH} = 100 µA			VDD – 0.3		V
		(V_n – V_{n-1}) and ($V1$ – V_{SS}) < V_{OV}, VDD = sum of the cell stack voltage, I_{OL} = 100 µA measured into OUT pin			250	400	mV
I_{OUTH}	OUT Source Current (during OV)	(V_n – V_{n-1}), ($V3$ – $V2$), or ($V1$ – V_{SS}) > V_{OV}, VDD = top V_n voltage, forced OUT = 0 V, measured out of OUT pin				4.5	mA
I_{OUTL}	OUT Sink Current (no OV)	(V_n – V_{n-1}) and ($V1$ – V_{SS}) < V_{OV}, VDD = top V_n voltage, forced OUT = VDD, measured into OUT pin. Pull-up resistor R_{PU} = 5 kΩ to VDD		0.5		14	mA
Internal Fixed Delay Timer							
t_{DELAY}	OV Delay Time[1]	Internal Fixed Delay, 3-s delay option		2.4	3	3.6	s
		Internal Fixed Delay, 4-s delay option		3.2	4	4.8	s
		Internal Fixed Delay, 5.5-s delay option		4.4	5.5	6.6	s
		Internal Fixed Delay, 6.5-s delay option		5.2	6.5	7.8	s
t_{DELAY_CTM}	Fault Detection Delay Time in Test Mode OV Delay Time	Internal Fixed Delay			15		ms
t_{DELAY_RESET}	OV delay timer count reset time; t_{DELAY} resets when the cell voltage falls below V_{OV} for t_{DELAY_RESET}.[1]	Internal Fixed Delay			0.6		ms

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7.5 Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VDD = 14.4 V, MIN/MAX values stated where T_A = –40°C to +110°C, and V_{DD} = 3 V to 15 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Regulated Supply Output, REG							
V_{REG}	REG Supply at 500 µA load	VDD ⩾ 4 V, I_{REG} = 500 µA, C_{REG} = 0.47 µF	V_{REG} = 3.3 V,	3.234	3.300	3.366	V
			V_{REG} = 3.15 V, BQ2962	3.087	3.150	3.213	
			V_{REG} = 3.0 V, BQ2962	2.940	3.000	3.060	
			V_{REG} = 2.5 V, BQ2961	2.450	2.500	2.550	
			V_{REG} = 1.8 V, BQ2961	1.764	1.800	1.836	
V_{REG}	REG Supply from 0 to 2 mA load	VDD ⩾ 4 V, I_{REG} = 0 µA to 2 mA, C_{REG} = 0.47 µF	V_{REG} = 3.3 V, BQ2961, BQ2962	3.200	3.300	3.400	V
			V_{REG} = 3.15 V, BQ2962	3.050	3.150	3.250	
			V_{REG} = 3.0 V, BQ2962	2.900	3.000	3.100	
			V_{REG} = 2.5 V, BQ2961	2.425	2.500	2.575	
			V_{REG} = 1.8 V, BQ2961	1.746	1.800	1.854	
I_{REG}	REG Current Output	VDD ⩾ 4 V, C_{REG} = 0.47 µF		0		2	mA
$I_{REG_SC_Limit}$	REG Output Short Circuit Current Limit	REG = V_{SS}, C_{REG} = 0.47 µF		4			mA
R_{REG_PD}	REG pull-down resistor	REG is disabled.		20	30	45	kΩ
Regulated Supply Output Enable, REG_EN							
V_{IH}	High-level Input			1.6			V
V_{IL}	Low-level Input					0.4	V
I_{LKG}	Input Leakage Current	V_{IH} < 6 V				0.1	µA
Regulated Supply Undervoltage Self-Disable							
V_{UVREG}	Undervoltage detection	Factory Configuration: 2.0 V to 2.8 V in 50 mV steps, T_A = 25°C		–50		50	mV
V_{UVHYS}	Undervoltage Detection Hysteresis			250	300	400	mV
$t_{UVDELAY}$	Undervoltage Detection Delay			4.5	6	7.5	s
V_{UVQUAL}	Cell voltage to qualify for UV detection				0.5		V

(1) Specified by design. Not 100% tested in production.

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7.6 Typical Characteristics

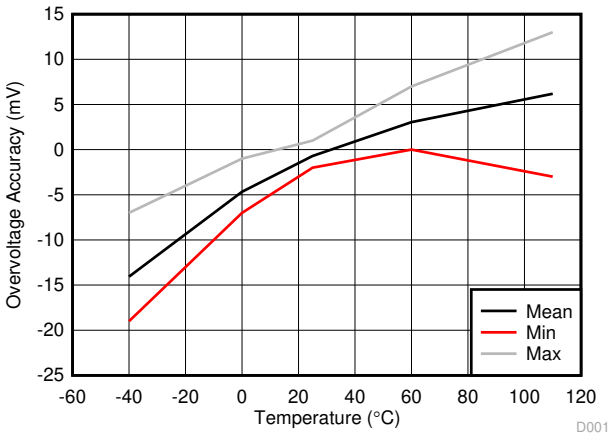


图 7-1. Overvoltage Threshold (V_{OV}) vs. Temperature

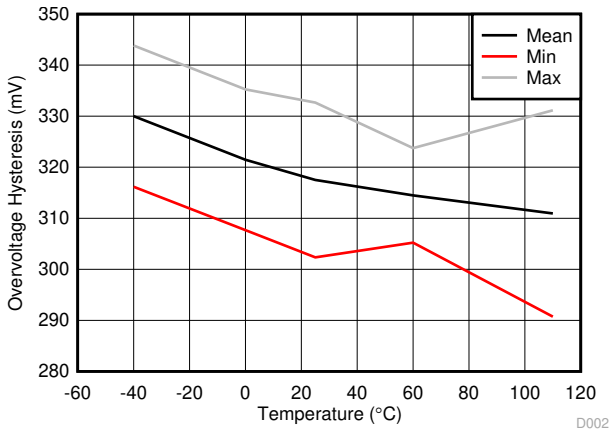


图 7-2. Hysteresis V_{HYS} vs. Temperature

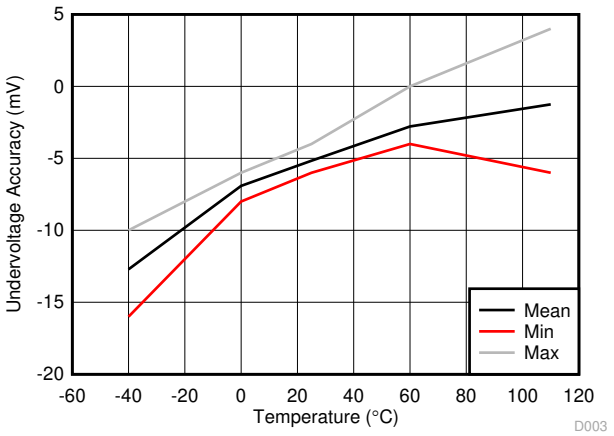


图 7-3. Undervoltage Accuracy

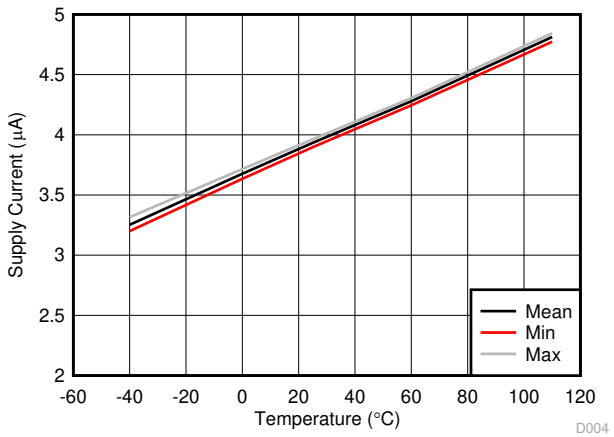


图 7-4. I_{DD} with Regulator On

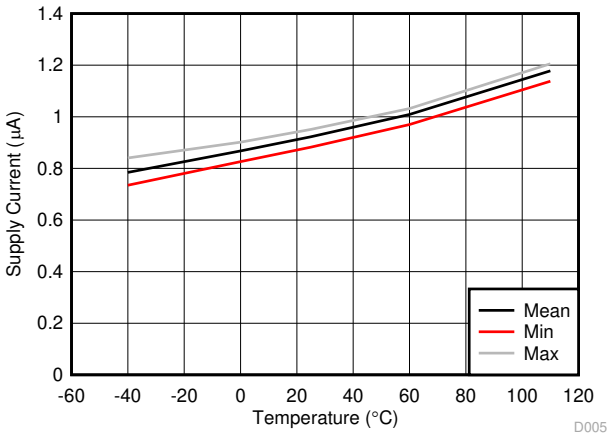


图 7-5. I_{DD} with Regulator Off

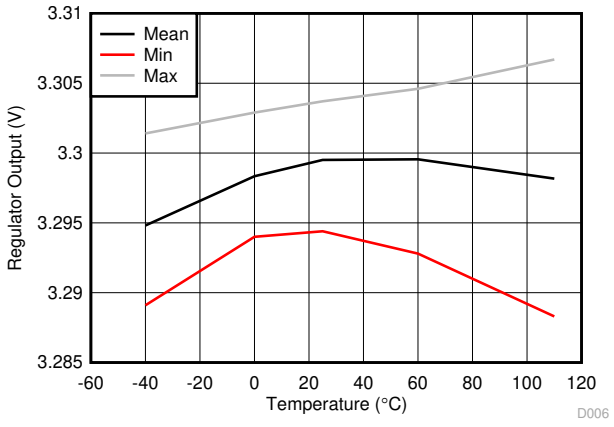


图 7-6. Regulator Output Without Load

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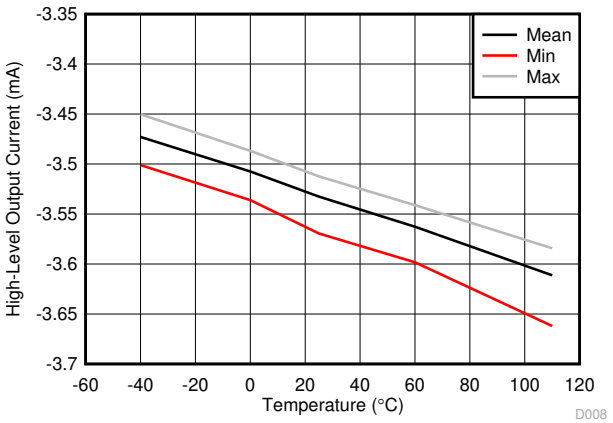


图 7-7. I_{OUTH} vs Temperature

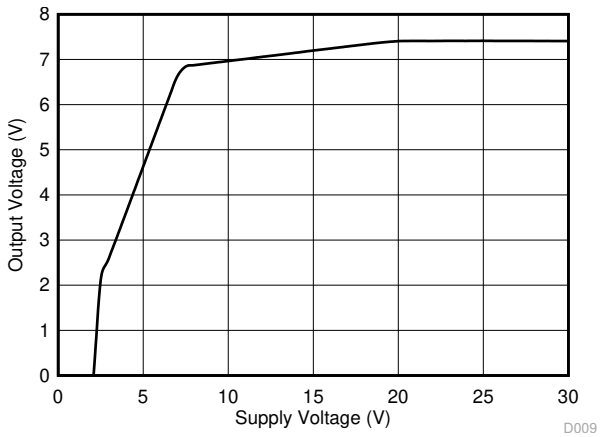


图 7-8. V_{OUT} vs V_{DD}

8 Detailed Description

8.1 Overview

The BQ2961 and BQ2962 devices are second-level overvoltage (OV) protectors with a regulated output. Each cell is monitored independently by comparing the actual cell voltage to an overvoltage threshold V_{OV}. The overvoltage threshold is preprogrammed at the factory with a range between 3.85 V to 4.65 V.

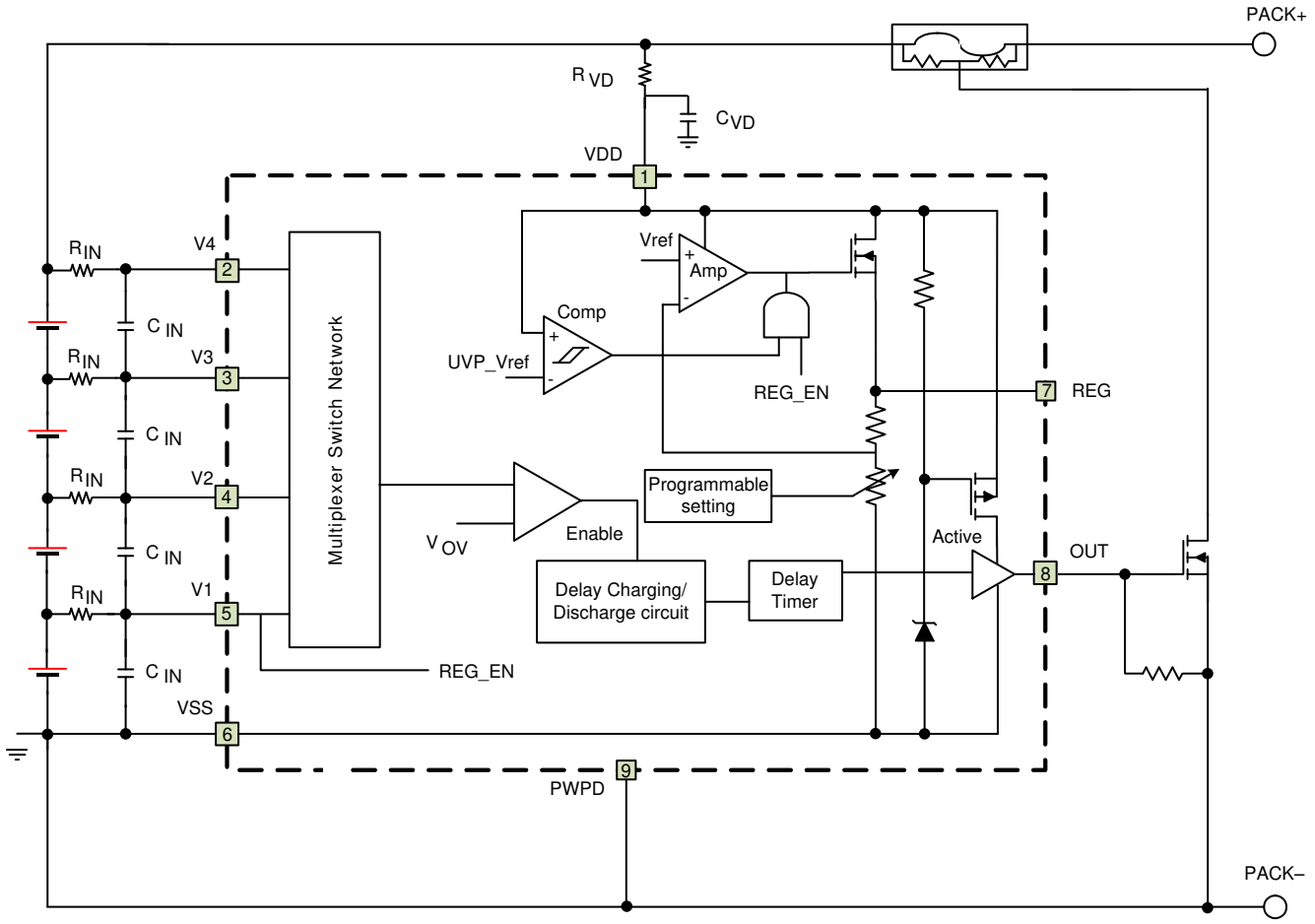
The regulated output is enabled unless any of the cell voltages fall below the V_{UVREG} threshold. This threshold is preprogrammed at the factory with a range between 2 V to 2.8 V.

表 8-1. Programmable Parameters

OVERVOLTAGE RANGE (V)	OVERVOLTAGE DELAY (s)	UNDERVOLTAGE RANGE (V)	REGULATOR (V)
3.85 to 4.6 in 50-mV step	3, 4, 5.5, 6.5	2.0 to 2.8 in 50-mV step	1.8, 2.5, 3.3 (BQ2961) 3.0, 3.15, 3.3 (BQ2962)

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8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Pin Details

8.3.1.1 Input Sense Voltage, Vx

These inputs sense each battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

8.3.1.2 Output Drive, OUT

This terminal serves as the fault signal output in active high.

8.3.1.3 Supply Input, VDD

This terminal is the unregulated input power source for the device. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

8.3.1.4 Regulated Supply Output, REG

This terminal is connected to an external capacitor and provides a regulated supply to power a circuit such as a real-time clock integrated circuit, or functions requiring a well-regulated supply. Maximum current load on this pin cannot exceed I_{REG} mA.

The REG output has protection for overcurrent, using a current limit protection circuit, and also detects and protects for excessive power dissipation due to short circuit of the external load. This pin requires a ceramic 1-µF capacitor connection to VSS for improved stability, noise immunity, and ESD performance of the supply output. This capacitor must be placed close to the REG and VSS pins for connection.

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8.3.2 Overvoltage Sensing for OUT

In the BQ296xxx device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{OV}. If any cell voltage exceeds the programmed OV value, an internal timer circuit is activated. This timer circuit causes a factory pre-programmed fixed delay before the OUT terminal goes from inactive to active state.

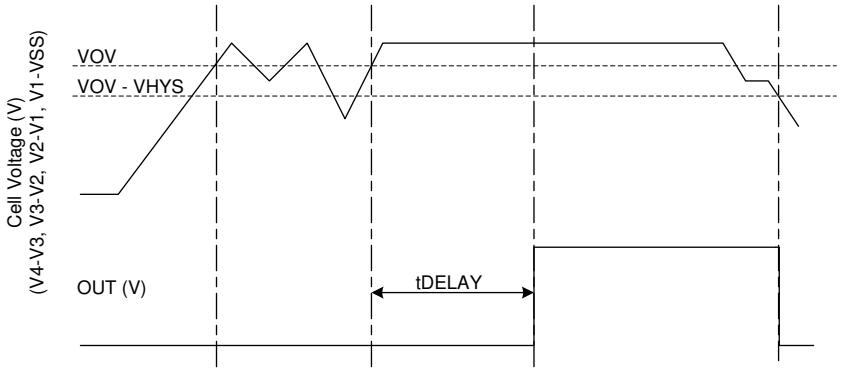


图 8-1. Timing for Overvoltage Sensing for OUT

8.3.3 Regulated Output Voltage and REG_EN Pin

For BQ2961, there are three factory-preprogrammed options for the regulated output voltage, 3.3 V, 2.5 V, and 1.8 V. For BQ2962, the regulated output voltage options are 3.3 V, 3.15 V, and 3.0 V. Potentially, the BQ2962xy device can provide other regulated voltage output between 3.3 V to 3.0 V. Contact Texas Instruments for details.

At power up, the regulated output is on by default. If any cell voltage is below V_{UVREG} at device power up, the regulated output will remain on until the t_{UV_DELAY} time has passed, the regulated output turns off after the delay time.

During discharge, if any cell voltage falls below the V_{UVREG} threshold for t_{UV_DELAY} time, the regulated output is self-disabled. The regulated output turns on again when all the cell voltages are above V_{UVREG} + V_{UVHYS}.

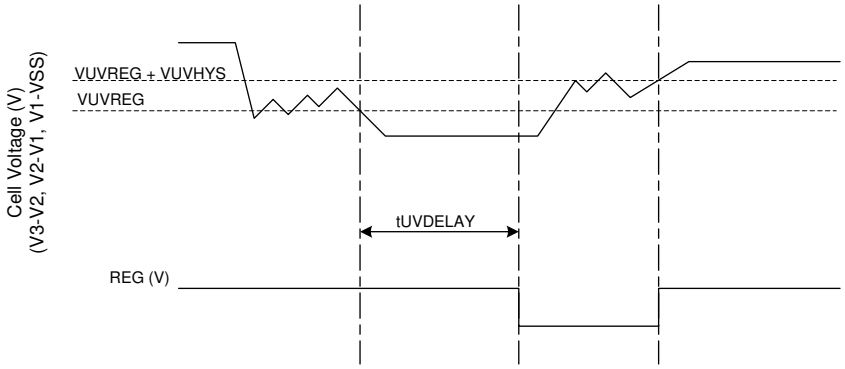


图 8-2. REG Output Timing

8.4 Device Functional Modes

8.4.1 NORMAL Mode

When all of the cell voltages are below the V_{OV} threshold AND above V_{UVREG} threshold, the device operates in NORMAL mode. The device monitors the differential cell voltages connected across (V1 – VSS), (V2 – V1), (V3 – V2), and (V4 – V3). The OUT pin is inactive in this mode. The regulated output is always enabled for BQ2961.

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8.4.2 OVERVOLTAGE Mode

OVERVOLTAGE mode is detected if any of the cell voltages exceed the overvoltage threshold, V_{OV}, for a configured OV delay time. The OUT pin is activated after a delay time preprogrammed at the factory. The OUT pin will pull high internally. Then an external FET is turned on, shorting the fuse to ground, which allows the battery and/or charger power to blow the fuse. When all of the cell voltages fall below (V_{OV} – V_{HYS}), the device returns to NORMAL mode. The regulated output (if enabled) remains on in this mode.

8.4.3 UNDERVOLTAGE Mode

The UNDERVOLTAGE mode is detected if any of the cell voltage across (V1 – VSS), (V2 – V1), (V3 – V2), or (V4 – V3) is below the V_{UVREG} threshold for t_{UV_DELAY} time. In this mode, the regulated output is disabled. To return to the NORMAL mode, all the cell voltages must be above (V_{UVREG} + V_{UVHYS}).

For a low cell configuration, V_n pin can be shorted to the (V_{n-1}) pin. The device ignores any differential cell voltage below V_{UVQUAL} threshold for undervoltage detection.

8.4.4 CUSTOMER TEST MODE

The Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay-timer parameter once the circuit is implemented into the battery pack. To enter CTM, the VDD pin should be set at least 10 V higher than V3 (see 图 8-3). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit CTM, remove the VDD to VC3 voltage differential of 10 V, so that the decrease in the value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the device into CTM. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V3 – V2), (V2 – V1) and (V1 – VSS). Stressing the pins beyond the rated limits can cause permanent damage to the device.

图 8-3 shows the timing for the Customer Test Mode.

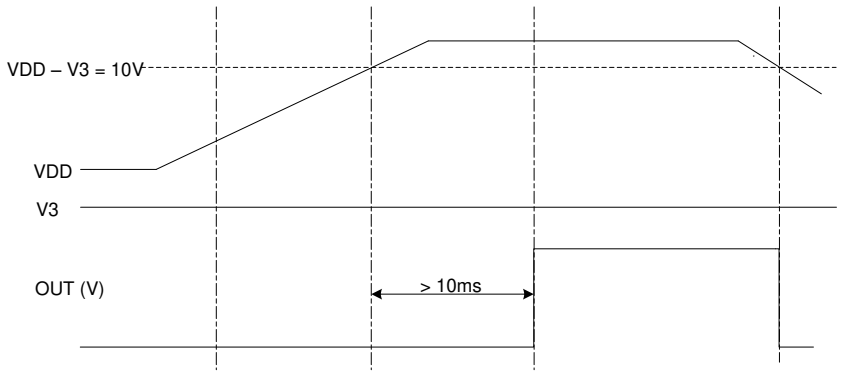


图 8-3. Timing for Customer Test Mode

图 8-4 shows the measurement for current consumption of the product for both VDD and Vx.

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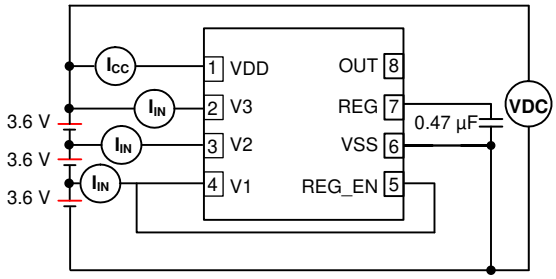


图 8-4. Configuration for Integrated Circuit Current Consumption Test

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The BQ296xxx family of second-level protectors is used for overvoltage protection of the battery pack in the application. A regulated output is available to drive a small circuit with maximum I_{REG} loading. The device OUT pin is active high, which drives a NMOS FET that connects the fuse to ground in the event of a fault condition. This provides a shorted path to use the battery and/or charger power to blow the fuse and cut the power path.

9.2 Typical Application

Application Schematic shows the recommended reference design components.

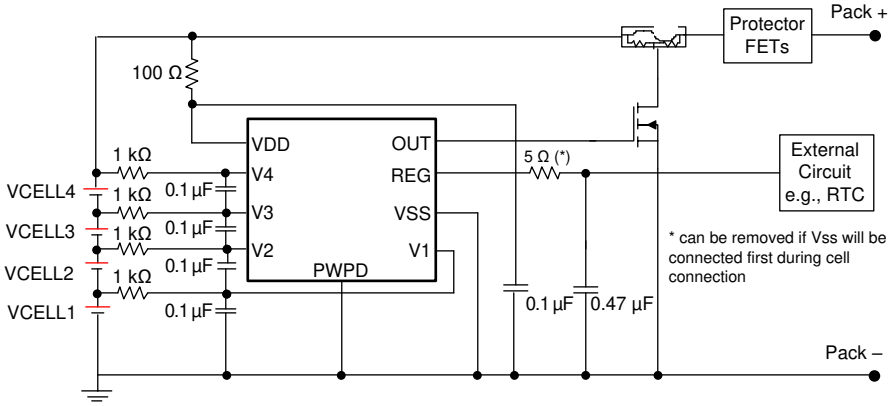


图 9-1. Application Schematic

9.2.1 Design Requirements

Note

Changes to the ranges shown in 表 9-1 will impact the accuracy of the cell measurements.

表 9-1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	R_{IN}	900	1000	4700	Ω
Voltage monitor filter capacitance	C_{IN}	0.01	0.1	1.0	µF
Supply voltage filter resistance	R_{VD}	0.1	—	1	KΩ
Supply voltage filter capacitance	C_{VD}	—	0.1	1.0	µF
REG output capacitance	C_{REG}	0.47	1	—	µF

Note

The device is calibrated using an R_{IN} value = 1 kΩ. Using a value other than the recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

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9.2.2 Detailed Design Procedure

Note

The device VSS must be connected first during PCB test or cell attachment. Failure to do so can damage the REG pin.

1. If the VSS pin cannot be connected first, it is required to add a resistor of a minimum of 5 Ω to a maximum of 10 Ω (a 5-Ω resistor is used in the reference schematic, 图 9-2) in series with the REG capacitor. When VSS is floating, the REG capacitor always charges up to the VDD voltage. When VSS is finally connected, the REG capacitor will be discharged. Adding a small resistor in series reduces the current strength and avoids any potential damage to the REG pin. The 5-Ω resistor can be placed in series with the REG connect circuit (as shown in 图 9-2) or in series of the REG capacitor (as shown in 图 9-3). Placing the resistor in series with the REG circuit results in a small drop of V_{REG} (for example: max loading of I_{REG} mA with a 5-Ω resistor will drop 5 mV on V_{REG}), but such a connection can protect again rush current discharge from a REG capacitor or an external filter capacitor connected to the REG pin. Placing the resistor in series with the REG capacitor is an alternative to avoiding an additional drop in V_{REG} if the filter capacitor used by the external circuit is much smaller than the REG capacitor.
2. After VSS is connected, the device allows a random cell connection to the Vx pin.
3. The cell should be connected to the lower V_n pin; the unused V_n pin should be shorted to the (V_{n-1}) pin. See 图 9-2 for details.

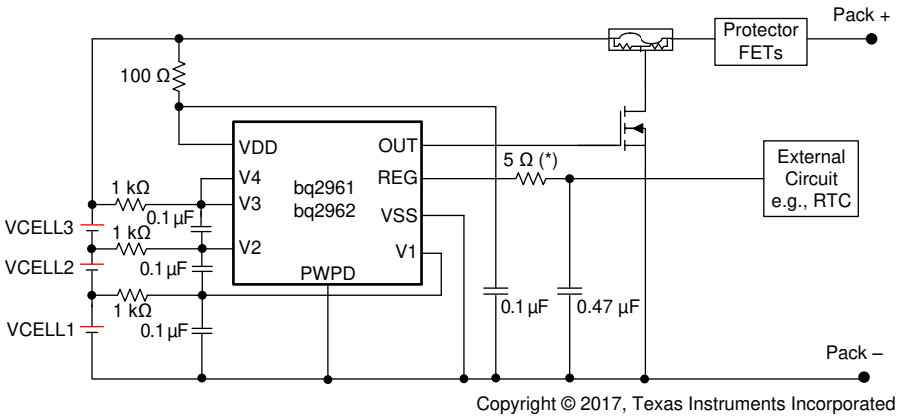


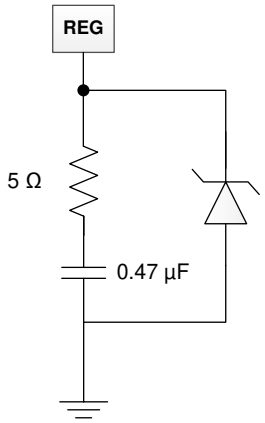
图 9-2. 3-Series BQ2961 and BQ2962 Schematic

4. A zener diode can be added to the REG pin to VSS, as shown in 图 9-3. This is recommended to protect the circuit connected to the REG pin if floating VSS in the field is a risk concern. When VSS is floating (during cell connection when VSS is not connected first or in a system fault with a broken BAT – wire), the REG voltage always pulls up to VDD. In a 4-series configuration, the REG voltage can reach approximately 16 V with VSS floating. Adding a zener diode clamps the REG voltage to a safe level for the external circuits connected to the REG pin. Having the zener diode can also protect the external circuits if the REG pin is shorted to the OUT pin or any other high-voltage output terminal. If a zener diode is used, TI recommends putting the diode on the battery side with the BQ296xxx device to allow protection on the REG pin, as well as the circuit connected to REG under the floating VSS condition. The resistor in series with the REG pin is not required in this case.

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The 5-Ω resistor limits the rush current discharge from the capacitor during cell connection when Vss is not connected first.

This resistor is not required if Vss is connected first in the cell connection sequence.



Loss of Vss connection or REG shorted to high voltage can bring the REG above the regulated range. This optional zener clamp can protect the downstream circuit under such an event.

图 9-3. 5-V Zener Diode

9.2.3 Application Curves

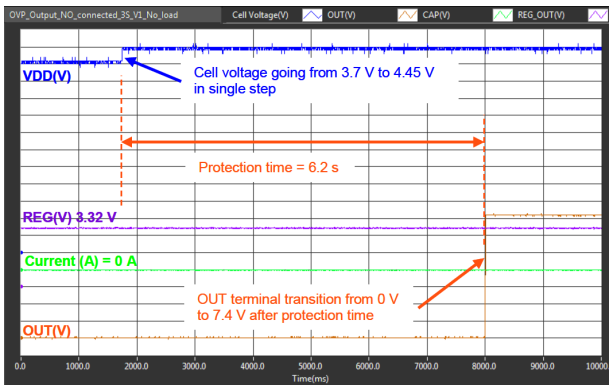


图 9-4. Overvoltage Protection

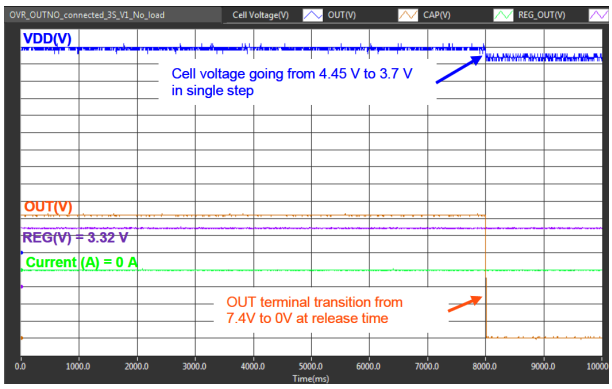


图 9-5. Overvoltage Protection Release

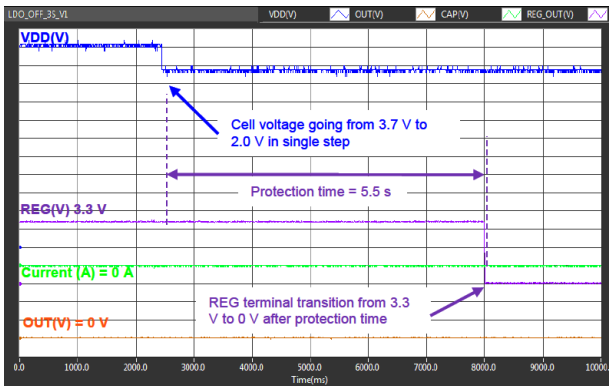


图 9-6. Undervoltage Detection to Turn Off the Regulator

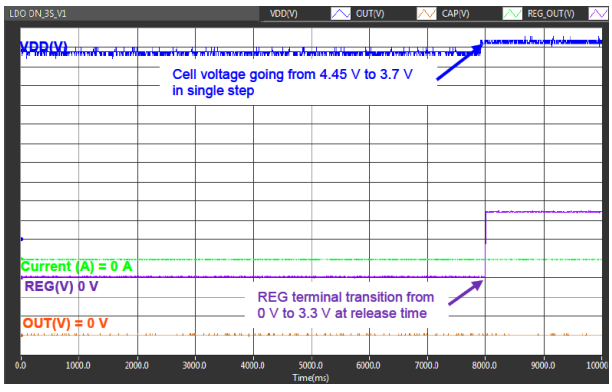


图 9-7. Undervoltage Release to Switch On the Regulator

10 Power Supply Recommendations

The maximum power is 20 V for BQ2961 and BQ2962 on VDD.

Note

Connect VSS first during power up.

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11 Layout

11.1 Layout Guidelines

Use the following layout guidelines:

1. Ensure the RC filters for the Vx pins and VDD pin are placed as close as possible to the target terminal, reducing the tracing loop area.
2. The capacitor for REG should be placed close to the device terminals.
3. Ensure the trace connecting the fuse to the gate, source of the NFET to the Pack – is sufficient to withstand the current during a fuse blown event.

11.2 Layout Example

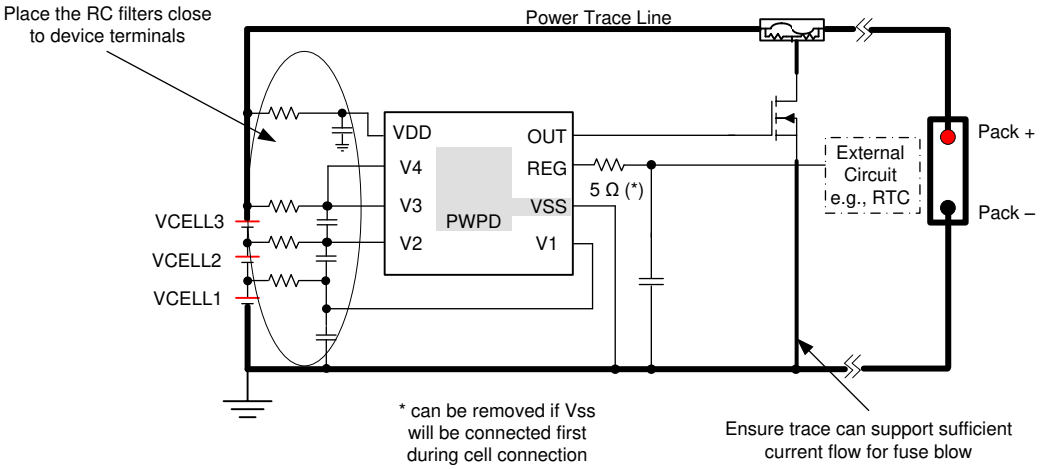


图 11-1. Layout Example

12 Device and Documentation Support

12.1 第三方产品免责声明

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To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ296100DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6100	Samples
BQ296100DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6100	Samples
BQ296103DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6103	Samples
BQ296103DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6103	Samples
BQ296106DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6106	Samples
BQ296106DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6106	Samples
BQ296107DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6107	Samples
BQ296107DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6107	Samples
BQ296111DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6111	Samples
BQ296111DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6111	Samples
BQ296112DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6112	Samples
BQ296112DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6112	Samples
BQ296113DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6113	Samples
BQ296113DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6113	Samples
BQ296114DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6114	Samples
BQ296114DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6114	Samples
BQ296115DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6115	Samples
BQ296202DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6202	Samples
BQ296202DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6202	Samples
BQ296203DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6203	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ296203DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6203	Samples
BQ296212DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6212	Samples
BQ296212DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6212	Samples
BQ296213DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6213	Samples
BQ296213DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6213	Samples
BQ296215DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6215	Samples
BQ296215DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6215	Samples
BQ296216DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6216	Samples
BQ296216DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6216	Samples
BQ296217DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6217	Samples
BQ296217DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6217	Samples
BQ296221DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6221	Samples
BQ296221DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6221	Samples
BQ296222DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6222	Samples
BQ296222DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6222	Samples
BQ296223DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6223	Samples
BQ296223DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6223	Samples
BQ296224DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6224	Samples
BQ296224DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6224	Samples
BQ296226DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6226	Samples
BQ296226DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6226	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ296227DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6227	Samples
BQ296228DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6228	Samples
BQ296228DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6228	Samples
BQ296229DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6229	Samples
BQ296229DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6229	Samples
BQ296230DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6230	Samples
BQ296230DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6230	Samples
BQ296231DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6231	Samples
BQ296231DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6231	Samples
BQ296232DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6232	Samples
BQ296232DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	6232	Samples
BQ296233DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6233	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

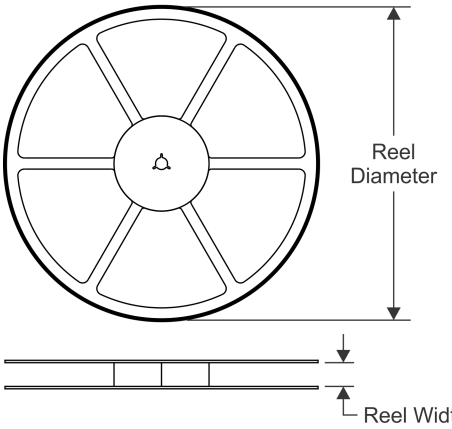
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

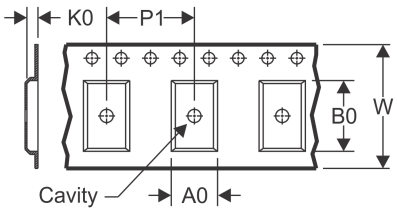
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

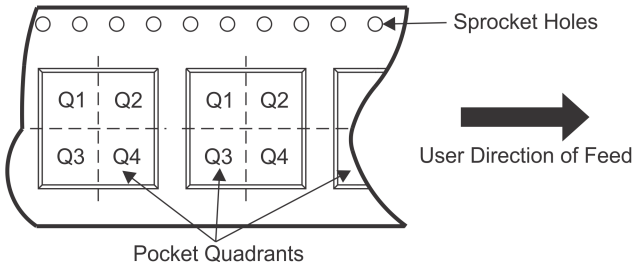


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



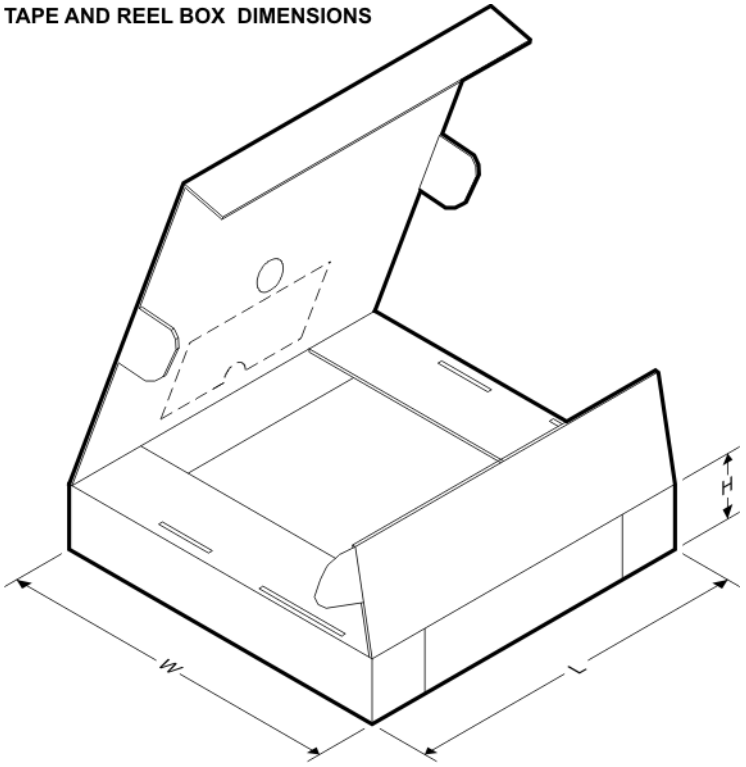
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ296100DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296100DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296103DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296103DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296103DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296103DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296106DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296106DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296106DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296106DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296107DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296107DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296107DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296107DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296111DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296111DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296112DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296112DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ296113DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296113DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296114DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296114DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296115DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296202DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296202DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296202DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296202DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296203DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296203DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296203DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296203DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296212DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296212DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296213DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296213DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296215DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296215DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296216DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296216DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296216DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296216DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296217DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296217DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296217DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296217DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296221DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296221DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296222DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296222DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296223DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296223DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296224DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296224DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296226DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296226DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296227DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296228DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296228DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296229DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296229DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296230DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ296230DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296231DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296231DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296232DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296232DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3
BQ296233DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ296100DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296100DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296103DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296103DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296103DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296103DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296106DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296106DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296106DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296106DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296107DSGR	WSON	DSG	8	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ296107DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296107DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296107DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296111DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296111DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296112DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296112DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296113DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296113DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296114DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296114DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296115DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296202DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296202DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296202DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296202DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296203DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296203DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296203DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296203DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296212DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296212DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296213DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296213DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296215DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296215DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296216DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296216DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296216DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296216DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296217DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296217DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296217DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296217DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296221DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296221DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296222DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296222DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296223DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296223DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296224DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296224DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296226DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296226DSGT	WSON	DSG	8	250	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ296227DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296228DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296228DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296229DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296229DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296230DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296230DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296231DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296231DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296232DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296232DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296233DSGR	WSON	DSG	8	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

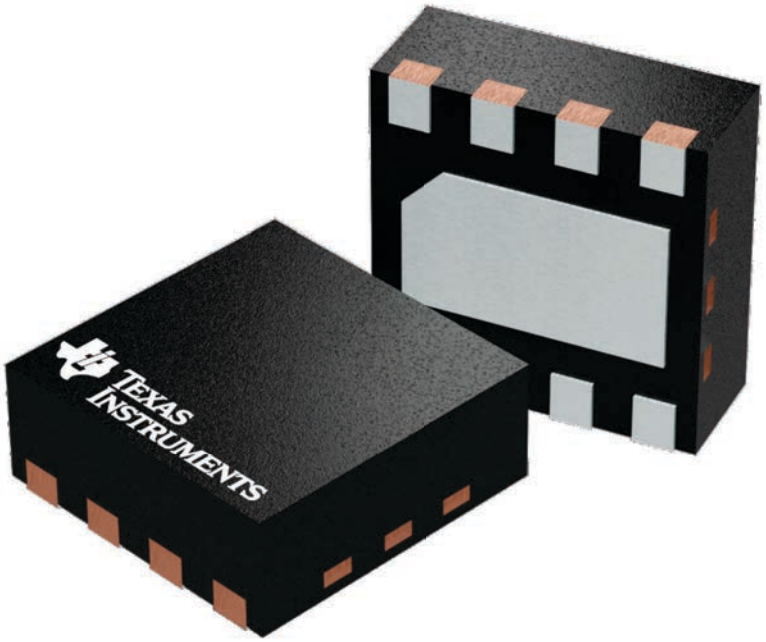
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



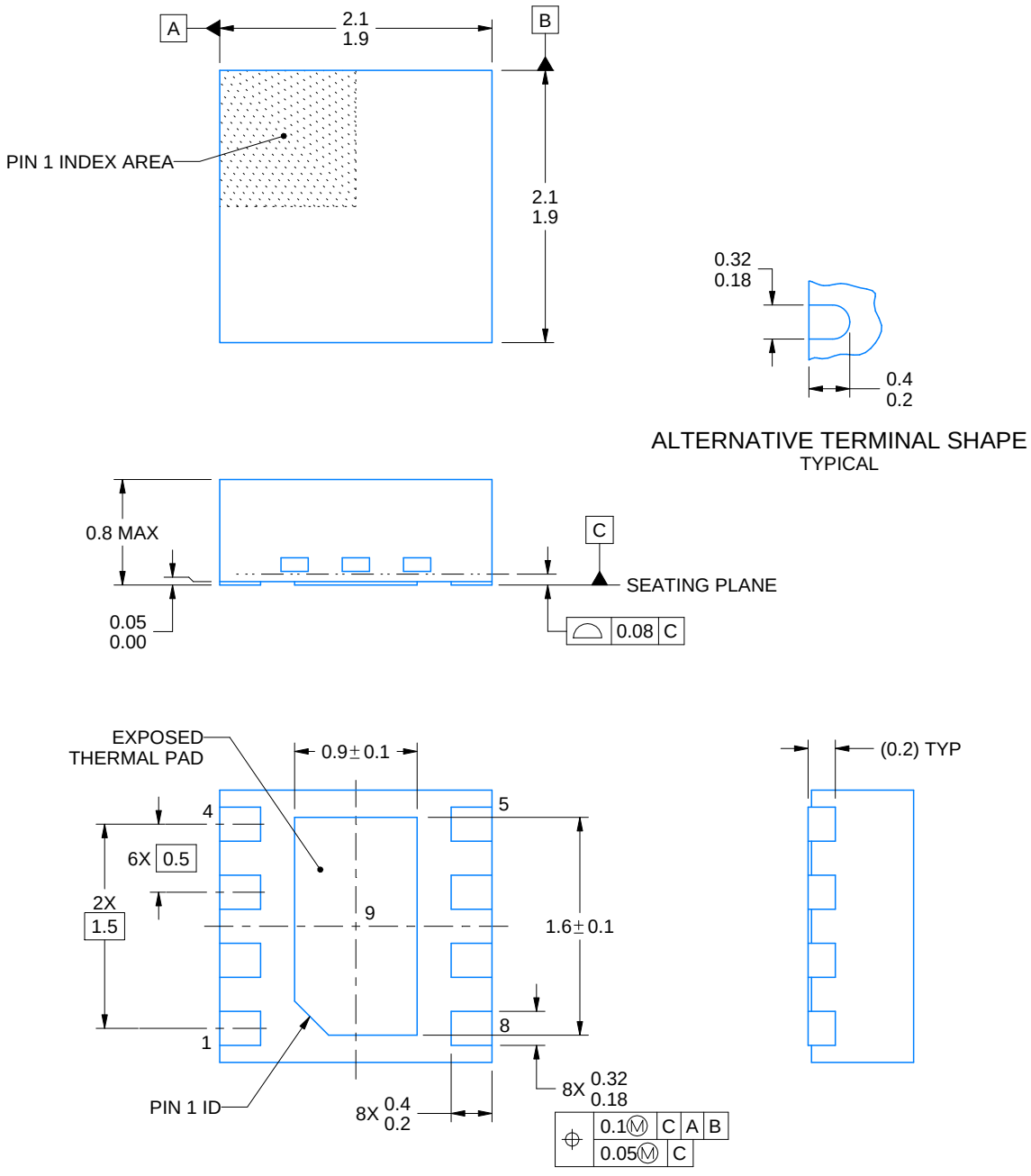
4224783/A

PACKAGE OUTLINE

DSG0008A

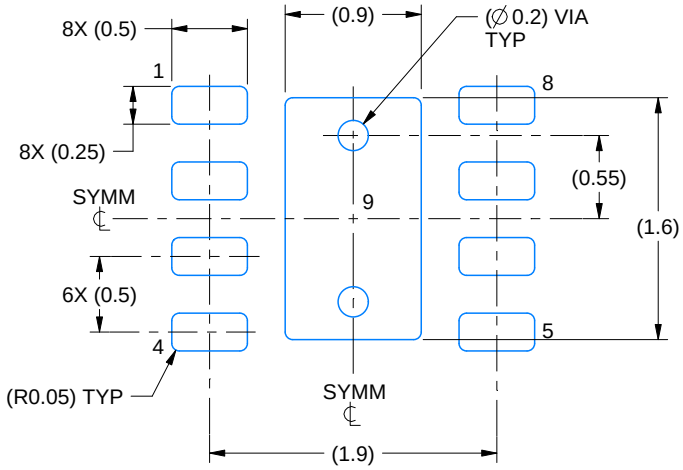
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

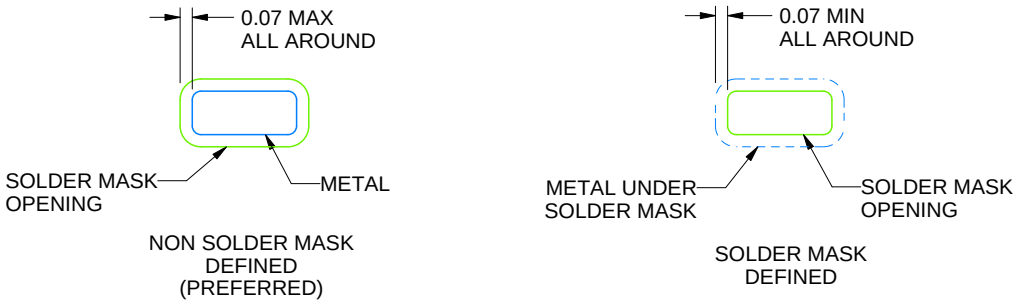


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/D 04/2020

NOTES: (continued)

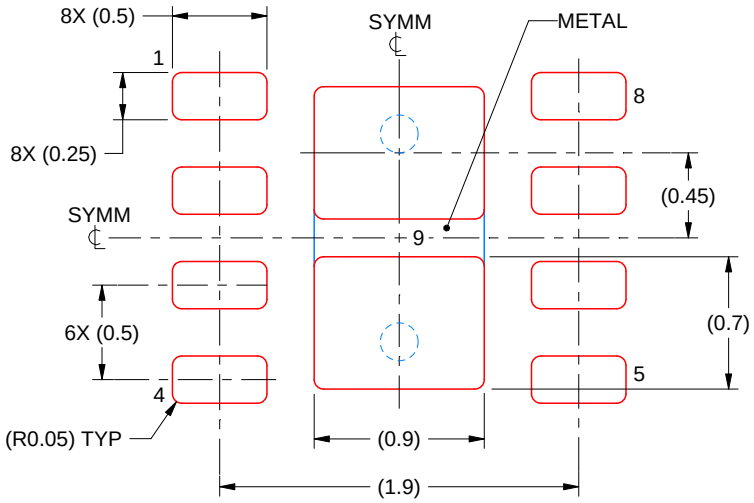
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/D 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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