DLPC3430 和 DLPC3435 显示控制器

1 特性

- 适用于 DLP2010 (0.2 WVGA) DMD 的显示控制器
  - 支持高达 720p 的输入图像大小和可扩展至 WVGA
  - 支持接口训练的低功耗 DMD 接口
- 输入帧速率高达 240Hz
- 像素数据处理：
  - IntelliBright™图像处理算法套件
    - 内容自适应照明控制 (CAIC)
    - 局部亮度增强 (LABB)
  - 图像大小调整（缩放）
  - 1D 梯形校正
  - 色彩坐标调整
  - 主动电源管理处理
  - 可编程 degamma
  - 色彩空间转换
  - 4:2:2 至 4:4:4 色度插值
- 24 位输入像素接口支持：
  - 并行或 BT656 接口协议
  - 高达 155MHz 的像素时钟
  - 多个输入像素数据格式选项
- MIPI®DSI（显示串行接口）3 类（仅 DLPC3430 控制器）：
  - 1-4 条通道，通道速率高达 470Mbps
- 支持外部闪存
- 断电时自动 DMD 停止
- 嵌入式帧存储器 (eDRAM)
- 系统 特性的 xHCI 控制器：
  - I^2C 器件控制
  - 可编程启动界面
  - 可编程 LED 电流控制
  - 显示图像旋转
  - 一帧延迟
- 与 DLPA2000、DLPA2005 或 DLPA3000 PMIC（电源管理集成电路）和 LED 驱动器配对使用

2 应用

- 移动投影仪
- 智能显示
- 智能手机
- 增强现实眼镜
- 智能家居显示
- Pico 投影仪

3 说明

DLPC3430 或 DLPC3435 数字控制器是 DLP2010 (0.2 WVGA) 芯片组的一部分，为 DLP2010 数字微镜器件 (DMD) 的运行提供支持。DLPC3430 和 DLCP3435 控制器提供了连接用户电子产品和 DMD 的便捷多功能接口，支持小尺寸和低功耗显示 应用。

访问 TI DLP ®Pico™ 显示技术入门页，并查看《编程人员指南》了解详情。

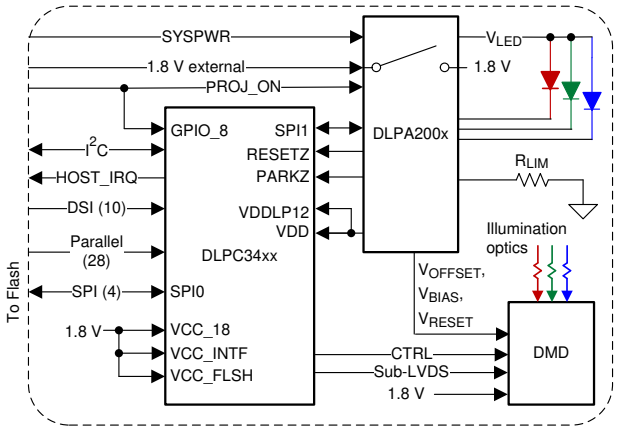
该芯片组提供现成的资源，可帮助用户加快设计周期。这些资源包括可直接用于生产环境的光学模块、光学模块制造商和设计公司。

器件信息(1)(2)

器件型号	封装	封装尺寸（标称值）
DLPC3430	NFBGA (176)	7.00 × 7.00 mm²
DLPC3435	NFBGA (201)	13.00 × 13.00mm²

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) DSI 仅适用于 DLPC3430。DSI 不适用于 DLPC3435。

典型简化系统图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (May 2019) to Revision E — **Page**

- 总数据表格式和订购更新 ... 1
- Deleted mention of mirror parking time from PARKZ pin description and moved to a specification table ... 7
- Changed JTAG pin names from Reserved to proper names ... 7
- Deleted support for adjustable DATAEN_CMD polarity ... 8
- Deleted mention of a specific 3D command ... 8
- Deleted support for adjusting PCLK capture edge in software ... 8
- Changed the description of how to use the CMP_OUT pin and corrected how the comparator must use GPIO_10 (RC_CHARGE) instead of CMP_PWM ... 10
- Deleted support for CMP_PWM ... 10
- Added note about VCC_INTF power up recommendations if slave devices are on the I^2C bus ... 10
- Deleted mention of unsupported keypad inputs ... 11
- Corrected optional MTR_SENSE support to GPIO_18 instead of GPIO_19 ... 11
- Deleted mention of unsupported light sensor on GPIO_13 and GPIO_12 ... 11
- Deleted reference of the RC_CHARGE circuit being used for the light sensor and added reference of it being used for the thermistor ... 11
- Deleted reference of the LS_PWR circuit being used for the light sensor ... 11

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修订历史记录 (接下页)

- Deleted mention of the unsupported LABB output sample and hold sensor control signal 11
- Deleted misleading note about GPIO pins defaulting to inputs 11
- Clarified GPIO_03 - GPIO_01 pins are required to be used as a SPI1 port 12
- Corrected how pins are mentioned that are only available on the DLPC3435 13
- Added missing I/O definition 10 14
- Deleted unneeded VCC_INTF and VCC_FLSH absolute maximum values 15
- Added high voltage tolerant note to Absolute Maximum Ratings table 15
- Changed incorrect pin tolerance 16
- Changed Power Electrical Characteristics table to reflect updated power measurement values and techniques 17
- Deleted reference to unsupported IDLE mode 17
- Added note that the power numbers vary depending on the utilized software 17
- Changed and fixed incorrect test conditions for current drive strengths 18
- Deleted redundant $|V_{OD}|$ specification which is referenced in later sections 18
- Added minimum and maximum values for V_{OH} for I/O type 4 18
- Added minimum and maximum values for V_{OL} for I/O type 4 18
- Deleted incorrect reference to 2.5V, 24mA drive 18
- Corrected I^2C buffer test conditions 18
- Deleted incorrect steady-state common mode voltage reference 18
- Changed high voltage tolerant I/O note to only refer to the I^2C buffer and changed VCC to VCC_INTF 18
- Added $|V_{OD}|$ minimum and maximum values, and changed the typical value 21
- Added high-level output voltage minimum and maximum values for the sub-LVDS DMD interface, deleted redundant mention of specification, and changed the typical value. 21
- Added low-level output voltage minimum and maximum values for the sub-LVDS DMD interface, deleted redundant mention of specification, and changed the typical value. 21
- Corrected the name of the DMD Low-Speed signals from inputs to outputs. 22
- Deleted $V_{OH(DC)}$ maximum and $V_{OL(DC)}$ minimum values. 22
- Added note about DMD input specs being met if a proper series termination resistor is used 22
- Deleted reference of selecting unsupported oscillator frequency 23
- Corrected system oscillator clock period to match clock frequency 23
- Changed pulse duration percent spec from a maximum to a minimum 23
- Added condition for VDD rise time 23
- Deleted the incorrect part of the t_{p_tvb} definition 24
- Deleted unneeded total horizontal blanking equation 24
- Changed minimum total vertical blanking equation 24
- Increased maximum PCLK from 150MHz to 155MHz 25
- Deleted reference to various signal's active edges being configurable 25
- Changed the minimum flash SPI_CLK frequency 27
- Corrected flash interface clock period to match clock frequency 27
- Added Other Timing Requirements section to more clearly list signal transition time requirements 27
- Changed DMD HS Clock switching rate from maximum to nominal and added accompanying clock specification 28
- Added DMD Parking Switching Characteristics section 28
- Added the Chipset Component Usage Specification section to clarify chipset support requirements 28
- Changed how chipset support is mentioned in the Detailed Description section 29
- Increased maximum frame rate from 122 Hz to 242 Hz 30
- Deleted support for 3D video over DSI 30
- Deleted reference to internal software tools and clarified how firmware affects the supported resolution and frame

修订历史记录 (接下页)

rates 30
- Added note stating bits per pixel limitation at 120 Hz with DSI input 30
- Added note that up to four DSI lanes may be required to fully utilize the bandwidth 30
- Deleted mention of sequencer sync mode as its generally assumed to be auto 30
- Clarified note about VSYNC_WE needing to remain active 31
- 已删除 support for changing the clock active edge and clarified support of changing the sync active edge 31
- 已更改 the DATAEN_CMD signal to not be optional 31
- 已添加 note that LP mode is required during vertical time for DSI 33
- 已更改 requirement related to DSI initialization 33
- 已删除 incorrect DSI data type; see software programmers guide instead 34
- 已添加 information that the parallel interface isn't ready to accept data until the auto-initialization process is completed.. 35
- 已更改 how the 500 ms startup time is described 35
- 已更改 SPI flash key timing parameter access frequency minimum and maximum values 35
- Added a new maximum frequency requirement for the SPI flash. 37
- 已更改 maximum flash size supported from 16Mb to 64Mb 37
- 已删除 SPI signal routing section 37
- 已删除 support for a light sensor integrated with the DLPC34xx controller 39
- 已添加 missing timing definitions 40
- Clarified that the mentioned SDR clock speed is the typical value 43
- 已更改 how the DMD Sub-LVDS Interface requirements are mentioned 43
- 已删除 DMD Interface stack-up image 43
- 已删除 equation concerning DMD interface system timing margin 43
- 已更改 the description of how PROJ_ON affects the power supplies 46
- 已更改 which signals are listed as tri-stated at power up and which signals are pulled low 51
- 已更改 1-oz copper plane recommendation 53
- 已删除 reference to unsupported option of variable frequency reference clock 54
- 已添加 additional DMD data and DMD clock signal matching requirements 57
- 已更改 maximum mismatch from ±0.1" to ±1.0" 57
- 已更改 incorrect signal matching requirement table note 57
- Added missing DMD HS layout signal requirements 58
- 已更改 differential signal layer change to a recommendation 59
- 已更改 wording requiring no more than two vias on certain DMD signals 59
- 已更改 更改了器件标记图像和定义 61

Changes from Revision C (July 2016) to Revision D — **Page**

- Changed mirror parking time from "500 μs" to "20 ms" for PARKZ description in *Pin Functions* table 7
- Updated mirror parking time from "500 μs" to "20 ms" in *Figure 27. DLPC343x Power-Up / PARKZ = 0 Initiated Fast PARK and Power-Down* 47

Changes from Revision B (February 2016) to Revision C — **Page**

- Added DSI pin functions in DSI Input Data and Clock table 9
- Removed GPIO_07 LED Enable features 11
- Added *DSI Host Timing Requirements* 26
- Updated *Supported Resolution and Frame Rates* 30

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- Added *DSI Interface - Supported Data Transfer Formats* 33
- Added *Display Serial Interface DSI* 34
- Added *3D Glasses Operation* 40
- Added *DSI Interface Layout* 56

Changes from Revision A (January 2016) to Revision B **Page**

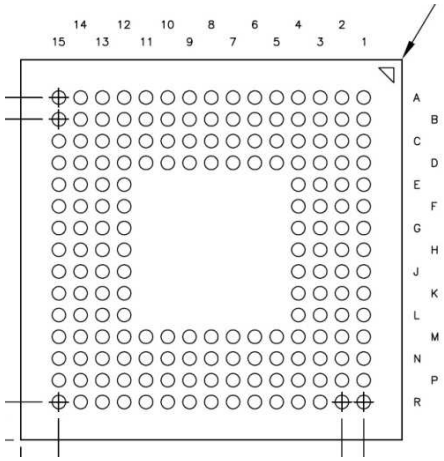
- 更新了整篇数据表以显示 DLPC3430 和 DLPC3435 控制器的正确信息，并更正了文本和图片中 DLPC3430 和 DLPC3435 的器件编号 1

Changes from Original (July 2014) to Revision A **Page**

- 更新的器件标记图像和表格 61

5 Pin Configuration and Functions

ZVB Package
176-Pin NFBGA
Bottom View



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	DMD_LS_CLK	DMD_LS_WDATA	DMD_HS_WDATAH_P	DMD_HS_WDATAG_P	DMD_HS_WDATAF_P	DMD_HS_WDATAE_P	DMD_HS_CLK_P	DMD_HS_WDATAD_P	DMD_HS_WDATAC_P	DMD_HS_WDATAB_P	DMD_HS_WDATAA_P	CMP_OUT	SPI0_CLK	SPI0_CSZ0	CMP_PWM
B	DMD_DEN_ARSTZ	DMD_LS_RDATA	DMD_HS_WDATAH_N	DMD_HS_WDATAG_N	DMD_HS_WDATAF_N	DMD_HS_WDATAE_N	DMD_HS_CLK_N	DMD_HS_WDATAD_N	DMD_HS_WDATAC_N	DMD_HS_WDATAB_N	DMD_HS_WDATAA_N	SPI0_DIN	SPI0_DOUT	LED_SEL_1	LED_SEL_0
C	DD3P	DD3N	VDDLP12	VSS	VDD	VSS	VCC	VSS	VCC	HWTEST_EN	RESETZ	SPI0_CSZ1	PARKZ	GPIO_00	GPIO_01
D	DD2P	DD2N	VDD	VCC	VDD	VSS	VDD	VSS	VDD	VSS	VCC_FLSH	VDD	VDD	GPIO_02	GPIO_03
E	DCLKP	DCLKN	VDD	VSS								VCC	VSS	GPIO_04	GPIO_05
F	DD1P	DD1N	RREF	VSS								VCC	VDD	GPIO_06	GPIO_07
G	DD0P	DD0N	VSS_PLLM	VSS								VSS	VSS	GPIO_08	GPIO_09
H	PLL_REFCLK_I	VDD_PLLM	VSS_PLLD	VSS								VSS	VDD	GPIO_10	GPIO_11
J	PLL_REFCLK_O	VDD_PLLD	VSS	VDD								VDD	VSS	GPIO_12	GPIO_13
K	PDATA_1	PDATA_0	VDD	VSS								VSS	VCC	GPIO_14	GPIO_15
L	PDATA_3	PDATA_2	VSS	VDD								VDD	VDD	GPIO_16	GPIO_17
M	PDATA_5	PDATA_4	VCC_INTF	VSS	VSS	VDD	VCC_INTF	VSS	VDD	VDD	VCC	VSS	JTAGTMS1	GPIO_18	GPIO_19
N	PDATA_7	PDATA_6	VCC_INTF	PDM_CVS_TE	HSYNC_CS	3DR	VCC_INTF	HOST_IRQ	IIC0_SDA	IIC0_SCL	JTAGTMS2	JTAGTDO2	JTAGTDO1	TSTPT_6	TSTPT_7
P	VSYNC_WE	DATEN_CMD	PCLK	PDATA_11	PDATA_13	PDATA_15	PDATA_17	PDATA_19	PDATA_21	PDATA_23	JTAGTRSTZ	JTAGTCK	JTAGTDI	TSTPT_4	TSTPT_5
R	PDATA_8	PDATA_9	PDATA_10	PDATA_12	PDATA_14	PDATA_16	PDATA_18	PDATA_20	PDATA_22	IIC1_SDA	IIC1_SCL	TSTPT_0	TSTPT_1	TSTPT_2	TSTPT_3

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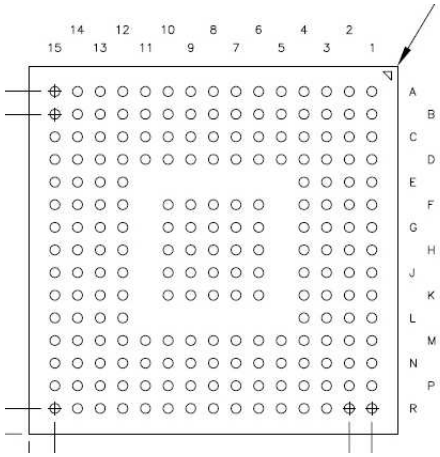
ZEZ Package
201-Pin NFBGA
Bottom View



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	DMD_LS_CLK	DMD_LS_WDATA	DMD_HS_WDATAH_P	DMD_HS_WDATAG_P	DMD_HS_WDATAF_P	DMD_HS_WDATAE_P	DMD_HS_CLK_P	DMD_HS_WDATAD_P	DMD_HS_WDATAC_P	DMD_HS_WDATAB_P	DMD_HS_WDATAA_P	CMP_OUT	SPI0_CLK	SPI0_CSZ0	CMP_PWM
B	DMD_DEN_ARSTZ	DMD_LS_RDATA	DMD_HS_WDATAH_N	DMD_HS_WDATAG_N	DMD_HS_WDATAF_N	DMD_HS_WDATAE_N	DMD_HS_CLK_N	DMD_HS_WDATAD_N	DMD_HS_WDATAC_N	DMD_HS_WDATAB_N	DMD_HS_WDATAA_N	SPI0_DIN	SPI0_DOUT	LED_SEL_1	LED_SEL_0
C	DD3P	DD3N	VDDLP12	VSS	VDD	VSS	VCC	VSS	VCC	HWTEST_EN	RESETZ	SPI0_CSZ1	PARKZ	GPIO_00	GPIO_01
D	DD2P	DD2N	VDD	VCC	VDD	VSS	VDD	VSS	VDD	VSS	VCC_FLSH	VDD	VDD	GPIO_02	GPIO_03
E	DCLKP	DCLKN	VDD	VSS								VCC	VSS	GPIO_04	GPIO_05
F	DD1P	DD1N	RREF	VSS		VSS	VSS	VSS	VSS	VSS		VCC	VDD	GPIO_06	GPIO_07
G	DD0P	DD0N	VSS_PLLM	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VSS	GPIO_08	GPIO_09
H	PLL_REFCLK_I	VDD_PLLM	VSS_PLLD	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VDD	GPIO_10	GPIO_11
J	PLL_REFCLK_O	VDD_PLLD	VSS	VDD		VSS	VSS	VSS	VSS	VSS		VDD	VSS	GPIO_12	GPIO_13
K	PDATA_1	PDATA_0	VDD	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VCC	GPIO_14	GPIO_15
L	PDATA_3	PDATA_2	VSS	VDD								VDD	VDD	GPIO_16	GPIO_17
M	PDATA_5	PDATA_4	VCC_INTF	VSS	VSS	VDD	VCC_INTF	VSS	VDD	VDD	VCC	VSS	JTAGTMS1	GPIO_18	GPIO_19
N	PDATA_7	PDATA_6	VCC_INTF	PDM_CVS_TE	HSYNC_CS	3DR	VCC_INTF	HOST_IRQ	IIC0_SDA	IIC0_SCL	JTAGTMS2	JTAGTDO2	JTAGTDO1	TSTPT_6	TSTPT_7
P	VSYNC_WE	DATEN_CMD	PCLK	PDATA_11	PDATA_13	PDATA_15	PDATA_17	PDATA_19	PDATA_21	PDATA_23	JTAGTRSTZ	JTAGTCK	JTAGTDI	TSTPT_4	TSTPT_5
R	PDATA_8	PDATA_9	PDATA_10	PDATA_12	PDATA_14	PDATA_16	PDATA_18	PDATA_20	PDATA_22	IIC1_SDA	IIC1_SCL	TSTPT_0	TSTPT_1	TSTPT_2	TSTPT_3

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Pin Functions – Test Pins and General Control

PIN		I/O	TYPE[1]	DESCRIPTION
NAME	NO.			
HWTEST_EN	C10	I	6	Manufacturing test enable signal. Connect this signal directly to ground on the PCB for normal operation.
PARKZ	C13	I	6	DMD fast park control (active low Input with a hysteresis buffer). This signal is used to quickly park the DMD when loss of power is imminent. The longest lifetime of the DMD may not be achieved with the fast park operation; therefore, this signal is intended to only be asserted when a normal park operation is unable to be completed. The PARKZ signal is typically provided from the DLPAxxxx interrupt output signal.
JTAGTCK	P12	I	6	TI internal use. Leave this pin unconnected.
JTAGTDI	P13	I	6	TI internal use. Leave this pin unconnected.
JTAGTDO1	N13[2]	O	1	TI internal use. Leave this pin unconnected.
JTAGTDO2	N12[2]	O	1	TI internal use. Leave this pin unconnected.
JTAGTMS1	M13	I	6	TI internal use. Leave this pin unconnected.
JTAGTMS2	N11	I	6	TI internal use. Leave this pin unconnected.
JTAGTRSTZ	P11	I	6	TI internal use. This pin must be tied to ground, through an external resistor for normal operation. Failure to tie this pin low during normal operation can cause start up and initialization problems.[3]
RESETZ	C11	I	6	Power-on reset (active low input with a hysteresis buffer). Self-configuration starts when a low-to-high transition is detected on RESETZ. All controller power and clocks must be stable before this reset is de-asserted. No signals are in their active state while RESETZ is asserted. This pin is typically connected to the RESETZ pin of the DLPA200x or RESET_Z of the DLPA3000.
TSTPT_0	R12	I/O	1	Test pins (includes weak internal pulldown). Pins are tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ, and then driven as outputs.[3][4] Normal use: reserved for test output. Leave open for normal use. Note: An external pullup may put the DLPC34xx in a test mode. See Test Point Support for more information.
TSTPT_1	R13	I/O	1	
TSTPT_2	R14	I/O	1	
TSTPT_3	R15	I/O	1	
TSTPT_4	P14	I/O	1	
TSTPT_5	P15	I/O	1	
TSTPT_6	N14	I/O	1	
TSTPT_7	N15	I/O	1	

(1) See Table 2 for type definitions.
(2) If the application design does not require an external pullup, and there is no external logic that can overcome the weak internal pulldown resistor, then this I/O pin can be left open or unconnected for normal operation. If the application design does not require an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown is recommended to ensure a logic low.
(3) External resistor must have a value of 8 kΩ or less to compensate for pins that provide internal pullup or pulldown resistors.
(4) If the application design does not require an external pullup and there is no external logic that can overcome the weak internal pulldown, then the TSTPT I/O can be left open (unconnected) for normal operation. If operation does not call for an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown resistor is recommended to ensure a logic low.

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Pin Functions – Parallel Port Input(1)(2)

PIN		I/O	Type(3)	DESCRIPTION	
NAME	NO.			PARALLEL RGB MODE	BT656 INTERFACE MODE
PCLK	P3	I	11	Pixel clock	Pixel clock
PDM_CVS_TE	N4	I/O	5	Parallel data mask. Programable polarity with default of active high. Optional signal.	Unused
VSYNC_WE	P1	I	11	Vsync(4)	Unused
HSYNC_CS	N5	I	11	Hsync(4)	Unused
DATAEN_CMD	P2	I	11	Data valid	Unused
				(TYPICAL RGB 888)	
PDATA_0	K2	I	11	Blue (bit weight 1)	BT656_Data (0)
PDATA_1	K1			Blue (bit weight 2)	BT656_Data (1)
PDATA_2	L2			Blue (bit weight 4)	BT656_Data (2)
PDATA_3	L1			Blue (bit weight 8)	BT656_Data (3)
PDATA_4	M2			Blue (bit weight 16)	BT656_Data (4)
PDATA_5	M1			Blue (bit weight 32)	BT656_Data (5)
PDATA_6	N2			Blue (bit weight 64)	BT656_Data (6)
PDATA_7	N1			Blue (bit weight 128)	BT656_Data (7)
				(TYPICAL RGB 888)	
PDATA_8	R1	I	11	Green (bit weight 1)	Unused
PDATA_9	R2			Green (bit weight 2)	
PDATA_10	R3			Green (bit weight 4)	
PDATA_11	P4			Green (bit weight 8)	
PDATA_12	R4			Green (bit weight 16)	
PDATA_13	P5			Green (bit weight 32)	
PDATA_14	R5			Green (bit weight 64)	
PDATA_15	P6			Green (bit weight 128)	
				(TYPICAL RGB 888)	
PDATA_16	R6	I	11	Red (bit weight 1)	Unused
PDATA_17	P7			Red (bit weight 2)	
PDATA_18	R7			Red (bit weight 4)	
PDATA_19	P8			Red (bit weight 8)	
PDATA_20	R8			Red (bit weight 16)	
PDATA_21	P9			Red (bit weight 32)	
PDATA_22	R9			Red (bit weight 64)	
PDATA_23	P10			Red (bit weight 128)	
3DR	N6	I	11	3D reference • For 3D applications: left or right 3D reference (left = 1, right = 0). To be provided by the host. Must transition in the middle of each frame (no closer than 1 ms to the active edge of VSYNC) • If a 3D application is not used, pull this input low through an external resistor.	

(1) PDATA(23:0) bus mapping depends on pixel format and source mode. See later sections for details.
(2) Connect unused inputs to ground or pulldown to ground through an external resistor (8 kΩ or less).
(3) See Table 2 for type definitions.
(4) VSYNC and HSYNC polarity can be adjusted by software.

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Pin Functions – DSI Input Data and Clock

PIN		I/O	Type(1)	DESCRIPTION
NAME	NO.			
DCLKN DCLKP	E2 E1	I/O	10	DSI LVDS Differential Clock for DSI Interface.
DD0N DD0P DD1N DD1P DD2N DD2P DD3N DD3P	G2 G1 F2 F1 D2 D1 C2 C1	I/O	10	Differential data bus for DSI data lane LVDS differential pair inputs 0 through 3 (Support a maximum of 4 input DSI lanes)(2)
RREF	F3	—		DSI reference resistor. RREF is an analog signal that requires a fixed precision 30-kΩ ±1% resistor connected from this pin to ground when DSI is used. If DSI is NOT used, leave this pin unconnected and floating.

(1) See Table 2 for type definitions.
(2) Differential data bus 0 (DD0x) is required for DSI operation. The remaining three data lanes are optional and only needed depending on the implementation and required video bandwidth. Leave any unused DSI LVDS pairs unconnected and floating.

Pin Functions – DMD Reset and Bias Control

PIN		I/O	TYPE(1)	DESCRIPTION
NAME	NO.			
DMD_DEN_ARSTZ	B1	O	2	DMD driver enable (active high). DMD reset (active low). When corresponding I/O power is supplied, the controller drives this signal low after the DMD is parked and before power is removed from the DMD. If the 1.8-V power to the DLPC34xx is independent of the 1.8-V power to the DMD, then TI recommends including a weak, external pulldown resistor to hold the signal low in case DLPC34xx power is inactive while DMD power is applied.
DMD_LS_CLK	A1	O	3	DMD, low speed (LS) interface clock
DMD_LS_WDATA	A2	O	3	DMD, low speed (LS) serial write data
DMD_LS_RDATA	B2	I	6	DMD, low speed (LS) serial read data

(1) See Table 2 for type definitions.

Pin Functions – DMD Sub-LVDS Interface

PIN		I/O	TYPE(1)	DESCRIPTION
NAME	NO.			
DMD_HS_CLK_P DMD_HS_CLK_N	A7 B7	O	4	DMD high speed (HS) interface clock
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	A3 B3 A4 B4 A5 B5 A6 B6 A8 B8 A9 B9 A10 B10 A11 B11	O	4	DMD sub-LVDS high speed (HS) interface write data lanes. The true numbering and application of the DMD_HS_WDATA pins depend on the software configuration. See 表 12.

(1) See Table 2 for type definitions.

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Pin Functions – Peripheral Interface[1]

PIN		I/O	TYPE[2]	DESCRIPTION
NAME	NO.			
CMP_OUT	A12	I	6	Successive approximation ADC (analog-to-digital converter) comparator output (DLPC34xx Input). To implement, use a successive approximation ADC with a thermistor feeding one input of the external comparator and the DLPC34xx controller GPIO_10 (RC_CHARGE) pin driving the other side of the comparator. It is recommended to use the DLPAxxxx to achieve this function. CMP_OUT must be pulled-down to ground if this function is not used. (hysteresis buffer)
CMP_PWM	A15	O	1	TI internal use. Leave this pin unconnected.
HOST_IRQ[3]	N8	O	9	Host interrupt (output) HOST_IRQ indicates when the DLPC34xx auto-initialization is in progress and most importantly when it completes. This pin is tri-stated during reset. An external pullup must be included on this signal.
IIC0_SCL[4]	N10	I/O	7	I^2C slave (port 0) SCL (bidirectional, open-drain signal with input hysteresis): This pin requires an external pullup resistor. The slave I^2C I/Os are 3.6-V tolerant (high-voltage-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I^2C pullups must be connected to a host supply with an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage does not typically satisfy the V_{IH} specification of the slave I^2C input buffers).
IIC1_SCL	R11	I/O	8	TI internal use. TI recommends an external pullup resistor.
IIC0_SDA[4]	N9	I/O	7	I^2C slave (port 0) SDA. (bidirectional, open-drain signal with input hysteresis): This pin requires an external pullup resistor. The slave I^2C port is the control port of controller. The slave I^2C I/O pins are 3.6-V tolerant (high-volt-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I^2C pullups must be connected to a host supply with an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage does not typically satisfy the V_{IH} specification of the slave I^2C input buffers).
IIC1_SDA	R10	I/O	8	TI internal use. TI recommends an external pullup resistor.
LED_SEL_0	B15	O	1	LED enable select. Automatically controlled by the DLPC34xx programmable DMD sequence LED_SEL(1:0) — Enabled LED 00 — None 01 — Red 10 — Green 11 — Blue The controller drives these signals low when RESETZ is asserted and the corresponding I/O power is supplied. The controller continues to drive these signals low throughout the auto-initialization process. A weak, external pulldown resistor is recommended to ensure that the LEDs are disabled when I/O power is not applied.
LED_SEL_1	B14	O	1	
SPI0_CLK	A13	O	13	SPI (Serial Peripheral Interface) port 0, clock. This pin is typically connected to the flash memory clock.
SPI0_CSZ0	A14	O	13	SPI port 0, chip select 0 (active low output). This pin is typically connected to the flash memory chip select. TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during controller reset assertion.
SPI0_CSZ1	C12	O	13	SPI port 0, chip select 1 (active low output). This pin typically remains unused. TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during controller reset assertion.
SPI0_DIN	B12	I	12	Synchronous serial port 0, receive data in. This pin is typically connected to the flash memory data out.
SPI0_DOUT	B13	O	13	Synchronous serial port 0, transmit data out. This pin is typically connected to the flash memory data in.

(1) External pullup resistor must be 8 kΩ or less.
(2) See Table 2 for type definitions.
(3) For more information about usage, see *Device Startup*.
(4) When VCC_INTF is powered and VDD is not powered, the controller may drive the IIC0_xxx pins low which prevents communication on this I^2C bus. Do not power up the VCC_INTF pin before powering up the VDD pin for any system that has additional slave devices on this bus.

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Pin Functions – GPIO Peripheral Interface(1)

PIN		I/O	TYPE(2)	DESCRIPTION(3)
NAME	NO.			
GPIO_19	M15	I/O	1	General purpose I/O 19 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_18	M14	I/O	1	General purpose I/O 18 (hysteresis buffer). Options: 1. Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input. 2. MTR_SENSE, Motor Sense (Input): For focus motor control applications, this GPIO must be configured as an input to the DLPC34xx and supplied from the focus motor position sensor.
GPIO_17	L15	I/O	1	General purpose I/O 17 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_16	L14	I/O	1	General purpose I/O 16 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_15	K15	I/O	1	General purpose I/O 15 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_14	K14	I/O	1	General purpose I/O 14 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_13	J15	I/O	1	General purpose I/O 13 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_12	J14	I/O	1	General purpose I/O 12 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_11	H15	I/O	1	General purpose I/O 11 (hysteresis buffer). Options: 1. Thermistor power enable (output). Turns on the power to the thermistor when it is used and enabled. 2. Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_10	H14	I/O	1	General Purpose I/O 10 (hysteresis buffer). Options: 1. RC_CHARGE (output): Intended to feed the RC charge circuit of the thermistor interface. 2. Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_09	G15	I/O	1	General purpose I/O 09 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_08	G14	I/O	1	General purpose I/O 08 (hysteresis buffer). Normal mirror parking request (active low): To be driven by the PROJ_ON output of the host. A logic low on this signal causes the DLPC34xx to PARK the DMD, but it does not power down the DMD (the DLPAxxxx does that instead). The minimum high time is 200 ms. The minimum low time is 200 ms.
GPIO_07	F15	I/O	1	General purpose I/O 07 (hysteresis buffer). If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_06	F14	I/O	1	General purpose I/O 06 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_05	E15	I/O	1	General purpose I/O 05 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.

(1) GPIO pins must be configured through software for input, output, bidirectional, or open-drain operation. Some GPIO pins have one or more alternative use modes, which are also software configurable. An external pullup resistor is required for each signal configured as open-drain.
(2) See Table 2 for type definitions.
(3) General purpose I/O for the DLPC3430 and DLPC3435 controllers. These GPIO pins are software configurable.

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Pin Functions – GPIO Peripheral Interface(1) (continued)

PIN		I/O	TYPE(2)	DESCRIPTION(3)
NAME	NO.			
GPIO_04	E14	I/O	1	General purpose I/O 04 (hysteresis buffer). Options: 1. 3D glasses control (output): Controls the shutters on 3D glasses (Left = 1, Right = 0). 2. SPI1_CSZ1 (active-low output): Optional SPI1 chip select 1 signal. Requires an external pullup resistor to deactivate this signal during reset and auto-initialization processes. 3. Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_03	D15	I/O	1	General purpose I/O 03 (hysteresis buffer). SPI1_CSZ0 (active low output): SPI1 chip select 0 signal. This pin is typically connected to the DLPAxxxx SPI_CSZ pin. Requires an external pullup resistor to deactivate this signal during reset and auto-initialization processes.
GPIO_02	D14	I/O	1	General purpose I/O 02 (hysteresis buffer). Options: 1. SPI1_DOUT (output): SPI1 data output signal. This pin is typically connected to the DLPAxxxx SPI_DIN pin. 2. Optional DSI Bus Width Config 1 (input): The controller samples this pin during boot and is used to define the number of lanes used for DSI operation. Requires an external pullup or pulldown resistor to configure as defined in Table 1. After boot, this GPIO pin will continue to be used as SPI1_DOUT. Select the external pullup or pulldown resistor to not interfere.
GPIO_01	C15	I/O	1	General purpose I/O 01 (hysteresis buffer). Options: 1. SPI1_CLK (output): SPI1 clock signal. This pin is typically connected to the DLPAxxxx SPI_CLK pin. 2. Optional DSI Bus Width Config 0 (input): The controller samples this pin during boot and is used to define the number of lanes used for DSI operation. Requires an external pullup or pulldown resistor to configure as defined in Table 1. After boot, this GPIO pin will continue to be used as SPI1_CLK. Select the external pullup or pulldown resistor to not interfere.
GPIO_00	C14	I/O	1	General purpose I/O 00 (hysteresis buffer). SPI1_DIN (input): SPI1 data input signal. This pin is typically connected to the DLPAxxxx SPI_DOUT pin.

Table 1. GPIO_01 and GPIO_02

GPIO_02	GPIO_01	Number of DSI Data Lanes
DSI Lane Config 1	DSI Lane Config 0	
0	0	1
0	1	2
1	0	3
1	1	4

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Pin Functions – Clock and PLL Support

PIN		I/O	TYPE(1)	DESCRIPTION
NAME	NO.			
PLL_REFCLK_I	H1	I	11	Reference clock crystal input. If an external oscillator is used instead of a crystal, use this pin as the oscillator input.
PLL_REFCLK_O	J1	O	5	Reference clock crystal return. If an external oscillator is used instead of a crystal, leave this pin unconnected (floating with no added capacitive load).

(1) See Table 2 for type definitions.

Pin Functions – Power and Ground

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDD	C5, D5, D7, D12, J4, J12, K3, L4, L12, M6, M9, D9, D13, F13, H13, L13, M10, D3, E3	—	PWR	Core 1.1-V power (main 1.1 V)
VDDLP12	C3	—	PWR	DSI PHY Low Power mode driver supply. It is recommended to externally tie this pin to VDD.
VSS	Common to all package types C4, D6, D8, D10, E4, E13, F4, G4, G12, H4, H12, J3, J13, K4, K12, L3, M4, M5, M8, M12, G13, C6, C8 Only available on DLPC3435 F6, F7, F8, F9, F10, G6, G7, G8, G9, G10, H6, H7, H8, H9, H10, J6, J7, J8, J9, J10, K6, K7, K8, K9, K10	—	GND	Core ground (eDRAM, DSI, I/O ground, thermal ground)
VCC18	C7, C9, D4, E12, F12, K13, M11	—	PWR	All 1.8-V I/O power: (1.8-V power supply for all I/O pins except the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ, LED_SEL, CMP_OUT, GPIO, IIC1, TSTPT, and JTAG pins)
VCC_INTF	M3, M7, N3, N7	—	PWR	Host or parallel interface I/O power: 1.8 V to 3.3 V (Includes IIC0, PDATA, video syncs, and HOST_IRQ pins)
VCC_FLSH	D11	—	PWR	Flash interface I/O power: 1.8 V to 3.3 V (Dedicated SPI0 power pin)
VDD_PLLM	H2	—	PWR	MCG PLL (master clock generator phase lock loop) 1.1-V power
VSS_PLLM	G3	—	RTN	MCG PLL return
VDD_PLLD	J2	—	PWR	DCG PLL (DMD clock generator phase lock loop) 1.1-V power
VSS_PLLD	H3	—	RTN	DCG PLL return

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Table 2. I/O Type Subscript Definition

I/O		SUPPLY REFERENCE	ESD STRUCTURE
SUBSCRIPT	DESCRIPTION		
1	1.8-V LVCMOS I/O buffer with 8-mA drive	V_{cc18}	ESD diode to GND and supply rail
2	1.8-V LVCMOS I/O buffer with 4-mA drive	V_{cc18}	ESD diode to GND and supply rail
3	1.8-V LVCMOS I/O buffer with 24-mA drive	V_{cc18}	ESD diode to GND and supply rail
4	1.8-V sub-LVDS output with 4-mA drive	V_{cc18}	ESD diode to GND and supply rail
5	1.8-V, 2.5-V, 3.3-V LVCMOS with 4-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
6	1.8-V LVCMOS input	V_{cc18}	ESD diode to GND and supply rail
7	1.8-V, 2.5-V, 3.3-V I^2C with 3-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
8	1.8-V I^2C with 3-mA drive	V_{cc18}	ESD diode to GND and supply rail
9	1.8-V, 2.5-V, 3.3-V LVCMOS with 8-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
10	DSI LVDS I/O	V_{DD} for high speed transmit, high speed receive, and low power receive. V_{DDLP12} for low power transmit	ESD diode to GND and supply rail
11	1.8-V, 2.5-V, 3.3-V LVCMOS input	V_{cc_INTF}	ESD diode to GND and supply rail
12	1.8-V, 2.5-V, 3.3-V LVCMOS input	V_{cc_FLSH}	ESD diode to GND and supply rail
13	1.8-V, 2.5-V, 3.3-V LVCMOS with 8-mA drive	V_{cc_FLSH}	ESD diode to GND and supply rail

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)[1]

		MIN	MAX	UNIT
SUPPLY VOLTAGE[2]				
$V_{(VDD)}$		–0.3	1.21	V
$V_{(VDDLP12)}$		–0.3	1.32	V
$V_{(VCC18)}$		–0.3	1.96	V
DMD Sub-LVDS Interface (DMD_HS_CLK_x and DMD_HS_WDATA_x_y)		–0.3	1.96	V
$V_{(VCC_INTF)}$		–0.3	3.60	V
$V_{(VCC_FLSH)}$		–0.3	3.60	V
$V_{(VDD_PLLM)}$ (MCG PLL)		–0.3	1.21	V
$V_{(VDD_PLLD)}$ (DCG PLL)		–0.3	1.21	V
$V_{I2C\ buffer}$ (I/O type 7)		–0.3	See [3]	V
GENERAL				
T_J	Operating junction temperature	–30	125	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to VSS (GND).
(3) I/O is high voltage tolerant; that is, if VCC_INTF = 1.8 V, the input is 3.3-V tolerant, and if VCC_INTF = 3.3 V, the input is 5-V tolerant.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(VDD)}$	Core power 1.1 V (main 1.1 V)		1.045	1.10	1.155	V
$V_{(VDDLP12)}$	DSI PHY low power mode driver supply	See (1) (2)	1.045	1.10	1.155	V
$V_{(VCC18)}$	All 1.8-V I/O power: (1.8-V power supply for all I/O pins except the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ LED_SEL, CMP_OUT, GPIO, IIC1, TSTPT, and JTAG pins.)		1.64	1.80	1.96	V
$V_{(VCC_INTF)}$	Host or parallel interface I/O power: 1.8 to 3.3 V (includes IIC0, PDATA, video syncs, and HOST_IRQ pins)	See (3)	1.64	1.80	1.96	V
			2.28	2.50	2.72	
			3.02	3.30	3.58	
$V_{(VCC_FLSH)}$	Flash interface I/O power: 1.8 V to 3.3 V	See (3)	1.64	1.80	1.96	V
			2.28	2.50	2.72	
			3.02	3.30	3.58	
$V_{(VDD_PLLM)}$	MCG PLL 1.1-V power	See (4)	1.025	1.100	1.155	V
$V_{(VDD_PLLD)}$	DCG PLL 1.1-V power	See (4)	1.025	1.100	1.155	V
T_A	Operating ambient temperature (5)		–30		85	°C
T_J	Operating junction temperature		–30		105	°C

(1) It is recommended that VDDLP12 rail is tied to the VDD rail. The DSI LP supply (VDDLP12) is only used for read responses from the controller which are not supported. Because of this, a separate 1.2-V rail is not required. If a separate 1.2-V supply is already being used to power this rail, a voltage tolerance of ±6.67% is allowed on this separate 1.2-V supply.
(2) When the DSI-PHY LP supply (VDDLP12) is fed from a supply separate from VDD, the VDDLP12 power must sequence ON after the 1.1-V core supply and must sequence OFF before the 1.1-V core supply.
(3) These supplies have multiple valid ranges.
(4) The minimum voltage is lower than other 1.1-V supply minimum to enable additional filtering. This filtering may result in an IR drop across the filter.
(5) The operating ambient temperature range assumes 0 forced air flow, a JEDEC JESD51 junction-to-ambient thermal resistance value at 0 forced air flow ($R_{\theta JA}$ at 0 m/s), a JEDEC JESD51 standard test card and environment, along with minimum and maximum estimated power dissipation across process, voltage, and temperature. Thermal conditions vary by application, and this affects $R_{\theta JA}$. Thus, maximum operating ambient temperature varies by application.
(a) $T_{a_min} = T_{j_min} – (P_{d_min} \times R_{\theta JA}) = –30°C – (0.0\ W \times 30.3°C/W) = –30°C$
(b) $T_{a_max} = T_{j_max} – (P_{d_max} \times R_{\theta JA}) = +105°C – (0.348\ W \times 30.3°C/W) = +94.4°C$

6.4 Thermal Information

THERMAL METRIC (1)			DLPC3430 ZVB (NFBGA) 176 PINS	DLPC3435 ZVB (NFBGA) 201 PINS	UNIT
$R_{\theta JC}$	Junction-to-case top thermal resistance		11.2	10.1	°C/W
$R_{\theta JA}$	Junction-to-air thermal resistance	at 0 m/s of forced airflow (2)	30.3	28.8	°C/W
		at 1 m/s of forced airflow (2)	27.4	25.3	
		at 2 m/s of forced airflow (2)	26.6	24.4	
ψ_{JT}	Temperature variance from junction to package top center temperature, per unit power dissipation (3)		0.27	0.23	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal coefficients abide by JEDEC Standard 51. $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC34xx PCB and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance.
(3) Example: (0.5 W) × (0.2 °C/W) ≈ 0.1°C temperature rise.

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6.5 Power Electrical Characteristics[(1)(2)(3)]

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[(4)]	MAX[(5)]	UNIT
$I_{(VDD)}$ + $I_{(VDD_PLLM)}$ + $I_{(VDD_PLLD)}$	1.1V rails	Frame rate = 60 Hz		111	160	mA
		Frame rate = 120 Hz		132	196	
		Frame rate = 240 Hz		179	295	
$I_{(VDD_PLLM)}$	MCG PLL 1.1-V current[(6)]	Frame rate = 60 Hz		6		mA
		Frame rate = 120 Hz		6		
		Frame rate = 240 Hz		6		
$I_{(VDD_PLLD)}$	DCG PLL 1.1-V current[(6)]	Frame rate = 60 Hz		6		mA
		Frame rate = 120 Hz		6		
		Frame rate = 240 Hz		6		
$I_{(VCC18)}$	All 1.8-V I/O current: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface)	Frame rate = 60 Hz		27	36	mA
		Frame rate = 120 Hz		27	36	
		Frame rate = 240 Hz		27	36	
$I_{(VCC_INTF)}$	Host or parallel interface I/O current: 1.8 to 3.3 V (includes IIC0, PDATA, video syncs, and HOST_IRQ pins)[(6)]	Frame rate = 60 Hz		2		mA
		Frame rate = 120 Hz		2		
		Frame rate = 240 Hz		2		
$I_{(VCC_FLSH)}$	Flash interface I/O current:1.8 to 3.3 V[(6)]	Frame rate = 60 Hz		1		mA
		Frame rate = 120 Hz		1		
		Frame rate = 240 Hz		1		

(1) For the measured cases, all pins using 1.1 V were tied together (including VDDLP12), and programmable host and flash I/O are at the minimum nominal voltage (that is 1.8 V).
(2) Input image is 854 × 480 (WVGA) 24-bits using reduced VESA timings on the parallel interface at the frame rate shown with the 0.2-inch WVGA (DLP2010) DMD. The controller has the CAIC and LABB algorithms turned off.
(3) The measured values do not take into account software updates or customer changes that may affect power performance.
(4) If measured on a system, typical PVT (process, voltage, and temperature) conditions (i.e. nominal process, typical voltage, and 25°C nominal ambient temperature) and various input images were used.
(5) Measured on a system with worst case PVT condition(s) (i.e. corner process, high voltage, and high temperature of 65°C) and white noise input image.
(6) This rail was not measured due to board limitations. Simulation values are used instead. Simulations assume 12.5% activity factor, 30% clock gating on appropriate domains, and mixed SVT (standard threshold voltage) or HVT (high threshold voltage) cells.

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6.6 Pin Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER (1)			TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
V_{IH}	High-level input threshold voltage	I^2C buffer (I/O type 7)		0.7 × VCC_INTF		See (3)	V
		I/O type 1, 2, 3, 6, 8 except pins noted in (4)	VCC18 = 1.8 V	1.17		3.6	
		I/O type 1, 6 for pins noted in (4)	VCC18 = 1.8 V	1.3		3.6	
		I/O type 5, 9, 11	VCC_INTF = 1.8 V	1.17		3.6	
		I/O type 12, 13	VCC_FLSH = 1.8 V	1.17		3.6	
		I/O type 5, 9, 11	VCC_INTF = 2.5 V	1.7		3.6	
		I/O type 12, 13	VCC_FLSH = 2.5 V	1.7		3.6	
		I/O type 5, 9, 11	VCC_INTF = 3.3 V	2.0		3.6	
		I/O type 12, 13	VCC_FLSH = 3.3 V	2.0		3.6	
V_{IL}	Low-level input threshold voltage	I^2C buffer (I/O type 7)		–0.5		0.3 × VCC_INTF	V
		I/O type 1, 2, 3, 6, 8 except pins noted in (4)	VCC18 = 1.8 V	–0.3		0.63	
		I/O type 1, 6 for pins noted in (4)	VCC18 = 1.8 V	–0.3		0.5	
		I/O type 5, 9, 11	VCC_INTF = 1.8 V	–0.3		0.63	
		I/O type 12, 13	VCC_FLSH = 1.8 V	–0.3		0.63	
		I/O type 5, 9, 11	VCC_INTF = 2.5 V	–0.3		0.7	
		I/O type 12, 13	VCC_FLSH = 2.5 V	–0.3		0.7	
		I/O type 5, 9, 11	VCC_INTF = 3.3 V	–0.3		0.8	
		I/O type 12, 13	VCC_FLSH = 3.3 V	–0.3		0.8	
V_{OH}	High-level output voltage	I/O type 1, 2, 3, 6, 8	VCC18 = 1.8 V	1.35			V
		I/O type 5, 9, 11	VCC_INTF = 1.8 V	1.35			
		I/O type 12, 13	VCC_FLSH = 1.8 V	1.35			
		I/O type 5, 9, 11	VCC_INTF = 2.5 V	1.7			
		I/O type 12, 13	VCC_FLSH = 2.5 V	1.7			
		I/O type 5, 9, 11	VCC_INTF = 3.3 V	2.4			
		I/O type 12, 13	VCC_FLSH = 3.3 V	2.4			
V_{OL}	Low-level output voltage	I^2C buffer (I/O type 7)	VCC_INTF > 2 V			0.4	V
		I^2C buffer (I/O type 7)	VCC_INTF < 2 V			0.2 × VCC_INTF	
		I/O type 1, 2, 3, 6, 8	VCC18 = 1.8 V			0.45	
		I/O Type 5, 9, 11	VCC_INTF = 1.8 V			0.45	
		I/O Type 12, 13	VCC_FLSH = 1.8 V			0.45	
		I/O Type 5, 9, 11	VCC_INTF = 2.5 V			0.7	
		I/O Type 12, 13	VCC_FLSH = 2.5 V			0.7	
		I/O Type 5, 9, 11	VCC_INTF = 3.3 V			0.4	
		I/O Type 12, 13	VCC_FLSH = 3.3 V			0.4	

(1) The I/O type refers to the type defined in Table 2.
(2) Test conditions that define a value for VCC18, VCC_INTF, or VCC_FLSH show the nominal voltage that the specified I/O's supply reference is set to.
(3) I/O is high voltage tolerant; that is, if VCC_INTF = 1.8 V, the input is 3.3-V tolerant, and if VCC_INTF = 3.3 V, the input is 5-V tolerant.
(4) Controller pins CMP_OUT, PARKZ, RESETZ, and GPIO_00 through GPIO_19 have slightly varied V_{IH} and V_{IL} range from other 1.8-V I/O.

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Pin Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER (1)			TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
I_{OH}	High-level output current (5)	I/O type 2, 4	VCC18 = 1.8 V	2			mA
		I/O type 5	VCC_INTF = 1.8 V	2			
		I/O type 1	VCC18 = 1.8 V	3.5			
		I/O type 9	VCC_INTF = 1.8 V	3.5			
		I/O type 13	VCC_FLSH = 1.8 V	3.5			
		I/O type 3	VCC18 = 1.8 V	10.6			
		I/O type 5	VCC_INTF = 2.5 V	5.4			
		I/O type 9, 13	VCC_INTF = 2.5V	10.8			
		I/O type 13	VCC_FLSH = 2.5 V	10.8			
		I/O type 5	VCC_INTF = 3.3 V	7.8			
		I/O type 9	VCC_INTF = 3.3 V	15			
		I/O type 13	VCC_FLSH = 3.3 V	15			
I_{OL}	Low-level output current (6)	I^2C buffer (I/O type 7)		3			mA
		I/O type 2, 4	VCC18 = 1.8 V	2.3			
		I/O type 5	VCC_INTF = 1.8 V	2.3			
		I/O type 1	VCC18 = 1.8 V	4.6			
		I/O type 9	VCC_INTF = 1.8 V	4.6			
		I/O type 13	VCC_FLSH = 1.8 V	4.6			
		I/O type 3	VCC18 = 1.8 V	13.9			
		I/O type 5	VCC_INTF = 2.5 V	5.2			
		I/O type 9	VCC_INTF = 2.5 V	10.4			
		I/O type 13	VCC_FLSH = 2.5 V	10.4			
		I/O type 5	VCC_INTF = 3.3 V	4.4			
		I/O type 9	VCC_INTF = 3.3 V	8.9			
		I/O type 13	VCC_FLSH = 3.3 V	8.9			
I_{OZ}	High-impedance leakage current	I^2C buffer (I/O type 7)	$V_{I2C\ buffer}$ < 0.1 × VCC_INTF or $V_{I2C\ buffer}$ > 0.9 × VCC_INTF	–10		10	µA
		I/O type 1, 2, 3, 6, 8,	VCC18 = 1.8 V	–10		10	
		I/O Type 5, 9, 11	VCC_INTF = 1.8 V	–10		10	
		I/O Type 12, 13	VCC_FLSH = 1.8 V	–10		10	
		I/O type 5, 9, 11	VCC_INTF = 2.5 V	–10		10	
		I/O Type 12, 13	VCC_FLSH = 2.5 V	–10		10	
		I/O Type 5, 9, 11	VCC_INTF = 3.3 V	–10		10	
		I/O type 12, 13	VCC_FLSH = 3.3 V	–10		10	

(5) At a high level output signal, the given I/O will be able to output at least the minimum current specified.
(6) At a low level output signal, the given I/O will be able to sink at least the minimum current specified.

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Pin Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER (1)		TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
C_I Input capacitance (including package)	I^2C buffer (I/O type 7)				5	pF
	I/O type 1, 2, 3, 6, 8	VCC18 = 1.8 V	2.6		3.5	
	I/O Type 5, 9, 11	VCC_INTF = 1.8 V	2.6		3.5	
	I/O Type 12, 13	VCC_FLSH = 1.8 V	2.6		3.5	
	I/O type 5, 9, 11	VCC_INTF = 2.5 V	2.6		3.5	
	I/O type 12, 13	VCC_FLSH = 2.5 V	2.6		3.5	
	I/O type 5, 9, 11	VCC_INTF = 3.3 V	2.6		3.5	
	I/O type 12, 13	VCC_FLSH = 3.3 V	2.6		3.5	
	sub-LVDS – DMD high speed (I/O type 4)	VCC18 = 1.8 V			3	

6.7 Internal Pullup and Pulldown Electrical Characteristics

over operating free-air temperature (unless otherwise noted) (1)

INTERNAL PULLUP AND PULLDOWN RESISTOR CHARACTERISTICS	TEST CONDITIONS (2)	MIN	MAX	UNIT
Weak pullup resistance	VCCIO = 3.3 V	29	63	kΩ
	VCCIO = 2.5 V	38	90	kΩ
	VCCIO = 1.8 V	56	148	kΩ
Weak pulldown resistance	VCCIO = 3.3 V	30	72	kΩ
	VCCIO = 2.5 V	36	101	kΩ
	VCCIO = 1.8 V	52	167	kΩ

(1) An external 8-kΩ pullup or pulldown (if needed) would work for any voltage condition to correctly pull enough to override any associated internal pullups or pulldowns.
(2) The resistance is dependent on VCCIO, the pin's supply reference (see a given pins supply reference in Table 2).

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6.8 DMD Sub-LVDS Interface Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CM}	Common mode voltage		0.8	0.9	1.0	V
V_{CM} (Δpp)(1)	V_{CM} change peak-to-peak (during switching)				75	mV
V_{CM} (Δss)(1)	V_{CM} change steady state		–10		10	mV
$\|V_{OD}\|$(2)	Differential output voltage magnitude		170	250	350	mV
V_{OD} (Δ)	V_{OD} change (between logic states)		–10		10	mV
V_{OH}	Single-ended output voltage high		0.825	1.025	1.175	V
V_{OL}	Single-ended output voltage low		0.625	0.775	0.975	V
Tx_{term}	Internal differential termination		80	100	120	Ω
Tx_{load}	100-Ω differential PCB trace (50-Ω transmission lines)		0.5		6	inches

(1) See Figure 1
(2) V_{OD} is the differential voltage measured across a 100-Ω termination resistance connected directly between the transmitter differential pins. $V_{OD} = V_P - V_N$, where P and N are the differential output pins. $|V_{OD}|$ is the magnitude of the peak-to-peak voltage swing across the P and N output pins (see Figure 2). V_{CM} cancels out between signals when measured differentially, thus the reason V_{OD} swings relative to zero.

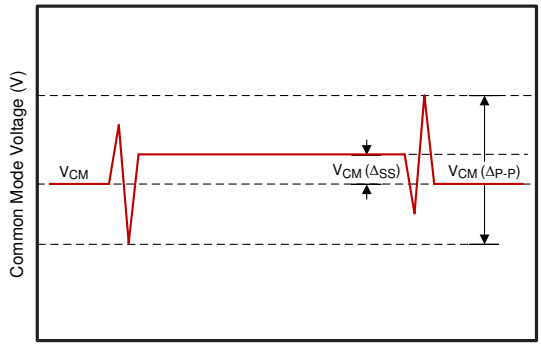
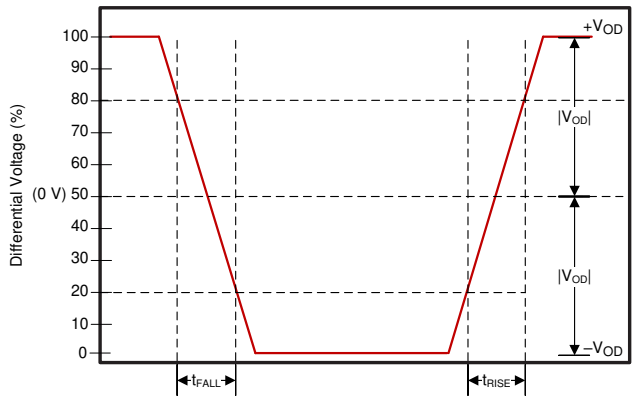


Figure 1. Common Mode Voltage



V_{CM} is removed when the signals are viewed differentially

Figure 2. Differential Output Signal

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6.9 DMD Low-Speed Interface Electrical Characteristics(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(DC)}$	DC output high voltage for DMD_LS_WDATA and DMD_LS_CLK		0.7 × VCC18			V
$V_{OL(DC)}$	DC output low voltage for DMD_LS_WDATA and DMD_LS_CLK				0.3 × VCC18	V
$V_{OH(AC)}$(2)	AC output high voltage for DMD_LS_WDATA and DMD_LS_CLK		0.8 × VCC18		VCC18 + 0.5	V
$V_{OL(AC)}$(3)	AC output low voltage for DMD_LS_WDATA and DMD_LS_CLK		-0.5		0.2 × VCC18	V
Slew rate	DMD_LS_WDATA and DMD_LS_CLK	$V_{OL(DC)}$ to $V_{OH(AC)}$ for rising edge and $V_{OH(DC)}$ to $V_{OL(AC)}$ for rising edge	1.0		3.0	V/ns
	DMD_DEN_ARSTZ	$V_{OL(AC)}$ to $V_{OH(AC)}$ for rising edge	0.25			
	DMD_LS_RDATA		0.5			

(1) See Figure 3 for DMD_LS_CLK, and DMD_LS_WDATA rise and fall times. See Figure 4 for DMD_DEN_ARSTZ rise and fall times.
(2) $V_{OH(AC)}$ maximum applies to overshoot. When the DMD_LS_WDATA and DMD_LS_CLK lines include a proper 43-Ω series termination resistor, the DMD operates within the LPSDR input AC specifications.
(3) $V_{OL(AC)}$ minimum applies to undershoot. When the DMD_LS_WDATA and DMD_LS_CLK lines include a proper 43-Ω series termination resistor, the DMD operates within the LPSDR input AC specifications.

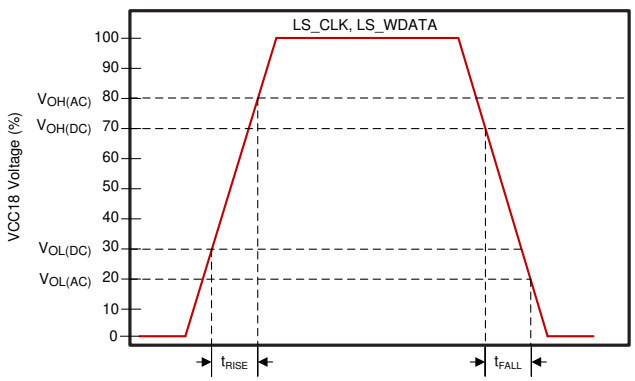

Figure 3. LS_CLK and LS_WDATA Slew Rate

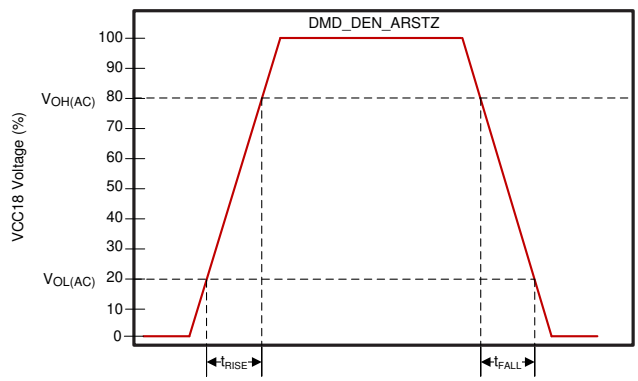

Figure 4. DMD_DEN_ARSTZ Slew Rate

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6.10 System Oscillator Timing Requirements

			MIN	NOM	MAX	UNIT
f_{clk}	Clock frequency, MOSC (master oscillator clock)(1)		23.998	24.000	24.002	MHz
t_c	Cycle time, MOSC (clock period)(1)	See Figure 5	41.663	41.667	41.670	ns
$t_{w(H)}$	Pulse duration as percent of t_c(2), MOSC, high	50% to 50% reference points (signal)	40%	50%		
$t_{w(L)}$	Pulse duration as percent of t_c(2), MOSC, low	50% to 50% reference points (signal)	40%	50%		
t_t	Transition time(2), MOSC	20% to 80% reference points (rising signal) 80% to 20% reference points (falling signal)			10	ns
t_{jp}	Long-term, peak-to-peak, period jitter(2), MOSC (that is the deviation in period from ideal period due solely to high frequency jitter)				2%	

(1) The frequency accuracy for MOSC is ±200 PPM. (This includes impact to accuracy due to aging, temperature, and trim sensitivity.) The MOSC input does not support spread spectrum clock spreading.
(2) Applies only when driven by an external digital oscillator.

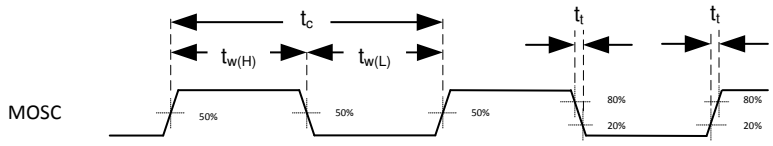

Figure 5. System Oscillators

6.11 Power Supply and Reset Timing Requirements

			MIN	MAX	UNIT
$t_{w(L)}$	Pulse duration, active low, RESETZ	50% to 50% reference points (signal)	1.25		µs
t_r	Rise time, RESETZ(1)	20% to 80% reference points (signal)		0.5	µs
t_f	Fall time, RESETZ(1)	80% to 20% reference points (signal)		0.5	µs
t_{rise}	Rise time, VDD (during VDD ramp up at turn-on)	0.3 V to 1.045 V (VDD)		1	ms

(1) For more information on RESETZ, see *Pin Configuration and Functions*.

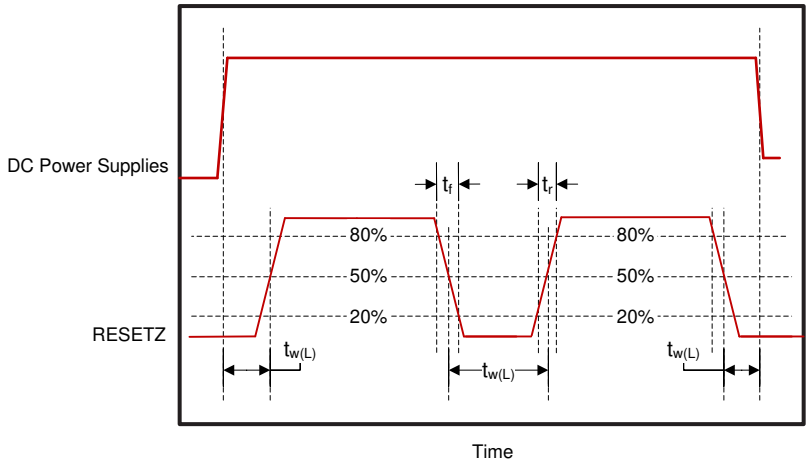

Figure 6. Power-Up and Power-Down RESETZ Timing

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6.12 Parallel Interface Frame Timing Requirements

See 视频时序参数定义 for additional information

			MIN	MAX	UNIT
t_{p_vsw}	Pulse duration – default VSYNC_WE high	50% reference points	1		lines
t_{p_vbp}	Vertical back porch (VBP) – time from the active edge of VSYNC_WE to the active edge of HSYNC_CS for the first active line (1)	50% reference points	2		lines
t_{p_vfp}	Vertical front porch (VFP) – time from the active edge of the HSYNC_CS following the last active line in a frame to the active edge of VSYNC_WE (1)	50% reference points	1		lines
t_{p_tvb}	Total vertical blanking – the sum of VBP and VFP (t_{p_vbp} + t_{p_vfp})	50% reference points	See (1)		lines
t_{p_hsw}	Pulse duration – default HSYNC_CS high	50% reference points	4	128	PCLKs
t_{p_hbp}	Horizontal back porch (HBP) – time from the active edge of HSYNC_CS to the rising edge of DATAEN_CMD	50% reference points	4		PCLKs
t_{p_hfp}	Horizontal front porch (HFP) – time from the falling edge of DATAEN_CMD to the active edge of HSYNC_CS	50% reference points	8		PCLKs

(1) The minimum total vertical blanking is defined by the following equation: t_{p_tvb}(min) = 6 + [8 × Max(1, Source_ALPF/ DMD_ALPF)] lines where:
(a) SOURCE_ALPF = Input source active lines per frame
(b) DMD_ALPF = Actual DMD used lines per frame supported

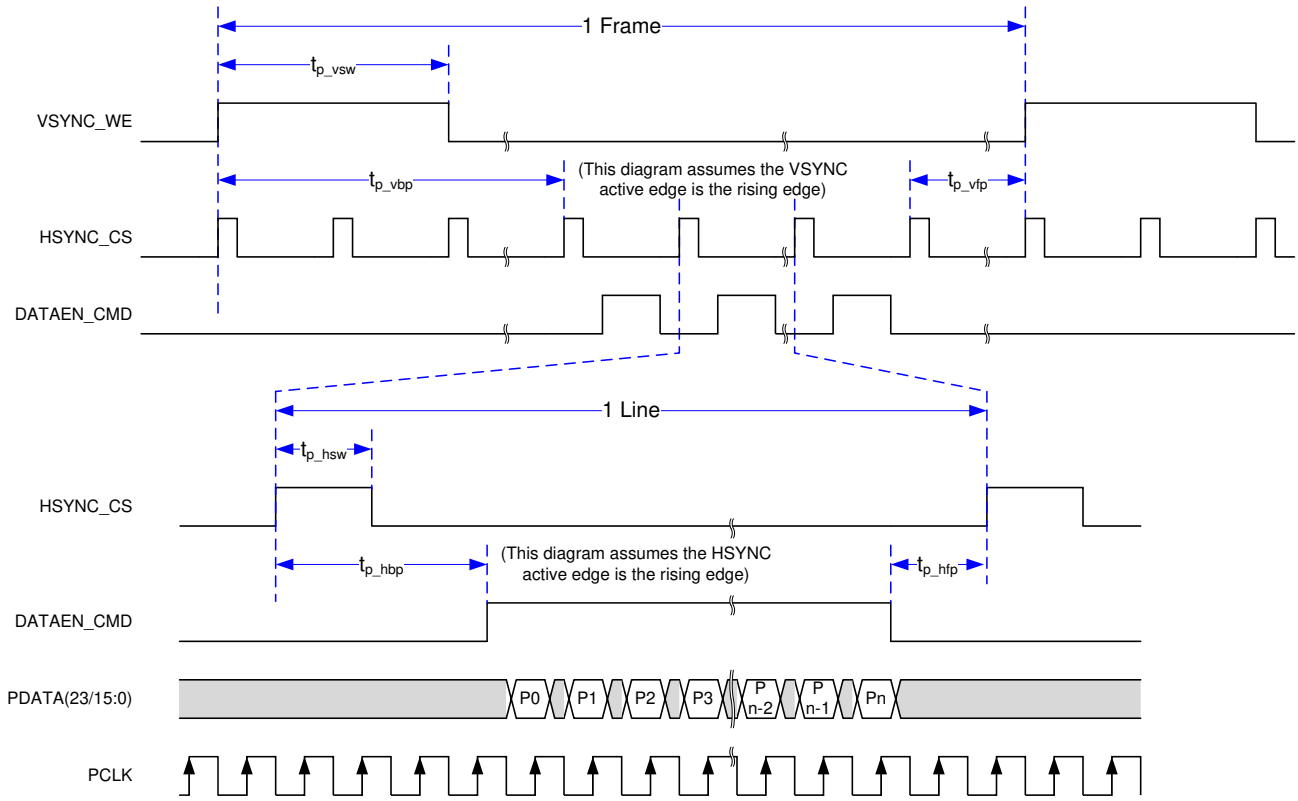

Figure 7. Parallel Interface Frame Timing

6.13 Parallel Interface General Timing Requirements

			MIN	MAX	UNIT
f_{clock}	PCLK frequency		1.0	155.0	MHz
t_{p_clkper}	PCLK period	50% reference points	6.45	1000	ns
t_{p_clkjit}	PCLK jitter	Max f_{clock}		see (1)	
t_{p_wh}	PCLK pulse duration high	50% reference points	2.43		ns
t_{p_wl}	PCLK pulse duration low	50% reference points	2.43		ns
t_{p_su}	Setup time – HSYNC_CS, DATAEN_CMD, PDATA(23:0) valid before the active edge of PCLK	50% reference points	0.9		ns
t_{p_h}	Hold time – HSYNC_CS, DATAEN_CMD, PDATA(23:0) valid after the active edge of PCLK	50% reference points	0.9		ns
t_t	Transition time – all signals	20% to 80% reference points (rising signal) 80% to 20% reference points (falling signal)	0.2	2.0	ns
t_{setup}, 3DR	This is the setup time with respect to VSYNC (2)	50% reference points	1.0		ms
t_{hold}, 3DR	This is the hold time with respect VSYNC (3)	50% reference points	1.0		ms

(1) Calculate clock jitter (in ns) using this formula: Jitter = [1 / f_{clock} – 5.76 ns]. Setup and hold times must be met even with clock jitter.
(2) In other words, the 3DR signal must change at least 1.0 ms before VSYNC changes
(3) In other words, the 3DR signal must not change for at least 1.0 ms after VSYNC changes

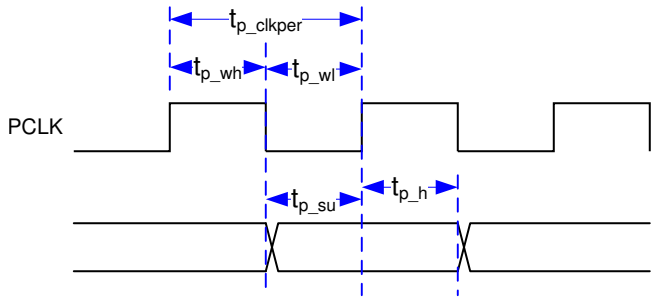

Figure 8. Parallel Interface Pixel Timing

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6.14 BT656 Interface General Timing Requirements

The DLPC34xx controller input interface supports the industry standard BT.656 parallel video interface. See the appropriate ITU-R BT.656 specification for detailed interface timing requirements. (1)

			MIN	MAX	UNIT
f_{cll}	PCLK frequency		1.0	33.5	MHz
t_{p_clkper}	PCLK period	50% reference points	29.85	1000	ns
t_{p_clkjit}	PCLK jitter	Max f_{clock}		See (2)	
t_{p_wh}	PCLK pulse duration high	50% reference points	10.0		ns
t_{p_wl}	PCLK pulse duration low	50% reference points	10.0		ns
t_{p_su}	Setup time – PDATA(7:0) before the active edge of PCLK	50% reference points	3.0		ns
t_{p_h}	Hold time – PDATA(7:0) after the active edge of PCLK	50% reference points	0.9		ns
t_t	Transition time – all signals	20% to 80% reference points (rising signal) 80% to 20% reference points (falling signal)	0.2	3.0	ns

(1) The BT.656 interface accepts 8-bits per color, 4:2:2 YCbCr data encoded per the industry standard through PDATA(7:0) on the active edge of PCLK. See Figure 9.
(2) Calculate clock jitter (in ns) using this formula: Jitter = [1 / f_{clock} – 5.76 ns]. Clock jitter must maintain setup and hold times. BT.656 data bits must be mapped to the DLPC34xx PDATA bus as shown in Figure 9 shows BT.656 bus mode YCbCr 4:2:2 source PDATA (23:0) mapping.

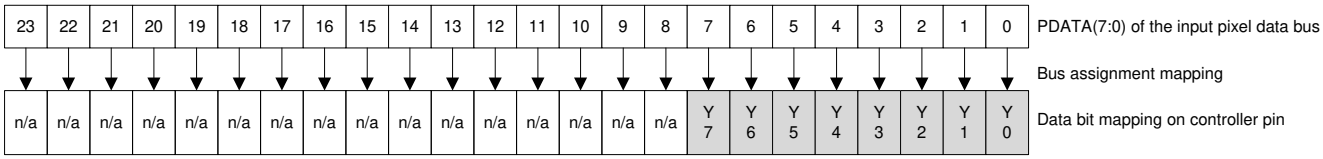

Figure 9. BT.656 Interface Mode Bit Mapping

6.15 DSI Host Timing Requirements

These timing requirements describe specific host minimum values that are higher than those specified in the MIPI standards. It is critical for proper operation that the host meet these minimum timing requirements for specified MIPI parameters. The decoded DSI data must also follow all *Parallel Interface Frame Timing Requirements*.

			MIN	MAX	UNIT
Clock lane	Frequency		80	235	MHz
Data lane	Effective data rate		160	470	Mbps
Number of data lanes	Selectable		1	4	Lanes
$t_{HS\text{-}PREPARE}$+ $t_{HS\text{-}ZERO}$	During a LP to HS transition, the time that the transmitter drives the HS-0 state prior to transmitting the synchronization sequence	80 MHz to 94 MHz HS Clock	565		ns
		95 MHz to 235 MHz HS Clock(1)	465(2)		ns
$t_{HS\text{-}SETTLE}$	Time interval during which the HS receiver ignores any data lane HS transitions, starting from the beginning of $T_{HS\text{-}PREPARE}$; the HS receiver ignores any data lane transitions before the minimum value, and responds to any data lane transitions after the maximum value	80 MHz to 94 MHz HS Clock		565(3)	ns
		95 MHz to 235 MHz HS Clock		465(3)	ns

(1) Example: At 172 MHz and $t_{HS\text{-}PREPARE}$ = 51.46 ns → 51.46 ns + $t_{HS\text{-}ZERO}$ ≥ 465 ns. Therefore $t_{HS\text{-}ZERO}$≥= 413.54 ns.
(2) Minimum values are higher than those required by the MIPI standard. $t_{HS\text{-}PREPARE}$ must be within the MIPI specified range.
(3) Maximum values are higher than those required by the MIPI standard.

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6.16 Flash Interface Timing Requirements

The DLPC34xx flash memory interface consists of a SPI flash serial interface with a programmable clock rate. The DLPC34xx can support 1- to 64-Mb flash memories.(1)(2)(3)

			MIN	MAX	UNIT
f_{clock}	SPI_CLK frequency	See (4)	1.4	36.0	MHz
t_{p_clkper}	SPI_CLK period	50% reference points	27.8	704	ns
t_{p_wh}	SPI_CLK pulse duration high	50% reference points	352		ns
t_{p_wl}	SPI_CLK pulse duration low	50% reference points	352		ns
t_t	Transition time – all signals	20% to 80% reference points (rising signal) 80% to 20% reference points (falling signal)	0.2	3.0	ns
t_{p_su}	Setup time – SPI_DIN valid before SPI_CLK falling edge	50% reference points	10.0		ns
t_{p_h}	Hold time – SPI_DIN valid after SPI_CLK falling edge	50% reference points	0.0		ns
t_{p_clqv}	SPI_CLK clock falling edge to output valid time – SPI_DOUT and SPI_CSZ	50% reference points		1.0	ns
t_{p_clqx}	SPI_CLK clock falling edge output hold time – SPI_DOUT and SPI_CSZ	50% reference points	–3.0	3.0	ns

(1) Standard SPI protocol is to transmit data on the falling edge of SPI_CLK and capture data on the rising edge. The DLPC34xx does transmit data on the falling edge, but it also captures data on the falling edge rather than the rising edge. This provides support for SPI devices with long clock-to-Q timing. DLPC34xx hold capture timing has been set to facilitate reliable operation with standard external SPI protocol devices.
(2) With the above output timing, DLPC34xx provides the external SPI device 8.2-ns input set-up and 8.2-ns input hold, relative to the rising edge of SPI_CLK.
(3) For additional requirements of the external flash device view the *SPI Flash Interface* section.
(4) This range include the ±200 ppm of the external oscillator (but no jitter).

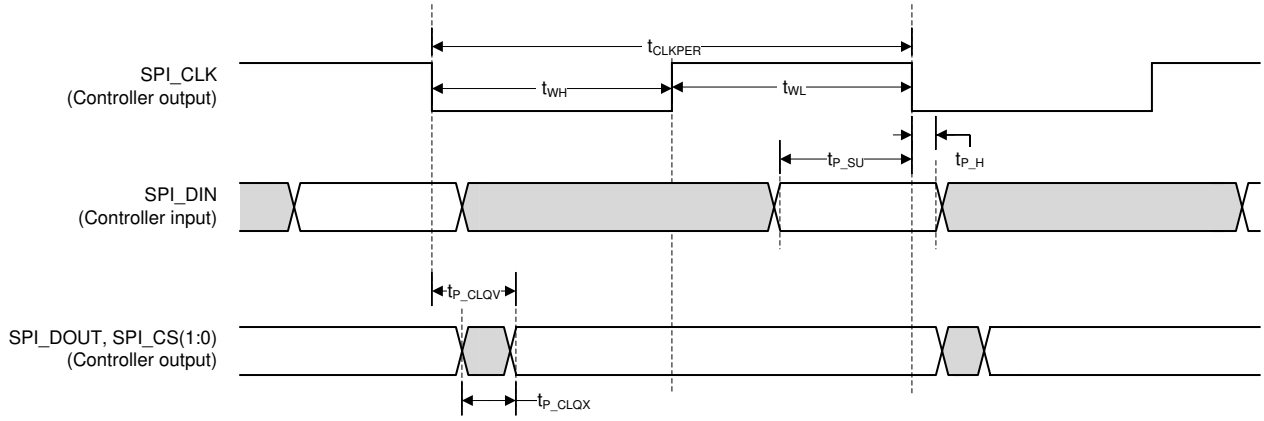

Figure 10. Flash Interface Timing

6.17 Other Timing Requirements

		MIN	MAX	UNIT
t_{rise}, all(1)(2)	20% to 80% reference points		10	ns
t_{fall}, all(1)(2)	80% to 20% reference points		10	ns
t_{rise}, PARKZ(2)	20% to 80% reference points		150	ns
t_{fall}, PARKZ(2)	80% to 20% reference points		150	ns
t_w, GPIO_08 (normal park) pulse width(3)		200		ms
I^2C baud rate			100	kHz

(1) Unless noted elsewhere, the following signal transition times are for all DLPC34xx signals.
(2) This is the recommended signal transition time to avoid input buffer oscillations.
(3) The pulse width encompasses the minimum high time and the minimum low time for this signal.

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6.18 DMD Sub-LVDS Interface Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R (1)	Differential output rise time				250	ps
t_F (1)	Differential output fall time				250	
t_{switch}	DMD HS Clock switching rate			1200		Mbps
f_{clock}	DMD HS Clock frequency			600		MHz
DCout	DMD HS Clock output duty cycle		45%	50%	55%	

(1) Rise and fall times are defined for the differential V_{OD} signal as shown in Figure 2.

6.19 DMD Parking Switching Characteristics

See (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{park}	Normal Park time (2)				20	ms
$t_{fast\ park}$	Fast park time (3)				32	µs

(1) The oscillator and power supplies must remain active for at least the duration of the park time. The power supplies must additionally be held on for a time after parking is completed to satisfy DMD requirements. See *System Power-Up and Power-Down Sequence* and the appropriate DMD or PMIC datasheet for more information.
(2) Normal park time is defined as how long it takes the DLPC34xx controller to complete the parking of the DMD after it receives the normal park request (GPIO_08 goes low).
(3) Fast park time is defined as how long it takes the DLPC34xx controller to complete the parking of the DMD after it receives the fast park request (PARKZ goes low).

6.20 Chipset Component Usage Specification

The DLPC3430 and DLPC3435 are components of a DLP chipset. Reliable function and operation of the DLP chipset requires that it be used with all components (DMD, PMIC, and controller) of the applicable DLP chipset.

Table 3. DLPC3430 and DLPC3435 Supported DMDs and PMICs

DLPC3430 and DLPC3435 DLP Chipset	
DMD	DLP2010
PMIC	DLPA2000
	DLPA2005
	DLPA3000

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7 Detailed Description

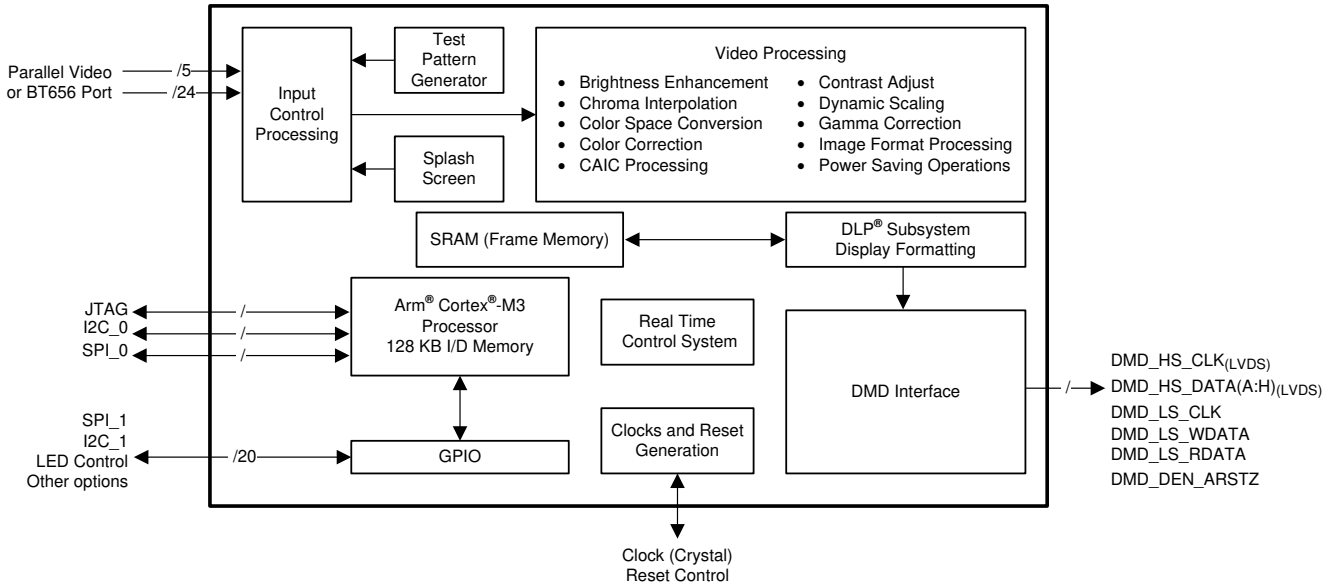
7.1 Overview

The DLPC3430 and DLPC3435 parts are display controllers for the DLP2010 (.2 WVGA) DMD. The DLPC3430 and DLPC3435 controllers are part of the chipset composed of the controller, DLP2010 (.2 WVGA) DMD, and DLPAxxxx PMIC (which includes an LED driver). To ensure reliable operation of the DLP chipset, the DLPC34xx must always be used with the supported devices shown in Table 3.

The DLPC34xx display controller provides interfaces along with data and image processing functions that are optimized for small form factor and power-constrained display applications. Applications include projection within mobile projectors, smart displays, smartphones, tablets, augmented reality glasses, mobile accessories, smart home displays, and pico projectors. The DLPC34xx is not a front-end processor; therefore, standalone projectors must include a separate front-end chip to interface to the outside world (for example, a video decoder, HDMI receiver, or USB I/F chip).

The DLPC3430 and DLPC3435 are functionally equivalent with the exception of package size and DSI functionality. The DLPC3430 comes in a smaller package and supports the DSI interface. The DLPC3435 comes in a larger package size and does not support the DSI interface.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Input Source Requirements

7.3.1.1 Supported Resolution and Frame Rates

Table 4. Supported Input Source Ranges(1)(2)(3)

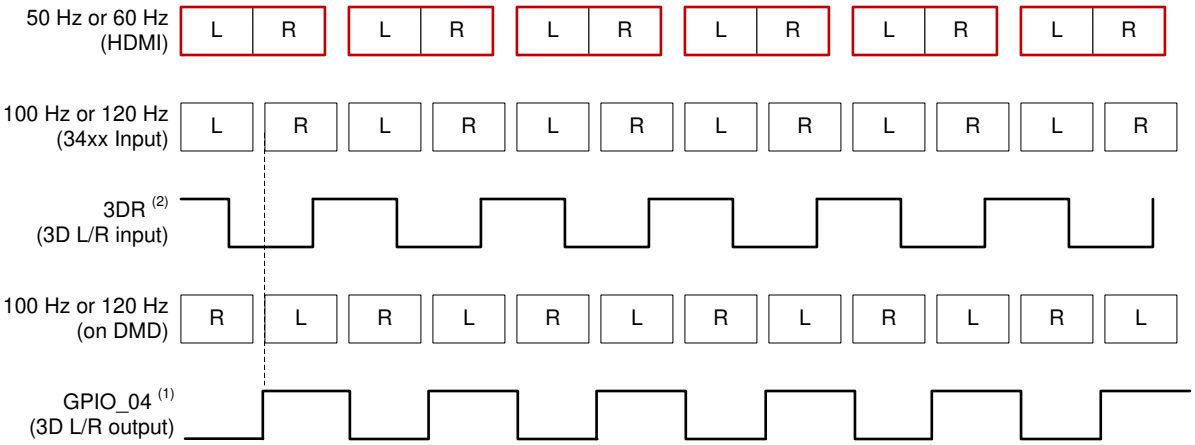
INTERFACE	Bits per Pixel (max)(4)	IMAGE TYPE	SOURCE RESOLUTION RANGE(5) (pixels)				FRAME RATE RANGE (Hz)
			HORIZONTAL		VERTICAL		
			Landscape	Portrait	Landscape	Portrait	
Parallel	24	2D only	320 to 1280	200 to 800	200 to 800	320 to 1280	10 to 242
	24	3D only	320 to 1280	200 to 720	200 to 720	320 to 1280	100 ±2 120 ±2
DSI(6)(7)	24	2D only	320 to 1280	200 to 800	200 to 800	320 to 1280	10 to 122
BT.656-NTSC(8)	See (9)	2D only	720	n/a	240	n/a	60 ±2
BT.656-PAL(8)	See (9)	2D only	720	n/a	288	n/a	50 ±2

(1) The application must remain within specifications for all source interface parameters such as maximum clock rate and maximum line rate.
(2) The maximum DMD size for all rows in the table is 854 × 480 pixels.
(3) To achieve the ranges stated, the firmware must support the source parameters. Review the firmware release notes or contact TI to determine the latest available frame rate and input resolution support for a given firmware image.
(4) Bits per pixel does not necessarily equal the number of data pins used on the DLPC34xx controller.
(5) By using an I^2C command, the controller can rotate portrait image inputs on the DMD by minus 90 degrees so that the image displays in landscape format.
(6) Only 16-bit pixel mode can be supported with 1280 × 720 pixel input resolution at 120 Hz due to the DSI data rate limit.
(7) Applications may require up to four DSI lanes in order to fully utilize the available DSI bandwidth (and therefore achieve the maximum display rates and resolutions).
(8) All parameters in this row follow the BT.656 standard. The image format is always landscape.
(9) BT.656 uses 16-bit 4:2:2 YCbCr.

7.3.1.2 3D Display

For 3D sources on the parallel or MIPI DSI interface, images must be frame sequential (L, R, L, ...) when input to the DLPC34xx controller. Any processing required to unpack 3D images and to convert them to frame sequential input must be done by external electronics prior to inputting the images to the controller. Each 3D source frame input must contain a single eye frame of data, separated by a VSYNC, where an eye frame contains image data for a single left or right eye. The signal 3DR input to the controller indicates whether the input frame is for the left eye or right eye.

Each DMD frame is displayed at the same rate as the input interface frame rate. Figure 11 shows the typical timing for a 50-Hz or 60-Hz 3D HDMI source frame, the input interface of the DLPC34xx controller, and the DMD. In general, video frames sent over the HDMI interface pack both the left and right content into the same video frame. GPIO_04 is optionally sent to a transmitter on the system PCB for wirelessly transmitting a synchronization signal to 3D glasses (usually an IR sync signal). The glasses are then in phase with the DMD images displayed. Alternately, *3D Glasses Operation* shows how DLP link pulses can be used instead.



(1) Left = 1, Right = 0

(2) 3DR must toggle at least 1 ms before VSYNC

Figure 11. 3D Display Left and Right Frame Timing

7.3.1.3 Parallel Interface

The parallel interface complies with standard graphics interface protocol, which includes the signals listed in Table 5.

Table 5. Parallel Interface Signals

SIGNAL	DESCRIPTION
VSYNC_WE	vertical sync
HSYNC_CS	horizontal sync
DATAEN_CMD	data valid
PDATA	24-bit data bus
PCLK	pixel clock
PDM_CVS_TE	parallel data mask (optional)

NOTE

VSYNC_WE must remain active at all times when using parallel RGB mode. When this signal is no longer active, the display sequencer stops and causes the LEDs to turn off.

The active edge of both sync signals are variable. *Parallel Interface Frame Timing Requirements* shows the relationship of these signals.

An optional parallel data mask signal (PDM_CVS_TE) allows periodic frame updates to be stopped without losing the displayed image. When active, PDM_CVS_TE acts as a data mask and does not allow the source image to be propagated to the display. A programmable PDM polarity parameter determines if it is active high or active low. PDM_CVS_TE defaults to active high. To disable the data mask function, tie PDM_CVS_TE to a logic low signal. PDM_CVS_TE must only change during vertical blanking.

The parallel interface supports six data transfer formats. They are as follows:

- 24-bit RGB888 or 24-bit YCbCr888 on a 24 data wire interface
- 18-bit RGB666 or 18-bit YCbCr666 on an 18 data wire interface
- 16-bit RGB565 or 16-bit YCbCr565 on a 16 data wire interface
- 16-bit YCbCr 4:2:2 (standard sampling assumed to be Y0Cb0, Y1Cr0, Y2Cb2, Y3Cr2, Y4Cb4, Y5Cr4, ...)
- 8-bit RGB888 or 8-bit YCbCr888 serial (1 color per clock input; 3 clocks per displayed pixel) on an 8 data wire interface
- 8-bit YCbCr 4:2:2 serial (1 color per clock input; 2 clocks per displayed pixel) on an 8 data wire interface

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The *PDATA Bus – Parallel Interface Bit Mapping Modes* section shows the required PDATA(23:0) bus mapping for these six data transfer formats.

7.3.1.3.1 PDATA Bus – Parallel Interface Bit Mapping Modes

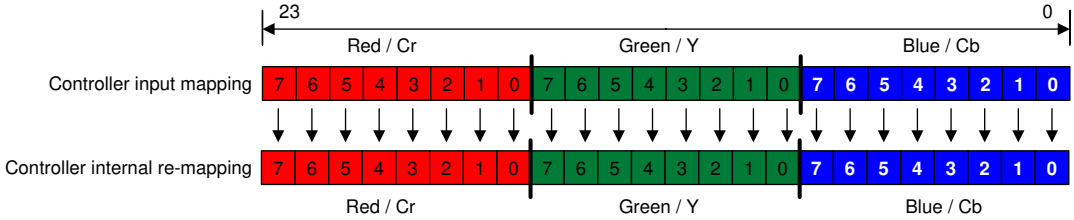

图 12. RGB-888 and YCbCr-888 I/O Mapping

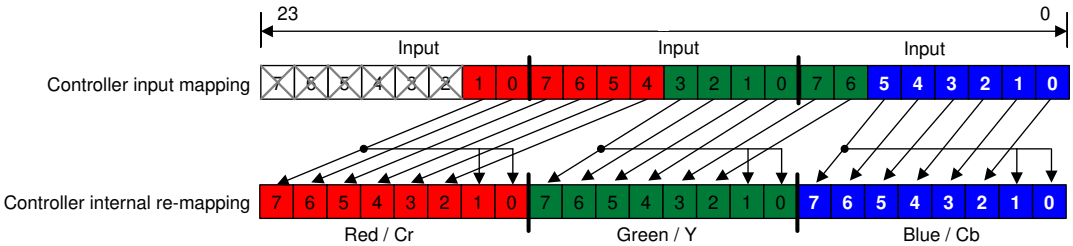

图 13. RGB-666 and YCbCr-666 I/O Mapping

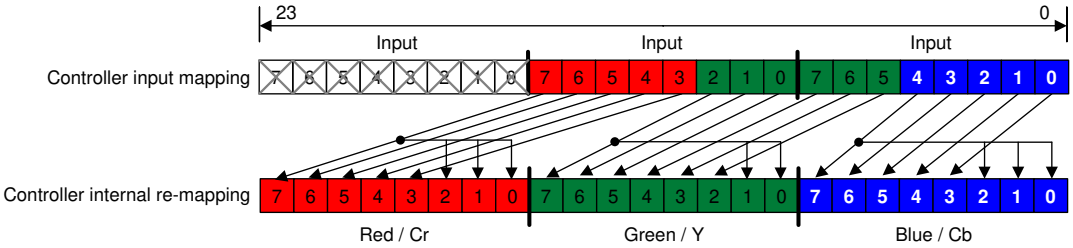

图 14. RGB-565 and YCbCr-565 I/O Mapping

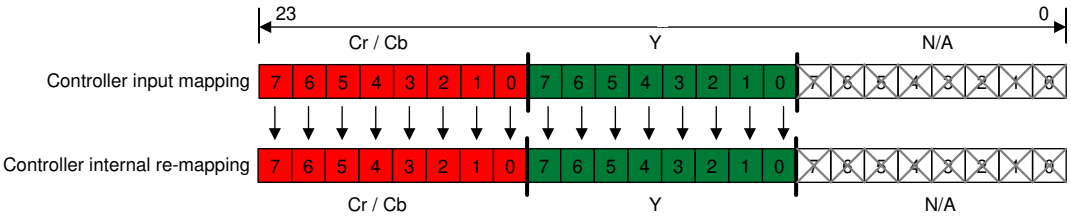

图 15. 16-Bit YCbCr-880 I/O Mapping

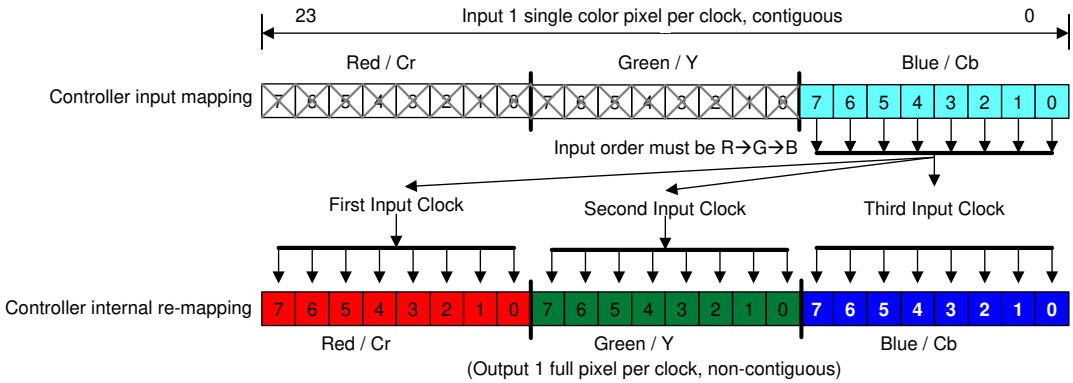

图 16. 8-Bit RGB-888 or YCbCr-888 I/O Mapping

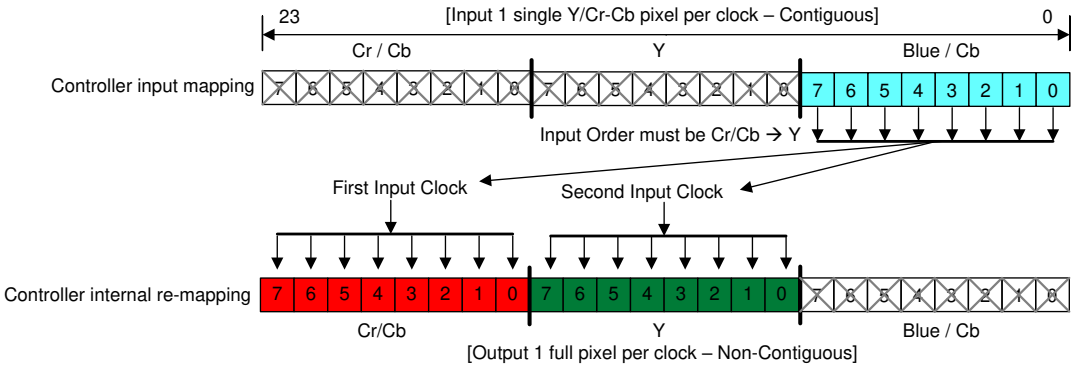

图 17. 8-Bit Serial YCbCr-422 I/O Mapping

7.3.1.4 DSI Interface

The DLPC34xx controller supports the industry standard DSI (Display Serial Interface) Type-3 LVDS video interface with up to four lanes. DSI is a source-synchronous, high-speed, low-power, low-cost physical layer. The DSI-PHY unit receives data when it operates in high-speed (HS) mode. The DSI-PHY unit receives and transmits data when it operates in low-power (LP) mode for unidirectional data lanes. Point-to-point lane interconnect can be used for either data or clock signal transmission. The high-speed receiver is a differential line receiver circuit. The low-power receiver is an unterminated, single-ended receiver circuit. Figure 18 shows a high-level view of the DSI interface.

For a given frame rate, the DSI high-speed (HS) clock frequency must be fixed. If a different DSI clock frequency is ever needed (such as to support another frame rate), an I^2C command must be sent to the controller with the updated HS clock frequency.

MIPI refers to the Mobile Industry Processor Interface standard.

Various DSI requirements and features of the DLPC34xx are as follows:

- compliant with the DSI-MIPI Specification for Display Serial Interface (V 1.02.00) except for those items noted in the *DSI Host Timing Requirements* table
- compliant with D-PHY standard MIPI Specification (V 1.0)
- MIPI DSI Type 3 architecture
- supports display resolutions from 320 × 200 to 1280 × 800
- supports video mode (command mode not supported)
- MIPI DCS^{SM} (Display Command Set^{SM}) commands sent over DSI not supported (send commands via I^2C instead)
- supports multiple packets per transmission

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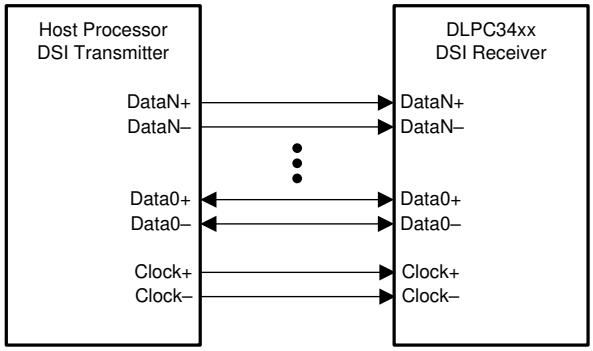
- supports trigger messages in the forward direction
- data lanes configurable from one to four channels
- EOT (End of Transfer) command is supported and must be enabled
- CRC (cyclic redundancy check) and ECC (error correction code) for header supported
  - CRC and ECC can be disabled
- checksum for long packets with error reporting (but no ECC)
- supports one virtual channel for video mode
- supports burst mode
- supports non-burst with sync pulses and with sync event
- BTA (bus turn-around) mode not supported and must be disabled in the DSI host processor
- LP mode is required during vertical blanking and vertical sync. LP mode is not supported between pixel lines (i.e. HS blanking must be used for horizontal blanking and horizontal sync)
- an active DSI HS clock is required during LP blanking



- one clock lane
- one bi-directional data lane (Data0)
- up to three additional uni-directional data lanes (Data1, Data2, and Data3)

Figure 18. DSI High Level View

The differential DSI clock lane (DCLKN and DCLKP) must be in the LP11 (Idle) state upon the de-assertion of RESETZ (zero-to-one transition) and must remain in this state until HOST_IRQ is de-asserted (one-to-zero transition) to ensure proper DSI initialization.

The controller requires differential data lane '0' (DD0N:DD0P) for DSI operation. The three remaining data lanes are optional depending on the desired input resolution and frame rate. Not all display resolutions and frame rates are supported without using all four data lanes.

The state of GPIO (2:1) pins upon the de-assertion of RESETZ (zero-to-one transition) determines the number of DSI data lanes that are enabled for both LP and HS bus operation.

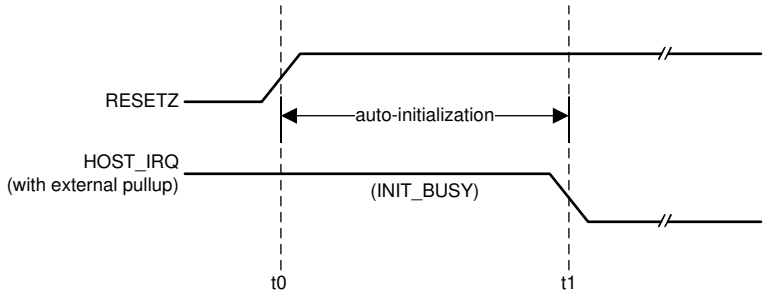
Only the DLPC3430 controller supports the DSI interface. The DLPC3435 controller does not support the DSI interface.

DSI supported data transfer formats are as follows:

- 24-bit RGB888 - each pixel uses 3 bytes
- 18-bit RGB666 - each pixel packed into 2 or more bytes
- 18-bit RGB666 - each pixel loosely packed into 3 bytes
- 16-bit RGB565 - each pixel uses 2 bytes
- 16-bit 4:2:2 YCbCr - each pixel uses 2 bytes

7.3.2 Device Startup

- The HOST_IRQ signal is provided to indicated when the system has completed auto-initialization.
- While reset is applied, HOST_IRQ is tri-stated (an external pullup resistor pulls the line high).
- HOST_IRQ remains tri-stated (pulled high externally) until the boot process completes. While the signal is pulled high, this indicates that the controller is performing boot-up and auto-initialization.
- As soon as possible after the controller boots-up, the controller drives HOST_IRQ to a logic high state to indicate that the controller is continuing to perform auto-initialization (no real state changes occur on the external signal).
- The software sets HOST_IRQ to a logic low state at the completion of the auto-initialization process. At the falling edge of the signal, the initialization is complete.
- The DLPC34xx controller is ready to receive commands through I^2C or accept video over the DSI or the parallel interface only after auto-initialization is complete.
- The controller initialization typically completes (HOST_IRQ goes low) within 500 ms of RESETZ being asserted. However, this time may vary depending on the software version and the contents of the user configurable auto initialization file.



t0: rising edge of RESETZ; auto-initialization begins

t1: falling edge of HOST_IRQ; auto-initialization is complete

Figure 19. HOST_IRQ Timing

7.3.3 SPI Flash

7.3.3.1 SPI Flash Interface

The DLPC34xx controller requires an external SPI serial flash memory device to store the firmware. Follow the below guidelines and requirements in addition to the requirements listed in the *Flash Interface Timing Requirements* section.

The controller supports a maximum flash size of 64 Mb (8 MB). See 表 9 for example compatible flash options. The minimum required flash size depends on the size of the utilized firmware. The firmware size depends upon a variety of factors including the number of sequences, lookup tables, and splash images.

The DLPC34xx controller uses a single SPI interface that complies to industry standard SPI flash protocol. The device will begin accessing the flash at a nominal 1.42 MHz frequency before running at a nominal 30 MHz rate. The flash device must support these rates.

The controller has two independent SPI chip select (CS) control lines. Ensure the flash device's chip select pin is connected to SPI0_CSZ0 as the controller's boot routine is executed from the device connected to chip select zero. The boot routine uploads program code from flash memory to program memory then transfers control to an auto-initialization routine within program memory.

The DLPC34xx is designed to support any flash device that is compatible with the modes of operation, features, and performance as defined in Table 6, Table 7, and Table 8.

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Table 6. Additional DLPC34xx SPI Flash Requirements

FEATURE	DLPC34xx REQUIREMENT
SPI interface width	Single
SPI polarity and phase settings	SPI mode 0
Fast READ addressing	Auto-incrementing
Programming mode	Page mode
Page size	256 B
Sector size	4 KB sector
Block size	Any
Block protection bits	0 = Disabled
Status register bit(0)	Write in progress (WIP), also called flash busy
Status register bit(1)	Write enable latch (WEN)
Status register bits(6:2)	A value of 0 disables programming protection
Status register bit(7)	Status register write protect (SRWP)
Status register bits(15:8) (that is expansion status byte)	Because the DLPC34xx controller supports only single-byte status register R/W command execution, it may not be compatible with flash devices that contain an expansion status byte. However, as long as the expansion status byte is considered optional in the byte 3 position and any write protection control in this expansion status byte defaults to unprotected, then the flash device is likely compatible with the DLPC34xx.

The DLPC34xx controller is intended to support flash devices with program protection defaults of either enabled or disabled. The controller assumes the default is enabled and proceeds to disable any program protection as part of the boot process.

The DLPC34xx issues these commands during the boot process:

- A write enable (WREN) instruction to request write enable, followed by
- A read status register (RDSR) instruction (repeated as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, a write status register (WRSR) instruction that writes 0 to all 8-bits (this disables all programming protection)

Prior to each program or erase instruction, the DLPC34xx controller issues similar commands:

- A write enable (WREN) instruction to request write enable, followed by
- A read status register (RDSR) instruction (repeated as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, the program or erase instruction

Note that the flash device automatically clears the write enable status after each program and erase instruction.

Table 7 and Table 8 list the specific instruction OpCode and timing compatibility requirements. The DLPC34xx controller does not adapt protocol or clock rate based on the flash type connected.

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Table 7. SPI Flash Instruction OpCode and Access Profile Compatibility Requirements

SPI FLASH COMMAND	BYTE 1 (OPCODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Fast READ (1 Output)	0x0B	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0)(1)
Read status	0x05	N/A	N/A	STATUS(0)		
Write status	0x01	STATUS(0)	(2)			
Write enable	0x06					
Page program	0x02	ADDRS(0)	ADDRS(1)	ADDRS(2)	DATA(0)(1)	
Sector erase (4 KB)	0x20	ADDRS(0)	ADDRS(1)	ADDRS(2)		
Chip erase	0xC7					

(1) Shows the first data byte only. Data continues.
(2) Access to a second (expansion) Write Status byte not supported by the DLPC34xx controller.

Table 8 and the *Flash Interface Timing Requirements* section list the specific timing compatibility requirements for a DLPC34xx compatible flash device.

Table 8. SPI Flash Key Timing Parameter Compatibility Requirements(1)(2)

SPI FLASH TIMING PARAMETER	SYMBOL	ALTERNATE SYMBOL	MIN	MAX	UNIT
Access frequency (all commands)	FR	f_C	≤1.4	≥ 30.1	MHz
Chip select high time (also called chip select deselect time)	t_{SHSL}	t_{CSH}	≤ 200		ns
Output hold time	t_{CLQX}	t_{HO}	≥ 0		ns
Clock low to output valid time	t_{CLQV}	t_V		≤ 11	ns
Data in set-up time	t_{DVCH}	t_{DSU}	≤ 5		ns
Data in hold time	t_{CHDX}	t_{DH}	≤ 5		ns

(1) The timing values apply to the specification of the peripheral flash device, not the DLPC34xx controller. For example, the flash device minimum access frequency (FR) must be 1.4 MHz or less and the maximum access frequency must be 30.1 MHz or greater.
(2) The DLPC34xx does not drive the $\overline{HOLD}$ or $\overline{WP}$ (active low write protect) pins on the flash device, and thus these pins must be tied to a logic high on the PCB through an external pullup.

In order for the DLPC34xx controller to support 1.8-V, 2.5-V, or 3.3-V serial flash devices, the VCC_FLSH pin must be supplied with the corresponding voltage. 表 9 contains a list of validated 1.8-V, 2.5-V, or 3.3-V compatible SPI serial flash devices supported by the DLPC34xx controller.

表 9. DLPC34xx Validated SPI Flash Device Options(1)(2)(3)

DENSITY (Mb)	VENDOR	PART NUMBER	PACKAGE SIZE
1.8-V COMPATIBLE DEVICES			
4 Mb	Winbond	W25Q40BWUXIG	2 × 3 mm USON
4 Mb	Macronix	MX25U4033EBAI-12G	1.43 × 1.94 mm WLCSP
8 Mb	Macronix	MX25U8033EBAI-12G	1.68 × 1.99 mm WLCSP
2.5- OR 3.3-V COMPATIBLE DEVICES			
16 Mb	Winbond	W25Q16CLZPIG	5 × 6 mm WSON

(1) The flash supply voltage must equal VCC_FLSH supply voltage on the DLPC34xx controller. Make sure to order the device that supports the correct supply voltage as multiple voltage options are often available.
(2) Numonyx (Micron) serial flash devices typically do not support the 4 KB sector size compatibility requirement for the DLPC34xx controller.
(3) The flash devices in this table have been formally validated by TI. Other flash options may be compatible with the DLPC34xx controller, but they have not been formally validated by TI.

7.3.3.2 SPI Flash Programming

The SPI pins of the flash can directly be driven for flash programming while the DLPC34xx controller I/Os are tri-stated. SPI0_CLK, SPI0_DOUT, and SPI0_CSZ0 I/O can be tri-stated by holding RESETZ in a logic low state while power is applied to the controller. The logic state of the SPI0_CSZ1 pin is not affected by this action. Alternatively, the DLPC34xx controller can program the SPI flash itself when commanded via I^2C if a valid firmware image has already been loaded and the controller is operational.

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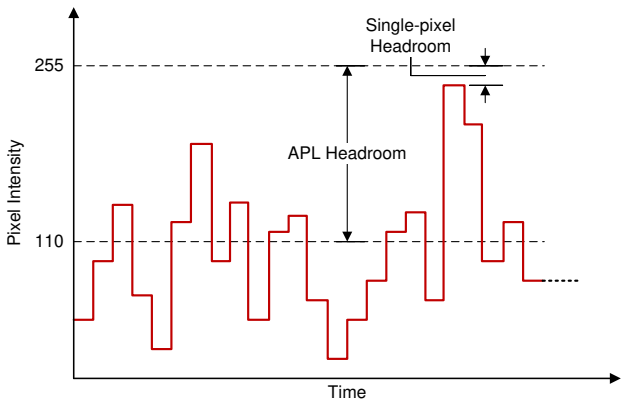
7.3.4 I²C Interface

Both of the DLPC34xx I²C interface ports support a 100-kHz baud rate. Because I²C interface transactions operate at the speed of the slowest device on the bus, there is no requirement to match the speed of all devices in the system.

7.3.5 Content Adaptive Illumination Control (CAIC)

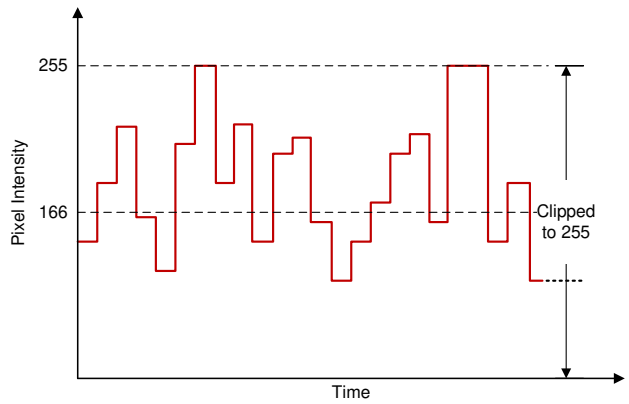
Content Adaptive Illumination control (CAIC) is part of the IntelliBright™ suite of advanced image processing algorithms that adaptively enhances brightness and reduces power. In common real-world image content most pixels in the images are well below full scale for the for the R (red), G (green), and B (blue) digital channels input to the DLPC34xx. As a result of this, the average picture level (APL) for the overall image is also well below full scale, and the dynamic range for the collective set of pixel values is not fully used. CAIC takes advantage of the headroom between the source image APL and the top of the available dynamic range of the display system.

CAIC evaluates images on a frame-by-frame basis and derives three unique digital gains, one for each of the R, G, and B color channel. During image processing, CAIC applies each gain to all pixels in the associated color channel. The calculated gain is applied to all pixels in that channel so that the pixels as a group collectively shift upward and as close to full scale as possible. To prevent any image quality degradation, the gains are set at the point where just a few pixels in each color channel are clipped. Figure 20 and Figure 21 show an example of the application of CAIC for one color channel.



(1) APL = 110

Figure 20. Source Pixels for a Color Channel

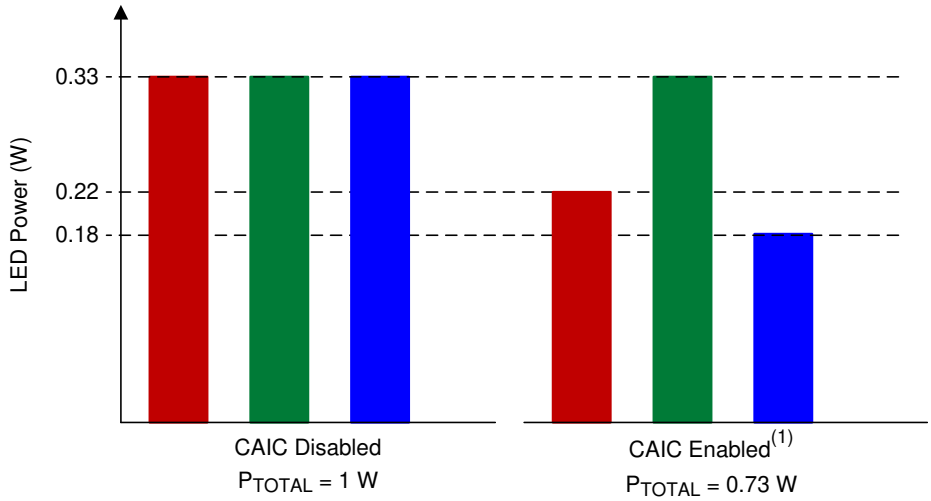


(1) APL = 166

(2) Channel gain = 166/110 = 1.51

Figure 21. Pixels for a Color Channel After CAIC Processing

Figure 21 shows the gain that is applied to a color processing channel inside the DLPC34xx. Additionally, CAIC adjusts the power for the R, G, and B LED by commanding different LED currents. For each color channel of an individual frame, CAIC intelligently determines the optimal combination of digital gain and LED power. The user configurable CAIC settings heavily influence the amount of digital gain that is applied to a color channel and the LED power for that color.



(1) With CAIC enabled, if red and blue LEDs require less than nominal power for a given input image, the red and blue LED power will reduce.

Figure 22. CAIC Power Reduction Mode (for Constant Brightness)

As CAIC applies a digital gain to each color channel and adjusts the power to each LED, CAIC ensures the resulting color balance in the final image matches the target color balance for the projector system. Thus, the effective displayed white point of images is held constant by CAIC from frame to frame.

CAIC can be used to increase the overall image brightness while holding the total power for all LEDs constant, or CAIC can be used to hold the overall image brightness constant while decreasing LED power. In summary, CAIC has two primary modes of operation:

- Power reduction mode holds overall image brightness constant while reducing LED power
- Enhanced brightness mode holds overall LED power constant while enhancing image brightness

In power reduction mode, since the R, G, and B channels can be gained up by CAIC inside the DLPC34xx, the LED power can be reduced for any color channel until the brightness of the color on the screen is unchanged. Thus, CAIC can achieve an overall LED power reduction while maintaining the same overall image brightness as if CAIC was not used. Figure 22 shows an example of LED power reduction by CAIC for an image where the red and blue LEDs can consume less power.

In enhanced brightness mode the R, G, and B channels can be gained up by CAIC with LED power generally being held constant. This results in an enhanced brightness with no power savings.

While there are two primary modes of operation described, the DLPC34xx actually operates within the extremes of pure power reduction mode and enhanced brightness mode. The user can configure which operating mode the DLPC34xx will more closely follow by adjusting the CAIC gain setting as described in the software programmer's guide.

7.3.6 Local Area Brightness Boost (LABB)

Local area brightness boost (LABB), part of the IntelliBright™ suite of advanced image processing algorithms, adaptively gains up regions of an image that are dim relative to the average picture level. The controller applies significant gain to some regions of the image, and applies little or no gain to other regions. The LABB algorithm evaluates images frame-by-frame and calculates the local area gains to be used for each image. Since many images have a net overall boost in gain, even if the controller applies no gain to some parts of the image, the controller boosts the overall perceived brightness of the image.

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Figure 23 shows a split screen example of the impact of the LABB algorithm for an image that includes dark areas.

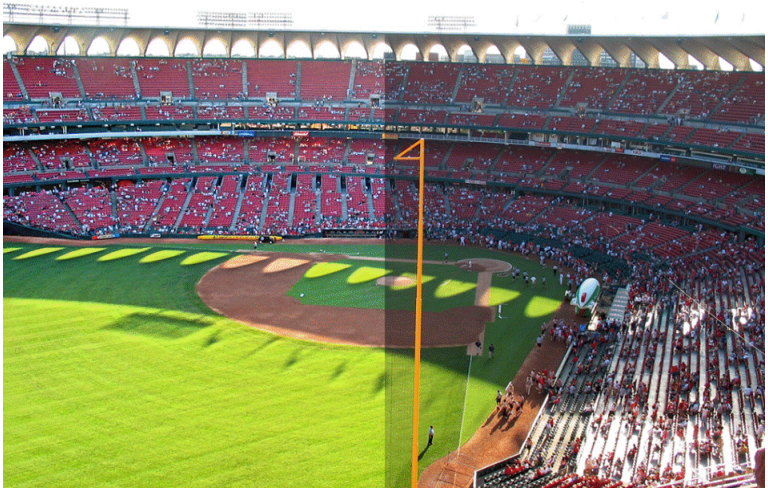

Figure 23. LABB enabled (left side) and LABB disabled (right side)

The LABB algorithm operates most effectively when ambient light conditions are used to help determine the decision about the strength of gains utilized. For this reason, it may be useful to include an ambient light sensor in the system design that is used to measure the display screen's reflected ambient light. This sensor can assist in dynamically controlling the LABB strength. Set the LABB gain higher for bright rooms to help overcome washed out images. Set the LABB gain lower in dark rooms to prevent overdriven pixel intensities in images.

7.3.7 3D Glasses Operation

When using 3D glasses (with 3D video input and appropriate software support), the controller outputs sync information to align the left eye and right eye shuttering in the glasses with the displayed DMD image frames. 3D glasses typically use either Infrared (IR) transmission or DLP Link ™technology to achieve this synchronization.

One glasses type uses an IR transmitter on the system PCB to send an IR sync signal to an IR receiver in the glasses. In this case DLPC34xx controller output signal GPIO_04 can be used to cause the IR transmitter to send an IR sync signal to the glasses. Figure 11 shows the timing sequence for the GPIO_04 signal.

The second type of glasses relies on sync information that is encoded into the light being output from the projection lens. This approach uses the DLP Link feature for 3D video. Many 3D glasses from different suppliers have been built using this method. The advantage of using the DLP Link feature is that it takes advantage of existing projector hardware to transmit the sync information to the glasses. This method may give an advantage in cost, size and power savings in the projector.

When using DLP Link technology, one light pulse per DMD frame is output from the projection lens while the glasses have both shutters closed. To achieve this, the DLPC34xx tells the DLPAxxxx when to turn on the illumination source (typically LEDs or lasers) so that an encoded light pulse is output once per DMD frame. Because the shutters in the glasses are both off when the pulse is sent, the projector illumination source is also off except when the light is sent to create the pulse. The pulses may use any color; however, due to the transmission property of the eye-glass LCD shutter lenses and the sensitivity of the white-light sensor used on the eye-glasses, it is highly recommended that blue is not used for pulses. Red pulses are the recommended color to use. Figure 24 shows 3D timing information. Figure 25 and Table 10 show the timing for the light pulses when using the DLP Link feature.

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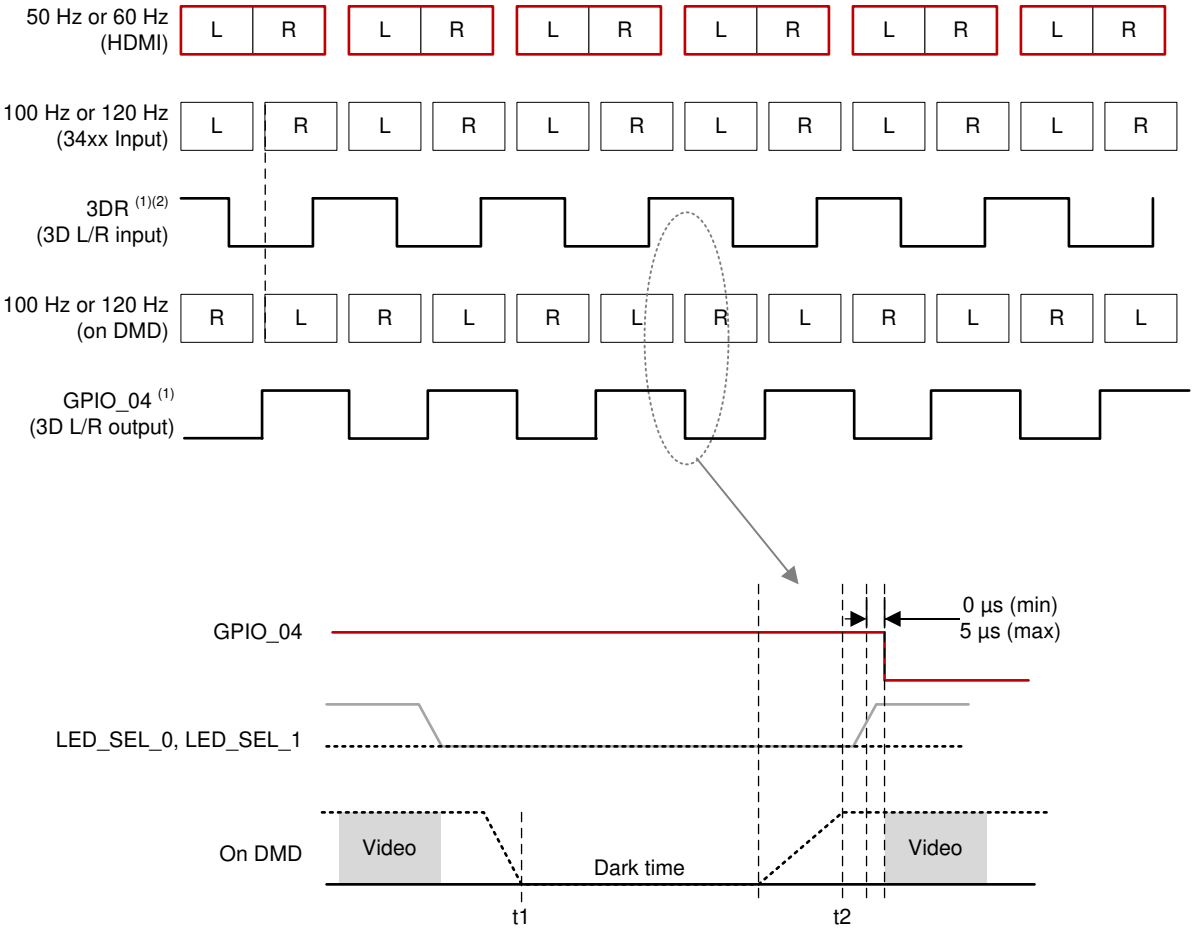


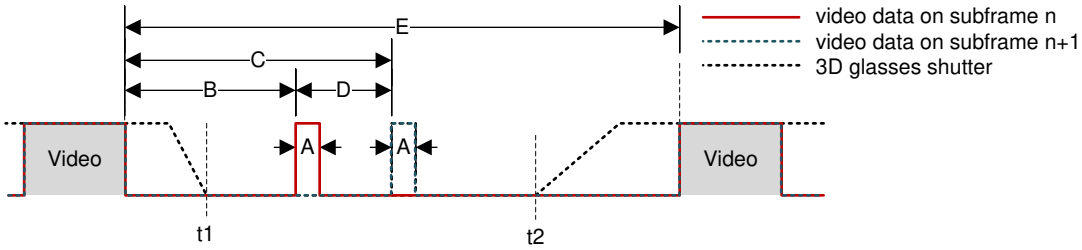
(1) Left = 1, Right = 0

(2) 3DR must toggle 1 ms before VSYNC

t1: both shutters turned off

t2: next shutter turned on

Figure 24. 3D Display Left and Right Frame and Signal Timing



The time offset of DLP Link pulses at the end of a subframe alternates between B and B+D where D is the delta offset.

Figure 25. 3D DLP Link Pulse Timing

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Table 10. 3D DLP Link Timing (1)

HDMI Source Frame Rate (Hz)	DLPC34xx Input Frame Rate (Hz)	A (µs)	B (µs)	C (µs)	D (µs)	E (µs)
49.0	98	20 - 32 (31.8 nominal)	>500	>622	128 - 163 (161.6 nominal)	>2000
50.0	100	20 - 32 (31.2 nominal)	>500	>658	128 - 163 (158.4 nominal)	>2000
51.0	102	20 - 32 (30.6 nominal)	>500	>655	128 - 163 (155.3 nominal)	>2000
59.0	118	20 - 32 (26.4 nominal)	>500	>634	128 - 163 (134.2 nominal)	>2000
60.0	120	20 - 32 (26.0 nominal)	>500	>632	128 - 163 (132.0 nominal)	>2000
61.0	122	20 - 32 (25.6 nominal)	>500	>630	128 - 163 (129.8 nominal)	>2000

(1) Timing parameter C is always the sum of B+D.

7.3.8 Test Point Support

The DLPC34xx test point output port, TSTPT_(7:0), provides selected system calibration and controller debug support. These test points are inputs when reset is applied. These test points are outputs when reset is released. The controller samples the signal state upon the release of system reset and then uses the captured value to configure the test mode until the next time reset is applied. Because each test point includes an internal pulldown resistor, external pullups must be used to modify the default test configuration.

The default configuration (b000) corresponds to the TSTPT_(2:0) outputs remaining tri-stated to reduce switching activity during normal operation. For maximum flexibility, a jumper to external pullup resistors is recommended for TSTPT_(2:0). The pullup resistors on TSTPT_(2:0) can be used to configure the controller for a specific mode or option. TI does not recommend adding pullup resistors to TSTPT_(7:3) due to potentially adverse effects on normal operation. For normal use TSTPT_(7:3) should be left unconnected. The test points are sampled only during a 0-to-1 transition on the RESETZ input, so changing the configuration after reset is released does not have any effect until the next time reset asserts and releases. Table 11 describes the test mode selections for one programmable scenario defined by TSTPT_(2:0).

Table 11. Test Mode Selection Scenario Defined by TSTPT_(2:0) (1)

TSTPT OUTPUT VALUE	NO SWITCHING ACTIVITY	CLOCK DEBUG OUTPUT
	TSTPT_(2:0) = 0b000	TSTPT_(2:0) = 0b010
TSTPT_0	HI-Z	60 MHz
TSTPT_1	HI-Z	30 MHz
TSTPT_2	HI-Z	0.7 to 22.5MHz
TSTPT_3	HI-Z	HIGH
TSTPT_4	HI-Z	LOW
TSTPT_5	HI-Z	HIGH
TSTPT_6	HI-Z	HIGH
TSTPT_7	HI-Z	7.5 MHz

(1) These are default output selections. Software can reprogram the selection at any time.

7.3.9 DMD Interface

The DLPC34xx controller DMD interface consists of one high-speed (HS), 1.8-V sub-LVDS, output-only interface and one low speed (LS), 1.8-V LVCMOS SDR interface with a typical fixed clock speed of 120 MHz.

7.3.9.1 Sub-LVDS (HS) Interface

The DLP2010 (.2 WVGA) DMD does not require all of the available output data lanes of the controller. Internal software selection allows the controller to support multiple DMD interface swap configurations. These options can improve board layout by remapping specific combinations of DMD interface lines to other DMD interface lines as needed. 表 12 shows the four options available for the DLP2010 DMD. Leave any unused DMD signal pairs unconnected on the final board design.

表 12. DLP2010 (.2 WVGA) DMD – Controller to 4-Lane DMD Pin Mapping Options

DLP2010 4-LANE DMD ROUTING OPTIONS				DMD PINS
OPTION 1	OPTION 2	OPTION 3	OPTION 4	
HS_WDATA_D_P HS_WDATA_D_N	HS_WDATA_E_P HS_WDATA_E_N	HS_WDATA_H_P HS_WDATA_H_N	HS_WDATA_A_P HS_WDATA_A_N	Input DATA_P_0 Input DATA_N_0
HS_WDATA_C_P HS_WDATA_C_N	HS_WDATA_F_P HS_WDATA_F_N	HS_WDATA_G_P HS_WDATA_G_N	HS_WDATA_B_P HS_WDATA_B_N	Input DATA_P_1 Input DATA_N_1
HS_WDATA_F_P HS_WDATA_F_N	HS_WDATA_C_P HS_WDATA_C_N	HS_WDATA_B_P HS_WDATA_B_N	HS_WDATA_G_P HS_WDATA_G_N	Input DATA_P_2 Input DATA_N_2
HS_WDATA_E_P HS_WDATA_E_N	HS_WDATA_D_P HS_WDATA_D_N	HS_WDATA_A_P HS_WDATA_A_N	HS_WDATA_H_P HS_WDATA_H_N	Input DATA_P_3 Input DATA_N_3

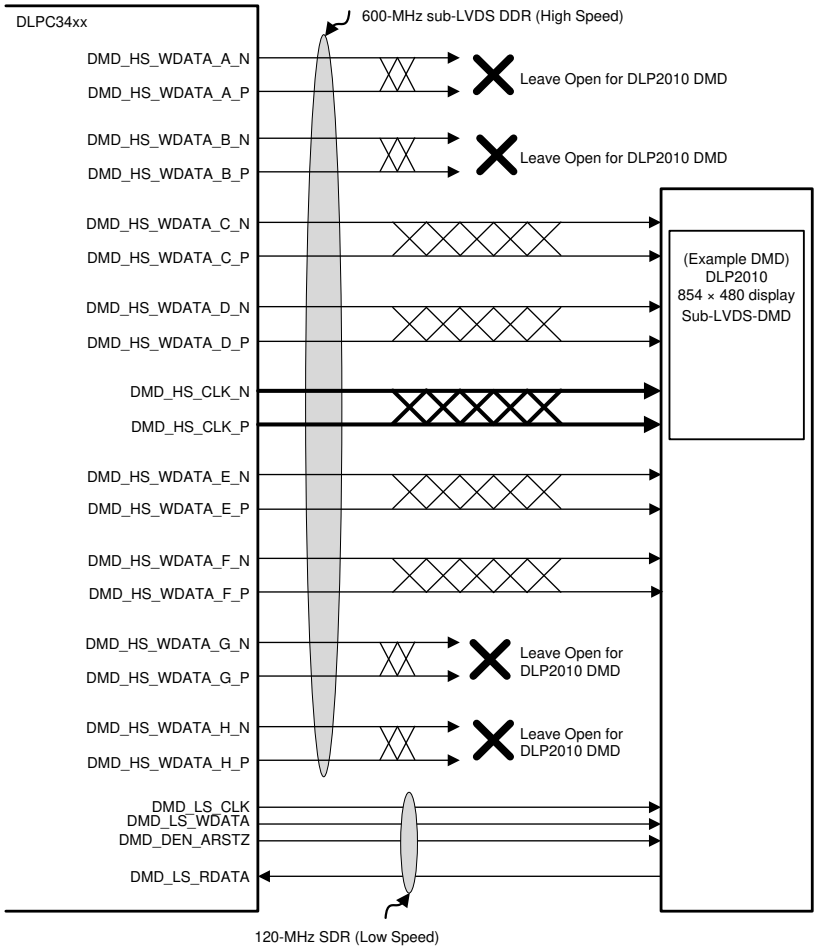

图 26. DLP2010 (.2 WVGA) DMD Interface Example (Option 1 and 2)

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The sub-LVDS high-speed interface waveform quality and timing on the DLPC34xx controller depends on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the *DMD Control and Sub-LVDS Signals* layout section is provided as a reference of an interconnect system that satisfy both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB signal integrity). Variation from these recommendations may also work, but should be confirmed with PCB signal integrity analysis or lab measurements.

7.4 Device Functional Modes

The DLPC34xx controller has two functional modes (ON and OFF) controlled by a single pin, PROJ_ON (GPIO_08).

- When the PROJ_ON pin is set high, the controller powers up and can be programmed to send data to the DMD.
- When the PROJ_ON pin is set low, the controller powers down and consumes minimal power.

7.5 Programming

The DLPC34xx controller contains an Arm® Cortex®-M3 processor with additional functional blocks to enable video processing and control. TI provides software as a firmware image. The customer is required to flash this firmware image onto the SPI flash memory. The DLPC34xx controller loads this firmware during startup and regular operation. The controller and its accompanying DLP chipset requires this proprietary software to operate. The available controller functions depend on the firmware version installed. Different firmware is required for different chipset combinations (such as when using different PMIC devices). Go to *Tools & Software* or contact TI to view or download the latest published software.

Users can modify software behavior through I^2C interface commands. For a list of commands, view the software user's guide accessible through the *Technical Documentation* links.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLPC34xx controller is used with the DLP2010 DMD to provide a reliable display solution for many data and video display applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into projection or collection optics. The optical architecture of the system and the format of the image digital data coming into the DLPC34xx are what primarily determine the application requirements.

Click these links to find more information about typical applications:

Mobile projector, Smart display, Smartphone, Tablet (multimedia), Augmented reality glasses, Smart home display, or Pico projector.

8.2 Typical Application

A common application when using the DLPC34xx controller with the DLP2010 DMD and the DLPAxxxx PMIC/LED driver is to create a pico projector embedded in a handheld product. For example, a pico projector may be embedded in a smartphone, a tablet, or a camera. The controller in the pico projector embedded module typically receives images from a host processor within the product.

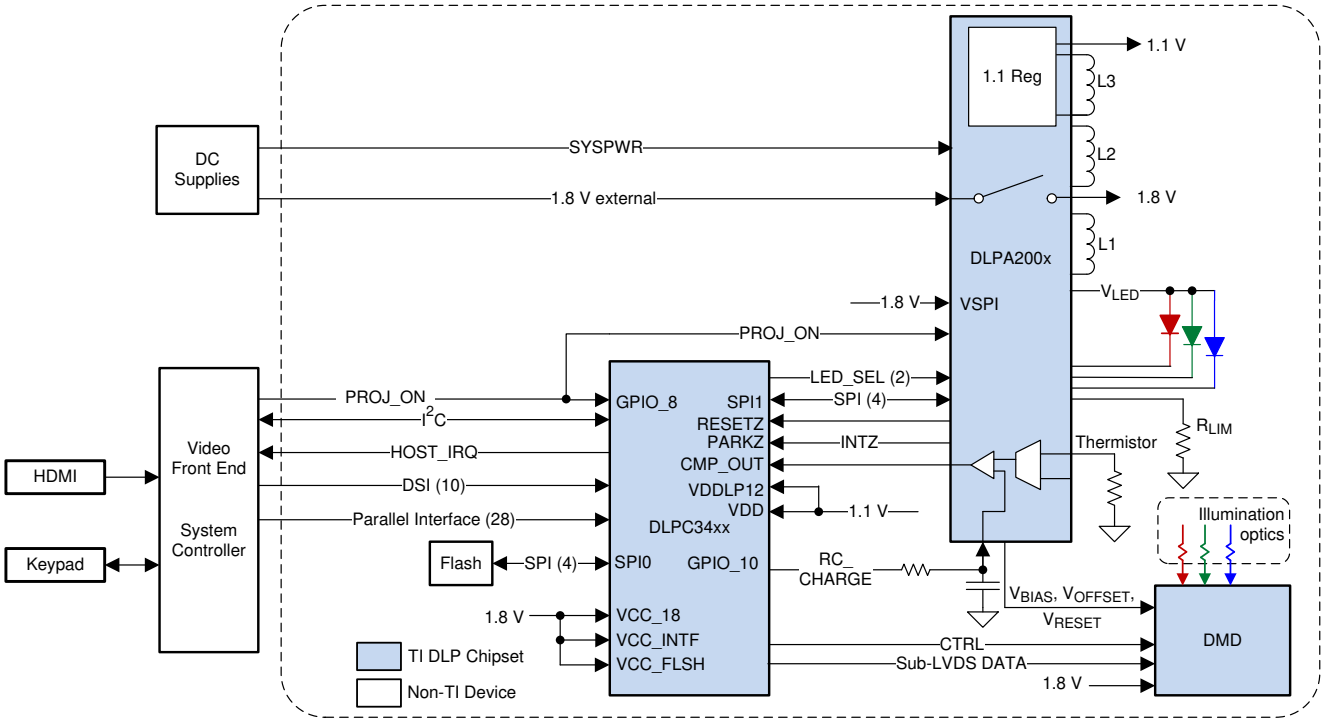

图 27. Typical Simplified Application Schematic

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Typical Application (接下页)

8.2.1 Design Requirements

A pico projector can be created by using the DLP chipset that includes the DLP2010 (.2 WVGA) DMD, the DLPC34xx controller, and the DLPAxxxx PMIC/LED driver. The DLPC34xx controller processes the digital images, the DLPAxxxx PMIC provides the analog functions for the chipset, and the DMD displays the image for projection.

In addition to the three DLP devices in the chipset, other components may be needed. At a minimum, a flash device is needed to store the firmware that controls the DLPC34xx controller.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These LEDs are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico projector.

To receive images, connect the DLPC34xx controller to the host processor using the parallel (or potentially DSI) interface. To send commands to the controller, connect it to the host processor using the I^2C interface.

The only required power supplies that are external to the projector system chipset are the battery (SYSPWR) and possibly a regulated 1.8-V supply (some TI PMICs generate the 1.8-V supply but the DLPA200x does not).

The entire projector chipset can be turned on and off by using a single signal called PROJ_ON. When PROJ_ON is high, the chipset turns on and can begin displaying images. When PROJ_ON is set low, the projector chipset turns off and draws just microamps of current on SYSPWR. If 1.8 V is supplied separately from the PMIC (as is the case with the DLPA200x), when PROJ_ON is set low, the 1.8 V supply can continue to be left at 1.8 V and used by other non-projector sections of the product.

8.2.2 Detailed Design Procedure

For connecting the DLP2010 (.2 WVGA) DMD, DLPC34xx controller, and DLPAxxxx PMIC, see the reference design schematic and board layout TIDA-00325. When a circuit board layout is created from this schematic, a small circuit board is possible. Follow the layout guidelines to design a reliable projector.

It is typical for an optical engine manufacturer to supply the optical engine that includes the LED packages and a mounted DMD. These manufacturers specialize in designing optics for DLP projectors. There exists production-ready optical modules, optical module manufacturers, and design houses.

8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is shown in 图 28. For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue LEDs. The shape of the curve depends on the LED devices used as well as the LED system-level heat sink implementation.

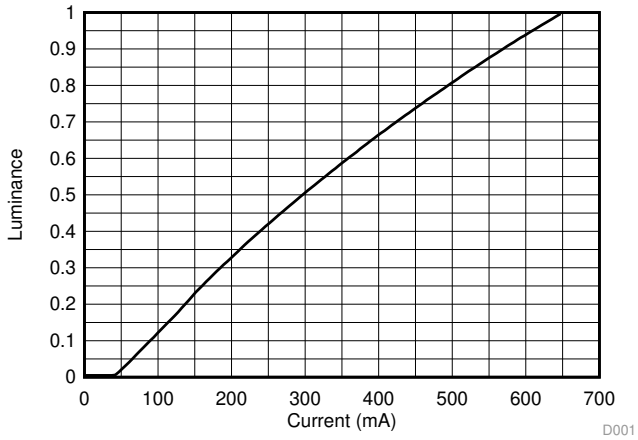

图 28. Typical Luminance vs Current

9 Power Supply Recommendations

9.1 PLL Design Considerations

It is acceptable for the VDD_PLLD and VDD_PLLM to be derived from the same regulator as the core VDD. However, to minimize the AC noise component, apply a filter as recommended in the *PLL Power Layout* section.

9.2 System Power-Up and Power-Down Sequence

Although the DLPC34xx controller requires an array of power supply voltage pins (for example, VDD, VDDLP12, VDD_PLLM/D, VCC18, VCC_FLSH, and VCC_INTF), if VDDLP12 is tied to the 1.1-V VDD supply (which is assumed to be the typical configuration), then there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC34xx controller (this remains true for both power-up and power-down scenarios). The controller requires no minimum delay time between powering-up and powering-down the individual supplies if the VDDLP12 is tied to the 1.1-V VDD supply.

However, if the VDDLP12 pin is not tied to the VDD supply, then the VDDLP12 pin must be powered-on only after the VDD supply is powered-on. And in a similar sequence, the VDDLP12 pin must be powered-off before the VDD supply is powered-off. If the VDDLP12 pin is not tied to VDD, then the VDDLP12 pin and VDD supply pins must be powered-on or powered-off within 100 ms of each other.

Although there is no risk of damaging the DLPC34xx controller when the above power sequencing rules are followed, these additional power sequencing recommendations must be considered to ensure proper system operation:

- To ensure that the DLPC34xx controller output signal states behave as expected, all controller I/O supplies are encouraged to remain applied while VDD core power is applied. If VDD core power is removed while the I/O supply (VCC_INTF) is applied, then the output signal states associated with the inactive I/O supply go to a high impedance state.
- Because additional power sequencing rules may exist for devices that share the supplies with the DLPC34xx controller (such as the PMIC and DMD), these devices may force additional system power sequencing requirements.

Figure 29, Figure 30, and Figure 31 show the DLPC34xx power-up sequence, the normal PARK power-down sequence, and the fast PARK power-down sequence of a typical DLPC34xx system.

When the VDD core power is applied, but I/O power is not applied, the controller may draw additional leakage current. This leakage current does not affect the normal DLPC34xx controller operation or reliability.

NOTE

During a Normal Park it is recommended to maintain SYSPWR within specification for at least 50 ms after PROJ_ON goes low. This is to allow the DMD to be parked and the power supply rails to safely power down. After 50 ms SYSPWR can be turned off. If a DLPA200x is used, it is also recommended that the 1.8-V supply fed into the DLPA200x load switch be maintained within specification for at least 50 ms after PROJ_ON goes low.

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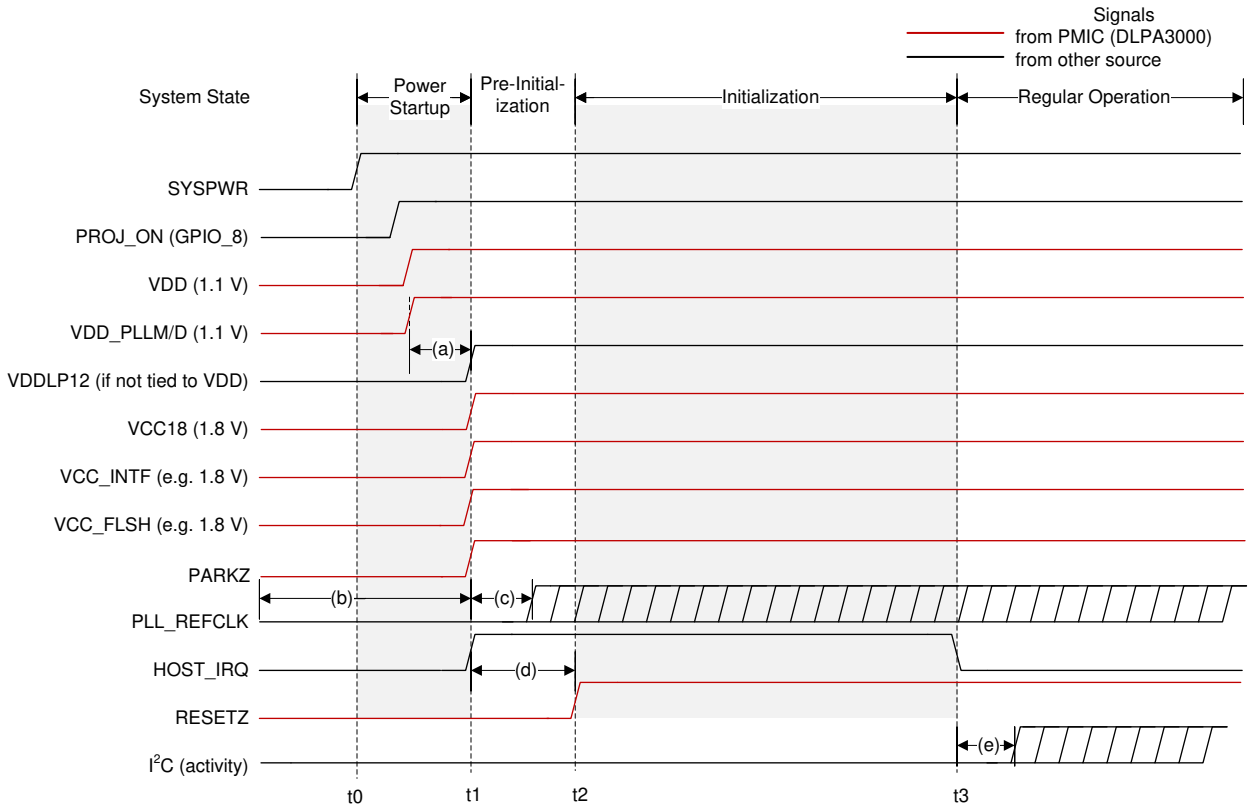
System Power-Up and Power-Down Sequence (continued)



t0: SYSPWR applied to the PMIC. All other voltage rails are derived from SYSPWR.

t1: All supplies reach 95% of their specified nominal value. Note HOST_IRQ may go high sooner if it is pulled-up to a different external supply.

t2: Point where RESETZ is deasserted (goes high). This indicates the beginning of the controller auto-initialization routine.

t3: HOST_IRQ goes low to indicate initialization is complete.

(a): VDDLP12 must be powered on after VDD if it is supplied from a separate source.

(b): PLL_REFCLK is allowed to be active before power is applied.

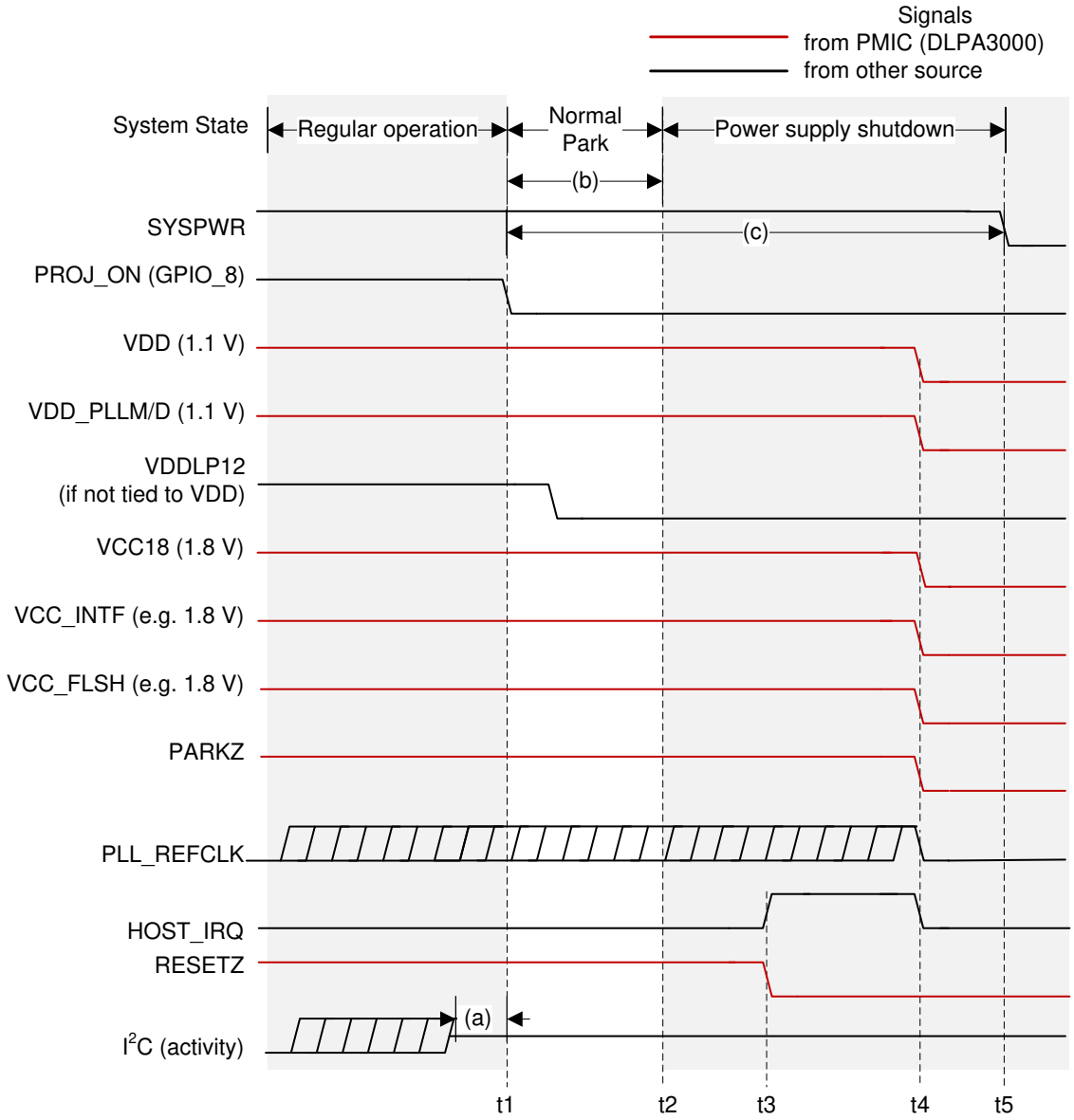
(c): PLL_REFCLK must be stable within 5 ms of all power being applied. For external oscillator applications this is oscillator dependent, and for crystal applications this is crystal and controller oscillator cell dependent.

(d) : PARKZ must be high before RESETZ releases to support auto-initialization. RESETZ must also be held low for at least 5 ms after the power supplies are in specification.

(e): I^2C activity cannot start until HOST_IRQ goes low to indicate auto-initialization completes.

Figure 29. System Power-Up Waveforms (with DLPA3000)

System Power-Up and Power-Down Sequence (continued)



t1: PROJ_ON goes low to begin the power down sequence.

t2: The controller finishes parking the DMD.

t3: RESETZ is asserted which causes HOST_IRQ to be pulled high.

t4: All controller power supplies are turned off.

t5: SYSPWR is removed now that all other supplies are turned off.

(a): I^2C activity must stop before PROJ_ON is deasserted (goes low).

(b): The DMD will be parked within 20 ms of PROJ_ON being deasserted (going low). VDD, VDD_PLLM/D, VCC18, VCC_INITF, and VCC_FLSH power supplies and the PLL_REFCLK must be held within specification for a minimum of 20 ms after PROJ_ON is deasserted (goes low). However, 20 ms does not satisfy the typical shutdown timing of the entire chipset. It is therefore recommended to follow note (c).

(c): It is recommended that SYSPWR not be turned off for 50 ms after PROJ_ON is deasserted (goes low). This time allows the DMD to be parked, the controller to turn off, and the PMIC supplies to shut down.

Figure 30. Normal Park Power-Down Waveforms

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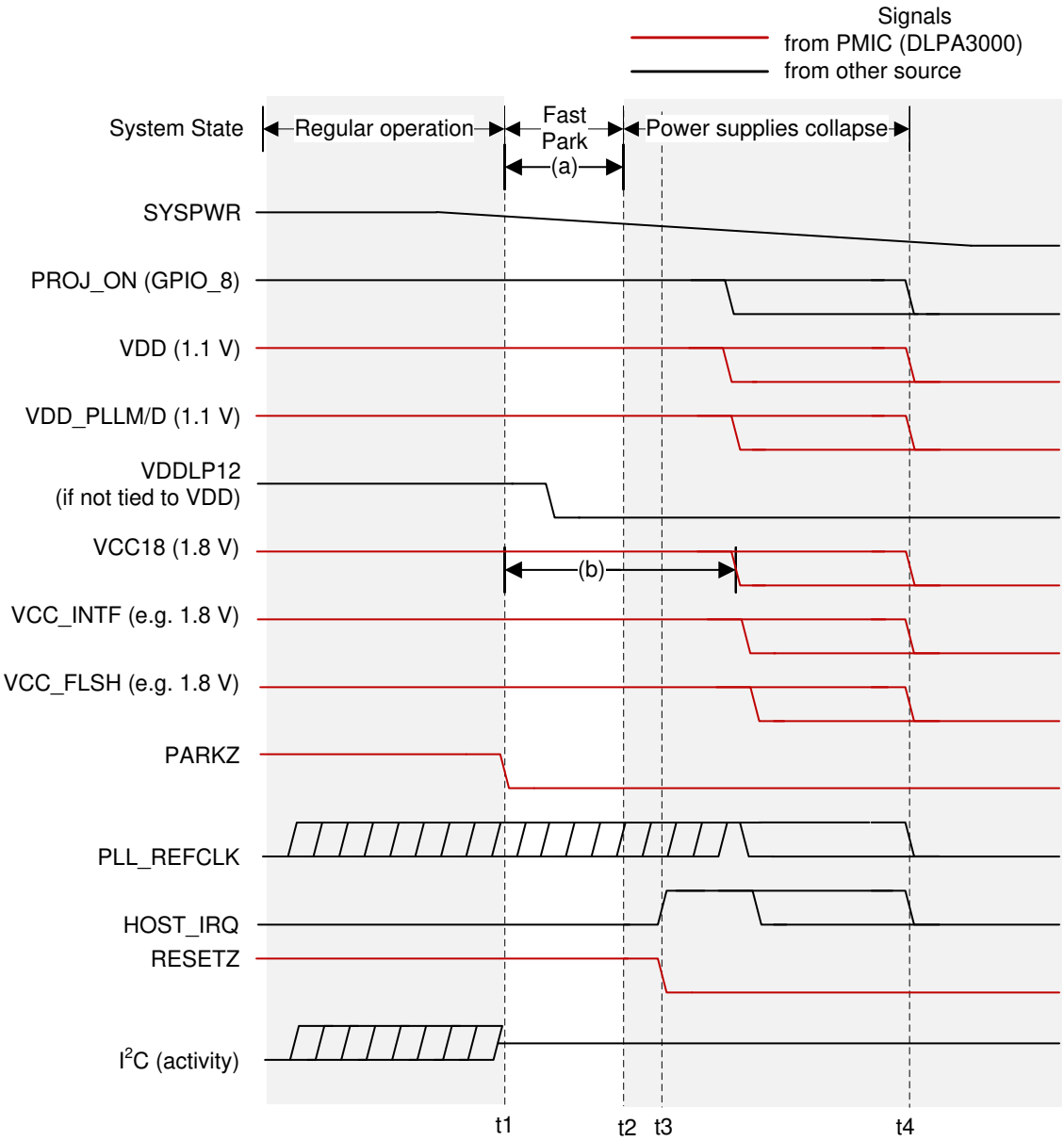
System Power-Up and Power-Down Sequence (continued)



t1: A fault is detected (in this example the PMIC detects a UVLO condition) and PARKZ is asserted (goes low) to tell the controller to initiate a fast park of the DMD.

t2: The controller finishes the fast park procedure.

t3: RESETZ is asserted which puts the controller in a reset state which causes HOST_IRQ to be pulled high.

t4: Eventually all power supplies that were derived from SYSPWR collapse.

(a): VDD, VDD_PLLM/D, VCC18, VCC_INITF, and VCC_FLSH power supplies and the PLL_REFCLK must be held within specification for a minimum of 32 µs after PARKZ is asserted (goes low).

(b): VCC18 must remain in specification long enough to satisfy DMD power sequencing requirements defined in the DMD datasheet. Also see the DLPAxxxx datasheets for more information.

Figure 31. Fast Park Power-Down Waveforms

9.3 Power-Up Initialization Sequence

An external power monitor is required to hold the DLPC34xx controller in system reset during the power-up sequence by driving RESETZ to a logic-low state. It shall continue to drive RESETZ low until all controller voltages reach the minimum specified voltage levels, PARKZ goes high, and the input clocks are stable. The external power monitoring is automatically done by the DLPAxxxx PMIC.

No signals output by the DLPC34xx controller will be in their active state while RESETZ is asserted. The following signals are tri-stated while RESETZ is asserted:

- SPI0_CLK
- SPI0_DOUT
- SPI0_CSZ0
- SPI0_CSZ1
- GPIO [19:00]

Add external pullup (or pulldown) resistors to all tri-stated output signals (including bidirectional signals to be configured as outputs) to avoid floating controller outputs during reset if they are connected to devices on the PCB that can malfunction. For SPI, at a minimum, include a pullup to any chip selects connected to devices. Unused bidirectional signals can be configured as outputs in order to avoid floating controller inputs after RESETZ is set high.

The following signals are forced to a logic low state while RESETZ is asserted and the corresponding I/O power is applied:

- LED_SEL_0
- LED_SEL_1
- DMD_DEN_ARSTZ

After power is stable and the PLL_REFCLK_I clock input to the DLPC34xx controller is stable, then RESETZ should be deactivated (set to a logic high). The DLPC34xx controller then performs a power-up initialization routine that first locks its PLL followed by loading self configuration data from the external flash. Upon release of RESETZ, all DLPC34xx I/Os will become active. Immediately following the release of RESETZ, the HOST_IRQ signal will be driven high to indicate that the auto initialization routine is in progress. However, since a pullup resistor is connected to signal HOST_IRQ, this signal will have already gone high before the controller actively drives it high. Upon completion of the auto-initialization routine, the DLPC34xx controller will drive HOST_IRQ low to indicate the initialization done state of the controller has been reached.

NOTE

No I^2C or DSI activity is permitted until HOST_IRQ goes low.

9.4 DMD Fast Park Control (PARKZ)

PARKZ is an input early warning signal that must alert the controller at least 32 µs before DC supply voltages drop below specifications. Typically, the PARKZ signal is provided by the DLPAxxxx interrupt output signal. PARKZ must be deasserted (set high) prior to releasing RESETZ (that is, prior to the low-to-high transition on the RESETZ input) for normal operation. When PARKZ is asserted (set low) the controller performs a Fast Park operation on the DMD which assists in maintaining the lifetime of the DMD. The reference clock must continue running and RESETZ must remain deactivated for at least 32 µs after PARKZ has been asserted (set low) to allow the park operation to complete.

Fast Park operation is only intended for use when loss of power is imminent and beyond the control of the host processor (for example, when the external power source has been disconnected or the battery has dropped below a minimum level). The longest lifetime of the DMD may not be achieved with Fast Park operation. The longest lifetime is achieved with a Normal Park operation (initiated through GPIO_08). Hence, PARKZ is typically only used instead of a Normal Park request if there is not enough time for a Normal Park. A Normal Park operation takes much longer than 32 µs to park the mirrors. During a Normal Park operation, the DLPAxxxx keeps on all power supplies, and keeps RESETZ high, until the longer mirror parking has completed. Additionally, the DLPAxxxx may hold the supplies on for a period of time after the parking has been completed. View the relevant DLPAxxxx datasheet for more information. The longer mirror parking time ensures the longest DMD lifetime and reliability. *DMD Parking Switching Characteristics* specifies the park timings.

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9.5 Hot Plug I/O Usage

The DLPC34xx controller provides fail-safe I/O on all host interface signals (signals powered by VCC_INTF). This allows these inputs to externally be driven even when no I/O power is applied. Under this condition, the controller does not load the input signal nor draw excessive current that could degrade controller reliability. For example, the I^2C bus from the host to other components is not affected by powering off VCC_INTF to the DLPC34xx controller. The allows additional devices on the I^2C bus to be utilized even if the controller is not powered on. TI recommends weak pullup or pulldown resistors to avoid floating inputs for signals that feed back to the host.

If the I/O supply (VCC_INTF) powers off, but the core supply (VDD) remains on, then the corresponding input buffer may experience added leakage current; however, the added leakage current does not damage the DLPC34xx controller.

However, if VCC_INTF is powered and VDD is not powered, the controller may drives the IIC0_xx pins low which prevents communication on this I^2C bus. Do not power up the VCC_INTF pin before powering up the VDD pin for any system that has additional slave devices on this bus.

10 Layout

10.1 Layout Guidelines

For a summary of the PCB design requirements for the DLPC34xx controller see *PCB Design Requirements for TI DLP Pico TRP Digital Micromirror Devices*. Some applications (such as high frame rate video) may require the use of 1-oz (or greater) copper planes to manage the controller package heat.

10.1.1 PLL Power Layout

Follow these recommended guidelines to achieve acceptable controller performance for the internal PLL. The DLPC34xx controller contains two internal PLLs which have dedicated analog supplies (VDD_PLLM, VSS_PLLM, VDD_PLLD, and VSS_PLLD). At a minimum, isolate the VDD_PLLx power and VSS_PLLx ground pins using a simple passive filter consisting of two series ferrite beads and two shunt capacitors (to widen the spectrum of noise absorption). It's recommended that one capacitor be 0.1-µF and one be 0.01-µF. Place all four components as close to the controller as possible. It's especially important to keep the leads of the high frequency capacitors as short as possible. Connect both capacitors from VDD_PLLM to VSS_PLLM and VDD_PLLD to VSS_PLLD on the controller side of the ferrite beads.

Select ferrite beads with these characteristics:

- DC resistance less than 0.40 Ω
- Impedance at 10 MHz equal to or greater than 180 Ω
- Impedance at 100 MHz equal to or greater than 600 Ω

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, VDD_PLLM and VDD_PLLD must be a single trace from the DLPC34xx controller to both capacitors and then through the series ferrites to the power source. Make the power and ground traces as short as possible, parallel to each other, and as close as possible to each other.

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Layout Guidelines (continued)

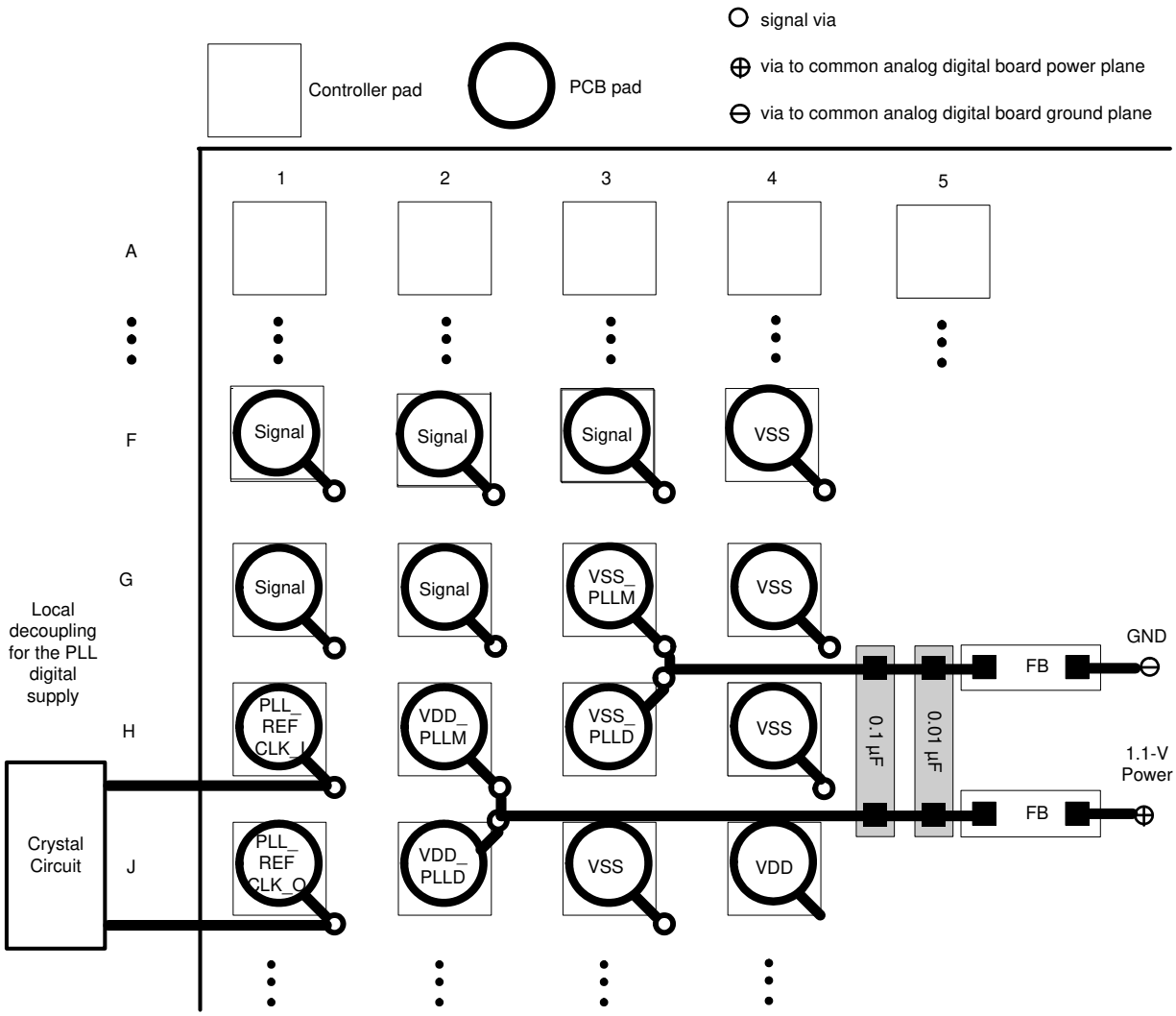


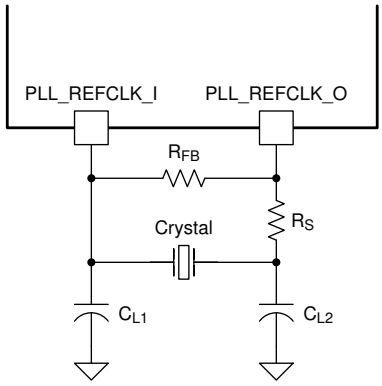
Figure 32. PLL Filter Layout

10.1.2 Reference Clock Layout

The DLPC34xx controller requires an external reference clock to feed the internal PLL. Use either a crystal or oscillator to supply this reference. The DLPC34xx reference clock must not exceed a frequency variation of ±200 ppm (including aging, temperature, and trim component variation).

Figure 33 shows the required discrete components when using a crystal.

Layout Guidelines (continued)



C_L = Crystal load capacitance (farads)

$C_{L1} = 2 \times (C_L – Cstray_pll_refclk_i)$

$C_{L2} = 2 \times (C_L – Cstray_pll_refclk_o)$

where:

- Cstray_pll_refclk_i = Sum of package and PCB stray capacitance at the crystal pin associated with the controller pin pll_refclk_i.
- Cstray_pll_refclk_o = Sum of package and PCB stray capacitance at the crystal pin associated with the controller pin pll_refclk_o.

Figure 33. Required Discrete Components

10.1.2.1 Recommended Crystal Oscillator Configuration

Table 13. Crystal Port Characteristics

PARAMETER	NOM	UNIT
PLL_REFCLK_I TO GND capacitance	1.5	pF
PLL_REFCLK_O TO GND capacitance	1.5	pF

Table 14. Recommended Crystal Configuration (1) (2)

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	24	MHz
Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity)	±200	PPM
Maximum startup time	1.0	ms
Crystal equivalent series resistance (ESR)	120 (max)	Ω
Crystal load	6	pF
R_S drive resistor (nominal)	100	Ω
R_{FB} feedback resistor (nominal)	1	MΩ
C_{L1} external crystal load capacitor	See equation in Figure 33 notes	pF
C_{L2} external crystal load capacitor	See equation in Figure 33 notes	pF
PCB layout	A ground isolation ring around the crystal is recommended	

(1) Temperature range of –30°C to 85°C
(2) The crystal bias is determined by the controllers VCC_INTF voltage rail, which is variable (not the VCC18 rail).

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If an external oscillator is used, then the oscillator output must drive the PLL_REFCLK_I pin on the DLPC34xx controller, and the PLL_REFCLK_O pin must be left unconnected.

Table 15. Recommended Crystal Parts(1)(2)

MANUFACTURER	PART NUMBER	SPEED (MHz)	TEMPERATURE AND AGING (ppm)	MAXIMUM ESR (Ω)	LOAD CAPACITANCE (pF)	PACKAGE DIMENSIONS (mm)
KDS	DSX211G-24.000M-8pF-50-50	24	±50	120	8	2.0 × 1.6
Murata	XRCGB24M000F0L11R0	24	±100	120	6	2.0 × 1.6
NDK	NX2016SA 24M EXS00A-CS05733	24	±145	120	6	2.0 × 1.6

(1) The crystal devices in this table have been validated to work with the DLPC34xx controller. Other devices may also be compatible but have not necessarily been validated by TI.
(2) Operating temperature range: –30°C to 85°C for all crystals

10.1.3 DSI Interface Layout

Follow these PCB layout guidelines for the DSI LVDS interface to ensure proper DSI operation.

- Route the differential clock and data lines to match 50-Ω single-ended and 100-Ω differential impedance.
- The length of dp and dn should be matched. If that is not possible, ensure that dp is only slightly longer than dn (delta delay not to exceed 8-10 ps), especially for the clock-lane. This is to prevent propagation on the clock lane during the HS to LP transition.
- No thru-hole vias permitted on high-speed traces.
- Create trace routes on top or bottom layers preferably.
- Must have a ground reference plane.
- Avoid power plane transitions in upper or lower layers.
- Avoid using SMD (surface mount device) resistors larger than 0402. If resistors are used in the traces, ensure that the layer below has a void.
- No thru-hole SMA (SubMiniature version A) connectors.
- Minimize trace length as much as possible.
- Perform signal integrity simulations to ensure board performance.

10.1.4 Unused Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends tying unused controller input pins through a pullup resistor to its associated power supply or a pulldown resistor to ground. For controller inputs with internal pullup or pulldown resistors, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Note that internal pullup and pulldown resistors are weak and should not be expected to drive an external device. The DLPC34xx controller implements very few internal resistors and these are listed in the *Pin Configuration and Functions* table. When external pullup or pulldown resistors are needed for pins that have weak pullup or pulldown resistors, choose a maximum resistance of 8 kΩ.

Never tie unused output-only pins directly to power or ground. Leave them open.

When possible, TI recommends that unused bidirectional I/O pins are configured to their output state such that the pin can remain open. If this control is not available and the pins may become an input, then include an appropriate pullup (or pulldown) resistor.

10.1.5 DMD Control and Sub-LVDS Signals

Table 16. Maximum Pin-to-Pin PCB Interconnect Recommendations(1)(2)

DMD BUS SIGNAL	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE-BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HS_CLK_P DMD_HS_CLK_N	6.0 (152.4)	See (3)	inch (mm)
DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	6.0 (152.4)	See (3)	inch (mm)
DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD_LS_CLK	6.5 (165.1)	See (3)	inch (mm)
DMD_LS_WDATA	6.5 (165.1)	See (3)	inch (mm)
DMD_LS_RDATA	6.5 (165.1)	See (3)	inch (mm)
DMD_DEN_ARSTZ	7.0 (177.8)	See (3)	inch (mm)

(1) Maximum signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.
(3) Due to PCB variations, these recommendations cannot be defined. Any board design should SPICE simulate with the controller IBIS model (found under the *Tools & Software* tab of the controller web page) to ensure routing lengths do not violate signal requirements.

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Table 17. High Speed PCB Signal Routing Matching Requirements (1) (2) (3)

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH (4)	UNIT
DMD (5)	DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	DMD_HS_CLK_P DMD_HS_CLK_N	±1.0 (±25.4)	inch (mm)
	DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
	DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
	DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
	DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
	DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
	DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
	DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD	DMD_HS_WDATA_x_P	DMD_HS_WDATA_x_N	±0.025 (±0.635)	inch (mm)
DMD	DMD_HS_CLK_P	DMD_HS_CLK_N	±0.025 (±0.635)	inch (mm)
DMD	DMD_LS_WDATA DMD_LS_RDATA	DMD_LS_CLK	±0.2 (±5.08)	inch (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	inch (mm)

(1) The length matching values apply to PCB routing lengths only. Internal package routing mismatch associated with the DLPC34xx controller or the DMD require no additional consideration.
(2) Training is applied to DMD HS data lines. This is why the defined matching requirements are slightly relaxed compared to the LS data lines.
(3) DMD LS signals are single ended.
(4) Mismatch variance for a signal group is always with respect to the reference signal.
(5) DMD HS data lines are differential, thus these specifications are pair-to-pair.

Table 18. Signal Requirements

PARAMETER	REFERENCE	REQUIREMENT
Source series termination	DMD_LS_WDATA	Required
	DMD_LS_CLK	Required
	DMD_DEN_ARSTZ	Acceptable
	DMD_LS_RDATA	Required
	DMD_HS_WDATA_x_y	Not acceptable
	DMD_HS_CLK_y	Not acceptable
Endpoint termination	DMD_LS_WDATA	Not acceptable
	DMD_LS_CLK	Not acceptable
	DMD_DEN_ARSTZ	Not acceptable
	DMD_LS_RDATA	Not acceptable
	DMD_HS_WDATA_x_y	Not acceptable
	DMD_HS_CLK_y	Not acceptable
PCB impedance	DMD_LS_WDATA	68 Ω ±10%
	DMD_LS_CLK	68 Ω ± 10%
	DMD_DEN_ARSTZ	68 Ω ±10%
	DMD_LS_RDATA	68 Ω ±10%
	DMD_HS_WDATA_x_y	100 Ω ±10%
	DMD_HS_CLK_y	100 Ω ±10%

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Table 18. Signal Requirements (continued)

PARAMETER	REFERENCE	REQUIREMENT
Signal type	DMD_LS_WDATA	SDR (single data rate) referenced to DMD_LS_DCLK
	DMD_LS_CLK	SDR referenced to DMD_LS_DCLK
	DMD_DEN_ARSTZ	SDR
	DMD_LS_RDATA	SDR referenced to DMD_LS_DLCK
	DMD_HS_WDATA_x_y	sub-LVDS
	DMD_HS_CLK_y	sub-LVDS

10.1.6 Layer Changes

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers. Ideally ensure that the signals of a given pair do not change layers.

10.1.7 Stubs

- Avoid using stubs.

10.1.8 Terminations

- DMD_HS differential signals require no external termination resistors.
- Make sure the DMD_LS_CLK and DMD_LS_WDATA signal paths include a 43-Ω series termination resistor located as close as possible to the corresponding controller pins.
- Make sure the DMD_LS_RDATA signal path includes a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.
- The DMD_DEN_ARSTZ pin requires no series resistor.

10.1.9 Routing Vias

- The number of vias on DMD_HS signals must be minimized and ideally not exceed two.
- Any and all vias on DMD_HS signals must be located as close to the controller as possible.
- The number of vias on the DMD_LS_CLK and DMD_LS_WDATA signals must be minimized and ideally not exceed two.
- Any and all vias on the DMD_LS_CLK and DMD_LS_WDATA signals must be located as close to the controller as possible.

10.1.10 Thermal Considerations

The underlying thermal limitation for the DLPC34xx controller is that the maximum operating junction temperature (T_J) not be exceeded (this is defined in *Recommended Operating Conditions*).

Some factors that influence T_J are as follows:

- operating ambient temperature
- airflow
- PCB design (including the component layout density and the amount of copper used)
- power dissipation of the DLPC34xx controller
- power dissipation of surrounding components.

The controller package is designed to primarily extract heat through the power and ground planes of the PCB. Thus, copper content and airflow over the PCB are important factors.

The recommends maximum operating ambient temperature (T_A) is provided primarily as a design target and is based on maximum DLPC34xx controller power dissipation and $R_{\theta JA}$ at 0 m/s of forced airflow, where $R_{\theta JA}$ is the thermal resistance of the package as measured using a glater test PCB with two, 1-oz power planes. This JEDEC test PCB is not necessarily representative of the DLPC34xx controller PCB, so the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance. TI highly recommended that thermal performance be measured and validated after the PCB is designed and the application is built.

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To evaluate the thermal performance, measure the top center case temperature under the worse case product scenario (maximum power dissipation, maximum voltage, maximum ambient temperature), and validate the controller does not exceed the maximum recommended case temperature (T_C). This specification is based on the measured φ_{JT} for the DLPC34xx controller package and provides a relatively accurate correlation to junction temperature.

Take care when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approximately 40 gauge) thermocouple. Place the bead and thermocouple wire so that they contact the top of the package. Cover the bead and thermocouple wire with a minimal amount of thermally conductive epoxy. Route the wires closely along the package and the board surface to avoid cooling the bead through the wires.

10.2 Layout Example

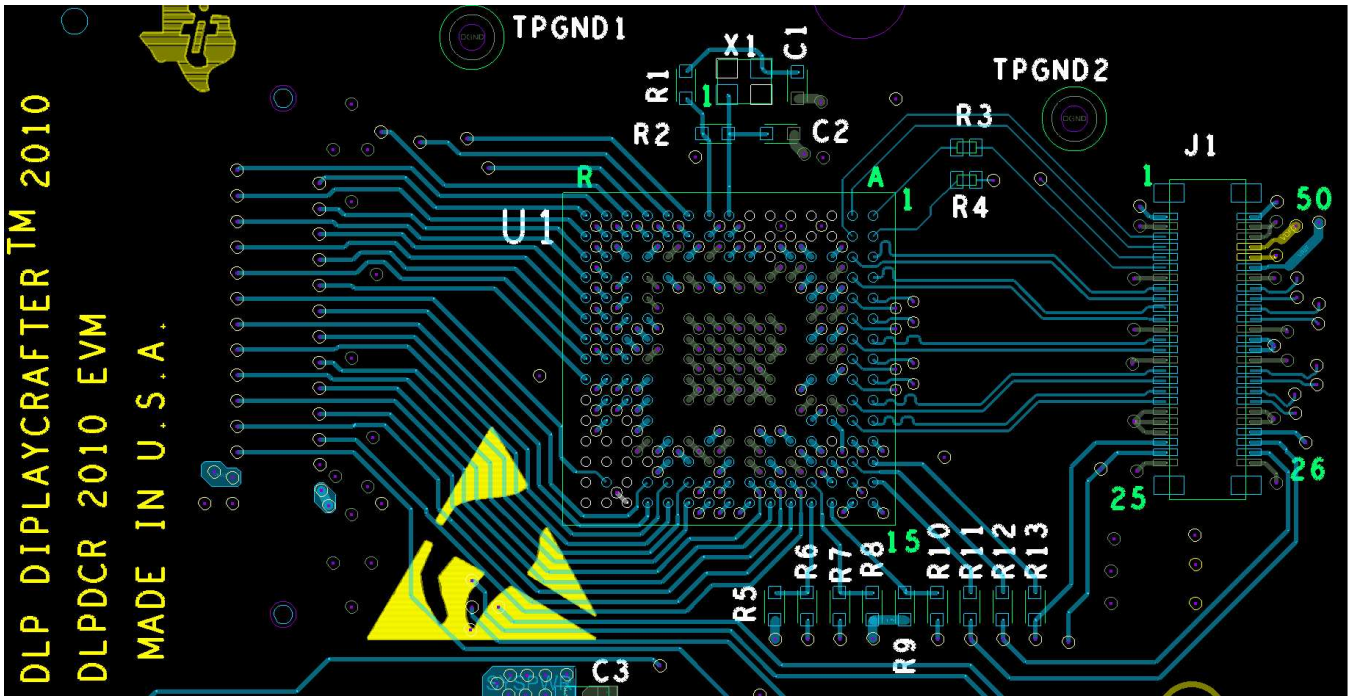


图 34. Layout Recommendation

11 器件和文档支持

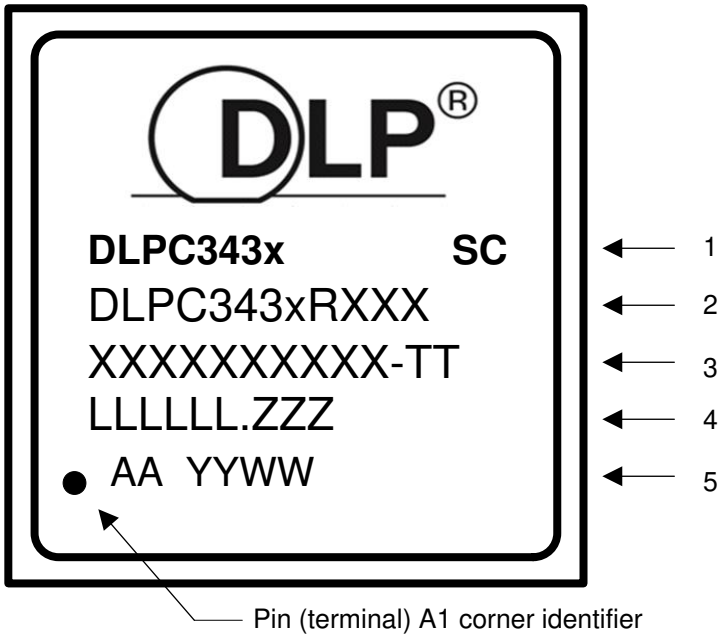
11.1 器件支持

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.1.2 器件命名规则

11.1.2.1 器件标记



标记定义：

第 1 行： DLP® 器件名称：DLPC343x = x 代表器件名称 ID 0 或 5。
SC：焊球成分
e1：表示含有 SnAgCu 的无铅焊球
G8：表示含有锡-银-铜 (SnAgCu) 的无铅焊球，其中银含量不超过 1.5%，且模压混合物符合 TI 的“绿色环保”定义。

第 2 行： TI 器件编号
DLP® 器件名称：DLPC343x = **x** 代表器件名称 ID 0 或 5。
R 表示 TI 器件版本字母，例如 A、B 或 C。
XXX 表示器件封装标识符。

第 3 行： XXXXXXXXXX-TT 制造商器件号

第 4 行： LLLLLLLL.ZZZ 半导体晶圆的铸造批次代码以及无铅焊锡球标记
LLLLLLLL：制造批次号码
ZZZ：分离批次号码

第 5 行： AA YYWW：封装组件信息
AA 代表制造工厂
YYWW：日期代码（YY = 年 :: WW = 周）

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器件支持 (continued)

注

1. 工程原型样品则在 TI 器件号之后加 **X** 后缀表示。例如：2512737-0001X。
2. 有关 DLPC34xx 控制器支持的输入分辨率，请参阅Table 4。

11.1.2.2 视频时序参数定义

See Figure 35 for a visual description below definitions.

Active Lines Per Frame (ALPF) Defines the number of lines in a frame containing displayable data. ALPF is a subset of the TLPF.

Active Pixels Per Line (APPL) Defines the number of pixel clocks in a line containing displayable data. APPL is a subset of the TPPL.

Horizontal Back Porch (HBP) Blanking Defines the number of blank pixel clocks after the active edge of horizontal sync but before the first active pixel.

Horizontal Front Porch (HFP) Blanking Defines the number of blank pixel clocks after the last active pixel but before horizontal sync.

Horizontal Sync (HS or Hsync) Timing reference point that defines the start of each horizontal interval (line). The active edge of the HS signal defines the absolute reference point. The active edge (either rising or falling edge as defined by the source) is the reference from which all horizontal blanking parameters are measured.

Total Lines Per Frame (TLPF) Total number of active and inactive lines per frame; defines the vertical period (or frame time).

Total Pixel Per Line (TPPL) Total number of active and inactive pixel clocks per line; defines the horizontal line period in pixel clocks.

Vertical Sync (VS or Vsync) Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all vertical blanking parameters are measured.

Vertical Back Porch (VBP) Blanking Defines the number of blank lines after the active edge of vertical sync but before the first active line.

Vertical Front Porch (VFP) Blanking Defines the number of blank lines after the last active line but before the active edge of vertical sync.

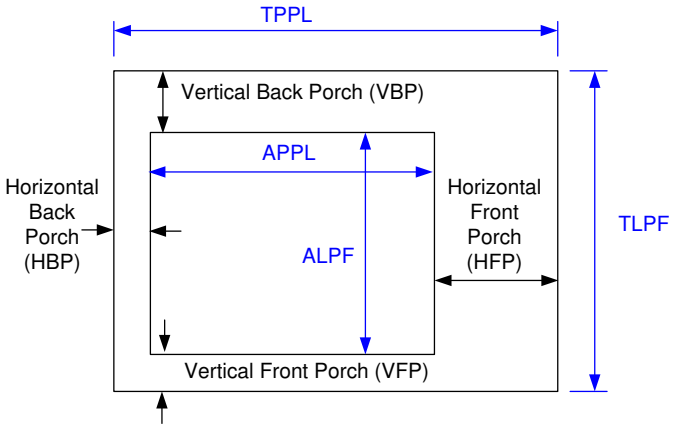

Figure 35. Parameter Definitions

11.2 文档支持

11.2.1 相关文档

下表列出了 DLP 芯片组相关器件的快速访问链接。

表 **19.** 芯片组文档

器件	产品文件夹	样片与购买	技术文档	工具与软件
DLPA2000	单击此处	单击此处	单击此处	单击此处
DLPA2005	单击此处	单击此处	单击此处	单击此处
DLPA3000	单击此处	单击此处	单击此处	单击此处
DLP2010	单击此处	单击此处	单击此处	单击此处

11.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **20.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
DLPC3430	单击此处	单击此处	单击此处	单击此处	单击此处
DLPC3435	单击此处	单击此处	单击此处	单击此处	单击此处

11.4 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.5 社区资源

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.7 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(4)(5)
DLPC3430CZVBR	ACTIVE	NFBGA	ZVB	176	3000	TBD	Call TI	Level-3-260C-168 HR	-30 to 85	
DLPC3435CZEZ	ACTIVE	NFBGA	ZEZ	201	160	TBD	Call TI	Level-3-260C-168 HR	-30 to 85	
DLPC3435ZEZ	NRND	NFBGA	ZEZ	201	160	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-30 to 85	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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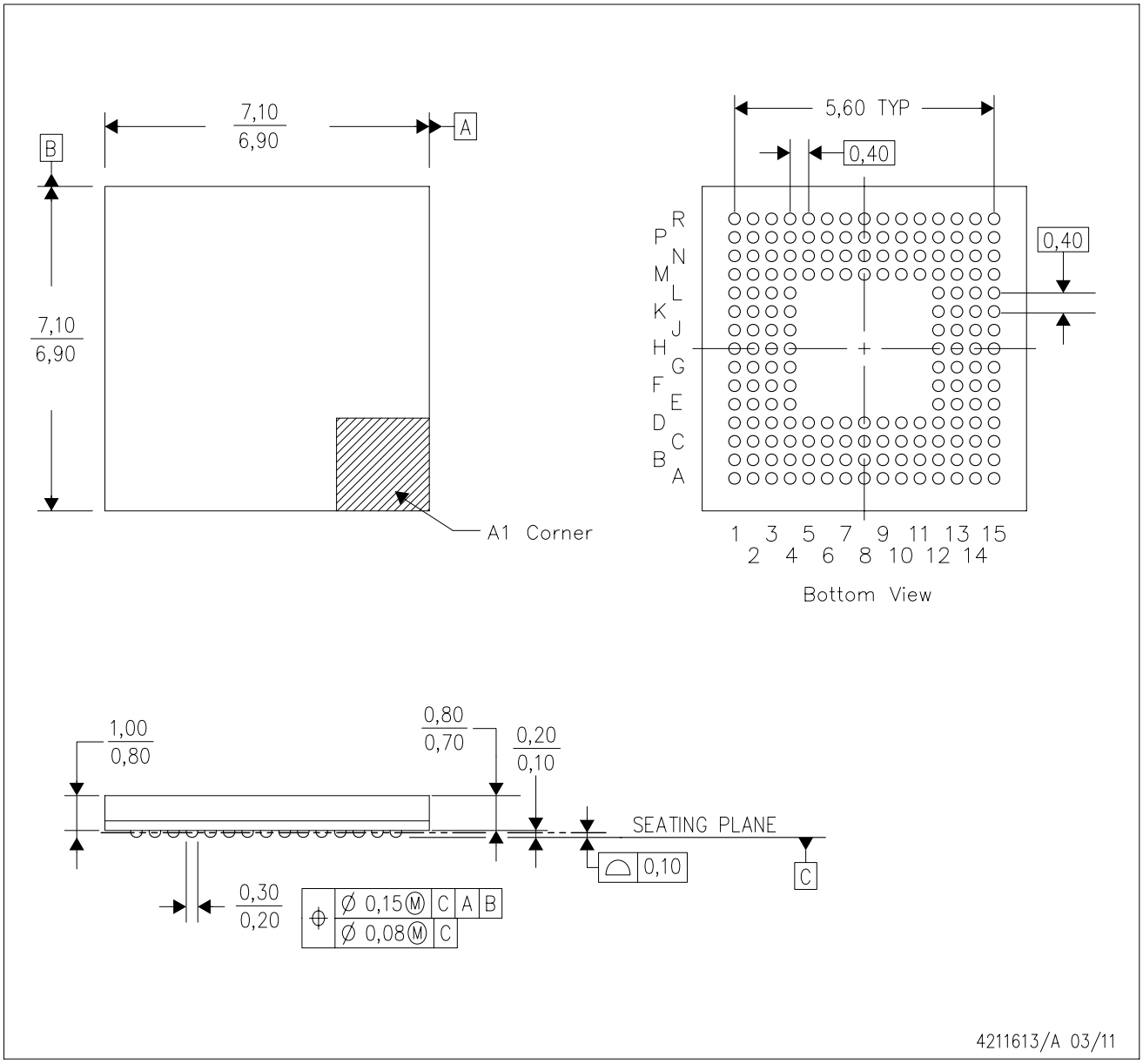
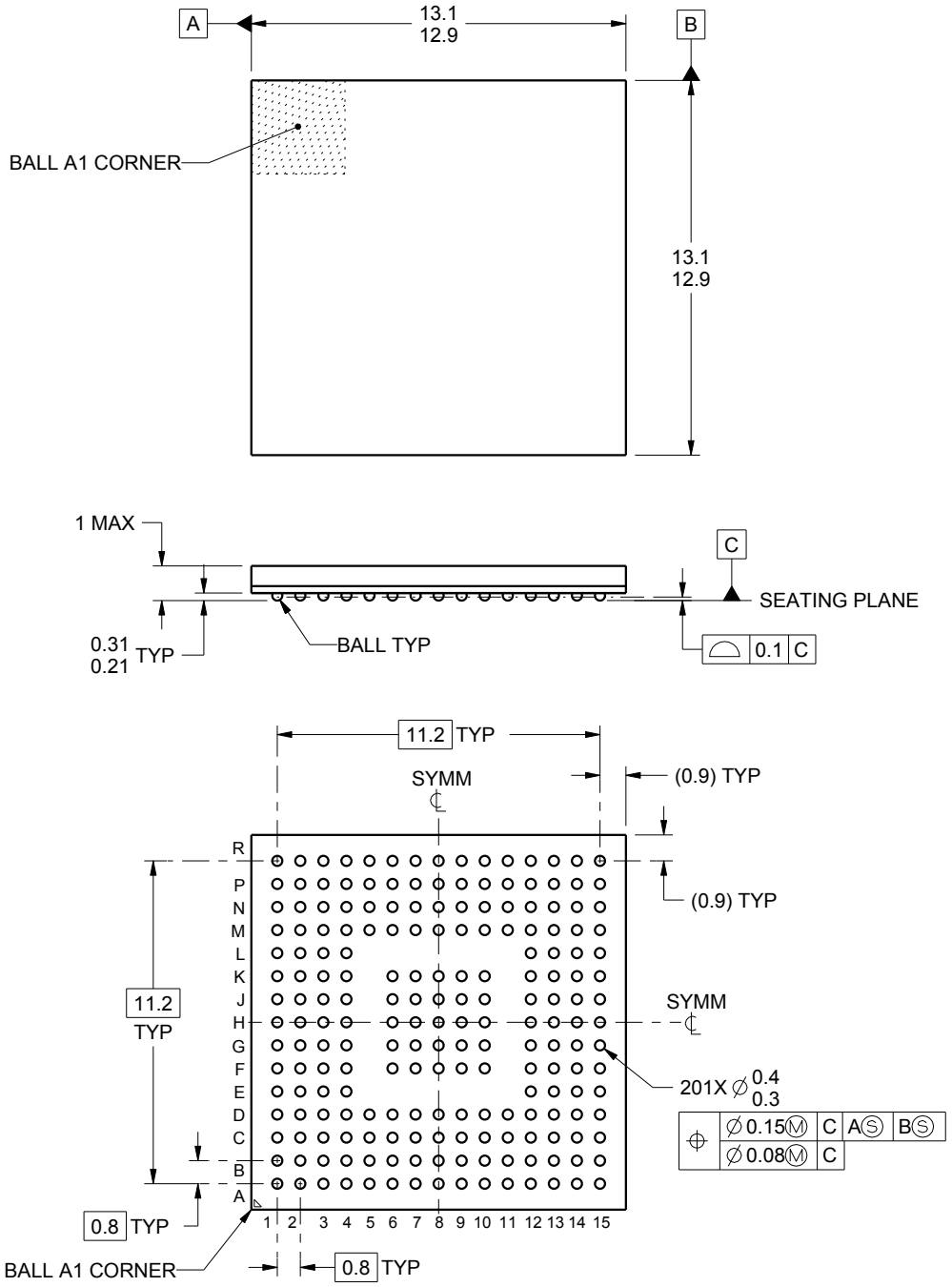
ZVB (S–PBGA–N176) PLASTIC BALL GRID ARRAY

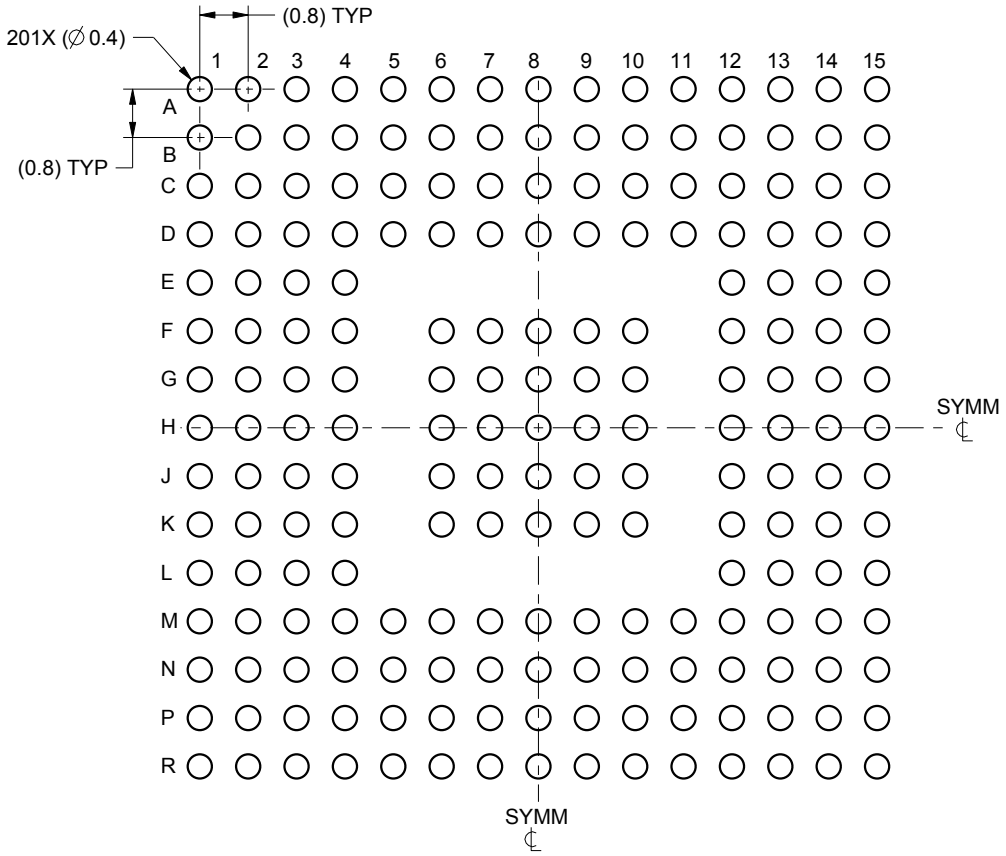


NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This package is Pb–free.

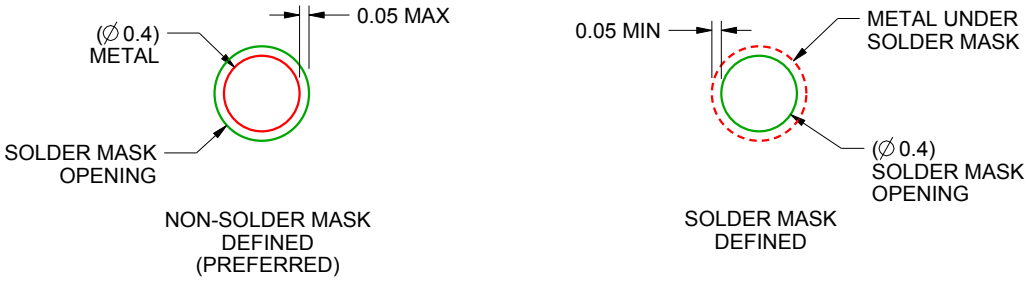


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X

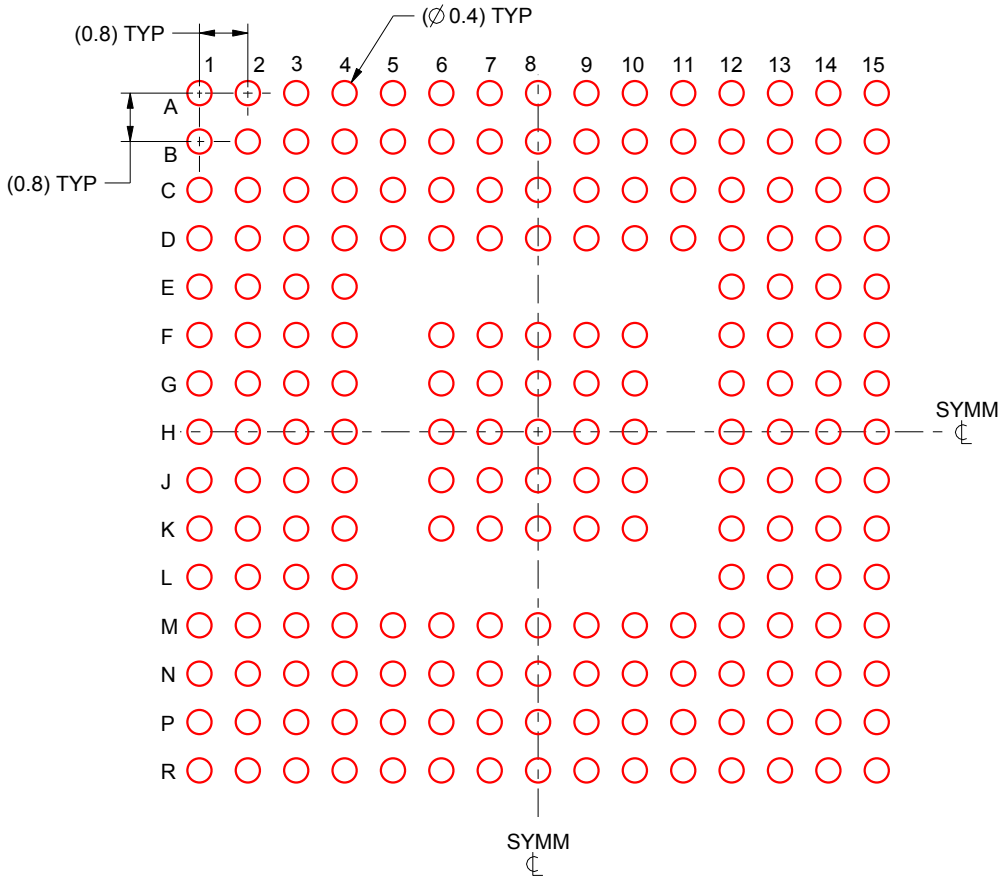


SOLDER MASK DETAILS
NOT TO SCALE

4221521/A 03/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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