具有使能功能的 INA186 双向、低功耗、零漂移、宽动态范围电流感应放大器

1 特性

- 宽共模电压范围 V_{CM}：–0.2V 至 +40V
- 低输入偏置电流 I_{IB}：500pA（典型值）（支持微安级电流测量）
- 低功耗：
  - 低电源电压 (V_S)：1.7V 至 5.5V
  - 低关断电流：100nA（最大值，DDF 封装）
  - 低静态电流 (I_Q)：48µA（典型值）
- 精度：
  - 共模抑制比：120dB（最小值）
  - 增益误差 (E_G)：±1%（最大值）
  - 增益漂移：10ppm/°C（最大值）
  - 失调电压 (V_{OS})：±50µV（最大值）
  - 温漂：0.5µV/°C（最大值）
- 双向电流感应功能
- 增益选项：
  - INA186A1：25V/V
  - INA186A2：50V/V
  - INA186A3：100V/V
  - INA186A4：200V/V
  - INA186A5：500V/V

2 应用

- 标准笔记本电脑
- 智能手机
- 消费类电池充电器
- 基带单元 (BBU)
- 商用网络和服务器 PSU
- 电池测试

3 说明

INA186 是一款低功耗、电压输出、电流感应放大器（也称为电流分流监控器）。此器件常用于过流保护、针对系统优化的精密电流测量或闭环反馈电路。INA186 可在独立于电源电压的 –0.2V 至 +40V 的共模电压下检测分流器上的压降。

INA186 的低输入偏置电流允许使用较大的电流感应电阻器，从而能够提供微安级的精确电流测量。零漂移架构的低失调电压扩展了电流测量的动态范围。此功能可支持较小的感应电阻器在具有较低功率损耗的同时，仍提供精确的电流测量。

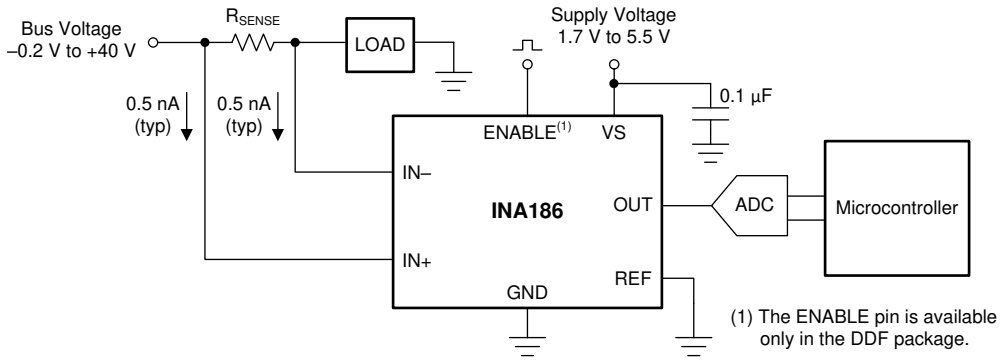
INA186 由 1.7V 至 5.5V 的单电源供电，在启用时消耗的最大电源电流为 90µA。提供五个固定增益选项：25V/V、50V/V、100V/V、200V/V 或 500V/V。该器件的额定工作温度范围为 –40°C 至 +125°C，并采用 SC70 和 SOT-23-THIN 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
INA186	SC70 (6)	2.00mm × 1.25mm
	SOT-23 (8)	3.00mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

典型应用



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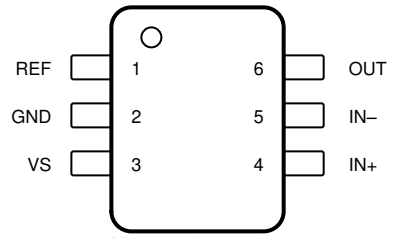
4 修订历史记录

Changes from Original (April 2019) to Revision A	**Page**
• 已添加 向数据表添加了 DDF (SOT-23) 封装和相关内容	1

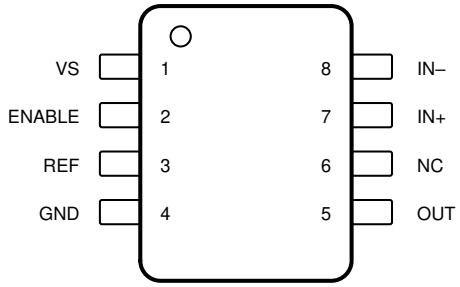
5 Pin Configuration and Functions

DCK Package
6-Pin SC70
Top View



Not to scale

DDF Package
8-Pin SOT23
Top View



Not to scale

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DCK	DDF		
ENABLE	—	2	Digital input	Enable Pin. When this pin is driven to VS, the device is on and functions as a current sense amplifier. When this pin is driven to GND, the device is off, the supply current is reduced, and the output is placed in a high-impedance state. This pin must be driven externally, or connected to VS if not used. DDF package only.
GND	2	4	Analog	Ground
IN–	5	8	Analog input	Current-sense amplifier negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
IN+	4	7	Analog input	Current-sense amplifier positive input. For high-side applications, connect to bus voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
NC	—	6	—	No internal connection. Can be left floating, grounded, or connected to supply.
OUT	6	5	Analog output	OUT pin. This pin provides an analog voltage output that is the gained up voltage difference from the IN+ to the IN– pins, and is offset by the voltage applied to the REF pin.
REF	1	3	Analog input	Reference input. Enables bidirectional current sensing with an externally applied voltage.
VS	3	1	Analog	Power supply, 1.7 V to 5.5 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage			6	V
V_{IN+}, $V_{IN–}$	Analog inputs	Differential (V_{IN+}) – ($V_{IN–}$)(2)	–42	42	V
		V_{IN+}, $V_{IN–}$, with respect to GND(3)	GND – 0.3	42	
V_{ENABLE}	ENABLE		GND – 0.3	6	V
	REF, OUT(3)		GND – 0.3	(V_S) + 0.3	V
	Input current into any pin(3)			5	mA
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage at any pin may exceed the voltage shown if the current at that pin is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input range	GND – 0.2		40	V
V_{IN+}, $V_{IN–}$	Input pin voltage range	GND – 0.2		40	V
V_S	Operating supply voltage	1.7		5.5	V
V_{REF}	Reference pin voltage range	GND		V_S	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA186		UNIT
		DCK (SC70)	DDF (SOT23)	
		6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170.7	137.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	132.7	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.3	57.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	45.7	5.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	65.2	56.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

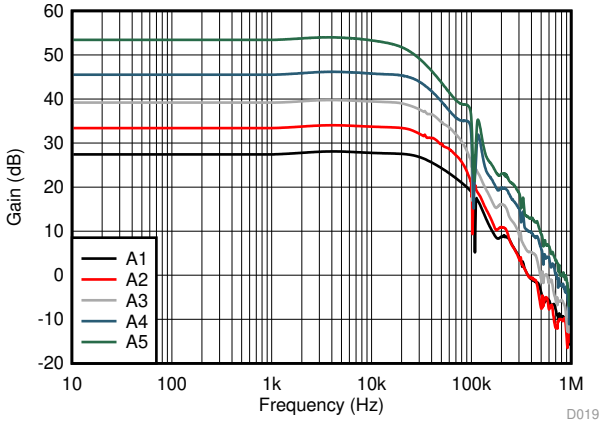
at T_A = 25°C, $V_{SENSE} = V_{IN+} - V_{IN-}$, V_S = 1.8 V to 5.0 V, V_{IN+} = 12 V, and $V_{REF} = V_S / 2$ (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
CMRR	Common-mode rejection ratio	V_{SENSE} = 0 mV, V_{IN+} = –0.1 V to 40 V, T_A = –40°C to +125°C	120	150		dB
V_{OS}	Offset voltage, RTI(1)	V_S = 1.8 V, V_{SENSE} = 0 mV		–3	±50	µV
dV_{OS}/dT	Offset drift, RTI	V_{SENSE} = 0 mV, T_A = –40°C to +125°C		0.05	0.5	µV/°C
PSRR	Power-supply rejection ratio, RTI	V_{SENSE} = 0 mV, V_S = 1.7 V to 5.5 V		–1	±10	µV/V
I_{IB}	Input bias current	V_{SENSE} = 0 mV		0.5	3	nA
I_{IO}	Input offset current	V_{SENSE} = 0 mV		±0.07		nA
OUTPUT						
G	Gain	A1 devices		25		V/V
		A2 devices		50		
		A3 devices		100		
		A4 devices		200		
		A5 devices		500		
E_G	Gain error	V_{OUT} = 0.1 V to V_S – 0.1 V		–0.04%	±1%	
	Gain error drift	T_A = –40°C to +125°C		2	10	ppm/°C
	Nonlinearity error	V_{OUT} = 0.1 V to V_S – 0.1 V		±0.01%		
RVRR	Reference voltage rejection ratio	V_{REF} = 100 mV to V_S – 100 mV, T_A = –40°C to +125°C		±2	±10	µV/V
	Maximum capacitive load	No sustained oscillation		1		nF
VOLTAGE OUTPUT						
V_{SP}	Swing to V_S power-supply rail	V_S = 1.8 V, R_L = 10 kΩ to GND, T_A = –40°C to +125°C		(V_S) – 20	(V_S) – 40	mV
V_{SN}	Swing to GND	V_S = 1.8 V, R_L = 10 kΩ to GND, T_A = –40°C to +125°C, V_{SENSE} = –10 mV, V_{REF} = 0 V		(V_{GND}) + 0.05	(V_{GND}) + 1	mV
V_{ZL}	Zero current output voltage	V_S = 1.8 V, R_L = 10 kΩ to GND, T_A = –40°C to +125°C, V_{SENSE} = 0 mV, V_{REF} = 0 V		(V_{GND}) + 2	(V_{GND}) + 10	mV
FREQUENCY RESPONSE						
BW	Bandwidth	A1 devices, C_{LOAD} = 10 pF		45		kHz
		A2 devices, C_{LOAD} = 10 pF		37		
		A3 devices, C_{LOAD} = 10 pF		35		
		A4 devices, C_{LOAD} = 10 pF		33		
		A5 devices, C_{LOAD} = 10 pF		27		
SR	Slew rate	V_S = 5.0 V, V_{OUT} = 0.5 V to 4.5 V		0.3		V/µs
t_S	Settling time	From current step to within 1% of final value		30		µs
NOISE, RTI(1)						
	Voltage noise density			75		nV/√Hz
ENABLE						
I_{EN}	Leakage input current	0 V ≤ V_{ENABLE} ≤ V_S		1	100	nA
V_{IH}	High-level input voltage		0.7 × V_S		6	V
V_{IL}	Low-level input voltage		0		0.3 × V_S	V
V_{HYS}	Hysteresis			300		mV
I_{ODIS}	Output leakage disabled	V_S = 5.0 V, V_{OUT} = 0 V to 5.0 V, V_{ENABLE} = 0 V		1	5	µA
POWER SUPPLY						
I_Q	Quiescent current	V_S = 1.8 V, V_{SENSE} = 0 mV		48	65	µA
		V_S = 1.8 V, V_{SENSE} = 0 mV, T_A = –40°C to +125°C			90	µA
I_{QDIS}	Quiescent current disabled	V_{ENABLE} = 0 V, V_{SENSE} = 0 mV		10	100	nA

(1) RTI = referred-to-input.

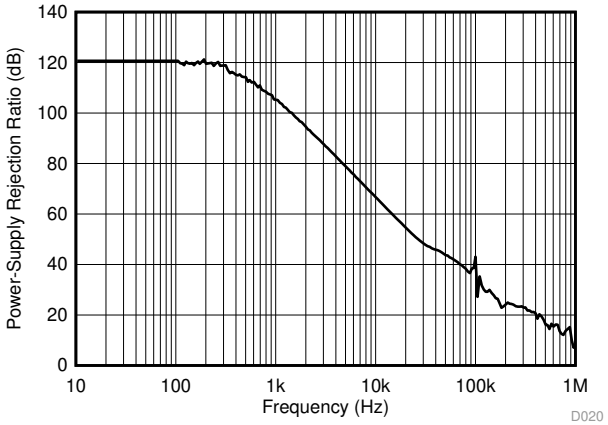
6.6 Typical Characteristics

at T_A = 25°C, V_{SENSE} = V_{IN+} – V_{IN-}, V_S = 1.8 V to 5.0 V, V_{IN+} = 12 V, V_{REF} = V_S / 2, V_{ENABLE} = V_S, and for all gain options (unless otherwise noted)



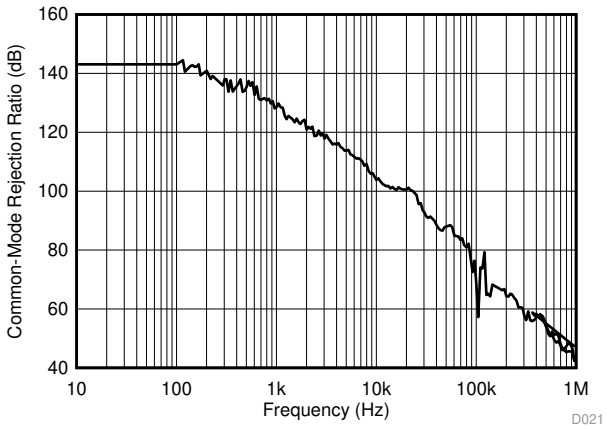
V_S = 5 V

图 1. Gain vs Frequency



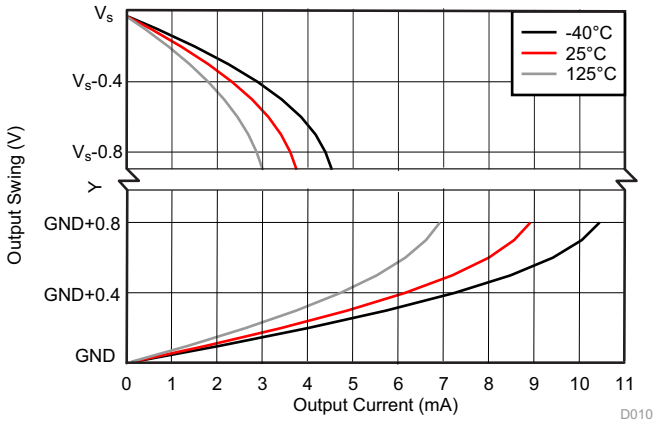
V_S = 5 V

图 2. Power-Supply Rejection Ratio vs Frequency



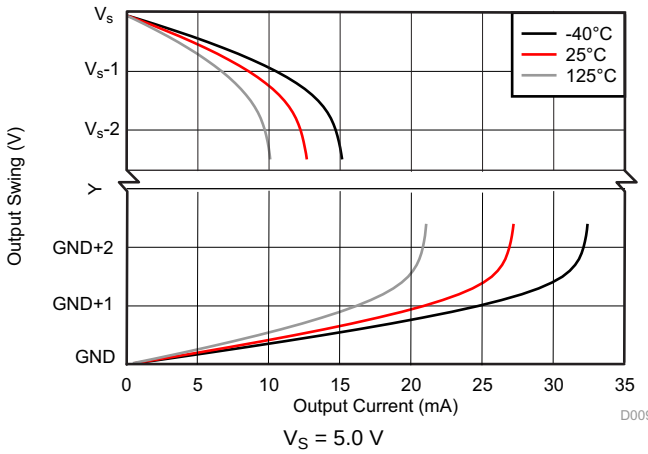
A3 devices

图 3. Common-Mode Rejection Ratio vs Frequency



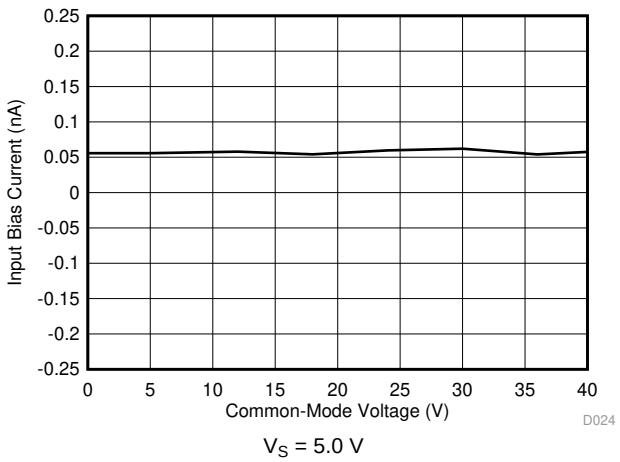
V_S = 1.8 V

图 4. Output Voltage Swing vs Output Current



V_S = 5.0 V

图 5. Output Voltage Swing vs Output Current



V_S = 5.0 V

图 6. Input Bias Current vs Common-Mode Voltage

Typical Characteristics (接下页)

at T_A = 25°C, $V_{SENSE} = V_{IN+} - V_{IN-}$, V_S = 1.8 V to 5.0 V, V_{IN+} = 12 V, $V_{REF} = V_S / 2$, $V_{ENABLE} = V_S$, and for all gain options (unless otherwise noted)

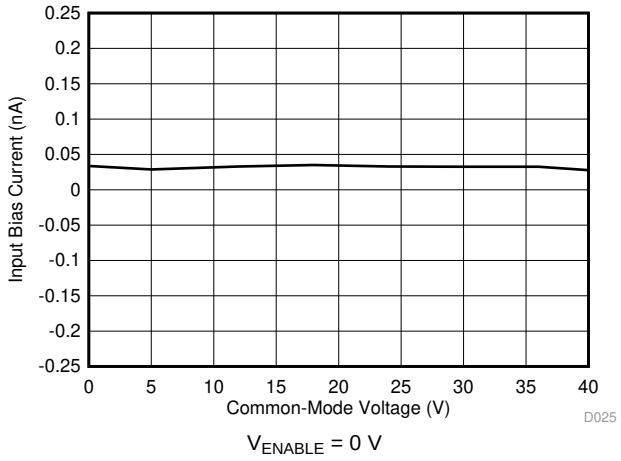


图 7. Input Bias Current vs Common-Mode Voltage (Shutdown)

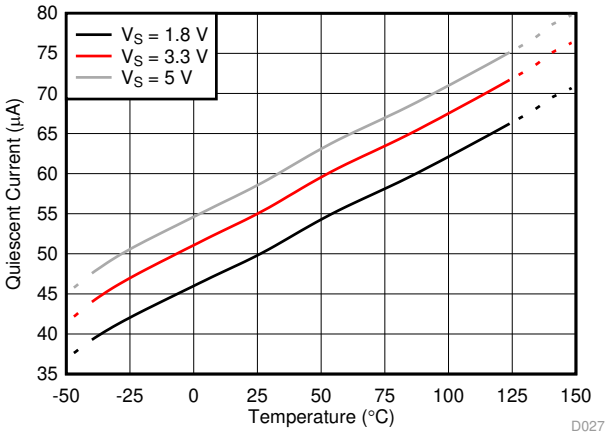


图 8. Quiescent Current vs Temperature (Enabled)

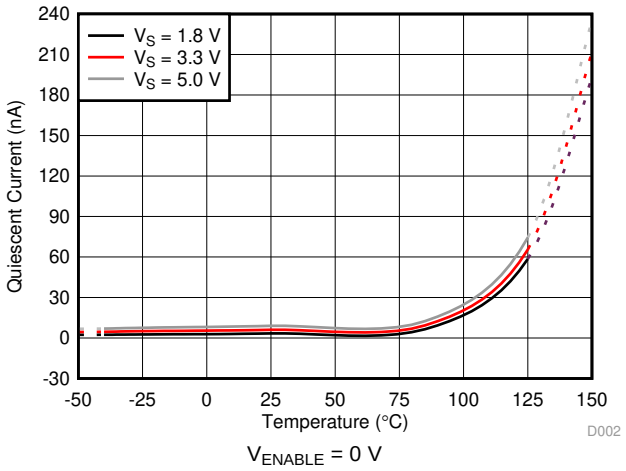


图 9. Quiescent Current vs Temperature (Disabled)

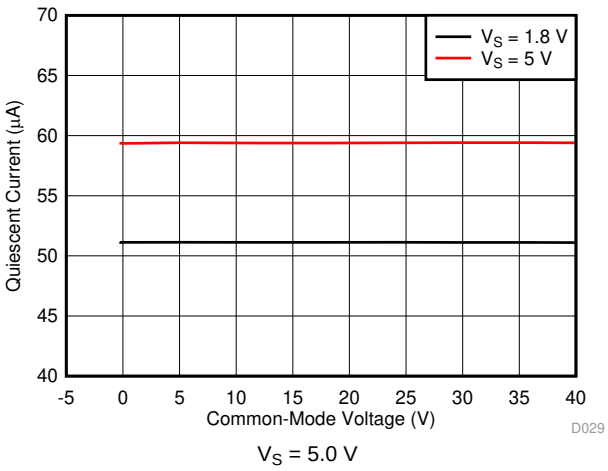


图 10. Quiescent Current vs Common Mode Voltage

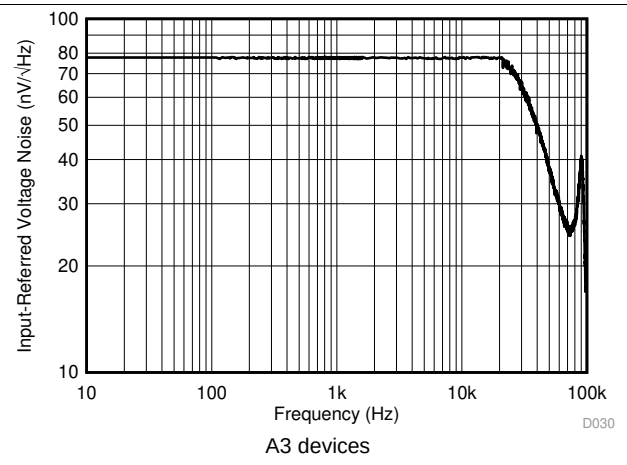


图 11. Input-Referred Voltage Noise vs Frequency

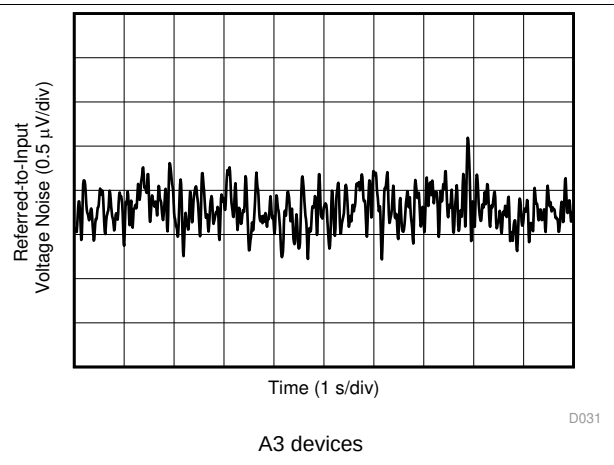
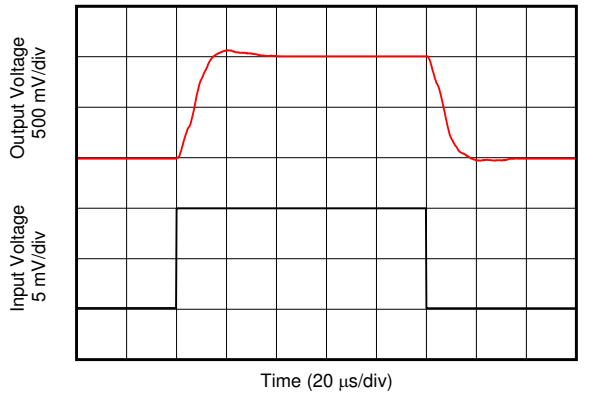


图 12. 0.1-Hz to 10-Hz Voltage Noise (Referred-To-Input)

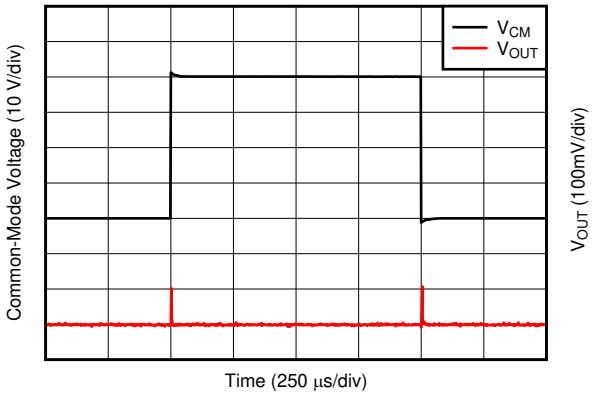
Typical Characteristics (接下页)

at T_A = 25°C, V_{SENSE} = V_{IN+} – V_{IN-}, V_S = 1.8 V to 5.0 V, V_{IN+} = 12 V, V_{REF} = V_S / 2, V_{ENABLE} = V_S, and for all gain options (unless otherwise noted)



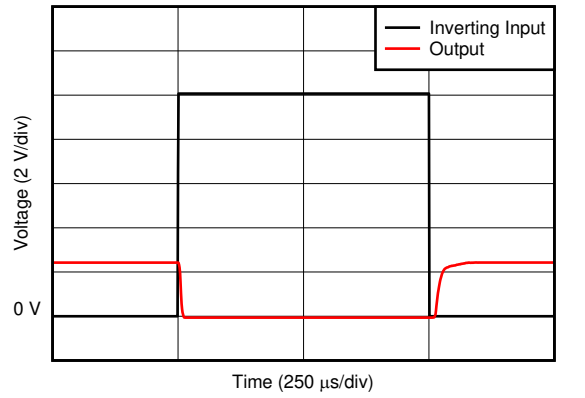
V_S = 5.0 V, A3 devices

图 13. Step Response (10-mV_{PP} Input Step)



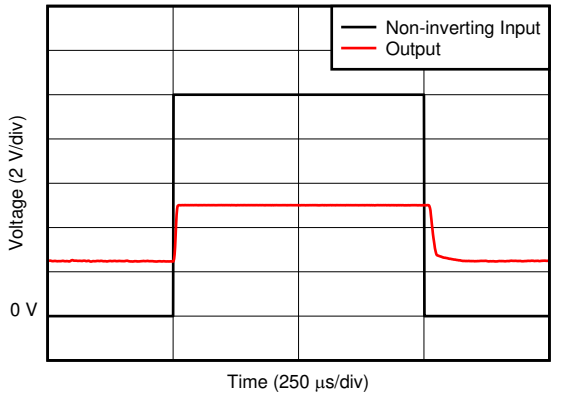
A3 devices

图 14. Common-Mode Voltage Transient Response



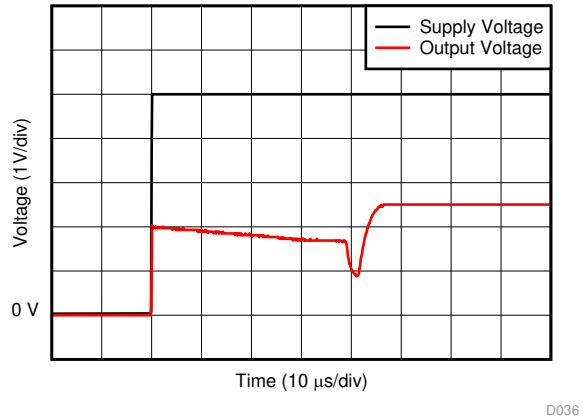
A3 devices

图 15. Inverting Differential Input Overload



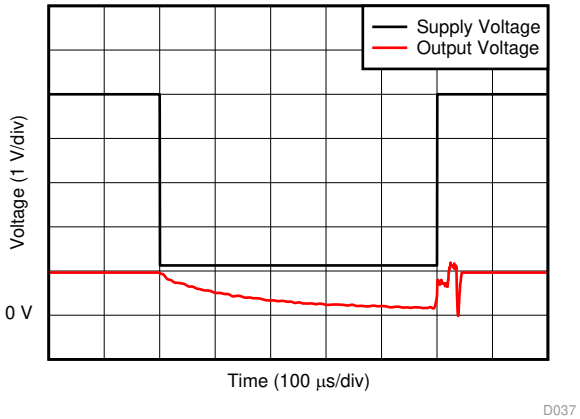
V_S = 5.0 V, A3 devices

图 16. Noninverting Differential Input Overload



V_S = 5.0 V, A3 devices

图 17. Start-Up Response

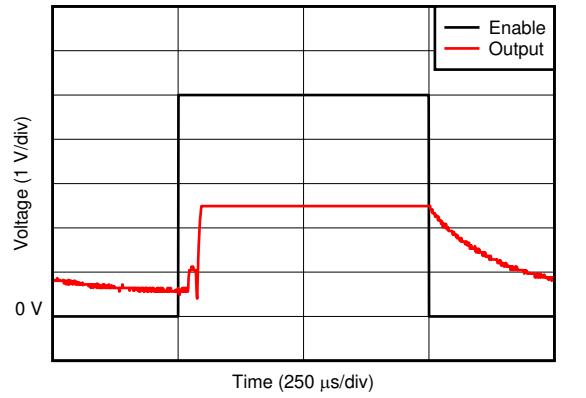


V_S = 5.0 V, A3 devices

图 18. Brownout Recovery

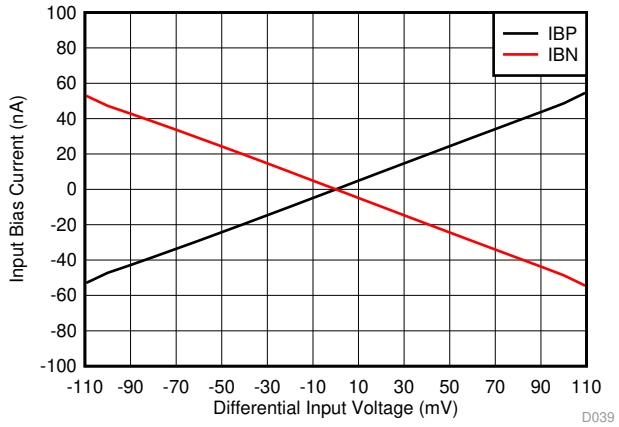
Typical Characteristics (接下页)

at T_A = 25°C, V_{SENSE} = V_{IN+} – V_{IN-}, V_S = 1.8 V to 5.0 V, V_{IN+} = 12 V, V_{REF} = V_S / 2, V_{ENABLE} = V_S, and for all gain options (unless otherwise noted)



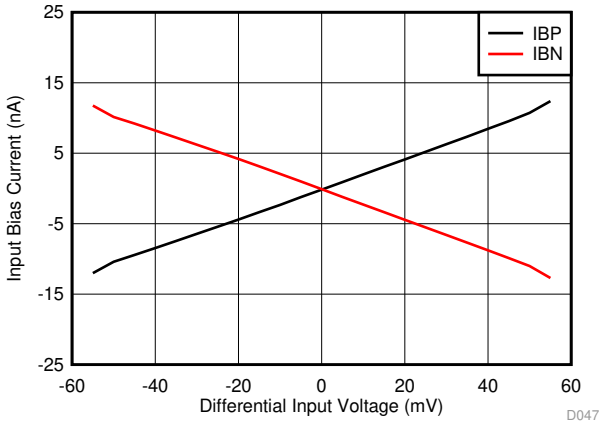
V_S = 5.0 V, A3 devices

图 19. Enable and Disable Response



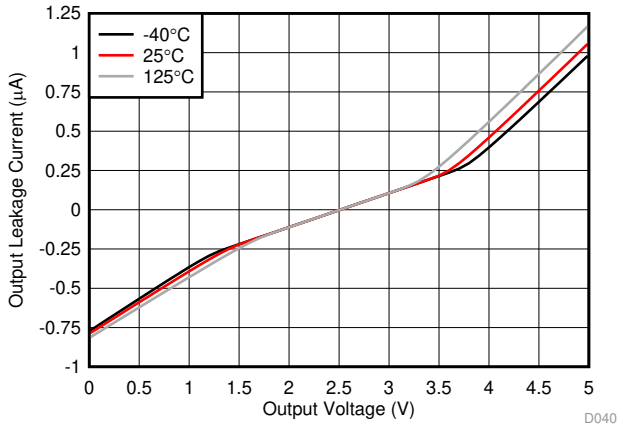
V_S = 5.0 V, V_{REF} = 2.5 V, A1 devices

图 20. IB+ and IB– vs Differential Input Voltage



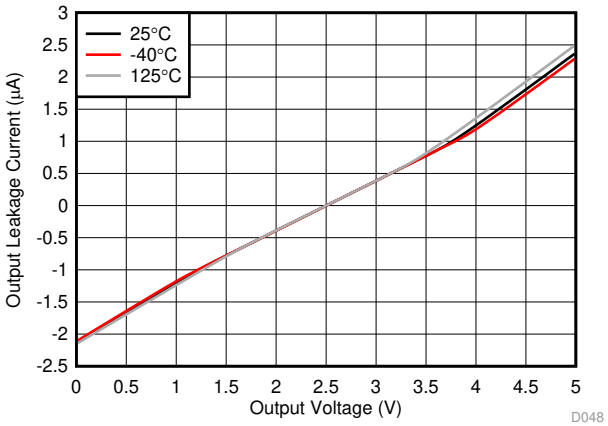
V_S = 5.0 V, V_{REF} = 2.5 V, A2, A3, A4, A5 devices

图 21. IB+ and IB– vs Differential Input Voltage



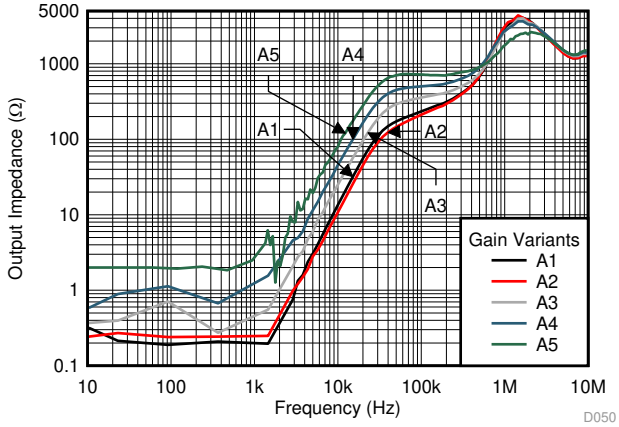
V_S = 5.0 V, V_{ENABLE} = 0 V, V_{REF} = 2.5 V

图 22. Output Leakage vs Output Voltage (A1, A2, and A3 Devices)



V_S = 5.0 V, V_{ENABLE} = 0 V, V_{REF} = 2.5 V

图 23. Output Leakage vs Output Voltage (A4 and A5 Devices)



V_S = 5.0 V, V_{CM} = 0 V

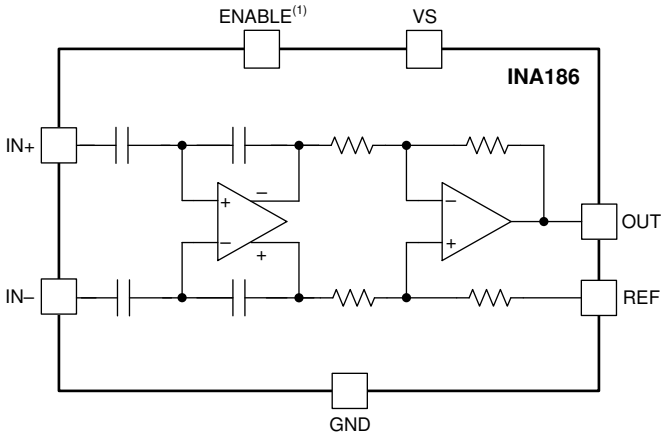
图 24. Output Impedance vs Frequency

7 Detailed Description

7.1 Overview

The INA186 is a low bias current, low offset, 40-V common-mode, current-sensing amplifier. The DDF SOT-23 package also comes with an enable pin.The INA186 is a specially designed, current-sensing amplifier that accurately measures voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage. Current is measured on input voltage rails as high as 40 V at V_{IN+} and $V_{IN–}$, with a supply voltage, V_S, as low as 1.7 V. When disabled, the output goes to a high-impedance state, and the supply current draw is reduced to less than 0.1 µA. The INA186 is intended for use in both low-side and high-side current-sensing configurations where high accuracy and low current consumption are required.

7.2 Functional Block Diagram



(1) The ENABLE pin is available only in the DDF package.

7.3 Feature Description

7.3.1 Precision Current Measurement

The INA186 allows for accurate current measurements over a wide dynamic range. The high accuracy of the device is attributable to the low gain error and offset specifications. The offset voltage of the INA186 is less than ±50 µV. In this case, the low offset improves the accuracy at light loads when V_{IN+} approaches $V_{IN–}$. Another advantage of low offset is the ability to use a lower-value shunt resistor that reduces the power loss in the current-sense circuit, and improves the power efficiency of the end application.

The maximum gain error of the INA186 is specified at ±1%. As the sensed voltage becomes much larger than the offset voltage, the gain error becomes the dominant source of error in the current-sense measurement. When the device monitors currents near the full-scale output range, the total measurement error approaches the value of the gain error.

7.3.2 Low Input Bias Current

The INA186 is different from many current-sense amplifiers because this device offers very low input bias current. The low input bias current of the INA186 has three primary benefits.

The first benefit is the reduction of the current consumed by the device. Classical current-sense amplifier topologies typically consume tens of microamps of current at the inputs. For these amplifiers, the input current is the result of the resistor network that sets the gain and additional current to bias the input amplifier. To reduce the bias current to near zero, the INA186 uses a capacitively coupled amplifier on the input stage, followed by a difference amplifier on the output stage.

The second benefit of low bias current is the ability to use input filters to reject high-frequency noise before the signal is amplified. In a traditional current-sense amplifier, the addition of input filters comes at the cost of reduced accuracy. However, as a result of the low bias currents, input filters have little effect on the measurement accuracy of the INA186.

The third benefit of low bias current is the ability to use a larger current-sense resistor. This ability allows the device to accurately monitor currents as low as 1 µA.

7.3.3 Low Quiescent Current With Output Enable

The device features low quiescent current (I_Q), while still providing sufficient small-signal bandwidth to be usable in most applications. The quiescent current of the INA186 is only 48 µA (typ), while providing a small-signal bandwidth of 35 kHz in a gain of 100. The low I_Q and good bandwidth allow the device to be used in many portable electronic systems without excessive drain on the battery. Because many applications only need to periodically monitor current, the INA186 features an enable pin that turns off the device until needed. When in the disabled state, the INA186 typically draws 10 nA of total supply current.

7.3.4 Bidirectional Current Monitoring

INA186 devices can sense current flow through a sense resistor in both directions. The bidirectional current-sensing capability is achieved by applying a voltage at the REF pin to offset the output voltage. A positive differential voltage sensed at the inputs results in an output voltage that is greater than the applied reference voltage. Likewise, a negative differential voltage at the inputs results in output voltage that is less than the applied reference voltage. The output voltage of the current-sense amplifier is shown in 公式 1.

$$V_{OUT} = \left(I_{LOAD} \times R_{SENSE} \times GAIN\right) + V_{REF} \quad (1)$$

where

- I_{LOAD} is the load current to be monitored.
- R_{SENSE} is the current-sense resistor.
- GAIN is the gain option of the selected device.
- V_{REF} is the voltage applied to the REF pin.

Feature Description (接下页)

7.3.5 High-Side and Low-Side Current Sensing

The INA186 supports input common-mode voltages from –0.2 V to +40 V. Because of the internal topology, the common-mode range is not restricted by the power-supply voltage (V_S). The ability to operate with common-mode voltages greater or less than V_S allows the INA186 to be used in high-side and low-side current-sensing applications, as shown in 图 25.

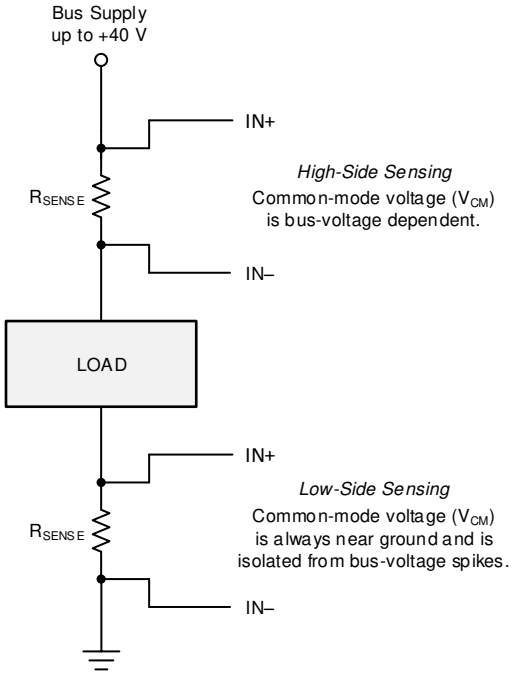


图 25. High-Side and Low-Side Sensing Connections

7.3.6 High Common-Mode Rejection

The INA186 uses a capacitively coupled amplifier on the front end. Therefore, dc common-mode voltages are blocked from downstream circuits, resulting in very high common-mode rejection. Typically, the common-mode rejection of the INA186 is approximately 150 dB. The ability to reject changes in the dc common-mode voltage allows the INA186 to monitor both high-voltage and low-voltage rail currents with very little change in the offset voltage.

7.3.7 Rail-to-Rail Output Swing

The INA186 allows linear current-sensing operation with the output close to the supply rail and ground. The maximum specified output swing to the positive rail is V_S – 40 mV, and the maximum specified output swing to GND is only GND + 1 mV. The close-to-rail output swing is useful to maximize the usable output range, particularly when operating the device from a 1.8-V supply.

7.4 Device Functional Modes

7.4.1 Normal Operation

The INA186 is in normal operation when the following conditions are met:

- The power-supply voltage (V_S) is between 1.7 V and 5.5 V.
- The common-mode voltage (V_{CM}) is within the specified range of –0.2 V to +40 V.
- The maximum differential input signal times the gain plus V_{REF} is less than the positive swing voltage V_{SP}.
- The ENABLE pin is driven or connected to V_S.
- The minimum differential input signal times the gain plus V_{REF} is greater than the zero load swing to GND, V_{ZL} (see the *Rail-to-Rail Output Swing* section).

During normal operation, this device produces an output voltage that is the *amplified* representation of the difference voltage from IN+ to IN– plus the voltage applied to the REF pin.

7.4.2 Unidirectional Mode

This device can be configured to monitor current flowing in one direction (unidirectional) or in both directions (bidirectional) depending on how the REF pin is connected. The most common case is unidirectional where the output is set to ground when no current is flowing by connecting the REF pin to ground, as shown in 图 26. When the current flows from the bus supply to the load, the input voltage from IN+ to IN– increases and causes the output voltage at the OUT pin to increase.

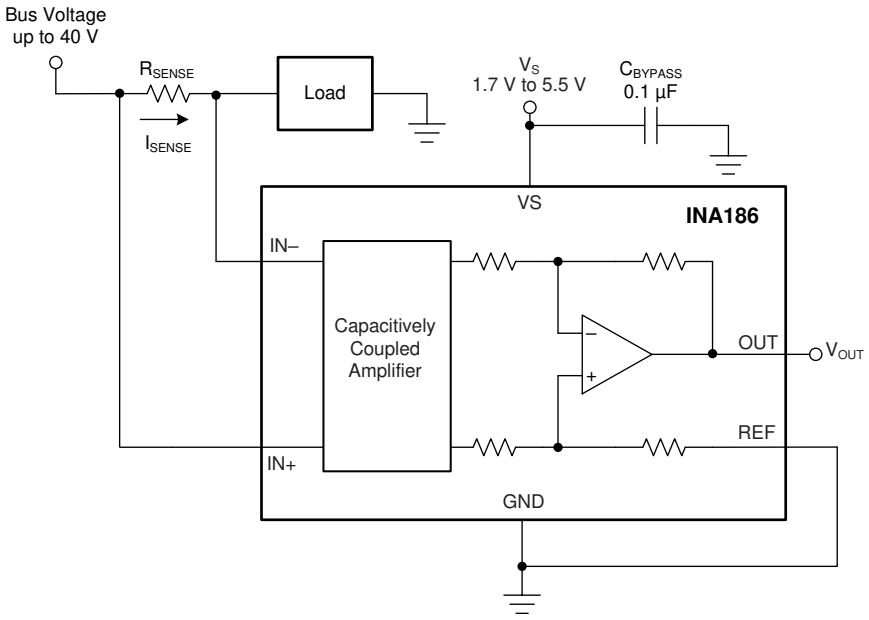


图 26. Typical Unidirectional Application

The linear range of the output stage is limited by how close the output voltage can approach ground under zero input conditions. The zero current output voltage of the INA186 is very small and for most unidirectional applications the REF pin is simply grounded. However, if the measured current multiplied by the current sense resistor and device gain is less than the zero current output voltage, then bias the REF pin to a convenient value above the zero current output voltage to get the output into the linear range of the device. To limit common-mode rejection errors, buffer the reference voltage connected to the REF pin.

A less-frequently used output biasing method is to connect the REF pin to the power-supply voltage, V_S. This method results in the output voltage saturating at 40 mV less than the supply voltage when no differential input voltage is present. This method is similar to the output saturated low condition with no differential input voltage when the REF pin is connected to ground. The output voltage in this configuration only responds to currents that develop negative differential input voltage relative to the device IN– pin. Under these conditions, when the negative differential input signal increases, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF pin must not exceed V_S.

Device Functional Modes (接下页)

Another use for the REF pin in unidirectional operation is to level shift the output voltage. 图 27 shows an application where the device ground is set to a negative voltage so currents biased to negative supplies, as seen in optical networking cards, can be measured. The GND of the INA186 can be set to negative voltages, as long as the inputs do not violate the common-mode range specification and the voltage difference between VS and GND does not exceed 5.5 V. In this example, the output of the INA186 is fed into a positive-biased analog-to-digital converter (ADC). By grounding the REF pin, the voltages at the output will be positive and not damage the ADC. To make sure the output voltage never goes negative, the supply sequencing must be the positive supply first, followed by the negative supply.

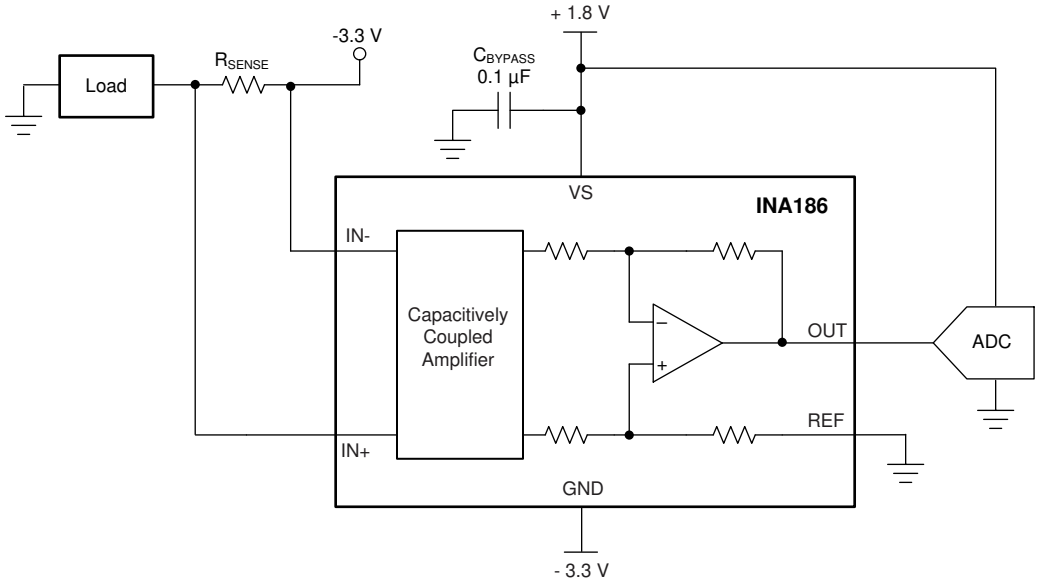


图 27. Using the REF Pin to Level-Shift Output Voltage

Device Functional Modes (接下页)

7.4.3 Bidirectional Mode

The INA186 is a bidirectional current-sense amplifier capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flowing through the resistor can change directions.

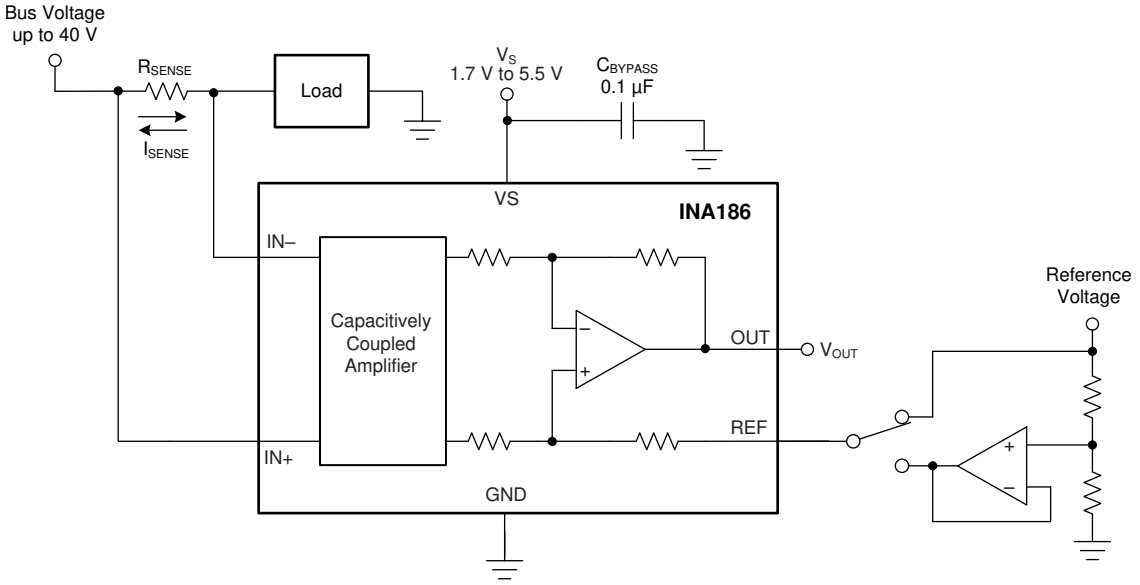


图 28. Bidirectional Application

The ability to measure this current flowing in both directions is achieved by applying a voltage to the REF pin, as shown in 图 28. The voltage applied to REF (V_{REF}) sets the output state that corresponds to the zero-input level state. The output then responds by increasing above V_{REF} for positive differential signals (relative to the IN– pin) and responds by decreasing below V_{REF} for negative differential signals. This reference voltage applied to the REF pin can be set anywhere between 0 V to V_S. For bidirectional applications, V_{REF} is typically set at $V_S/2$ for equal signal range in both current directions. In some cases, V_{REF} is set at a voltage other than $V_S/2$; for example, when the bidirectional current and corresponding output signal do not need to be symmetrical.

7.4.4 Input Differential Overload

If the differential input voltage ($V_{IN+} – V_{IN–}$) times gain exceeds the voltage swing specification, the INA186 drives its output as close as possible to the positive supply or ground, and does not provide accurate measurement of the differential input voltage. If this input overload occurs during normal circuit operation, then reduce the value of the shunt resistor or use a lower-gain version with the chosen sense resistor to avoid this mode of operation. If a differential overload occurs in a time-limited fault event, then the output of the INA186 returns to the expected value approximately 80 µs after the fault condition is removed.

Device Functional Modes (接下页)

7.4.5 Shutdown

The INA186 features an active-high ENABLE pin that shuts down the device when pulled to ground. When the device is shut down, the quiescent current is reduced to 10 nA (typ), and the output goes to a high-impedance state. In a battery-powered application, the low quiescent current extends the battery lifetime when the current measurement is not needed. When the ENABLE pin is driven to the supply voltage, the device turns back on. The typical output settling time when enabled is 130 µs.

The output of the INA186 goes to a high-impedance state when disabled. Therefore, you can connect multiple outputs of the INA186 together to a single ADC or measurement device, as shown in 图 29.

When connected in this way, enable only one INA186 at a time, and make sure all devices have the same supply voltage.

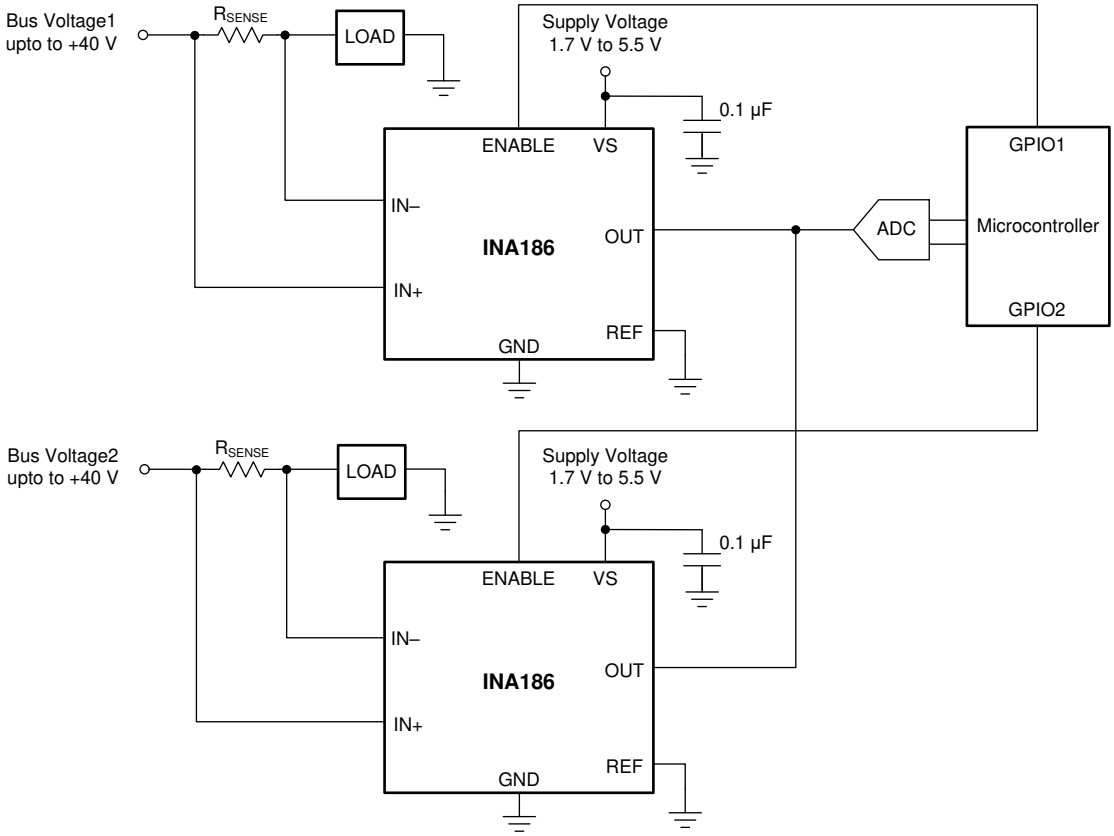


图 29. Multiplexing Multiple Devices With the ENABLE Pin

8 Application and Implementation

注

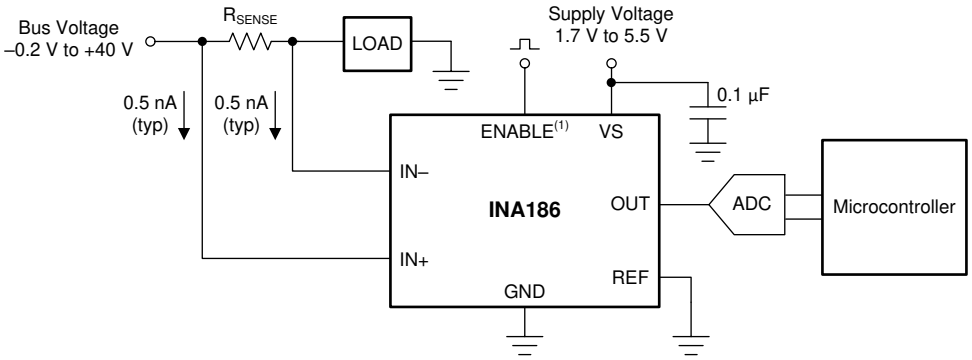
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA186 amplifies the voltage developed across a current-sensing resistor as current flows through the resistor to the load or ground. The high common-mode rejection of the INA186 makes it usable over a wide range of voltage rails while still maintaining an accurate current measurement.

8.1.1 Basic Connections

图 30 shows the basic connections of the INA186. Place the device as close as possible to the current sense resistor and connect the input pins (IN+ and IN–) to the current sense resistor through kelvin connections. If present, the ENABLE pin must be controlled externally or connected to VS if not used.



(1) The ENABLE pin is available only in the DDF package.

NOTE: To help eliminate ground offset errors between the device and the analog-to-digital converter (ADC), connect the REF pin to the ADC reference input. When driving SAR ADCs, filter or buffer the output of the INA186 before connecting directly to the ADC.

图 30. Basic Connections

Application Information (接下页)

8.1.2 R_{SENSE} and Device Gain Selection

The accuracy of any current-sense amplifier is maximized by choosing the current-sense resistor to be as large as possible. A large sense resistor maximizes the differential input signal for a given amount of current flow and reduces the error contribution of the offset voltage. However, there are practical limits as to how large the current-sense resistor can be in a given application because of the resistor size and maximum allowable power dissipation. 公式 2 gives the maximum value for the current-sense resistor for a given power dissipation budget:

$$R_{SENSE} < \frac{PD_{MAX}}{I_{MAX}^2} \quad (2)$$

where:

- PD_{MAX} is the maximum allowable power dissipation in R_{SENSE}.
- I_{MAX} is the maximum current that will flow through R_{SENSE}.

An additional limitation on the size of the current-sense resistor and device gain is due to the power-supply voltage, V_S, and device swing-to-rail limitations. In order to make sure that the current-sense signal is properly passed to the output, both positive and negative output swing limitations must be examined. 公式 3 provides the maximum values of R_{SENSE} and GAIN to keep the device from exceeding the positive swing limitation.

$$I_{MAX} \times R_{SENSE} \times GAIN < V_{SP} - V_{REF} \quad (3)$$

where:

- I_{MAX} is the maximum current that will flow through R_{SENSE}.
- GAIN is the gain of the current-sense amplifier.
- V_{SP} is the positive output swing as specified in the data sheet.
- V_{REF} is the externally applied voltage on the REF pin.

To avoid positive output swing limitations when selecting the value of R_{SENSE}, there is always a trade-off between the value of the sense resistor and the gain of the device under consideration. If the sense resistor selected for the maximum power dissipation is too large, then it is possible to select a lower-gain device in order to avoid positive swing limitations.

The negative swing limitation places a limit on how small the sense resistor value can be for a given application. 公式 4 provides the limit on the minimum value of the sense resistor.

$$I_{MIN} \times R_{SENSE} \times GAIN > V_{SN} - V_{REF} \quad (4)$$

where:

- I_{MIN} is the minimum current that will flow through R_{SENSE}.
- GAIN is the gain of the current-sense amplifier.
- V_{SN} is the negative output swing of the device (see the *Rail-to-Rail Output Swing* section).
- V_{REF} is the externally applied voltage on the REF pin.

In addition to adjusting R_{SENSE} and the device gain, the voltage applied to the REF pin can be slightly increased above GND to avoid negative swing limitations.

Application Information (接下页)

8.1.3 Signal Conditioning

When performing accurate current measurements in noisy environments, the current-sensing signal is often filtered. The INA186 features low input bias currents. Therefore, adding a differential mode filter to the input without sacrificing the current-sense accuracy is possible. Filtering at the input is advantageous because this action attenuates differential noise before the signal is amplified. 图 31 provides an example of how to use a filter on the input pins of the device.

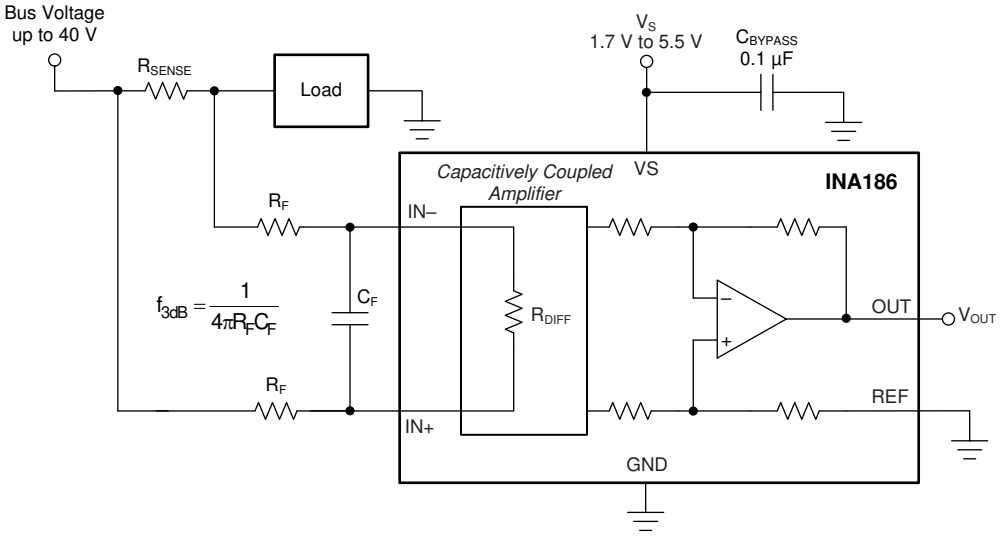


图 31. Filter at the Input Pins

The differential input impedance (R_{DIFF}) shown in 图 31 limits the maximum value for R_F. The value of R_{DIFF} is a function of the device temperature, as shown in 图 32.

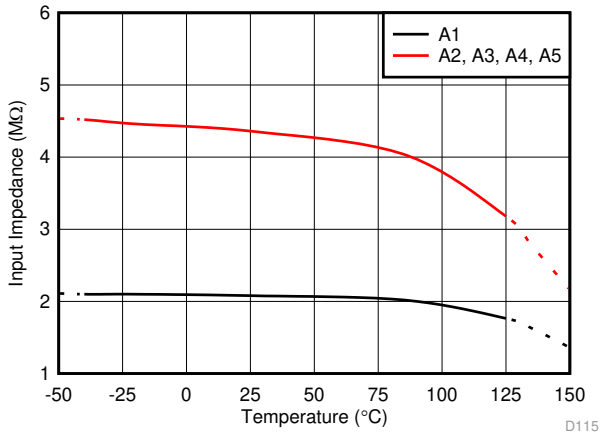


图 32. Differential Input Impedance vs Temperature

Application Information (接下页)

As the voltage drop across the sense resistor (V_{SENSE}) increases, the amount of voltage dropped across the input filter resistors (R_F) also increases. The increased voltage drop results in additional gain error. The error caused by these resistors is calculated by the resistor divider equation shown in 公式 5.

$$\text{Error}(\%) = \left(1 - \frac{R_{DIFF}}{R_{SENSE} + R_{DIFF} + (2 \times R_F)}\right) \times 100 \quad (5)$$

where:

- R_{DIFF} is the differential input impedance.
- R_F is the added value of the series filter resistance.

The input stage of the INA186 uses a capacitive feedback amplifier topology in order to achieve high dc precision. As a result, periodic high-frequency shunt voltage (or current) transients of significant amplitude (10 mV or greater) and duration (hundreds of nanoseconds or greater) may be amplified by the INA186, even though the transients are greater than the device bandwidth. Use a differential input filter in these applications to minimize disturbances at the INA186 output.

The high input impedance and low bias current of the INA186 provide flexibility in the input filter design without impacting the accuracy of current measurement. For example, set R_F = 100 Ω and C_F = 22 nF to achieve a low-pass filter corner frequency of 36.2 kHz. These filter values significantly attenuate most unwanted high-frequency signals at the input without severely impacting the current sensing bandwidth or precision. If a lower corner frequency is desired, increase the value of C_F.

Filtering the input filters out differential noise across the sense resistor. If high-frequency, common-mode noise is a concern, add an RC filter from the OUT pin to ground. The RC filter helps filter out both differential and common mode noise, as well as internally generated noise from the device. The value for the resistance of the RC filter is limited by the impedance of the load. Any current drawn by the load manifests as an external voltage drop from the INA186 OUT pin to the load input. To select the optimal values for the output filter, use 图 24 and see the *Closed-Loop Analysis of Load-Induced Amplifier Stability Issues Using ZOUT* application report

Application Information (接下页)

8.1.4 Common-Mode Voltage Transients

With a small amount of additional circuitry, the INA186 can be used in circuits subject to transients that exceed the absolute maximum voltage ratings. The most simple way to protect the inputs from negative transients is to add resistors in series with the IN– and IN+ pins. Use resistors that are 1 kΩ or less, and limit the current in the ESD structures to less than 5 mA. For example, using 1-kΩ resistors in series with the INA186 allows voltages as low as –5 V, while limiting the ESD current to less than 5 mA. If protection from high-voltage or more-negative, common-voltage transients is needed, use the circuits shown in 图 33 and 图 34. When implementing these circuits, use only Zener diodes or Zener-type transient absorbers (sometimes referred to as *transzorbs*); any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as a working impedance for the Zener diode, as shown in 图 33. Keep these resistors as small as possible; most often, use around 100 Ω. Larger values can be used with an effect on gain that is discussed in the *Signal Conditioning* section. This circuit limits only short-term transients; therefore, many applications are satisfied with a 100-Ω resistor along with conventional Zener diodes of the lowest acceptable power rating. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

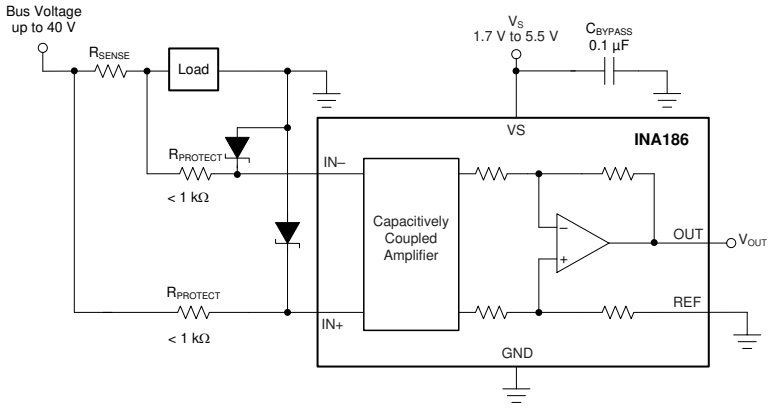


图 33. Transient Protection Using Dual Zener Diodes

In the event that low-power Zener diodes do not have sufficient transient absorption capability, a higher-power transzorb must be used. The most package-efficient solution involves using a single transzorb and back-to-back diodes between the device inputs, as shown in 图 34. The most space-efficient solutions are dual, series-connected diodes in a single SOT-523 or SOD-523 package. In either of the examples shown in 图 33 and 图 34, the total board area required by the INA186 with all protective components is less than that of an SO-8 package, and only slightly greater than that of an VSSOP-8 package.

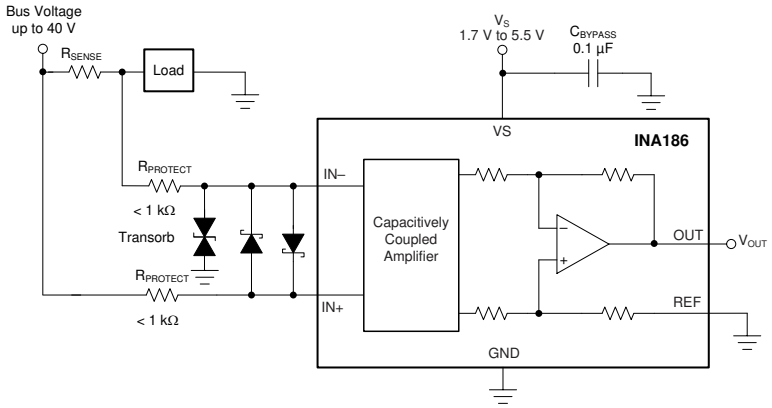


图 34. Transient Protection Using a Single Transzorb and Input Clamps

For more information, see the *Current Shunt Monitor With Transient Robustness* reference design.

8.2 Typical Applications

The low input bias current of the INA186 allows accurate monitoring of small-value currents. To accurately monitor currents in the microamp range, increase the value of the sense resistor to increase the sense voltage so that the error introduced by the offset voltage is small. The circuit configuration for monitoring low-value currents is shown in 图 35. As a result of the differential input impedance of the INA186, limit the value of R_{SENSE} to 1 kΩ or less for best accuracy.

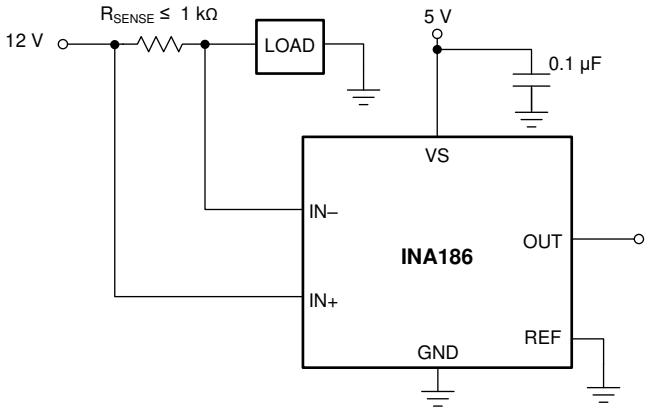


图 35. Microamp Current Measurement

8.2.1 Design Requirements

The design requirements for the circuit shown in 图 35 are listed in 表 1.

表 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage (V_S)	5 V
Bus supply rail (V_{CM})	12 V
Minimum sense current (I_{MIN})	1 µA
Maximum sense current (I_{MAX})	150 µA
Device gain (GAIN)	25 V/V
Reference voltage (V_{REF})	0 V

8.2.2 Detailed Design Procedure

The maximum value of the current-sense resistor is calculated based on choice of gain, value of the maximum current the be sensed (I_{MAX}), and the power supply voltage (V_S). When operating at the maximum current, the output voltage must not exceed the positive output swing specification, V_{SP}. Using 公式 6, for the given design parameters the maximum value for R_{SENSE} is calculated to be 1.321 kΩ.

$$R_{SENSE} < \frac{V_{SP}}{I_{MAX} \times GAIN} \tag{6}$$

However, because this value exceeds the maximum recommended value for R_{SENSE}, a resistance value of 1 kΩ must be used. When operating at the minimum current value, I_{MIN} the output voltage must be greater than the swing to GND (V_{SN}), specification. For this example, the output voltage at the minimum current is calculated using 公式 7 to be 25 mV, which is greater than the value for V_{SN}.

$$V_{OUTMIN} = I_{MIN} \times R_{SENSE} \times GAIN \tag{7}$$

8.2.3 Application Curve

图 36 shows the output of the device under the conditions given in 表 1 and with R_{SENSE} = 1 kΩ.

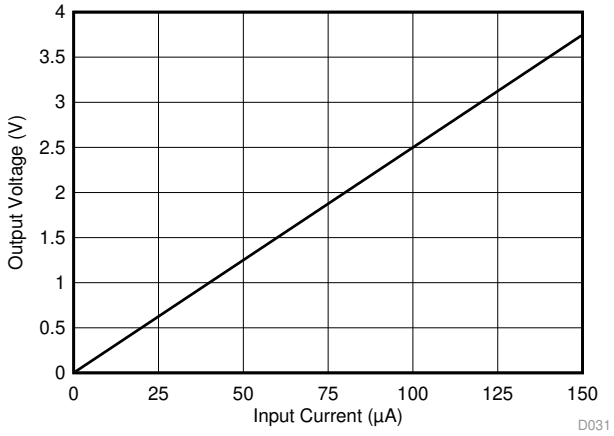


图 36. Typical Application DC Transfer Function

9 Power Supply Recommendations

The input circuitry of the INA186 accurately measures beyond the power-supply voltage, V_S. For example, V_S can be 5 V, whereas the bus supply voltage at IN+ and IN– can be as high as 40 V. However, the output voltage range of the OUT pin is limited by the voltage on the VS pin. The INA186 also withstands the full differential input signal range up to 40 V at the IN+ and IN– input pins, regardless of whether the device has power applied at the VS pin. There is no sequencing requirement for V_S and V_{IN+} or $V_{IN–}$.

10 Layout

10.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the device power supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- When routing the connections from the current-sense resistor to the device, keep the trace lengths as short as possible. The input filter capacitor C_F should be placed as close as possible to the input pins of the device.

10.2 Layout Examples

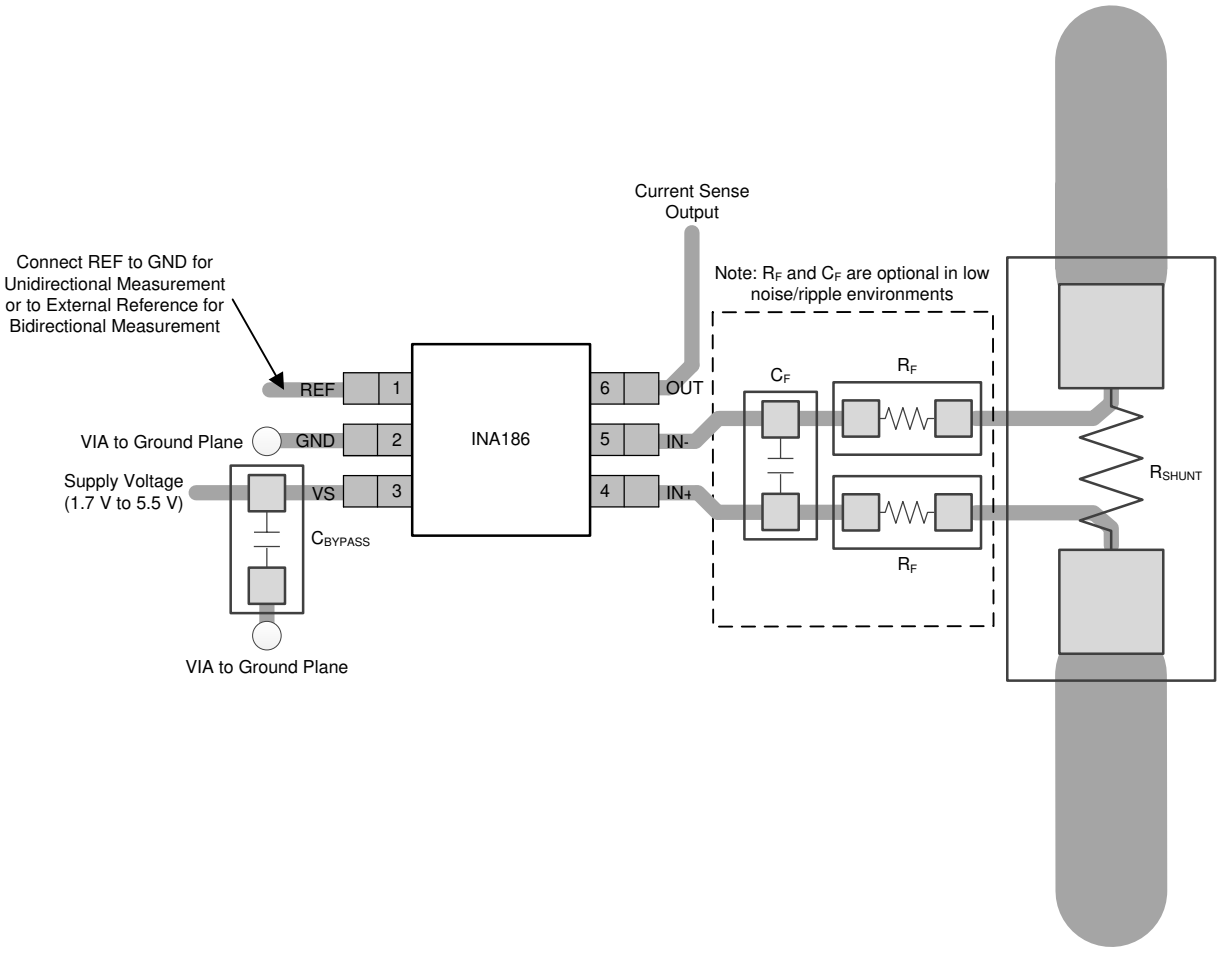


图 37. Recommended Layout for SC70 (DCK) Package

Layout Examples (接下页)

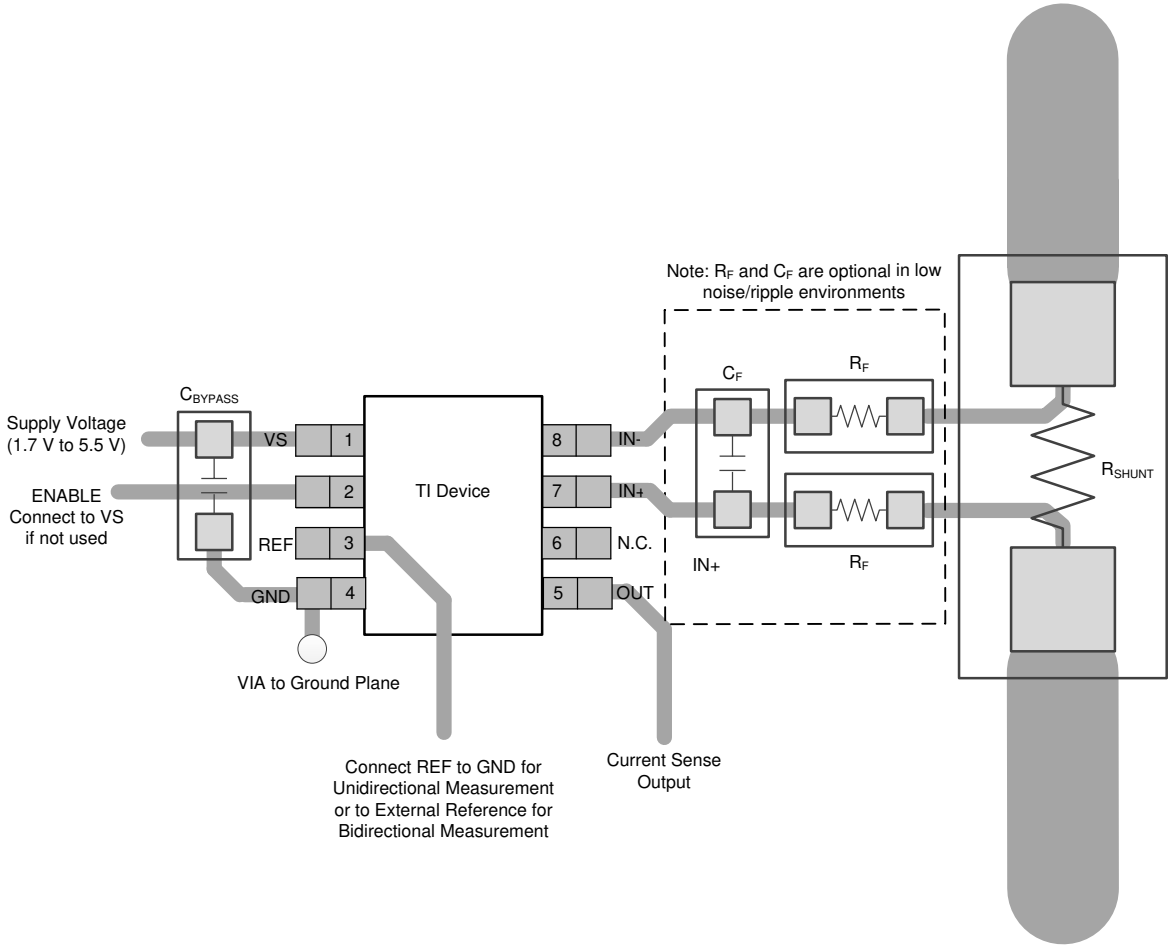


图 38. Recommended Layout for SOT-23 (DDF) Package

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：德州仪器 (TI)，*INA186EVM 用户指南*

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA186A1IDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1E7	Samples
INA186A1IDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1E7	Samples
INA186A1IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZLW	Samples
INA186A1IDDFT	ACTIVE	SOT-23-THIN	DDF	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZLW	Samples
INA186A1IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1IJ	Samples
INA186A2IDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1E8	Samples
INA186A2IDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1E8	Samples
INA186A2IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZMW	Samples
INA186A2IDDFT	ACTIVE	SOT-23-THIN	DDF	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZMW	Samples
INA186A2IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1IK	Samples
INA186A3IDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1E9	Samples
INA186A3IDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1E9	Samples
INA186A3IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZNW	Samples
INA186A3IDDFT	ACTIVE	SOT-23-THIN	DDF	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZNW	Samples
INA186A3IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1IL	Samples
INA186A4IDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1EA	Samples
INA186A4IDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1EA	Samples
INA186A4IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZOW	Samples
INA186A4IDDFT	ACTIVE	SOT-23-THIN	DDF	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZOW	Samples
INA186A4IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1IM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA186A5IDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1EB	Samples
INA186A5IDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1EB	Samples
INA186A5IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZPW	Samples
INA186A5IDDFT	ACTIVE	SOT-23-THIN	DDF	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZPW	Samples
INA186A5IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1IN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA186 :

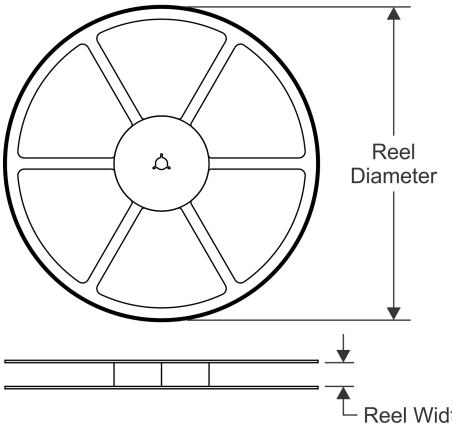
- Automotive : INA186-Q1

NOTE: Qualified Version Definitions:

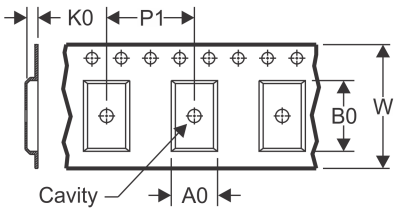
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

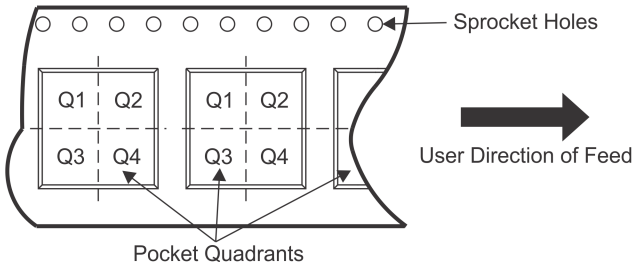


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

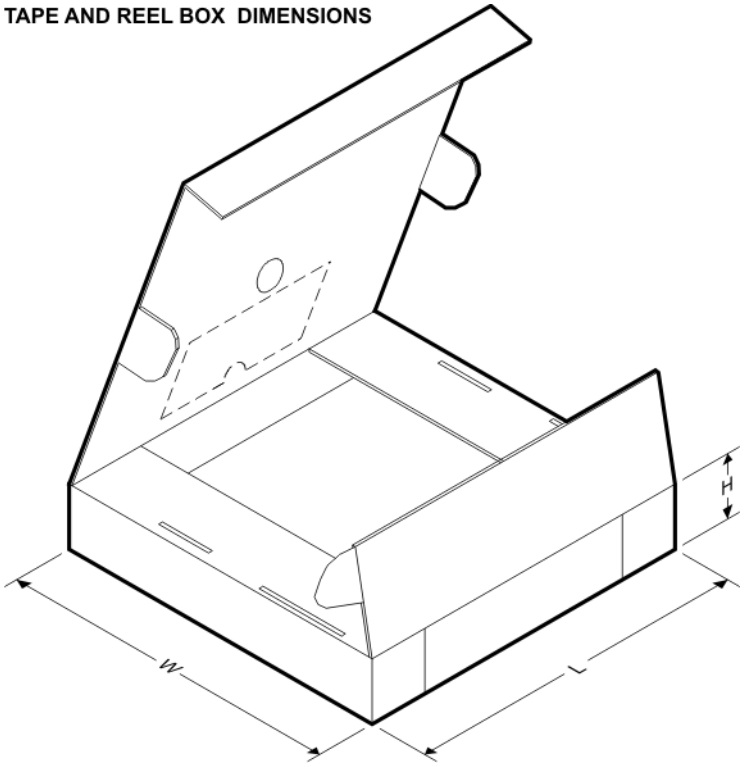


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA186A1IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A1IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A1IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A1IYFDR	DSBGA	YFD	6	3000	178.0	8.4	0.84	1.27	0.46	4.0	8.0	Q2
INA186A2IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A2IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A2IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A2IDDFT	SOT-23-THIN	DDF	8	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A2IYFDR	DSBGA	YFD	6	3000	178.0	8.4	0.84	1.27	0.46	4.0	8.0	Q2
INA186A3IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A3IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A3IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A3IDDFT	SOT-23-THIN	DDF	8	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A3IYFDR	DSBGA	YFD	6	3000	178.0	8.4	0.84	1.27	0.46	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA186A4IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A4IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A4IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A4IYFDR	DSBGA	YFD	6	3000	178.0	8.4	0.84	1.27	0.46	4.0	8.0	Q2
INA186A5IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A5IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A5IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A5IDDFT	SOT-23-THIN	DDF	8	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A5IYFDR	DSBGA	YFD	6	3000	178.0	8.4	0.84	1.27	0.46	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA186A1IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA186A1IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA186A1IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
INA186A1IYFDR	DSBGA	YFD	6	3000	220.0	220.0	35.0
INA186A2IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA186A2IDCKT	SC70	DCK	6	250	180.0	180.0	18.0

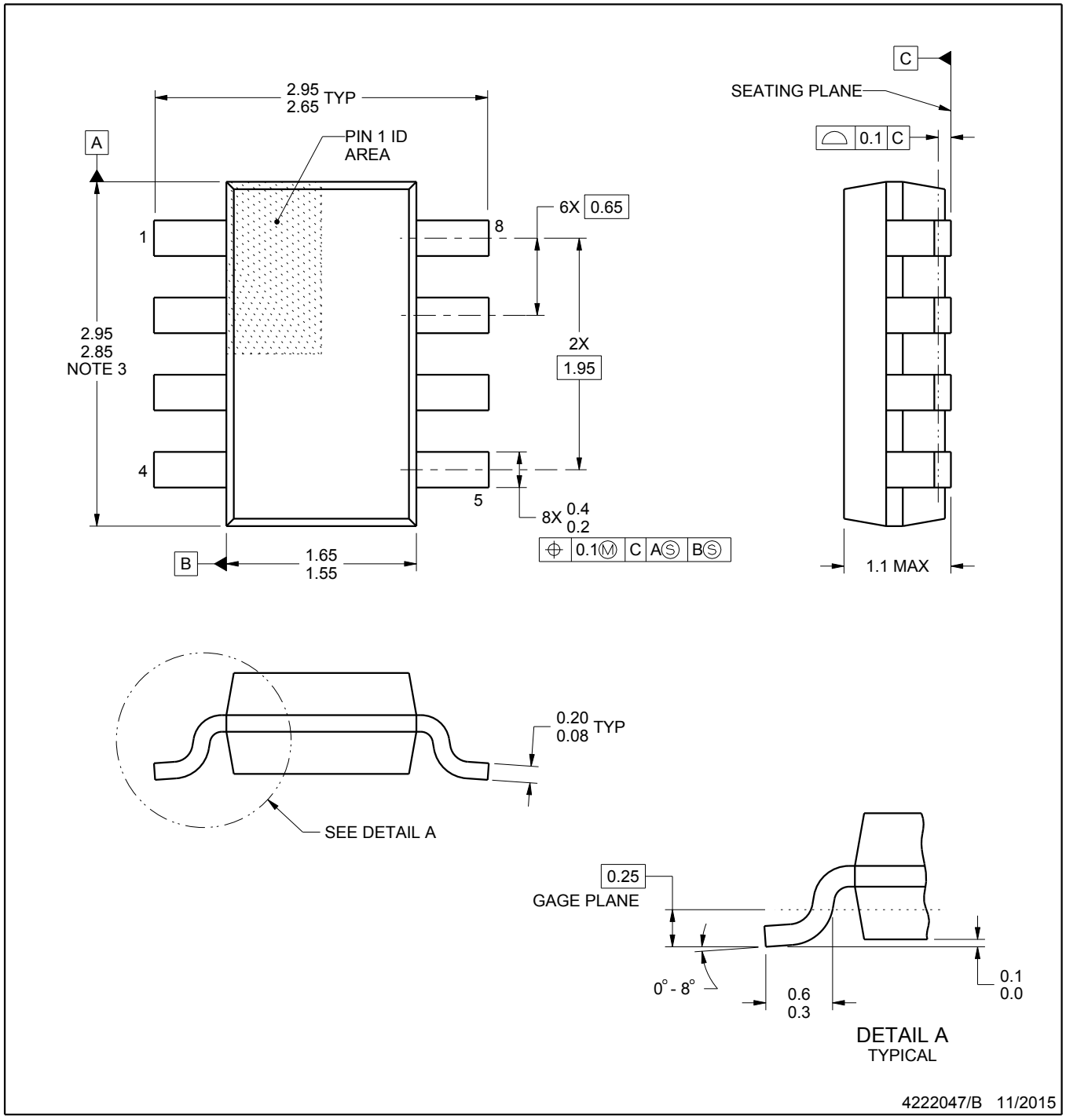
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA186A2IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
INA186A2IDDFT	SOT-23-THIN	DDF	8	250	210.0	185.0	35.0
INA186A2IYFDR	DSBGA	YFD	6	3000	220.0	220.0	35.0
INA186A3IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA186A3IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA186A3IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
INA186A3IDDFT	SOT-23-THIN	DDF	8	250	210.0	185.0	35.0
INA186A3IYFDR	DSBGA	YFD	6	3000	220.0	220.0	35.0
INA186A4IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA186A4IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA186A4IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
INA186A4IYFDR	DSBGA	YFD	6	3000	220.0	220.0	35.0
INA186A5IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA186A5IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA186A5IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
INA186A5IDDFT	SOT-23-THIN	DDF	8	250	210.0	185.0	35.0
INA186A5IYFDR	DSBGA	YFD	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DDF0008A

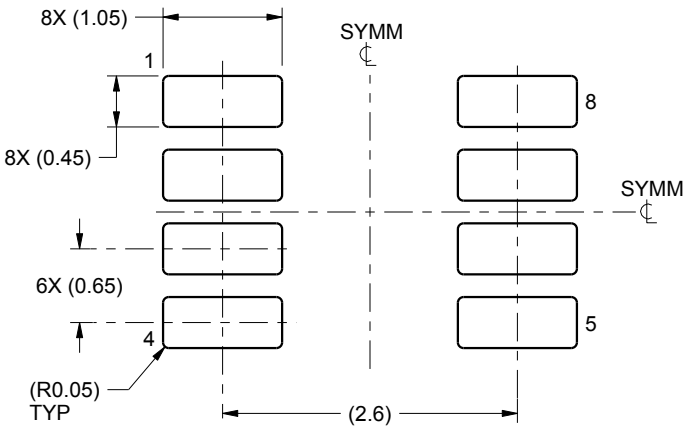
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

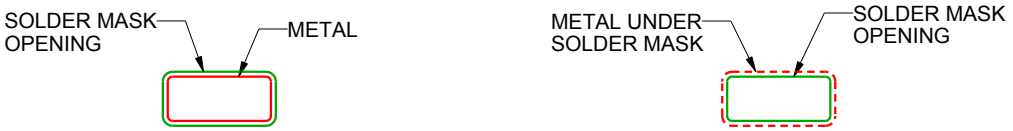


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

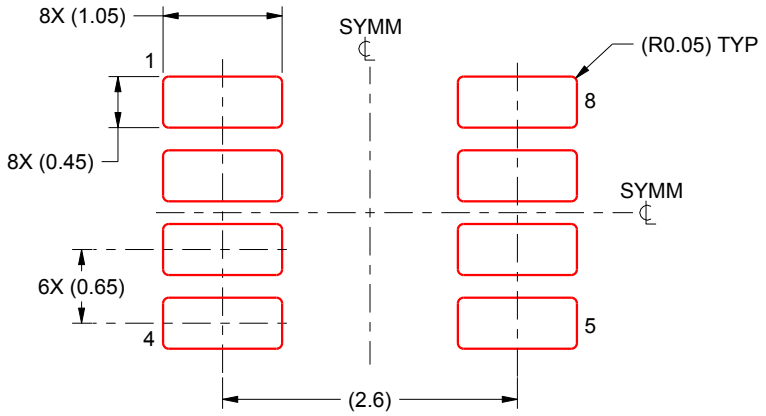
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

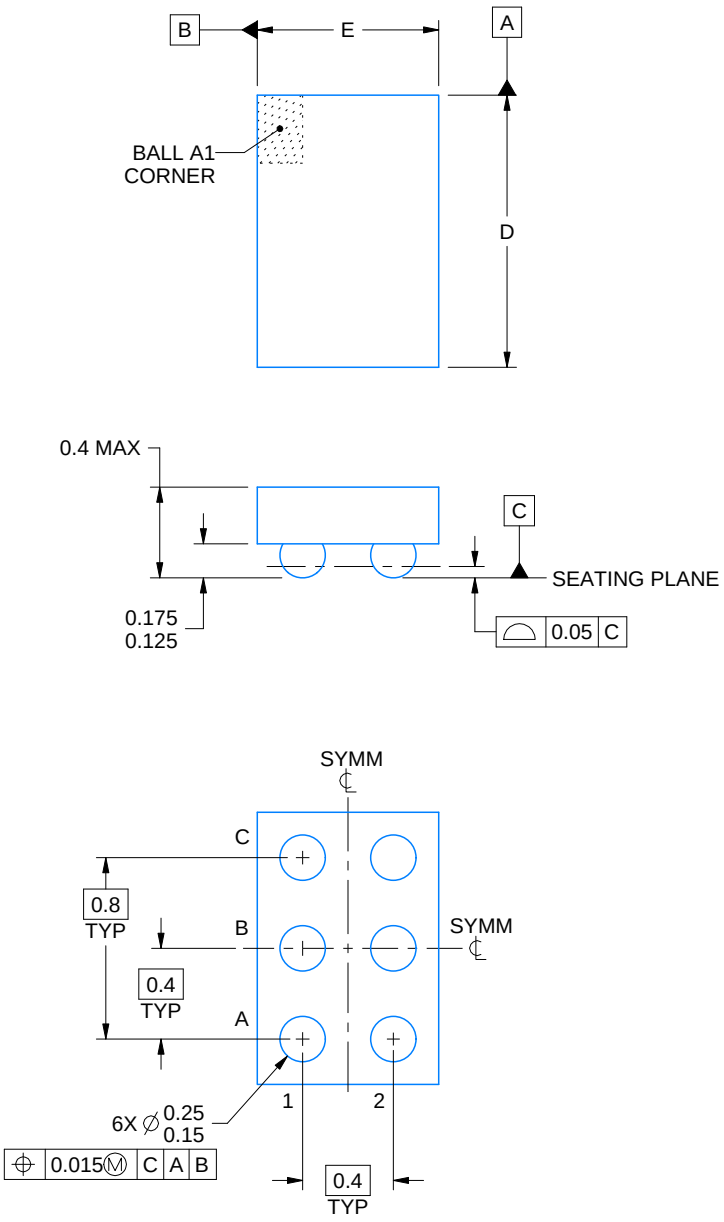
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

YFD0006

PACKAGE OUTLINE

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



4219510/A 11/2019

NOTES:

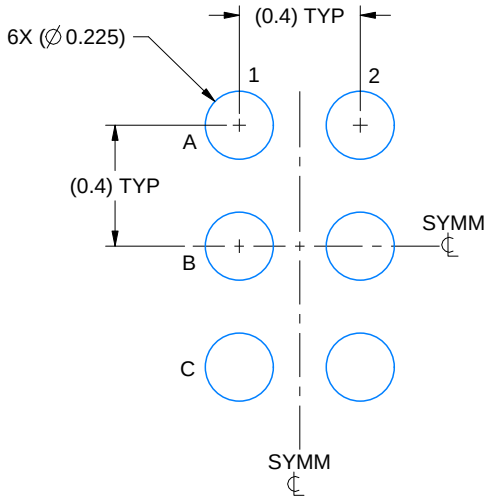
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

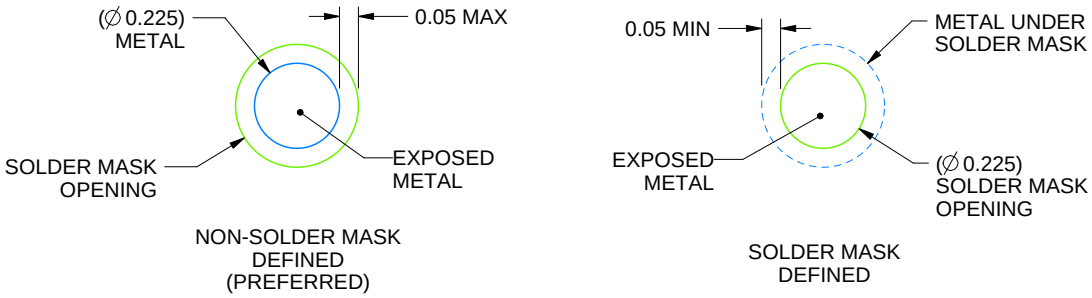
YFD0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219510/A 11/2019

NOTES: (continued)

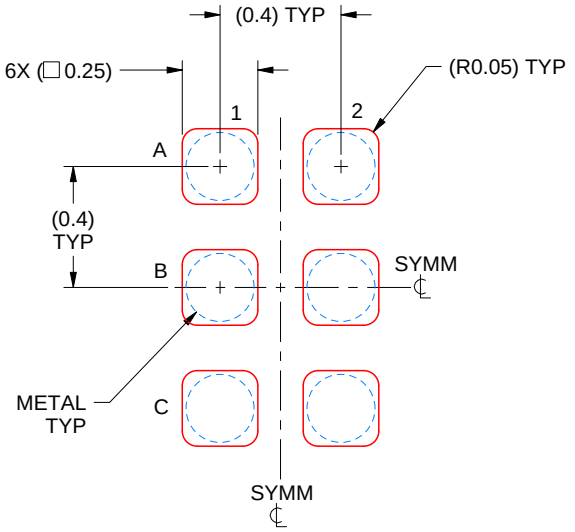
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFD0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



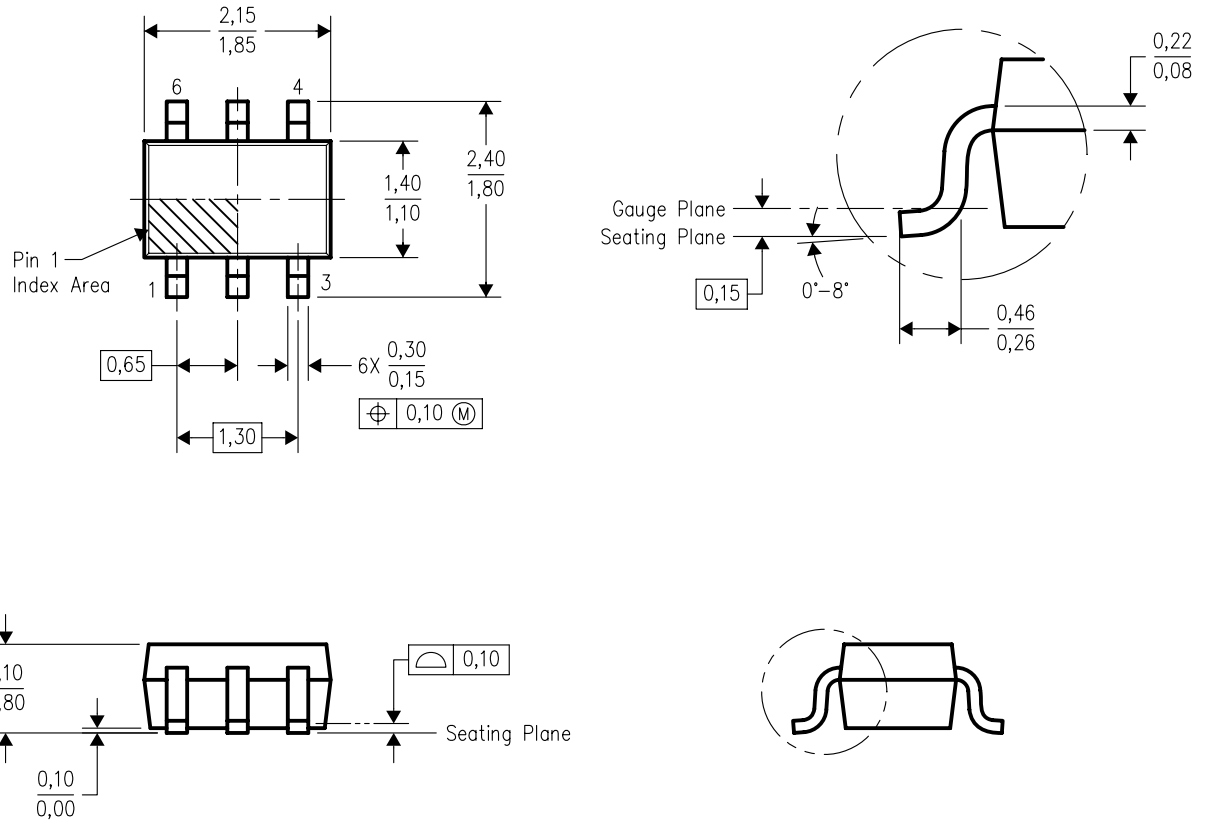
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219510/A 11/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

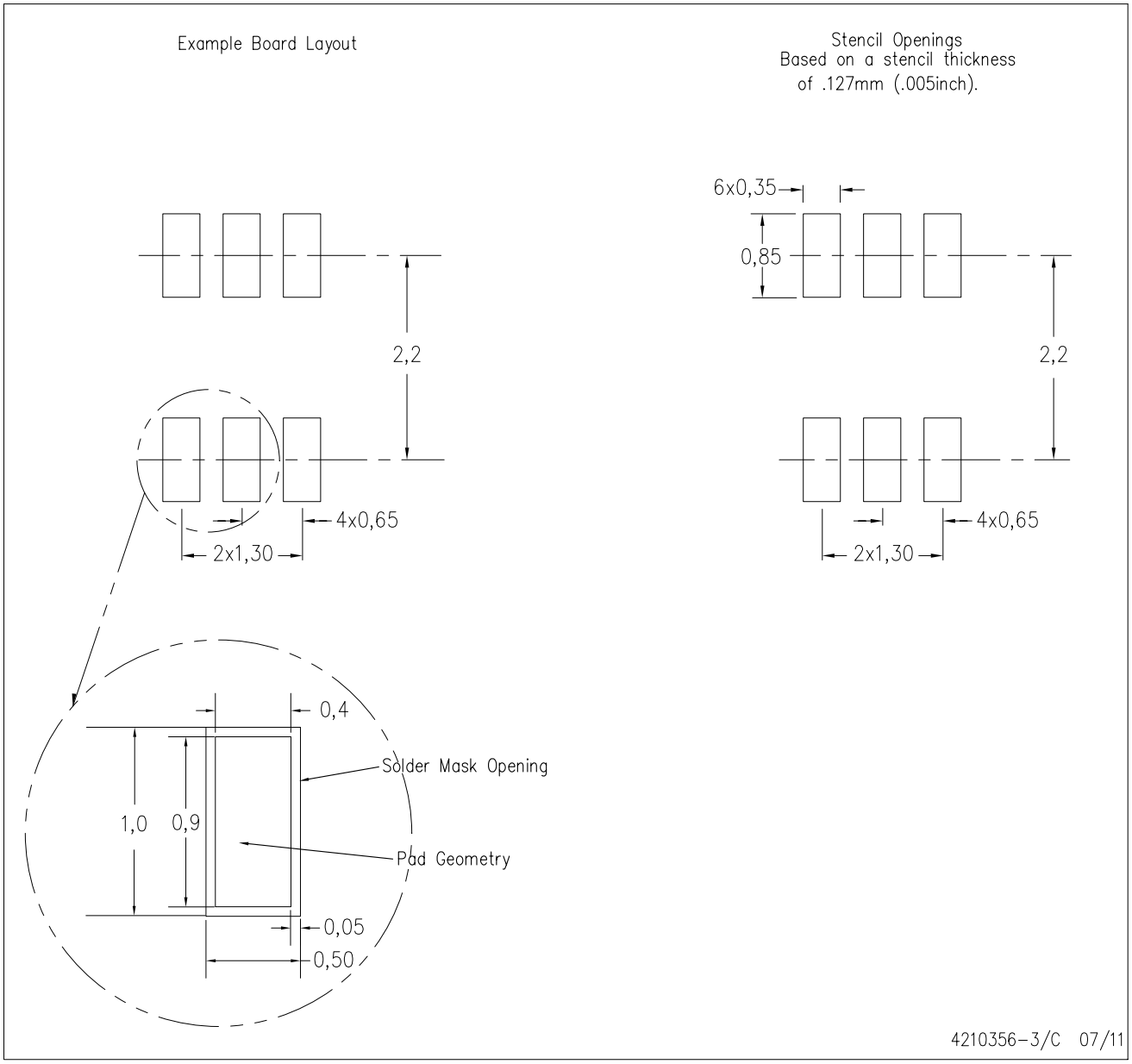
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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